Michael Steven Towns
2/8/18
CSC364
Homework 4

1. A computer memory system is addressable by a 28 bit address bus. The cache in this system supports direct addressing, with a 4-bit word, and 19-bit line, and a 5-bit Tag. Answer the following questions:
    a. What is the size of this memory system?
        i. **2^{28} bits = 32 MB**
    b. What is the size of cache in this system?
        i. **2^{19+5} bits = 2^{24} bits = 2 MB**
    c. How many words are in each cache line?
        i. **2^4 bits = 2 Bytes**
    d. What is the maximum number of different tags that can be loaded in this cache
        i. **2^5 = 32 tags**
2. Consider a machine with a byte addressable main memory of 2^{16} bytes and a block size of 8 bytes. Assume that a direct cache consisting of 32 lines is used with this machine.
    a. How is the 16-bit memory address divided into Tag, Line number, and byte number
        i. **8 bits for Tag, 5 bits for Line, 3 bits for words**
    b. Into what lines would bytes with each of the following addresses be stored:
        i. 0001 0001 0001 1011
            1. **Line 3**
        ii. 1100 0011 0011 0100
            1. **Line 6**
        iii. 1101 0000 0001 1101
            1. **Line 3**
        iv. 1010 1010 1010 1010
            1. **Line 21**
    c. How many total bytes of memory can be stored in the cache?
        i. **2^{5+3} = 2^8 = 256 bytes = 32 Bytes**
3. For the hexadecimal main memory addresses 444444, 999999, CCCCCC, show the following information:
    a. Tag, Line, and Word values for a direct mapped cache using the format of (8-bit tag, 14-bit line and 2-bit word)
        i. **Tag: 44, Line: 1111, Word: 0**
        ii. **Tag: 99, Line: 2666, Word: 1**
        iii. **Tag: CC, Line: 3333, Word: 0**
    b. For an associative-mapped cache, with a 22-bit tag, what are the tag and word values
        i. **Tag: 111111, Word: 0**
        ii. **Tag: 266666, Word: 1**
        iii. **Tag: 333333, Word: 0**

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4. Consider a CPU with the following specifications:
    - It can access 256 words of memory, each word being 8 bits wide. The CPU does this by outputting a 8-bit address on its output pins A[7…0] and reading in the 8-bit value from memory on its inputs D[7…0]
    - The CPU contains an 8-bit address register (AR), program counter (PC), accumulator (AC), data register (DR), and a 4-bit instruction register (IR).
    - The CPU must realize the following instruction set. Note that β is an 8-bit value stored in the location immediately following the instruction

    Write and Design the following parts for this CPU:
    a. RTL (Register Transfer language)
    b. Data path / Register Section

Instruction	**Instruction Code**	**Operation**
LD	0000XXXX β	AC <- M[β]
STI	0001XXXX β	β <- AC
ADD	0100XXXX β	AC <- AC + M[β]
JUMP	1000XXXX β	PC <- β
SKIP	1100XXXX	PC <- PC + 1
RST	1110XXXX	PC <- 0 , AC <- 0