OAI-222
(Static CMOS).

Group Number: 6

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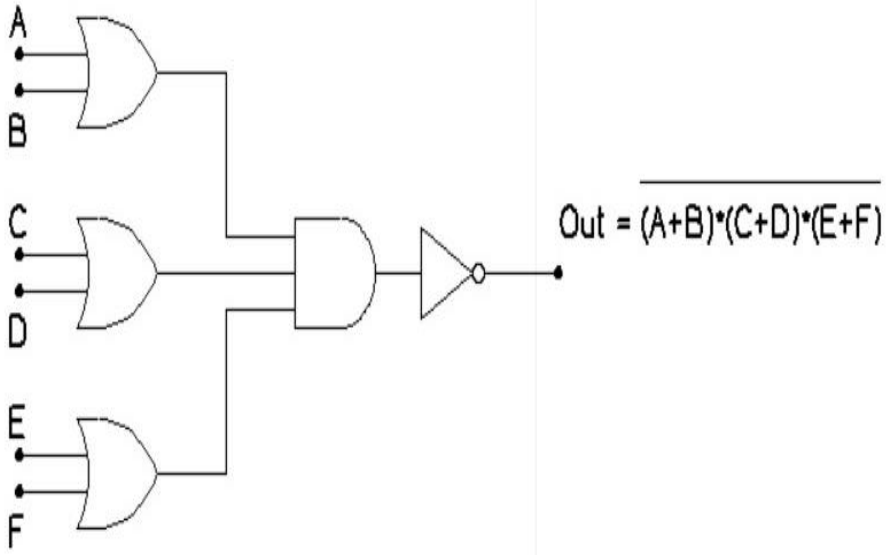
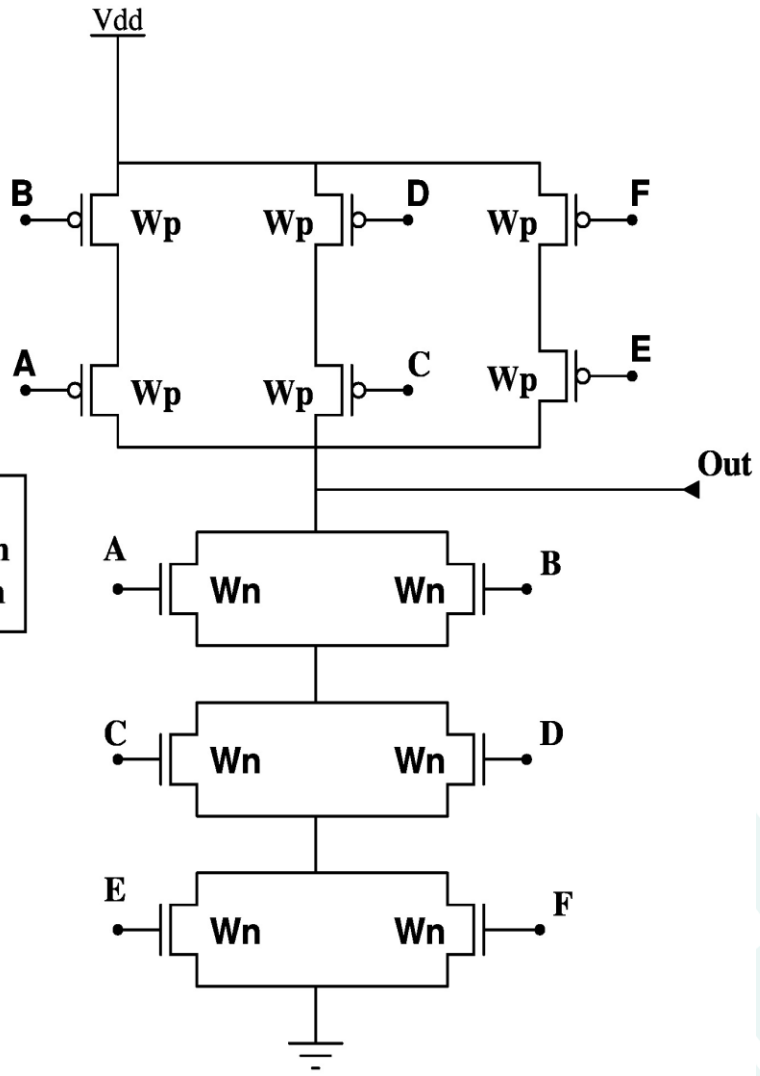
OAI-222 Implementation - Complex



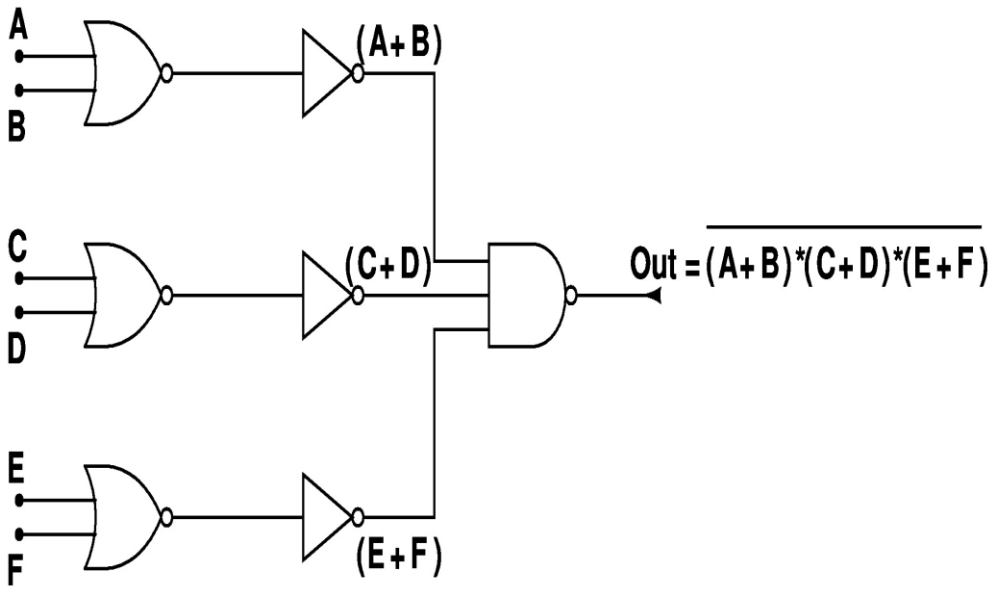
Xcircuit Schematic:

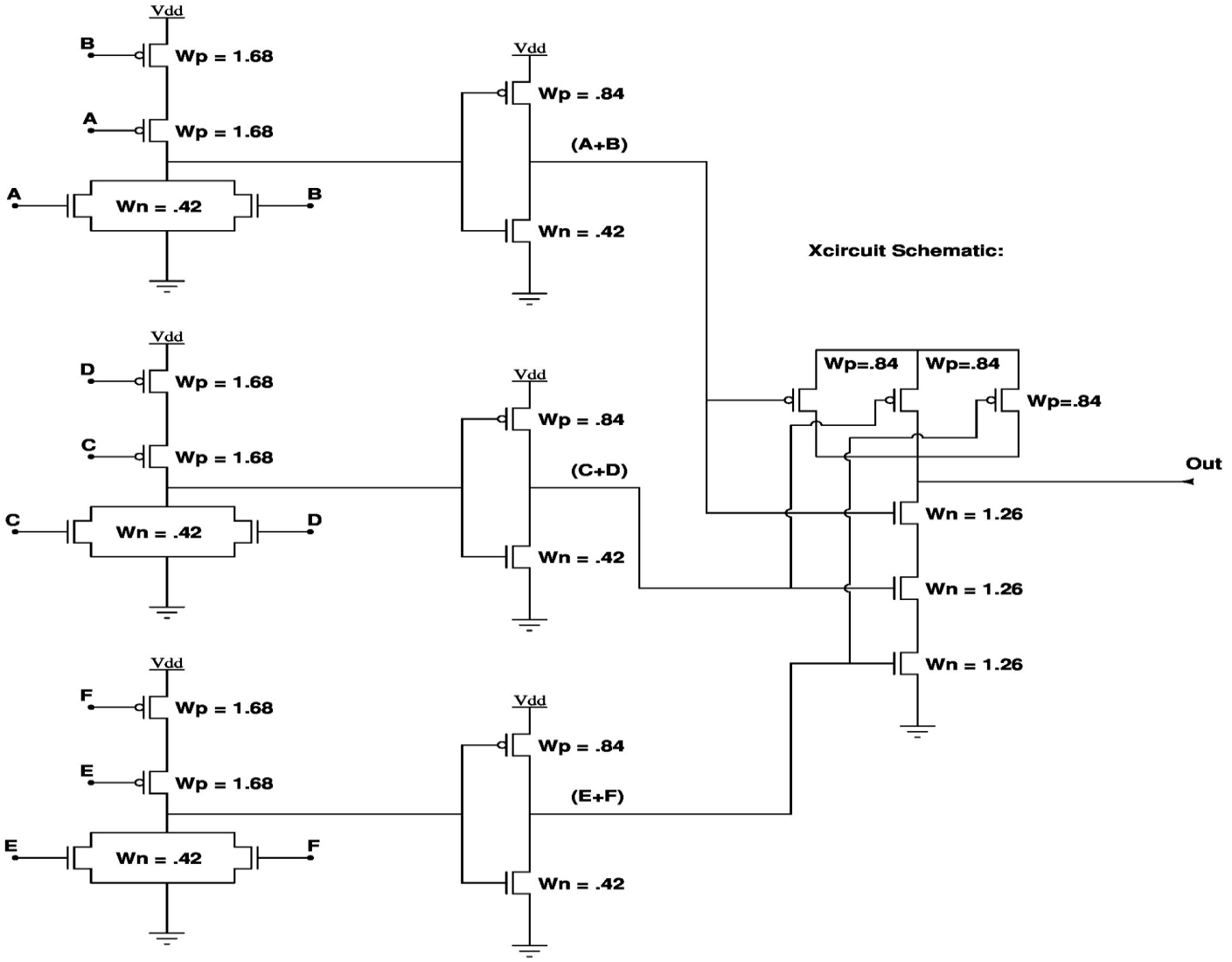


Sizing:
NMOS: Wn = 1.26 nm, L = .15 nm
PMOS: Wp = 1.68 nm, L = .15 nm

Complex implementation with sizing in reference to unit inverter.

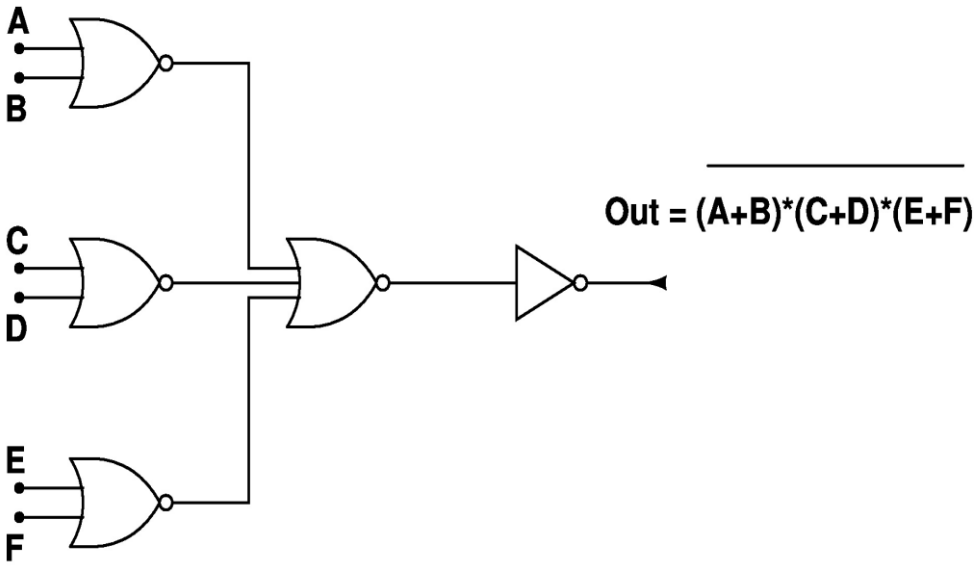
OAI-222 Implementation – Non Complex Basic



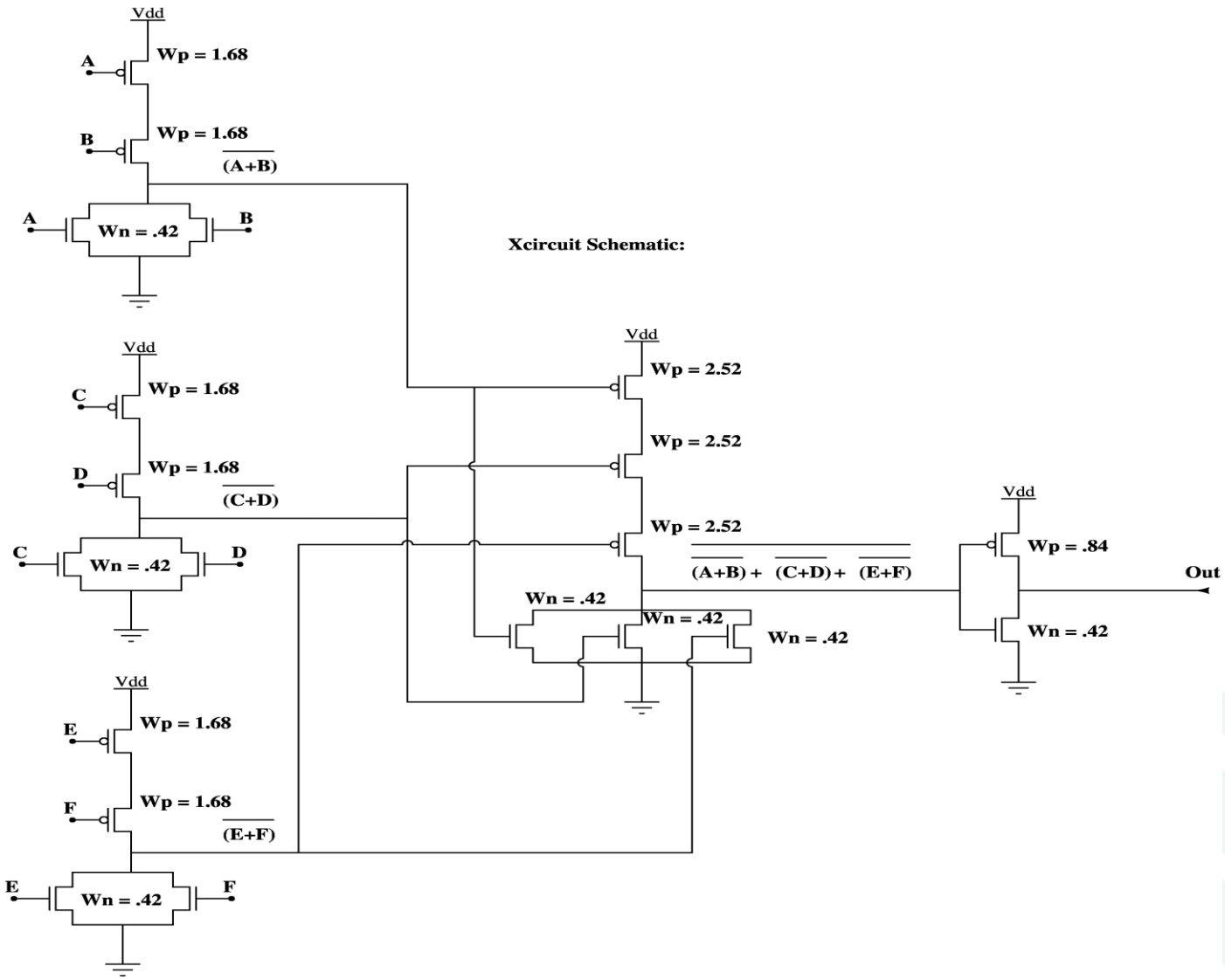


Non complex basic implementation with sizing in reference to unit inverter.

OAI-222 Implementation – Non Complex with Bubble Push

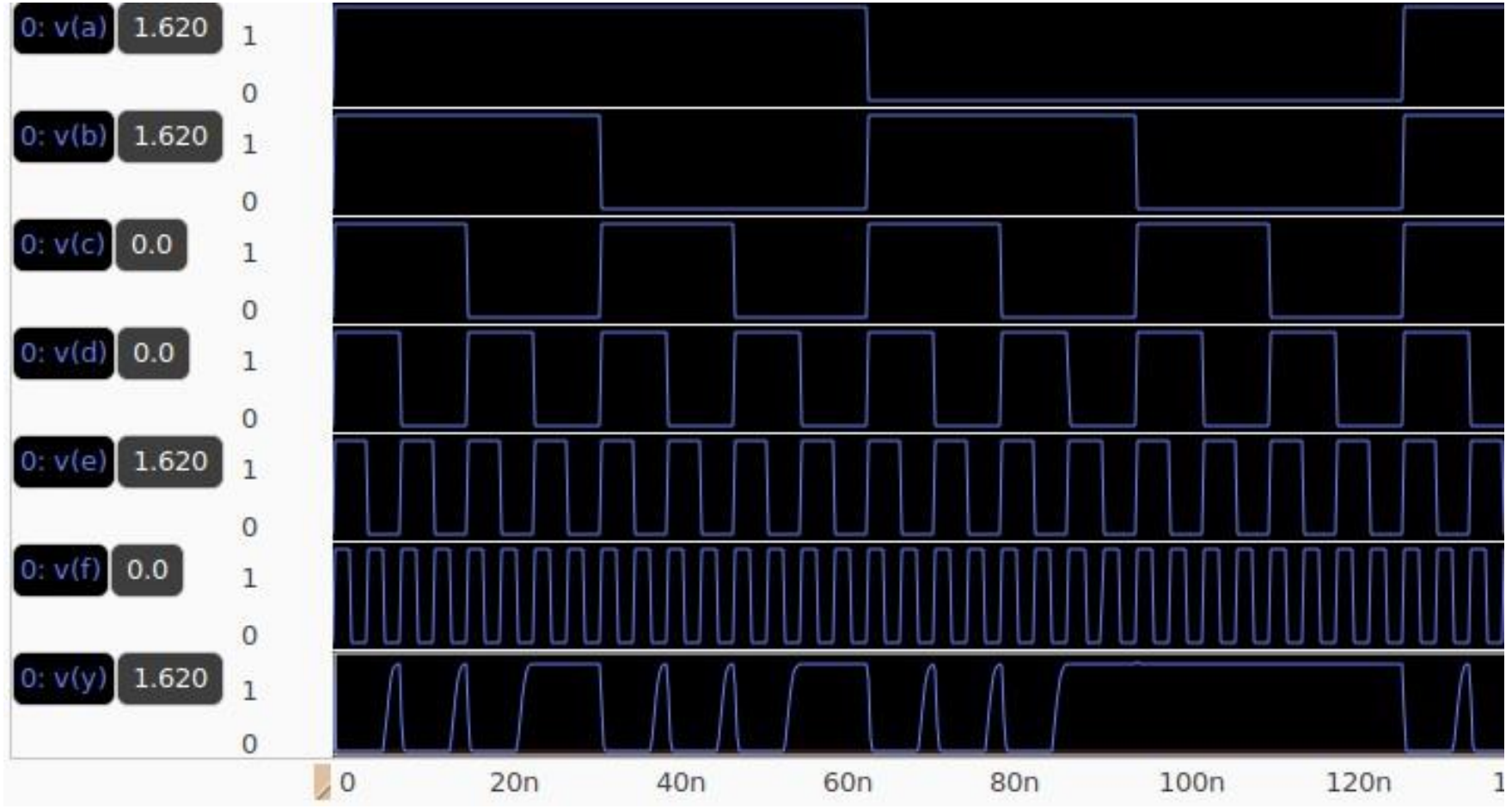


$$Out = \overline{(A+B)*(C+D)*(E+F)}$$



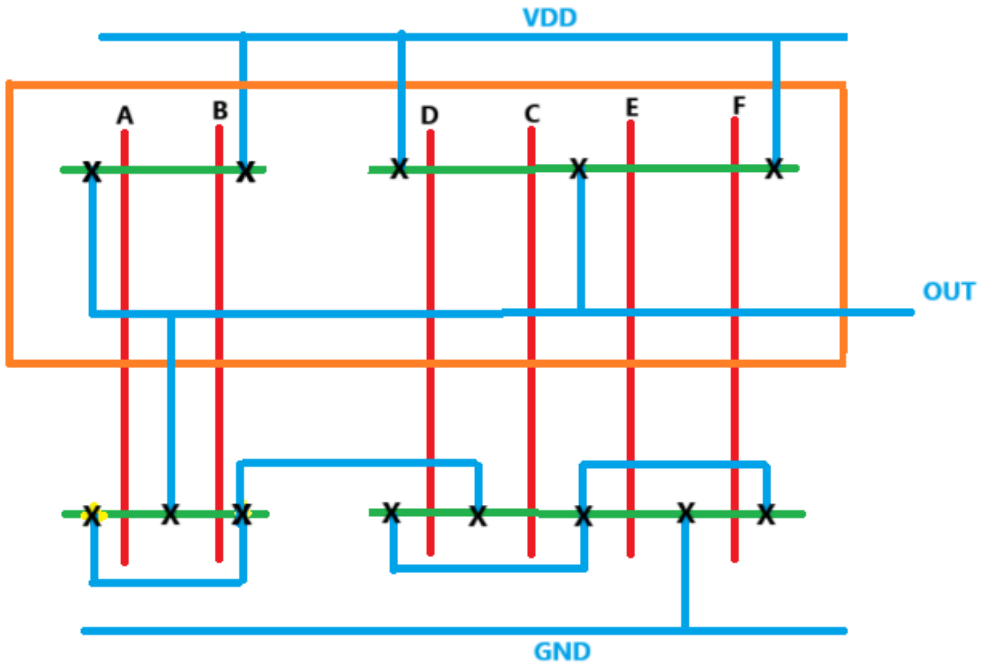
Non complex implementation with **bubble pushing** and sizing in reference to unit inverter.

Waveform:

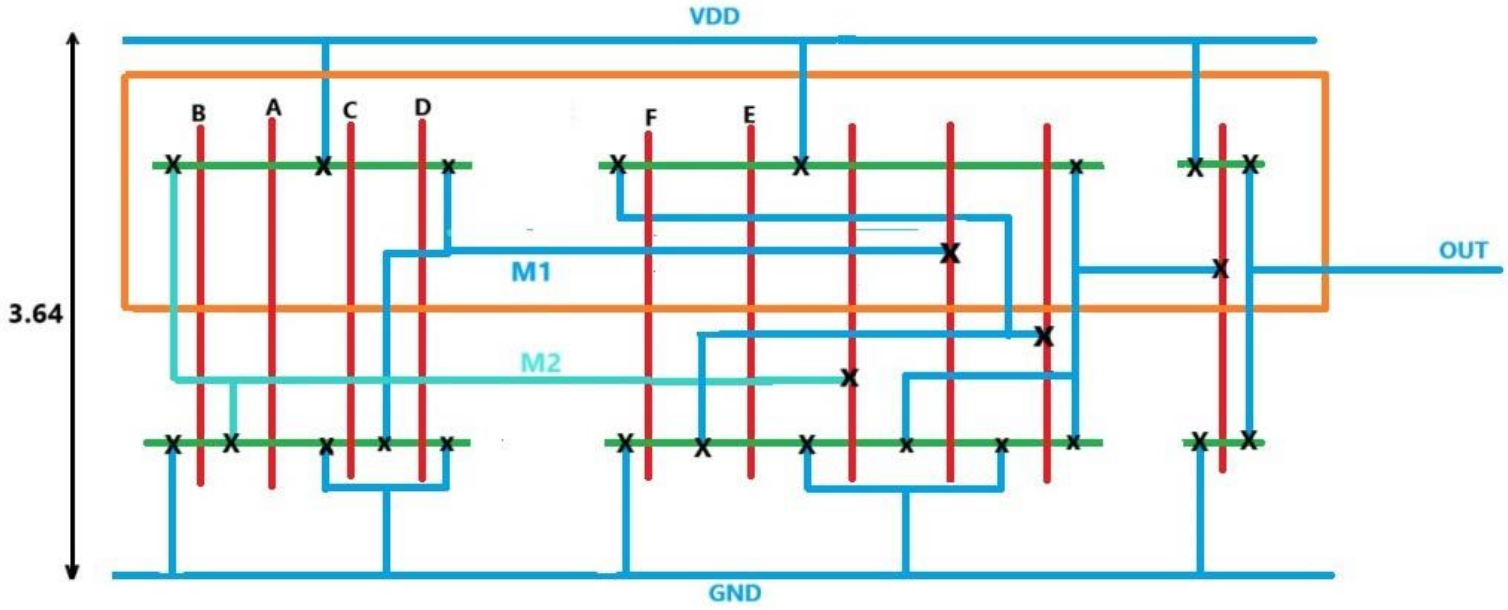


Inputs and output waveform

Stick Diagram:



Complex Stick Diagram



Non Complex With Bubble Pushing

PVT Conditions For Verification:

Verified for all input combinations $(2^6) = 64$

- Leakage:
  FF, 1.8V, 125C

- Dynamic Power:
  TT, 1.62V, 25C

- Delays:
  SS, 1.2V, -40C
  SS, 1.2V, 125C
  TT, 1.62, 25C
  FF, 1.8, -40C

Stimuli For Verification & Verification Plan:

Complex OAI (Pre-Layout)						
Parameters	Pre-Conditions	Stimuli	Delay (PVT: SS, 1.2V, -40C)	Delay (PVT: SS, 1.2V, 125C)	Delay (PVT: TT, 1.62V, 25C)	Delay (PVT: FF, 1.8V, -40C)
Rise Propagation Delay	A=0 C=D=E=F=1 B=1	A=0 C=D=E=F=1 B=0	1764.141 Ps	522.125 Ps	169.414 Ps	95.929 Ps
Fall Propagation Delay	A=B=C=D=1 E=0 F=0	A=B=C=D=1 E=0 F=1	475.062 Ps	589.826 Ps	185.560 Ps	117.487 Ps
Rise Contamination Delay	B=D=F=0 A=C=E=1	B=D=F=0 A=C=E=0	591.895 Ps	172.552 Ps	55.546 Ps	31.041 Ps
Fall Contamination Delay	C=D=E=F=1 A=B=0	C=D=E=F=1 A=B=1	296.680 Ps	350.097 Ps	116.535 Ps	73.972 Ps

Stimuli For Verification & Verification Plan:

Complex OAI (Post-Layout)						
Parameters	Pre-Conditions	Stimuli	Delay (PVT: SS, 1.2V, -40C)	Delay (PVT: SS, 1.2V, 125C)	Delay (PVT: TT, 1.62V, 25C)	Delay (PVT: FF, 1.8V, -40C)
Rise Propagation Delay	A=0 C=D=E=F=1 B=1	A=0 C=D=E=F=1 B=0	1817.659 Ps	537.331 Ps	174.47 Ps	98.902 Ps
Fall Propagation Delay	A=B=C=D=1 E=0 F=0	A=B=C=D=1 E=0 F=1	489.829 Ps	607.498 Ps	191.154 Ps	120.98 Ps
Rise Contamination Delay	B=D=F=0 A=C=E=1	B=D=F=0 A=C=E=0	612.742 Ps	178.582 Ps	57.632 Ps	32.267 Ps
Fall Contamination Delay	C=D=E=F=1 A=B=0	C=D=E=F=1 A=B=1	306.656 Ps	361.416 Ps	119.941 Ps	76.186 Ps

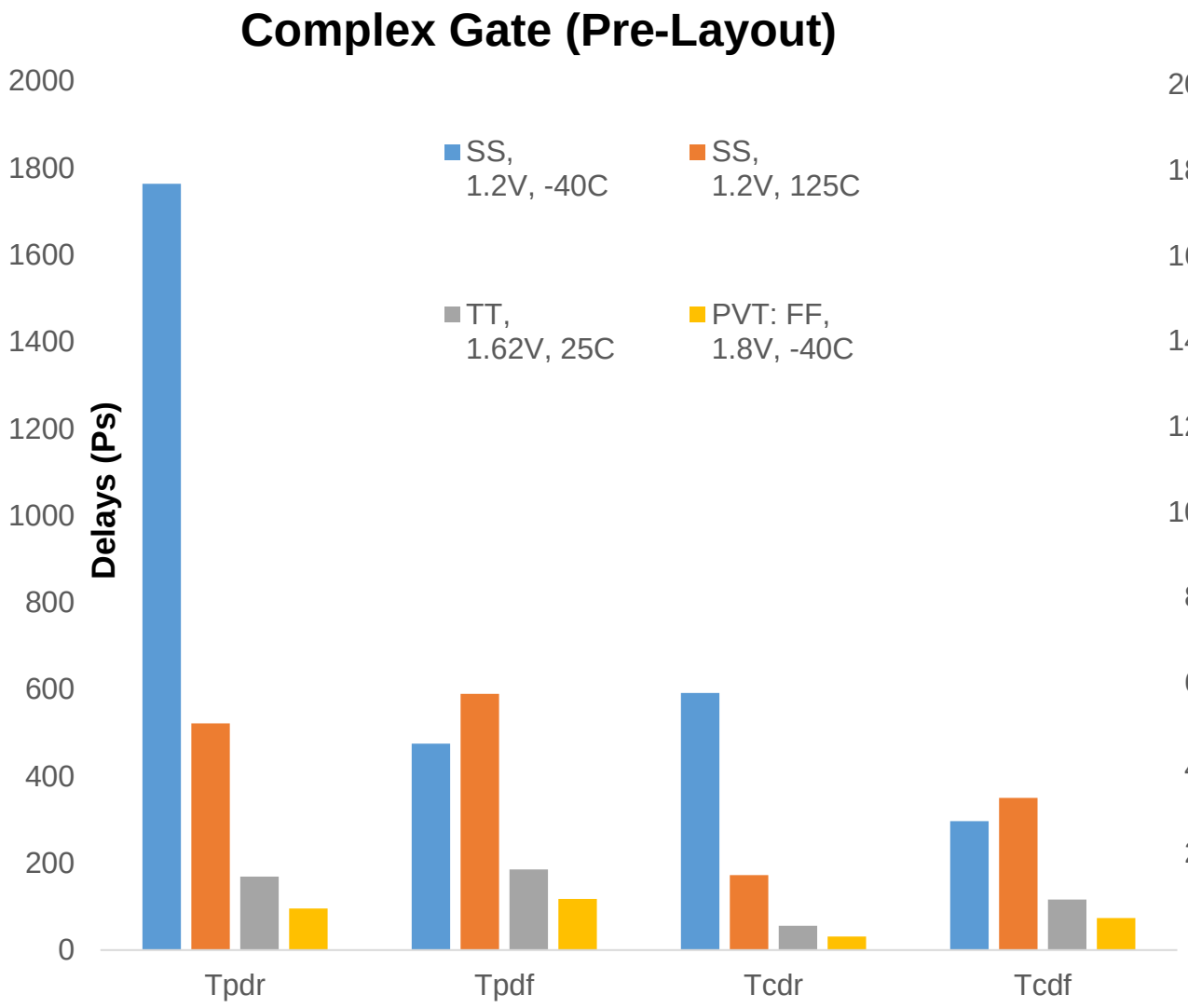
Stimuli For Verification & Verification Plan:

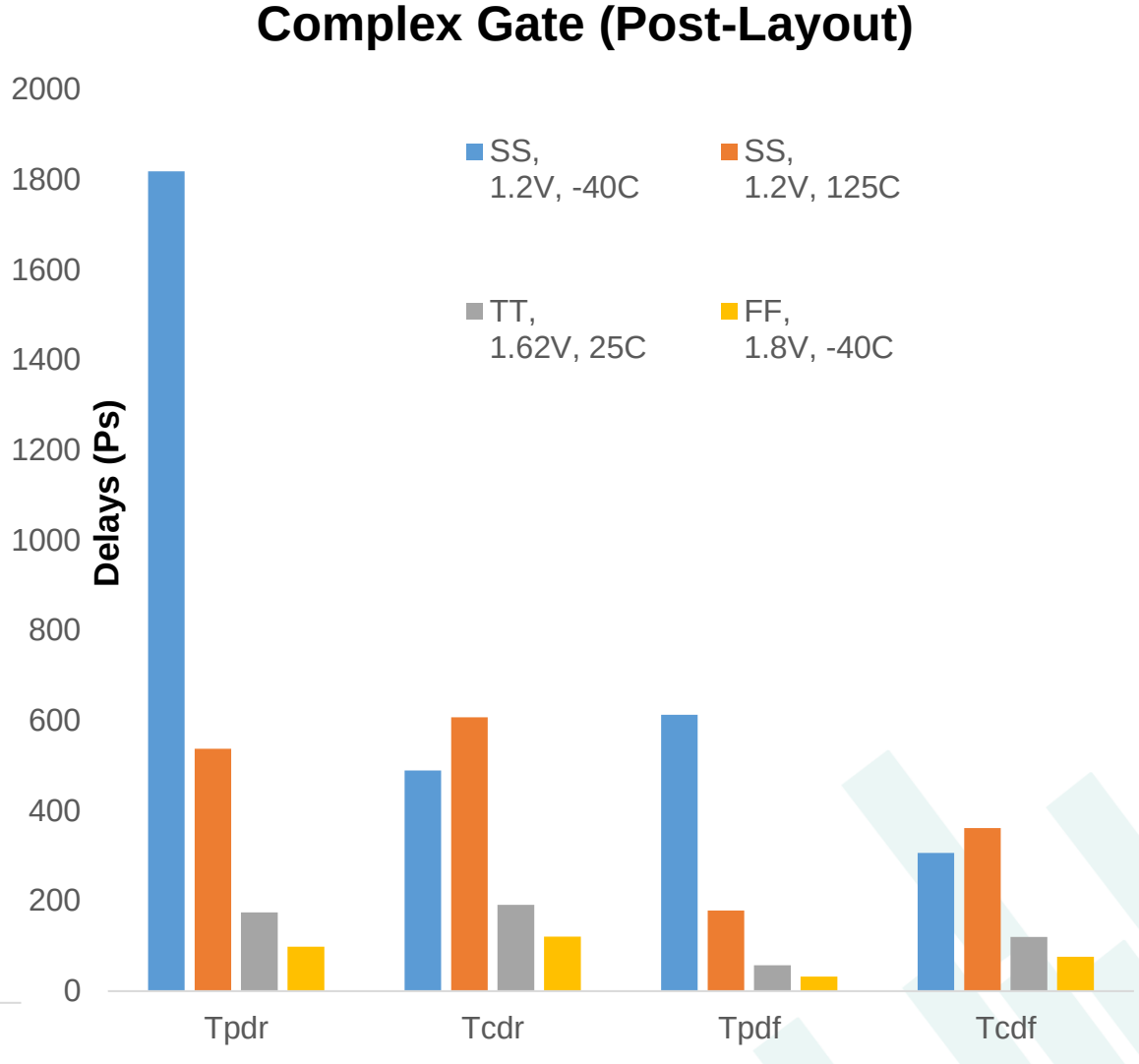
Non-Complex OAI (Pre-Layout)						
Parameters	**Pre-Conditions**	**Stimuli**	**Delay (PVT: SS, 1.2V, -40C)**	**Delay (PVT: SS, 1.2V, 125C)**	**Delay (PVT: TT, 1.62V, 25C)**	**Delay (PVT: FF, 1.8V, -40C)**
Rise Propagation Delay	B=D=F=0 C=E=1 A=1	B=D=F=0 C=E=1 A=0	1495.252 Ps	614.077 Ps	206.945 Ps	118.367 Ps
Fall Propagation Delay	B=D=F=0 C=E=1 A=0	B=D=F=0 C=E=1 A=1	1972.882 Ps	882.294 Ps	329.837 Ps	203.633 Ps
Rise Contamination Delay	A=B=C=1 D=E=F=1	A=B=C=0 D=E=F=0	1379.219 Ps	495.942 Ps	164.663 Ps	93.101 Ps
Fall Contamination Delay	A=B=C=0 D=E=F=0	A=B=C=1 D=E=F=1	1938.711 Ps	815.835 Ps	306.985 Ps	193.046 Ps

Stimuli For Verification & Verification Plan:

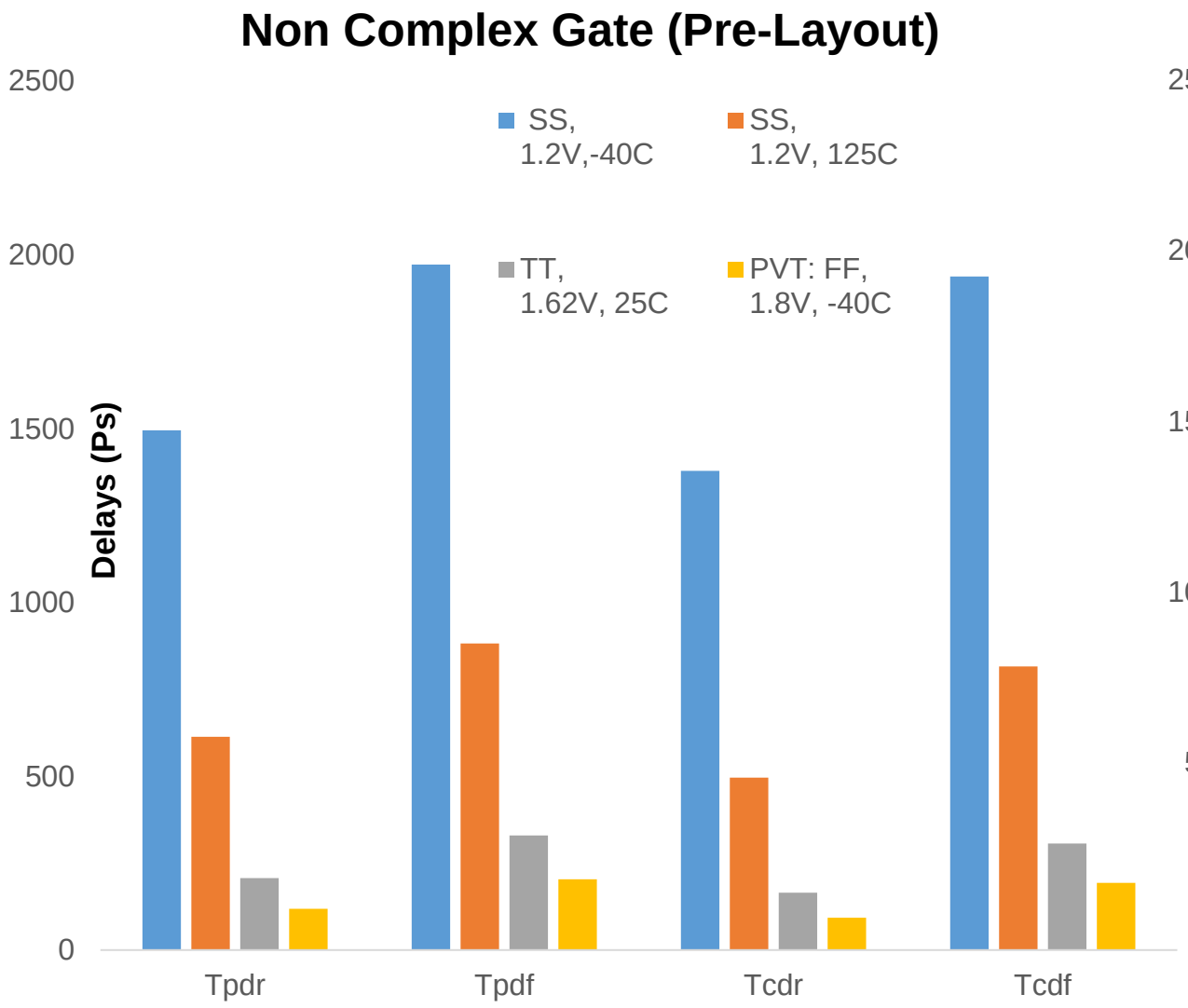
Non-Complex OAI (Post-Layout)						
Parameters	Pre-Conditions	Stimuli	Delay (PVT: SS, 1.2V, -40C)	Delay (PVT: SS, 1.2V, 125C)	Delay (PVT: TT, 1.62V, 25C)	Delay (PVT: FF, 1.8V, -40C)
Rise Propagation Delay	B=D=F=0 C=E=1 A=1	B=D=F=0 C=E=1 A=0	1669.151 Ps	669.105 Ps	227.015 Ps	130.374 Ps
Fall Propagation Delay	B=D=F=0 C=E=1 A=0	B=D=F=0 C=E=1 A=1	2078.939 Ps	924.096 Ps	344.721 Ps	212.278 Ps
Rise Contamination Delay	A=B=C=1 D=E=F=1	A=B=C=0 D=E=F=0	1490.11 Ps	529.488 Ps	175.77 Ps	98.713 Ps
Fall Contamination Delay	A=B=C=0 D=E=F=0	A=B=C=1 D=E=F=1	2102.620 Ps	860.788 Ps	321.208 Ps	201.008 Ps

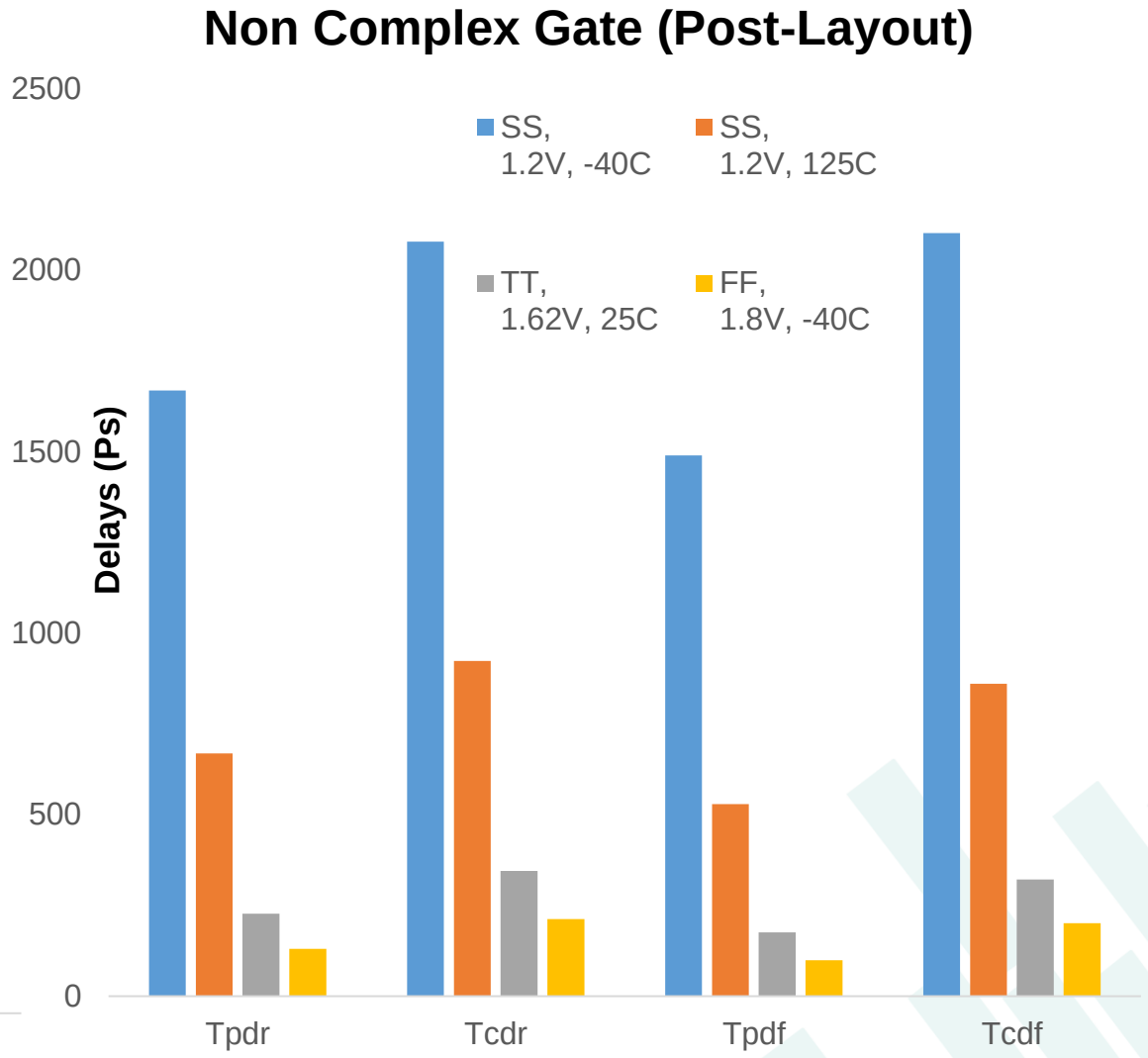
Delay Trends:



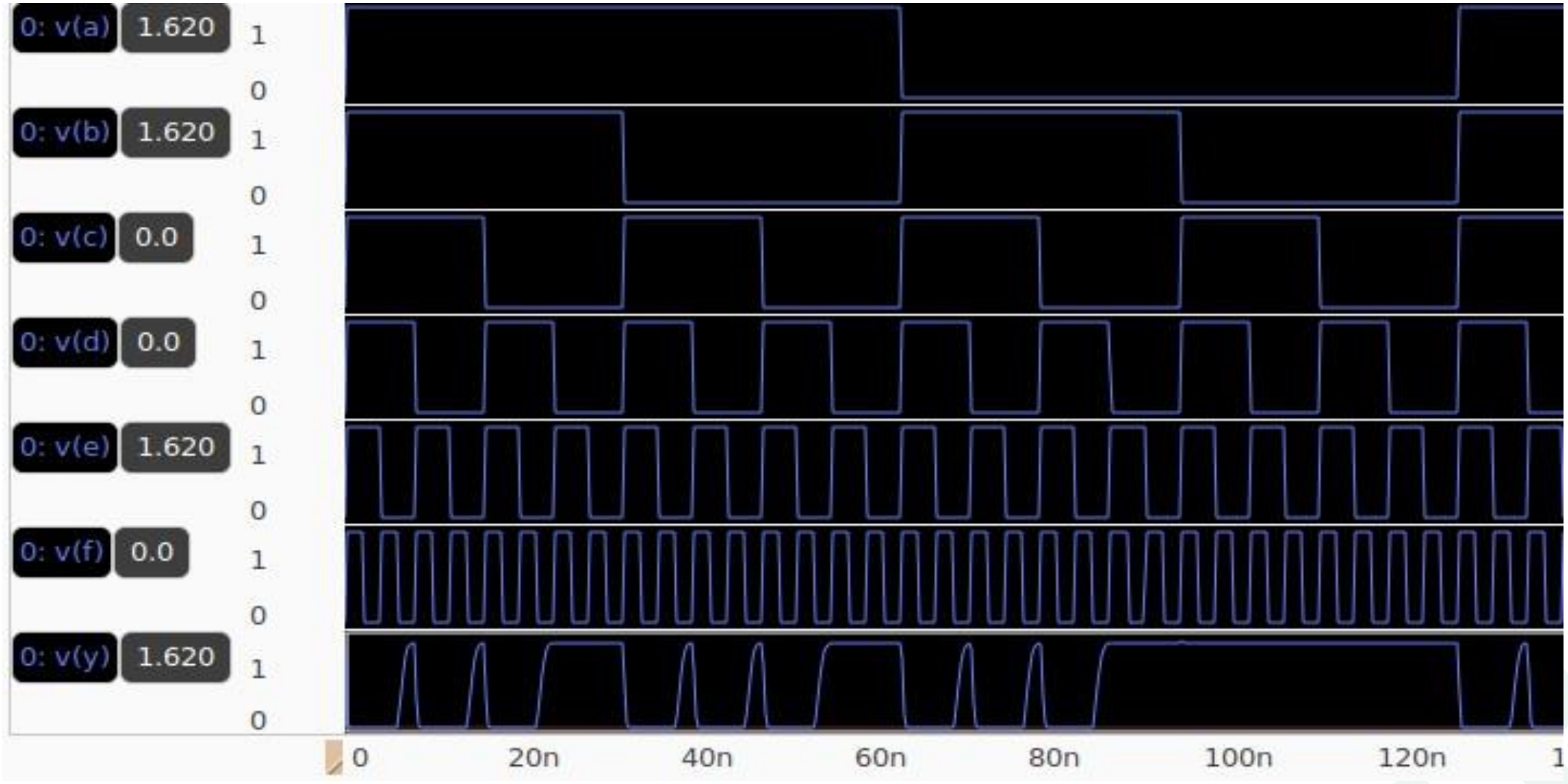


Delay Trends:



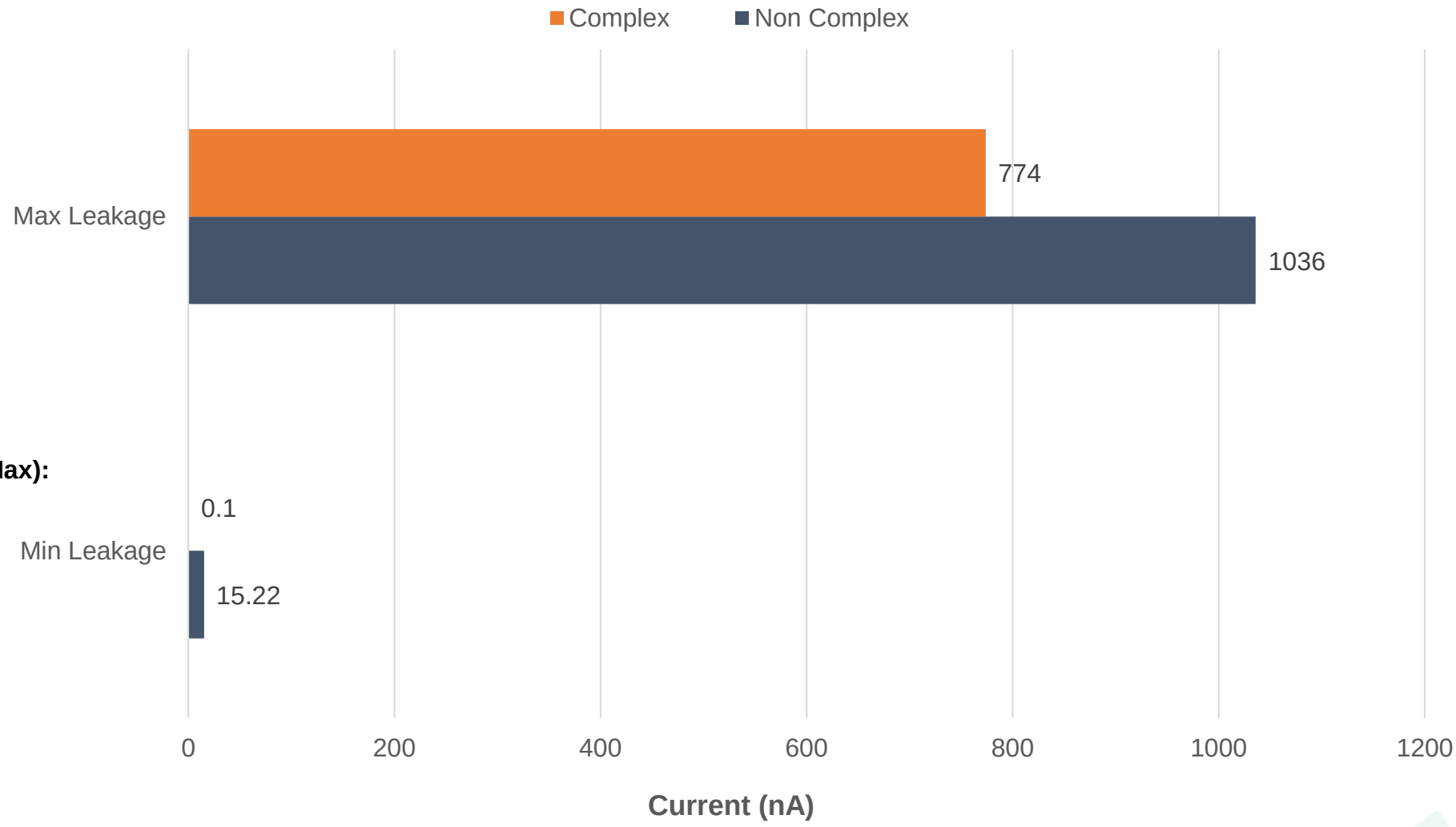


Waveform:



Input and Output Waveform

Leakage Complex vs Non Complex (Post Layout):



Stimuli-

Complex (Max):
101010

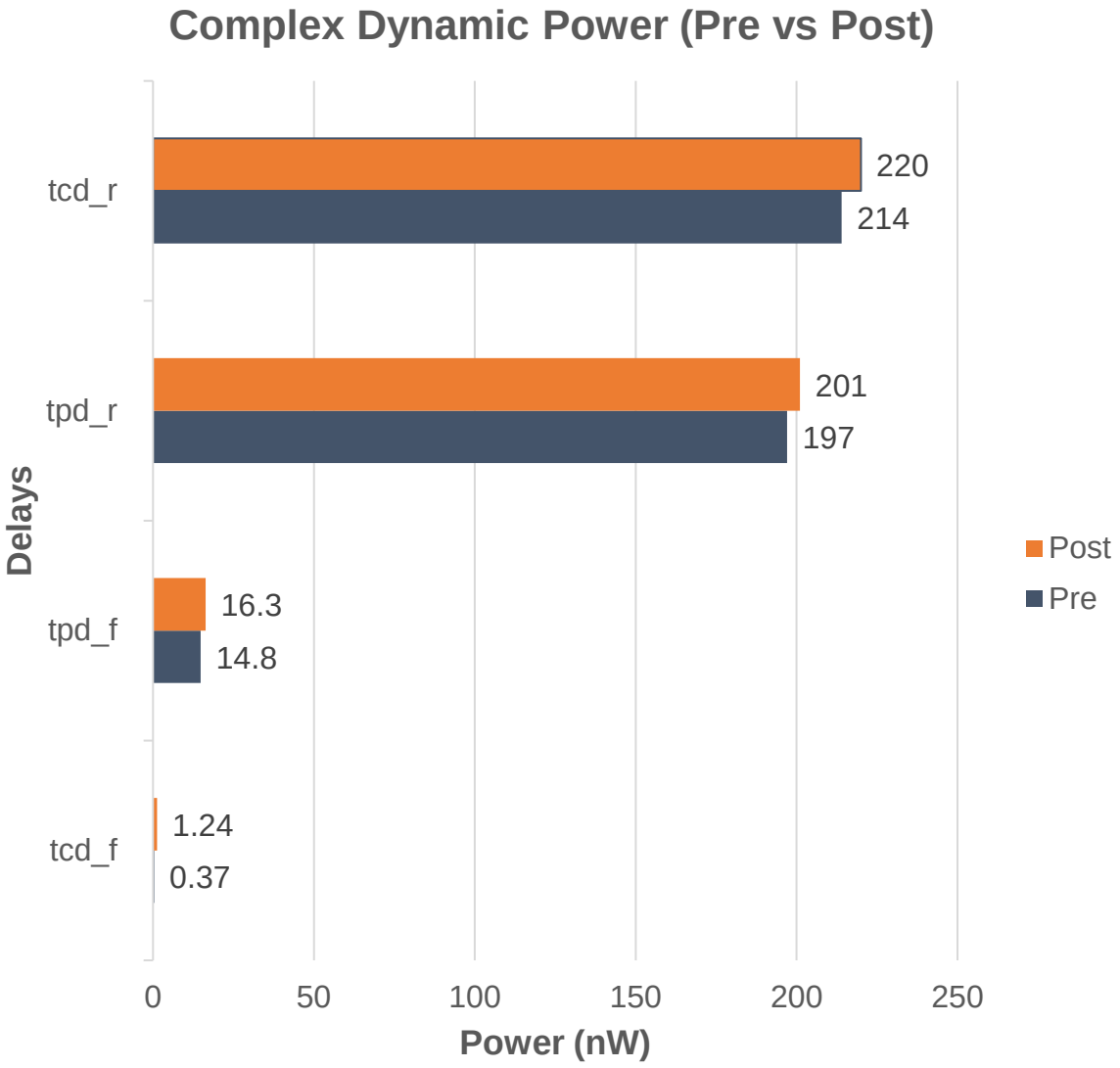
Non Complex (Max):
010101

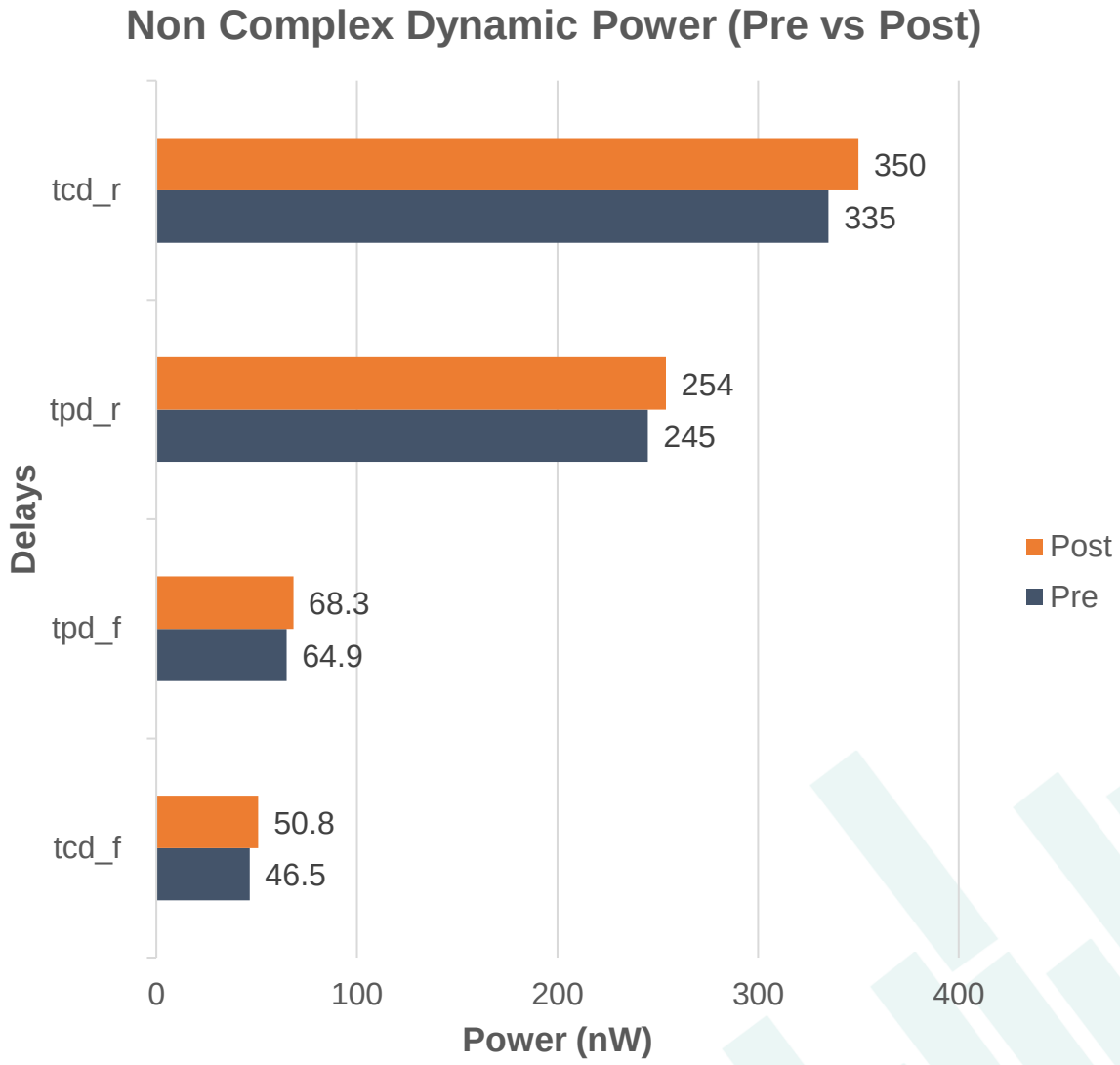
Stimuli-

Complex (Min):
000000

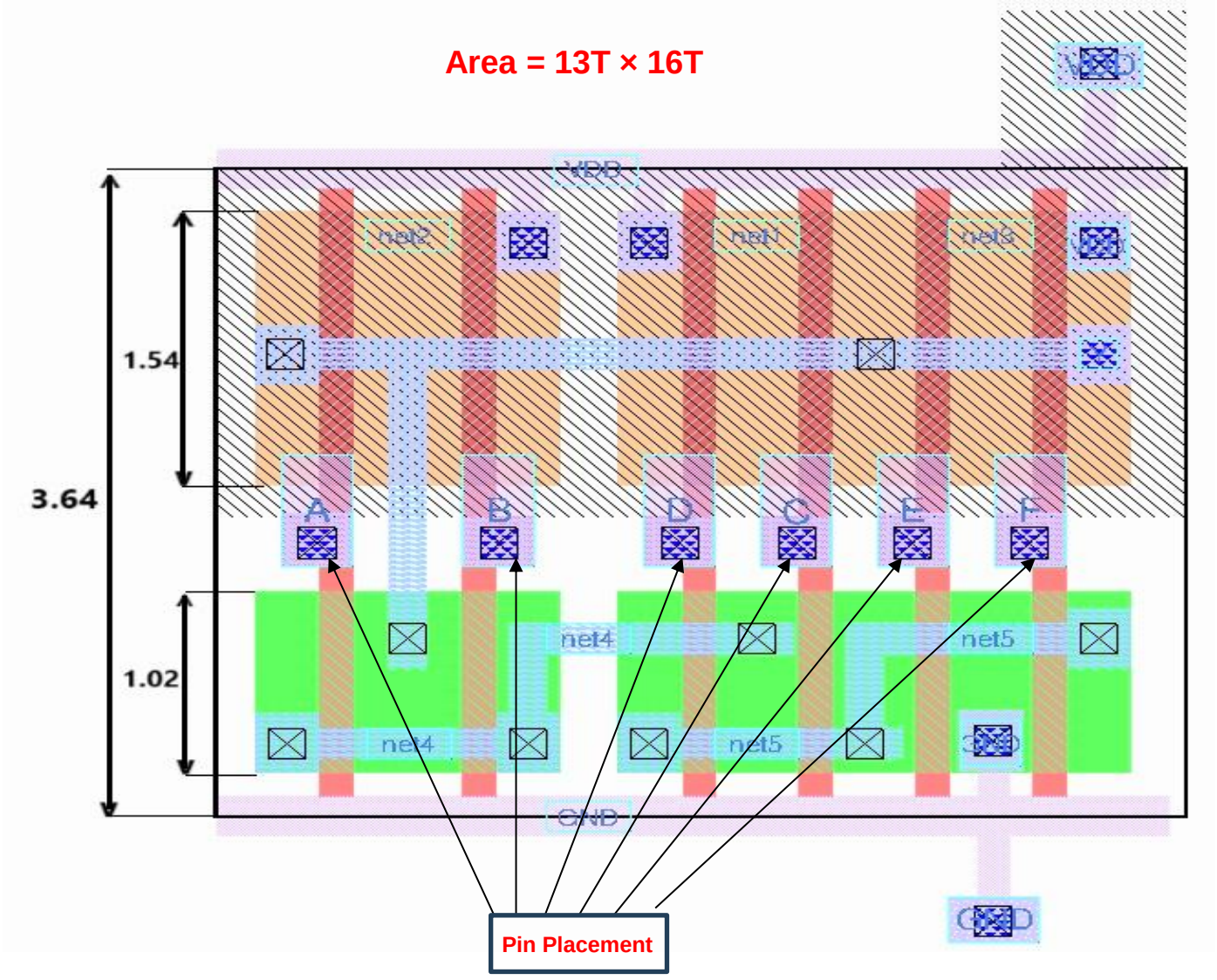
Non Complex (Min):
000000

Dynamic Power Comparison:





Layout – Complex Gate:



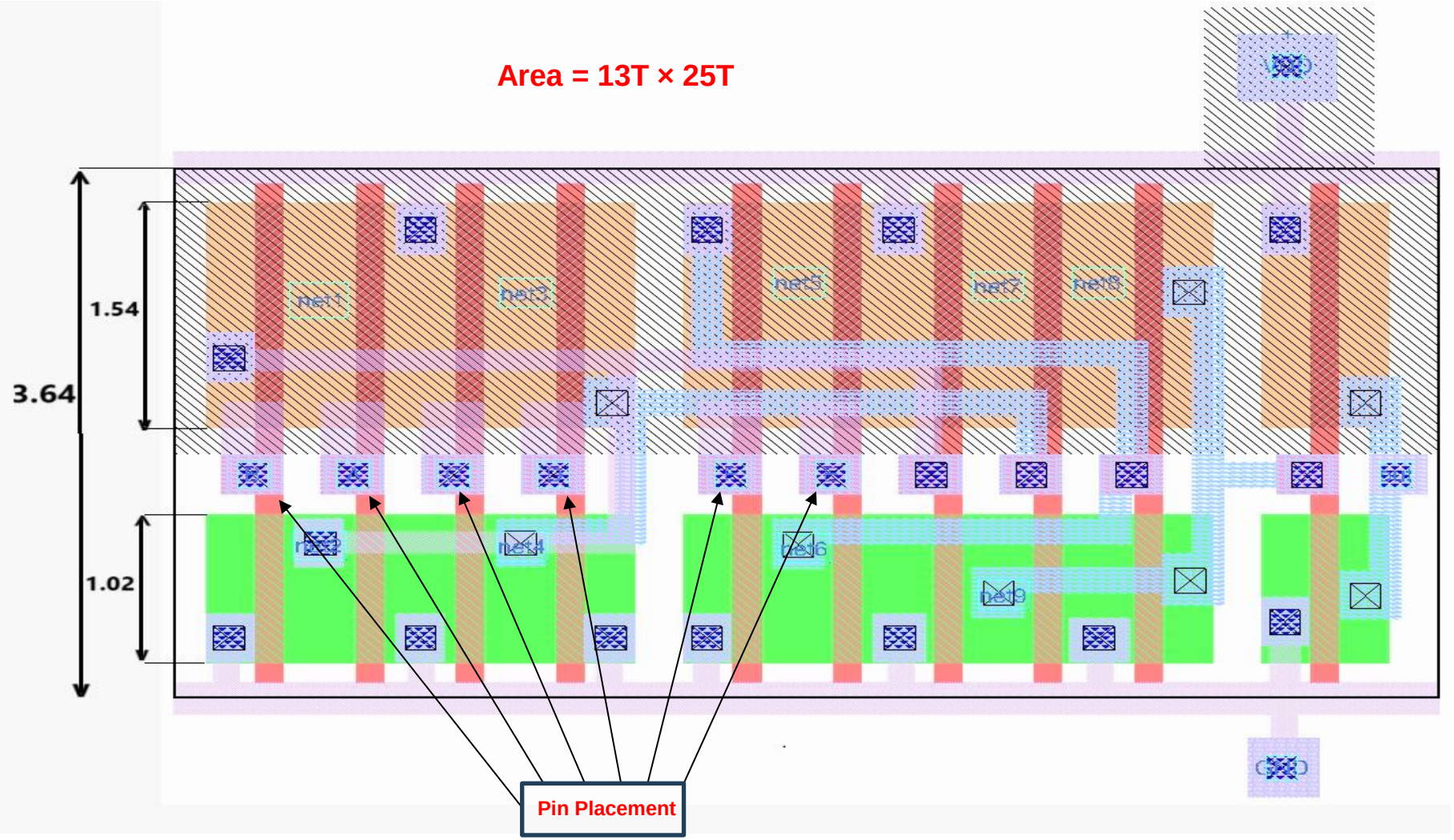
LVS Clean:

```
Contents of circuit 1:  Circuit: 'aoi_complex.spice'
Circuit aoi_complex.spice contains 12 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   6
  Class: sky130_fd_pr__pfet_01v8 instances:   6
Circuit contains 14 nets.
Contents of circuit 2:  Circuit: 'aoi_complex_xschem.spice'
Circuit aoi_complex_xschem.spice contains 12 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   6
  Class: sky130_fd_pr__pfet_01v8 instances:   6
Circuit contains 14 nets.

Circuit 1 contains 12 devices, Circuit 2 contains 12 devices.
Circuit 1 contains 14 nets,    Circuit 2 contains 14 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
(netgen) 2 %
```

Layout – Non Complex Gate (Bubble Push):



LVS Clean:

```
Contents of circuit 1:  Circuit: 'project.spice'
Circuit project.spice contains 20 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  10
  Class: sky130_fd_pr__pfet_01v8 instances:  10
Circuit contains 18 nets.
Contents of circuit 2:  Circuit: 'schematic-project.spice'
Circuit schematic-project.spice contains 20 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  10
  Class: sky130_fd_pr__pfet_01v8 instances:  10
Circuit contains 18 nets.

Circuit 1 contains 20 devices, Circuit 2 contains 20 devices.
Circuit 1 contains 18 nets,    Circuit 2 contains 18 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
(netgen) 2 % lvs project.spice schematic-project.spice
```

Results:

Circuits → Parameters ↓	Complex (Pre Layout)	Non Complex (Pre Layout)	Complex (Post Layout)	Non Complex (Post Layout)
Area (um^2)	------	------	16.3072	25.48
Maximum Delay (Ps)	1764.141	1972.882	1817.659	2102.620
Minimum Delay (Ps)	31.041	93.101	32.267	98.713
Max Dynamic Power (nW)	214	314	220	350
Min Dynamic Power (nW)	0.37	46.5	1.24	50.8
Max Leakage Power (nW)	------	------	1393	1866
Min Leakage Power (nW)	------	------	0.18	27.4

Conclusion:

Power:

- In pre-layout, the observed dynamic power in non-complex OAI is approximately 1.5 times more in comparison with complex OAI.
- In post-layout, the observed dynamic power in non-complex OAI is approximately 1.6 times more in comparison with complex OAI.

Performance:

Overall, complex OAI has lower delays as compared with non-complex OAI.

Area:

Ratio of layout of non-complex OAI to complex OAI is **1.5625**

(**36%** Improvement)**.**