Design of 1R/1W 8T SRAM Cell

ECE-611 (Memory Design and Testing)

Group - 1

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Design Specifications

Given specification :

- Vmin (read port) = 0.81V
- Vmin (write port) = 1.08V when mux 16
- Vmin (write port) = 0.81V when mux 1 with WL Boost
  Icell = 100uA at wc, 1.08V

Understanding of Design Specifications

For MUX_1:

- VDD applied to bitcell is 0.81 V, precharge should charge BL, BLB & RBL up to 0.81 V.
- Vmin applied to read and write port is 0.81 V.
- WL boost (Vmin + δ) is employed, Ids of PG ↑, Time to discharge '1' ↓, Write speed ↑. Since SNM constraints, WL boost is used only for MUX_1.
- Icell needs to be 100uA at worst PVT condition, i.e. SS, Low voltage (1.08V), High Temp. Icell is the discharge current of RBL that flows into the cell when RBL discharges during read.
- Icell determines the sizing of NMOS stack at the read ports- Icell ↑, Read speed ↑.
- Sizing of PU, PG, and PD were determined separately for write operation at the write port, as both read and write ports are separated.

For MUX_16:

- VDD for write port is given at 1.08 V, whereas for read port it is kept at 0.81 V.

Design of 1R/1W 8T SRAM Cell

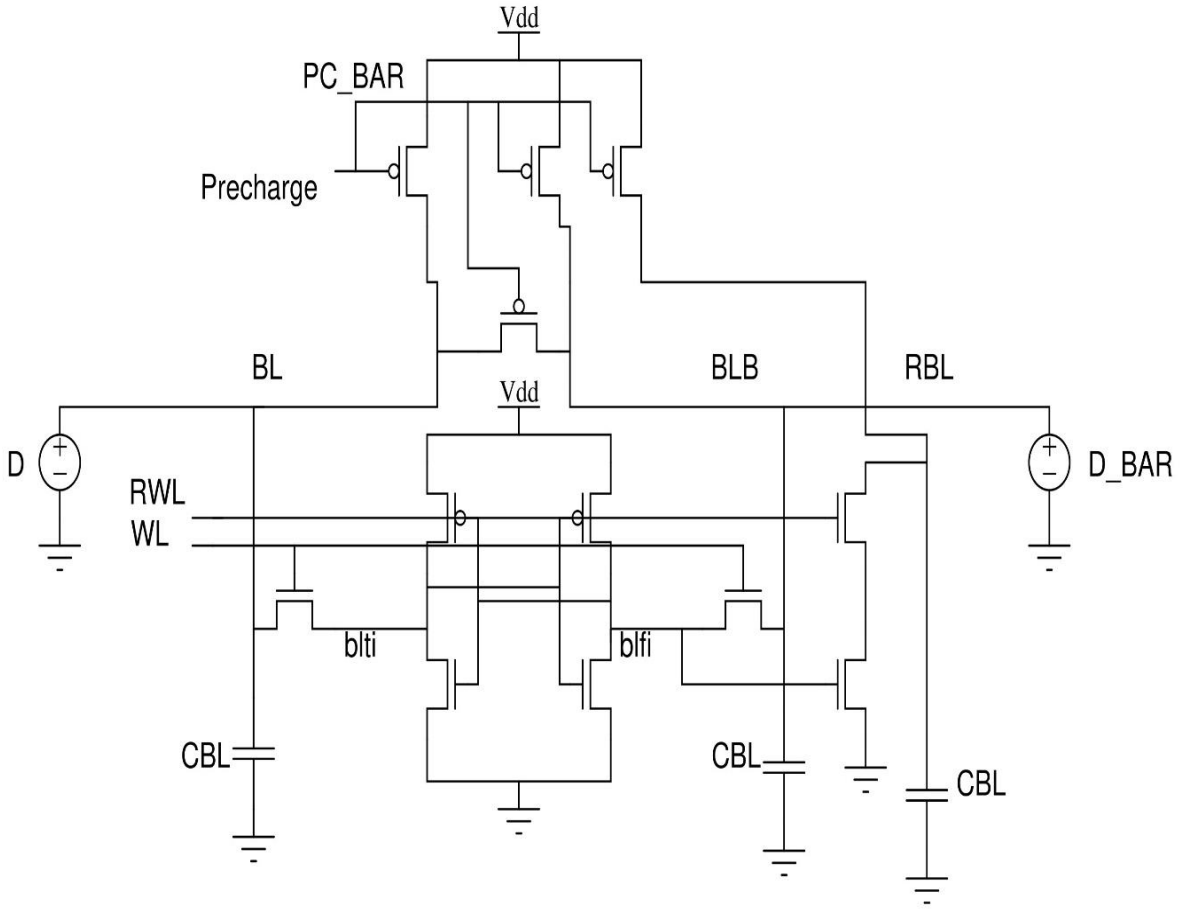


Fig 1: Schematic of 8T SRAM cell

KEY POINTS:

- The Read and Write ports are decoupled.
- NMOS stack in Read Port is sized according to Icell.
- More stable and faster cell, suitable for LV operations as retention voltage gets reduced.
- Additionally the cell can also use ports as 1RW/1R.

For proper write operation
Sizing should be PD>PG>PU

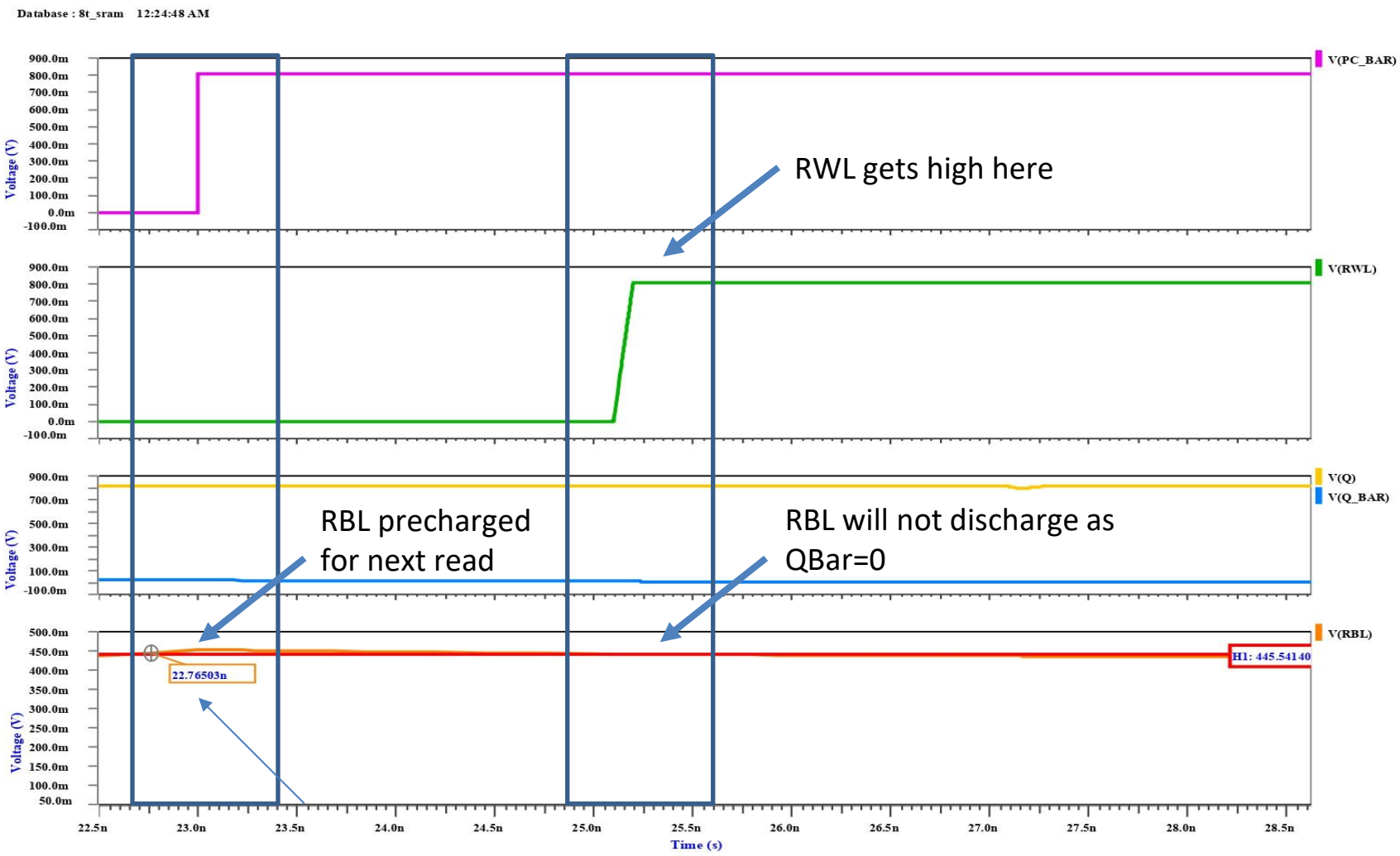
- Write Port

PU: W = 0.135, L = 0.085
PG: W = 0.175, L = 0.085
PD: W = 0.260, L = 0.085

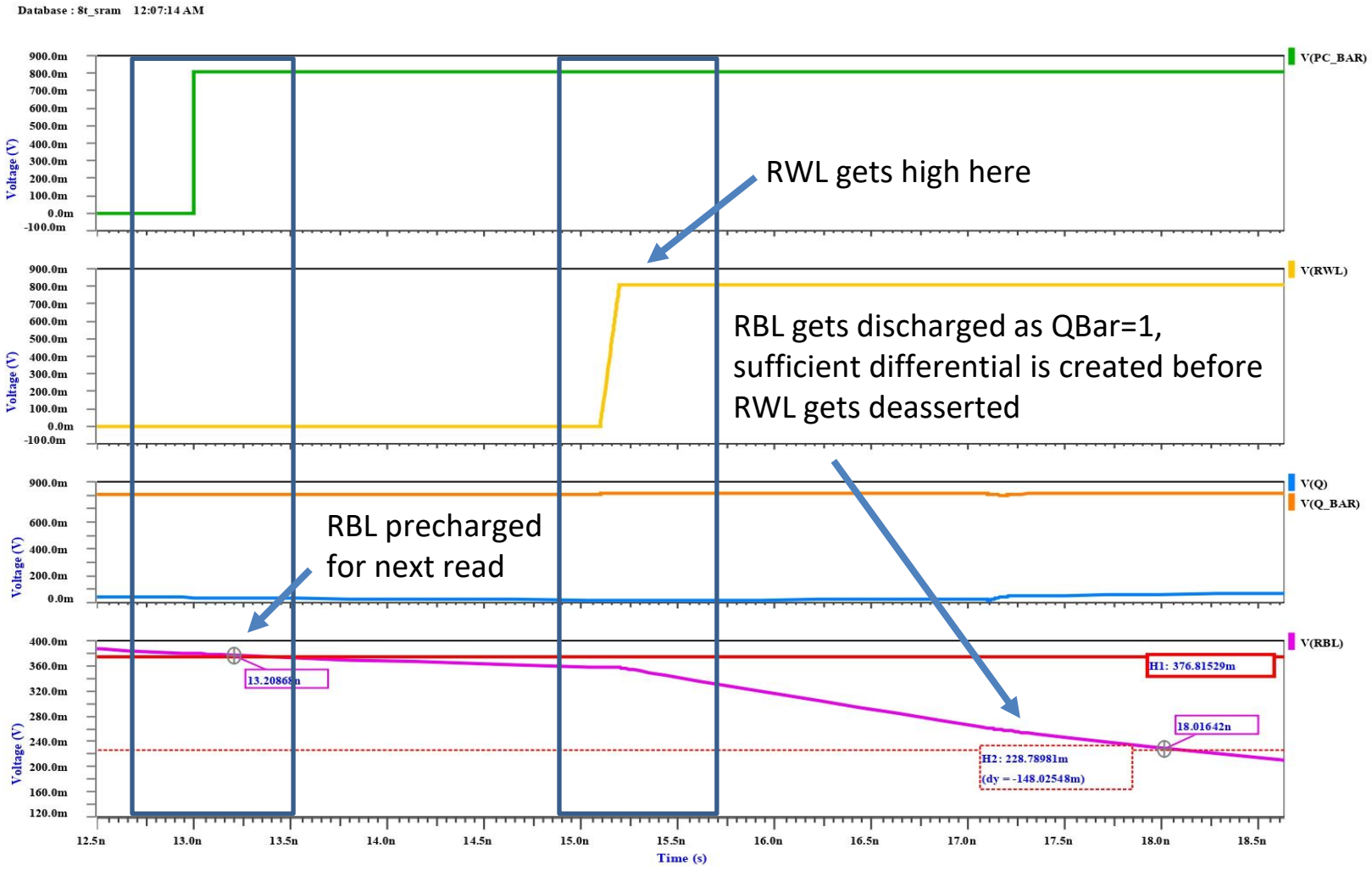
- Read Port NMOS:

W = 0.220, L = 0.085
W = 0.220, L = 0.085

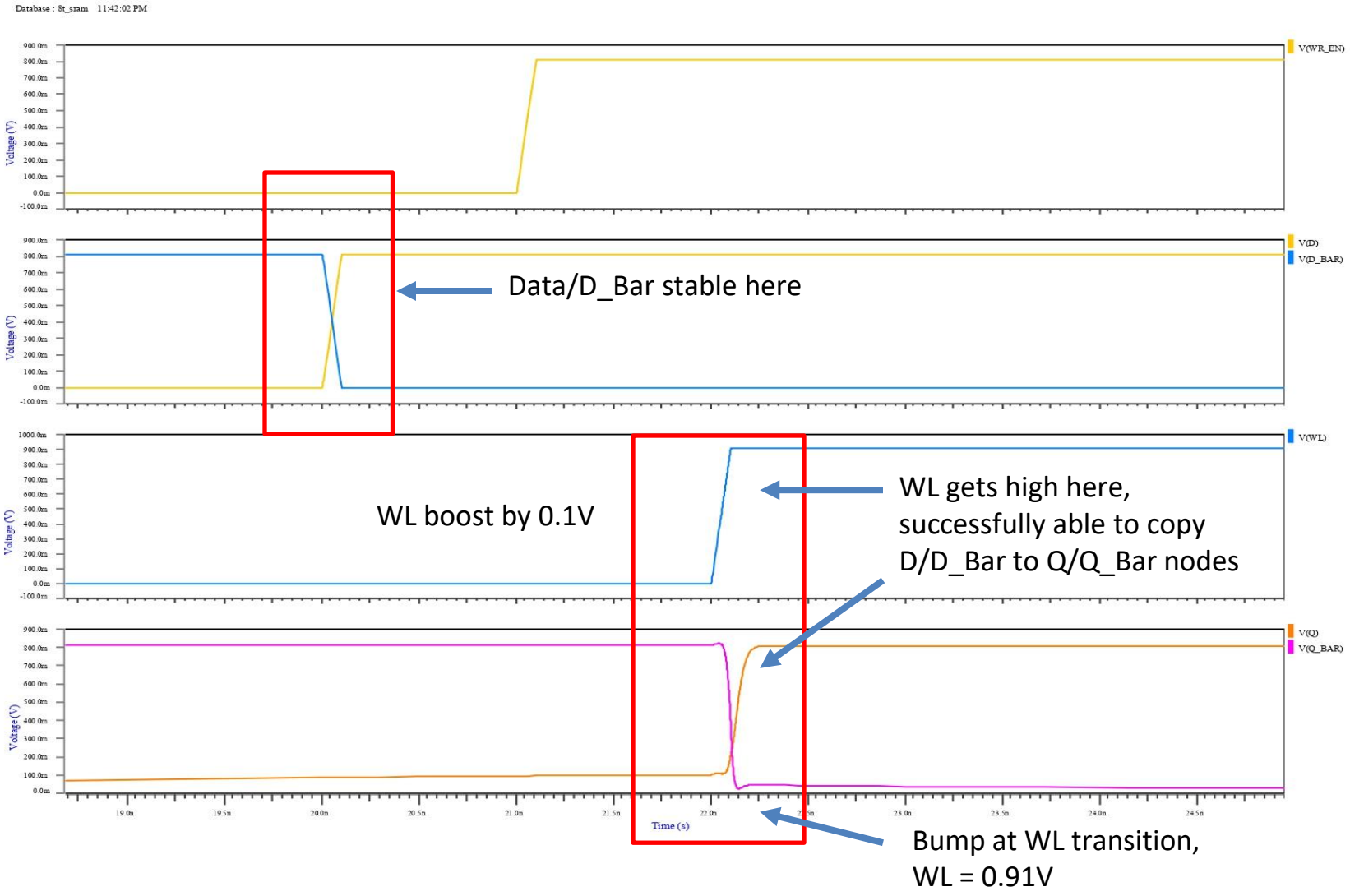
Simulation Waveform – Read Operation (Read '0')
PVT -TT, 0.81V, 25 C



Simulation Waveform – Read Operation (Read '1')
PVT -TT, 0.81V, 25 C



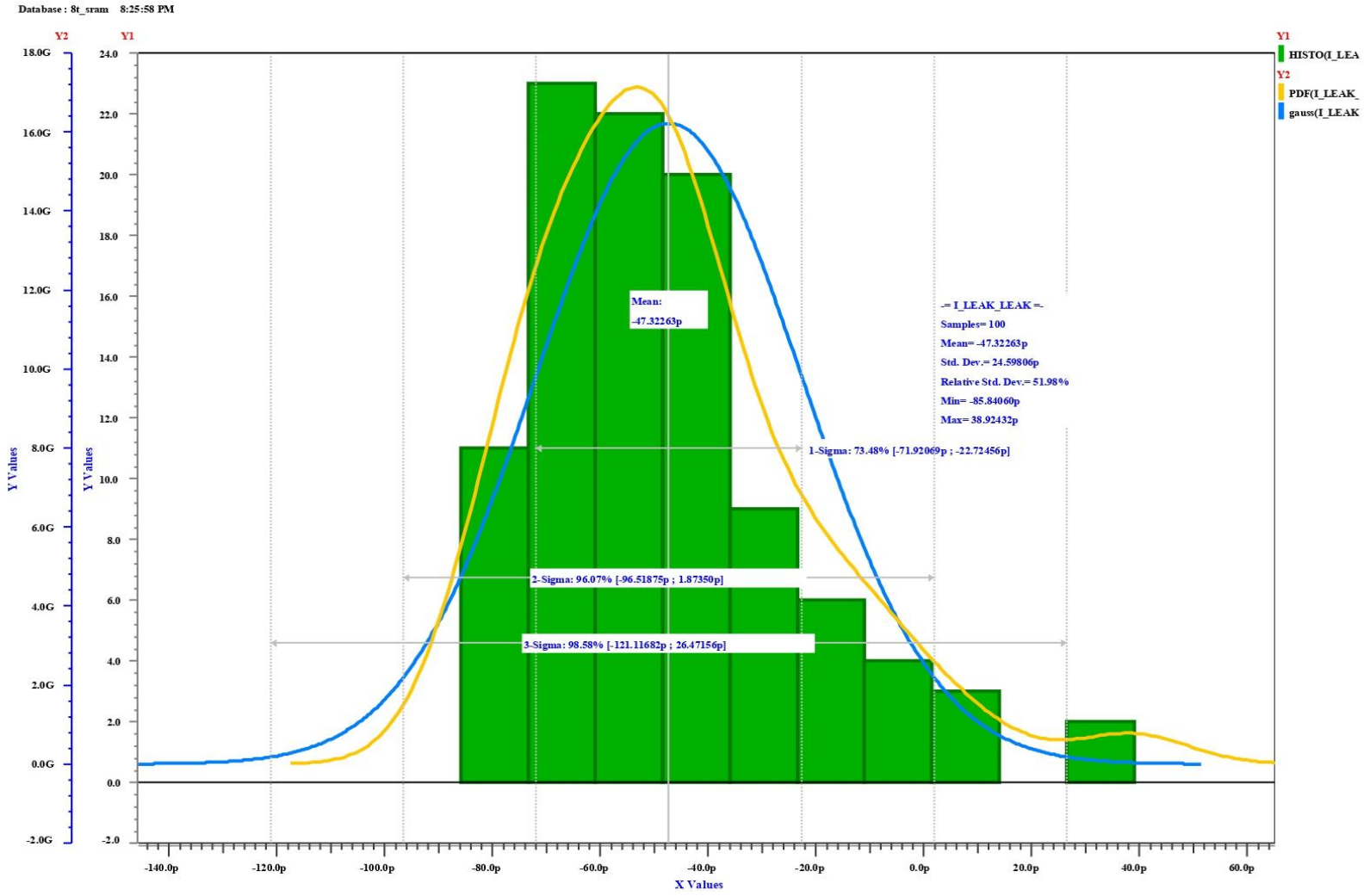
Simulation Waveform – Write Operation
PVT -TT,0.81V, 25 C



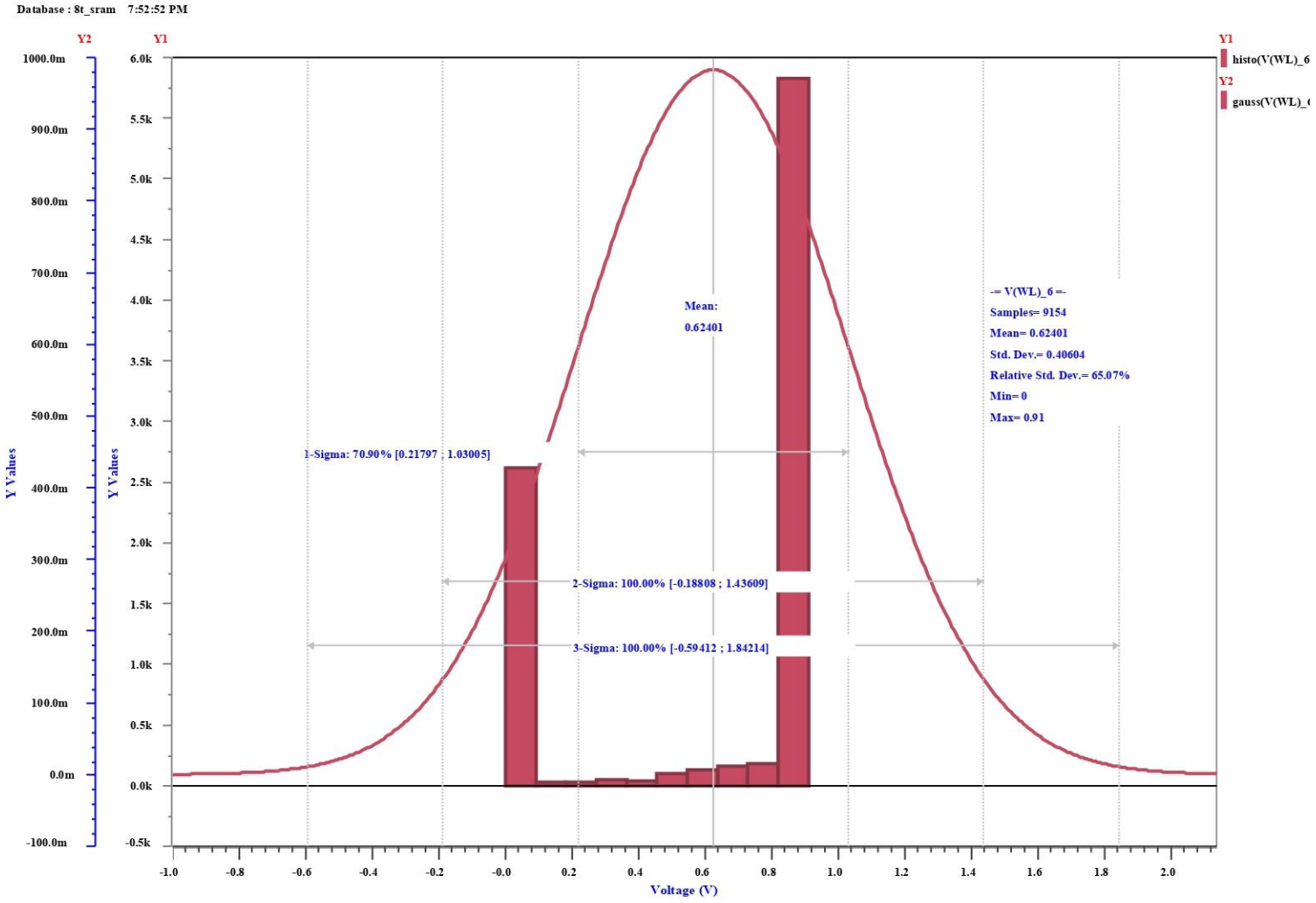
Work Done and PVT condition

FOM	PROCESS CORNER	STIMULI	PRE SIMULATION VALUE	POST SIMULATION VALUE
Cell Current	SS, 0.81V, 125C	RWL=High, QBar=1	51.75uA	NA
	SS, 1.08V, 125C		151.78uA	NA
Write Margin (Word Line)	SF, 0.81V, 125C	BLB =High, BL=Low, Q=0.81, QBar=0, WL=High	0.607V	NA
	SF, 0.81V, -40C		0.61V	NA
Write Time	SF, 0.81V, -40C	BLB=High, BL=Low, WL=High	6.24ns	NA
	TT, 0.81V, -40C		3.118ns	NA
Leakage	FF, 1.08V, 125C	All devices are in OFF state. WL, RWL =0	77.35pA	NA
	TT, 0.81V, 25C		29.67pA	NA

PDF for Leakage (Pre Layout)



PDF for WL Write Margin (Pre Layout)



Challenges and Future Plan

Challenges faced :

- Determining sizing to meet min Icell requirements during read operations.
- Determining PVT, stimuli for various FoMs.

Future Plans :

- To generate DRC and LVS clean bitcell layout for 8T 1R/1W SRAM cell.
- To generate a highly optimized 16×16 bit cell array using the technique of sharing utilized specifically for arrays in memories.
- RC parasitic extraction to carry out post-layout simulations.
- Perform MC simulations for various FoMs to qualify bit cell design for required sigma values.

References

- MDT by Dr Anuj Grover.

- Simulations: "Eldo." Siemens EDA. [Online].
  Available: https://eda.sw.siemens.com/en-US/ic/eldo/.
  [Accessed: March 10, 2024].

- Waveform Viewer: "EZwave." Siemens EDA. [Online].
  Available: https://www.eda-solutions.com/products/ezwave/.
  [Accessed: March 10, 2024].

Work Distribution

Schematic Design	Sizing and PVT Conditions	FOMs and Simulations
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