Design of 1R/1W 8T SRAM Cell

ECE-611 (Memory Design and Testing)

Group - 1

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Design specifications & understanding:

Given specification :

- Vmin (read port) = 0.81V
- Vmin (write port) = 1.08V when mux 16
- Vmin (write port) = 0.81V when mux 1 with WL Boost

  Icell = 100uA at wc, 1.08V

Understanding:

- Sizing of write port is determined on the basis of SNM and write functionality.
- Icell needs to be 100uA at worst PVT condition, i.e. SS, Low voltage 1.08V, 125C.
- Icell determines the sizing of NMOS stack at the read ports, Icell ↑, Read speed ↑.

Challenges

- Eldo commands for various FOM simulations to be done for SNM, Icell, Write Time, Write Margin etc.
- Six sigma qualification of SNM, such that sizing should ensure that the lowest and worst PVT has required 6-7 sigma margin only.
- Obtaining minimum area bitcell layout to meet design requirements efficiently.
- Designing array structure by flipping and sharing bitcell and routing various shared signals with different metal layers across the array in the minimum area possible.
- Overcoming challenges in creating layouts that meet Design Rule Checks (DRC) and Layout versus Schematic (LVS) criteria, ensuring cleanliness and compliance with design standards.
- We encountered challenge in achieving sigma qualification for bitcell figure of merits (FOMs).

Design of 1R/1W 8T SRAM Cell

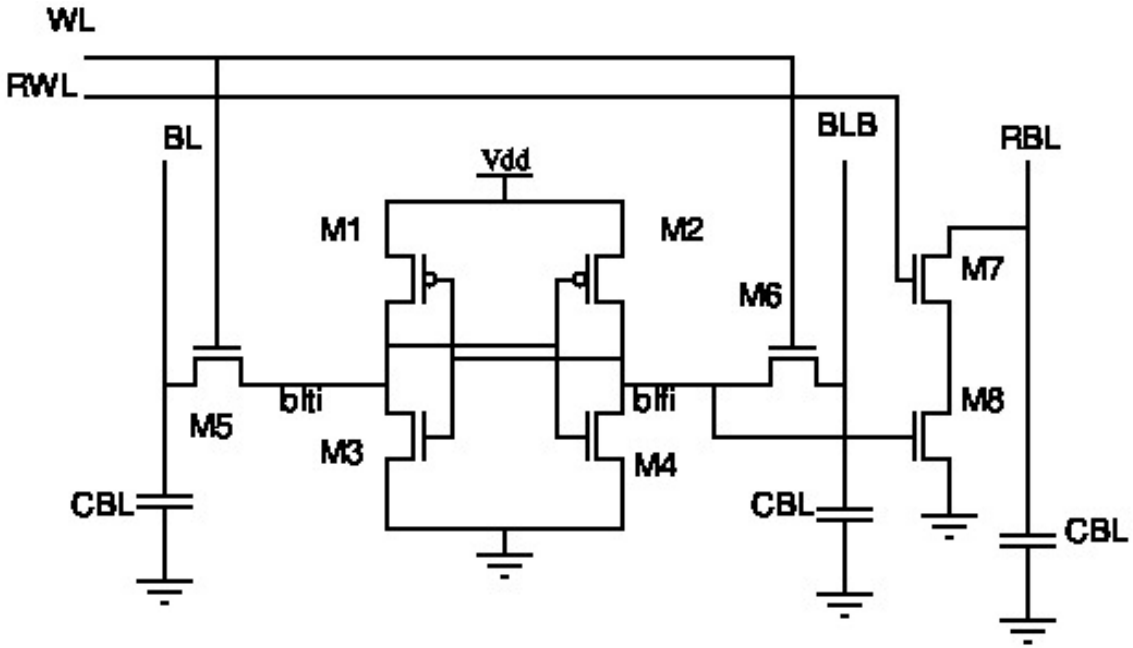


Fig 1: Schematic of 8T SRAM cell

KEY POINTS:

- The Read and Write ports are decoupled.
- NMOS stack in Read Port is sized according to Icell.
- More stable and faster cell, suitable for LV operations as retention voltage gets reduced.
- Additionally the cell can also use ports as 1RW/1R.
- I_Pon is the additional FOM that needs to be taken care to avoid accidental read by SA.

Sizings

Transistor	Sizings (W/L)		Constraint
	Initial	Final	
Read Port (M7, M8)	0.220/0.085	0.200/0.08	Icell=100uA
Pull Up (M1,M2)	0.135/0.085	0.135/0.085	Minimum sized device
Pass Gate (M5,M6)	0.175/0.085	0.170/0.085	Read SNM 6-Sigma Write Functionality
Pull Down (M3,M4)	0.260/0.085	0.210/0.085	Read SNM 6-Sigma Write Functionality

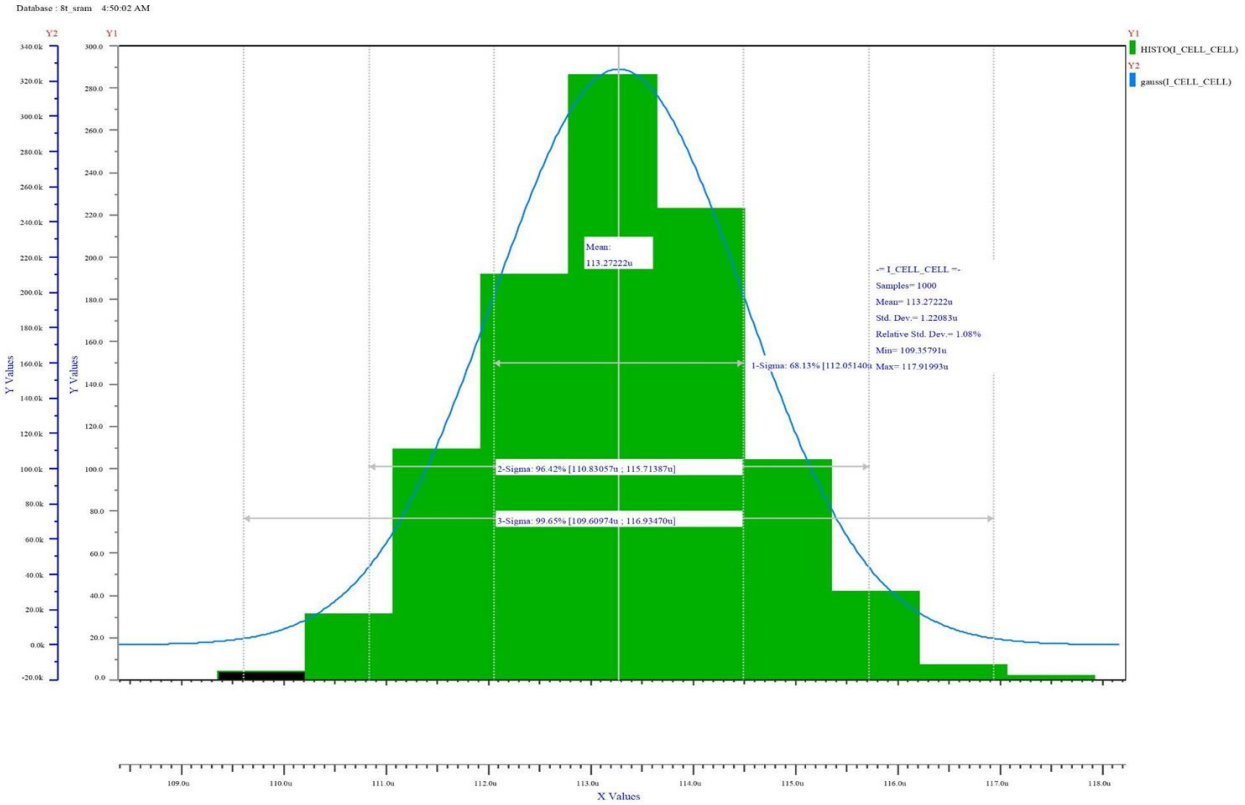
Verification Plan, Stimuli and PVT conditions

FOMs		PROCESS CORNER	STIMULI	PRE SIMULATION VALUE	POST SIMULATION VALUE
Read SNM		FS, 1.08V, 125C	BL, WL = High	—	132.64 mV
		FS, 0.81V, 125C		—	110.16 mV
Cell Current		SS, 1.08V, 125C	RWL, WL = High, Q_Bar = 1	151.78 µA	123.88 µA
		SS, 0.81V, 125C		105.12 µA	97.27 µA
Write Margins	***WL Write Margin***	SF, 0.81V, 125C	BLB=High, BL=Low, WL=High	0.607 V	0.570 V
		SF, 0.81V, -40C		0.61 V	0.565 V
	BL Write Margin	SF, 0.81V, 125C		—	0.530 V
		SF, 0.81V, -40C		—	0.567 V

Verification Plan, Stimuli and PVT conditions

FOMs	PROCESS CORNER	STIMULI	PRE SIMULATION VALUE	POST SIMULATION VALUE
Write Time	SF, 0.81V, -40C	BLB=High, BL=Low, WL=High	6.24 ns	12.194 ns
	TT, 0.81V, -40C		3.118 ns	10.23 ns
Leakage	FF, 1.08V, 125C	All devices are in OFF state. WL, RWL =0	77.35 pA	430 pA
	FF, 0.81V, 25C		29.67 pA	81 pA
I_Partial_(ON) (Additional FOM for 8T)	FS, 1.08V, 125C	RWL = High, Q = 1 Q_Bar = 0	—	2.4008 µA

PDF for Icell (Post Layout)

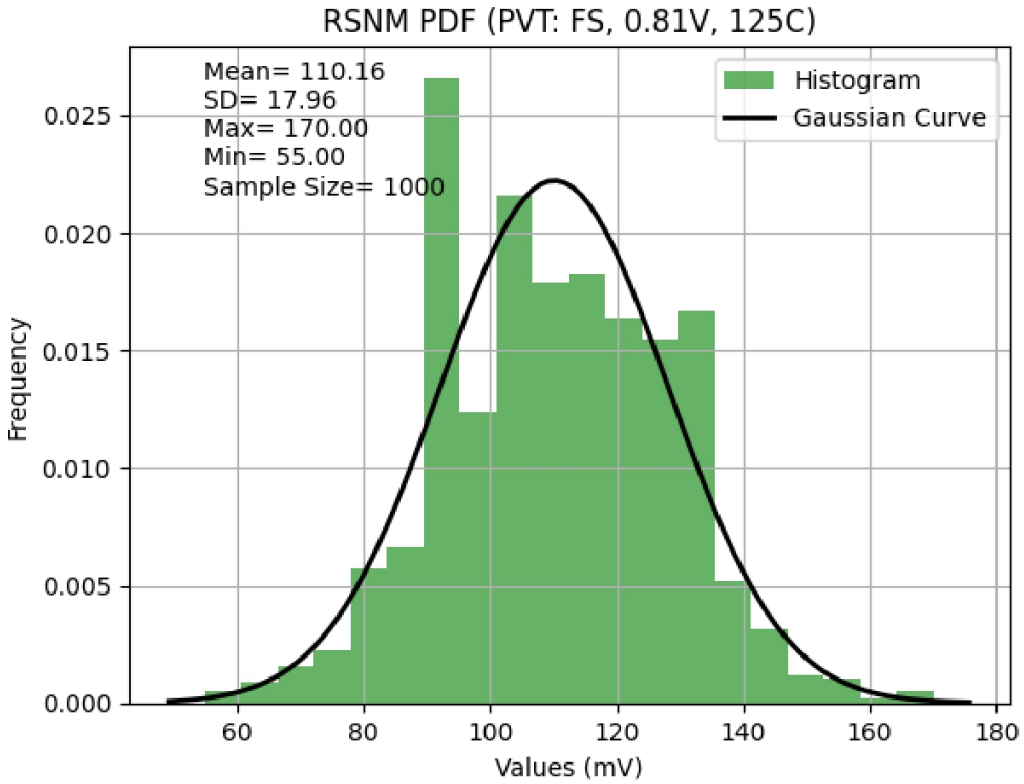


Icell @SS, 1.08V, 125C
Six Sigma Qualified

Mean (μ) = 113.27 μA
SD (**σ**) = 1.221

μ - 6*(**σ**) =
105.95 μA > 100 μA

PDF for SNM (Post Layout)

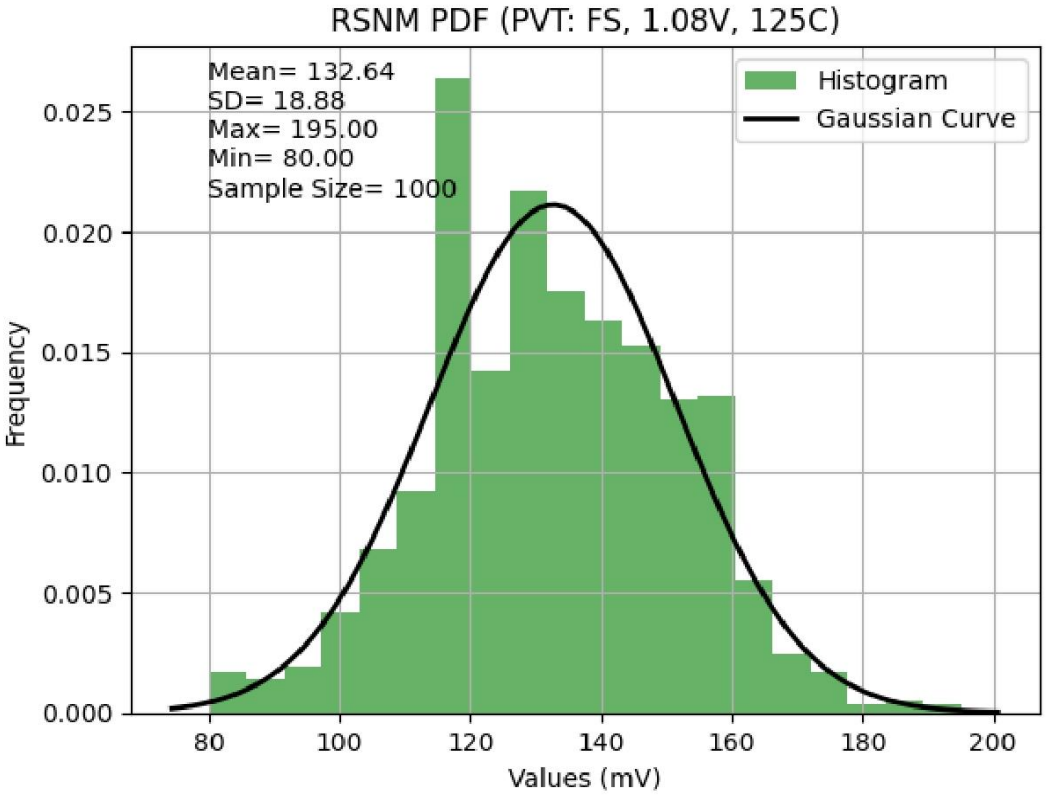


SNM @FS, 0.81V, 125C
Six Sigma Qualified

Mean (μ) = 110.16 mV
SD ($\boldsymbol{\sigma}$) = 17.96

μ/($\boldsymbol{\sigma}$) = 6.1336

PDF for SNM (Post Layout)

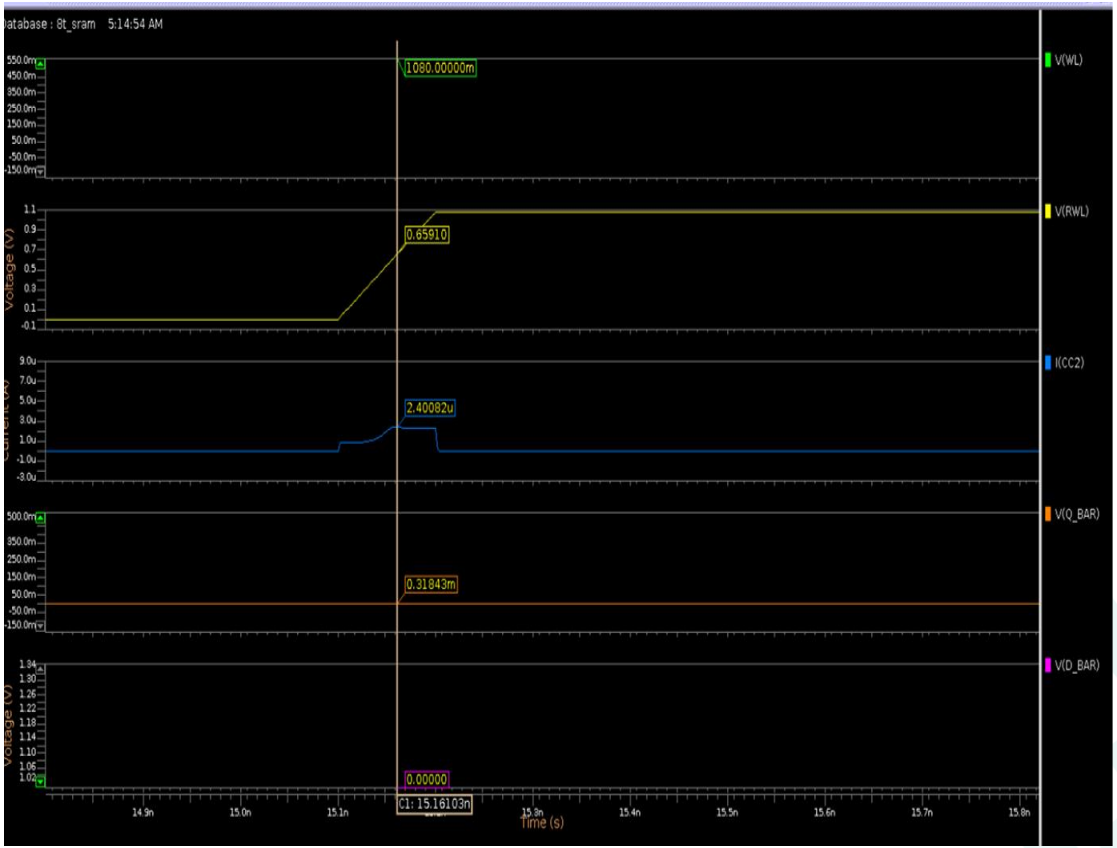


SNM @FS, 1.08V, 125C
Six Sigma Qualified

Mean (μ) = 132.64 mV
SD ($\boldsymbol{\sigma}$) = 18.88

μ/($\boldsymbol{\sigma}$) = 7.025

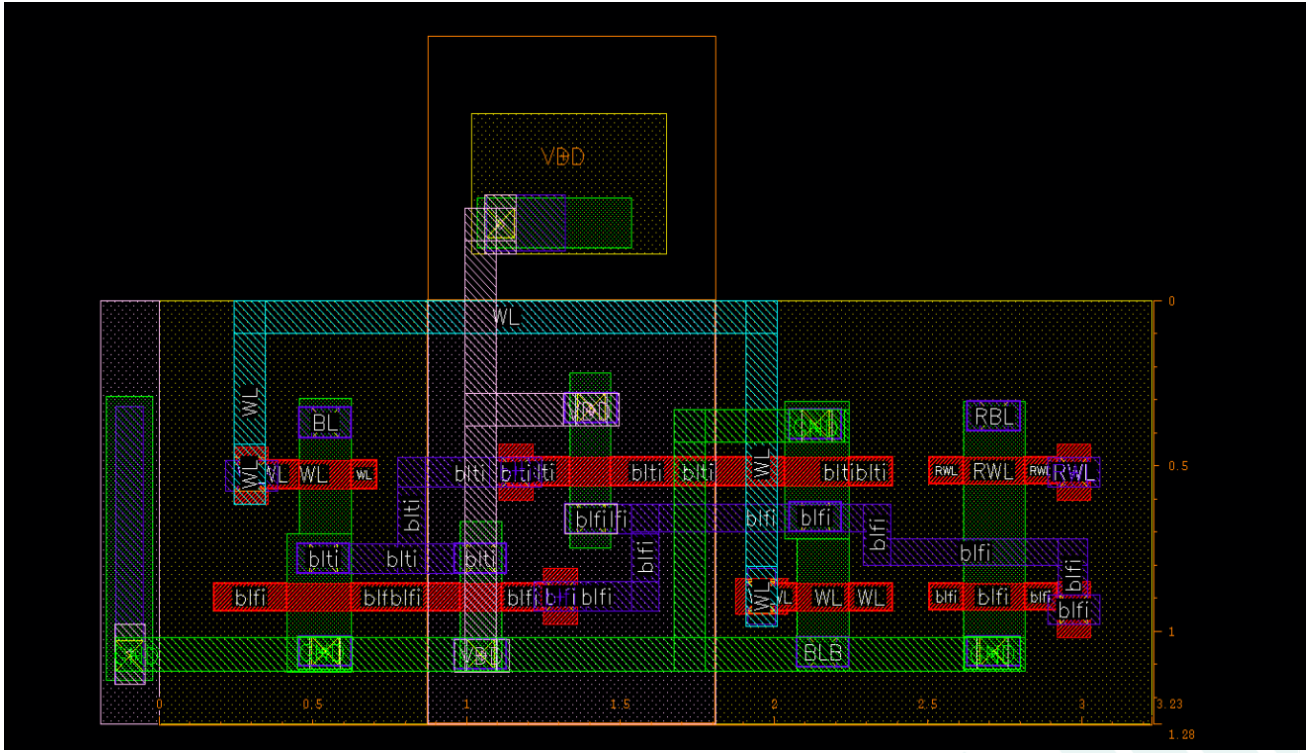
I_Partial_(ON)



- In an scenario when,
  Q = 1.08 v Q' = 0v
- Ideally, RBL should not discharge, current should be zero when RWL gets high.
- However, due to a voltage bump (**blfi gets charged up**), both M7 and M8 experience a partial turn-on, represented by I_partial_on.

I_Partial_(ON)	
1.08V	2.4008 µA

Layout

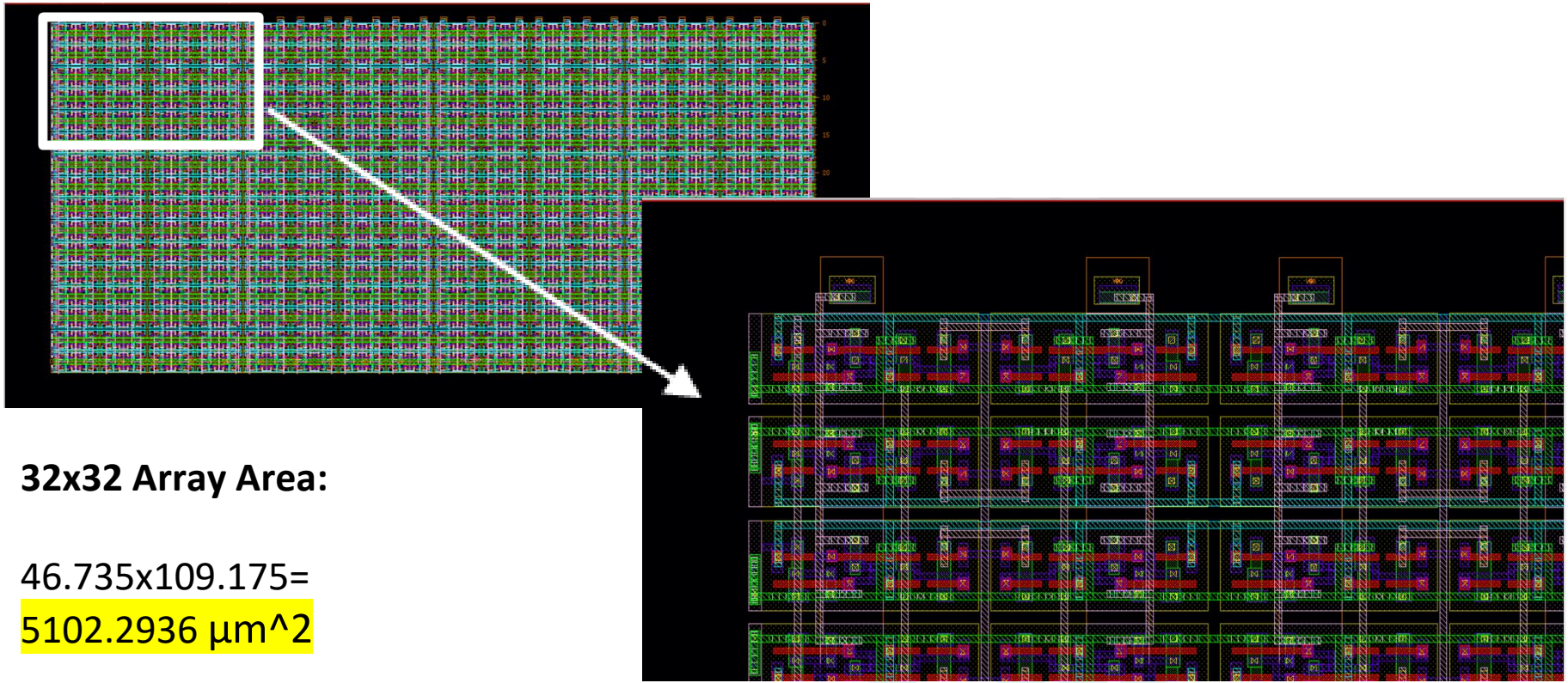


Bitcell Area:

1.28x3.23 =

4.134 µm^2

Layout of 32X32 Array

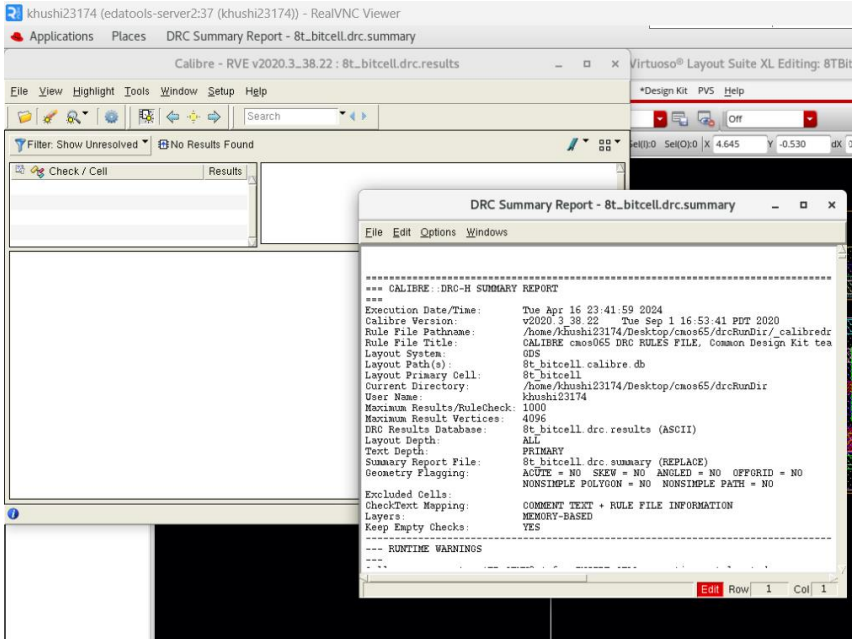


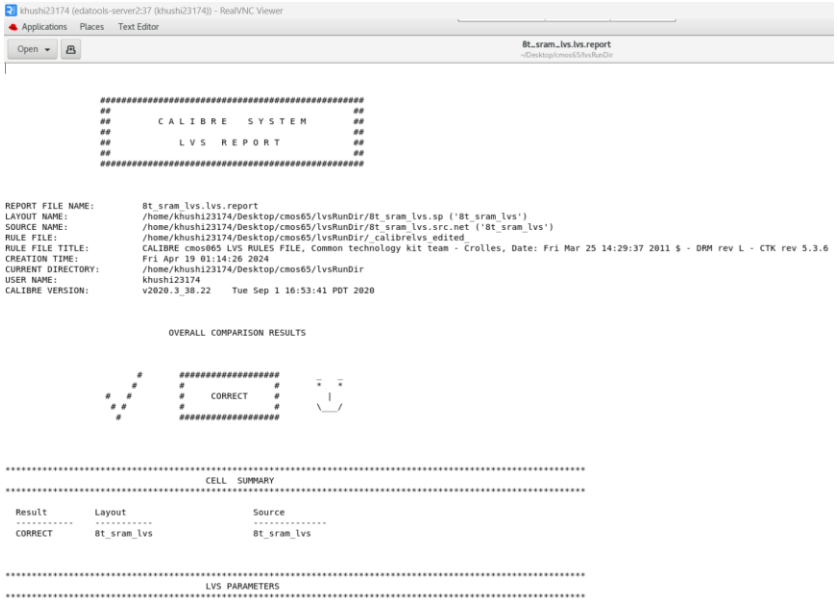
32x32 Array Area:

46.735x109.175=

5102.2936 µm^2

DRC and LVS clean Reports





Conclusions and Future Plans:

- **Technical conclusions**
  - Designed and analysed 8T sram cell, design specifications were met.
  - Accomplished denser **32x32** SRAM cell array using technique of flipping and sharing.
  - We successfully achieved custom layout design using Virtuoso, ensuring precise control over the placement and routing to meet minimum area constraint.
- **Emphasise on learning from the project**
  - We were able to practically implement concepts related to SNM, statistics for VLSI and sram cell design.
  - We utilize Virtuoso for schematic design and layout creation, ensuring LVS and DRC via Calibre.
  - Post-layout parasitic extraction is performed using PEX.
  - For evaluation FOMs and Monte Carlo simulations were done using Eldo and analyze waveforms with EZwave to validate and optimize our design for given specifications.
  - Parasitic extraction degraded FOMs of cell to some extent.
- **Future plans**
  - FOMs can be compared with different bitcells (viz. 6T, 8T 2R/W, 10T etc) for application specific analysis.
  - Impact of parasitic extraction can be lowered by having performance oriented design approach.
  - Performance improved 8T sram cell can be employed for IMC applications.

References

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- Simulations: "Eldo." Siemens EDA. [Online]. Available: https://eda.sw.siemens.com/en-US/ic/eldo/. [Accessed: March 10, 2024].

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Work Distribution

Schematic Design, Layout and Array	Sizing and PVT Conditions	FOMs and Simulations
Khushi Kasbe, Vansh Singhai	Gangaprasad Horke, Khushi Kasbe	Vansh Singhai, Gangaprasad Horke