X86 - ISA

The 80x86 Family

Name	Date	Transistors	Clock speed	Data width
8080	1974	6K	2MHz	8
8086	1978	29K	5MHz	16
80286	1982	134K	12 MHz	16
80386	1985	275K	16-33 MHz	32
80486	1989	1.2 M	20 -100 MHz	32
Pentium	1993	3.1M	60-200 MHz	32 /64
Pentium II	1997	7.5 M	233-450 MHz	32/ 64
Pentium III	1999	9.5M	450 -933 MHz	32 /64
Pentium 4	2000	42 M	1.5 GHz	32/ 64

The Evolution of Microprocessors

The 16-bit Processors

8086

- 20 Address lines
- 2^{20} – 1 MB
- 2.5 MIPS

80286

- 24 Address lines
- 2^{24} – 16 MB
- 4 MIPS

The 32-bit Processors

80386

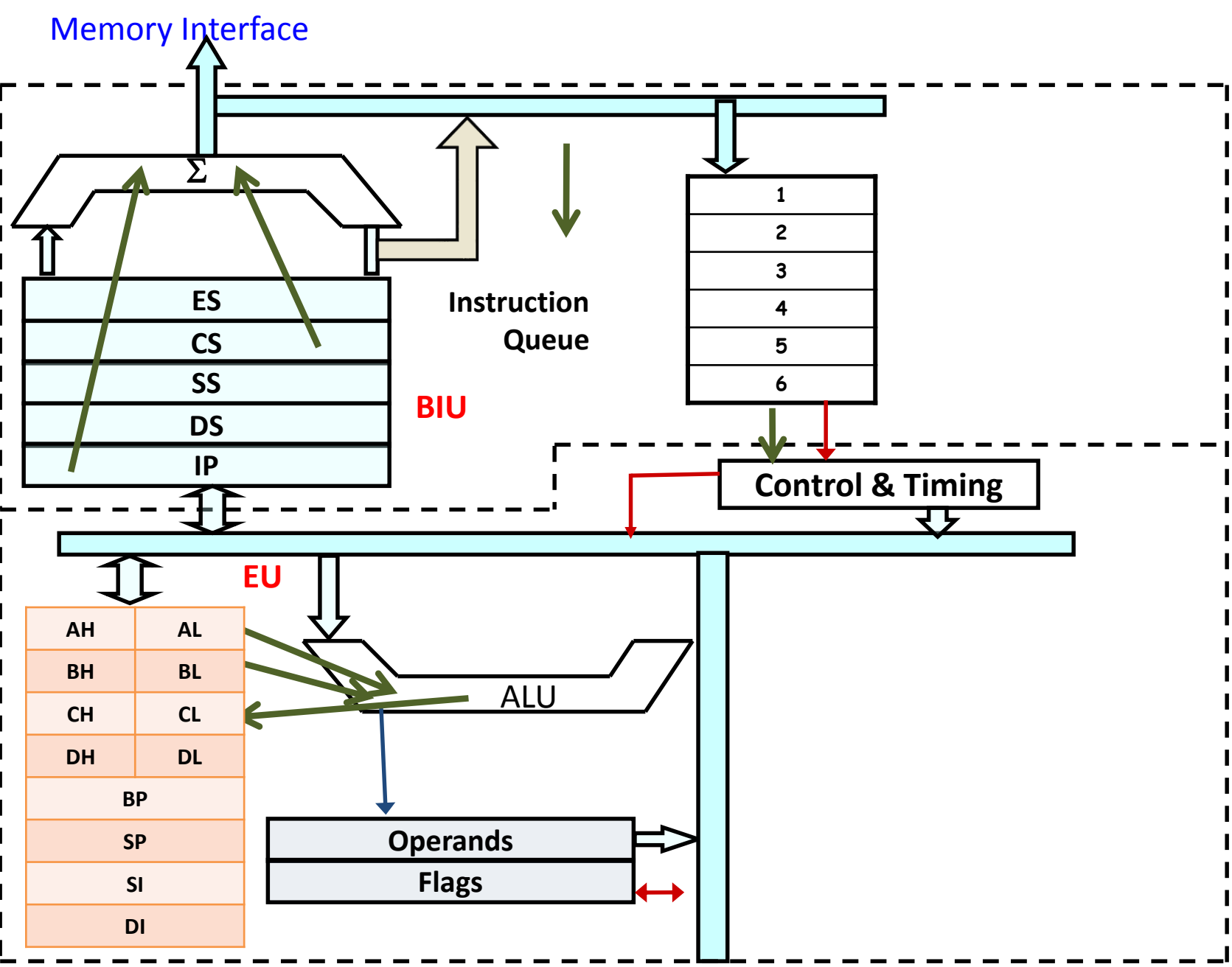
- 32 Address lines
- 2^{32} – 4GB

80486

- 32 Address lines
- 2^{32} – 4GB
- Floating Pt Unit
- Internal Cache
- 50 MIPS

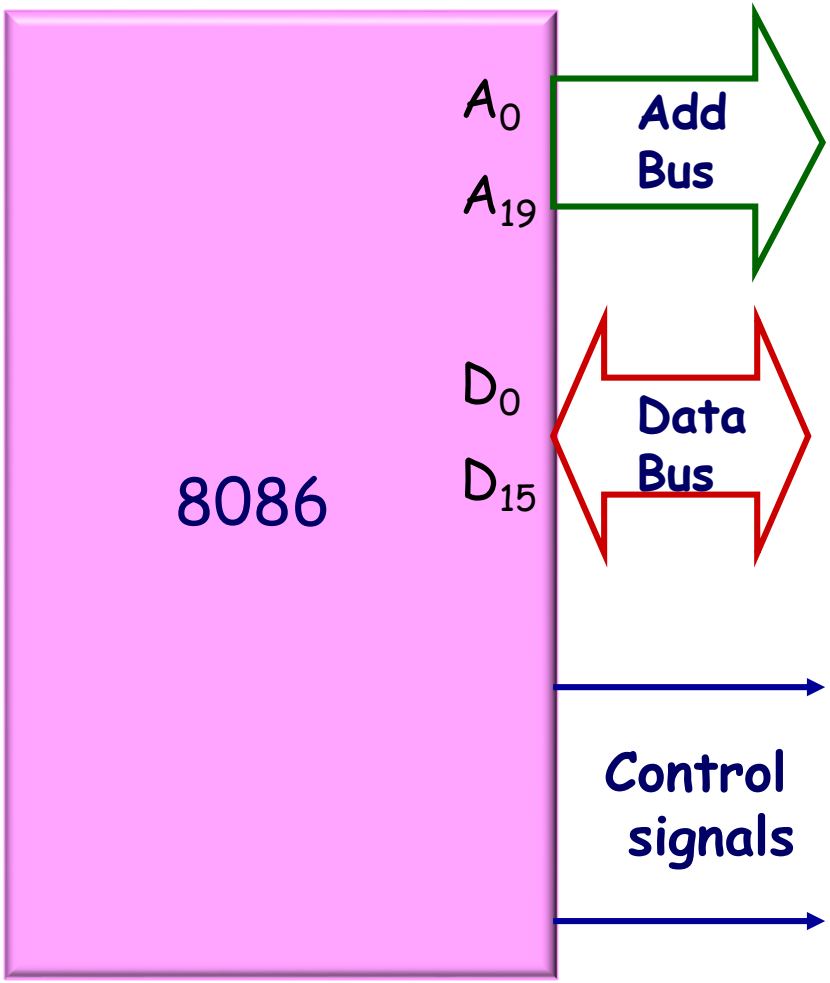
Characteristics of the X86 Family

- CISC
- Instructions – broken up into µops
- Complex Instruction Decoder

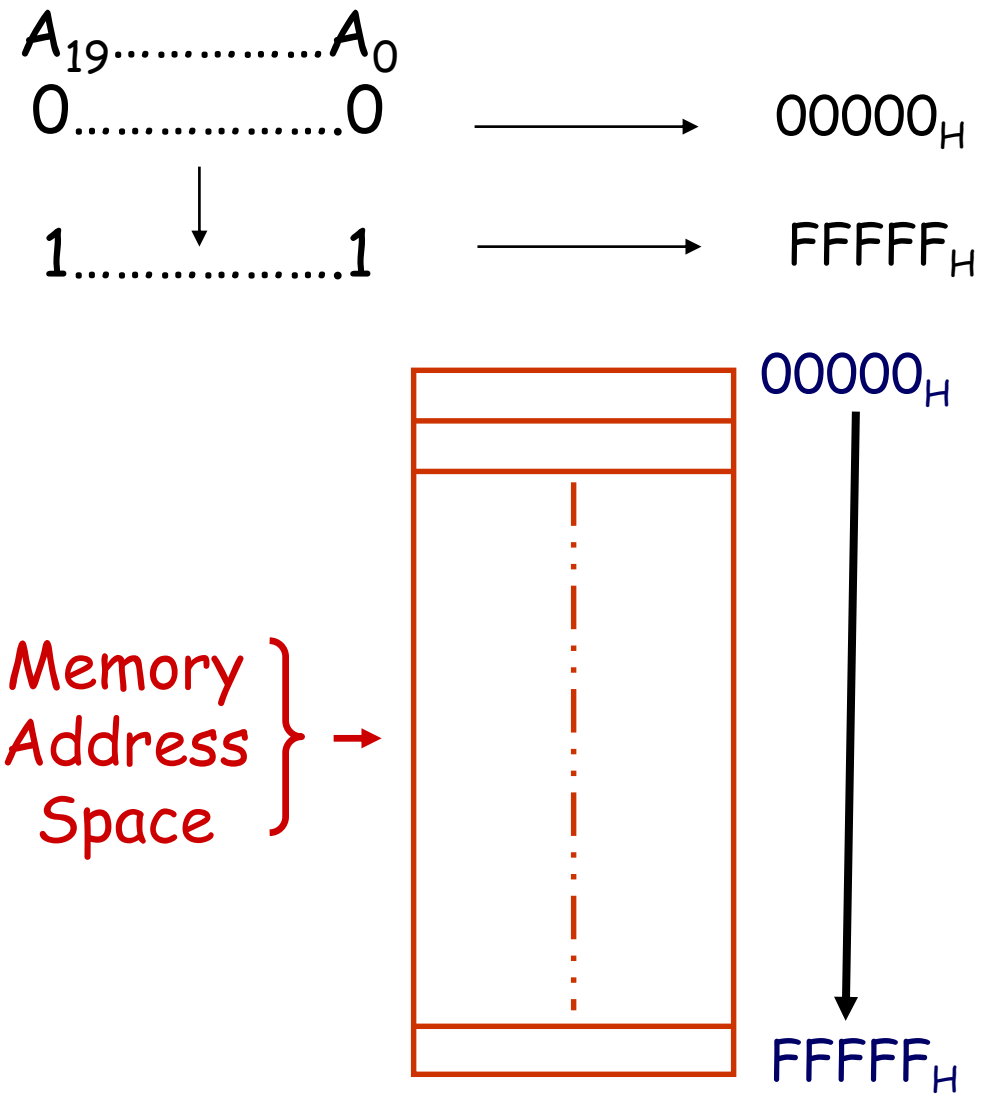


Block Diagram of 8086

8086 - Buses

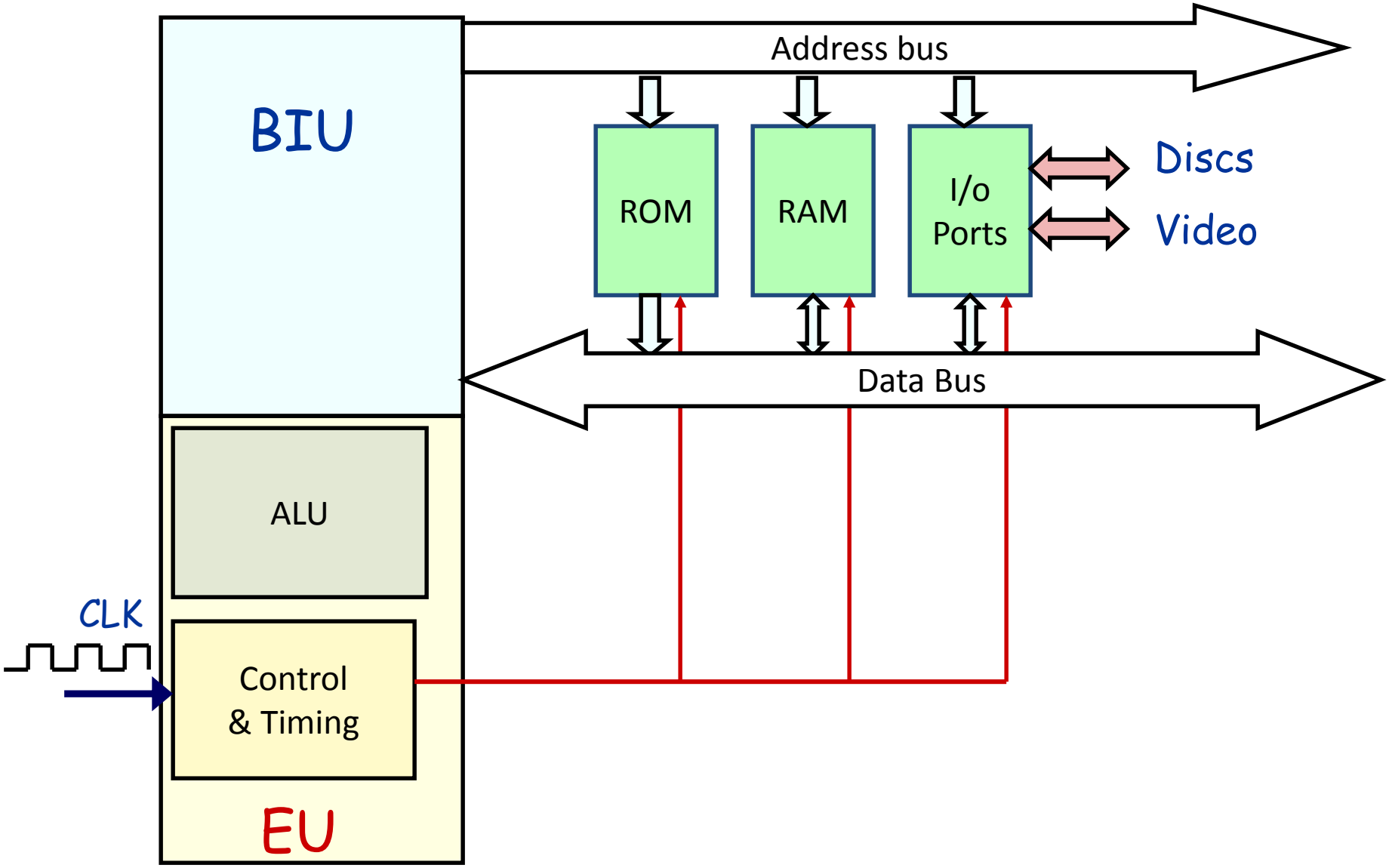


Memory Address Space



Microprocessor

- Fetches Instruction ⟶ BIU
- Executes Instruction ⟶ EU


BIU
Address bus
ROM
RAM
I/o
Ports
Discs
Video
Data Bus
ALU
CLK
Control
& Timing
EU

Variation of 8086 - 8088

- External Data Bus – 8-bits
- Inst Queue – 4 bytes

X86 - ISA

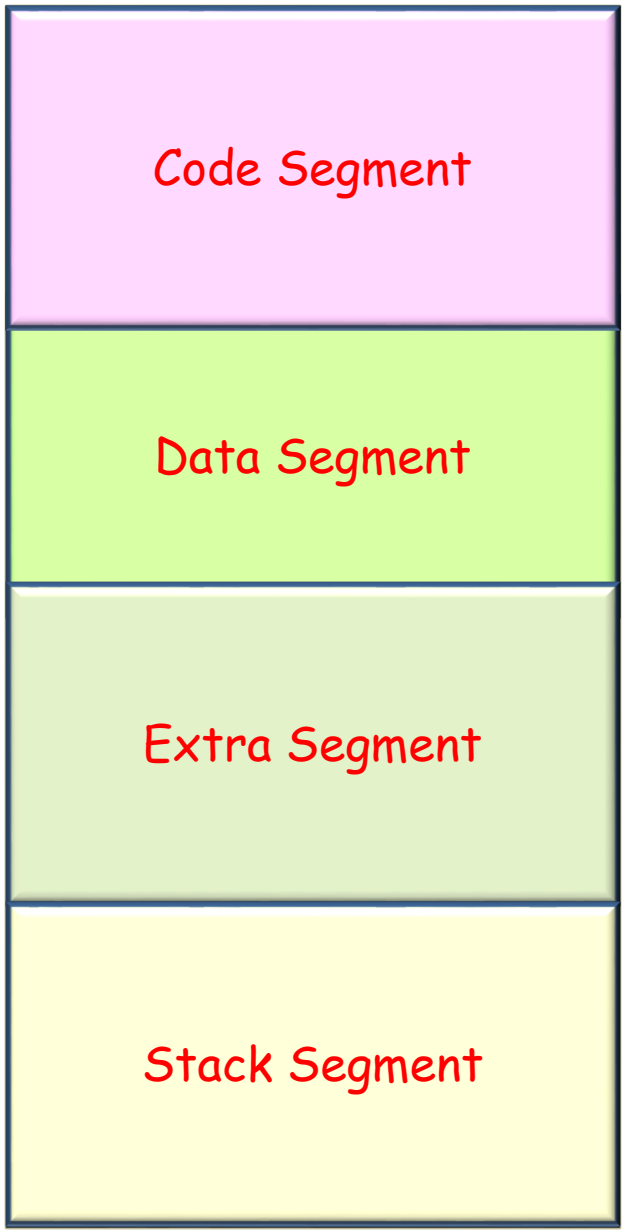
8086-80486 Programmers Model

BIU

Memory Addressing

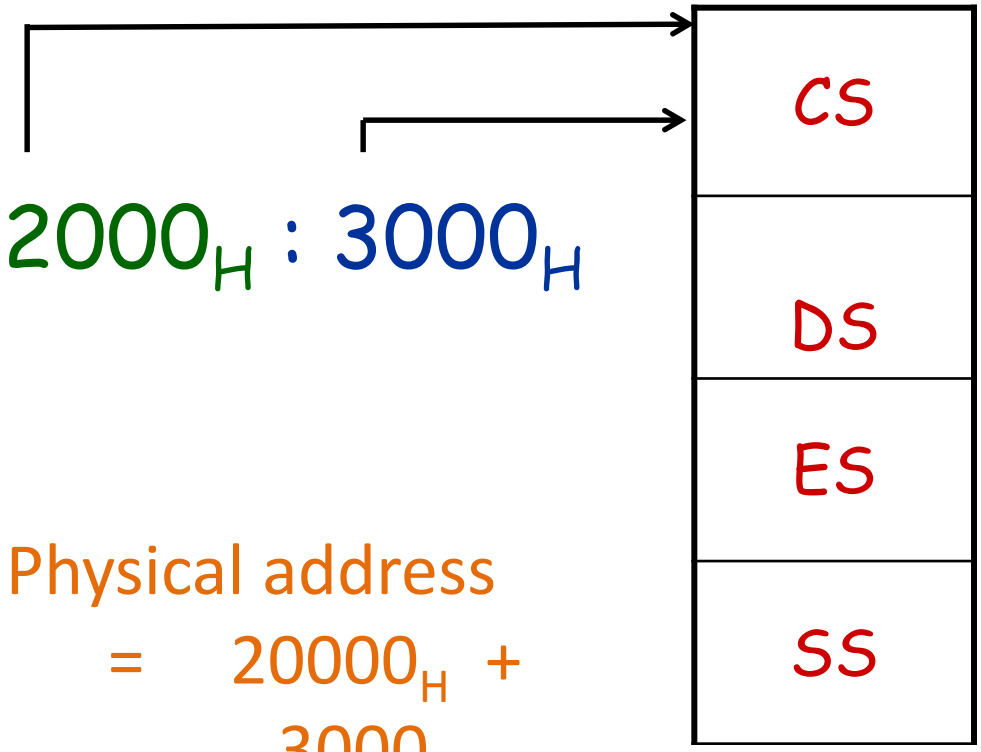
- Real
  - Access only 1 MB of Memory
  - Only 20 Address Lines Required
- Protected

Programmer's Model - BIU


Code Segment
Data Segment
Extra Segment
Stack Segment

$CS = 2000_H$ Base address

$IP = 3000_H$ Offset address

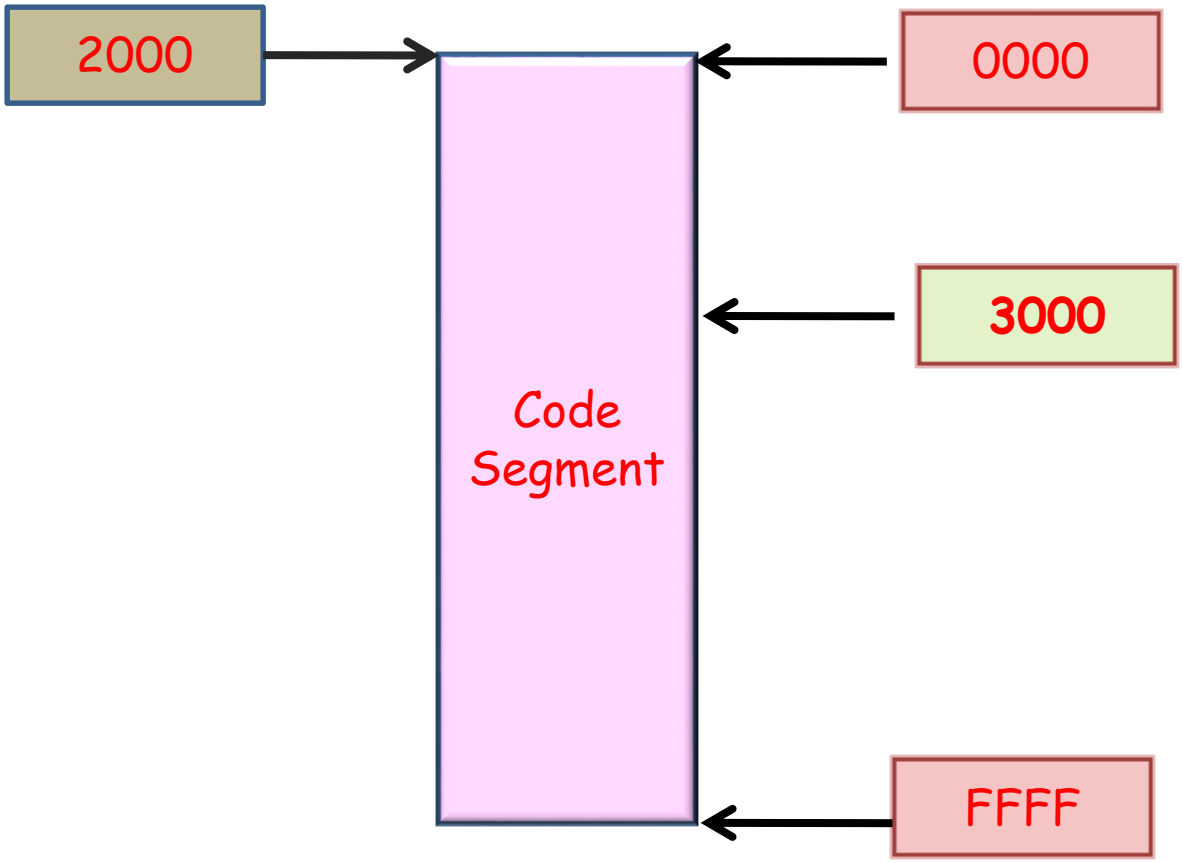


$2000_H : 3000_H$

Physical address

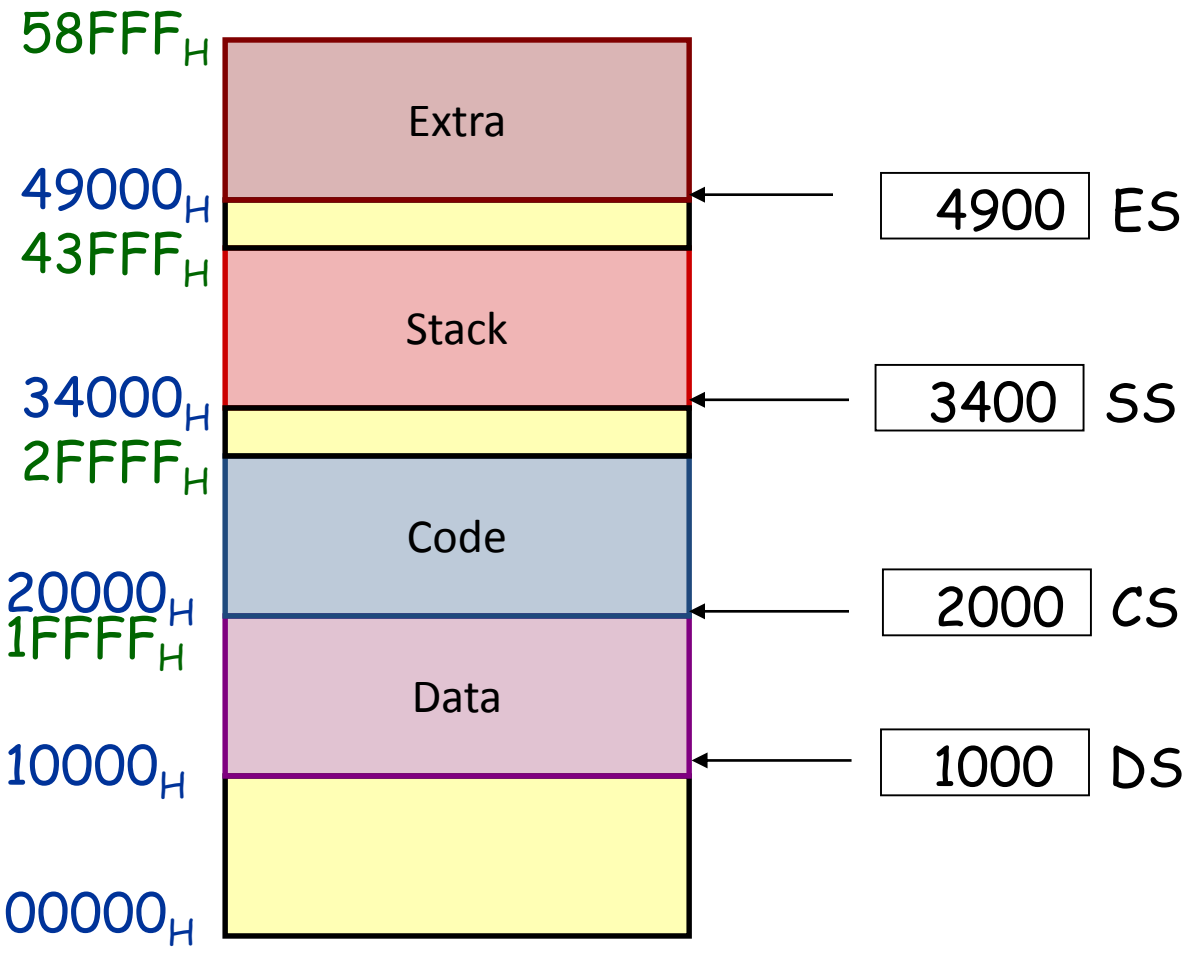
$= 20000_H + 3000_H$

23000_H


2000
0000
3000
Code
Segment
FFFF

Advantage of Segmentation

- Relocation
- Program – Specify only offset
- Program – $F0000_H \rightarrow 10000_H$
- Program contents need not be change – only Segment needs to change from $F000_H \rightarrow 0000_H$


58FFF H
Extra
49000 H
43FFF H
Stack
34000 H
2FFFF H
Code
20000 H
1FFFF H
Data
10000 H
00000 H
4900
ES
3400
SS
2000
CS
1000
DS

High Memory

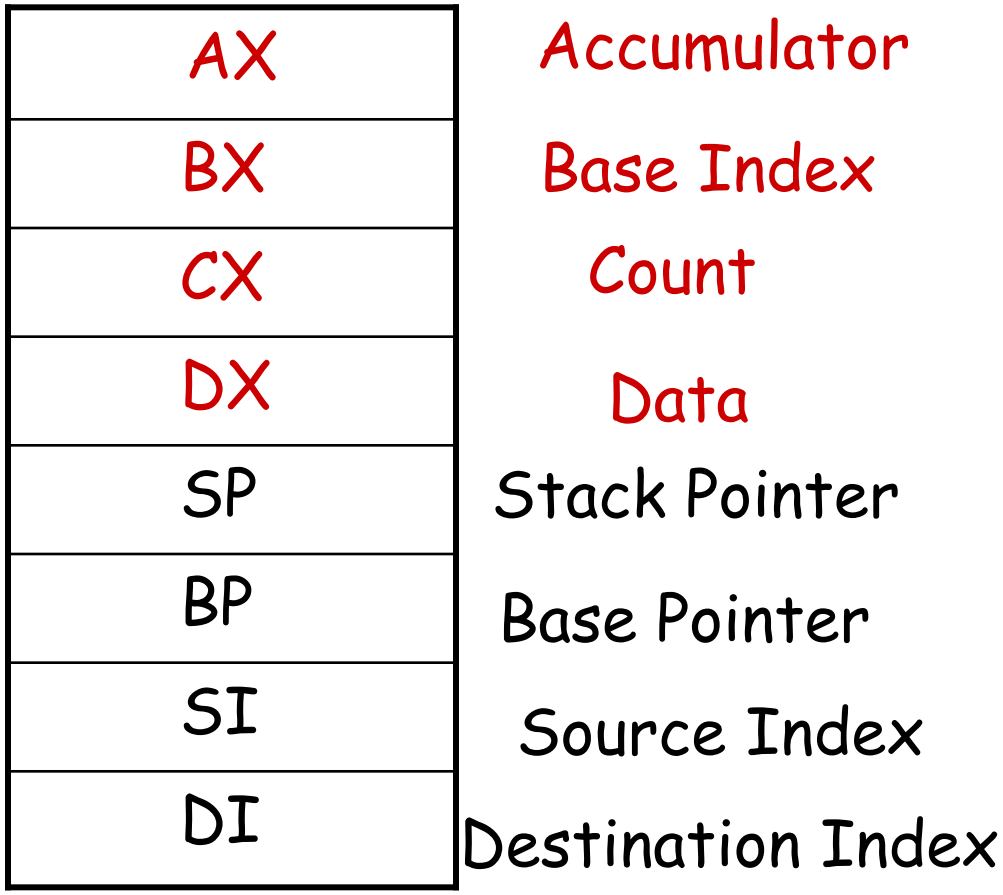
- HIMEM.SYS
- A_{20}
- Segment Address – $FFFF_H$
- Offset Address – 4000_H
- $103FF0_H$
- $03FF0_H$

X86 - ISA

8086-80486 Programmers Model

EU

Programmers Model



Registers

MULTIPURPOSE REGISTERS

AX, BX, CX, DX, BP, DI, SI

SPECIAL PURPOSE REGISTERS

IP, SP, FLAGS

CS, DS, SS, ES
(Segment Registers)

Registers - MPR

AX — AH (8 bit) — AL (8 bit)

(Accumulator)

BX — BH — BL

(Base Register)

CX — CH — CL

(Used as a counter)

DX — DH — DL

(Used to point to data in I/O operations)

Programmer's Model-MPR

EAX	AH	AL
EBX	BH	BL
ECX	CH	CL
EDX	DH	DL
EBP	BP	
ESI	SI	
EDI	DI	
ESP	SP	

Default 16 bit segment and offset address combinations

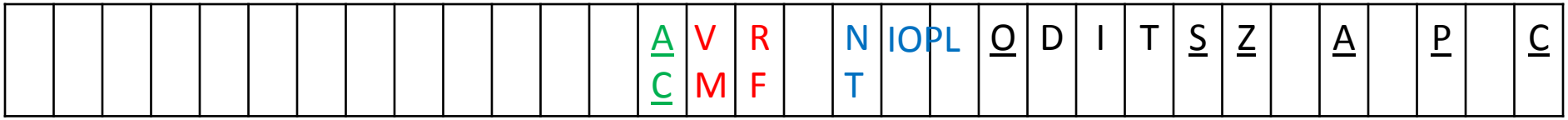
Segment	offset	special purpose
CS	IP	Instruction Address
SS	SP (or) BP	Stack address
DS	BX,DI,SI an 8-bit number 16 – bit number	Data address
ES	DI for string Instructions	String destination address

Programmer’s Model -SFR

Flags

- Status
- Control

Flag Register



80x86-Summary

BIU (Bus Interface Unit)
provides hardware funcns for generation of the memory and I/O addresses for the transfer of data between itself and the outside world

EU (Execution Unit)
receives program instruction codes and data from the BIU executes these instructions and stores the results in the general- purpose registers