80286,80386 & 80486

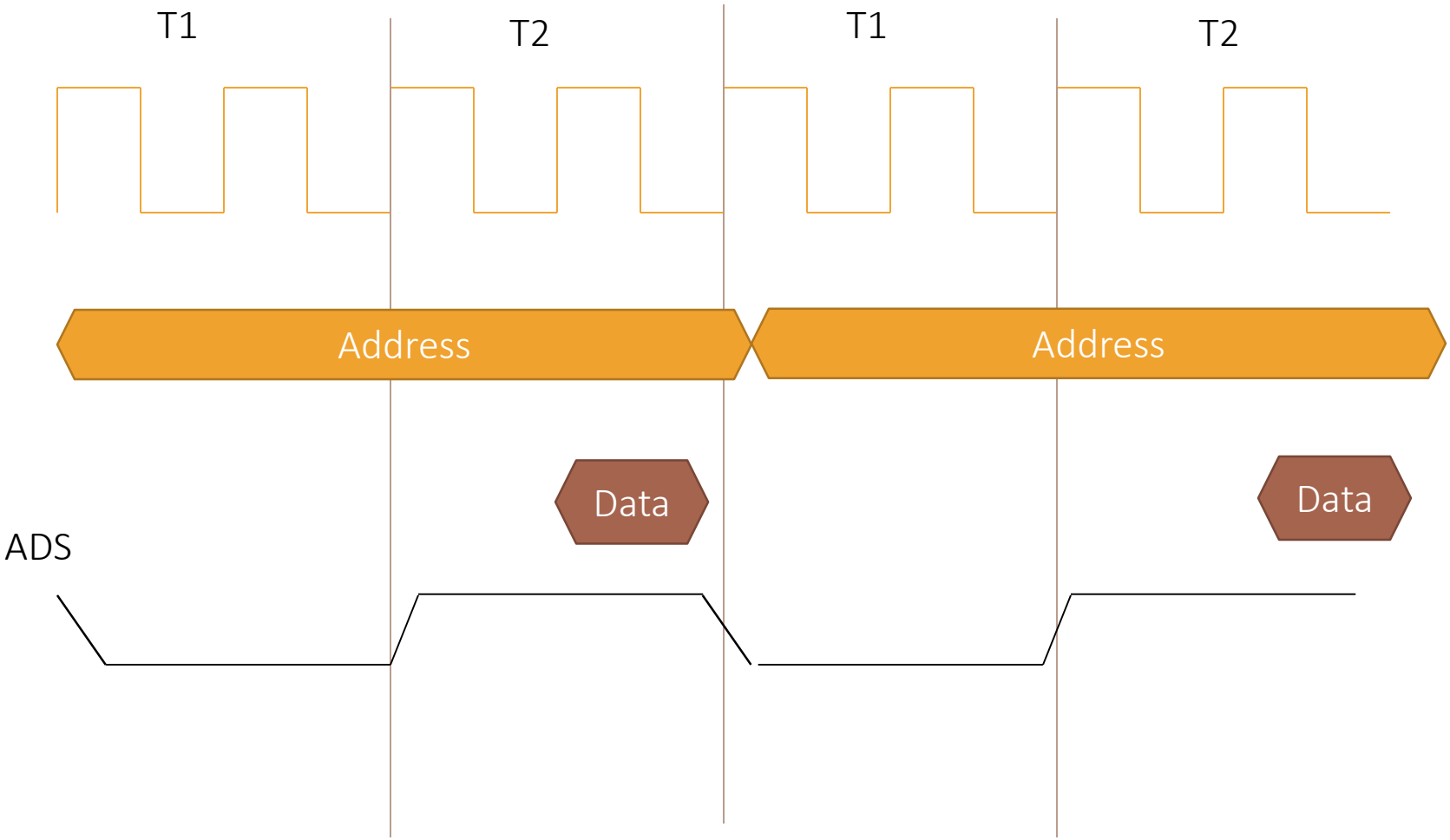
Bus Pipelining

Bus Pipelining

Split Transactions supported 80386

- Address
- Data

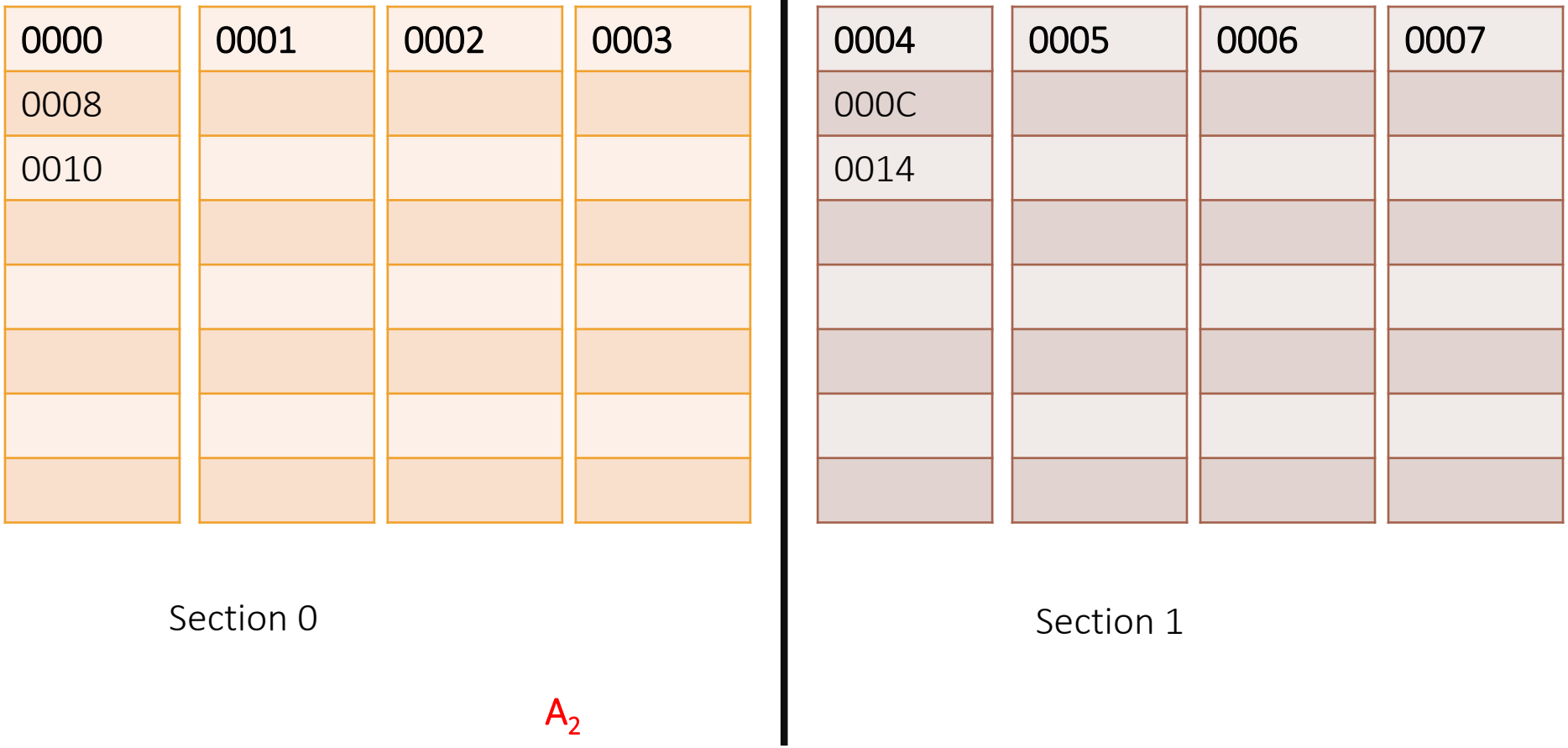
Non-Pipelined Bus



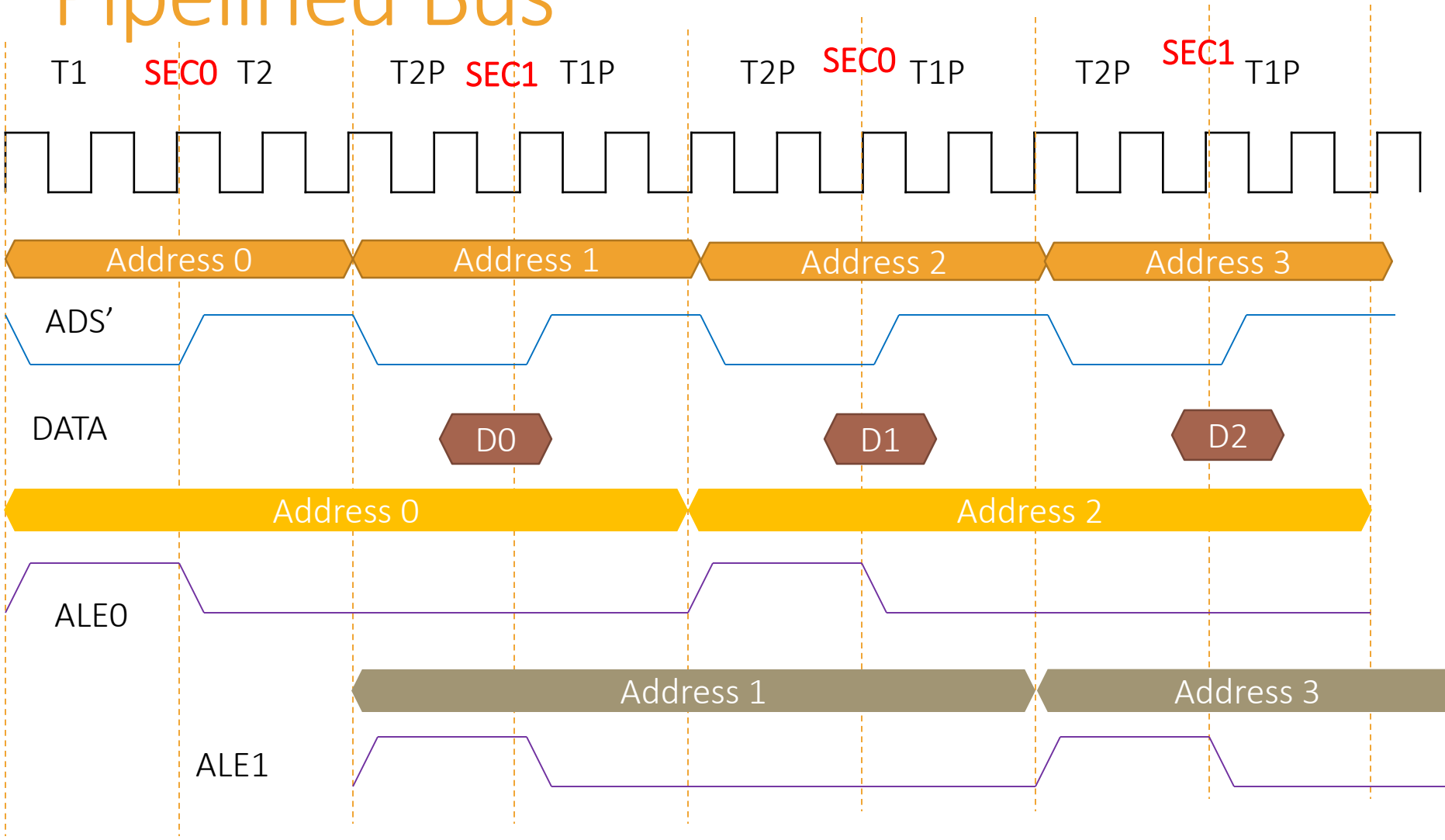
Pipeline

Memory Interleaving

Memory Interleaving



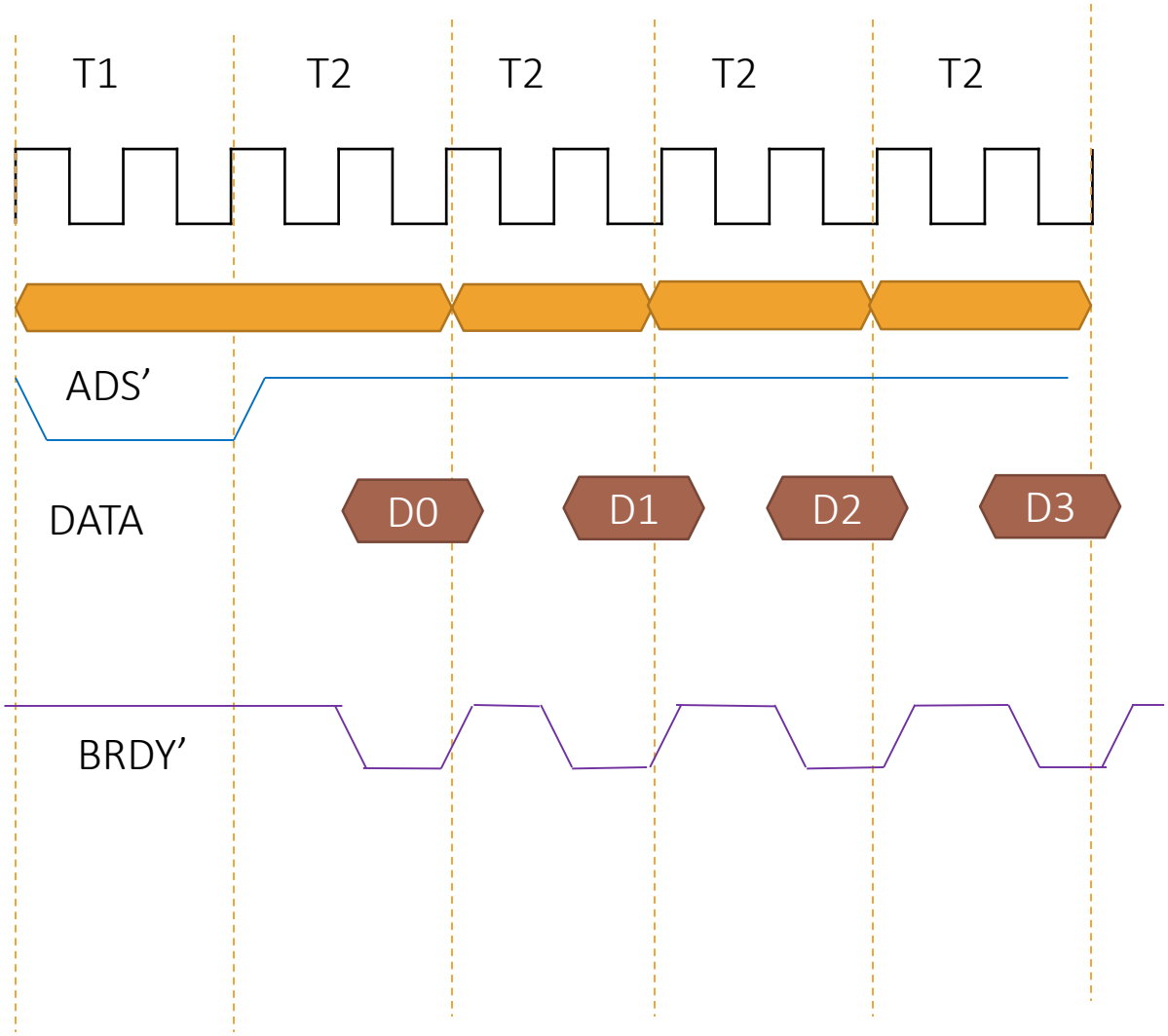
Pipelined Bus



80486

Burst Transfers

Burst Bus



Cache

Introduction & 80486 Cache

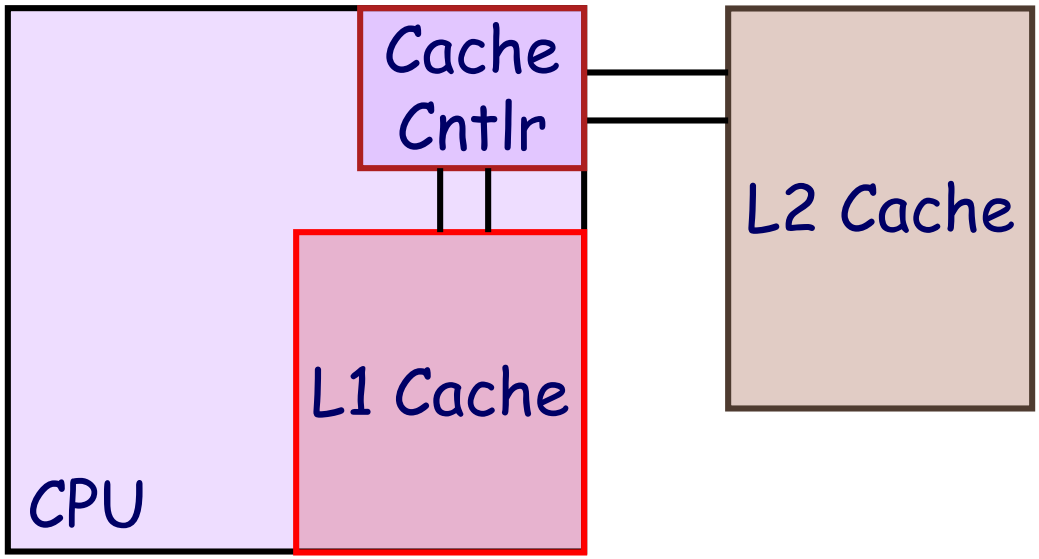
Cache Memory

Extreme Fast Memory

Internal/External to CPU

CPU uses cache memory to store instructions that are repeatedly required to run programs- working set

Cache hit/miss



Miss Types

Compulsory Miss/Cold Miss

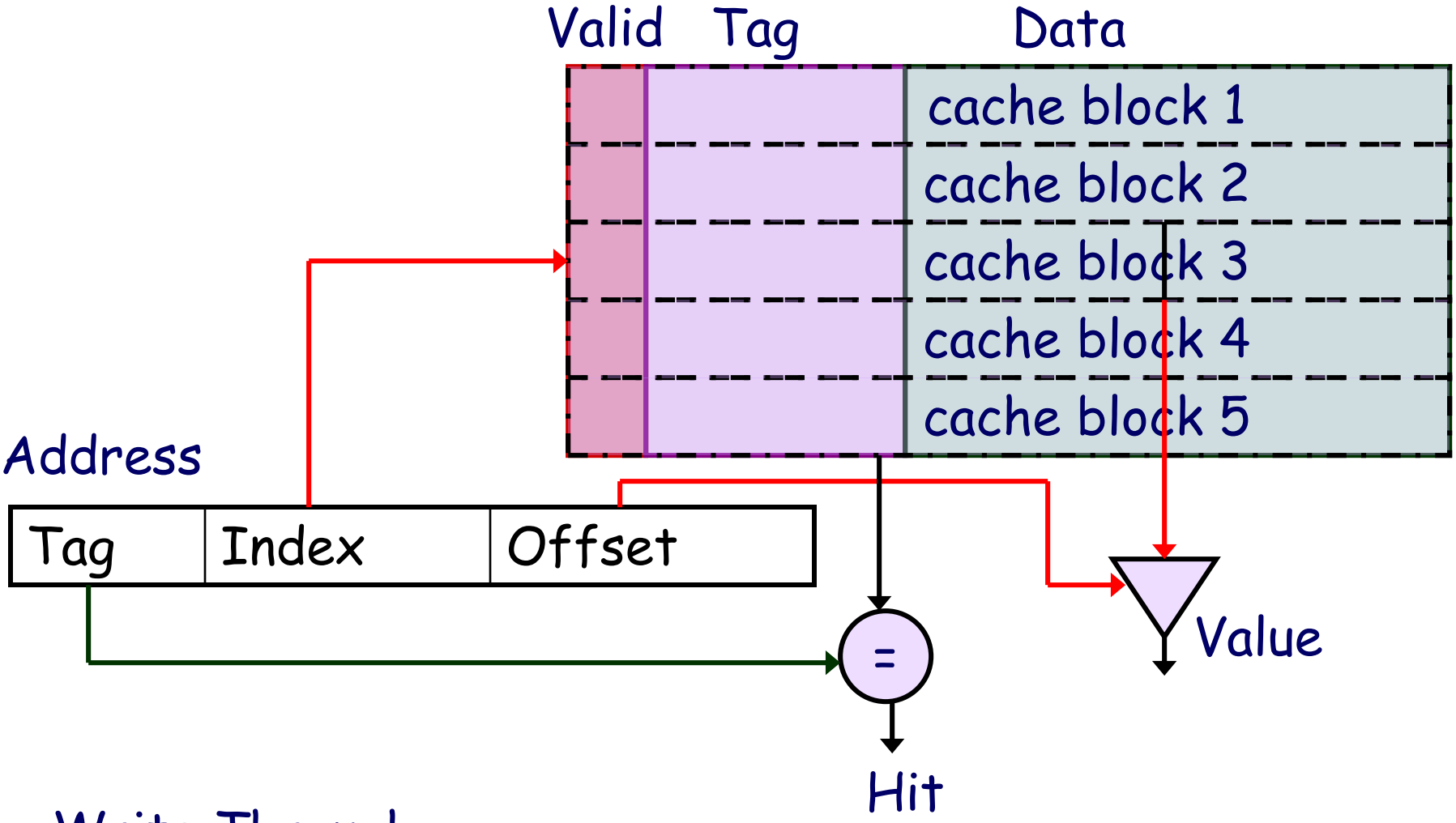
Capacity Miss

Conflict Miss

Cache Organization

Direct Mapped

Set Associative



Write Through

Write Back

001

100

010

101

Address	Data
000	0101
001	1111
010	0110
011	0000
100	1000
101	0001
110	1010
111	0100

Block	Tag	Data
00	1	1000
01	0	0001
10	0	0110
11	-	-

001

100

010

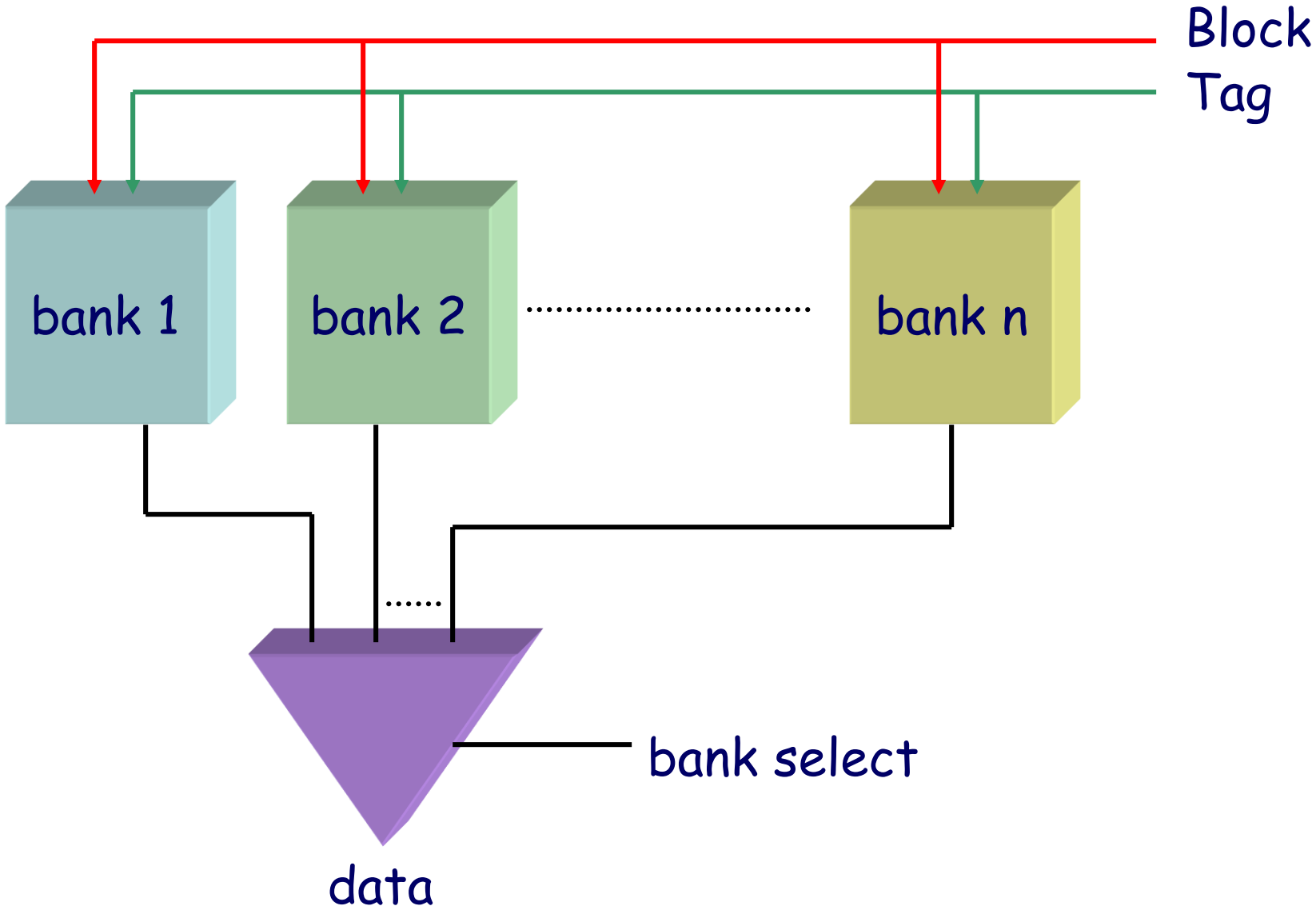
101

Address	Data
000	0101
001	1111
010	0000
011	0110
100	1000
101	0001
110	1010
111	0100

0	10	1000	01	0000
1	00	0101	10	0001

Block S0 Tag S0 Data S1Tag S1Data

Set Associative Cache


Block
Tag
bank 1
bank 2
bank n
bank select
data

Cache in 80486

Four way set associative cache

Each line – 16 bytes of data

Write Through Cache

4 ways -128 lines in each way – 16 bytes