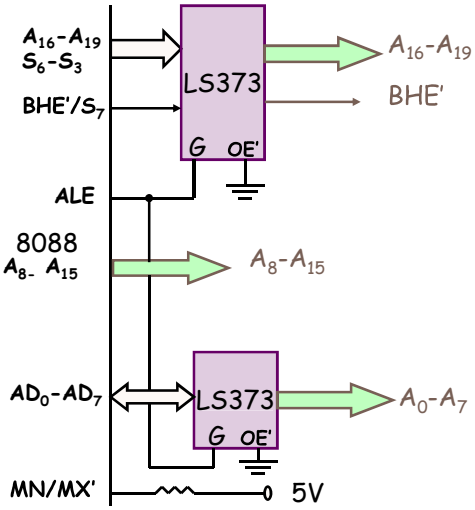
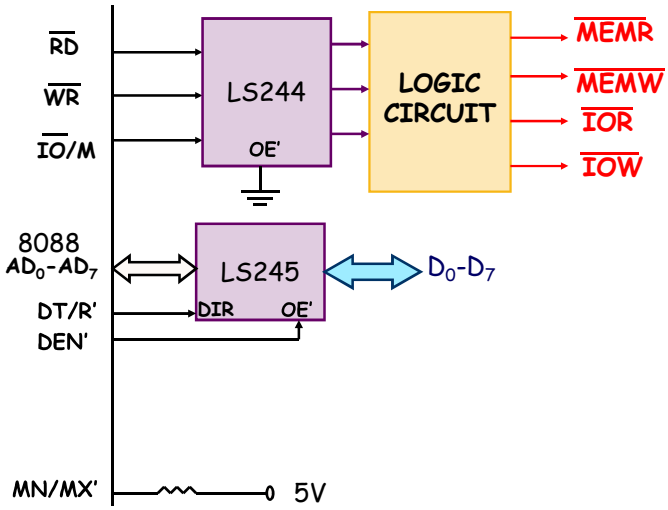
Memory

Interfacing to Processor

Memory Interfacing

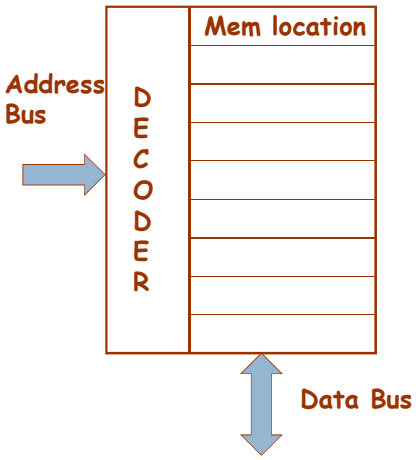
8088



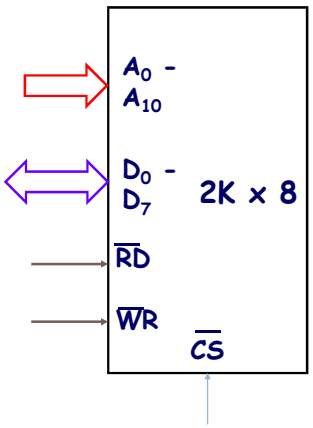


Memory

- Address Bus
- Data Bus
- Control Signals
- Based on the size of the chip



A 2K Memory Chip



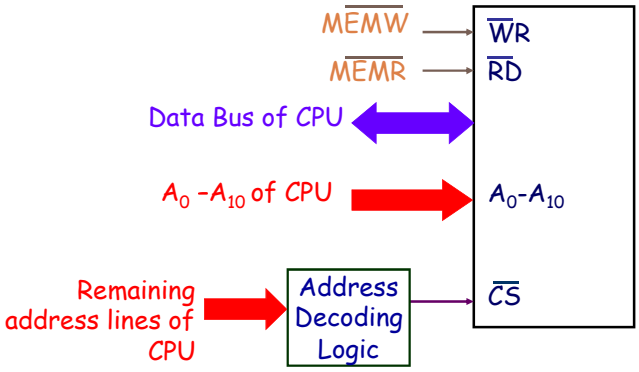
Interface using 2K Memory chips - 8 K bytes of Memory to 8088

- No of Memory chips
- Address Space
- Decoding logic

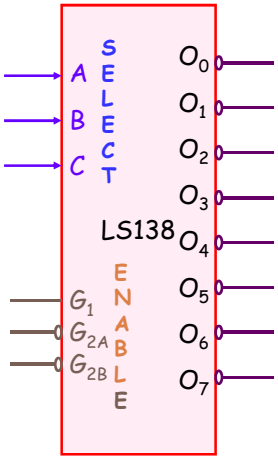
Memory Maps

- 8K Memory - 4 - 2K chips of memory
- Memory Mapping

RAM1	00000_H - $007FF_H$
RAM2	00800_H- $00FFF_H$
RAM3	01000_H- $017FF_H$
RAM4	01800_H-$01FFF_H$



Memory Address Decoding



INPUT						OUTPUT							
ENABLE			SELECT										
G_1	G_{2A}	G_{2B}	A	B	C	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

RAM_1 00000_H - $007FF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

RAM_2 00800_H- $00FFF_H$

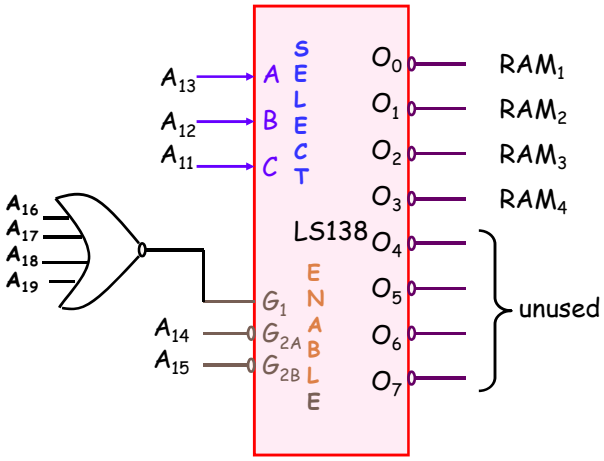
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM_3 01000_H-$017FF_H$

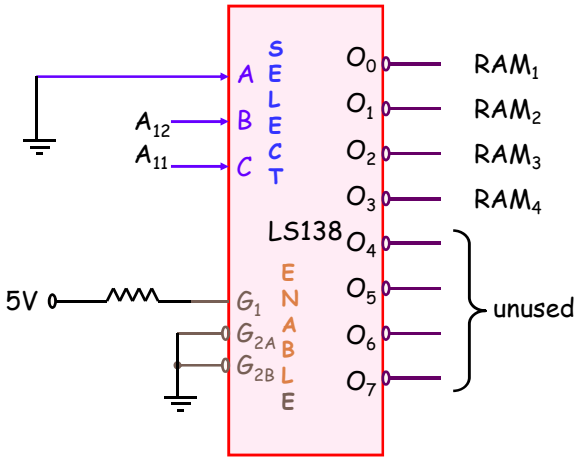
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1

RAM_4 01800_H-$01FFF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1



Absolute Addressing



Incremental Addressing

Memory Interfacing

For the memory chips available each do the interfacing for 8088

Ex: Interface

4K - 2716 (ROM) starting at 00000_H

8K - 6116 (SRAM) starting at 08000_H

Memory Requirements

2716 – ROM - size 2K (16/8)

ROM – 4k

Number of 2716 required – 2

6116 – RAM size 2k (16/8)

RAM – 8k

Number of 6116 required - 4

Memory Map

ROM $_1$ - 00000_H – $007FF_H$

ROM_2 - 00800_H – $00FFF_H$

RAM_1 - 08000_H – $087FF_H$

RAM_2 - 08800_H – $08FFF_H$

RAM_3 - 09000_H – $097FF_H$

RAM_4 - 09800_H – $09FFF_H$

ROM_1 00000_H - $007FF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

ROM_2 00800_H- $00FFF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM_1 08000_H-$087FF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

RAM_2 08800_H- $08FFF_H$

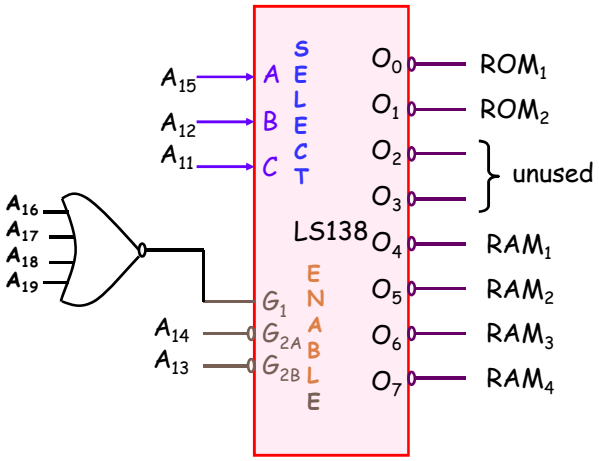
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM_3 09000_H-$097FF_H$

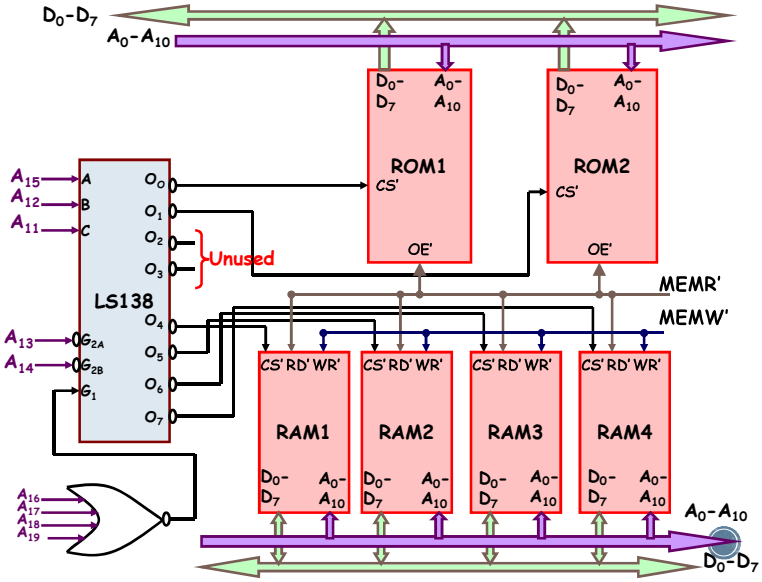
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1

RAM_4 09800_H-$09FFF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1



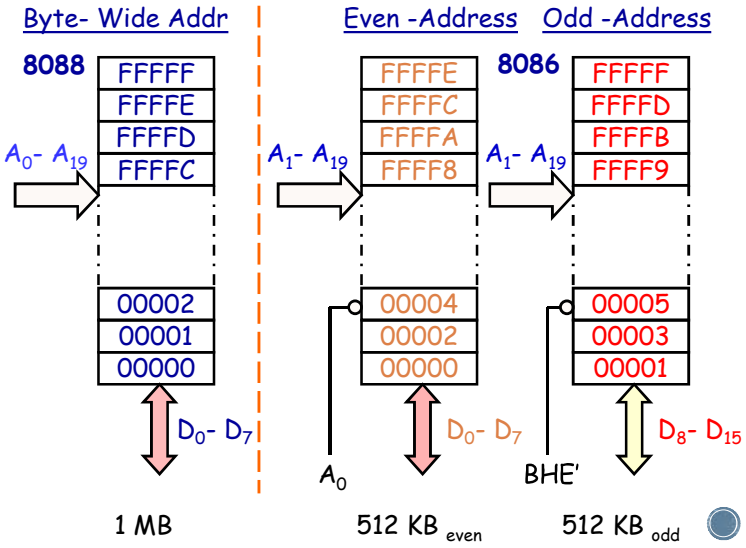
Absolute Addressing



Memory Interfacing

8086/80286

- 8086 has 20 bit address bus / 80286 has 24 bit address
- 1 MB / 16 MB - each address represent a byte
- An Inst such as MOV [$437A_H$] , BX
- Word written to two consecutive locations $0437A_H$ & $0437B_H$
- To complete the write in one cycle memory set up as two banks
- 512 K bytes each
- ODD Bank &
- EVEN Bank



BHE'	A_0	Selection
0	0	Whole Word
0	1	High byte to/from odd address
1	0	Low byte to/from even address
1	1	No Selection

Address	Data Type	BHE'	A_0	Bus Cycles	Data lines used
00000	Byte	1	0	one	D_0 -D_7
00000	Word	0	0	one	D_0 -D_{15}
00001	Byte	0	1	one	D_8 -D_{15}
00001	Word	0	1	first	D_8 -D_{15}
		1	0	second	D_0 -D_7

Memory Interfacing

8086/80286

If memory chips available are only 2KB each do the interfacing for 8086

Ex: Interface

4K 2716 (ROM) starting at 00000_H

8K 6116 (SRAM) starting at 08000_H

Memory Requirements

2716 – size 2K

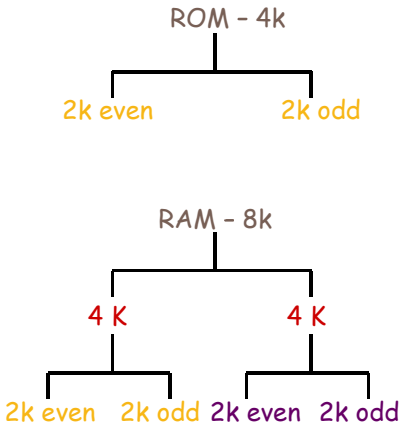
ROM – 4k

Number of 2716 – 2 ROM – 4k

6116 – size 2k

RAM – 8k RAM – 8k

Number of 6116 -4



Memory Map

ROM $_{1E}$ -	00000_H ,00002_H, 00004_H	$00FFE_H$
ROM $_{1O}$ -	00001_H, 00003_H, 00005_H	$00FFF_H$
RAM $_{1E}$ -	08000_H, 08002_H, 08004_H	$08FFE_H$
RAM $_{1O}$ -	08001_H, 08003_H, 08005_H	$08FFF_H$
RAM $_{2E}$ -	09000_H, 09002_H, 09004_H	$09FFE_H$
RAM $_{2O}$ -	09001_H, 09003_H, 09005_H	$09FFF_H$

ROM_1 00000_H – $00FFF_H$

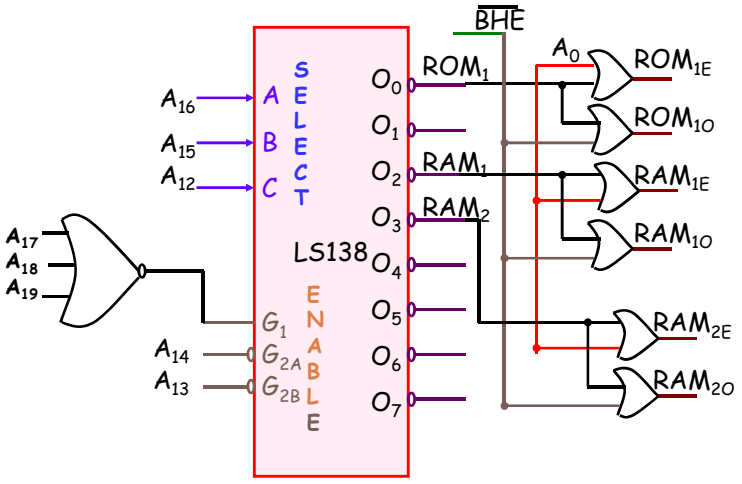
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM_1 08000_H- $08FFF_H$

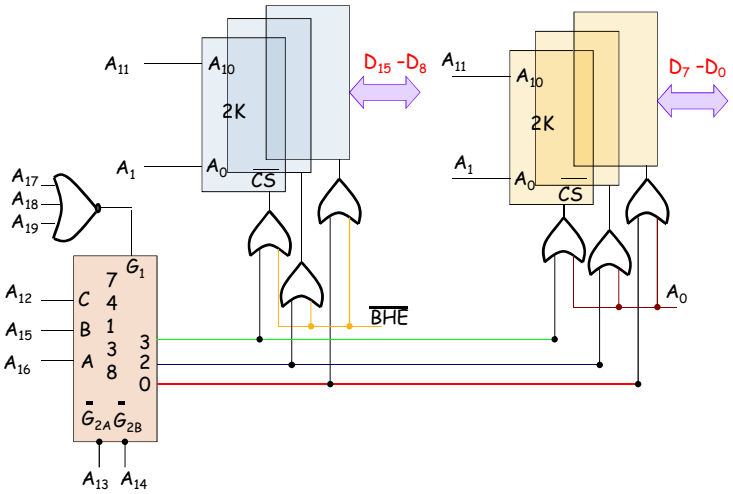
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM2 09000_H-$09FFF_H$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1



Absolute Addressing



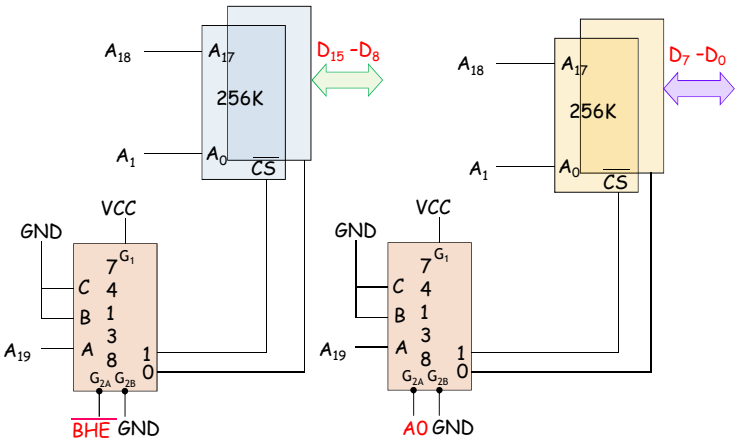
Memory Interfacing

8086-80286

Interface 1M of SRAM to 8086

Chips available are of size 256K each

A_{19}	$A_{18}A_{17}A_{16}$	$A_{15}A_{14}A_{13}A_{12}$	$A_{11}A_{10}A_9A_8$	$A_7A_6A_5A_4$	$A_3A_2A_1A_0$	
0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	512KB
0	1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	
1	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	512KB
1	1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	



Memory Interfacing

8086-80286

Interface 16K of RAM to 8086 starting at 00000_H

Chips available are 2KB(4 Chips) and 4KB (2 Chips)

RAM_{1even} 00000_H, 00002_H, 00004_H, ...$00FFE_H$

RAM_{1odd} 00001_H, 00003_H, 00005_H, ...$00FFF_H$

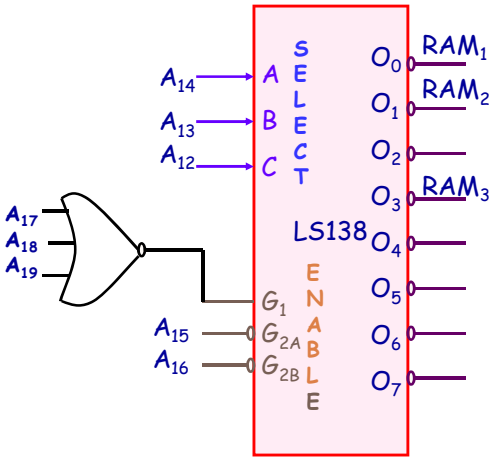
RAM_{2even} 01000_H, 01002_H, 01004_H, ...$01FFE_H$

RAM_{2odd} 01001_H, 01003_H, 01005_H, ...$01FFF_H$

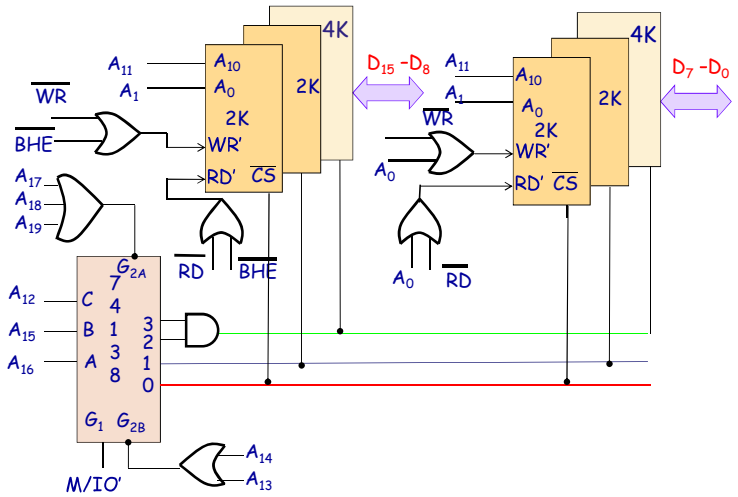
RAM_{3even} 02000_H, 02002_H, 02004_H, ...$03FFE_H$

RAM_{3odd} 02001_H, 02003_H, 02005_H, ...$03FFF_H$

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1



Absolute Addressing



Memory Interfacing

80286

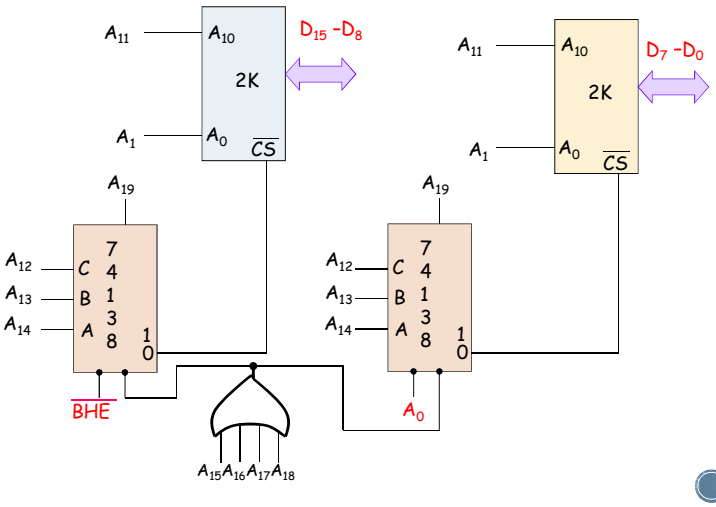
Interface 4K of ROM to 80286 starting at 080000_H

Chips available are 2716.

ROM_{even} $080000_H, 080002_H, 080004_H, \ldots\ldots\ldots 080FFE_H$

ROM_{odd} $080001_H, 080003_H, 080005_H, \ldots\ldots\ldots 080FFF_H$

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1



Memory Interfacing

80286

Interface 8K of ROM to 80286 starting at 080000_H
Chips available are 2 KB each

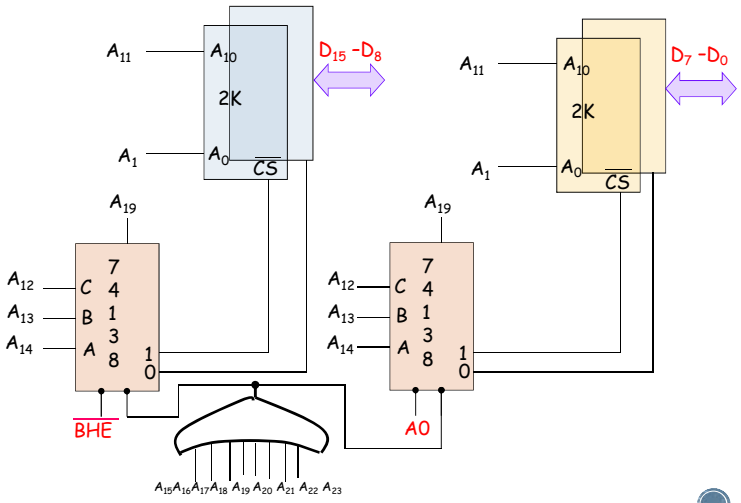
ROM_{1even} $080000_H, 080002_H, 080004_H, \ldots\ldots\ldots 080FFE_H$

ROM_{1odd} $080001_H, 080003_H, 080005_H, \ldots\ldots\ldots 080FFF_H$

ROM_{2even} $081000_H, 081002_H, 081004_H, \ldots\ldots\ldots 081FFE_H$

ROM_{1odd} $081001_H, 081003_H, 081005_H, \ldots\ldots\ldots 081FFF_H$

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1



Memory Interfacing

80386-80486

80386-80486

- 32-bit data bus
- Four banks of memory
- 80386 - SX & DX
- 386 DX/486
- BE'_0
- BE'_1
- BE'_2
- BE'_3

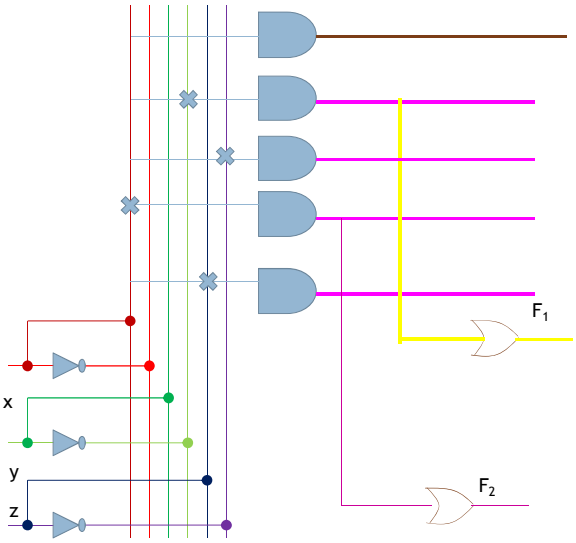
Write Strobes

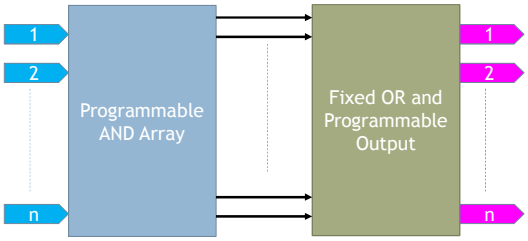
Memory Interfacing

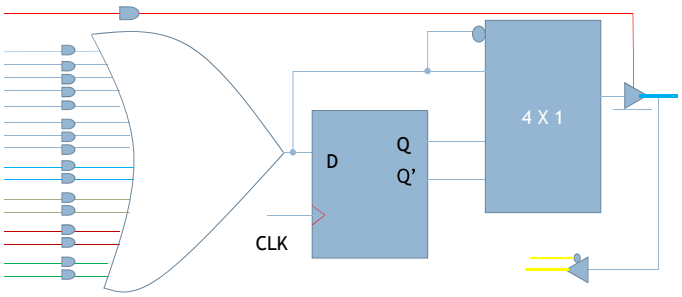
80386-80486

Decoding Done using PLD

- Generic Array Logic
- Programmable AND
- Fixed OR
- Output Stage
  - OLMC
    - Mux
    - FF
    - Tristate o/p buffers

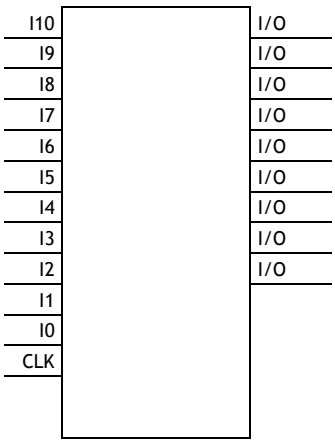






OLMC

GAL22V10C

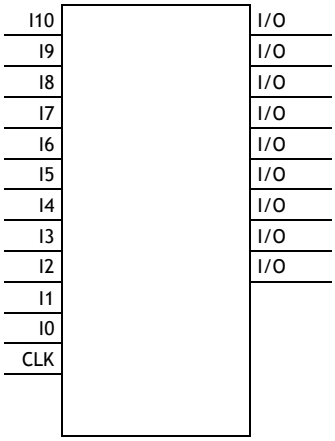


Memory Interfacing

80386-80486

Write Strobes

GAL22V10C



Memory Interface

- 1 M SRAM - 02 00 00 00_H
- MS621000 128 K x 8
- 4 Banks - 512K

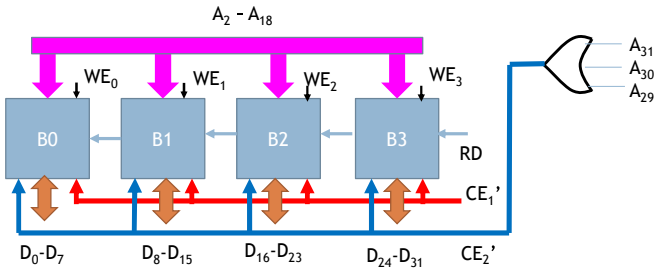
MS62100

- Address Lines - 17
- Data - 8
- OE'
- WE'
- CE'_1
- CE'_2

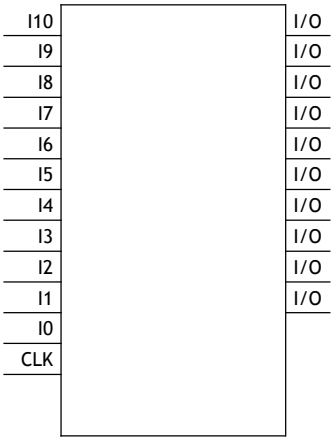
Memory Interface

- RAM1 - 02 00 00 00 - 02 07 FF FF
- RAM2 - 02 08 00 00 - 02 0F FF FF

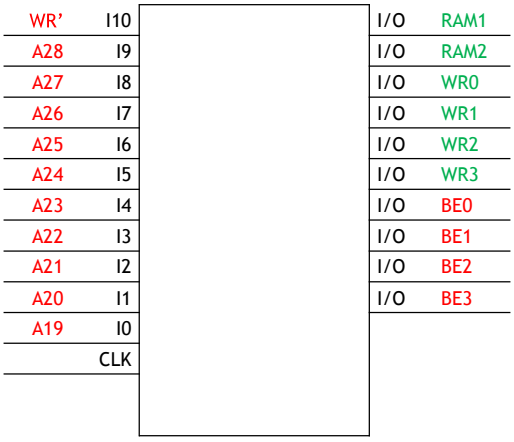
RAM Layout 02 00 00 00 02 07 FF FF



GAL22V10C



GAL22V10C



Program

```
port (
        A28, A27, A26, A25, A24, A23, A22, A21, A20, A19,
        BE0, BE1, BE2,BE3,WR: in STD_LOGIC
        RAM1, RAM2, WR0,WR1,WR2,WR3 :out STD_LOGIC
        );
```

Program

- WR0 <= BE0 OR WR
- WR1 <= BE1 OR WR
- WR2 <= BE2 OR WR
- WR3 <= BE3 OR WR

Program

RAM1 = A29 or A28 or A27 or A26 or Not (A25) or A24 or A23 or A22 or A21 or A20 or A19

RAM1 = A29 or A28 or A27 or A26 or Not (A25) or A24 or A23 or A22 or A21 or A20 or Not (A19)