MEMORY

Real & Protected Modes

REAL MEMORY

- First 1 MB
  - conventional memory
  - DOS Memory
- 8086/8088 – operate only in real mode
- Segment Registers & Monitors
  - Code
  - Data
  - Stack
  - Extra
  - FS & GS
- Maximum segment size 64 K
- Segments - Relocatability

PROTECTED MEMORY

- Above 1M
- Windows operate
- Segment + Offset
- Segment Register –*Selector – Selects Descriptor from Descriptor Table*
- Descriptor
  - Location
  - Length
  - Access Rights
- Instructions don't change as still it is segment-offset combo
- In 80386 & 80486 – 32-bit pointers possible

HOW DOES IT WORK?

- Two Descriptor Tables
  - Global / System
    - Apply to all programs
  - Local /Application
    - Apply to particular appln
- Each Descriptor Table has 8192 entries
  - 16,384 descriptors
  - 16,384 segments
  - 4G size (80386)
  - Virtually – 4G x 16K – 64T

MEMORY

Protected Modes- Descriptor

DESCRIPTOR

- 8 bytes
- Total memory for GDT /LDT – 64K
- 80286 – upward compatible

DESCRIPTOR - 80286

0000 0000	0000 0000
Access Rights	Base Address $B_{16} - B_{24}$
Base Address B_8- B_{15}	Base Address $B_0 - B_7$
Limit L_8 - L_{15}	Limit L_0 – L_7

DESCRIPTOR - 80386

Base Address $B_{24} - B_{31}$	G	D	0	AV	Limit $L_{16} - L_{19}$
Access Rights	Base Address $B_{16} - B_{24}$				
Base Address B_8- B_{15}	Base Address $B_0 - B_7$				
Limit L_8 - L_{15}	Limit L_0 – L_7				

EXAMPLE

- Base = Start = $1000\ 0000_H$
- G = 0
- Limit – $001FF_H$
- End = $1000\ 0000 + 001FF_H = 1000\ 01FF_H$
- G =1
- End = $1000\ 0000 + 001FF\ FFF = 101F\ FFFF_H$

MEMORY

Protected Modes- Descriptor – The Access Right Byte

ACCESS RIGHTS BYTE FORMAT

P	DPL	DPL	S	E	ED/C	R/W	A

E	ED/C	R/W	?
0	0	0	Data- Expands Upward – Read Only
0	0	1	Data- Expands Upward - Write
0	1	0	Data - Expand Downward – Read Only
0	1	1	Data- Expand Downward - Write
1	0	0	Code – Ignore DPL – Execute Only
1	0	1	Code – Ignore DPL – Read allowed
1	1	0	Code – Abide DPL – Execute Only
1	1	1	Code – Abide DPL – Read allowed

MEMORY

Protected Modes- Descriptor – Address Translation

ACCESS RIGHTS BYTE FORMAT

P	DPL	DPL	S	E	ED/C	R/W	A

ADDRESS TRANSLATION - SEGMENT

Selector (15-3)	TI	RPL	RPL

INVISIBLE REGISTERS

	Base Address	Limit	Access
CS			
DS			
ES			
SS			
FS			
GS			

	Base Address	Limit	Access
LDTR			
TR			

GDTR
IDTR

EXAMPLES

- DS:1000
- DS = 0018
- 1st 13 bits – 0000 0000 0001 1*000 - GDT*
- GDTR + 0018 (entry no. 3)
- GDTR – 00 00 00 00
- DS starts at – 00 20 00 00
- Linear Address

	00
	10
	93
	20
	00
	00
	FF
3	FF
2	
1	

MEMORY

Protected Modes- Descriptor – Address Translation

EXAMPLES

- MOV AX,[1000_H]
- DS:1000
- DS = 001C
- 1st 13 bits – 0000 0000 0001 1*100 - LDT*
- Selector – LDTR
- LDTR – 0018 – 0000 0000 0001 *1000*
- GDTR + 0018 (entry no. 3)
- GDTR – 00 00 00
- LDT starts at – 40 00 00

	00
	00
	93
	40
	00
	00
	FF
3	FF
2	
1	

INVISIBLE REGISTERS

	Base Address	Limit	Access
CS	40 00 00	FF FF	93
DS			
ES			
SS			
FS			
GS			

	Base Address	Limit	Access
LDTR			
TR			

GDTR
IDTR

EXAMPLES

- DS:1000
- DS = 001C
- 1st 13 bits – 0000 0000 0001 1*100 - LDT*
- Selector – LDTR
- LDTR + 0018 (entry no. 3)
- GDTR – 00 00 00
- DS starts at – 80 00 00
- Linear Address – 80 10 00

	00
	00
	93
	80
	00
	00
	00
3	FF
2	
1	

MEMORY

Real & Protected Modes- Paging

MEMORY – 8086 TO 80486

- Segment (SR) - Offset
- 8086 /8088 – Real mode
- Segment Value shifted left by 4 bits + offset – 20 –bit address
- 80286
  - Real Mode
  - Protected Mode
    - Segment Register – Selector – points to descriptor (LDT/GDT) – descriptor has starting address of segment – Starting Address + Offset
    - Virtual address – Physical Address (24-bits)
    - Segmentation

MEMORY – 8086 TO 80486

- 80386/80486
  - Real Mode
  - Protected Mode
    - Segment Register – Selector – points to descriptor (LDT/GDT) – descriptor has starting address of segment – Starting Address + Offset
    - Segmentation -Virtual address – Linear Address (32-bits)
    - Linear to Physical Address - Paging

DESCRIPTOR – 80386 - 80486

Base 24-31	G	D	0	A V	Limit 16-19	Access Rights	Base 16-23
Base 0-15						Limit	

ADDRESS TRANSLATION - SEGMENT

Selector (15-3)	TI	RPL	RPL

EXAMPLES

- DS:0000
- DS = 0018
- 1st 13 bits – 0000 0000 0001 1*000 - GDT*
- GDTR + 0018 (entry no. 3)
- GDTR – 00 00 00 00
- DS starts at – 00 00 20 00
- Linear Address

	00
	00
	93
	00
	20
	00
	FF
18	FF
	00
	00
	93
	40
	00
	00
	00
10	FF
08	

PAGING – 80386 ONWARDS

- Linear – physical
- CR0 – CR3
- Page directory – 1024 entries – 4 bytes – each point to Page Table
  - 1024 * 4 = 4k
- Page table – 1024 entries – 4 bytes – each point to Page
  - 1024 *4 =4k
- Total no.pages
  - 1024 * 1024 = 1 M
- Page block of 4k

LINEAR TO PHYSICAL

Directory 31-22	Page Table 21-12	Offset 11-0

00 00 20 00

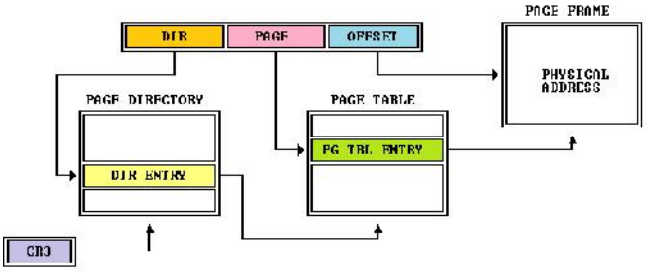
0000 0000 0000 0000 0010 0000 0000 0000

CR0 -3

- CR0 – MSB PG bit
- CR3 – BITS 12 -31- base address of Page Directory

PD/ PT ENTRY

Address (31-12)						D	A	PCD	PWT	U	W	P



LINEAR TO PHYSICAL

- 00 00 20 00
- 0000 0000 0000 0000 0010 0000 0000 0000
- CR3 – PD Base Address – 00 00 2 000
- Page Directory – 00 00 20 00 + *0000 0000 0000*$_b$
- PT address – 20 00 00 00
- PT Entry – 20 00 00 00 + *00 0000 10 00*$_b$
- PT Entry – 20 00 00 8
- Physical Address – 45 00 20 00 + 000

00002003	**20**
00002002	**00**
00002001	**00**
00002000	**03**

2000 000C	
2000 000B	45
2000 000A	00
2000 0009	20
2000 0008	00
2000 0007	
2000 0006	
2000 0005	
2000 0004	