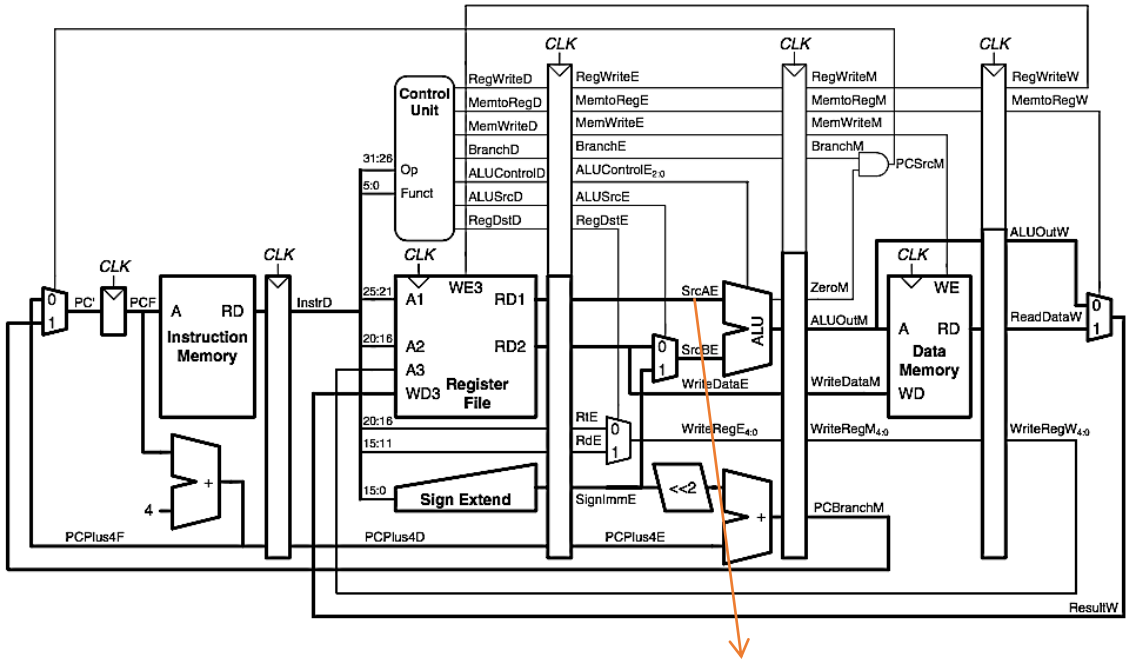
IMPORTANT: SUBMIT TOGETHER WITH PART-I OF THE FINAL EXAM!

Name-Last Name: _____ **Student ID:** _____

Questions	4	5
Marks	20	20
Earned		



SrcAE=0x0000 0005

Q4. a) The MIPS program below is executed on the pipelined architecture given above. At a time instant, we observe that SrcAE=0x0000 0005 as shown on the figure. At the same moment, write down the instructions in the following phases:

Fetch	Decode	Execute	Memory	Writeback
`and $s5,$t2,$t3`	`sub $s4,$t3,$t4`	`add $s3,$t1,$t2`	`lw $s2,40($0)`	`addi $t4,$0,5`

b) At the same moment, what are the values of the following signals?

Signal	Value
InstrD	`sub $s4,$t3,$t4`
SrcBE	6
ALUOutM	40
MemWriteM	0
WriteRegW	t4

MIPS program:

```
addi $t1, $0, 5
addi $t2, $0, 6
addi $t3, $0, 4
addi $t4, $0, 5
lw   $s2, 40($0)
add $s3, $t1, $t2
sub $s4, $t3, $t4
and $s5, $t2, $t3
sw   $s6, 20($t1)
or   $s7, $t3, $t4
```

Q4. A cache has the following parameters: *b*, block size given in numbers of words; *S*, number of sets; *N*, number of ways; and *A*, number of address bits. The following repeating sequence of lw addresses (given in hexadecimal) are retrieved in a loop which is executed **three times**.

40 44 48 4C 70 74 78 7C 80 84 88 8C

Assuming least recently used (LRU) replacement for associative caches, determine the miss rate at each loop if the sequence is input to the following caches. Cache is empty at the beginning.

a) direct mapped cache,
S = 16, b = 1 word

Data	
7C	Set 15
78	Set 14
74	Set 13
70	Set 12
	Set 11
	Set 10
	Set 9
	Set 8
	Set 7
	Set 6
	Set 5
	Set 4
4C 8C	Set 3
48 88	Set 2
44 84	Set 1
40 80	Set 0

	No of hits	No of misses
1st loop	0	12
2nd loop	4	8
3rd loop	4	8

b) 2-way associative cache
S=8, *b*=1 word

Way 1 Data	Way 0 Data	
	7C	Set 7
	78	Set 6
	74	Set 5
	70	Set 4
8C	4C	Set 3
88	48	Set 2
84	44	Set 1
80	40	Set 0

	No of hits	No of misses
1st loop	0	12
2nd loop	12	0
3rd loop	12	0

c) direct mapped cache,
S=8, b=2 words

Data	Data	
7C	78	Set 7
74	70	Set 6
		Set 5
		Set 4
		Set 3
		Set 2
4C 8C	48 88	Set 1
44 84	40 80	Set 0

	No of hits	No of misses
1st loop	6	6
2nd loop	8	4
3rd loop	8	4