Hacettepe University
Computer Engineering Department
BBM234 Computer Organization

Homework 1

Assigned date : 1.3.2018
Due date : 13.3.2018 (Section 1)
: 15.3.2018 (Section 2)

You must hand in your homework in class.
Don't email your homework! Stamp your homework papers. Do not put them in the plastic bags.
LATE HOMEWORKS WILL NOT BE ACCEPTED…

Questions: (Each one is 20 points.)

Q1. Suppose two programmers wrote different programs (P1 and P2) for the same problem. The instruction types, their clock cycles, and number of instructions for P1 and P2 programs are given in the following table. Suppose the frequency of the processor is 1GHz.

Instruction types	Clock cycles for Instructions	Percentage of instructions for P1 (%)	Percentage of instructions for P2 (%)
A	4	40%	25%
B	2	30%	25%
C	1	30%	50%

a) Calculate the average CPI for P1 and P2.
b) If P1 has 10 billion and P2 has 12 billion instructions, what are the execution times in second for P1 and P2?

- Weighted average CPI

$$CPI = \frac{\text{Clock Cycles}}{\text{Instruction Count}} = \sum_{i=1}^{n} \left(CPI_i \times \underbrace{\frac{\text{Instruction Count}_i}{\text{Instruction Count}}}_{\text{Relative frequency}} \right)$$

$$\text{CPU Time} = \text{Instruction Count} \times CPI \times \text{Clock Cycle Time} = \frac{\text{Instruction Count} \times CPI}{\text{Clock Rate}}$$

a) P1: 4×40% + 2×30% + 1×30% = 2.5

P2: 4×25% + 2×25% + 1×50% = 2.0

b) P1: $10\times10^9 \times 2.5 / 10^9 = 25$ s

P2: $12\times10^9 \times 2.0 / 10^9 = 24$ s

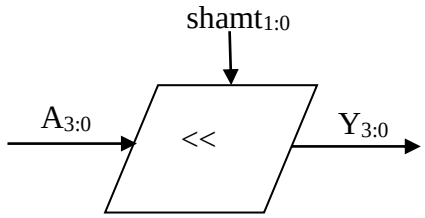
Q2. **a)** Show how to represent -12 and +12 in 8 bits in signed magnitude and two's complement formats. Then, express them in hexadecimal form.

	Signed Magnitude		Two's complement	
	8 bits	Hexadecimal	8 bits	Hexadecimal
-12	10001100	0x8C	11110100	0xF4
+12	00001100	0x0C	00001100	0x0C

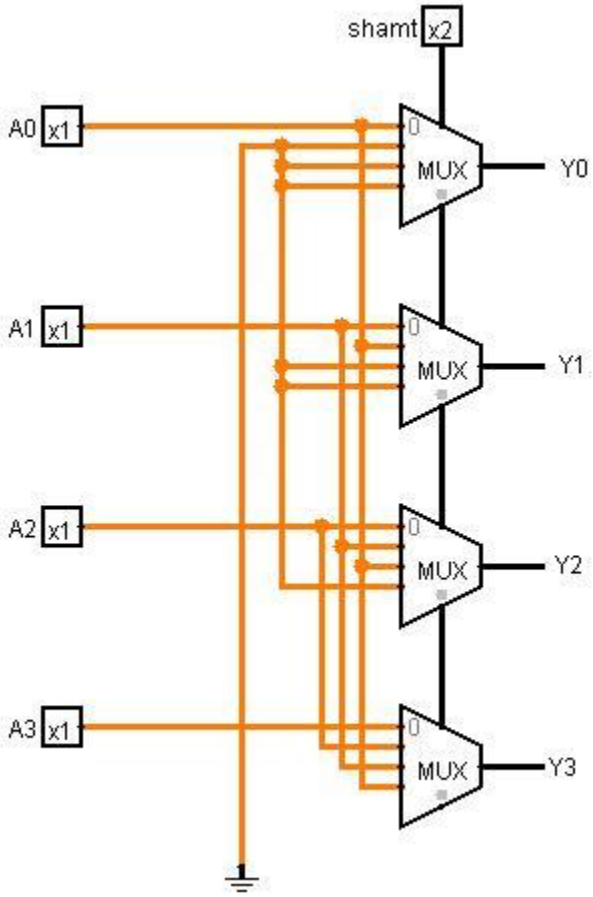
b) Suppose following numbers are represented in two's complement number system, what are their decimal and hexadecimal values?

Number	Decimal value	Hexadecimal value
001010	10	0x0A
111010	-6	0x3A
01010	10	0x0A
11010	-6	0x1A

Q3. You are to design a shifter that shifts the given four-bit number ($A_{3:0}$) to the left by the shift amount ($shamt_{1:0}$) and determines the shifted output ($Y_{3:0}$). The sketch of the shifter is given below. Design this shifter by using only four 4x1 Multiplexers.



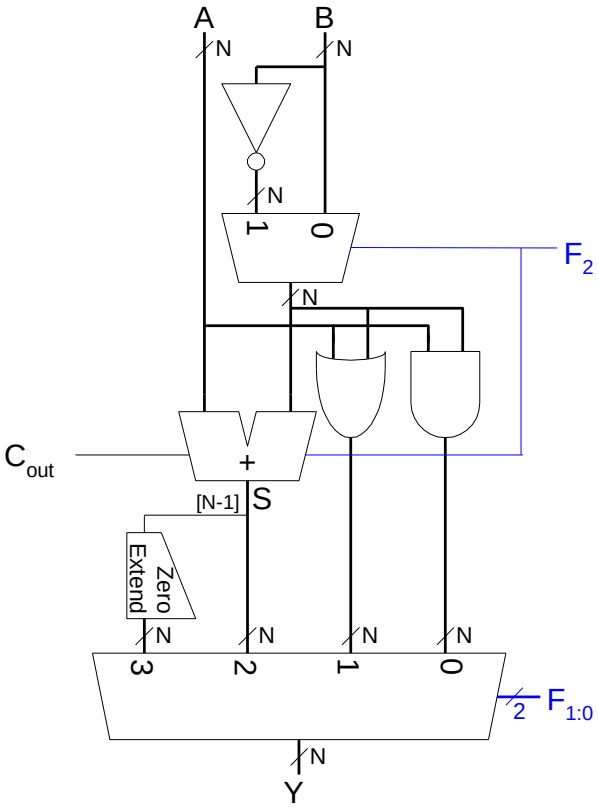
$shamt_{1:0}$	**Y_3**	**Y_2**	**Y_1**	**Y_0**
00	A_3	A_2	A_1	A_0
01	A_2	A_1	A_0	0
10	A_1	A_0	0	0
11	A_0	0	0	0



Q4. Consider the ALU given below. This ALU has N bits A and B inputs and 3 bits F input to control the operation mode of the ALU. It outputs N bits output Y based on the selected operation. We would like add more functionality to this ALU.

a) Add a single bit output to this ALU and name this signal as *zero*. The output *zero* must be 1, whenever the result Y equals to zero (That is if Y=0, *zero*=1). Otherwise, *zero*=0.
b) Add another output signal to the ALU and name it as LTEZ (Less Than Equal to Zero). LTEZ=1 when the result is less than or equal to zero (i.e., Y<=0). Otherwise, LTEZ=0.

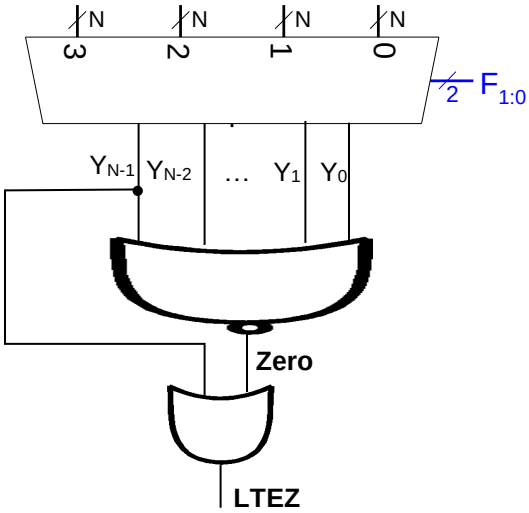
Show your additional circuits on the ALU and explain them.



$F_{2:0}$	Function
000	A & B
001	A | B
010	A + B
011	not used
100	A & ~B
101	A | ~B
110	A - B
111	SLT

Y_{N-1}	Y_{N-2}	…	Y_1	Y_0	Zero
0	0	0	0	0	1
0	0		0	1	0
0	0		1	0	0
0	0		1	1	0
.	.	.	.	.	0
.	.	.	.	.	0

NOR



Y_{N-1}	Zero	LTEZ
0	0	0
0	1	1
1	0	1
1	1	X

XOR/OR

Q5. In Fig. 1, we give a 3-ported register file with 2 read and 1 write ports. When addresses A1 and A2 are applied to the input, the values of the selected registers are read at the outputs RD1 and RD2, respectively. Similarly, when the address of the register is given at the A3 input to select the register and the data is given to the WD3 inputs and the WE3 (Write Enable) signal is one, the data is written to the selected register. The possible write port design is given in Fig. 2.

In this problem, you are asked to add another write port to the register file (A4 and WD4 inputs). In other words, we will be able to write two separate data to two registers. Show the sketch of your design by drawing the digital circuits inside of this register file. Draw a similar sketch as the one in Fig. 2.

Fig. 1: Register file

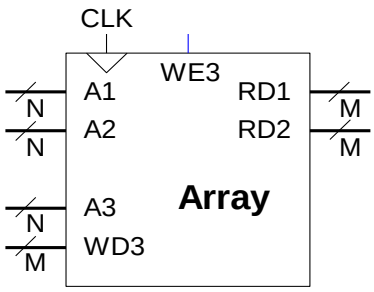
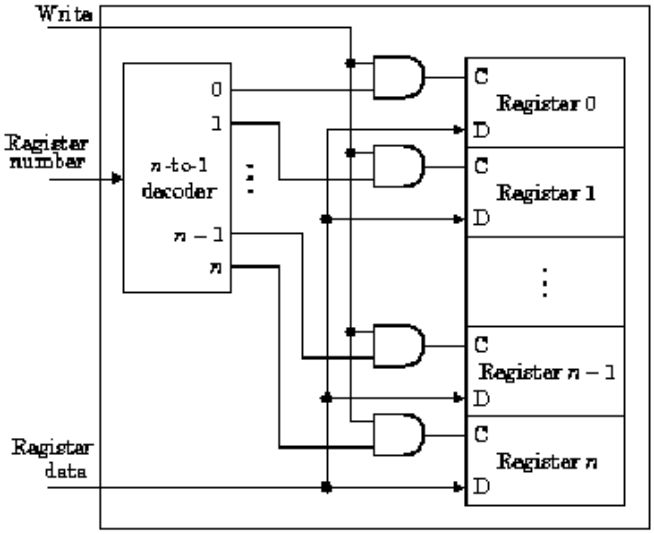


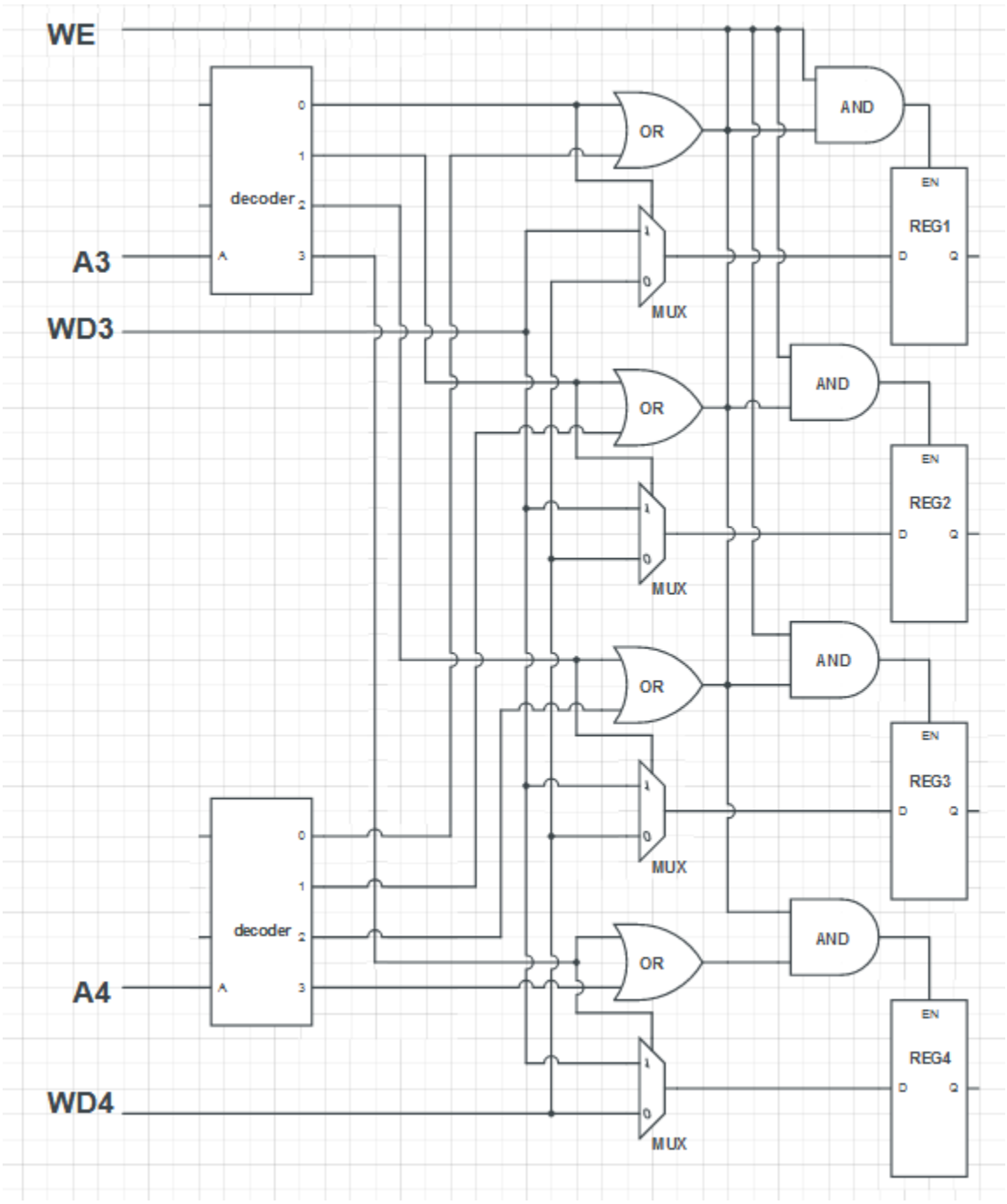
Fig.2: Write logic for register file



Solution:

Another decoder needs to be added in order to resolve the address A4. Decoder outputs for each register need to be OR'ed (since either address may point to that register) before they are AND'ed with WE. To select which data will be written, WD3 and WD4 should go through a multiplexer for which we can choose the corresponding output of the A3 decoder as the select line. In this case WD3 should be connected to the input 1 of the multiplexer (to give priority to A3 in case A3 and A4 are the same).

For the sake of simplicity, a circuit sketch is given for a Register File of size four (see the next page).


WE
A3
WD3
A4
WD4
decoder
decoder
A
A
0
1
2
3
OR
OR
OR
OR
AND
AND
AND
AND
MUX
MUX
MUX
MUX
1
0
EN
D
Q
REG1
REG2
REG3
REG4