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Final	
Duration: 120 minutes	Exam Date: 05.06.2018

Questions	1	2	3	4	5	Total
Marks	20	20	30	20	10	100
Earned						

Q1. You are given the following MIPS function (funct) and data memory.

```
funct:
       la $t1, array
       addi $t2, $0, 9
       addi $t3, $0, 0
        addi $s0, $0, 0

loop:  beq $t2, $t3, done
       lw $t4, 0($t1)
       lw $t5, 4($t1)
       bne $t4, $t5, L1
       sw $0, 0($t1)
        addi $s0, $s0, 1
L1:    addi $t3, $t3, 1
       addi $t1, $t1, 4
       j loop
done:  add $v0, $s0, $0
```

Address	Data
.	
.	6
.	5
.	4
.	4
.	3
.	3
.	2
.	2
0x1234ABC4	1
0x1234ABC0	1

array in the memory before program execution

a) [5 points] "la $t1, array" in funct is a pseudo instruction, which loads the address of the first array element to t1. Write the corresponding MIPS code for "la $t1, array".

Pseudo instruction	MIPS code
la $t1, array	**lui $t1, 0x1234** **ori $t1, $t1, 0xABC0**

b) [10 points] Write the data in the memory below after program execution.

Address	Data
.	
.	**6**
.	**5**
.	**4**
.	**0**
.	**3**
.	**0**
.	**2**
.	**0**
0x1234ABC4	**1**
0x1234ABC0	**0**

c) [5 points] What is the value returned in v0 register?

v0	**4**

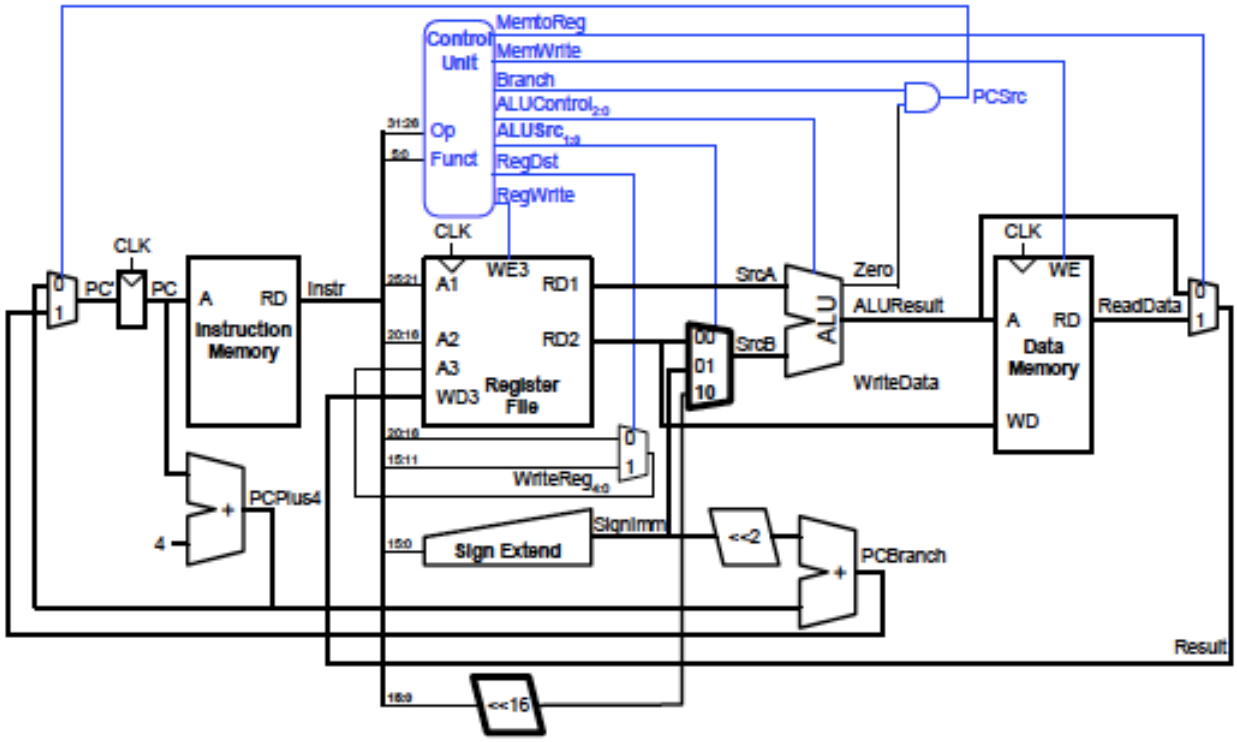
Q2. Modify the MIPS processor so that it can perform the lui instruction. Remember that the lui instruction loads the value in the 16-bit immediate field of the instruction into the upper 16 bits of the destination register. The instruction lui $s0, 2 would load the 16-bit representation of "2" into the upper 16 bits of register $s0. The machine code fields are as follows:

opcode-field	rs-field	rt-field	immediate-field
0xf	0	rt	imm
6 bits	5 bits	5 bits	16 bits

The MIPS Single-Cycle Processor Datapath is given below for your convenience.

a) Show any changes necessary on the single-cycle data-path. [12]
b) Fill out the control signal table for single cycle processor. [8]

a)



b)

Table I: Control signals for lui instruction

Instr.	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$
lui	001111	**1**	**0**	**10**	**0**	**0**	**0**	**00**

Q3. A cache has the following parameters: *b*, block size given in numbers of words; *S*, number of sets; *N*, number of ways; and *A=32*, number of address bits. LRU replacement is used.

You are given the following MIPS code with the lw addresses given in hexadecimal. Suppose C=8 words and b=1 word. Assume the cache is initially empty. Answer the following questions.

For all questions, show where the addresses 4, 24, 0, and 20 are mapped on the figures.

```
# MIPS assembly code
        addi $t0, $0, 2
loop:   beq  $t0, $0, done
        lw   $t1, 0x4($0)
        lw   $t2, 0x24($0)
        lw   $t3, 0x0($0)
        lw   $t3, 0x20($0)
        addi $t0, $t0, -1
        j    loop
done:
```

a) If N=1 (direct mapped), what is the miss rate?

	Set 7 (111)
	Set 6 (110)
	Set 5 (101)
	Set 4 (100)
	Set 3 (011)
	Set 2 (010)
0x4 0x24	Set 1 (001)
0x0 0x20	Set 0 (000)

Miss Rate = **8/8 = 100%**

b) If N=2, what is the miss rate?

Way 1	Way 0	
		Set 3 (11)
		Set 2 (10)
0x24	**0x4**	Set 1 (01)
0x20	**0x0**	Set 0 (00)

Miss Rate = **4/8 = 50%**

c) If N=1 and b=2, what is the miss rate?

Block 1	Block 0	
		Set 3 (11)
		Set 2 (10)
		Set 1 (01)
0x4 0x24	**0x0 0x20**	Set 0 (00)

Miss Rate = **8/8 = 100%**

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d) If N=2 and b=2, what is the miss rate?

Way 1		Way 0		
Block 1	Block 0	Block 1	Block 0	
				Set 1 (1)
0x24	**0x20**	**0x4**	**0x0**	Set 0 (0)

Miss Rate = **2/8 = 25%**

Q4. In the following table, the access time of CPU to the different components are given. Suppose the CPU accesses **100 instructions in the same block**. Assume the block is initially in the main memory and both TLB and cache are initially empty.

Access time (Clock Cycle)		
Cache	TLB	Main memory
1	1	10

a) How many clock cycles does it take to access 100 instructions **if there is no TLB in the architecture**?
Since there is no TLB, CPU must access to page table in main memory for every virtual to physical address translation. For data access, the first one is miss, others will be hit in the cache.
100 x 10cc (100 accesses to page table) + 100 x 1cc (cache accesses) + 1 x 10cc (miss penalty for the first miss) = 1110 clock cycles

Answer: **1110**

b) How many clock cycles does it take to access 100 instructions **if there is a TLB in the architecture**?
Since there is TLB, the first TLB access will be miss and the others will be hit in TLB. Same for the cache.

1 x 1cc (first TLB access) + 1 x 10cc (TLB miss penalty for the first miss) + 1 x 1cc (first cache accsess) + 1 x 10cc (cache miss penalty for the first miss) + 99 x 1 (TLB hits) + 99 x 1 (cache hits) = 220 clock cycles

Answer: **220**

Q5. Suppose we have a 1GB main memory and 1KB cache. Block size is 32B and associativity is 4 for the cache.

a) What is the minimum number of bits to address main memory? [3]
1 GB = 2^{30} Bytes => 30 bits necessary for address

Answer: **30**

b) What is the maximum number of sets in the cache? [4]

Cache = 1 KB = 2^{10} Bytes, b = 32 B = 2^5 Bytes => B= => $2^{10}/2^5=2^5$ (number of block in cache)
Associativity = 4 = 2^2 => $S=2^5/2^2=2^3$

Answer: **8**

c) What is the number of tag bits for each block address? [3]

30 – 5 (bits of Block Offset, including byte offset) – 3 (set bits) = 22

Answer: **22**