Hacettepe University
Computer Engineering Department
BBM234 Computer Organization
2017-2018 Spring Term

Homework 1

Assigned date : 2.3.2018
Due date : 13 or 15 March, 2018

You must hand in your homework in class. It does not matter in which day you submit your homework, either 13th or 15th of March. Don't email your homework!
LATE HOMEWORKS WILL NOT BE ACCEPTED…

Questions: (Each one is 20 points.)

Q1. Suppose two programmers wrote different programs (P1 and P2) for the same problem. The instruction types, their clock cycles, and number of instructions for P1 and P2 programs are given in the following table. Suppose the frequency of the processor is 1GHz.

Instruction types	Clock cycles for Instructions	Percentage of instructions for P1 (%)	Percentage of instructions for P2 (%)
A	4	40%	25%
B	2	30%	25%
C	1	30%	50%

a) Calculate the average CPI for P1 and P2.
b) If P1 has 10 billion and P2 has 12 billion instructions, what are the execution times in second for P1 and P2?

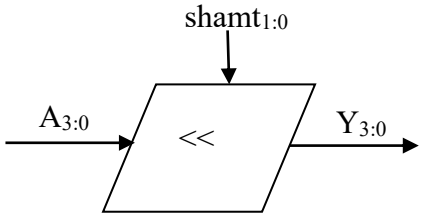
Q2. **a)** Show how to represent -12 and +12 in 8 bits in signed magnitude and two's complement formats. Then, express them in hexadecimal form.

	Signed Magnitude		Two's complement	
	8 bits	Hexadecimal	8 bits	Hexadecimal
-12				
+12				

b) Suppose following numbers are represented in two's complement number system, what are their decimal and hexadecimal values?

Number	Decimal value	Hexadecimal value
001010		
111010		
01010		
11010		

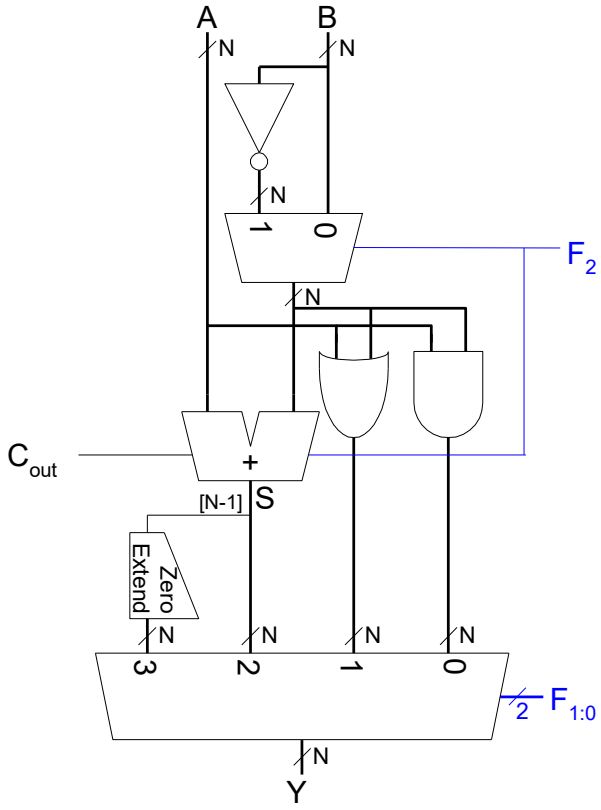
Q3. You are to design a shifter that shifts the given four bit number ($A_{3:0}$) to the left by the shift amount ($shamt_{1:0}$) and determines the shifted output ($Y_{3:0}$). The sketch of the shifter is given below. Design this shifter by using only four 4x1 Multiplexers.



Q4. Consider the ALU given below. This ALU has N bits A and B inputs and 3 bits F input to control the operation mode of the ALU. It outputs N bits output Y based on the selected operation. We would like add more functionality to this ALU.

a) Add a single bit output to this ALU and name this signal as *zero*. The output *zero* must be 1, whenever the result Y equals to zero (That is if Y=0, *zero*=1). Otherwise, *zero*=0.
b) Add another output signal to the ALU and name it as LTEZ (Less Than Equal to Zero). LTEZ=1 when the result is less than or equal to zero (i.e., Y<=0). Otherwise, LTEZ=0.

Show your additional circuits on the ALU and explain them.



$F_{2:0}$	Function

Q5. In Fig. 1, we give a 3-ported register file with 2 read and 1 write ports. When addresses A1 and A2 are applied to the input, the values of the selected registers are read at the outputs RD1 and RD2, respectively. Similarly, when the address of the register is given at the A3 input to select the register and the data is given to the WD3 inputs and the WE3 (Write Enable) signal is one, the data is written to the selected register. The possible write port design is given in Fig. 2.

In this problem, you are asked to add another write port to the register file (A4 and WD4 inputs). In other words, we will be able to write two separate data to two registers. Assume A3 has priority over A4 in case two are the same.

Show the sketch of your design by drawing the digital circuits inside of this register file. Draw a similar sketch as the one in Fig. 2.

Fig. 1: Register file

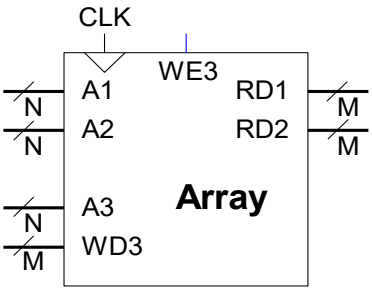


Fig.2: Write logic for register file