

**HACETTEPE UNIVERSITY**  
**DEPARTMENT OF COMPUTER ENGINEERING**  
**BBM231 LOGIC DESIGN**

**Homework 4 (For all sections)**

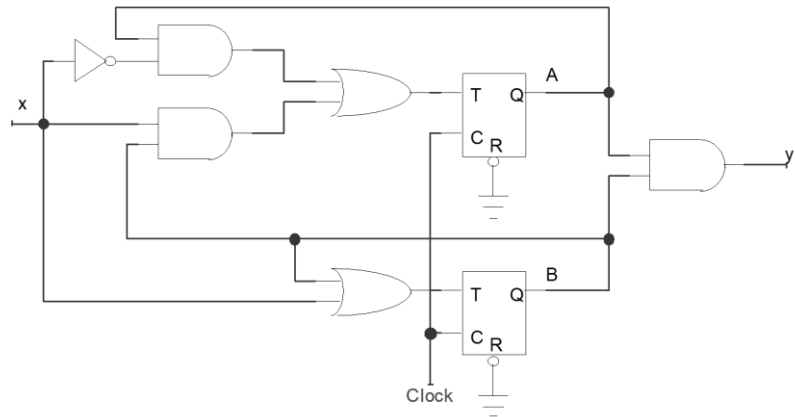
**Assigned : 12.12.2018**

**Due : 17.12.2018**

**QUESTIONS:**

**Q1.** For the sequential circuit given at right, find:

- Input equations and state table.
- State equations and output equation.
- State diagram.

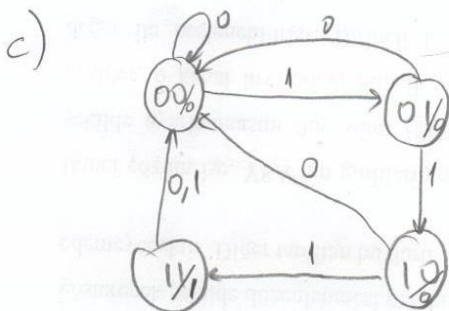


a)  $T_A = Ax' + Bx$ ,  $T_B = B + x$

A	B	x	A*	B*	y	T <sub>A</sub>	T <sub>B</sub>
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	1
0	1	1	1	0	0	1	1
1	0	0	0	0	0	1	0
1	0	1	1	1	0	0	1
1	1	0	0	0	1	1	1
1	1	1	0	0	1	1	1

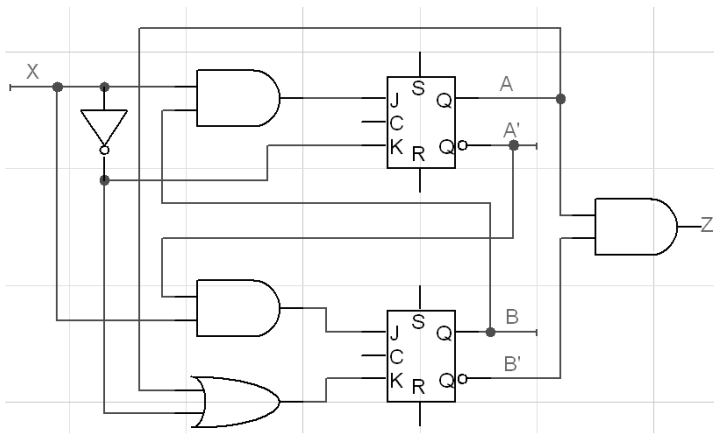
b)  $A^* = A'Bx + AB'x$   
 $= x(A \oplus B)$

$B^* = B'x$   
 $y = AB$



**Q2.** For the sequential circuit below:

- Find flip-flop input equations ( $J_A$ ,  $K_A$ ,  $J_B$ ,  $K_B$ ) and fill the state table.
- Write state equations and output equation.
- Draw its state diagram.



A4

a)

$$J_A = X \cdot B$$

$$K_A = X'$$

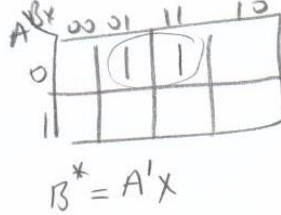
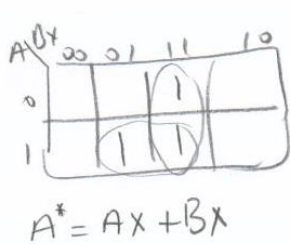
$$J_B = A' \cdot X$$

$$K_B = A + X'$$

$$Z = A \cdot B'$$

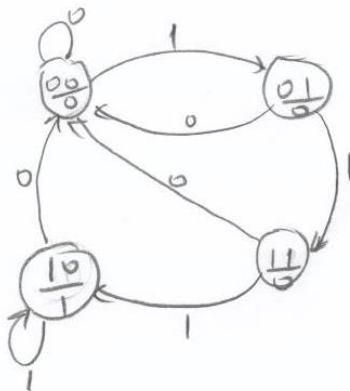
A	B	X	A*	B*	Z	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	0	0	0	0	1	0	1
0	0	1	0	1	0	0	0	1	0
0	1	0	0	0	0	0	1	0	1
0	1	1	1	1	0	1	0	1	0
1	0	0	0	0	1	0	1	0	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	0	0	1	0	1
1	1	1	1	0	0	1	0	0	1

b)

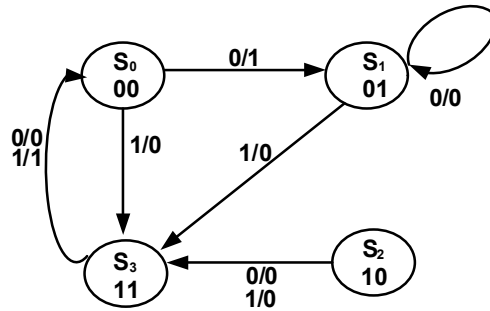


$Z = AB'$

c)



**Q3.** A Mealy type state diagram is given in the figure below. Using JK type flip-flops and gates, design and draw the circuit for this sequential system. (In the diagram  $X$ (input) /  $Y$ (output))



$Q_A Q_B X$	$Q_A+$	$Q_B+$	$J_A$	$K_A$	$J_B$	$K_B$	$Z$
000	0	1	0	x	1	x	1
001	1	1	1	x	1	x	0
010	0	1	0	x	x	0	0
011	1	1	1	x	x	0	0
100	1	1	x	0	1	x	0
101	1	1	x	0	1	x	0
110	0	0	x	1	x	1	0
111	0	0	x	1	x	1	1

$Q_A Q_B$	00	01	11	10
$X$				
0			X	X
1	1	1	X	X

$J_A = X$

$Q_A Q_B$	00	01	11	10
$X$				
0	X	X	1	
1	X	X	1	

$K_A = Q_B$

$Q_A Q_B$	00	01	11	10
$X$				
0	1	X	X	1
1	1	X	X	1

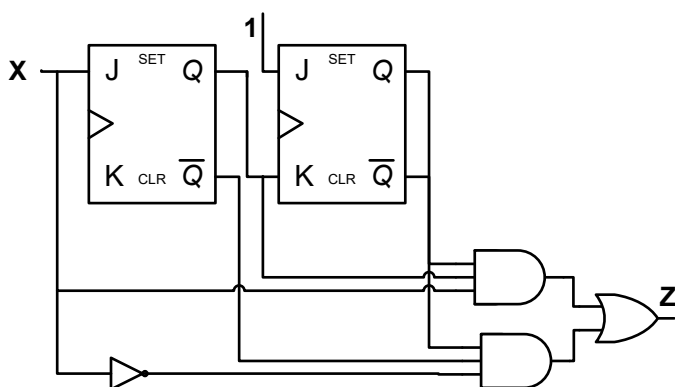
$J_B = 1$

$Q_A Q_B$	00	01	11	10
$X$				
0	X		1	X
1	X		1	X

$K_B = Q_A$

$Q_A Q_B$	00	01	11	10
$X$				
0	1			
1			1	

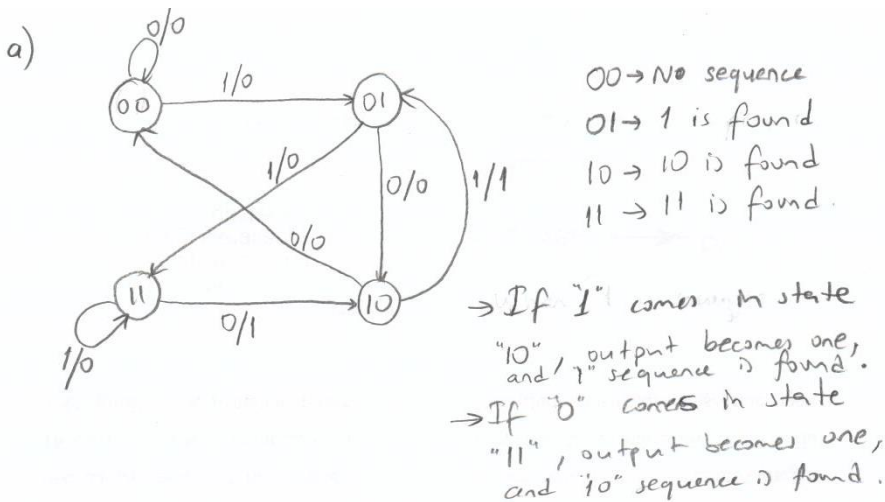
$Z = Q_A' Q_B' X' + Q_A Q_B X$



**Q4.** Design a Mealy type state machine with input X and output Y. Y should be 1 whenever the sequence **110 or 101** has been detected on X on the last 3 consecutive rising clock edges (or ticks). Otherwise, Y=0. Use at most two D flip-flops. An example input–output combination is given below:

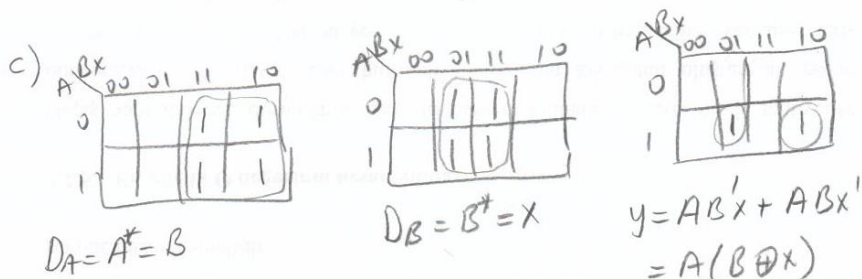
X	0	0	1	1	0	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1
Y	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0

You should show: a) State diagram. b) State table. c) Flip flop input equations and output equation.



b)

A	B	X	A*	B*	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	0



Q5. A PN flip-flop has four functions given below:

PN	Functions
00	Reset to 0
01	No change
10	Complement
11	Set to 1

- Derive the characteristic equation for PN flip-flop. Show your work.
- Draw the Mealy type state diagram of a sequence detector that detects the sequence 1101. You must have at most four states. When the sequence 1101 is detected, the output Z becomes 1.
- Design the sequence detector using two PN flip-flops. (Hint: You should determine the flip-flop input equations,  $P_A$ ,  $N_A$ ,  $P_B$ ,  $N_B$ , and the output equation.)

(A3)

a)

P	N	Q	Q*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$Q^* = PQ' + NQ$

b)

$S_0 \rightarrow 00$   
 $S_1 \rightarrow 01$   
 $S_2 \rightarrow 10$   
 $S_3 \rightarrow 11$

c)

A	B	X	A*	B*	Z	$P_A$	$N_A$	$P_B$	$N_B$
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	0	0	0	X	X	0
0	1	1	1	0	0	1	X	X	0
1	0	0	1	1	0	X	1	1	X
1	0	1	1	0	0	X	1	0	X
1	1	0	0	0	0	X	0	X	0
1	1	1	0	1	1	X	0	X	1

Excitation table

Q	Q*	P	N
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

$P_A = Bx$   
 $N_A = B'$   
 $P_B = A'x + Ax' = A \oplus x$   
 $N_B = Ax$   
 $Z = ABx$