Verilog

Coding in Xilinx ISE Design Suite v14.6

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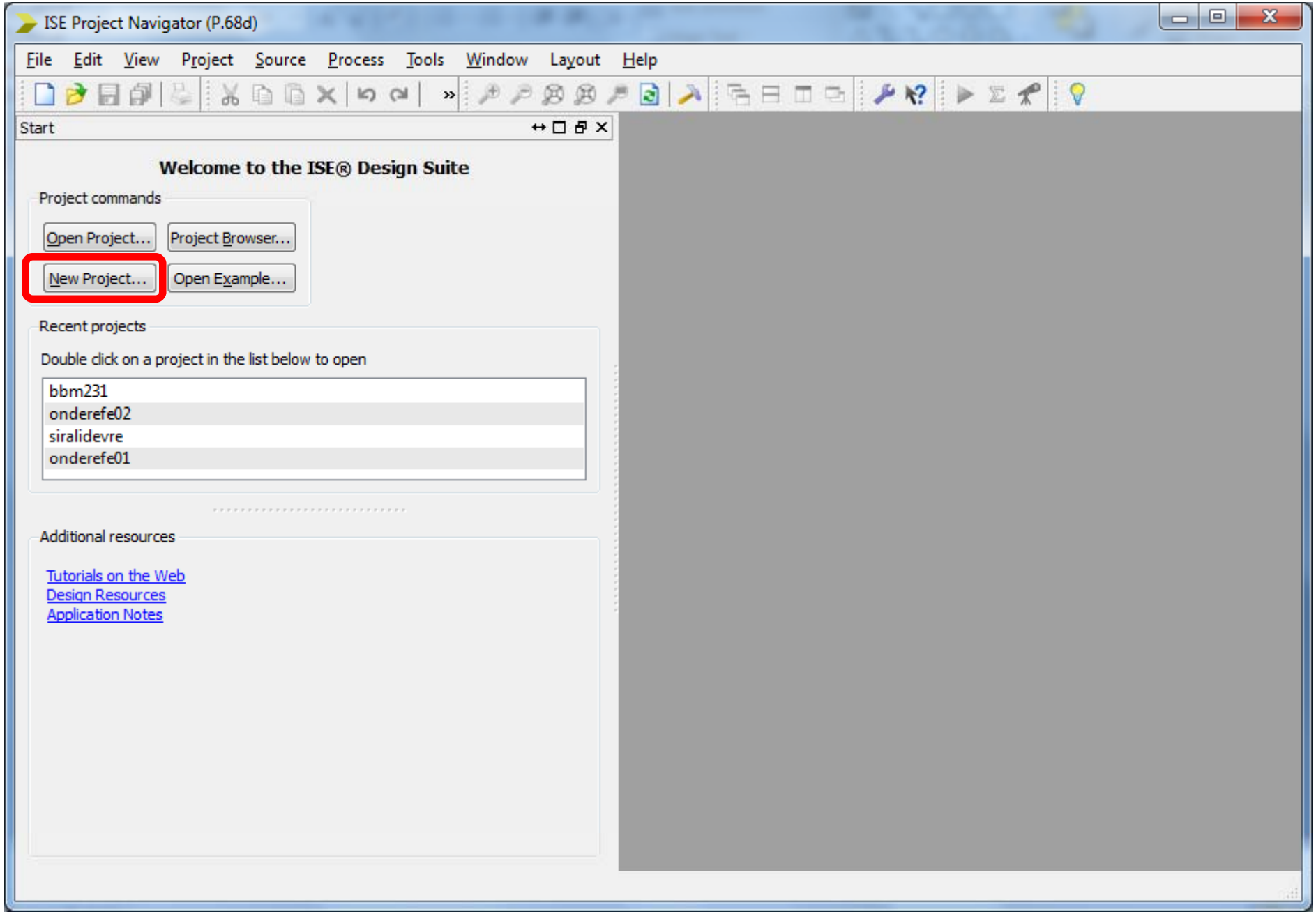
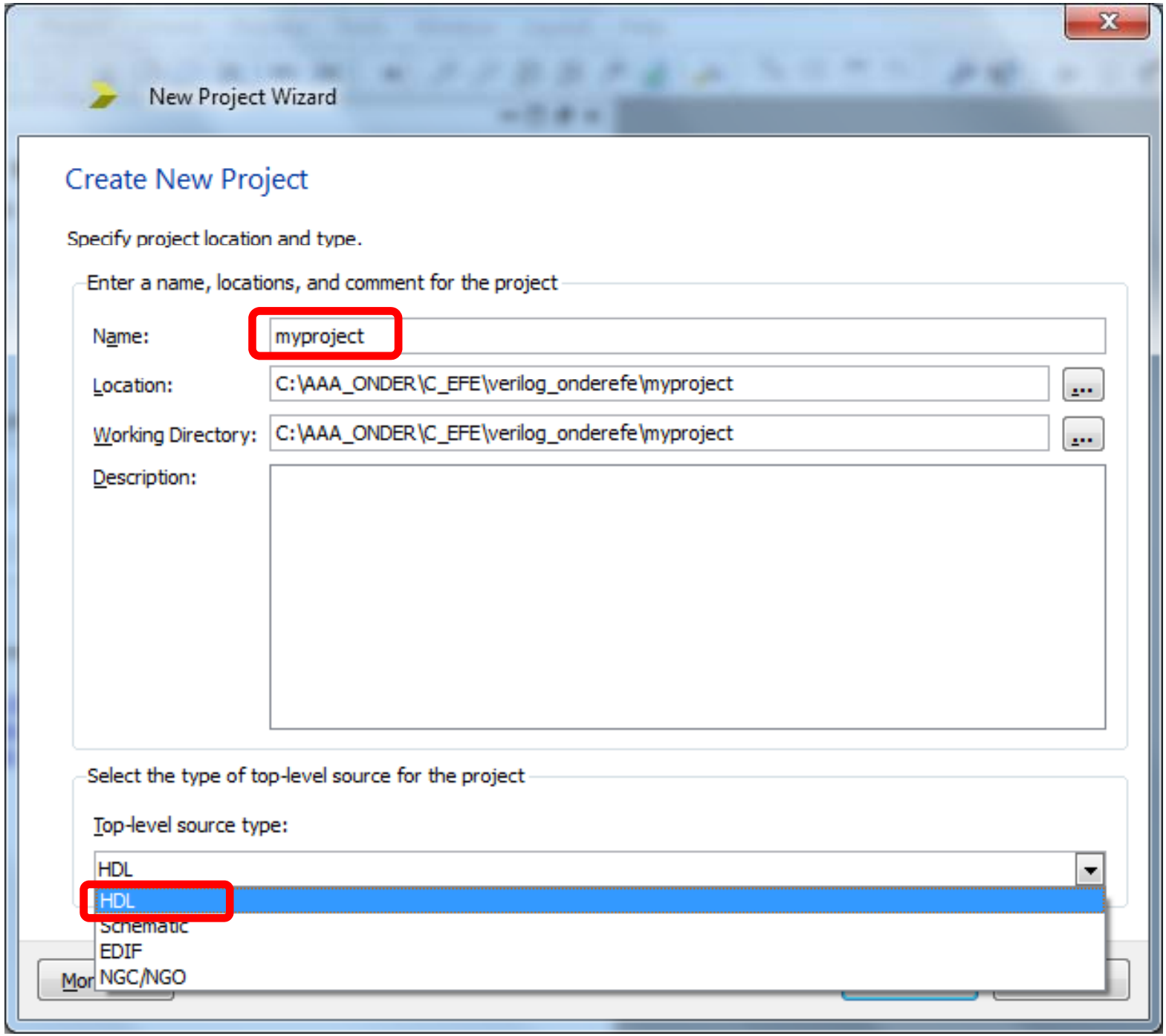
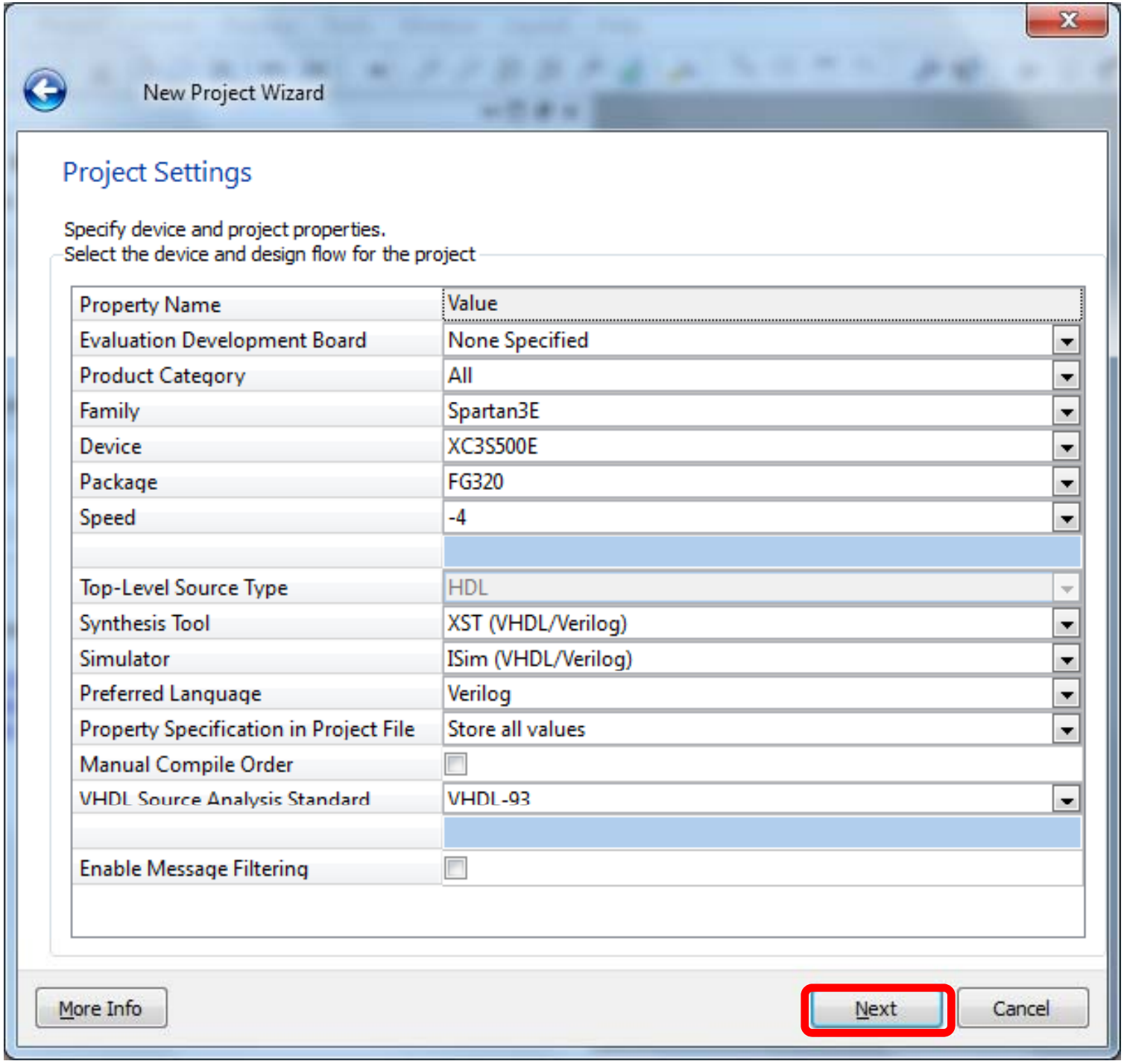
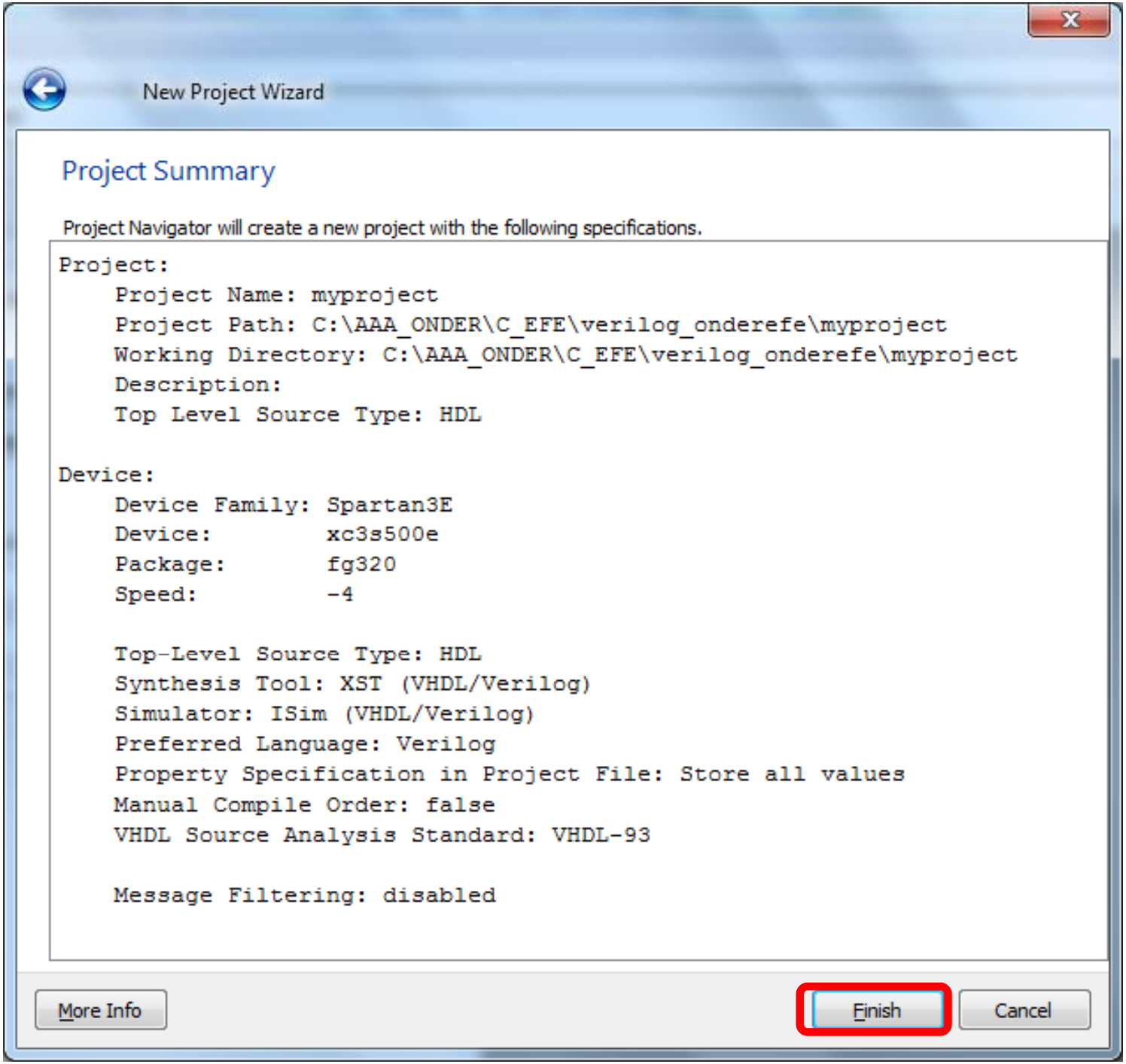
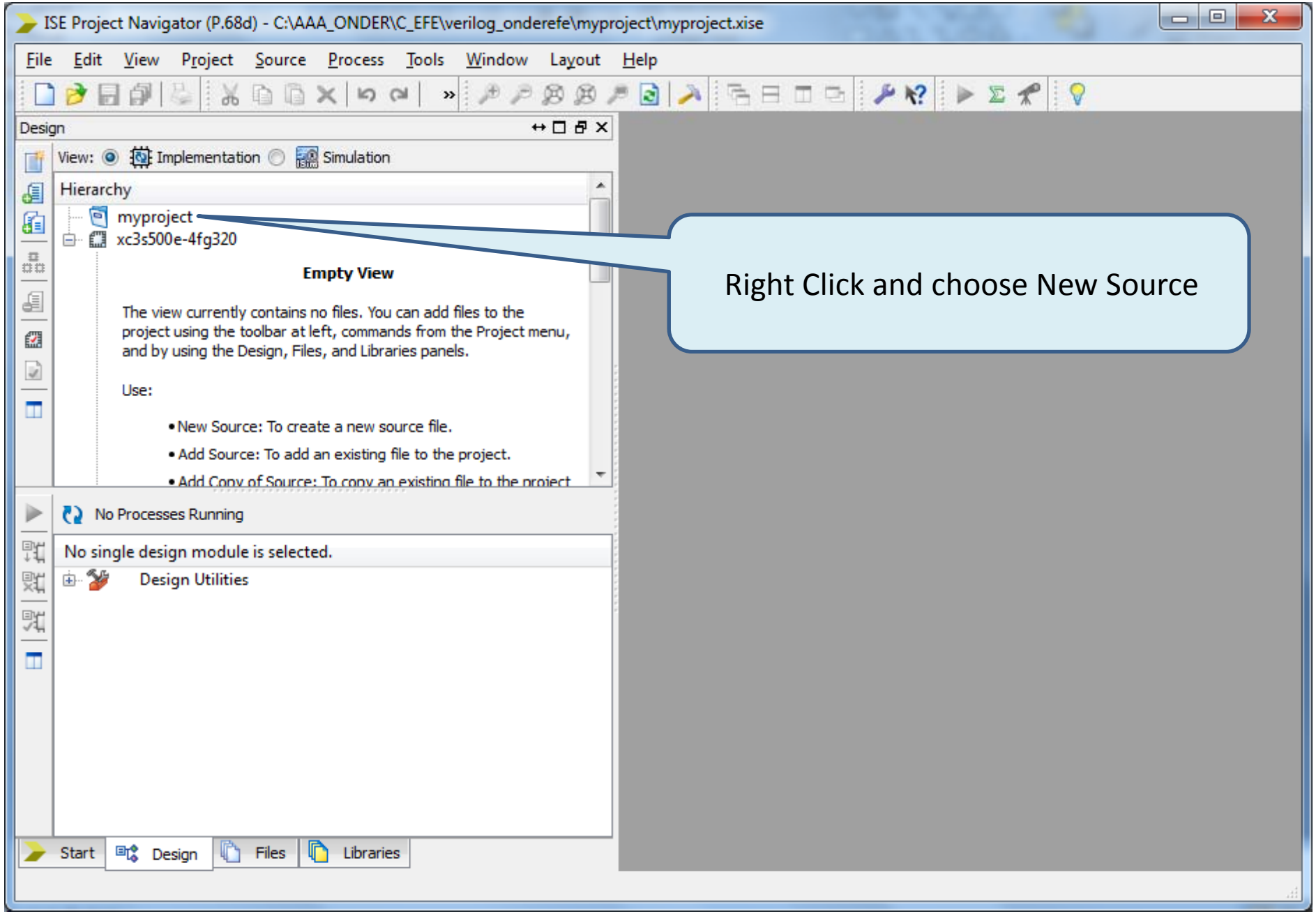
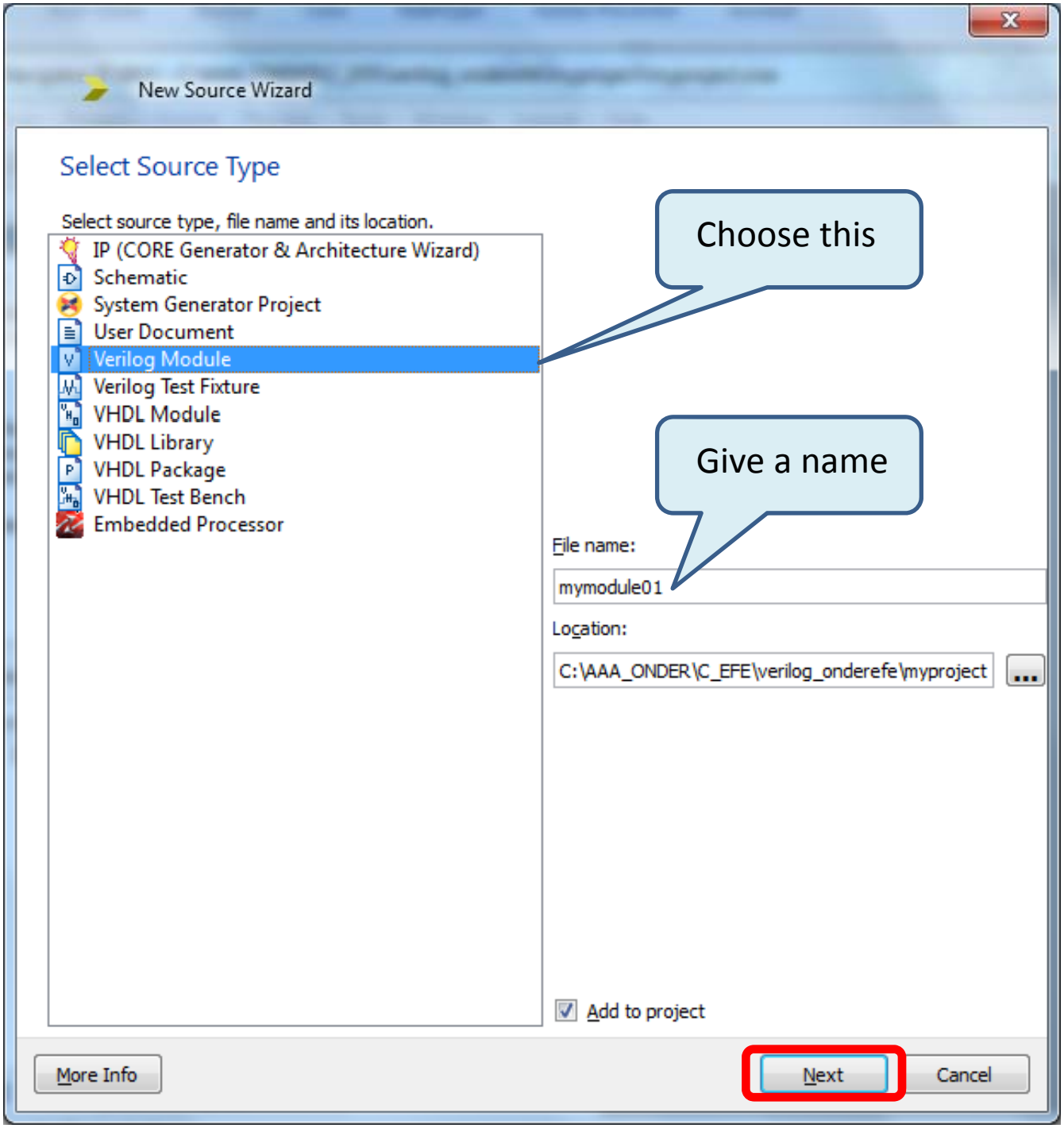

ISE Project Navigator (P.68d)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
bbm231
onderefe02
siralidevre
onderefe01
Additional resources
Tutorials on the Web
Design Resources
Application Notes

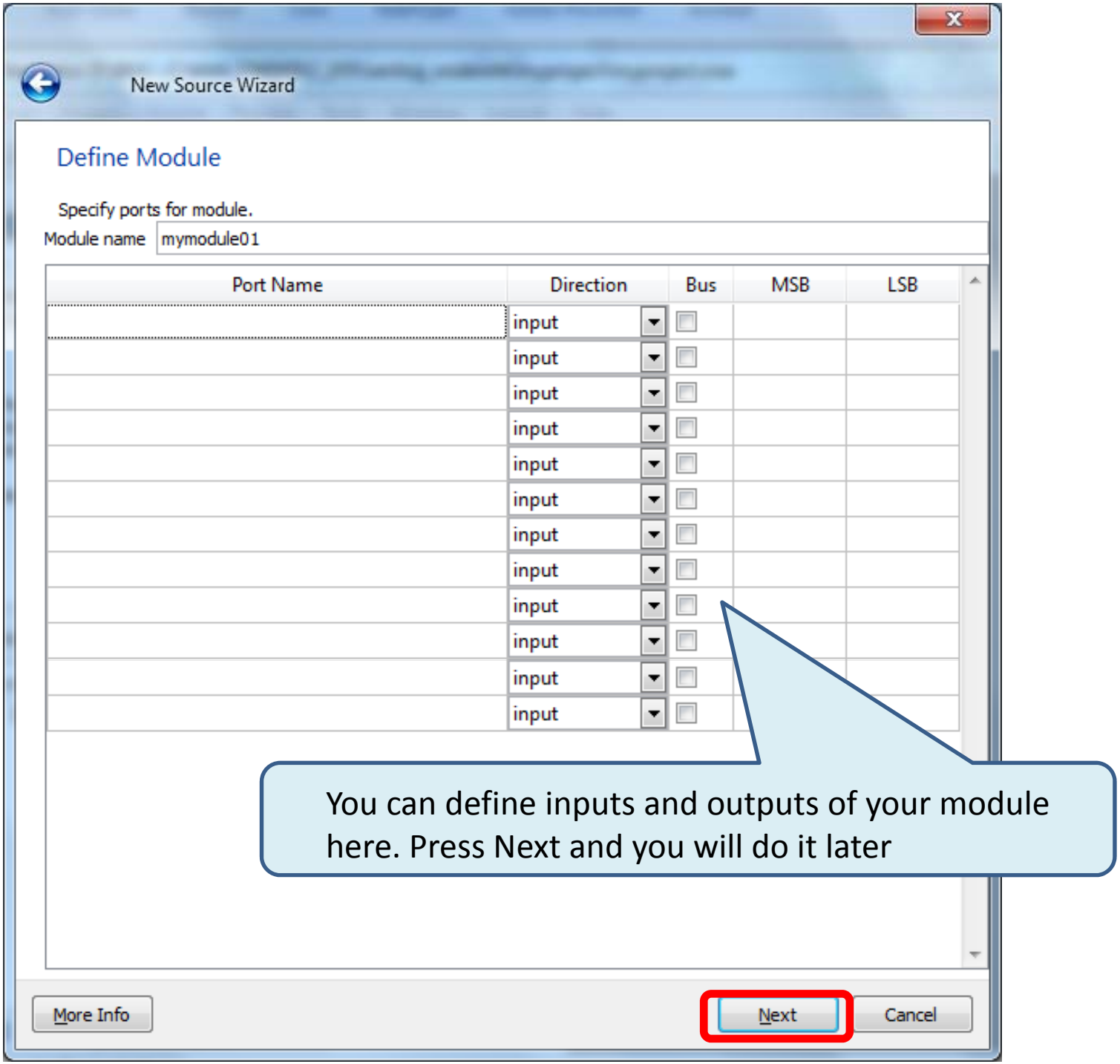

New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name:
myproject
Location:
C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Working Directory:
C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
HDL
Schematic
EDIF
NGC/NGO

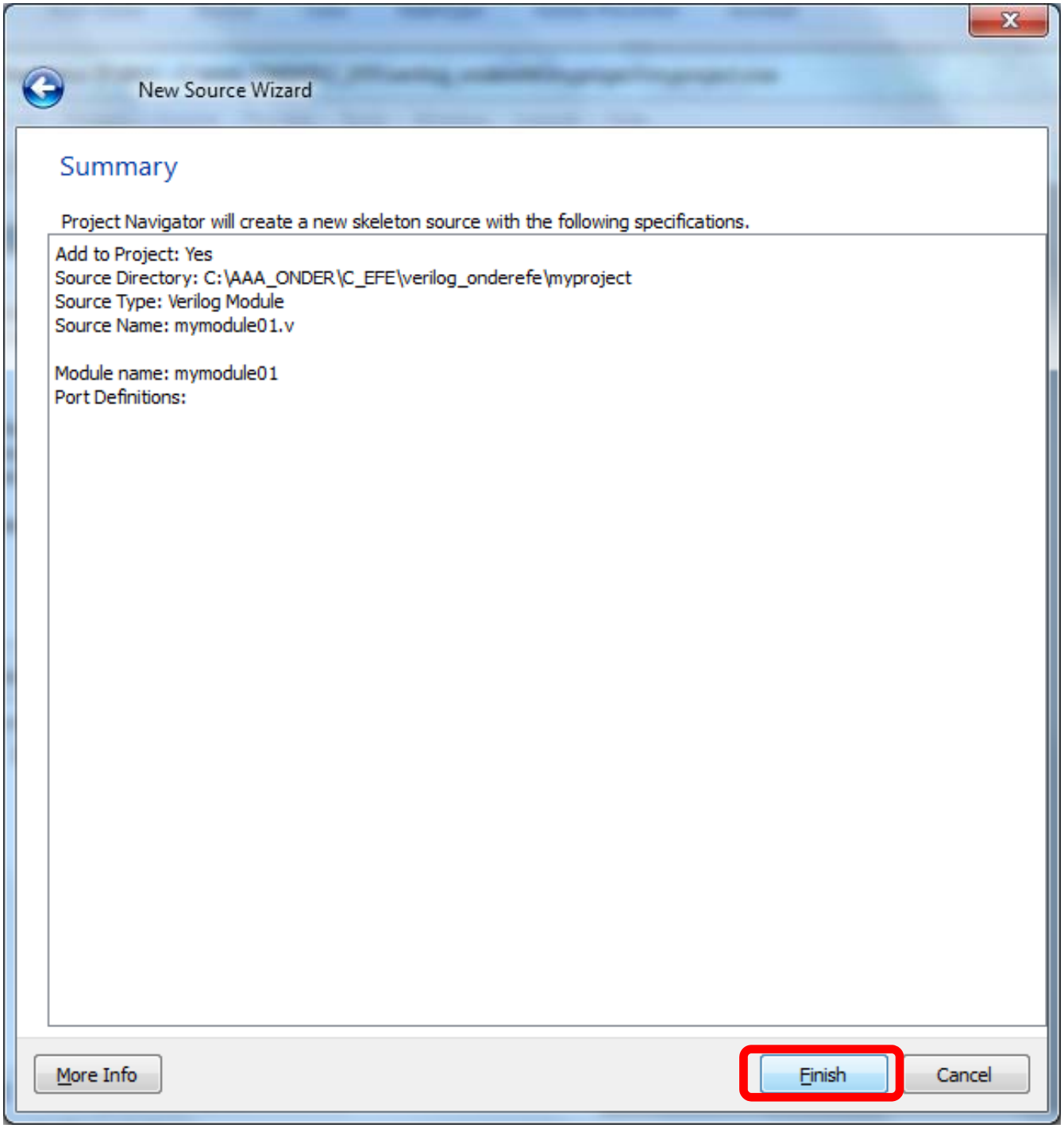

New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan3E
Device
XC3S500E
Package
FG320
Speed
-4
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
Next
Cancel

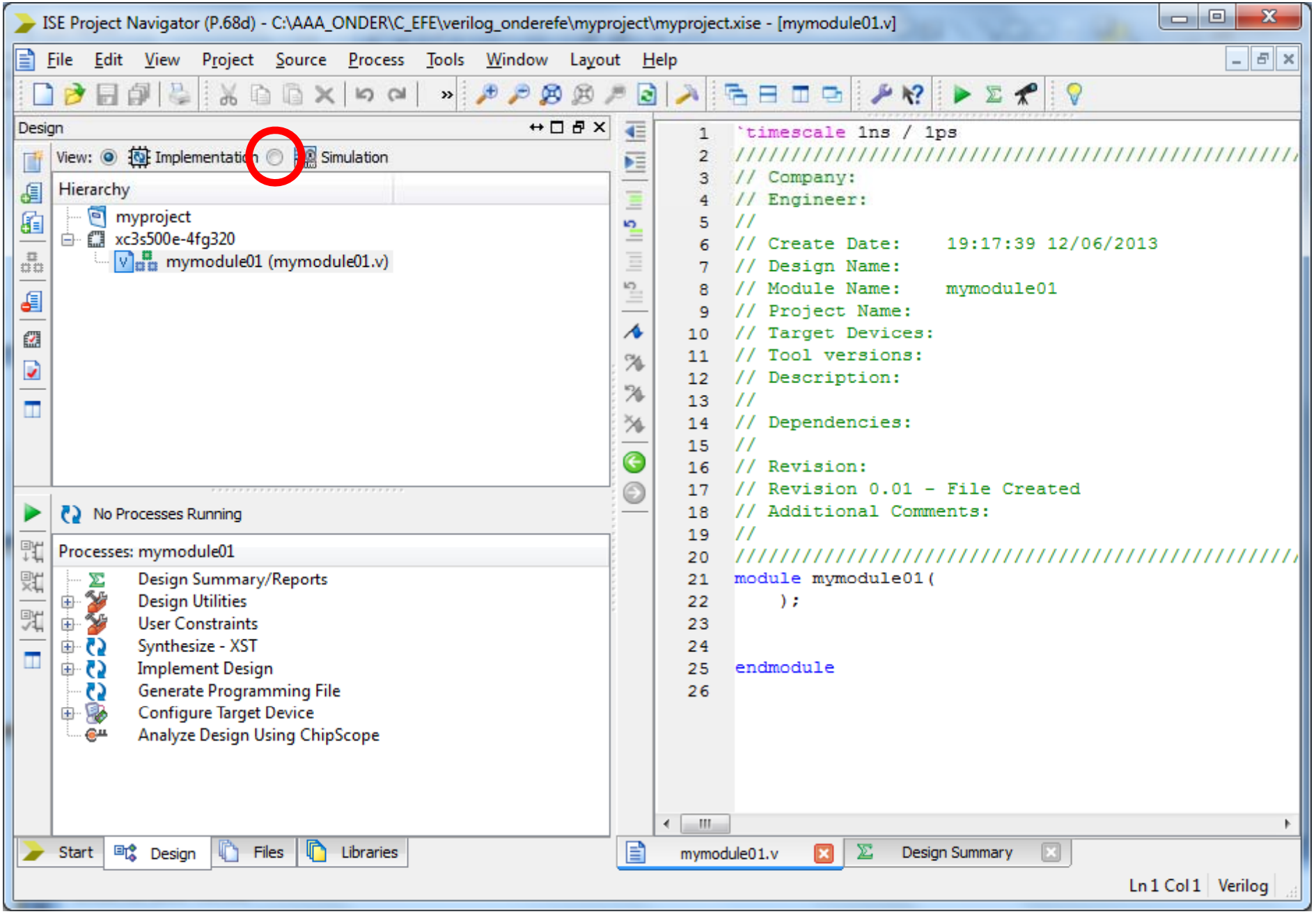

New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: myproject
Project Path: C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Working Directory: C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan3E
Device: xc3s500e
Package: fg320
Speed: -4
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
Finish
Cancel

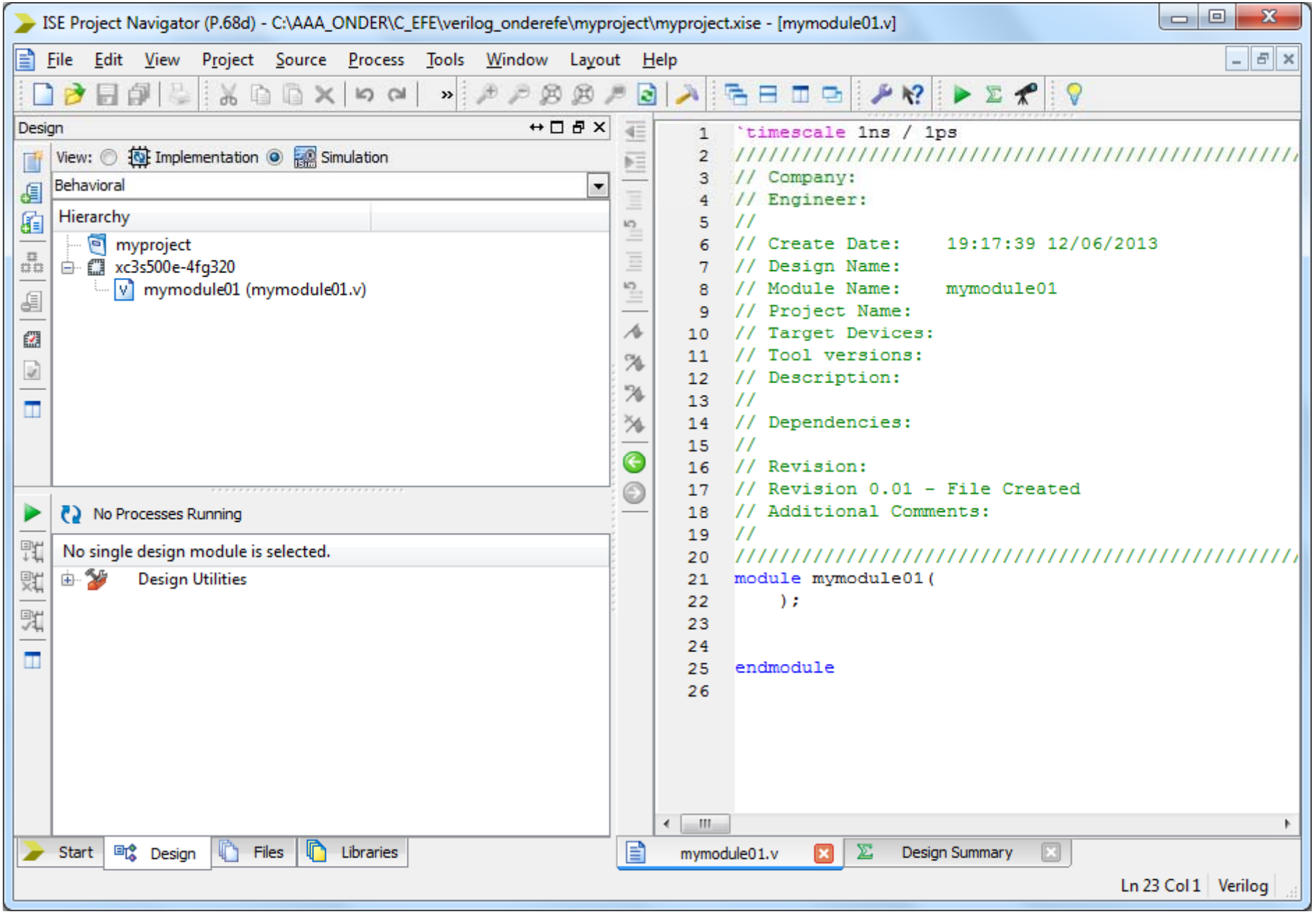

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
myproject
xc3s500e-4fg320
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
Right Click and choose New Source


New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
System Generator Project
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
Choose this
Give a name
File name:
mymodule01
Location:
C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
...
Add to project
More Info
Next
Cancel


New Source Wizard
Define Module
Specify ports for module.
Module name
mymodule01
Port Name
Direction
Bus
MSB
LSB
input
You can define inputs and outputs of your module here. Press Next and you will do it later
More Info
Next
Cancel

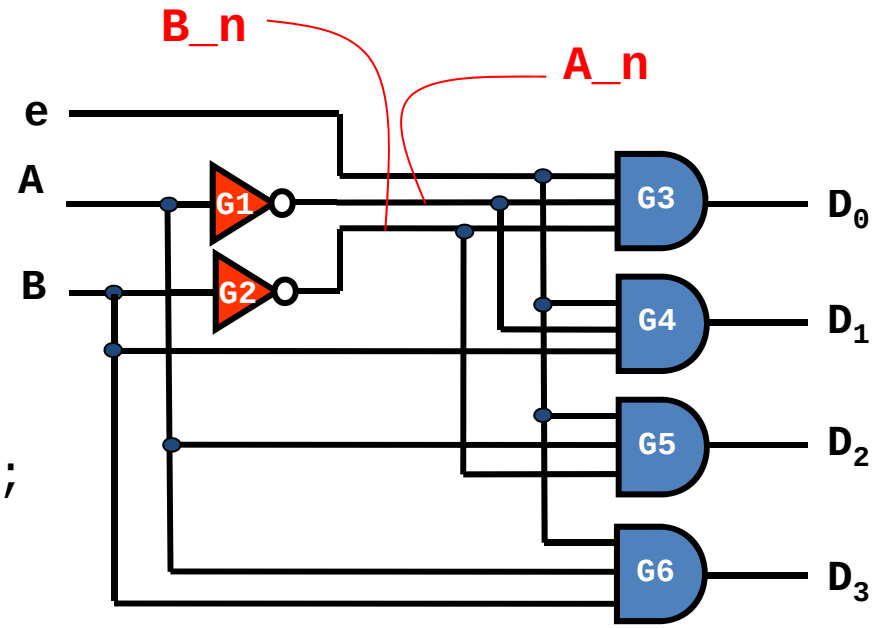

New Source Wizard
Summary
Project Navigator will create a new skeleton source with the following specifications.
Add to Project: Yes
Source Directory: C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Source Type: Verilog Module
Source Name: mymodule01.v
Module name: mymodule01
Port Definitions:
More Info
Finish
Cancel

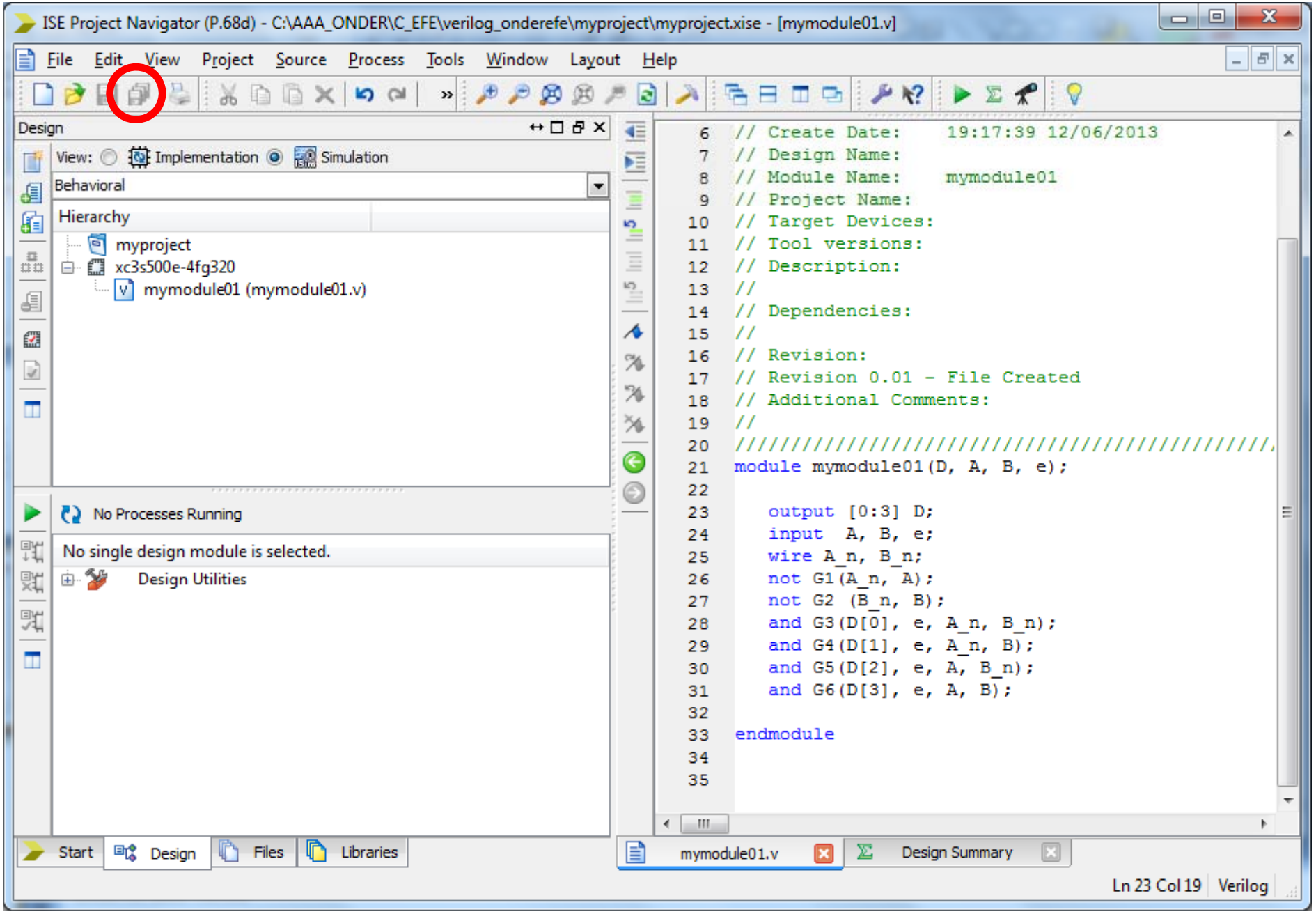

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
myproject
xc3s500e-4fg320
mymodule01 (mymodule01.v)
No Processes Running
Processes: mymodule01
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 19:17:39 12/06/2013
7 // Design Name:
8 // Module Name: mymodule01
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mymodule01(
22);
23
24
25 endmodule
26
mymodule01.v
Design Summary
Ln 1 Col 1
Verilog


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01 (mymodule01.v)
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 19:17:39 12/06/2013
7 // Design Name:
8 // Module Name: mymodule01
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mymodule01(
22);
23
24
25 endmodule
26
mymodule01.v
Design Summary
Ln 23 Col 1 Verilog

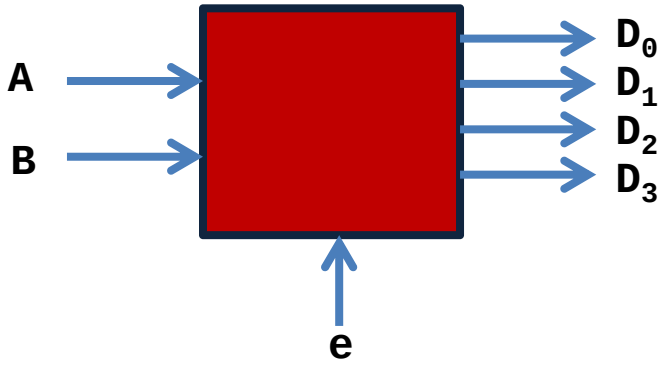
mymodule01 : 2 to 4 decoder

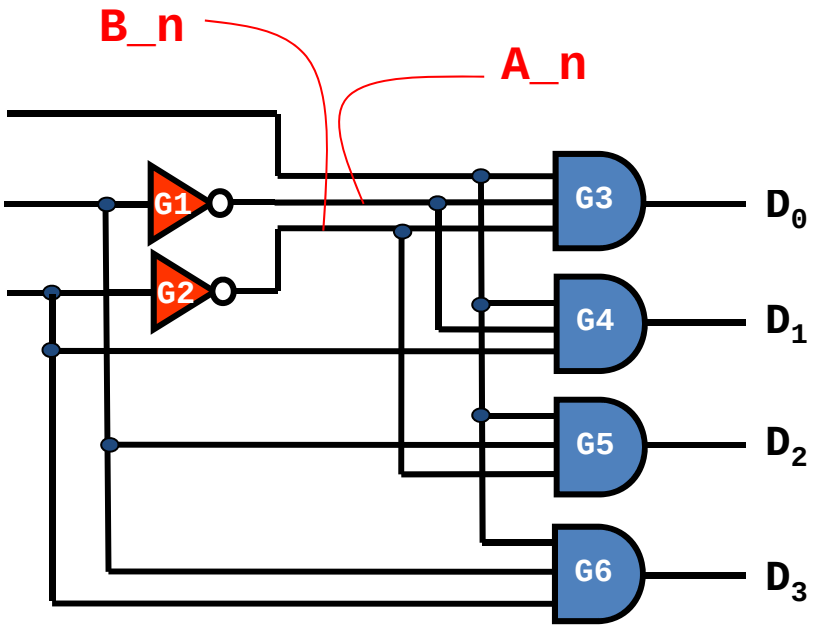
```
module mymodule01(D, A, B, e);

        output [0:3] D;
        input  A, B, e;
        wire A_n, B_n;
        not G1(A_n, A);
        not G2 (B_n, B);
        and G3(D[0], e, A_n, B_n);
        and G4(D[1], e, A_n, B);
        and G5(D[2], e, A, B_n);
        and G6(D[3], e, A, B);

endmodule
```




ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01 (mymodule01.v)
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
mymodule01.v
Design Summary
Ln 23 Col 19 Verilog
6 // Create Date: 19:17:39 12/06/2013
7 // Design Name:
8 // Module Name: mymodule01
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mymodule01(D, A, B, e);
22
23 output [0:3] D;
24 input A, B, e;
25 wire A_n, B_n;
26 not G1(A_n, A);
27 not G2 (B_n, B);
28 and G3(D[0], e, A_n, B_n);
29 and G4(D[1], e, A_n, B);
30 and G5(D[2], e, A, B_n);
31 and G6(D[3], e, A, B);
32
33 endmodule
34
35

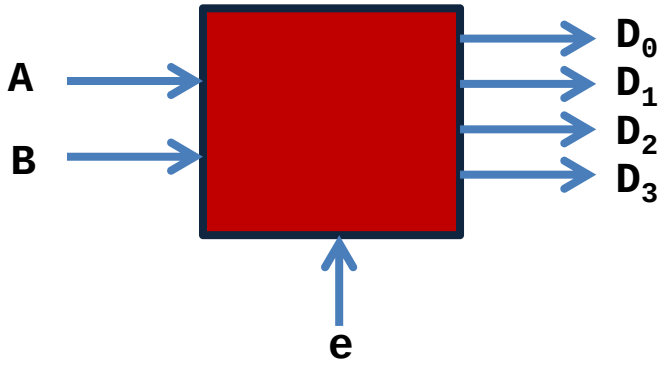
Our decoder code is ready. Save it.



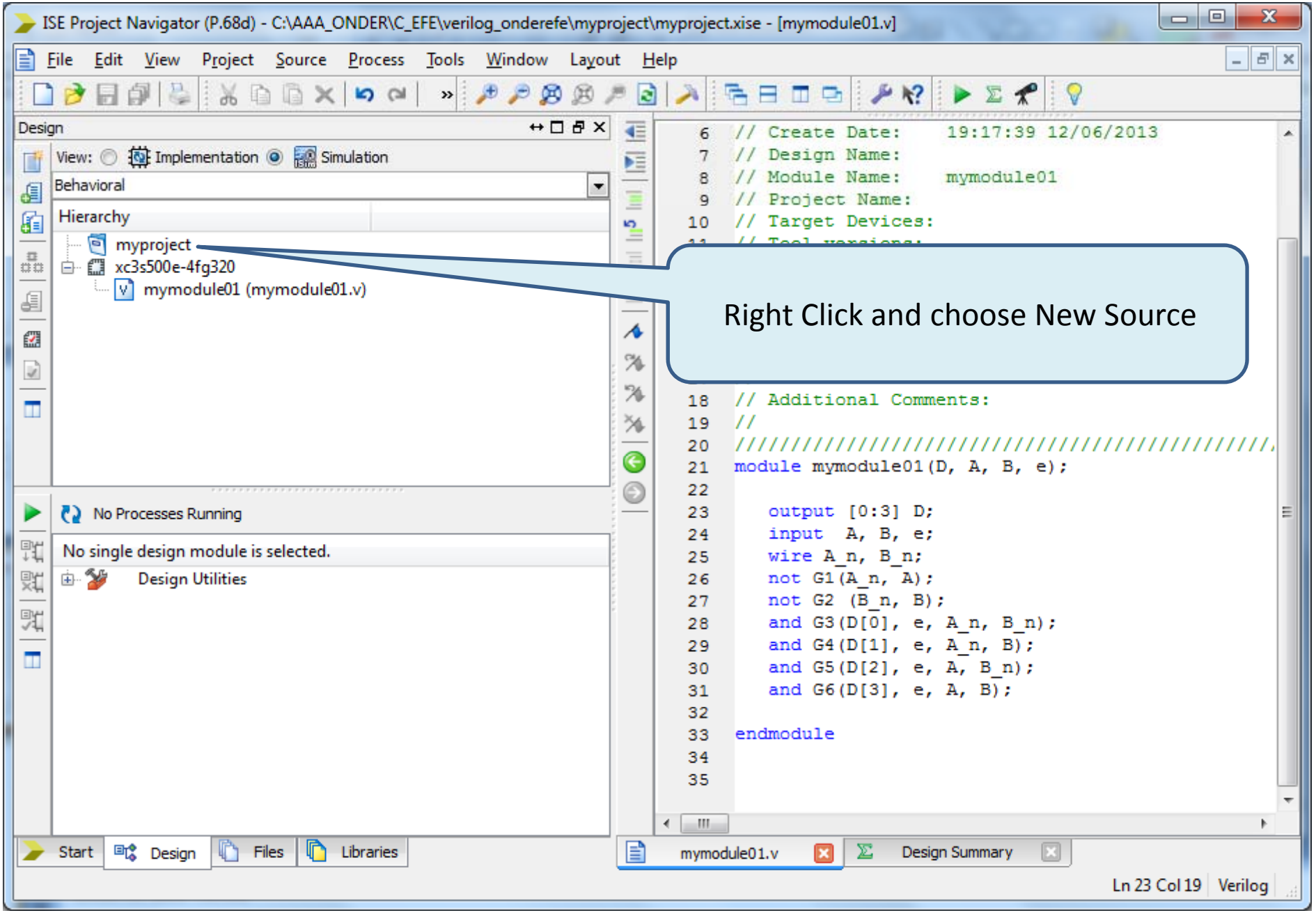


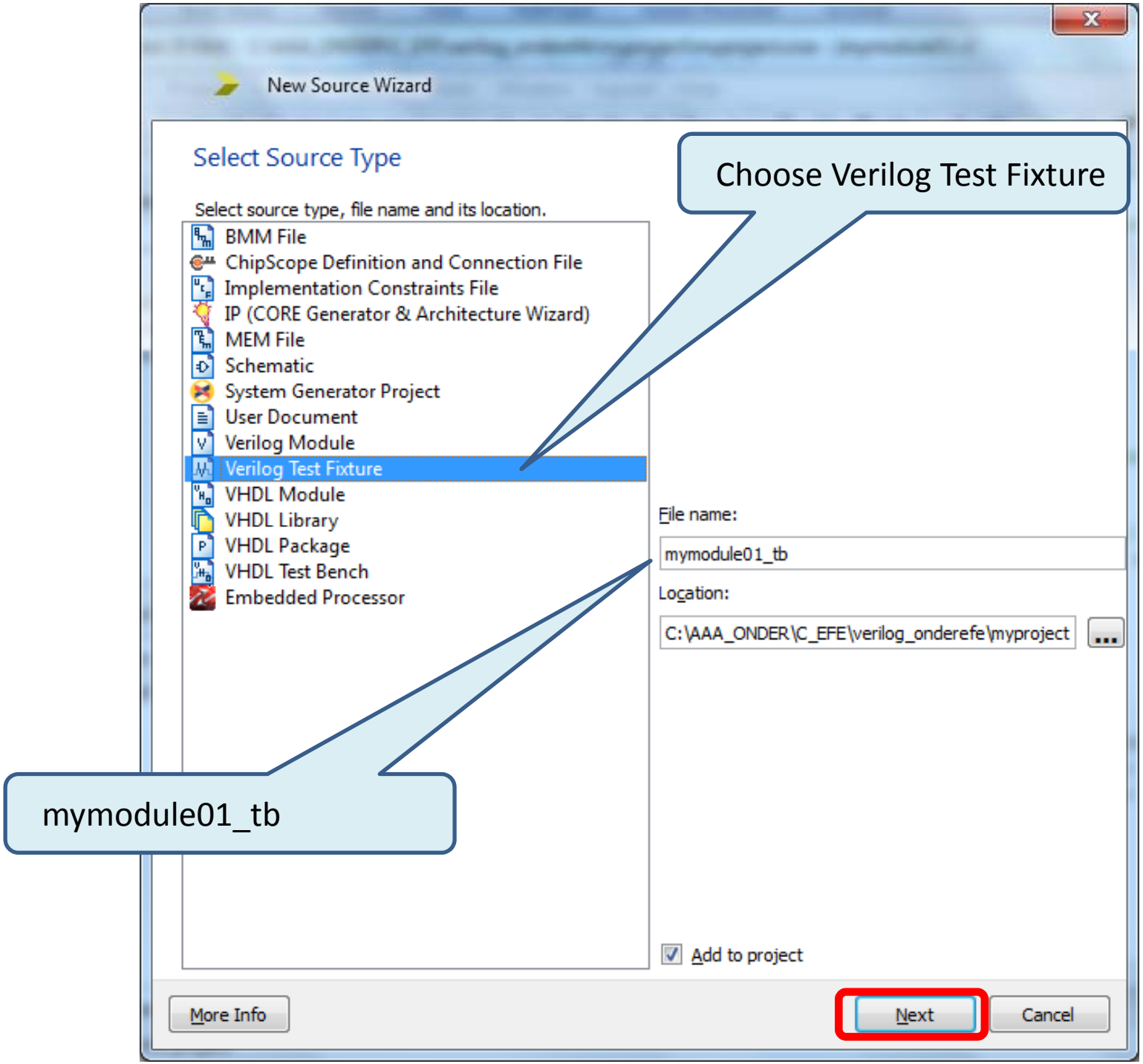
$D_0 = eA'B'$
$D_1 = eA'B$
$D_2 = eAB'$
$D_3 = eAB$

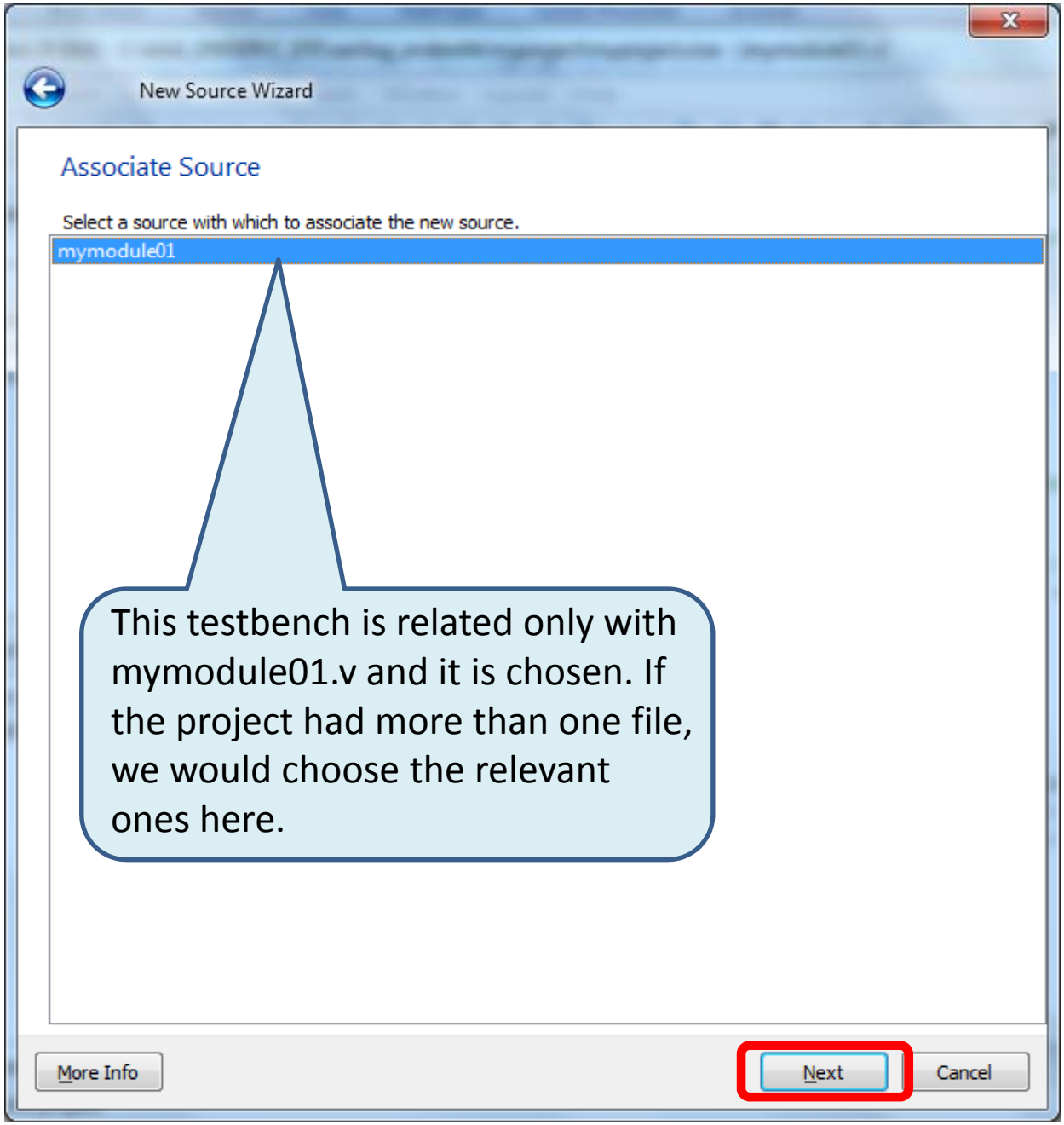
Now we will write a testbench
Apply A, B, e, obtain D_0, D_1, D_2, D_3

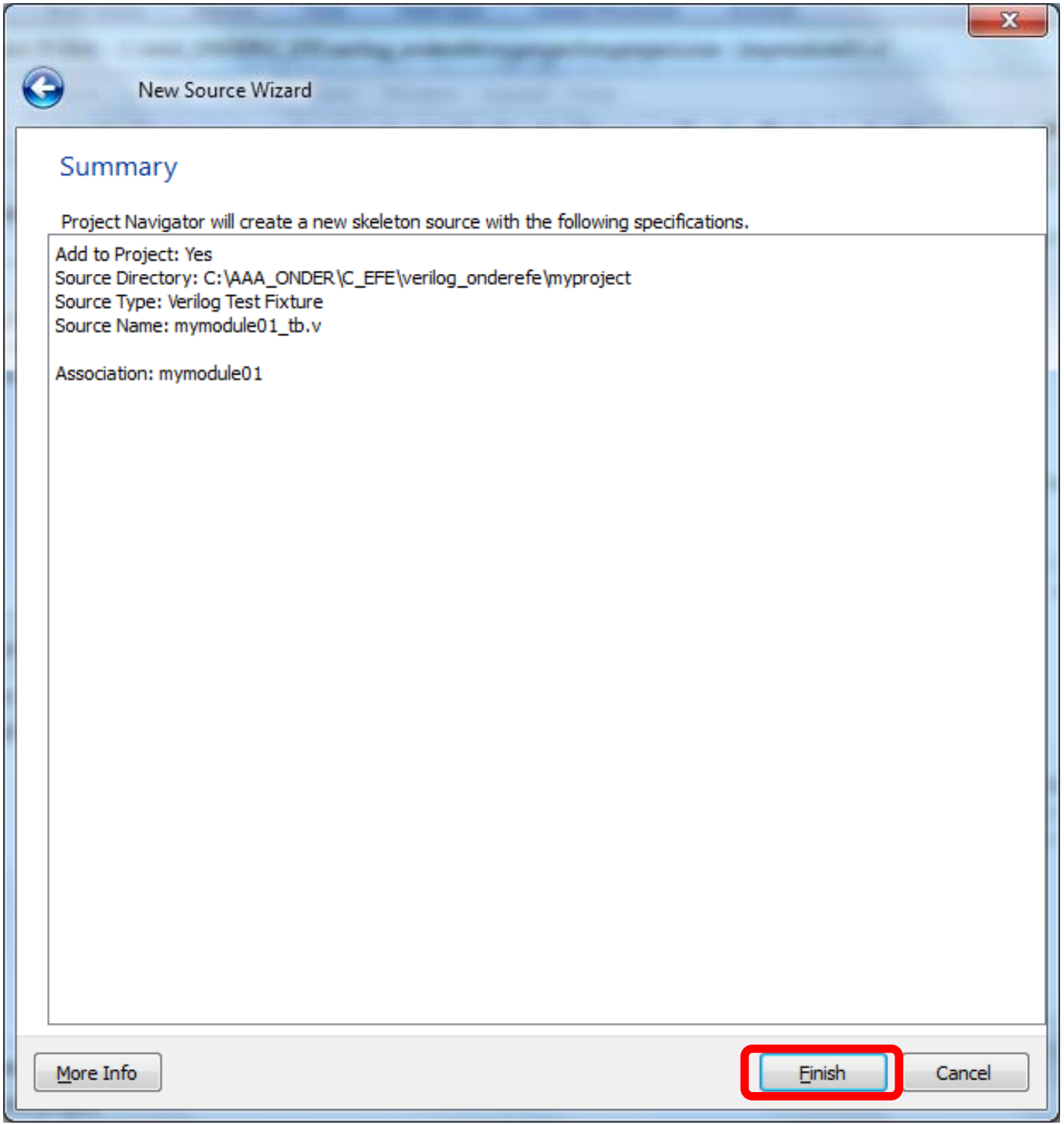


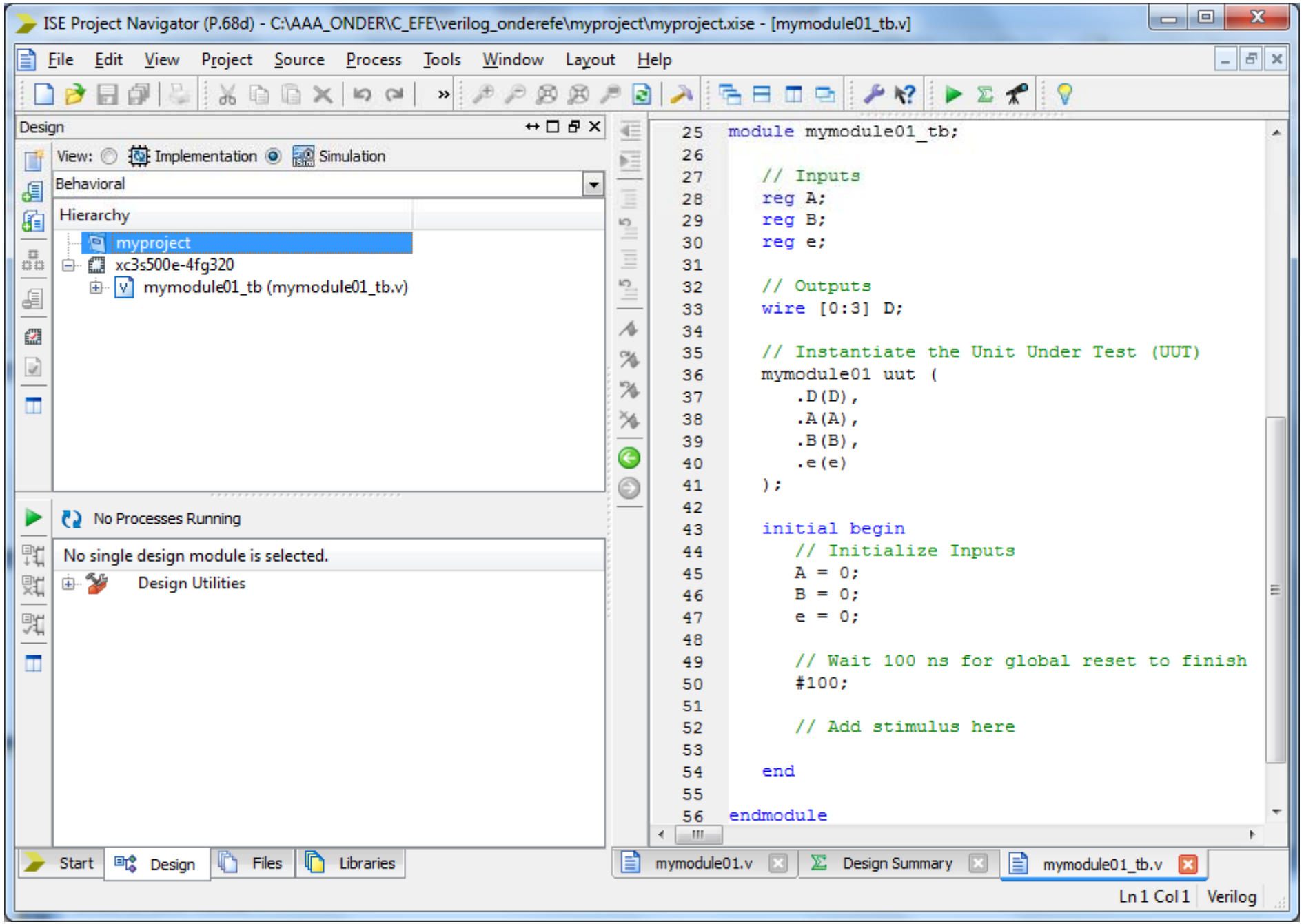
$D_0 = eA'B'$
$D_1 = eA'B$
$D_2 = eAB'$
$D_3 = eAB$


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01 (mymodule01.v)
Right Click and choose New Source
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
mymodule01.v
Design Summary
Ln 23 Col 19 Verilog
6 // Create Date: 19:17:39 12/06/2013
7 // Design Name:
8 // Module Name: mymodule01
9 // Project Name:
10 // Target Devices:
18 // Additional Comments:
19 //
20 //
21 module mymodule01(D, A, B, e);
22
23 output [0:3] D;
24 input A, B, e;
25 wire A_n, B_n;
26 not G1(A_n, A);
27 not G2 (B_n, B);
28 and G3(D[0], e, A_n, B_n);
29 and G4(D[1], e, A_n, B);
30 and G5(D[2], e, A, B_n);
31 and G6(D[3], e, A, B);
32
33 endmodule
34
35

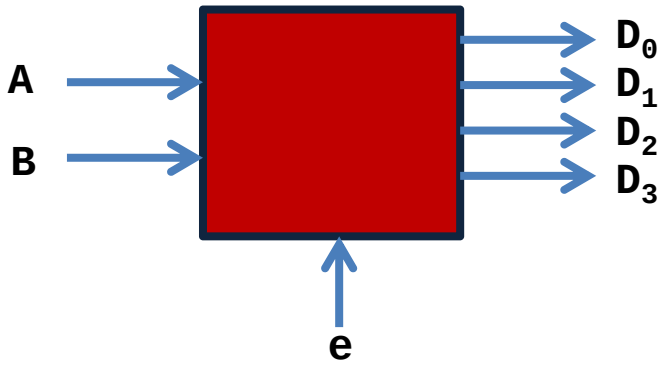

New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
System Generator Project
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
Choose Verilog Test Fixture
File name:
mymodule01_tb
Location:
C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
...
Add to project
mymodule01_tb
More Info
Next
Cancel


New Source Wizard
Associate Source
Select a source with which to associate the new source.
mymodule01
This testbench is related only with mymodule01.v and it is chosen. If the project had more than one file, we would choose the relevant ones here.
More Info
Next
Cancel

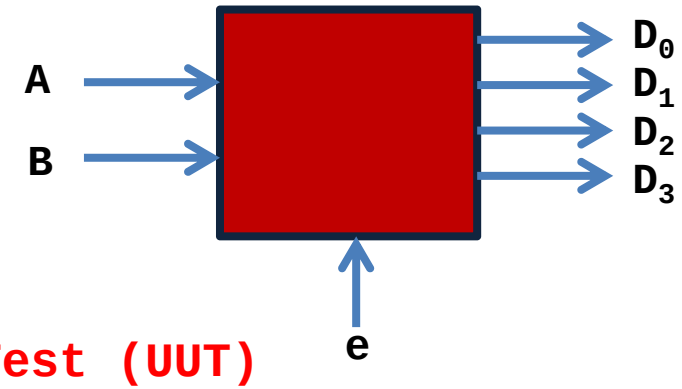

New Source Wizard
Summary
Project Navigator will create a new skeleton source with the following specifications.
Add to Project: Yes
Source Directory: C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject
Source Type: Verilog Test Fixture
Source Name: mymodule01_tb.v
Association: mymodule01
More Info
Finish
Cancel

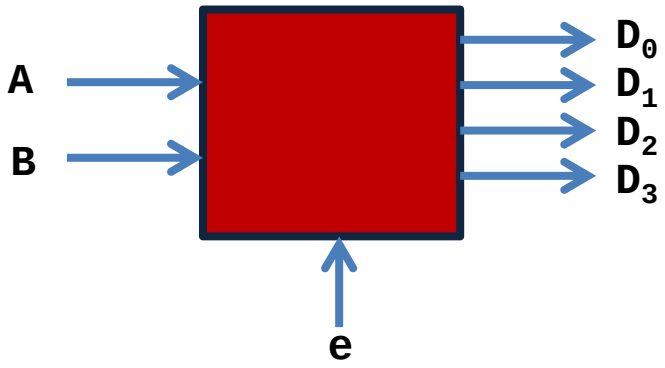

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
25 module mymodule01_tb;
26
27 // Inputs
28 reg A;
29 reg B;
30 reg e;
31
32 // Outputs
33 wire [0:3] D;
34
35 // Instantiate the Unit Under Test (UUT)
36 mymodule01 uut (
37 .D(D),
38 .A(A),
39 .B(B),
40 .e(e)
41);
42
43 initial begin
44 // Initialize Inputs
45 A = 0;
46 B = 0;
47 e = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
52 // Add stimulus here
53
54 end
55
56 endmodule
mymodule01.v
Design Summary
mymodule01_tb.v
Ln 1 Col 1
Verilog

```
module mymodule01_tb;

        // Inputs
        reg A;
        reg B;
        reg e;

        // Outputs
        wire [0:3] D;

        // Instantiate the Unit Under Test (UUT)
        mymodule01 uut (
                .D(D),
                .A(A),
                .B(B),
                .e(e)
        );

        initial begin
                // Initialize Inputs
                A = 0;
                B = 0;
                e = 0;

                // Wait 100 ns for global reset to finish
                #100;

                // Add stimulus here

        end

endmodule
```



```
module mymodule01_tb;

        // Inputs
        reg A;
        reg B;
        reg e;

        // Outputs
        wire [0:3] D;

        // Instantiate the Unit Under Test (UUT)
        mymodule01 uut (
                .D(D),
                .A(A),
                .B(B),
                .e(e)
        );

        initial begin
                // Initialize Inputs
                A = 0;
                B = 0;
                e = 0;

                // Wait 100 ns for global reset to finish
                #100;

                // Add stimulus here

        end

endmodule
```



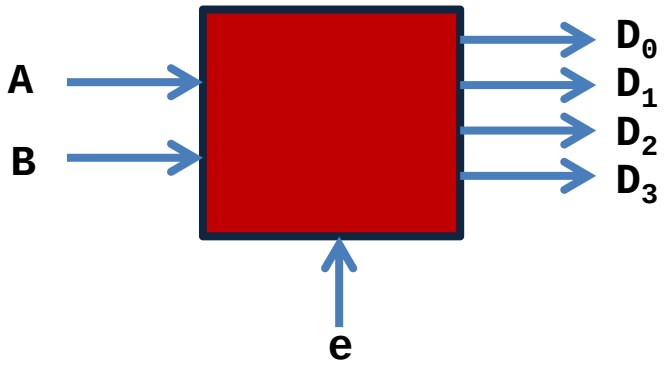


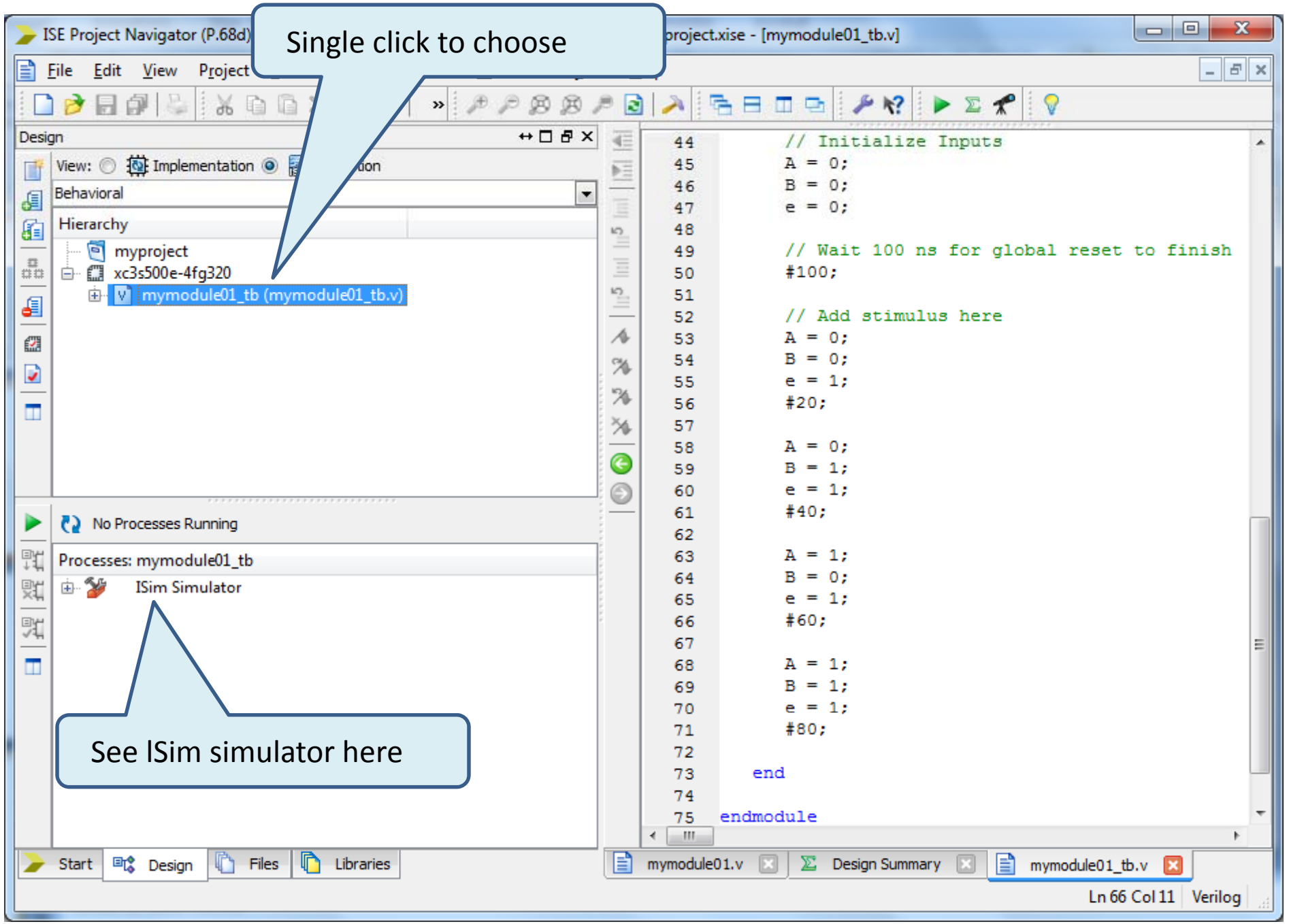
. . .

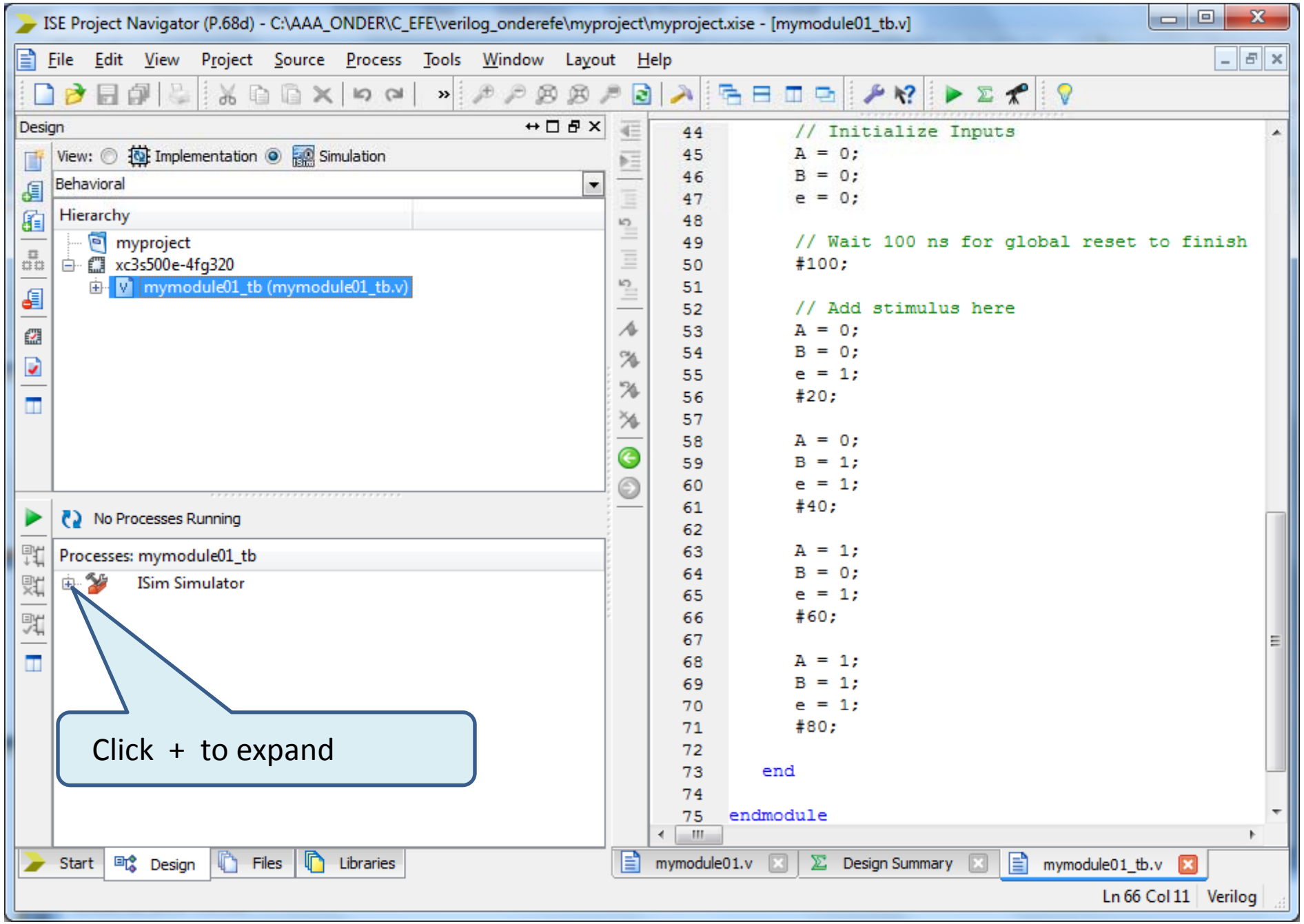
. . .

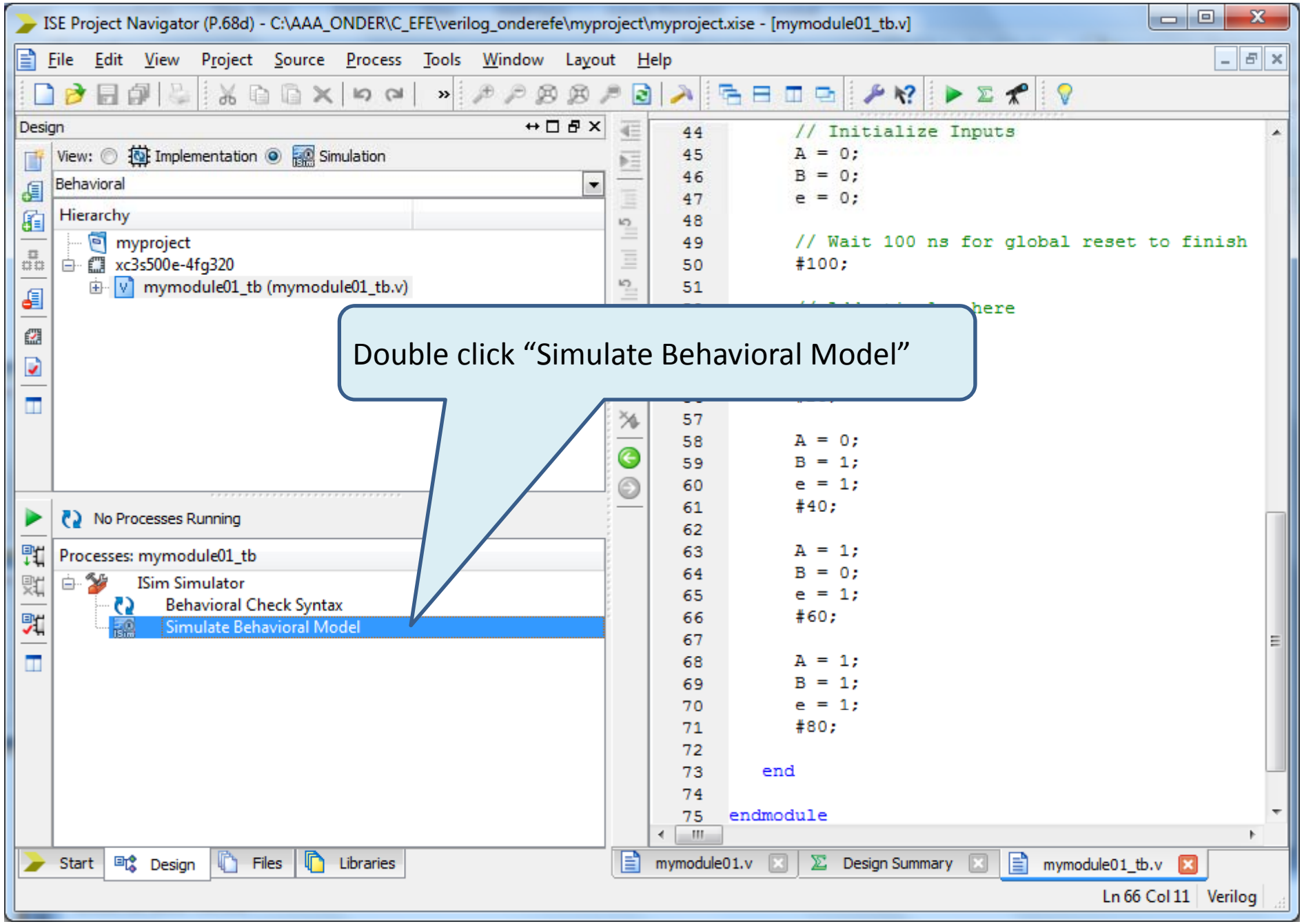
```
initial begin
        // Initialize Inputs
        A = 0;
        B = 0;
        e = 0;

        // Wait 100 ns for global reset to finish
        #100;

        // Add stimulus here
        // ENTER YOUR TESTING CONDITIONS HERE
end

endmodule
```

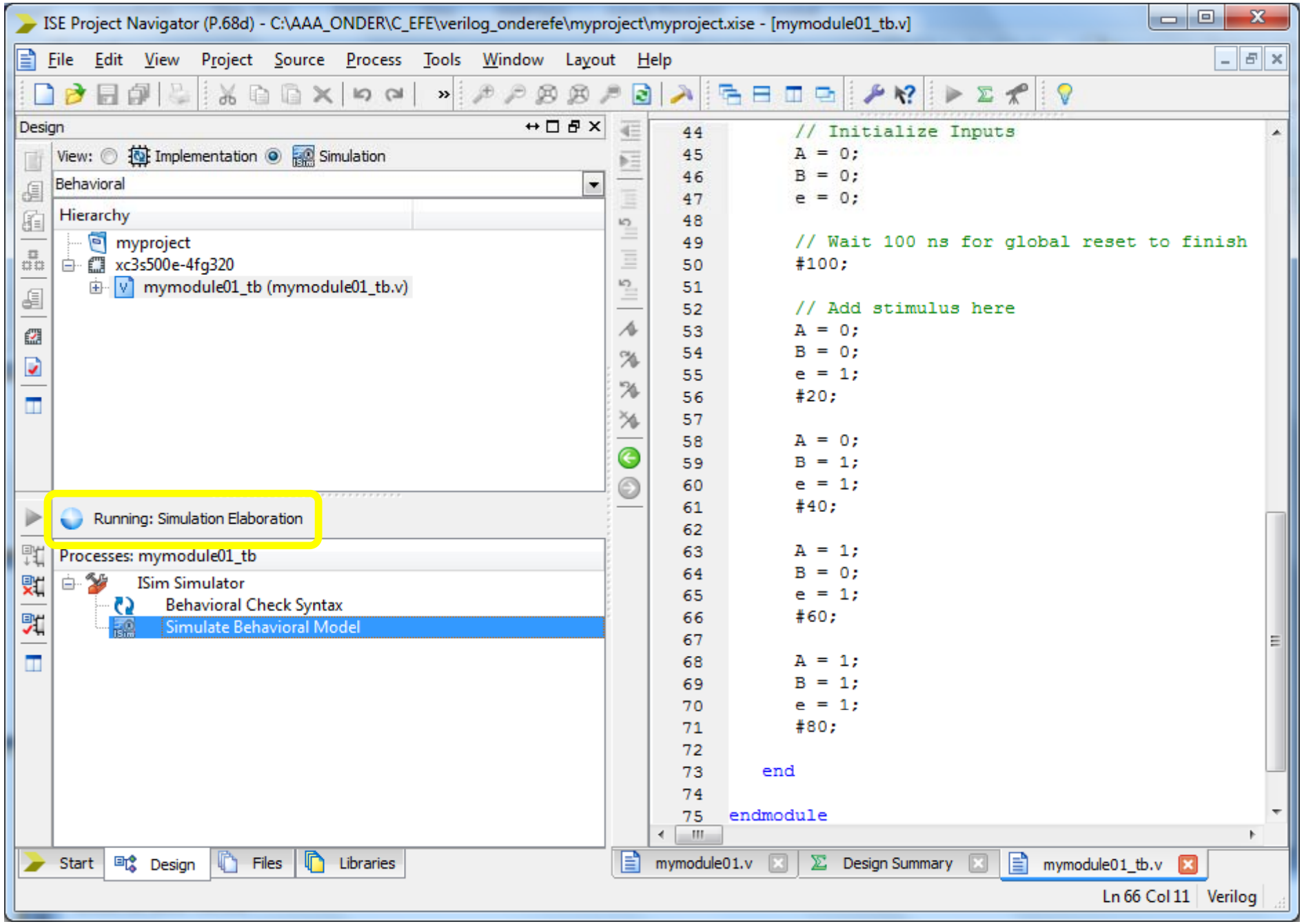
```
// Add stimulus here
A = 0;
B = 0;
e = 1;
#20;

A = 0;
B = 1;
e = 1;
#40;

A = 1;
B = 0;
e = 1;
#60;

A = 1;
B = 1;
e = 1;
#80;
```




Single click to choose
See lSim simulator here
ISE Project Navigator (P.68d)
project.xise - [mymodule01_tb.v]
File Edit View Project
Design
View: Implementation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
No Processes Running
Processes: mymodule01_tb
ISim Simulator
Start Design Files Libraries
mymodule01.v Design Summary mymodule01_tb.v
Ln 66 Col 11 Verilog
44 // Initialize Inputs
45 A = 0;
46 B = 0;
47 e = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
52 // Add stimulus here
53 A = 0;
54 B = 0;
55 e = 1;
56 #20;
57
58 A = 0;
59 B = 1;
60 e = 1;
61 #40;
62
63 A = 1;
64 B = 0;
65 e = 1;
66 #60;
67
68 A = 1;
69 B = 1;
70 e = 1;
71 #80;
72
73 end
74
75 endmodule

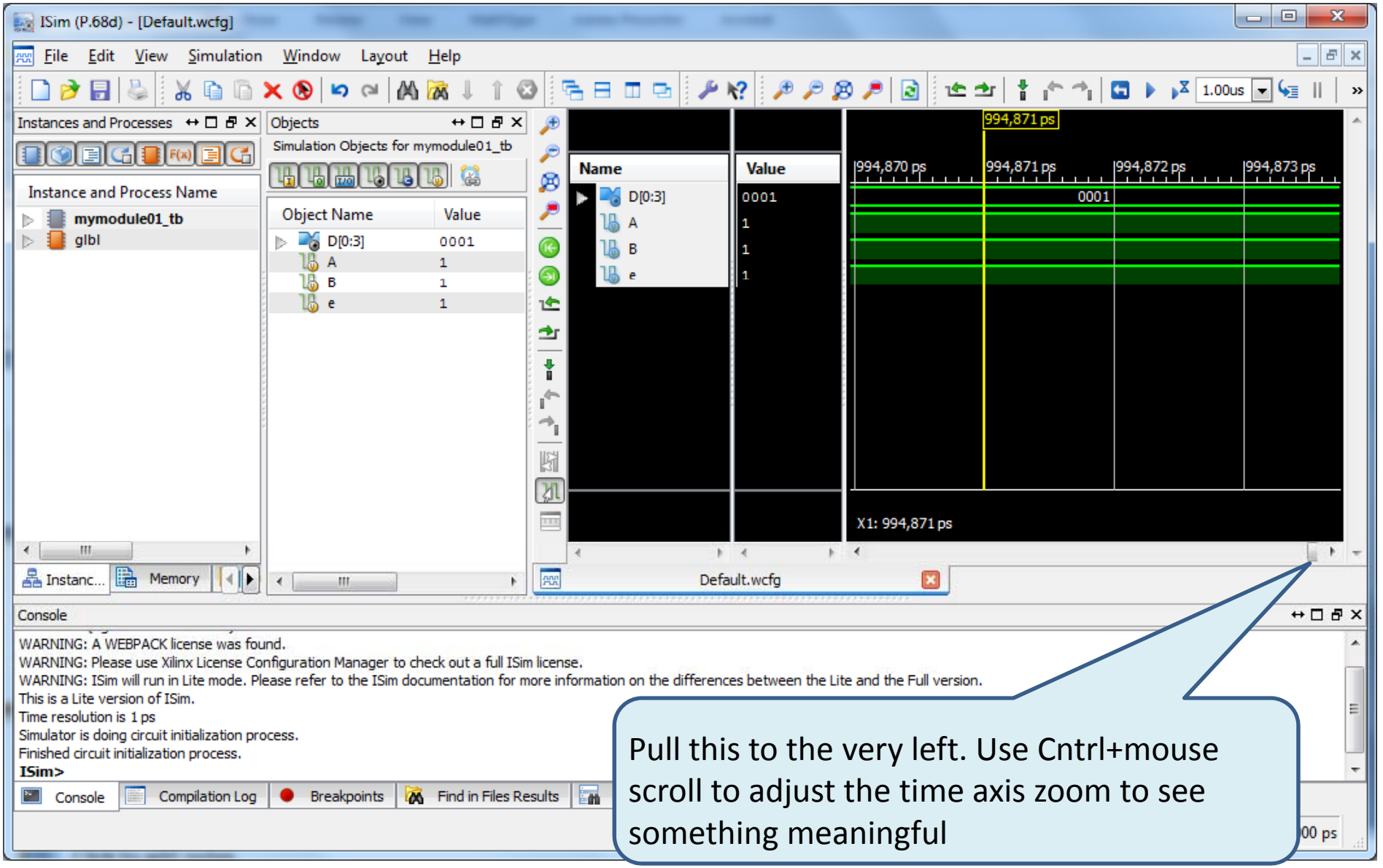

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
No Processes Running
Processes: mymodule01_tb
ISim Simulator
Click + to expand
44 // Initialize Inputs
45 A = 0;
46 B = 0;
47 e = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
52 // Add stimulus here
53 A = 0;
54 B = 0;
55 e = 1;
56 #20;
57
58 A = 0;
59 B = 1;
60 e = 1;
61 #40;
62
63 A = 1;
64 B = 0;
65 e = 1;
66 #60;
67
68 A = 1;
69 B = 1;
70 e = 1;
71 #80;
72
73 end
74
75 endmodule
Start Design Files Libraries
mymodule01.v Design Summary mymodule01_tb.v
Ln 66 Col 11 Verilog

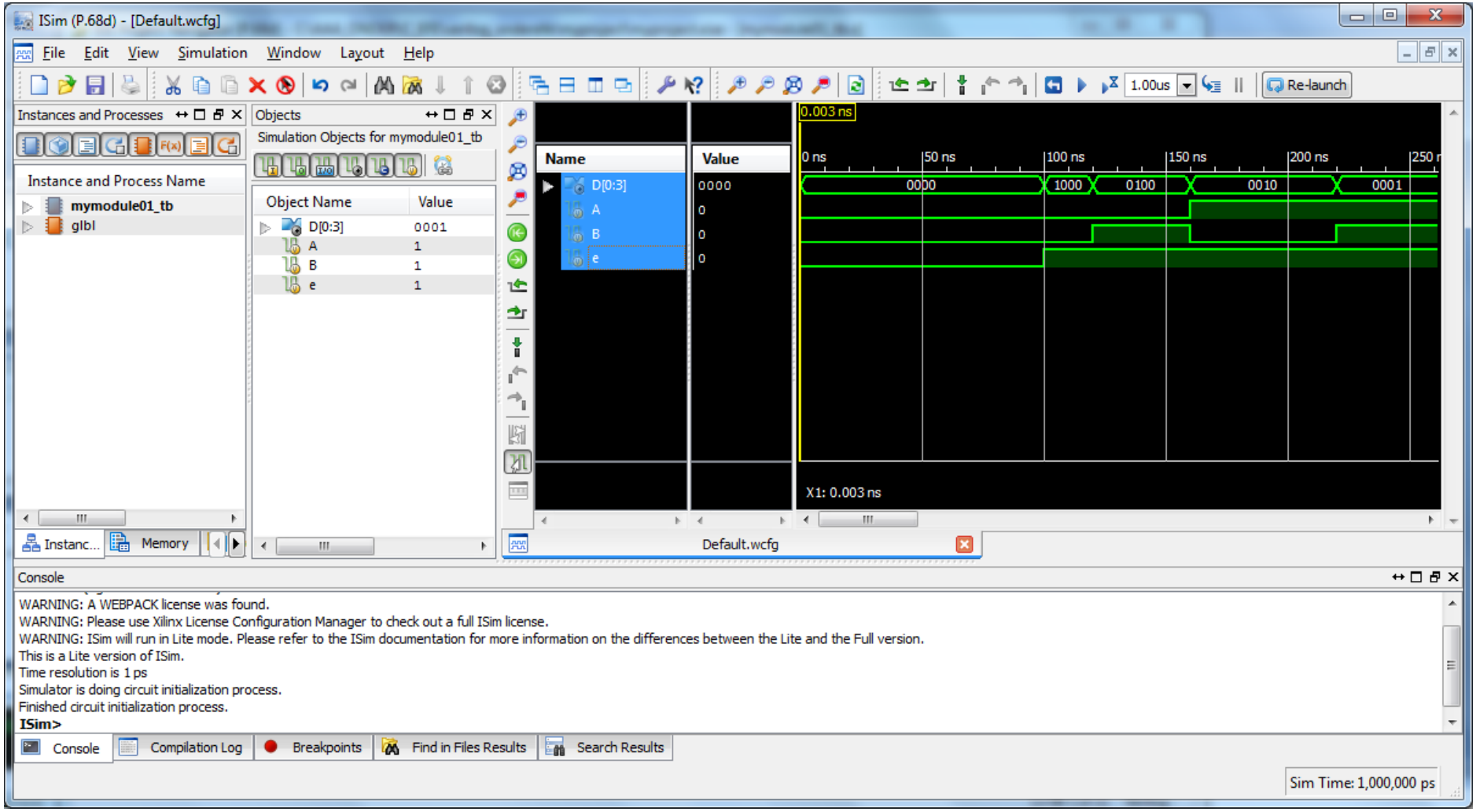

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
No Processes Running
Processes: mymodule01_tb
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Double click “Simulate Behavioral Model”
44 // Initialize Inputs
45 A = 0;
46 B = 0;
47 e = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
57
58 A = 0;
59 B = 1;
60 e = 1;
61 #40;
62
63 A = 1;
64 B = 0;
65 e = 1;
66 #60;
67
68 A = 1;
69 B = 1;
70 e = 1;
71 #80;
72
73 end
74
75 endmodule
Start Design Files Libraries
mymodule01.v Design Summary mymodule01_tb.v
Ln 66 Col 11 Verilog

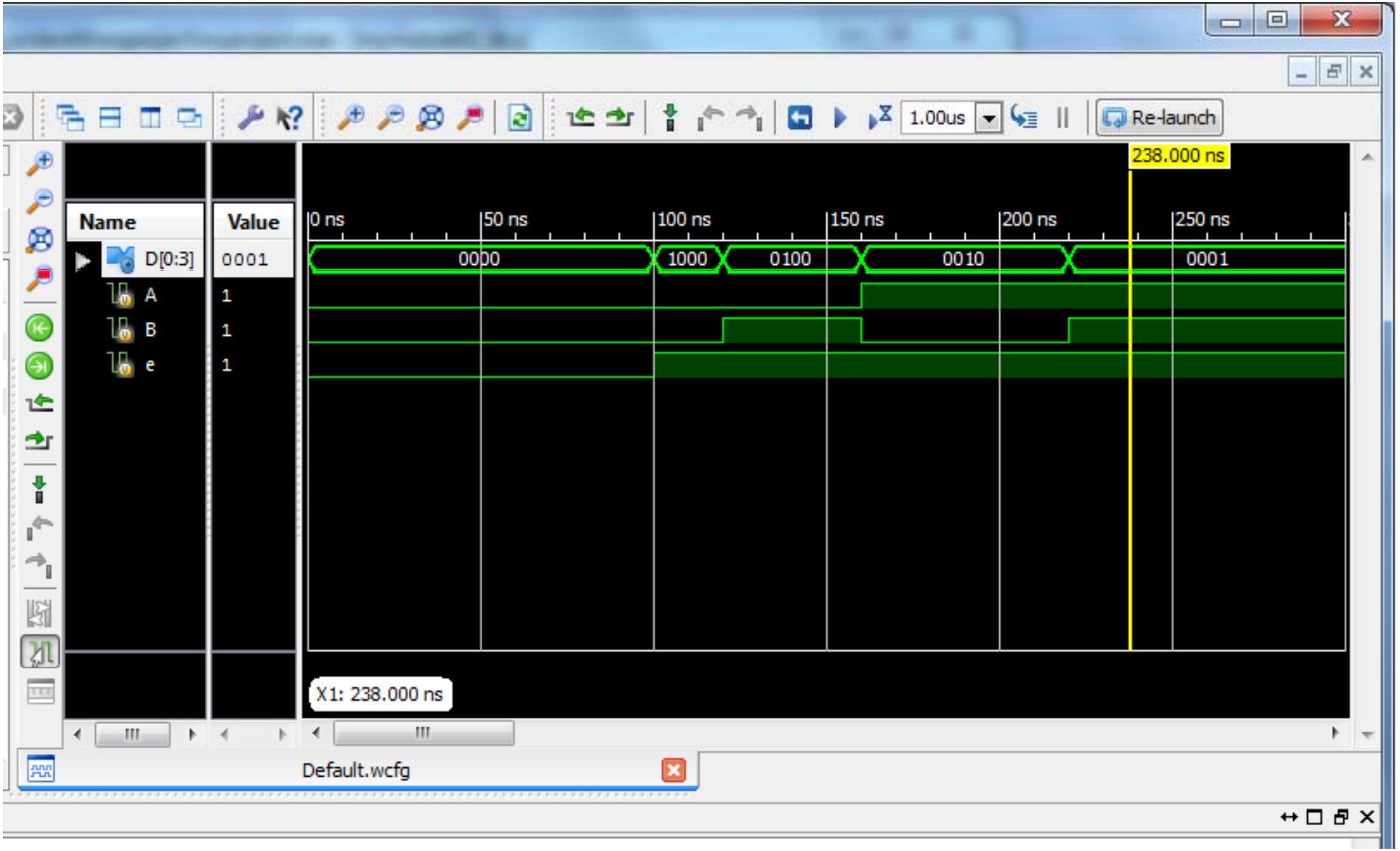

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
Running: Simulation Elaboration
Processes: mymodule01_tb
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
44 // Initialize Inputs
45 A = 0;
46 B = 0;
47 e = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
52 // Add stimulus here
53 A = 0;
54 B = 0;
55 e = 1;
56 #20;
57
58 A = 0;
59 B = 1;
60 e = 1;
61 #40;
62
63 A = 1;
64 B = 0;
65 e = 1;
66 #60;
67
68 A = 1;
69 B = 1;
70 e = 1;
71 #80;
72
73 end
74
75 endmodule
mymodule01.v
Design Summary
mymodule01_tb.v
Ln 66 Col 11
Verilog

What is next?

- After the processing is finished, Isim window will appear automatically

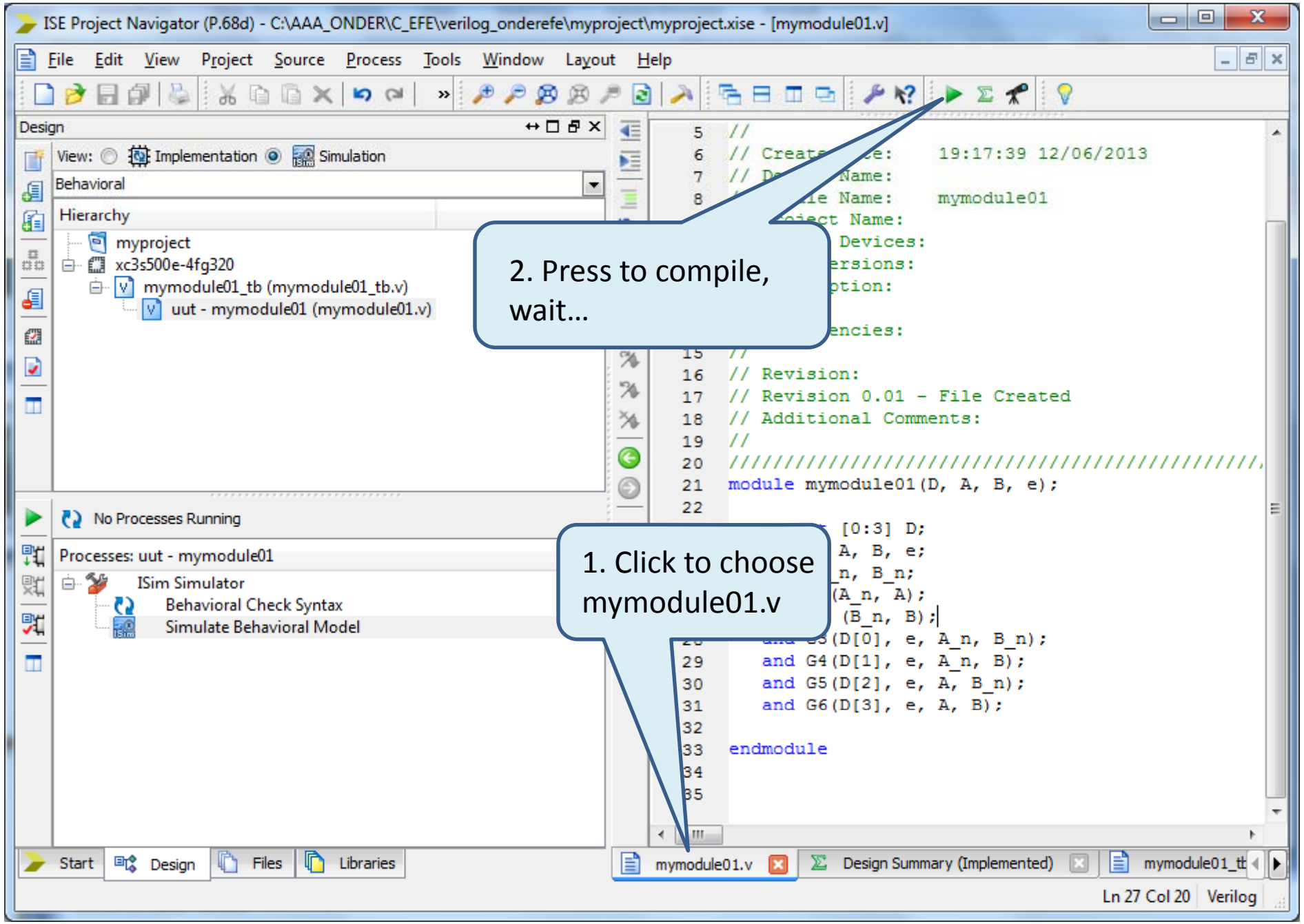

ISim (P.68d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
mymodule01_tb
glbl
Objects
Simulation Objects for mymodule01_tb
Object Name
Value
D[0:3]
0001
A
1
B
1
e
1
Name
Value
D[0:3]
0001
A
1
B
1
e
1
994,871 ps
994,870 ps
994,871 ps
994,872 ps
994,873 ps
0001
X1: 994,871 ps
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Pull this to the very left. Use Cntrl+mouse scroll to adjust the time axis zoom to see something meaningful

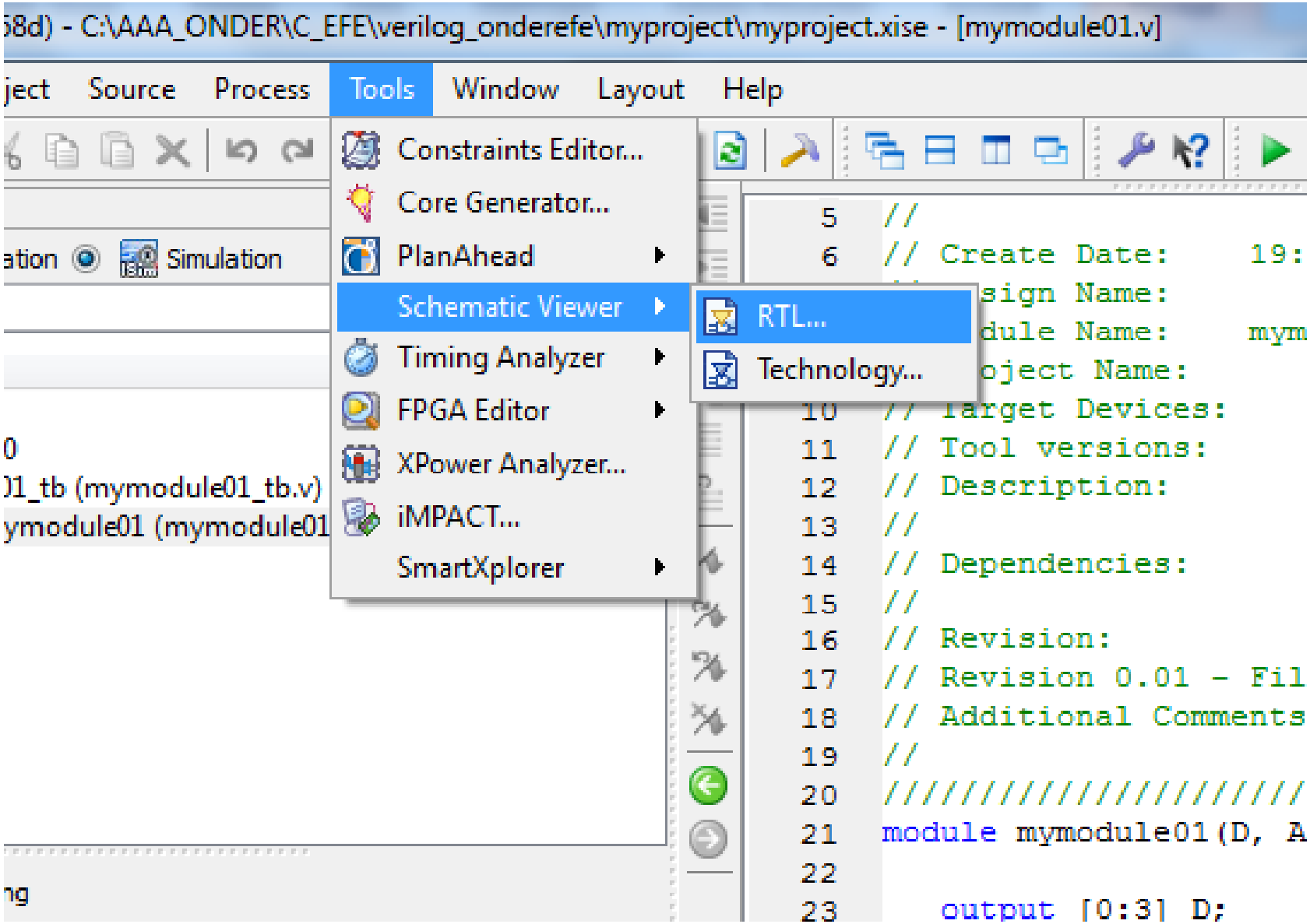

ISim (P.68d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
mymodule01_tb
glbl
Objects
Simulation Objects for mymodule01_tb
Object Name
Value
D[0:3]
0001
A
1
B
1
e
1
Name
Value
D[0:3]
0000
A
0
B
0
e
0
0.003 ns
0 ns
50 ns
100 ns
150 ns
200 ns
0000
1000
0100
0010
0001
X1: 0.003 ns
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

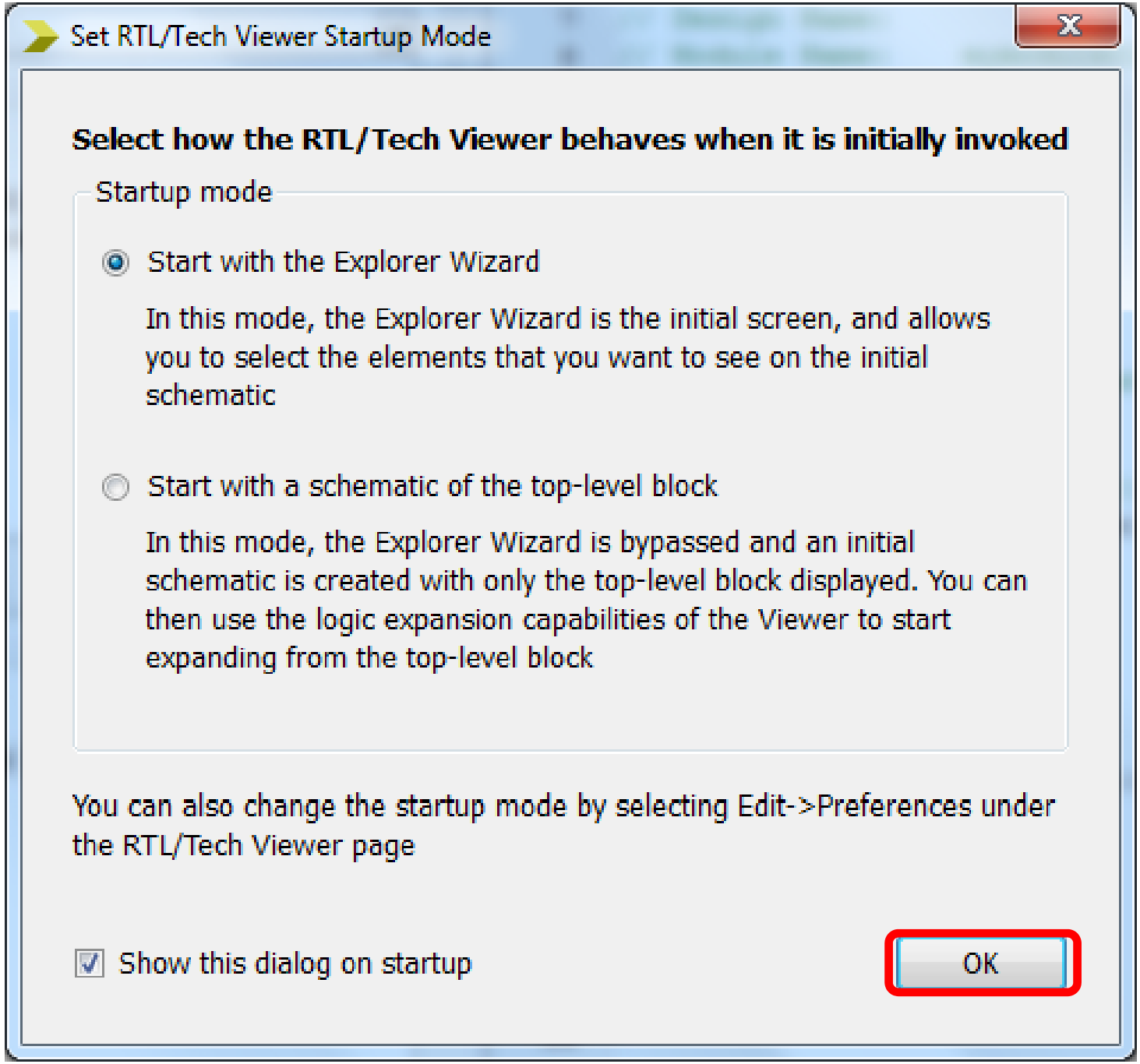

1.00us
Re-launch
238.000 ns
Name
Value
D[0:3]
0001
A
1
B
1
e
1
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
0000
1000
0100
0010
0001
X1: 238.000 ns
Default.wcfg

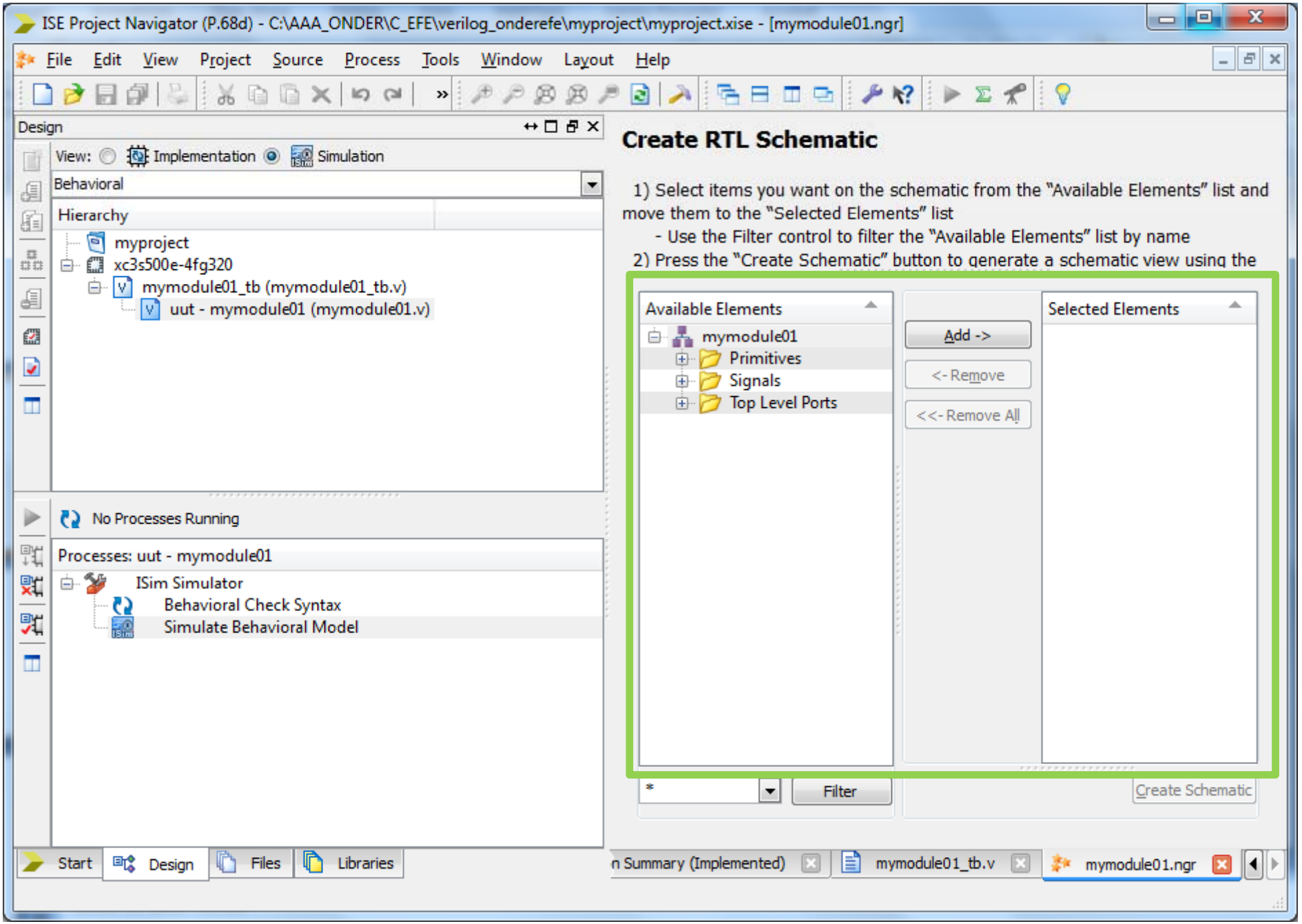
Creating the Schematic - Syntesis

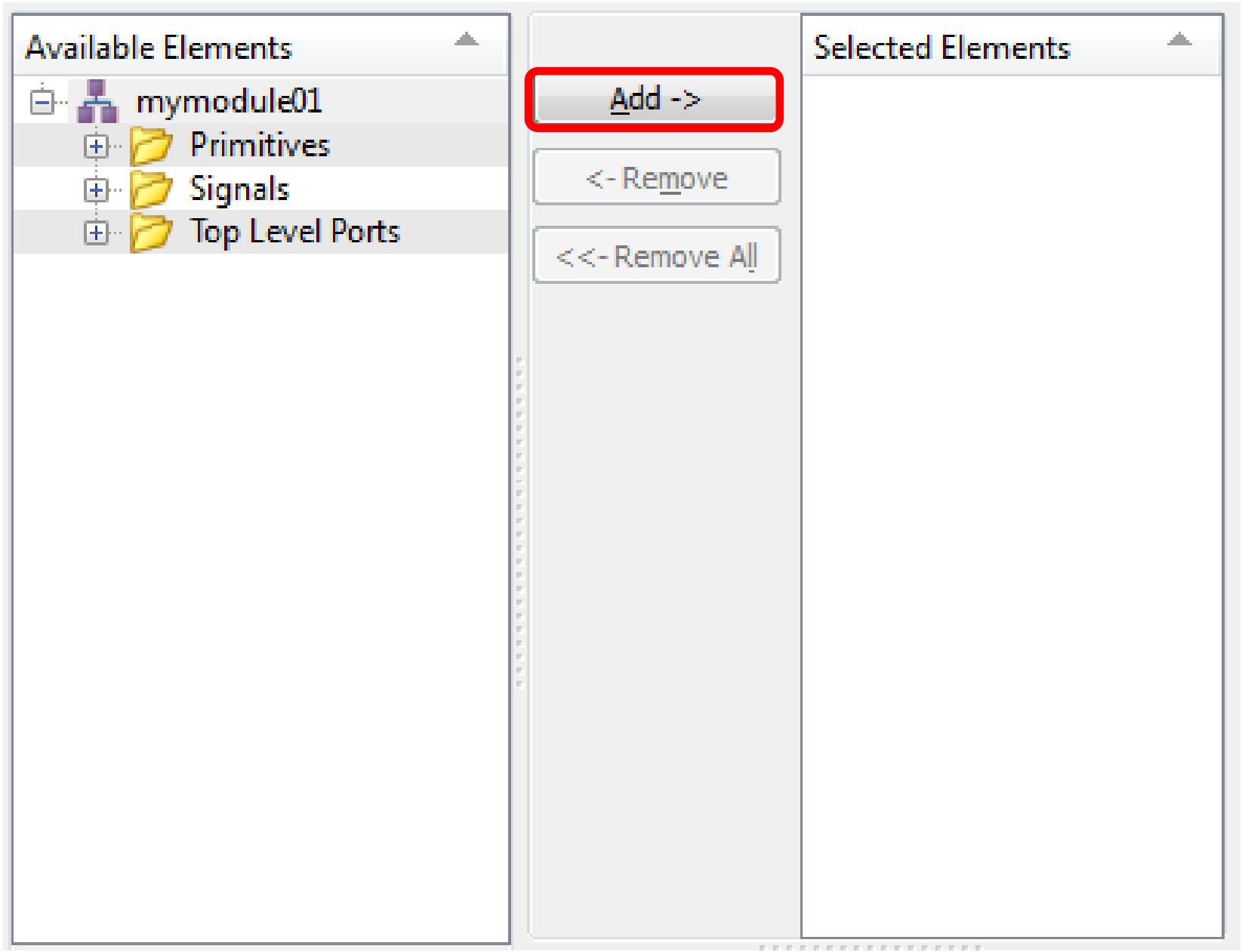
- We defined the logic system via a bunch of code lines. What is the circuit corresponding to our code?
- Can it be optimized according to the physical hardware in hand?

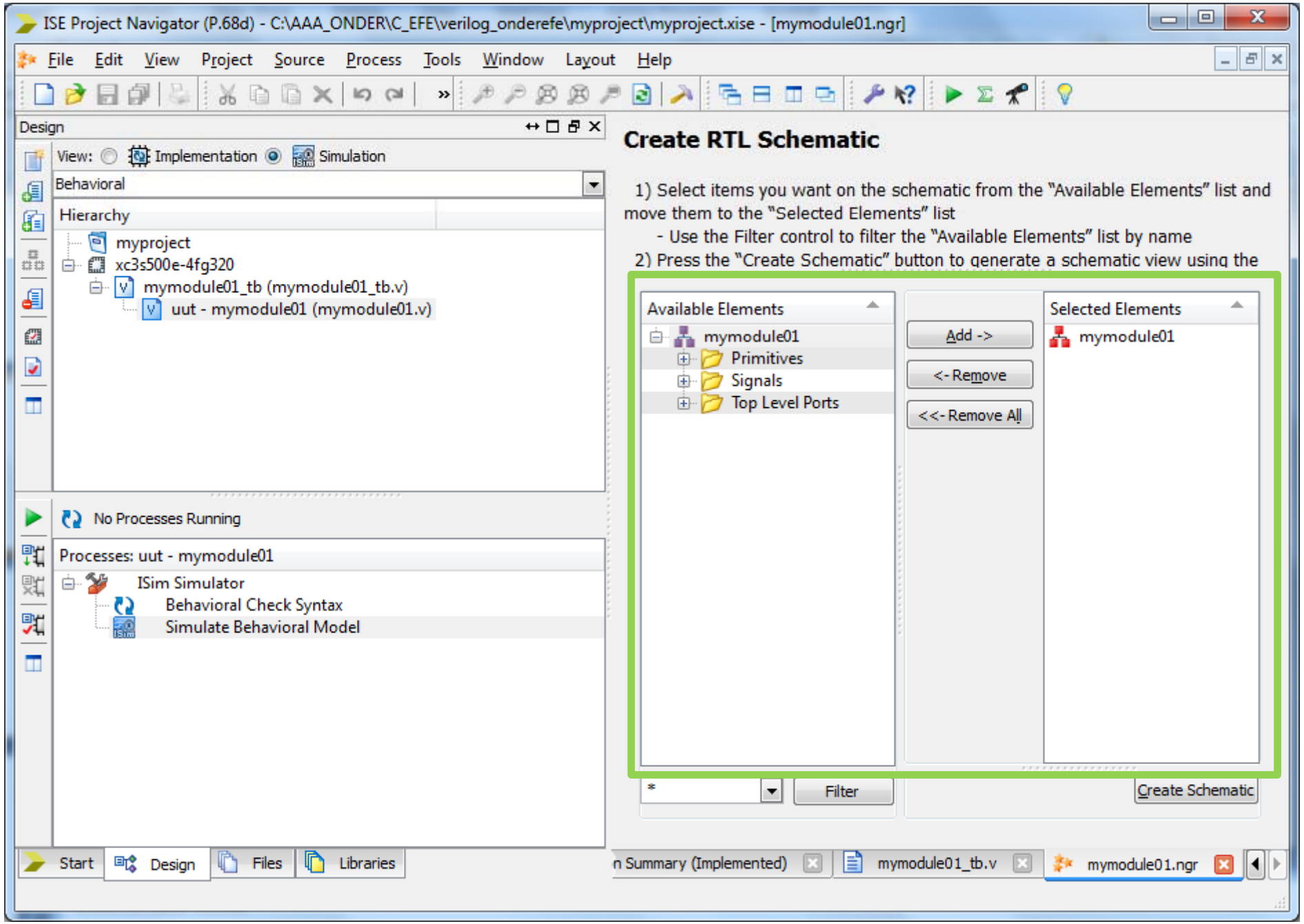

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
2. Press to compile, wait…
1. Click to choose mymodule01.v
// Create Date: 19:17:39 12/06/2013
// Module Name: mymodule01
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module mymodule01(D, A, B, e);
and G4(D[1], e, A_n, B);
and G5(D[2], e, A, B_n);
and G6(D[3], e, A, B);
endmodule
Start Design Files Libraries
mymodule01.v
Design Summary (Implemented)
Ln 27 Col 20 Verilog

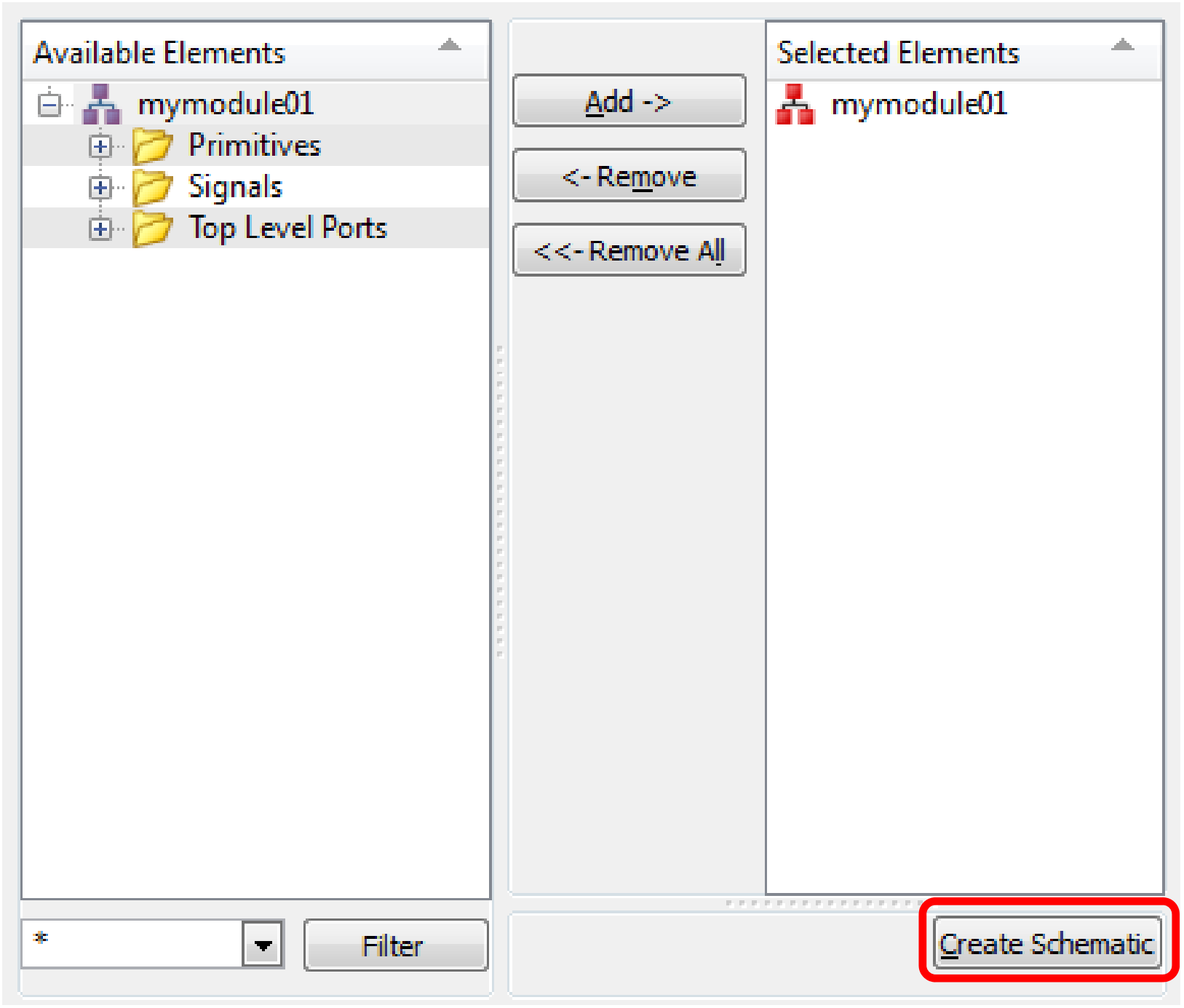

58d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.v]
ject Source Process Tools Window Layout Help
Constraints Editor...
Core Generator...
PlanAhead
Schematic Viewer
Timing Analyzer
FPGA Editor
XPower Analyzer...
iMPACT...
SmartXplorer
RTL...
Technology...
ation Simulation
0
01_tb (mymodule01_tb.v)
ymodule01 (mymodule01
ng
5 //
6 // Create Date: 19:
sign Name:
dule Name: mym
oject Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - Fil
18 // Additional Comments
19 //
20 //////////////////////
21 module mymodule01(D, A
22
23 output [0:3] D;

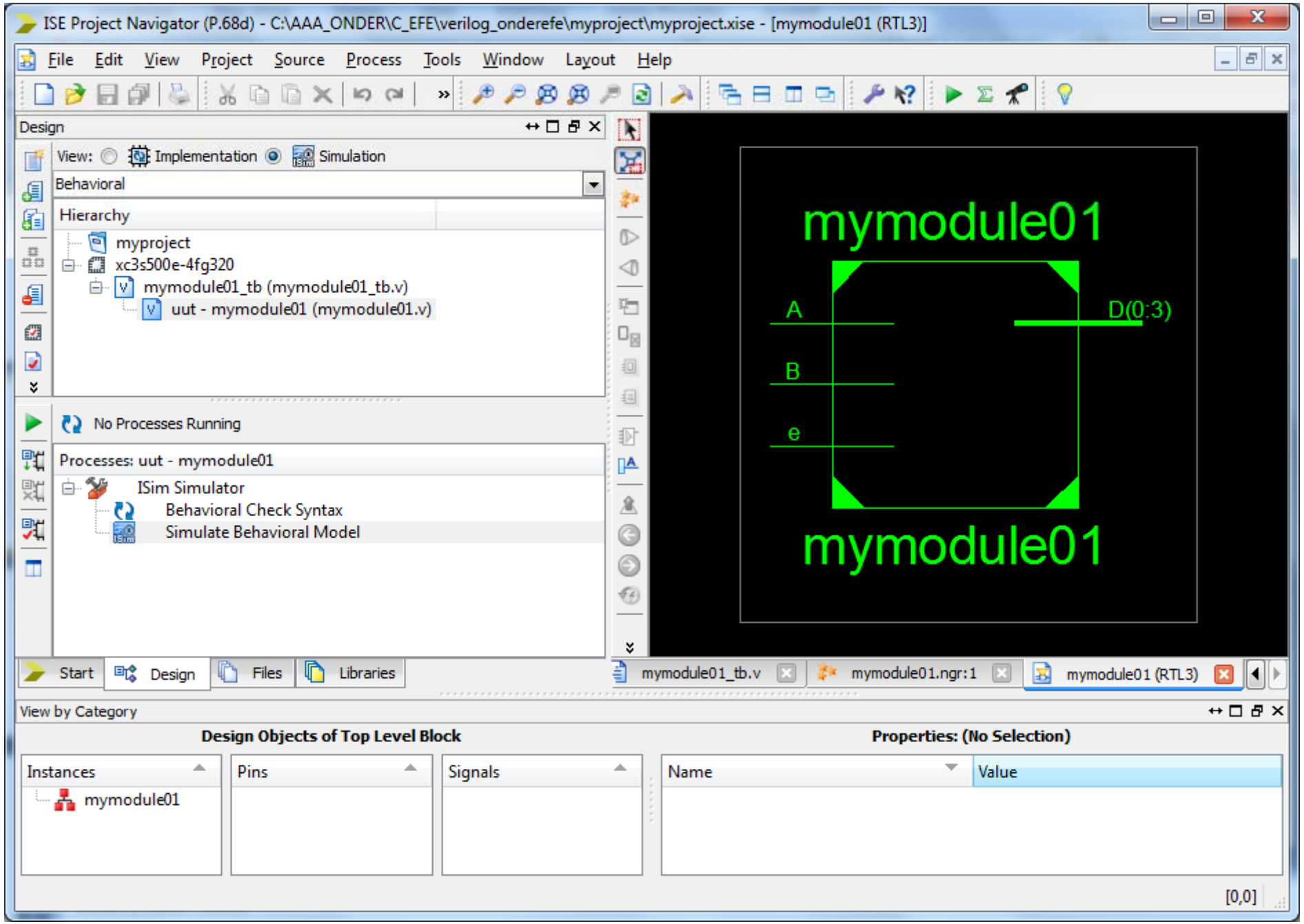

Set RTL/Tech Viewer Startup Mode
Select how the RTL/Tech Viewer behaves when it is initially invoked
Startup mode
Start with the Explorer Wizard
In this mode, the Explorer Wizard is the initial screen, and allows you to select the elements that you want to see on the initial schematic
Start with a schematic of the top-level block
In this mode, the Explorer Wizard is bypassed and an initial schematic is created with only the top-level block displayed. You can then use the logic expansion capabilities of the Viewer to start expanding from the top-level block
You can also change the startup mode by selecting Edit->Preferences under the RTL/Tech Viewer page
Show this dialog on startup
OK

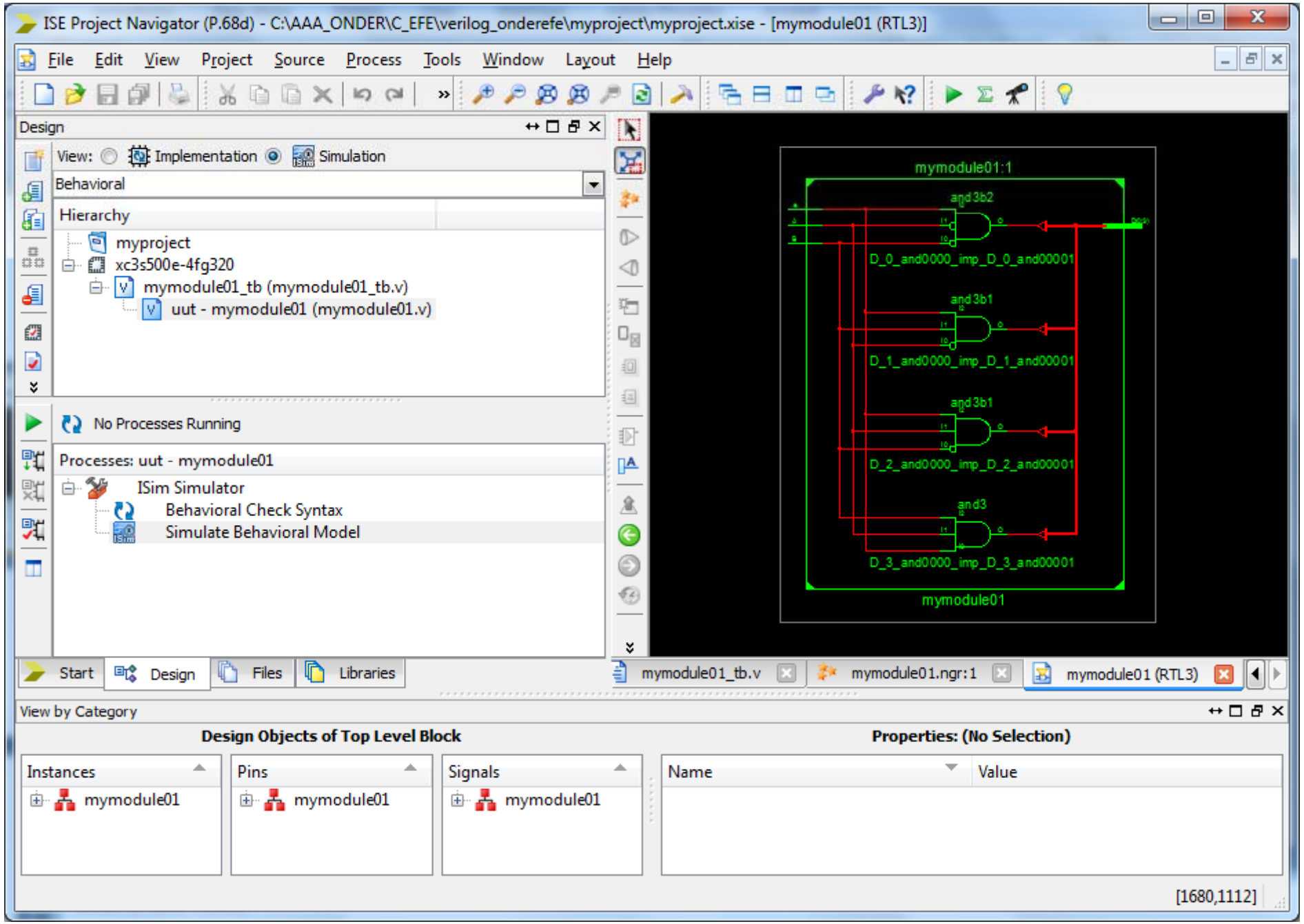

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.ngr]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Create RTL Schematic
1) Select items you want on the schematic from the "Available Elements" list and move them to the "Selected Elements" list
- Use the Filter control to filter the "Available Elements" list by name
2) Press the "Create Schematic" button to generate a schematic view using the
Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Selected Elements
*
Filter
Create Schematic
Start
Design
Files
Libraries
n Summary (Implemented)
mymodule01_tb.v
mymodule01.ngr

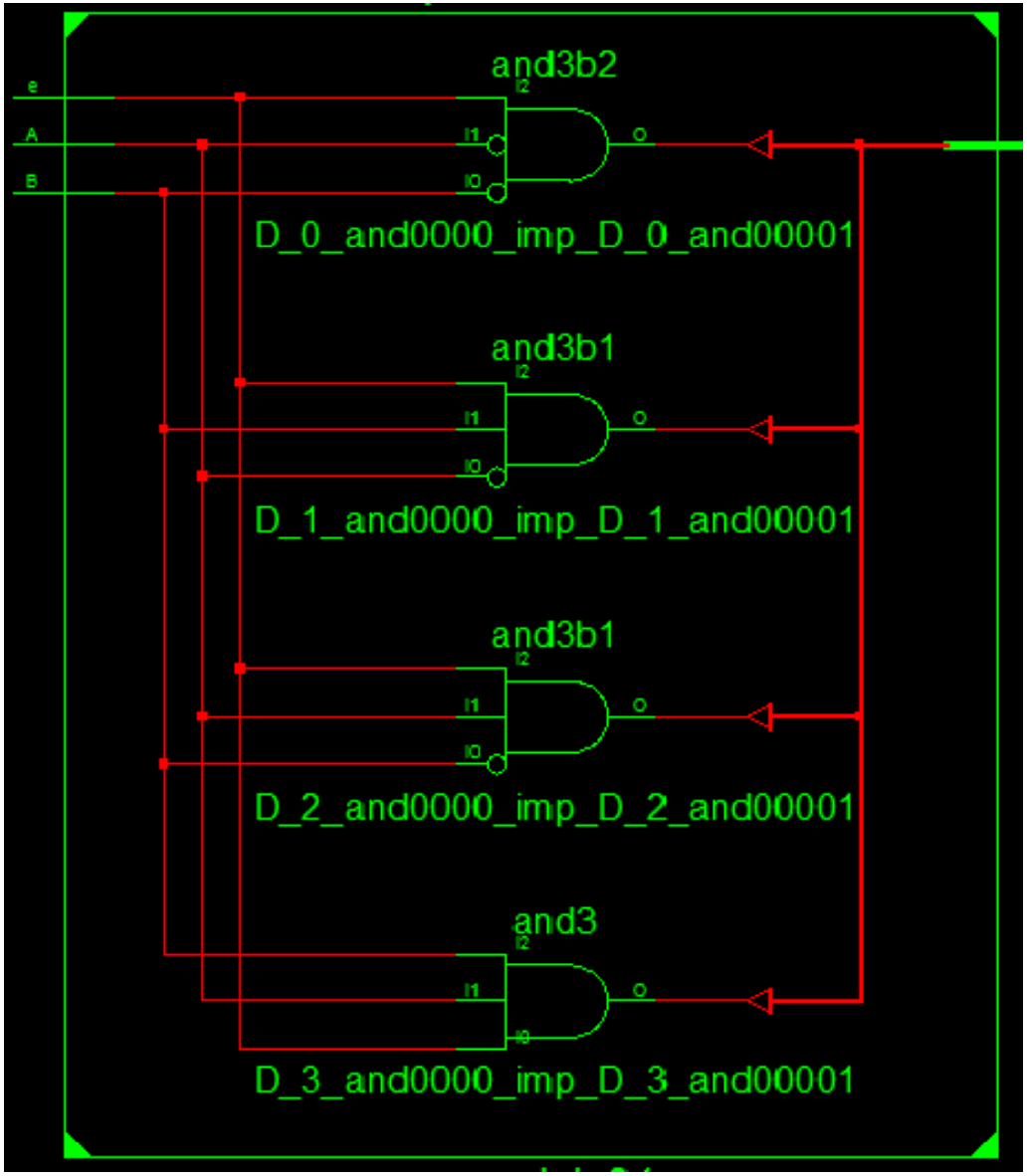

Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Selected Elements

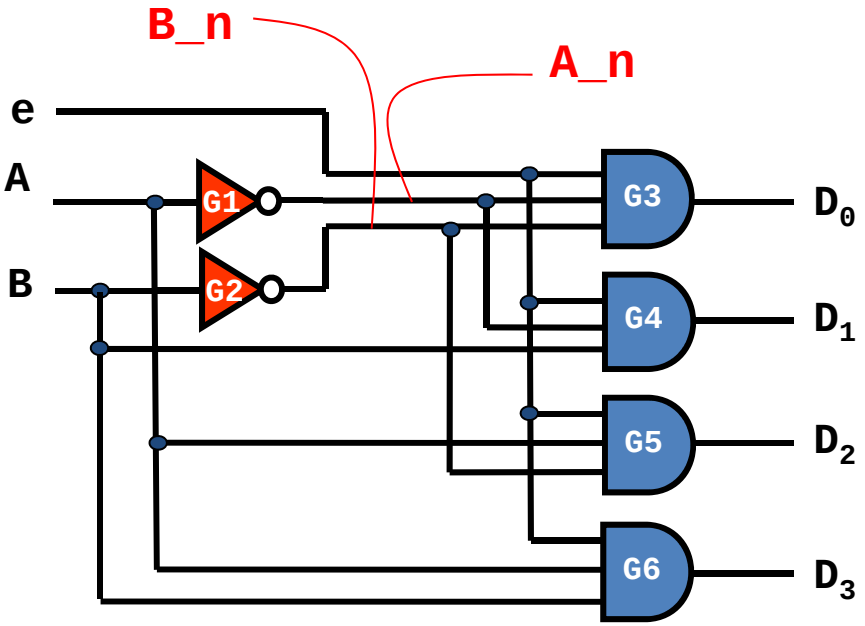

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.ngr]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Create RTL Schematic
1) Select items you want on the schematic from the "Available Elements" list and move them to the "Selected Elements" list
- Use the Filter control to filter the "Available Elements" list by name
2) Press the "Create Schematic" button to generate a schematic view using the
Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Selected Elements
mymodule01
*
Filter
Create Schematic
Start
Design
Files
Libraries
n Summary (Implemented)
mymodule01_tb.v
mymodule01.ngr

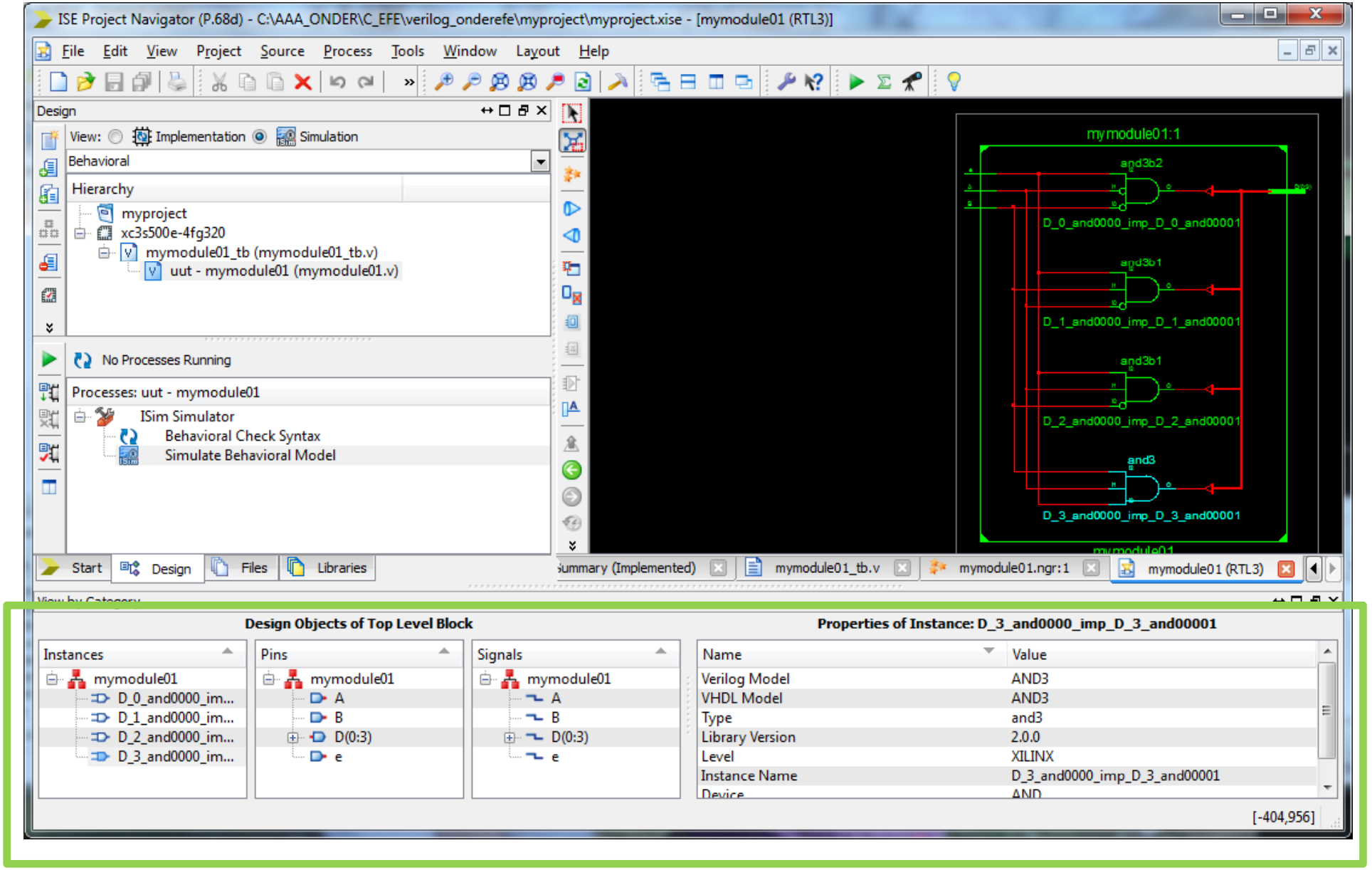

Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Selected Elements
mymodule01
*
Filter
Create Schematic

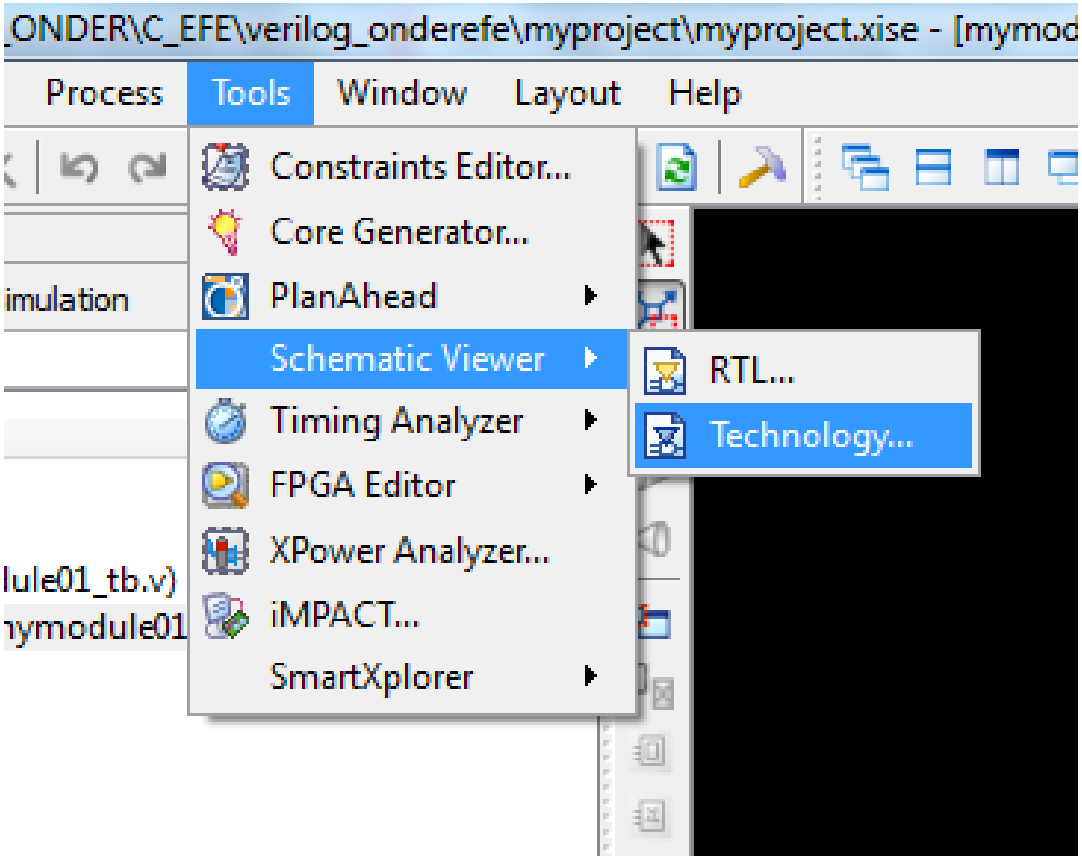

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01 (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
mymodule01
A
B
e
D(0:3)
mymodule01
Start Design Files Libraries
mymodule01_tb.v mymodule01.ngr:1 mymodule01 (RTL3)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances Pins Signals Name Value
mymodule01
[0,0]


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01 (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
mymodule01:1
and3b2
D_0_and0000_imp_D_0_and00001
and3b1
D_1_and0000_imp_D_1_and00001
and3b1
D_2_and0000_imp_D_2_and00001
and3
D_3_and0000_imp_D_3_and00001
mymodule01
Start Design Files Libraries
mymodule01_tb.v
mymodule01.ngr:1
mymodule01 (RTL3)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
mymodule01
mymodule01
mymodule01
[1680,1112]


and3b2
e
A
B
I1
I0
O
D_0_and0000_imp_D_0_and00001
and3b1
D_1_and0000_imp_D_1_and00001
and3b1
D_2_and0000_imp_D_2_and00001
and3
D_3_and0000_imp_D_3_and00001


B_n
A_n
e
A
B
G1
G2
G3
G4
G5
G6
D0
D1
D2
D3


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01 (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
mymodule01:1
and3b2
D_0_and0000_imp_D_0_and00001
and3b1
D_1_and0000_imp_D_1_and00001
and3b1
D_2_and0000_imp_D_2_and00001
and3
D_3_and0000_imp_D_3_and00001
mymodule01
Summary (Implemented)
mymodule01_tb.v
mymodule01.ngr:1
mymodule01 (RTL3)
Design Objects of Top Level Block
Instances
mymodule01
D_0_and0000_im...
D_1_and0000_im...
D_2_and0000_im...
D_3_and0000_im...
Pins
mymodule01
A
B
D(0:3)
e
Signals
mymodule01
A
B
D(0:3)
e
Properties of Instance: D_3_and0000_imp_D_3_and00001
Name
Value
Verilog Model
AND3
VHDL Model
AND3
Type
and3
Library Version
2.0.0
Level
XILINX
Instance Name
D_3_and0000_imp_D_3_and00001
Device
AND
[-404,956]


_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymod
Process
Tools
Window
Layout
Help
Constraints Editor...
Core Generator...
PlanAhead
Schematic Viewer
Timing Analyzer
FPGA Editor
XPower Analyzer...
iMPACT...
SmartXplorer
RTL...
Technology...
imulation
lule01_tb.v)
ymodule01

RTL View

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic.

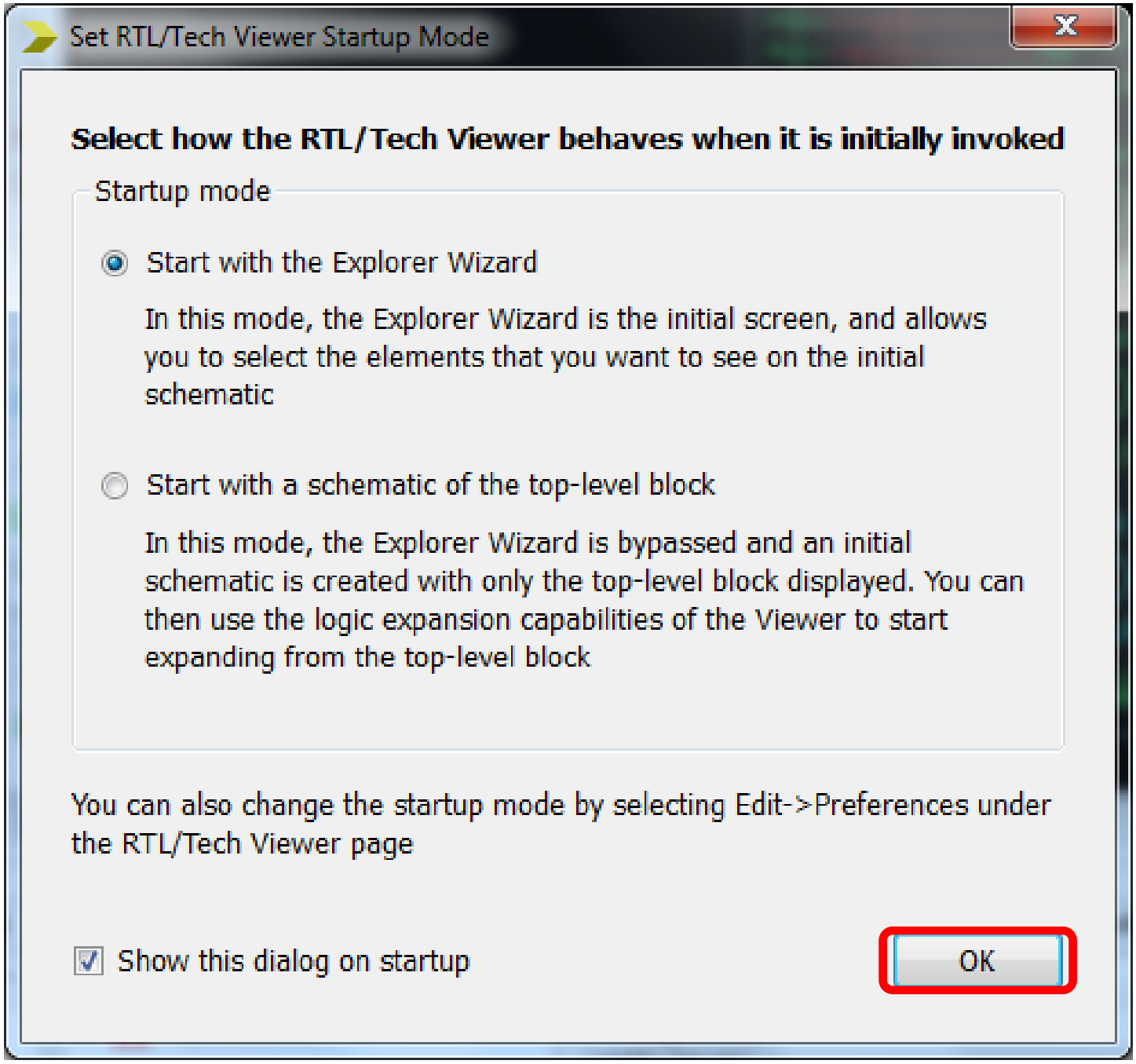
This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

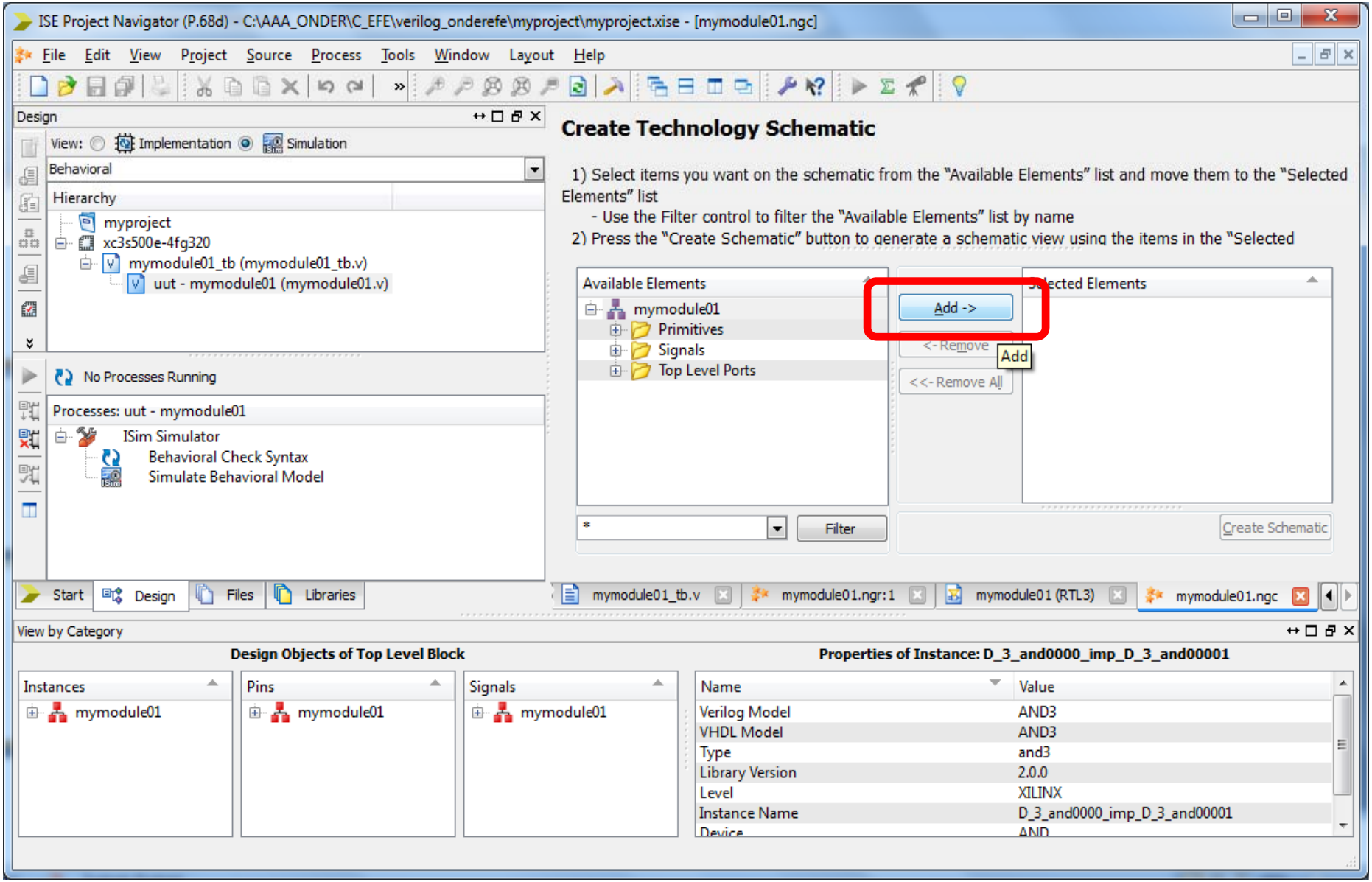
Technology View

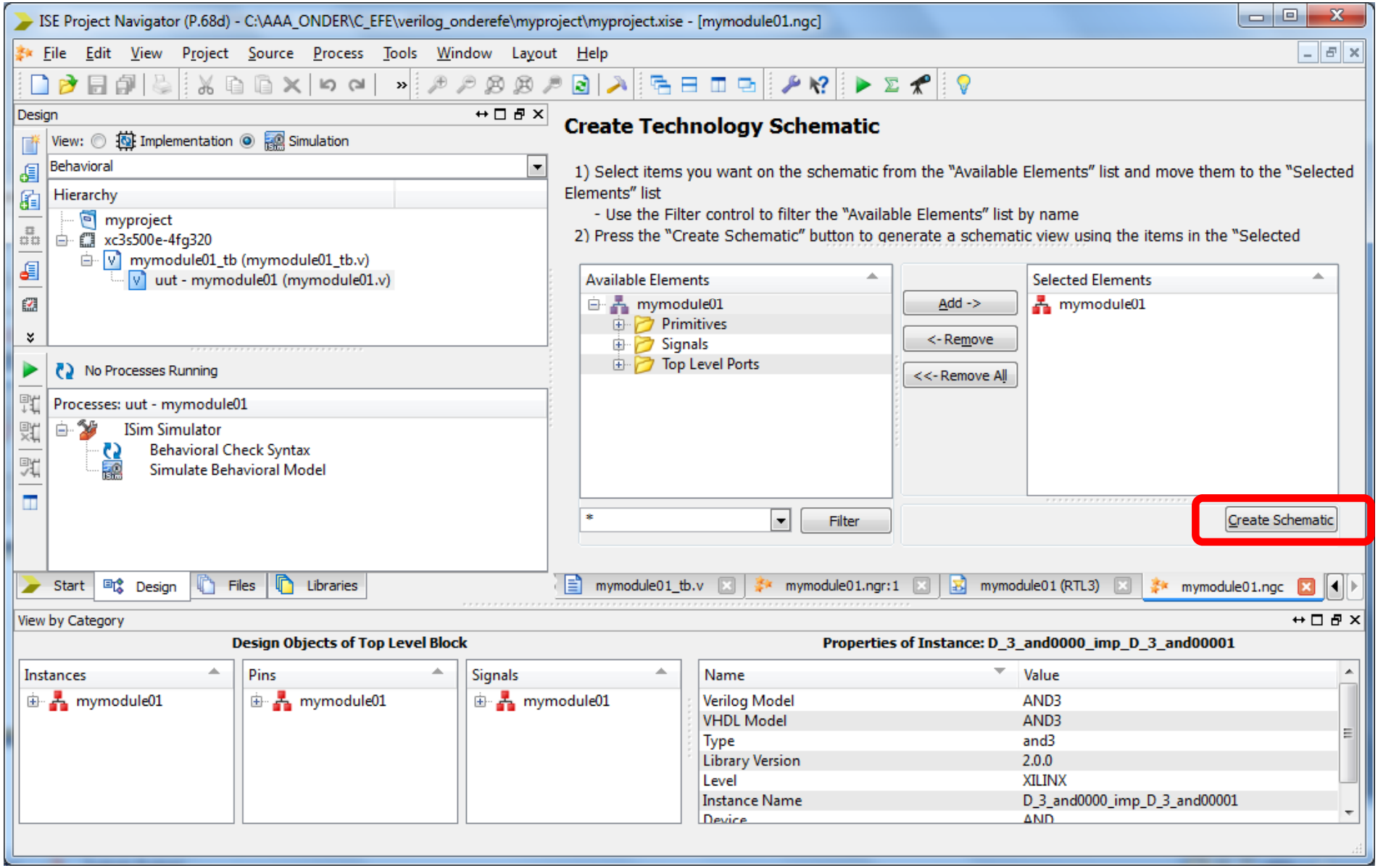
Viewing a Technology schematic opens an NGC file that can be viewed as an architecture-specific schematic.

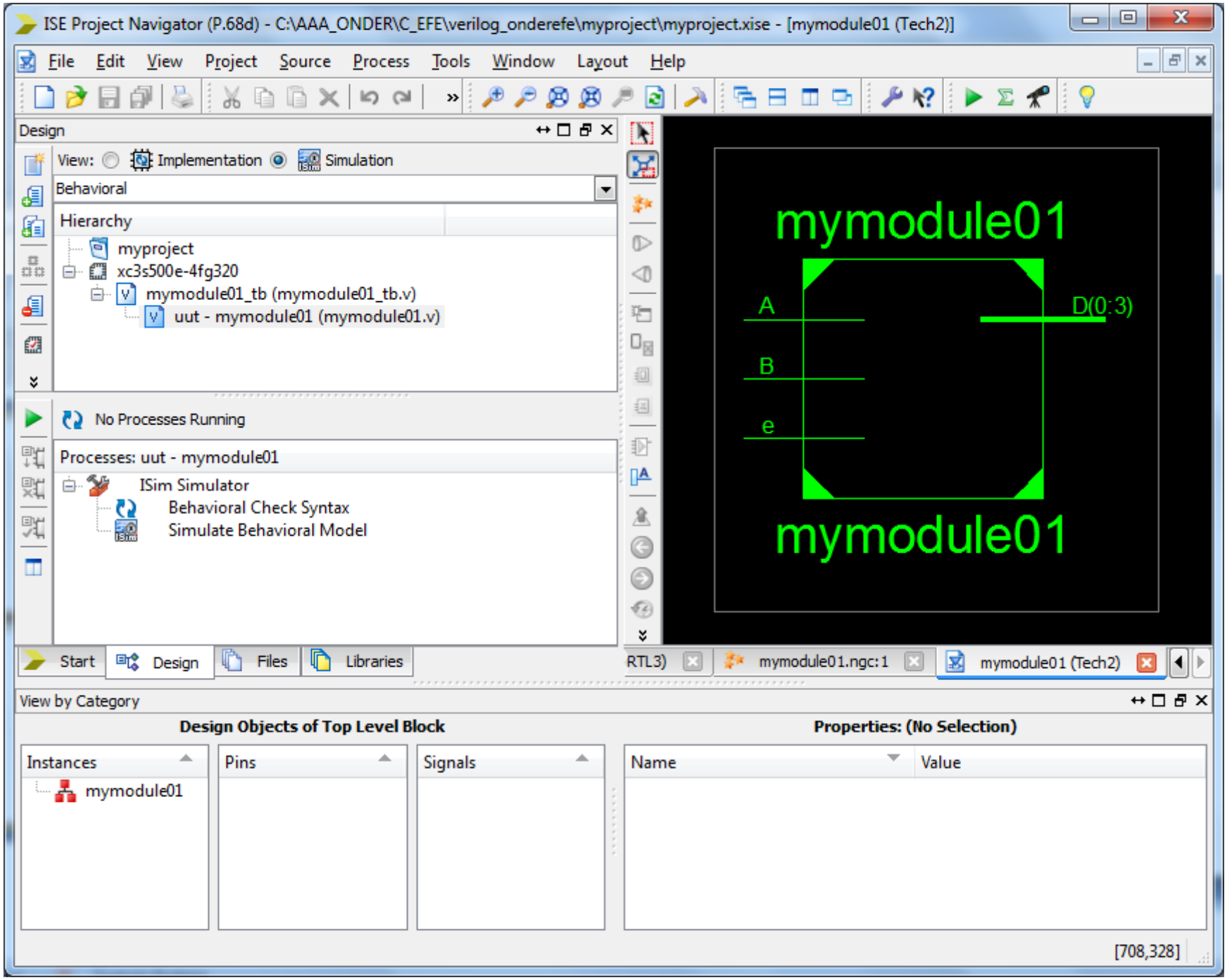
This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of of LUTs, carry logic, I/O buffers, and other technology-specific components. Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture, which might help you discover design issues early in the design process.

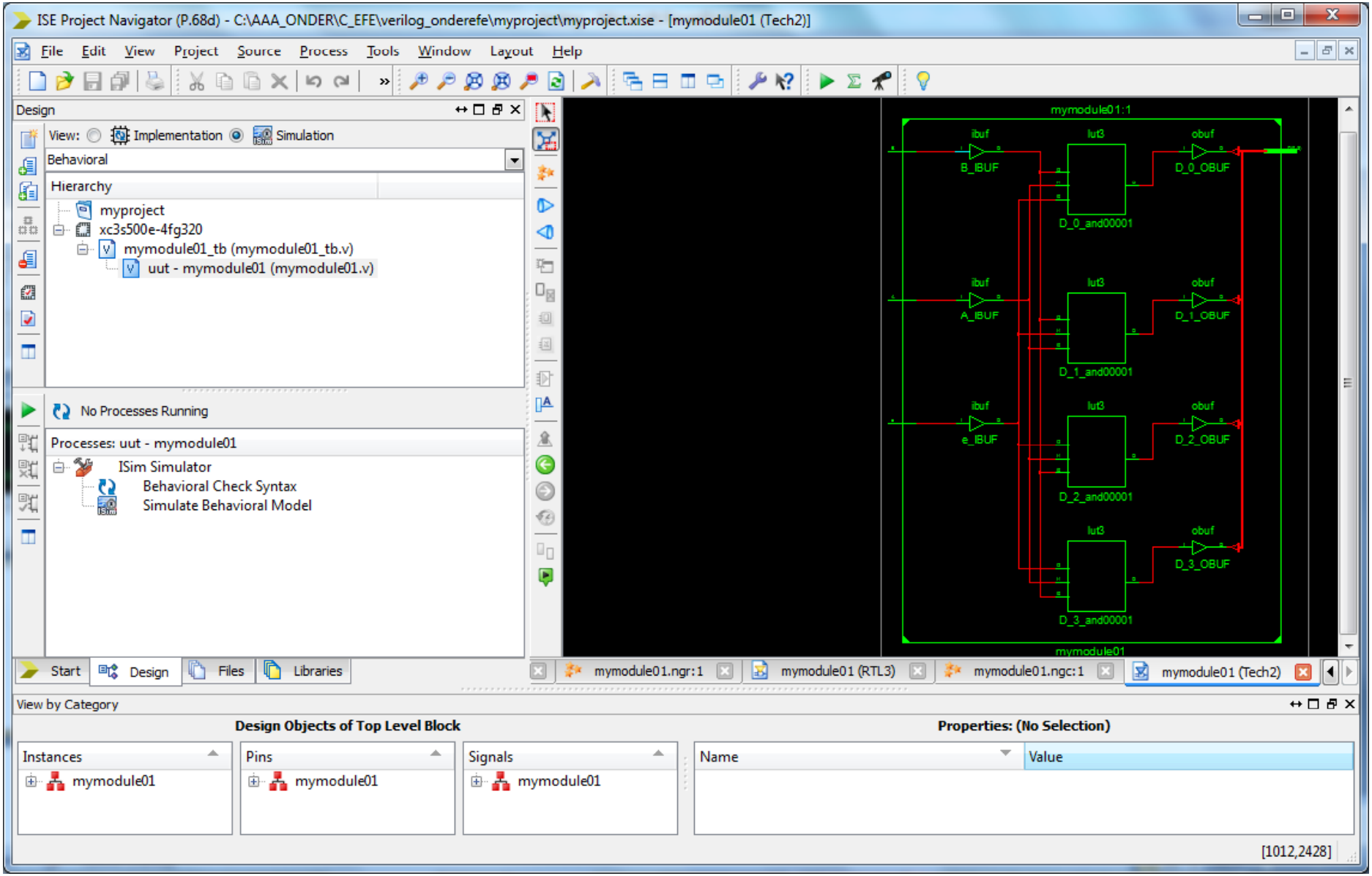
You should always refer to technology schematic for synthesized result.

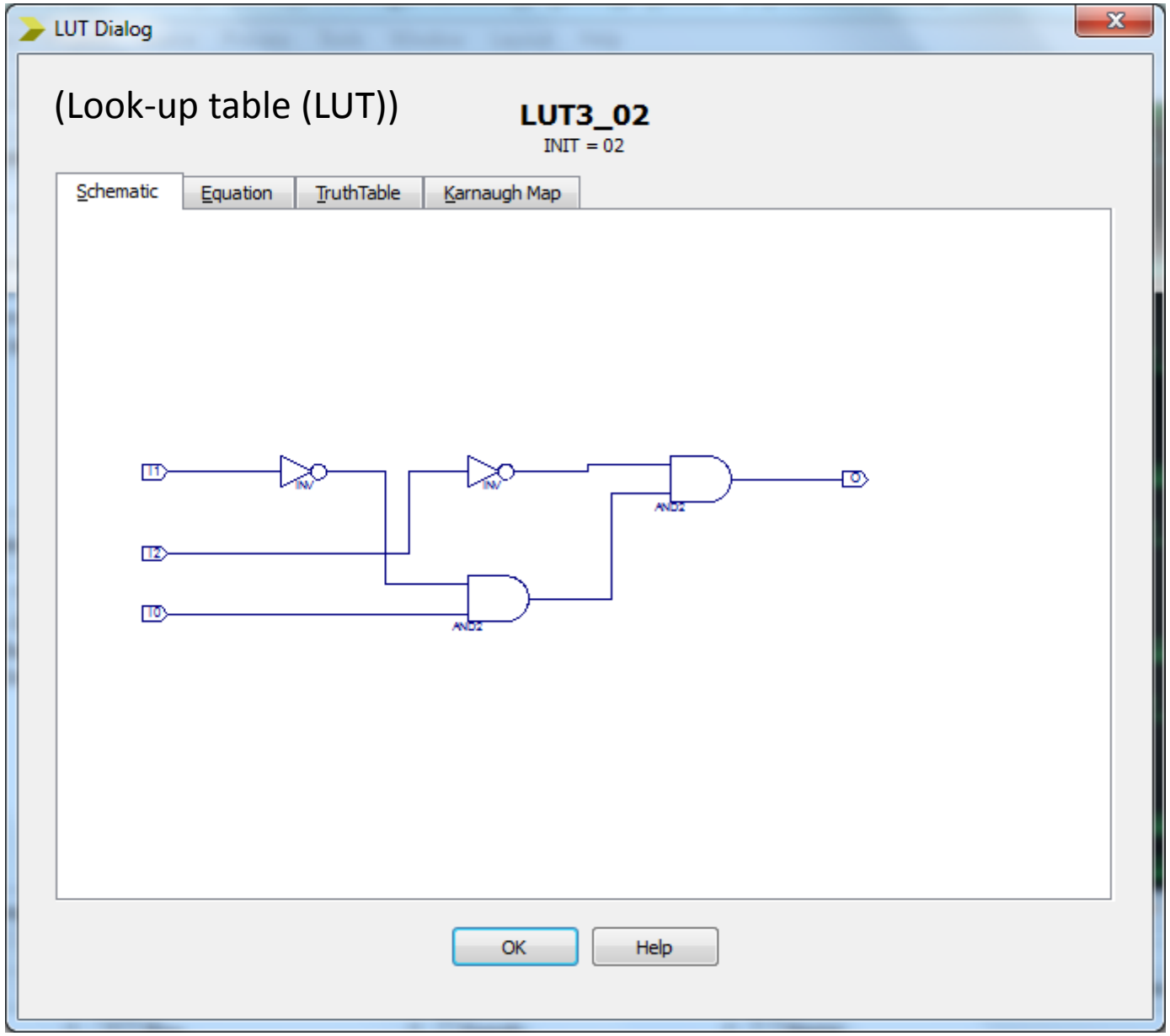

Set RTL/Tech Viewer Startup Mode
Select how the RTL/Tech Viewer behaves when it is initially invoked
Startup mode
Start with the Explorer Wizard
In this mode, the Explorer Wizard is the initial screen, and allows you to select the elements that you want to see on the initial schematic
Start with a schematic of the top-level block
In this mode, the Explorer Wizard is bypassed and an initial schematic is created with only the top-level block displayed. You can then use the logic expansion capabilities of the Viewer to start expanding from the top-level block
You can also change the startup mode by selecting Edit->Preferences under the RTL/Tech Viewer page
Show this dialog on startup
OK

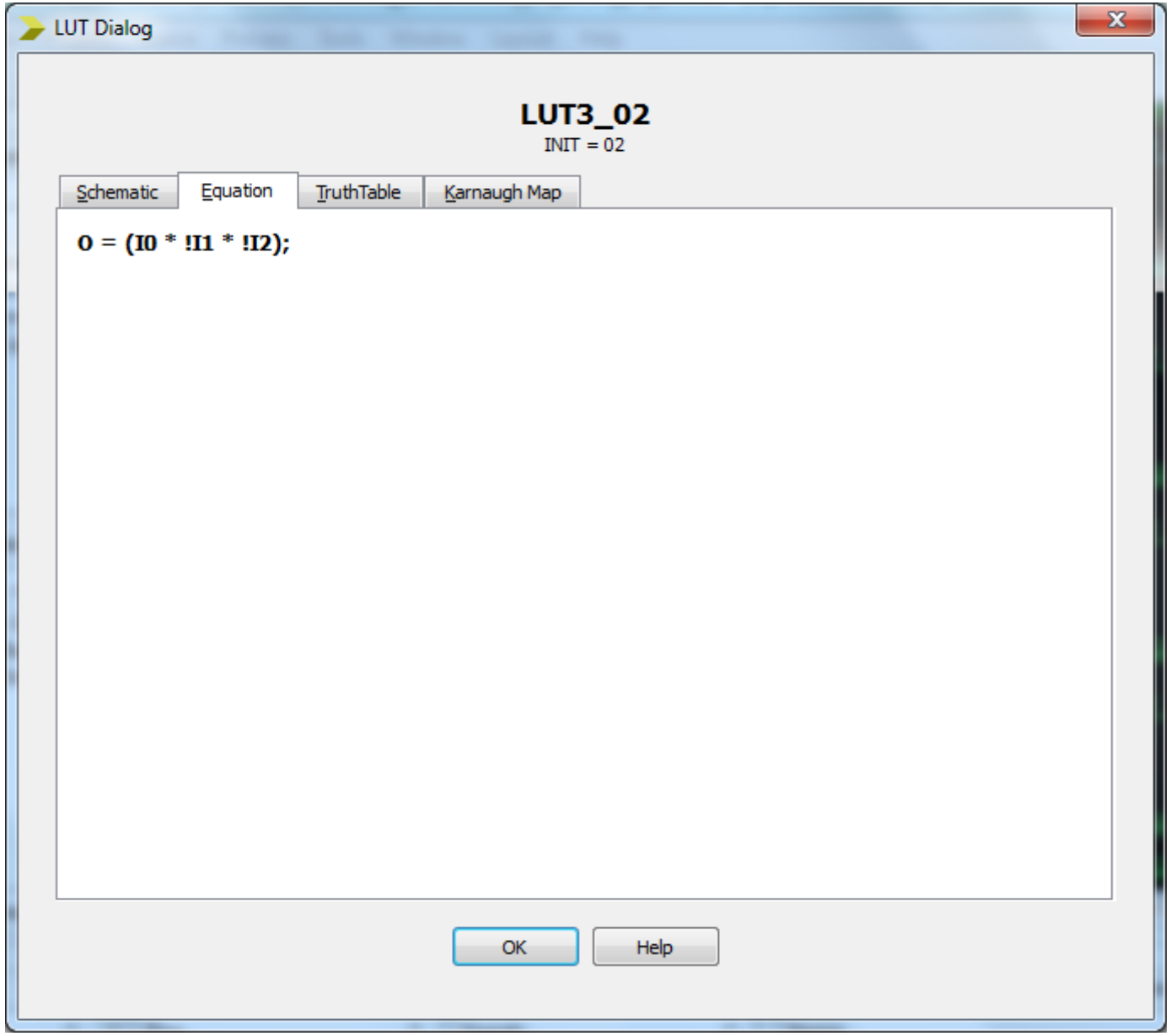

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.ngc]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Create Technology Schematic
1) Select items you want on the schematic from the "Available Elements" list and move them to the "Selected Elements" list
- Use the Filter control to filter the "Available Elements" list by name
2) Press the "Create Schematic" button to generate a schematic view using the items in the "Selected
Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Add
Filter
Create Schematic
Start Design Files Libraries
mymodule01_tb.v
mymodule01.ngr:1
mymodule01 (RTL3)
mymodule01.ngc
View by Category
Design Objects of Top Level Block
Instances
mymodule01
Pins
mymodule01
Signals
mymodule01
Properties of Instance: D_3_and0000_imp_D_3_and00001
Name
Value
Verilog Model AND3
VHDL Model AND3
Type and3
Library Version 2.0.0
Level XILINX
Instance Name D_3_and0000_imp_D_3_and00001
Device AND

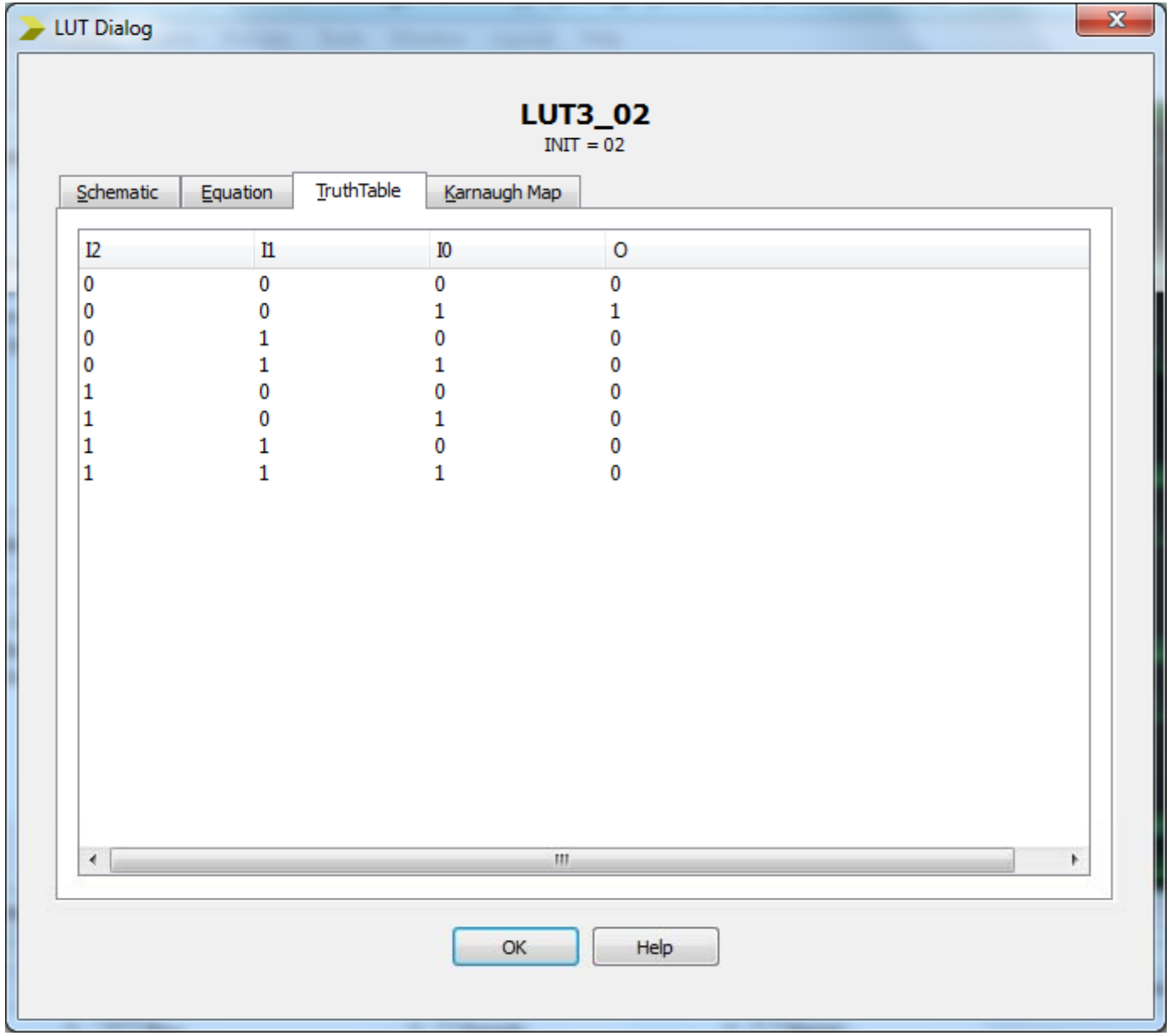

ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01.ngc]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Create Technology Schematic
1) Select items you want on the schematic from the "Available Elements" list and move them to the "Selected Elements" list
- Use the Filter control to filter the "Available Elements" list by name
2) Press the "Create Schematic" button to generate a schematic view using the items in the "Selected
Available Elements
mymodule01
Primitives
Signals
Top Level Ports
Add ->
<- Remove
<<- Remove All
Selected Elements
mymodule01
*
Filter
Create Schematic
Start Design Files Libraries
mymodule01_tb.v
mymodule01.ngr:1
mymodule01 (RTL3)
mymodule01.ngc
View by Category
Design Objects of Top Level Block
Instances
mymodule01
Pins
mymodule01
Signals
mymodule01
Properties of Instance: D_3_and0000_imp_D_3_and00001
Name
Value
Verilog Model AND3
VHDL Model AND3
Type and3
Library Version 2.0.0
Level XILINX
Instance Name D_3_and0000_imp_D_3_and00001
Device AND


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01 (Tech2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
mymodule01
A
B
e
D(0:3)
mymodule01
Start
Design
Files
Libraries
RTL3)
mymodule01.ngc:1
mymodule01 (Tech2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
mymodule01
[708,328]


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [mymodule01 (Tech2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
myproject
xc3s500e-4fg320
mymodule01_tb (mymodule01_tb.v)
uut - mymodule01 (mymodule01.v)
No Processes Running
Processes: uut - mymodule01
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
mymodule01:1
ibuf
lut3
obuf
B_IBUF
D_0_OBUF
D_0_and00001
A_IBUF
D_1_OBUF
D_1_and00001
e_IBUF
D_2_OBUF
D_2_and00001
D_3_OBUF
D_3_and00001
mymodule01
Start
Design
Files
Libraries
mymodule01.ngr:1
mymodule01 (RTL3)
mymodule01.ngc:1
mymodule01 (Tech2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
mymodule01
[1012,2428]


LUT Dialog
(Look-up table (LUT))
LUT3_02
INIT = 02
Schematic
Equation
TruthTable
Karnaugh Map
I1
I2
I0
INV
INV
AND2
AND2
O
OK
Help


LUT Dialog
LUT3_02
INIT = 02
Schematic
Equation
TruthTable
Karnaugh Map
O = (I0 * !I1 * !I2);
OK
Help

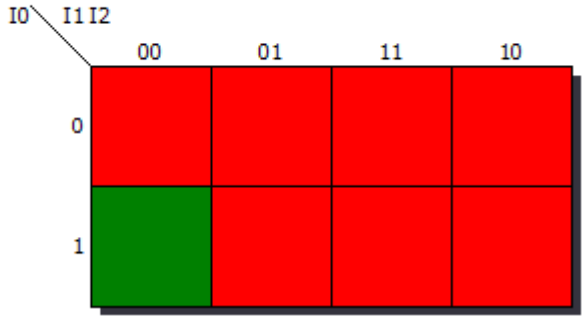

LUT Dialog
LUT3_02
INIT = 02
Schematic
Equation
TruthTable
Karnaugh Map
I2 I1 I0 O
0 0 0 0
0 0 1 1
0 1 0 0
0 1 1 0
1 0 0 0
1 0 1 0
1 1 0 0
1 1 1 0
OK
Help

LUT Dialog

LUT3_02

INIT = 02

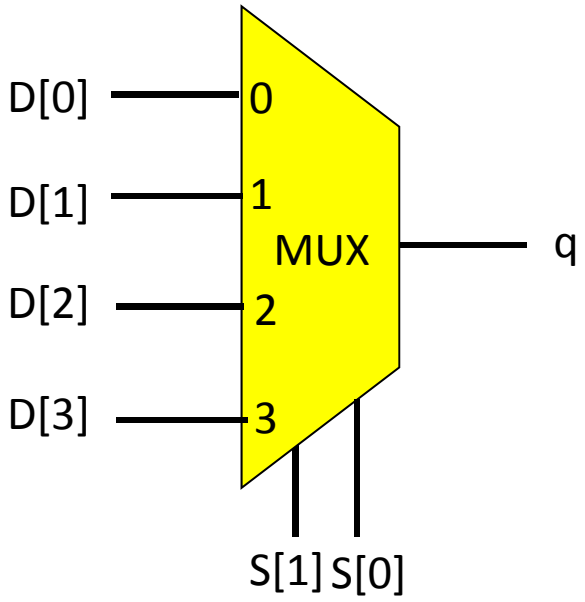
Schematic | Equation | TruthTable | Karnaugh Map



OK | Help

MUX

```
module mux1( select, d, q );
   input[1:0] select;
   input[3:0] d;
   output q;
   wire q;
   wire[1:0] select;
   wire[3:0] d;
   assign q = d[select];
endmodule
```



MUX Testbench 1/4

```
module mux1_tb;
        // Inputs
        reg [1:0] select;
        reg [3:0] d;
        // Outputs
        wire q;
        integer  i;
        // Instantiate the Unit Under Test (UUT)
        mux1 uut (
                .select(select),
                .d(d),
                .q(q)
        );
```

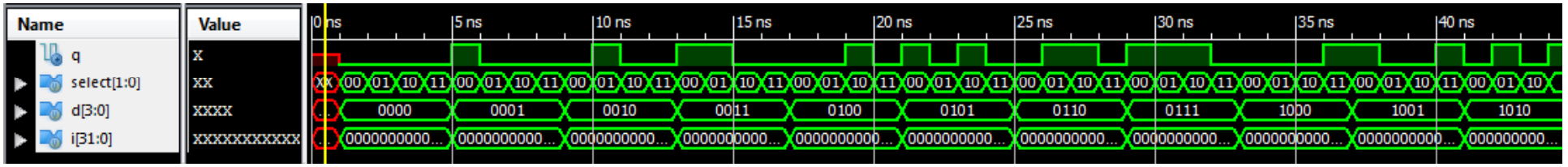
MUX Testbench 2/4

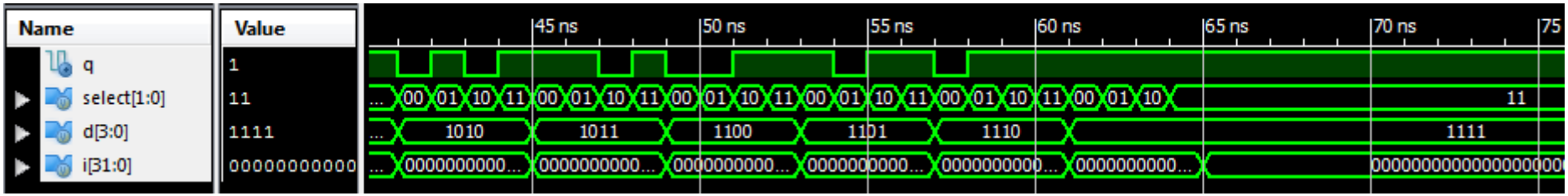
```
initial
begin
#1 $monitor("d = %b", d, “ | select = ", select, " | q = ", q );
        for( i = 0; i <= 15; i = i + 1)
        begin
                d = i;
                select = 0;  #1;
                select = 1;  #1;
                select = 2;  #1;
                select = 3;  #1;
                $display("------------------------------");
         end
end
endmodule
```

MUX Testbench 3/4

d = 0000 | select = 0 | q = 0
d = 0000 | select = 1 | q = 0
d = 0000 | select = 2 | q = 0
d = 0000 | select = 3 | q = 0
---
d = 0001 | select = 0 | q = 1
d = 0001 | select = 1 | q = 0
d = 0001 | select = 2 | q = 0
d = 0001 | select = 3 | q = 0
---
d = 0010 | select = 0 | q = 0
d = 0010 | select = 1 | q = 1
d = 0010 | select = 2 | q = 0
d = 0010 | select = 3 | q = 0
---
d = 0011 | select = 0 | q = 1
d = 0011 | select = 1 | q = 1
d = 0011 | select = 2 | q = 0
d = 0011 | select = 3 | q = 0
---
d = 0100 | select = 0 | q = 0
d = 0100 | select = 1 | q = 0
d = 0100 | select = 2 | q = 1
d = 0100 | select = 3 | q = 0
---
d = 0101 | select = 0 | q = 1
d = 0101 | select = 1 | q = 0
d = 0101 | select = 2 | q = 1
d = 0101 | select = 3 | q = 0
---
d = 0110 | select = 0 | q = 0
d = 0110 | select = 1 | q = 1
d = 0110 | select = 2 | q = 1
d = 0110 | select = 3 | q = 0
---
d = 0111 | select = 0 | q = 1
d = 0111 | select = 1 | q = 1
d = 0111 | select = 2 | q = 1
d = 0111 | select = 3 | q = 0
---
d = 1000 | select = 0 | q = 0
d = 1000 | select = 1 | q = 0
d = 1000 | select = 2 | q = 0
d = 1000 | select = 3 | q = 1
---
d = 1001 | select = 0 | q = 1
d = 1001 | select = 1 | q = 0
d = 1001 | select = 2 | q = 0
d = 1001 | select = 3 | q = 1
---
d = 1010 | select = 0 | q = 0
d = 1010 | select = 1 | q = 1
d = 1010 | select = 2 | q = 0
d = 1010 | select = 3 | q = 1
---
d = 1011 | select = 0 | q = 1
d = 1011 | select = 1 | q = 1
d = 1011 | select = 2 | q = 0
d = 1011 | select = 3 | q = 1
---
d = 1100 | select = 0 | q = 0
d = 1100 | select = 1 | q = 0
d = 1100 | select = 2 | q = 1
d = 1100 | select = 3 | q = 1
---
d = 1101 | select = 0 | q = 1
d = 1101 | select = 1 | q = 0
d = 1101 | select = 2 | q = 1
d = 1101 | select = 3 | q = 1
---
d = 1110 | select = 0 | q = 0
d = 1110 | select = 1 | q = 1
d = 1110 | select = 2 | q = 1
d = 1110 | select = 3 | q = 1
---
d = 1111 | select = 0 | q = 1
d = 1111 | select = 1 | q = 1
d = 1111 | select = 2 | q = 1
d = 1111 | select = 3 | q = 1

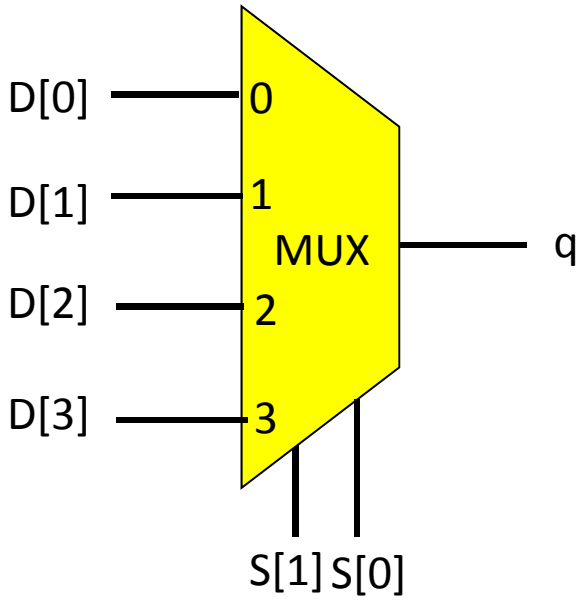
MUX Testbench 4/4





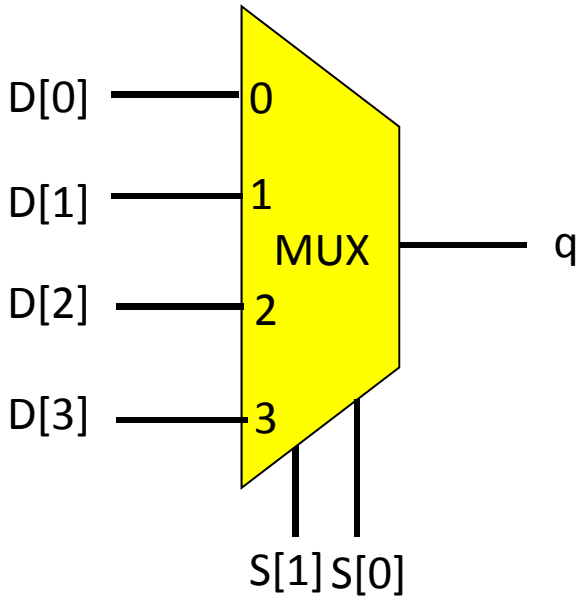
MUX using always block

```
module mux2( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    reg q;
    wire[1:0] select;
    wire[3:0] d;
    always @(d or select)
        q = d[select];
endmodule
```



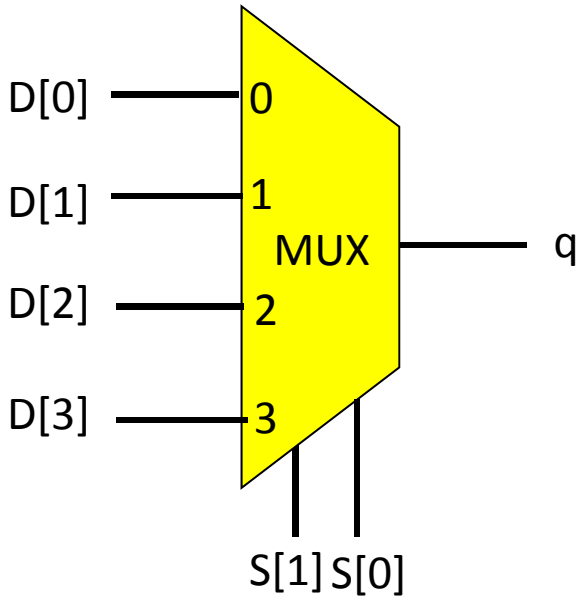
MUX using if statements

```
module mux3( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    reg q;
    wire[1:0] select;
    wire[3:0] d;
    always @( select or d )
    begin
    if( select == 0)
            q = d[0];
    if( select == 1)
            q = d[1];
    if( select == 2)
            q = d[2];
    if( select == 3)
            q = d[3];
    end
endmodule
```



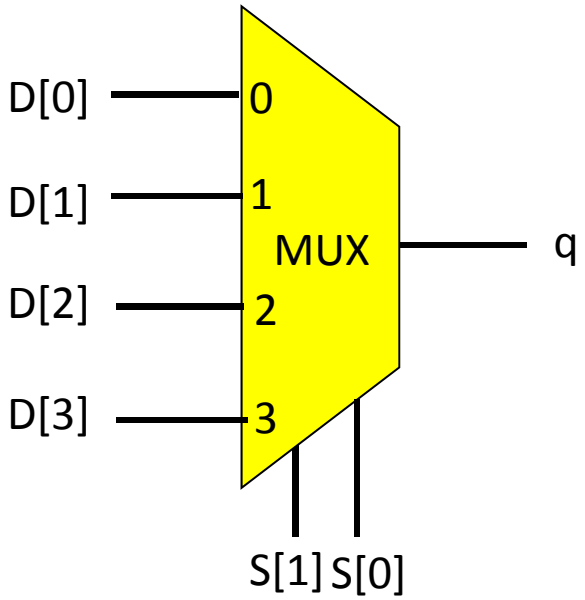
MUX using case statements

```
module mux4( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    reg q;
    wire[1:0] select;
    wire[3:0] d;
    always @( select or d )
    begin
        case( select )
            0 : q = d[0];
            1 : q = d[1];
            2 : q = d[2];
            3 : q = d[3];
        endcase
    end
endmodule
```



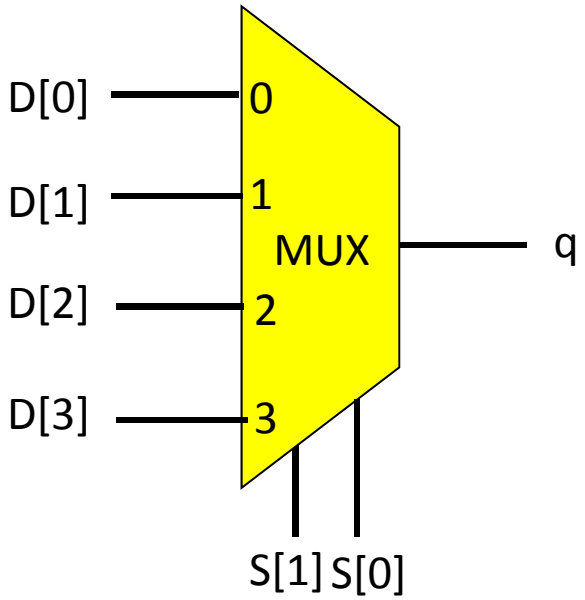
MUX using nested conditional statements

```
module mux5( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    wire q;
    wire[1:0] select;
    wire[3:0] d;
    assign q = ( select == 0 )? d[0] : ( select == 1 )? d[1] : ( select == 2 )? d[2] : d[3];
endmodule
```



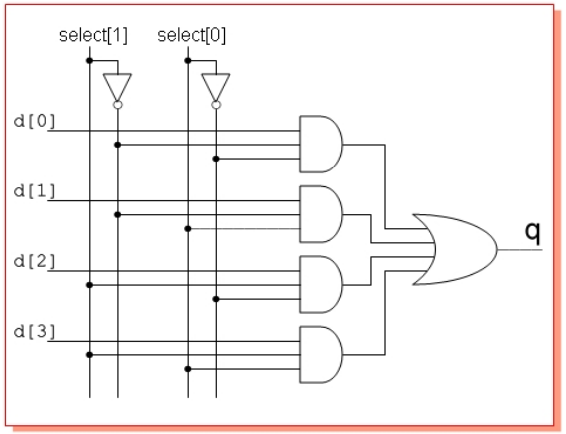
MUX using nested conditional statements

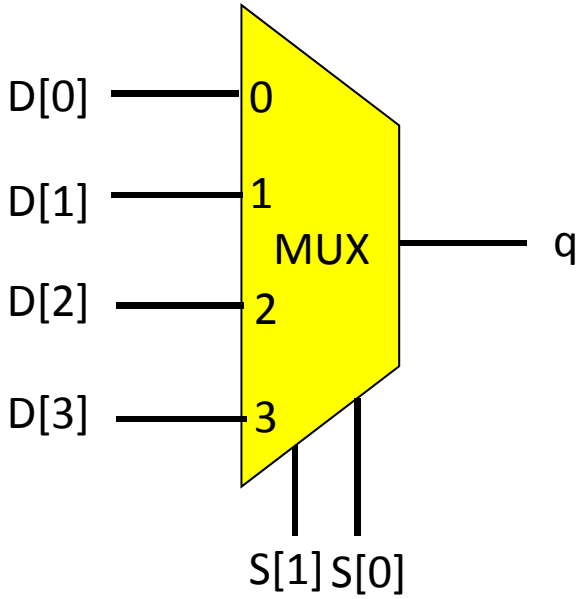
```
module mux6( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    reg q;
    wire[1:0] select;
    wire[3:0] d;
    always @( select or d)
    begin q = ( ~select[0] & ~select[1] & d[0] )
            | ( select[0] & ~select[1] & d[1] )
            | ( ~select[0] & select[1] & d[2] )
            | ( select[0] & select[1] & d[3] );
    end
endmodule
```



MUX using gates

```
module mux7( select, d, q );
    input[1:0] select;
    input[3:0] d;
    output q;
    wire q, q1, q2, q3, q4, NOTselect0, NOTselect1;
    wire[1:0] select;
    wire[3:0] d;
    not n1( NOTselect0, select[0] );
    not n2( NOTselect1, select[1] );
    and a1( q1, NOTselect0, NOTselect1, d[0] );
    and a2( q2, select[0], NOTselect1, d[1] );
    and a3( q3, NOTselect0, select[1], d[2] );
    and a4( q4, select[0], select[1], d[3] );
    or o1( q, q1, q2, q3, q4 );
endmodule
```





DEMUX

```
module demux1(select,d,q);
    input d;
    input [2:0] select;
    output [7:0] q;
    assign q[0] = d & ~select[2] & ~select[1] & ~select[0];
    assign q[1] = d & ~select[2] & ~select[1] &  select[0];
    assign q[2] = d & ~select[2] &  select[1] & ~select[0];
    assign q[3] = d & ~select[2] &  select[1] &  select[0];
    assign q[4] = d &  select[2] & ~select[1] & ~select[0];
    assign q[5] = d &  select[2] & ~select[1] &  select[0];
    assign q[6] = d &  select[2] &  select[1] & ~select[0];
    assign q[7] = d &  select[2] &  select[1] &  select[0];
endmodule
```

DEMUX Testbench 1/3

```
module demux1_tb;
    // Inputs
    reg [2:0] select;
    reg d;
    // Outputs
    wire [7:0] q;
    integer i;
    // Instantiate the Unit Under Test (UUT)
    demux1 uut (
            .select(select),
            .d(d),
            .q(q)
    );
```

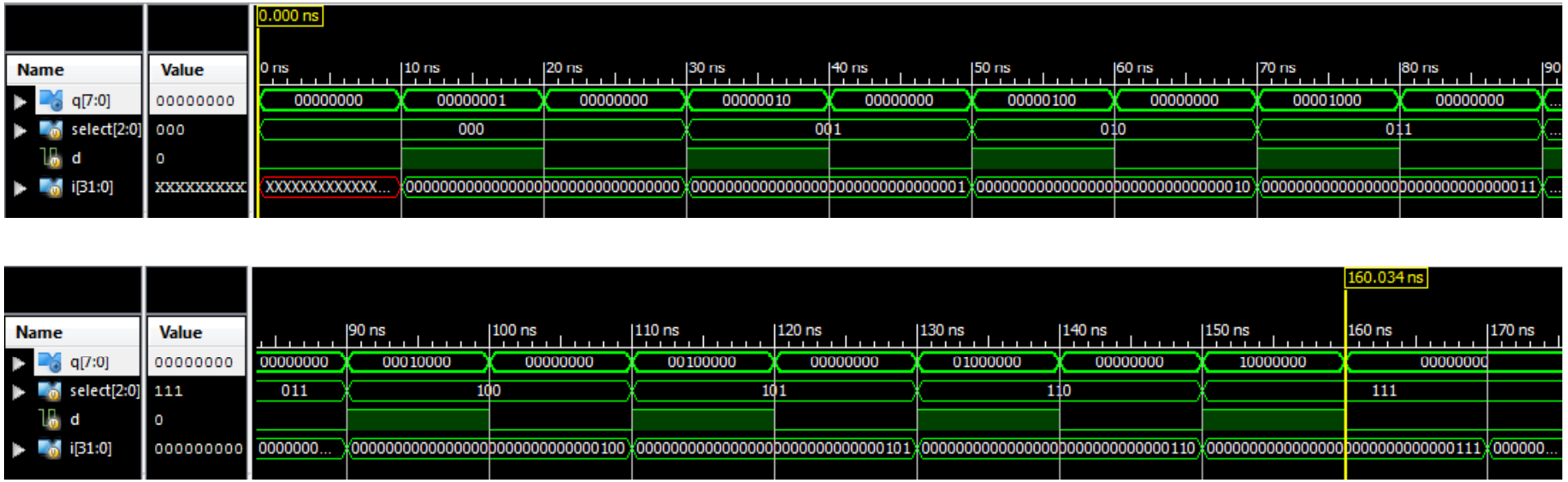
```
initial begin
        // Initialize Inputs
        select = 3'b000;
        d = 0;

        // Wait 100 ns for global reset to finish
        #10;
```

DEMUX Testbench 2/3
Choose left code or right code
Are they the same?

```
        d = 1;select = 3'b000;#10;
        d = 1;select = 3'b001;#10;
        d = 1;select = 3'b010;#10;
        d = 1;select = 3'b011;#10;
        d = 1;select = 3'b100;#10;
        d = 1;select = 3'b101;#10;
        d = 1;select = 3'b110;#10;
        d = 1;select = 3'b111;#10;
        d = 0;select = 3'b000;#10;
    end

endmodule
```

```
        for(i = 0; i <= 7; i = i + 1)
        begin
                select = i;
                d=1;
                #10;
                d=0;
                #10;
        end
    end

endmodule
```

DEMUX Testbench 3/3



Few Notes

- Initial block declares a single-pass behavior
  - Executes once when simulator is activated
- Delay control operator (#) and delay value - #10
- Timescale compiler directive
  - timescale <reference_time_unit>/<time_precision>
  - `timescale 1ns/1ps
- Inputs are declared as reg values – retains value until updated
- Outputs are just monitored as wires

Sequential Logic Implementations

- Generating clock signal
- Single D Flip Flop
- Three D Flip flops in series
- Parallel load shift register

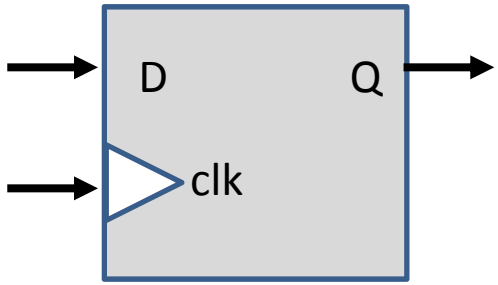
Generating Clock Signal

```
always
   begin
        clk = 0;
        #5;
        clk = 1;
        #5;
   end
```

```
initial begin
    clk = 0;
end

always begin
        #5; clk = 0;
        #5; clk = 1;
end
```

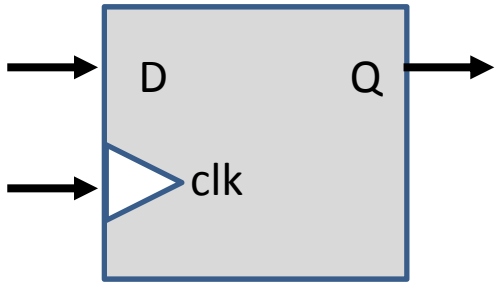
Single D Flip-Flop

```
module single_d_ff(clk,D,Q);
    input clk;
    input D;
    output reg Q;
    always @(posedge clk)
    begin
        Q <= D;
    end
endmodule
```



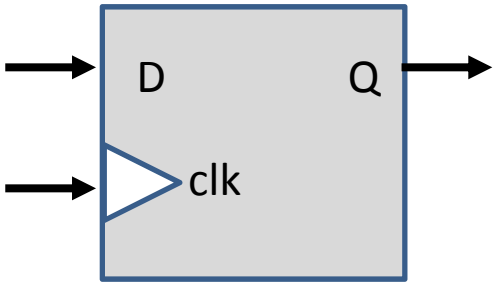
Single D Flip-flop Testbench 1/3

```
module single_d_ff_tb;
    // Inputs
    reg clk;
    reg D;
    // Outputs
    wire Q;
    // Instantiate the Unit Under Test (UUT)
    single_d_ff uut (
            .clk(clk),
            .D(D),
            .Q(Q)
    );
```



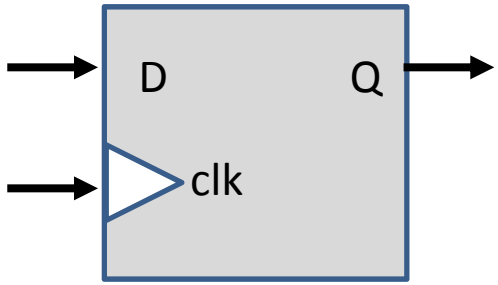
Single D Flip-flop Testbench 2/3

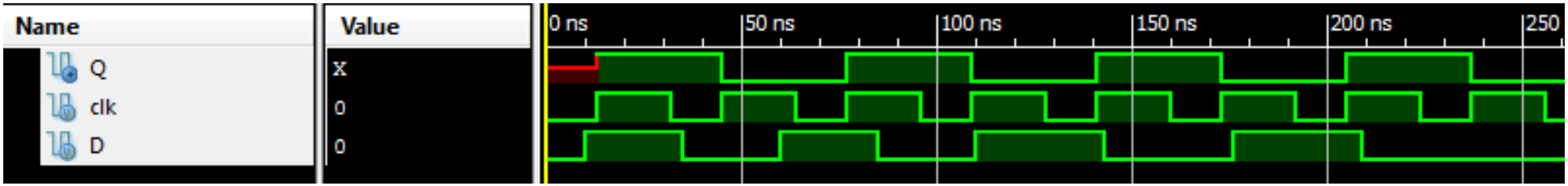
```
initial begin
        // Initialize Inputs
        clk = 0;
        D   = 0;
        // Wait 10 ns for global reset to finish
        #10;
        // Add stimulus here
        D = 1; # 25;
        D = 0; # 25;
        D = 1; # 25;
        D = 0; # 25;
        D = 1; # 33;
        D = 0; # 33;
        D = 1; # 33;
        D = 0; # 33;
end
```

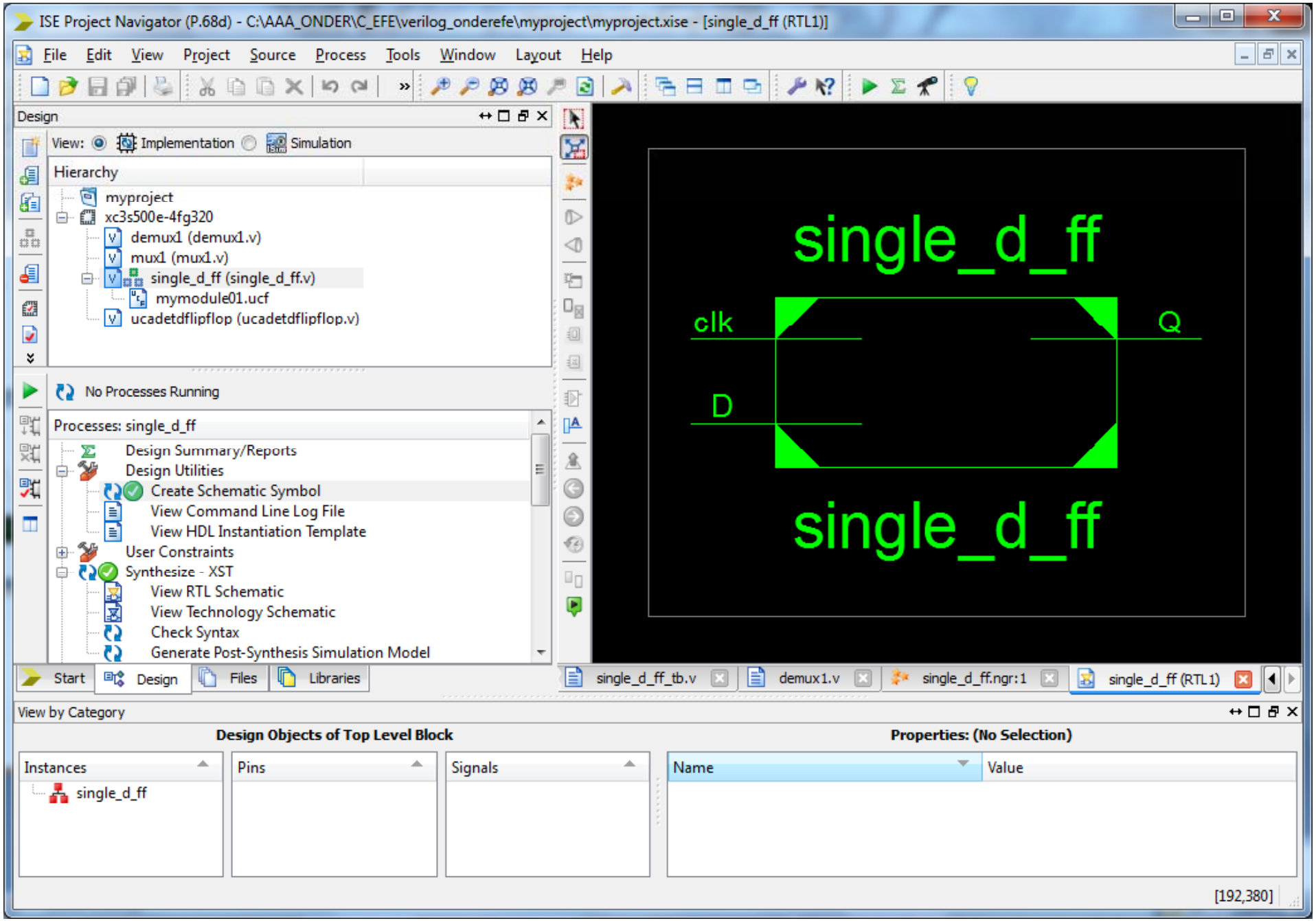


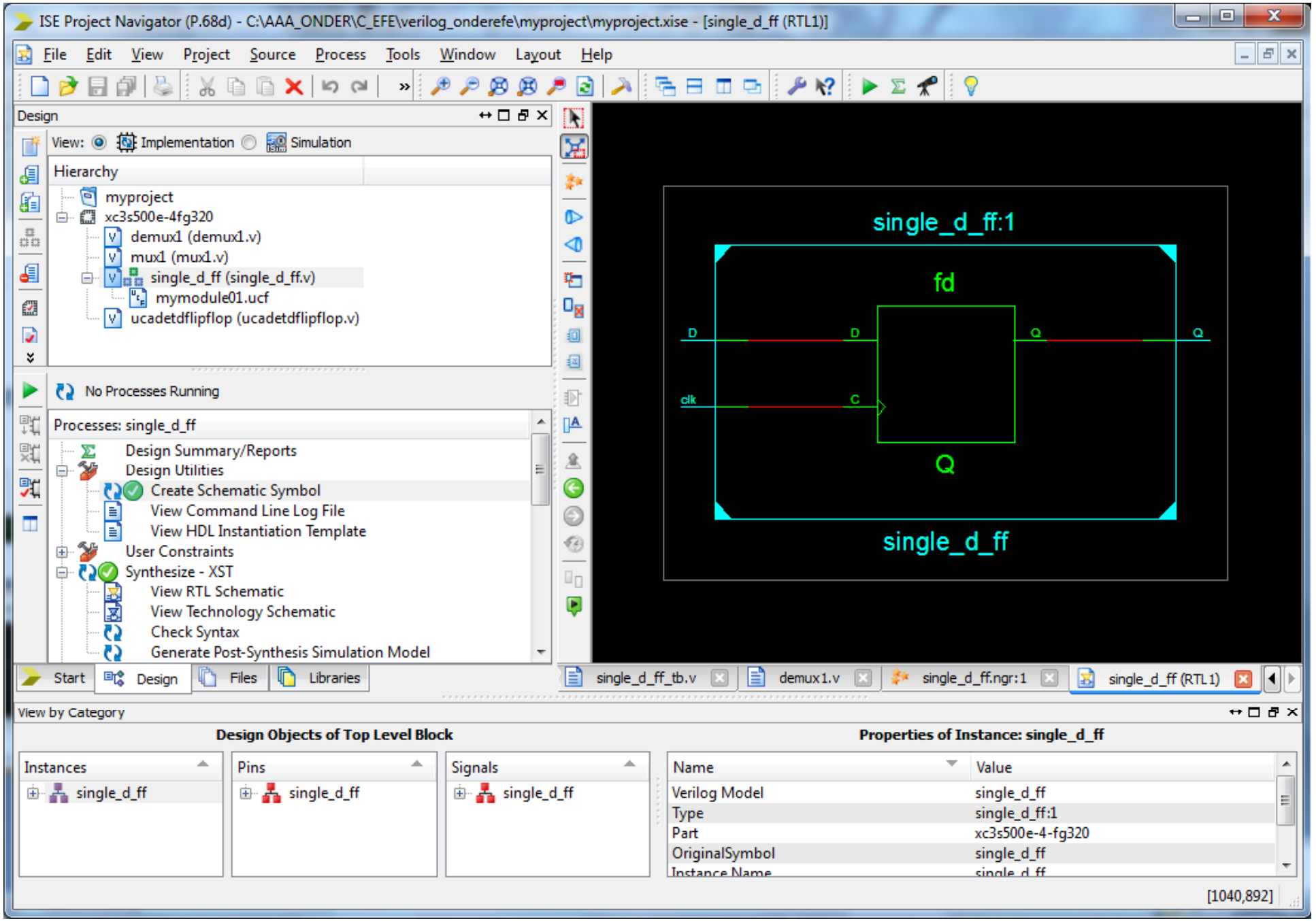
Single D Flip-flop Testbench 3/3

```
always begin
        clk = 0 ; #13;
        clk = 1 ; #19;
end
endmodule
```






ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [single_d_ff (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
myproject
xc3s500e-4fg320
demux1 (demux1.v)
mux1 (mux1.v)
single_d_ff (single_d_ff.v)
mymodule01.ucf
ucadetdflipflop (ucadetdflipflop.v)
No Processes Running
Processes: single_d_ff
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log File
View HDL Instantiation Template
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
single_d_ff
clk
D
Q
single_d_ff
Start Design Files Libraries
single_d_ff_tb.v demux1.v single_d_ff.ngr:1 single_d_ff (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
single_d_ff
[192,380]


ISE Project Navigator (P.68d) - C:\AAA_ONDER\C_EFE\verilog_onderefe\myproject\myproject.xise - [single_d_ff (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
myproject
xc3s500e-4fg320
demux1 (demux1.v)
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mymodule01.ucf
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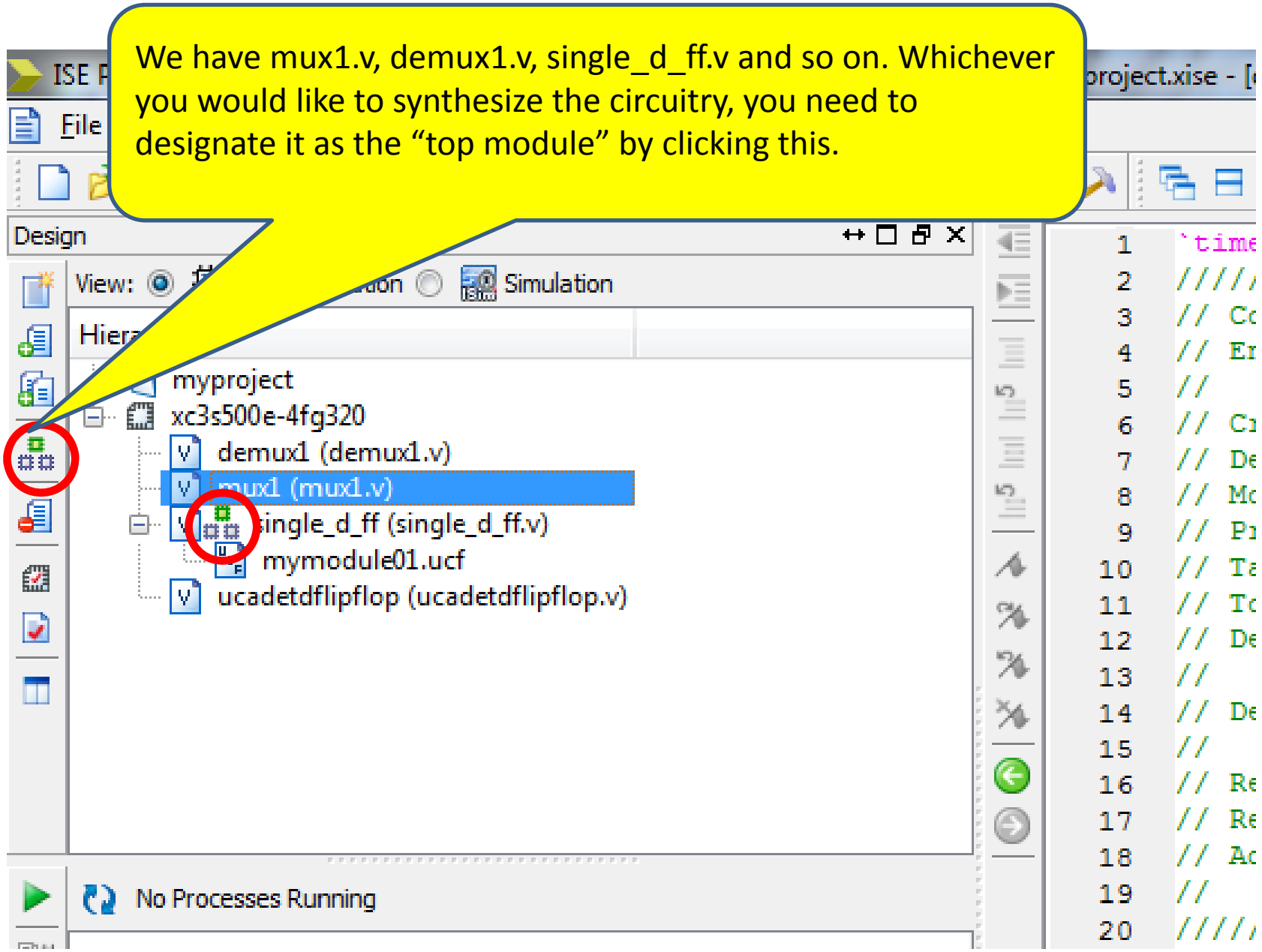
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Start Design Files Libraries
single_d_ff:1
fd
D
D
Q
Q
clk
C
Q
single_d_ff
single_d_ff_tb.v
demux1.v
single_d_ff.ngr:1
single_d_ff (RTL1)
View by Category
Design Objects of Top Level Block
Instances
single_d_ff
Pins
single_d_ff
Signals
single_d_ff
Properties of Instance: single_d_ff
Name
Value
Verilog Model
single_d_ff
Type
single_d_ff:1
Part
xc3s500e-4-fg320
OriginalSymbol
single_d_ff
Instance Name
single_d_ff
[1040,892]


We have mux1.v, demux1.v, single_d_ff.v and so on. Whichever you would like to synthesize the circuitry, you need to designate it as the “top module” by clicking this.
File
Design
View:
Simulation
myproject
xc3s500e-4fg320
demux1 (demux1.v)
mux1 (mux1.v)
single_d_ff (single_d_ff.v)
mymodule01.ucf
ucadetdflipflop (ucadetdflipflop.v)
No Processes Running