Hacettepe University
Computer Engineering Department
BBM341 Systems Programming
2nd Midterm – 18 December 2018

Name : .....

ID No : .....

Section : .....

Question 1. **(20 points)** Assume the following:

- The memory is byte addressable.
- Memory accesses are to **1-byte words** (not to 4-byte words).
- Addresses are 13 bits wide.
- The cache is two-way set associative (E = 2), with a 4-byte block size (B = 4) and eight sets (S = 8).

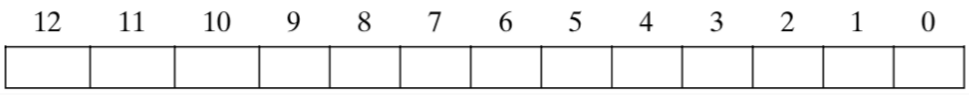
A. The contents of the cache are as follows, with all numbers given in hexadecimal notation.

2-way set associative cache

	Line 0						Line 1					
Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	09	1	86	30	3F	10	00	0	—	—	—	—
1	45	1	60	4F	E0	23	38	1	00	BC	0B	37
2	EB	0	—	—	—	—	0B	0	—	—	—	—
3	06	0	—	—	—	—	32	1	12	08	7B	AD
4	C7	1	06	78	07	C5	05	1	40	67	C2	3B
5	71	1	0B	DE	18	4B	6E	0	—	—	—	—
6	91	1	A0	B7	26	2D	F0	0	—	—	—	—
7	46	0	—	—	—	—	DE	1	12	C0	88	37

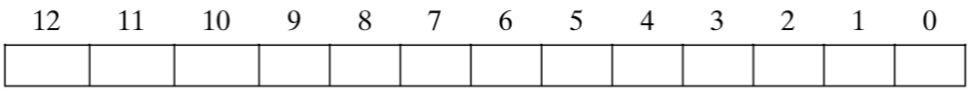
The following figure shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

CO The cache block offset
CI The cache set index
CT The cache tag



Suppose a program running on the machine references the byte at address 0x0E38. Indicate the cache entry accessed and the cache byte value returned **in hex**. Indicate whether a cache miss occurs. If there is a cache miss, enter "–" for "Cache byte returned."

B. Address format (one bit per box):



C. Memory reference:

Parameter	Value
Cache block offset (CO)	0x_____
Cache set index (CI)	0x_____
Cache tag (CT)	0x_____
Cache hit? (Y/N)	_____
Cache byte returned	0x_____

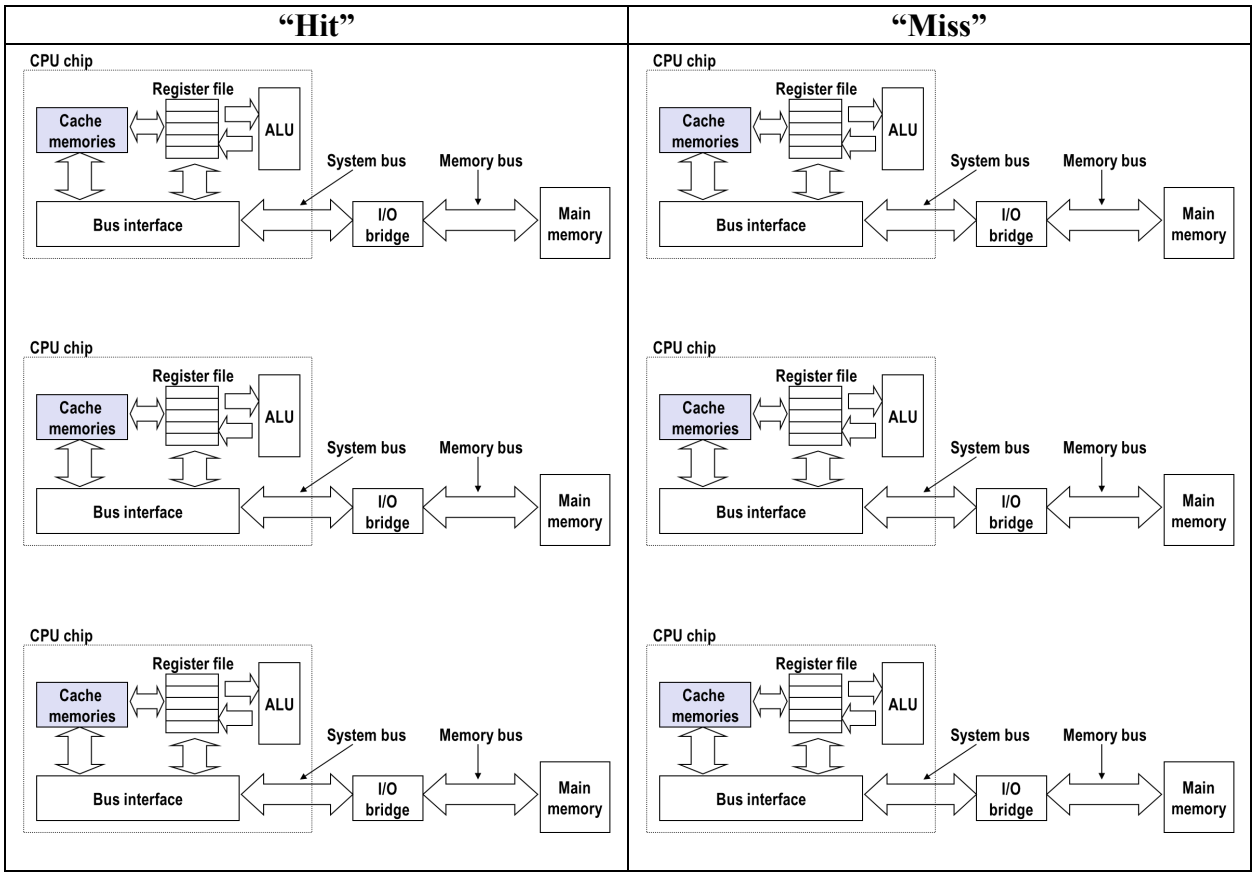
Question 2. (10 points) List the differences between DRAM and SRAM.

Question 3. (10 points) If the hit rate increases from 95% to 100%, how much improvement can be observed in the average access time? Take cache hit time of 1 cycle and miss penalty of 100 cycles.

Question 4. (20 points) For the following matrix multiplication algorithm, explain how the algorithm benefits from Spatial and Temporal Localities. (For both instruction and data references)

```
float A[100][100], B[100][100], C[100][100];
int i, j, k, m, n, p;
...
for (i = 0; i < m; i++)
   for (j = 0; j < n; j++)
      for (k = 0; k < p; k++)
         C[i][j]+= A[i][k] * B[k][j];
...
```

Question 5. (10 points) For **`movl (%edx),%ebx`** instruction, visualize data access steps for both *miss* and *hit* cases. Use arrows to depict dataflow, addressing, entry checks etc., and use keywords such as **check**, **address**, **read** and/or **write** to identify each step.



Question 6. (20 points) Using the following information fill in the content and addressing mode columns in the table below.

Address	Content
0x100	0xFF
0x104	0xAB
0x108	0x13
0x10C	0x11

Register	Content
%eax	0x100
%ecx	0x1
%edx	0x3

Operand	Content	Addressing Mode
%eax	.....	.....
0x104	.....	.....
$0x108	.....	.....
(%eax)	.....	.....
4(%eax)	.....	.....
9(%eax,%edx)	.....	.....
260(%ecx,%edx)	.....	.....
0xFC(,%ecx,4)	.....	.....
(%eax,%edx,4)	.....	.....

Question 7. (10 points) List the differences between SSD and Rotating Disks.