# BBM233 LOGIC DESIGN LAB.

# DESIGN HOMEWORK

# 2017-2018

**Due Date: 20. 01.2018 up to 23:59 via submit page**

*This is not an individual homework. For this homework, study with your assigned lab. group friends. The authorized person is expected to submit the assignment on behalf of the group.*

## Homework Description

Design 4 bit prime number counter with JK flip flop(s). Verify the design on Verilog.

Submit the files that have been described.

1) ***Design report must contain*** :
    a. Truth table of the design
    b. Karnaugh map
    c. Circuit diagram
    d. General description of the design.
    e. Verilog code
2) ***Result of the simulation with screen shots***.
   **IMPORTANT NOTE:** Print out each cycle, contains prime number, to the screen.
3) ***Expected file formats*** :
   .pdf (for report)
   .v
   .tb
   .jpg (for screen shots)