Hacettepe University
Computer Engineering Department
BBM234 Computer Organization

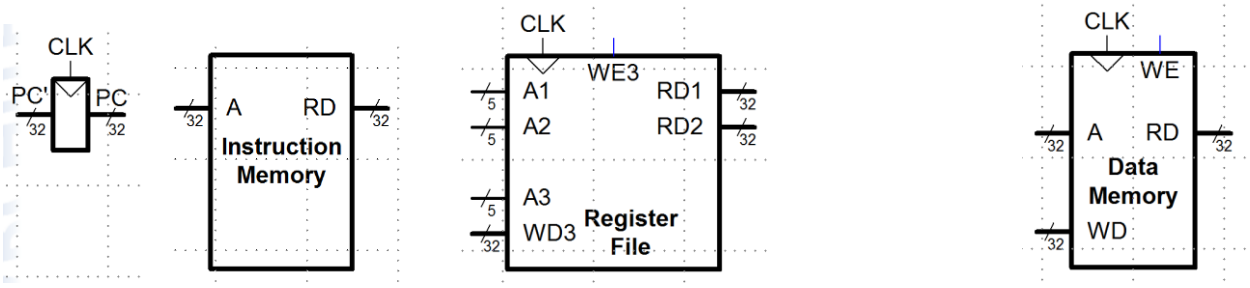
Homework 3

Assigned date : 19.04.2018
Due date : 26.04.2018 (All Sections)

You can bring your homework to the class. Or, you can give them to TA Selma Dilek or slide under my office door. Don't email your homework!
LATE HOMEWORKS WILL NOT BE ACCEPTED…

Questions: (Each one is 20 points.)

Q1. You are given 32-bit Program Counter (PC), instruction memory, register file with 32 registers, and a data memory. First, show the machine code fields (instruction format) of the **addi** instruction. Then, draw the data-path of the **addi** for the single-cycle processor by using the following units and adding new hardware. Show your extra equipment and what bits are connected to which inputs of the components.



Q2. We would like to add bne instruction to the single cycle architecture given below. bne instruction is a branch instruction and it loads branch target address (BTA) to the PC (PC=BTA) if [rs] != [rt].

a) Show the necessary changes on the data-path in Figure 1 and explain your changes. Your new architecture should be able to execute both beq and bne instructions. [12]

b) Fill the control signals in Table I. Add new control signal/signals to the table if necessary. [8]

a)

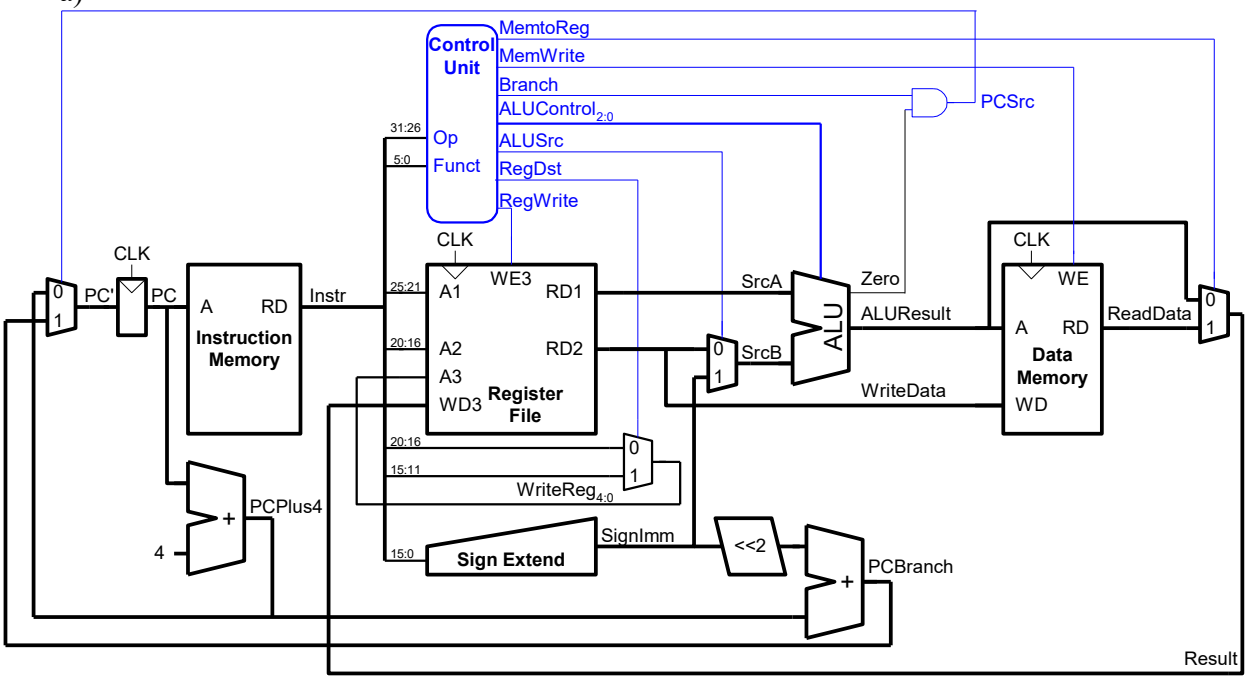


Figure 1: Single cycle processor

b)

Table I: **bne** control signals

Inst.	$Op_{31:26}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$
bne	000101							

Q3. You are given the following MIPS code. You have 5 stage pipelined MIPS processor running the code. Assume processors can flush the instructions after the branch is resolved.

a) If there is no forwarding and early branch resolution in the MIPS processor, **insert enough NOPs between the instructions** to have correct execution of the code.
   i. How many cycles does it take to execute all instructions if the branch is not taken?
   ii. How many cycles does it take to execute all instructions if the branch is taken? Show your calculations or explain how you found the cycle time.

 # MIPS assembly code

```
        lw  $s0, 0($0)

        lw  $s1, 4($0)

        beq $s0, $s1, L

        add $t0, $t0, $s0

        add $t1, $t1, $s1

        add $t2, $t0, $t1

    L:  addi $t2, $t2, 1
```

b) If there is a hazard unit (data forwarding and early branch resolution hardware) in the MIPS processor, insert enough NOPs between the instructions to have correct execution of the code.
   i. How many cycles does it take to execute all instructions if the branch is not taken?
   ii. How many cycles does it take to execute all instructions if the branch is taken? Show your calculations or explain how you found the cycle time.

 # MIPS assembly code

```
        lw  $s0, 0($0)

        lw  $s1, 4($0)

        beq $s0, $s1, L

        add $t0, $t0, $s0

        add $t1, $t1, $s1

        add $t2, $t0, $t1

    L:  addi $t2, $t2, 1
```

Q4. You are given the following MIPS code. You have 5 stage pipelined MIPS processor running the code.

a) If there is no forwarding unit in the MIPS processor, **insert enough nop's between the instructions** to have correct execution of the code. How many cycles does it take to execute all instructions? Show your calculations or explain how you found the cycle time.

 # MIPS assembly code

```
lw  $s0, 0($0)

lw  $s1, 4($0)

add $t0, $s0, $s1

or $t1, $s2, $s3

and $t1, $t1, $t0
```

b) If there is a forwarding unit in the MIPS processor, insert enough nop's between the instructions to have correct execution of the code. How many cycles does it take to execute all instructions? Show your calculations or explain how you found the cycle time.

c) If there is a forwarding unit in the MIPS processor, rearrange the code if possible to minimize the clock cycles and your code still executes correctly. How many cycles does it take to execute all instructions? Show your calculations or explain how you found the cycle time.

Q5. The distribution of the instructions for the program with one billion (10^9) instructions is given below.

%40 load, %10 store, %10 branch, %10 jump, %30 R-type

Suppose

- %50 load instruction results are used by the next instruction.
- %50 R-type instruction results are used by the next instruction.
- 50% branches are taken.
- All jumps flush the next instruction.

a) How many clock cycles does this program take in a single cycle MIPS processor?

b) How many clock cycles does it take on a pipelined MIPS processor with no hazard unit (no forwarding and no early branch resolution)?

c) How many clock cycles does it take on a pipelined MIPS processor with hazard unit (with forwarding and early branch resolution)?