HACETTEPE UNIVERSITY

DEPARTMENT OF COMPUTER ENGINEERING

BBM231 LOGIC DESIGN

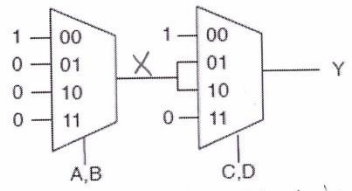
Homework 3 (For all sections)

Assigned : 26.11.2018

Due : 03.12.2018

A1.

a) Give the minimum boolean function for output Y for the circuit given below.
b) Implement Y with 8x1 MUX and inverters.

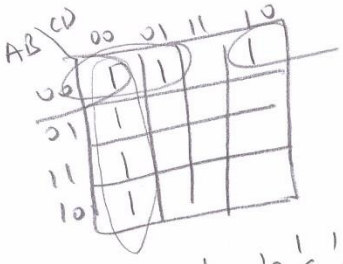


when CD=00 ⇒ y=1
CD=01 ⇒ y=X
CD=10 ⇒ y=X
CD=11 ⇒ y=0

(a)

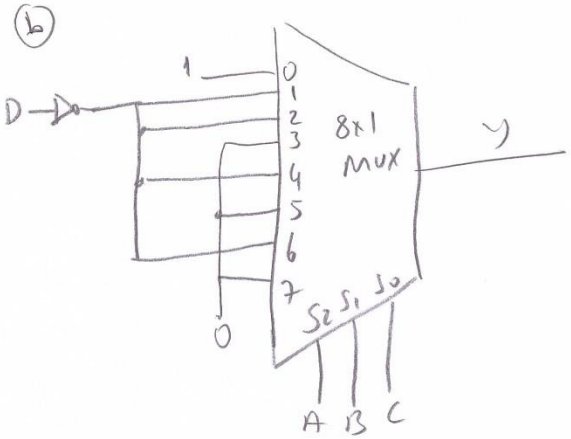
A	B	C	D	X	y	
0	0	0	0	1	1	F=1
0	0	0	1	1	1	
0	0	1	0	1	1	F=D'
0	0	1	1	1	0	
0	1	0	0	0	1	F=D'
0	1	0	1	0	0	
0	1	1	0	0	0	F=0
0	1	1	1	0	0	
1	0	0	0	0	1	F=D'
1	0	0	1	0	0	
1	0	1	0	0	0	F=0
1	0	1	1	0	0	
1	1	0	0	0	1	F=D'
1	1	0	1	0	0	
1	1	1	0	0	0	F=0
1	1	1	1	0	0	

b şıkkı için



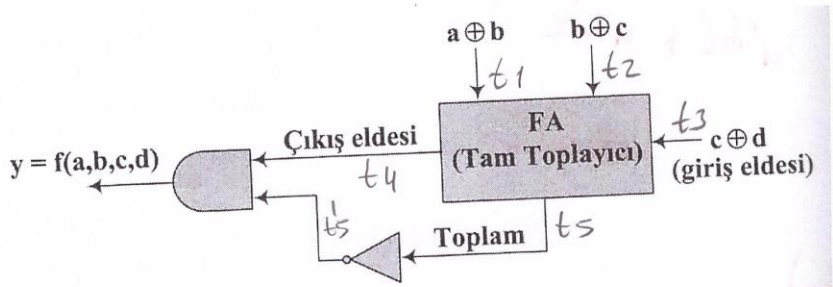
$y = C'D' + A'B'C' + A'B'D'$

(b)



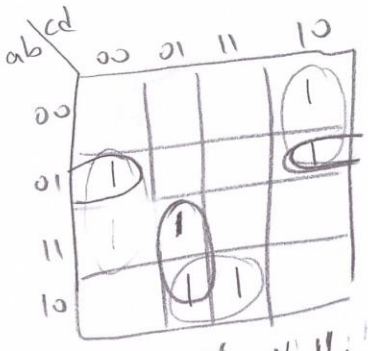
A2.

a) Determine the output function **y** for the following circuit.
b) Implement it using two 3x8 decoders with Enable signal, an inverter and OR gate.



a)

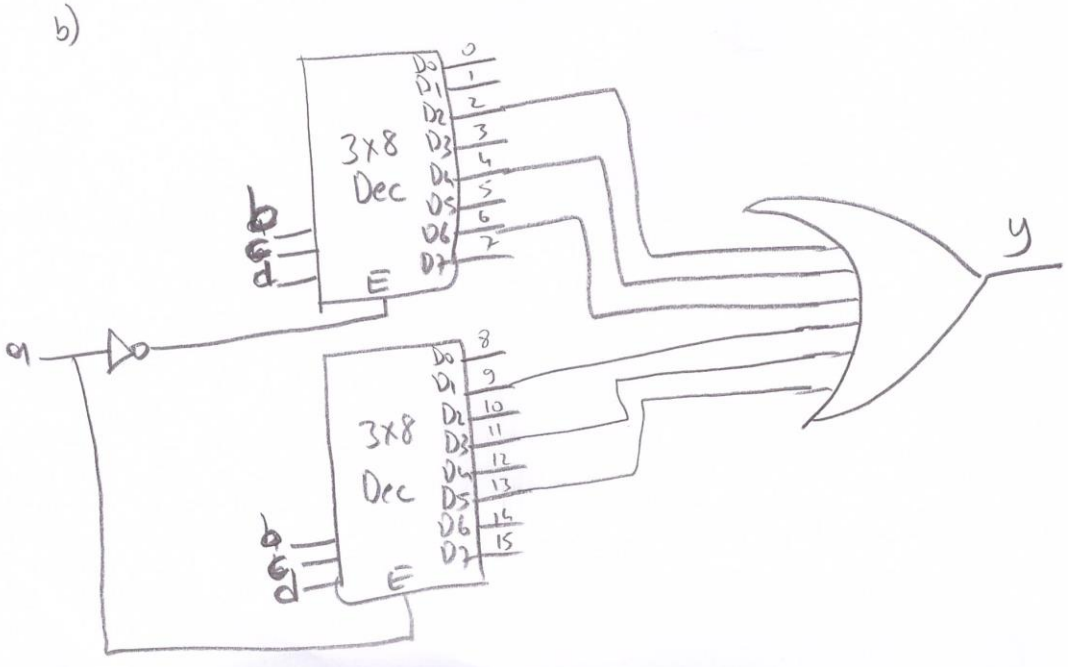
a	b	c	d	t_1	t_2	t_3	t_4	t_5	t_5'	y
0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	1	0	0
0	0	1	0	0	1	1	1	0	1	1
0	0	1	1	0	1	0	0	1	0	0
0	1	0	0	1	1	0	1	0	1	1
0	1	0	1	1	1	1	1	1	0	0
0	1	1	0	1	0	1	1	0	1	1
0	1	1	1	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0	0
1	0	0	1	1	0	1	1	0	1	1
1	0	1	0	1	1	1	1	1	0	0
1	0	1	1	1	1	0	1	0	1	1
1	1	0	0	0	1	0	0	1	0	0
1	1	0	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	0	1	0	0
1	1	1	1	0	0	0	0	0	1	0



$y = a'cd' + a'bd' + ac'd + ab'd$

$y = \Sigma(2,4,6,9,11,13)$

b)

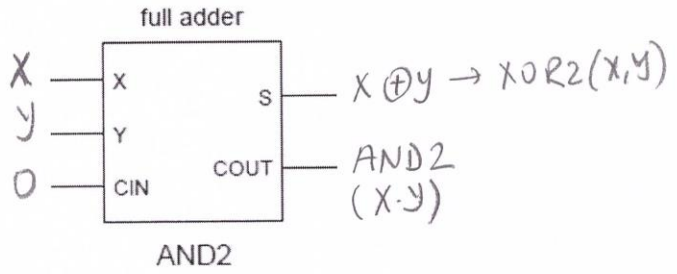


A3.

Full adders are complete. Full adders form a complete set of logic gates; that is, every Boolean function can be implemented using only full adders.

a. Wire each of the full adders below to produce the specified logic function (AND2, OR2, and NOT). In each case, only one output of the full adder is used. The full adder inputs may be connected to primary input signals or to constant values 0 or 1.

b. In each case, the "unused" output of the full adder is a Boolean function. Write next to that output pin the name or formula for this bonus output.



$C_{OUT} = XY + X C_{IN} + Y C_{IN}$

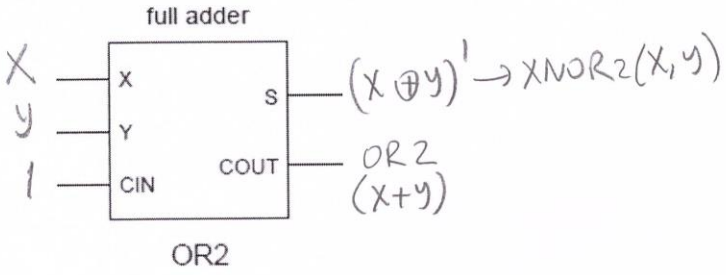
$C_{IN}=0 \Rightarrow$

$C_{OUT} = XY$

$S = X \oplus Y \oplus C_{IN}$

$C_{IN}=0 \Rightarrow$

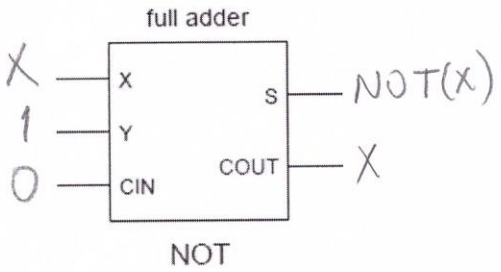
$S = X \oplus Y$



$C_{IN} = 1 \Rightarrow$

$C_{OUT} = XY + X + Y = X + Y$

$S = X \oplus Y \oplus 1 = (X \oplus Y)'$



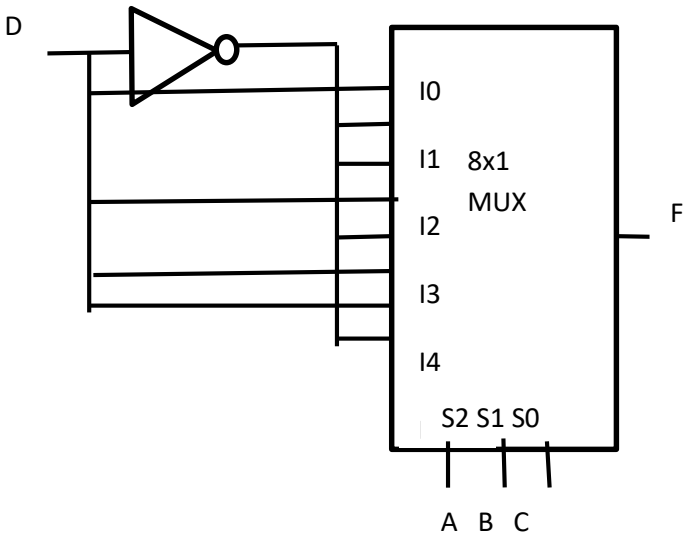
$y = 1$ and $C_{IN}=0 \Rightarrow$

$C_{OUT} = X \cdot 1 + X \cdot 0 + X \cdot 0 = X$

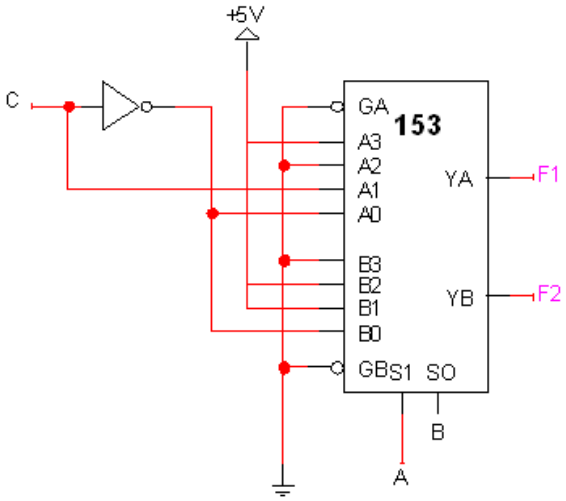
$S = X \oplus 1 \oplus 0 = X \oplus 1 = X'$

A4. Using only one 8X1 MUX and one inverter (NOT gate), design a 4-bit even parity generator.

A	B	C	D	P	P
0	0	0	0	0	P=D
0	0	0	1	1	I0
0	0	1	0	1	P=D’
0	0	1	1	0	I1
0	1	0	0	1	P=D’
0	1	0	1	0	I2
0	1	1	0	0	P=D
0	1	1	1	1	I3
1	0	0	0	1	P=D’
1	0	0	1	0	I4
1	0	1	0	0	P=D
1	0	1	1	1	I5
1	1	0	0	0	P=D
1	1	0	1	1	I6
1	1	1	0	1	P=D’
1	1	1	1	0	I7



A5. 74LS153 is a dual 4x1 multiplexer that consists of two 4x1 multiplexer in it. It has two selection lines S1 and S0. For example, when S1S0=00, outputs YA=A0 and YB=B0. The figure at right shows an implementation for two functions F1 and F2. The inputs to the circuit are ABC.



a. Find the functions F1 and F2 using K-maps.

b. Implement the functions using 3x8 decoder and additional gates.

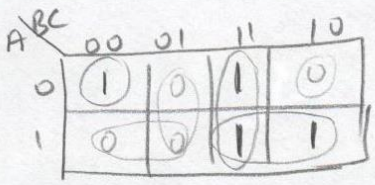
a)

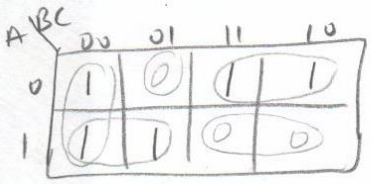
For F1:

A	B	C	F1	
0	0	0	1	$F1=C'$
0	0	1	0	
0	1	0	0	$F1=C$
0	1	1	1	
1	0	0	0	$F1=0$
1	0	1	0	
1	1	0	1	$F1=1$
1	1	1	1	

For F2

A	B	C	F2	
0	0	0	1	$F2=C'$
0	0	1	0	
0	1	0	1	$F2=1$
0	1	1	1	
1	0	0	1	$F2=1$
1	0	1	1	
1	1	0	0	$F2=0$
1	1	1	0	





$F_1 = AB + BC + A'B'C'$

$F_1 = (AB' + B'C + A'BC')'$

$F_2 = B'C' + AB' + A'B$

$F_2 = (AB + A'B'C)'$