2017 - BIL231 LOGIC DESIGN LECTURE VERILOG PROJECT

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Subject	FSM design with Verilog
Development Environment	Verilog HDL IDE , iverilog-gtkwave
Programming Language	Verilog
Start Date	18th December 2017
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1. Introduction

In this assignment, you will design a counter that counts as 1-8-3-21-16 as long as the clock hit, and you will implement the counter using the verilog language.

In your homework, you use the finite state machines; you are expected to define and construct the desired counter structure as a finite state machine.

1.1.Finite State Machines

Finite state machines (FSM) are mathematical models which are used to design computer programs and digital circuits. The FSM contains a finite number of state clusters describing the states they can perform and they can be in only one state in a certain time [1].

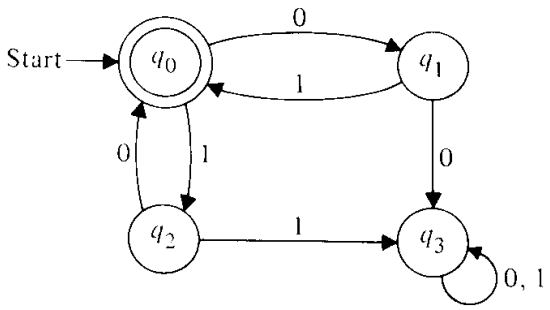

Figure. 1: Finite State Machine

On finite state machines; As a result of the events, transitions occur between the states of the machine. Those transitions depends on the machine model and they are described by the state transition table. The FSM shown in Fig. 1 contains the states {q0, q1, q2, q3} and for example, this machine changes its state to q0 when event 1 occurs while in state q1.

1.2.Finite State Machine Structure

FSM generally consists of three basic structures: combinational logic, sequential logic and output logic [2]. The combinational logic determines what the next state will be by using the state and / or inputs in that state. Sequential logic SDM keeps the current state. The output logic determines what the outputs will be. The output logic may include both combinatorial and sequential logic structures. But it is usually designed in a combinational structure. The generalized FSM structure is shown in Fig.2

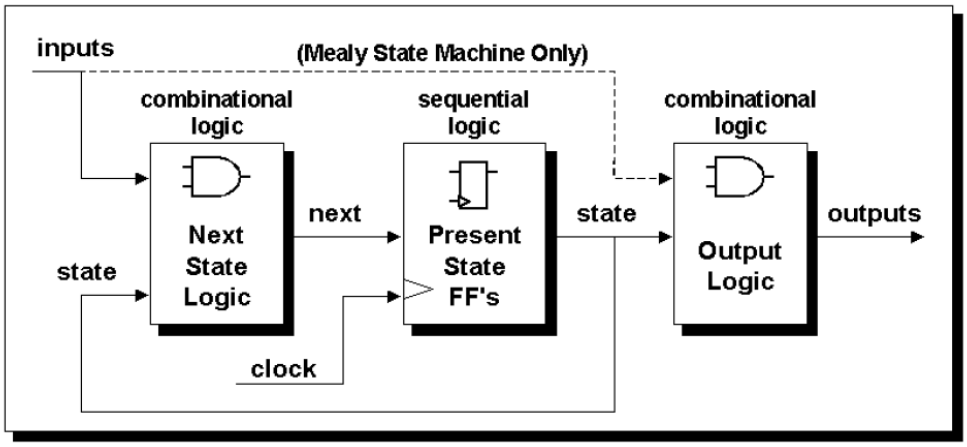

Fig. 2: The generalized FSM structure [2]

1.3. Finite state machine types

FSM is divided into two different types: Mealy and Moore machines. In Moore machines, the next situation only on the current situation. In Mealy machines, the next state depends on the current situation and the inputs. The generalized construction of Mealy and Moore machines is shown in Figure 3.

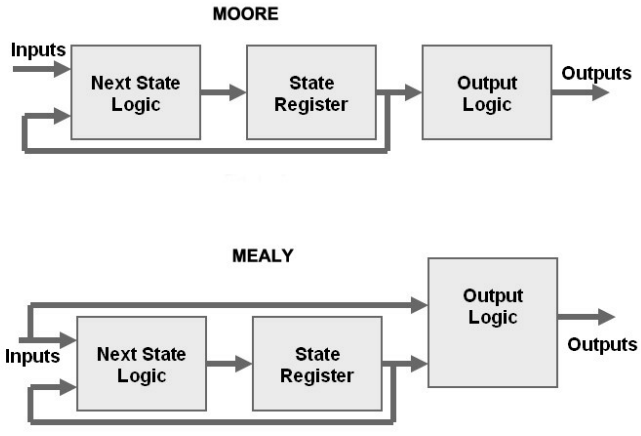

Fig. 3: Mealy ve Moore Machines

2. Problem

In this project, you are expected to design and implement a counter that counts in order of "1-8-3-21-16". The counter works synchronously and it passes to next counter value on at the falling edge of clock pulse. The counter counts continuously; When counting forward, it returns to 1 after 16, and it returns 16 after 1 while it counts backward.

The desired counter structure is shown in Fig-4. The counter has 3 inputs and 1 output port. Counter mode input determines which direction the counter will count. When the counter modeinput is 0, the counter is counting forward and while 1 the counter will count clockwise. Therefore, when mode input is 0, counter will count as "1-8-3-21-16"; and while the mode input is 1 it will count as "16-21-3-8-1". Mode changes can occur can occur at any time counter instantly. For example, if the counter is pulled from 0 to 1 while the counter is at value 3, the counter will return to the value of 8 in the next clock pulse and will advance backward.

The reset input returns the counter to its initial state. At the next falling edge of the clock after the reset is set, the counter will return to state 1 again and continue counting by counter direction.

The counter value output is a 5-bit gate that shows the current value of the counter.

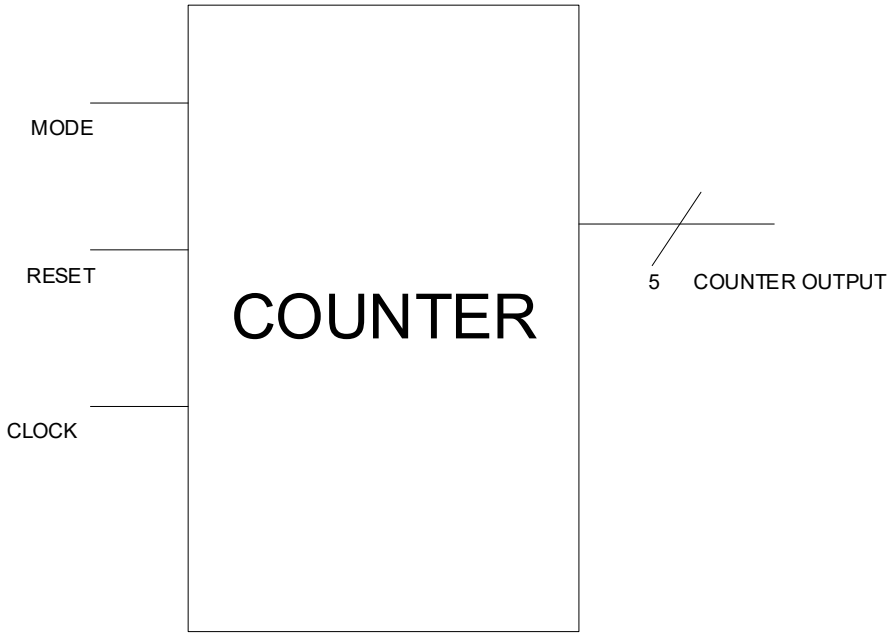

Figure. 4: Counter structure

3. Uyarılar

- **In the project, it is forbidden to use any library or function of Verilog, except for if, always and assign blocks and binary level functions**
- Save all your work until the experiment is graded.
- All codes downloaded from the Internet or shared among students will be considered as CHEAT.
- The assignment must be original, INDIVIDUAL work. All codes downloaded from the Internet or shared source codes will be considered as cheating. Also the students who share their works will be punished in the same way.
- You can ask your questions via piazza class group http://piazza.com/hacettepe.edu.tr/fall2017/bbm231/home. Discussion of the solution on the newsgroups will be considered “group work”, which means “cheating”.
- You are expected to follow the course’s group and you will be held responsible for the announcements made there.
- Cheaters will not be tolerated.

References

1. Finite State Machines, Wikipedia, http://en.wikipedia.org/wiki/Finite-state_machine
2. Clifford E. Cummings, The Fundamentals of Efficient Synthesizable Finite State Machine Design using NC-Verilog and BuildGates