CASPER

CS773-2022-Autumn: Computer Architecture for Performance and Security

Lecture 9: CAOS (friends forever)

https://www.cse.iitb.ac.in/~biswa/


ON SILENT MODE PLEASE

Operating System and Architecture: Bandish 101

Case 1: Programmer wants to run 100 things

CPU says I am alone ☹

OS says I can create an illusion of multiple CPUs ☺

Case 2: Programmer wants 100s of GBs of data

Memory says I am just 10 GB ☹

OS says, never mind, I can create an illusion of TBs ☺

Operating System and Architecture: Bandish 101

Case 3: Programmer wants protection/security of data

OS says I can do it but need your support ☹

CPU says sure ☺

Case 4: Programmer wants parallelism

OS says, why not ☺ but the cost of parallelism ☹

CPU says I will take care by providing instructions ☺

Operating System and Architecture: Bandish 101

Case 5: OS needs clflush, why?

User needs clflush, why?

CPU says sure, why not? ☺

From a program to a process

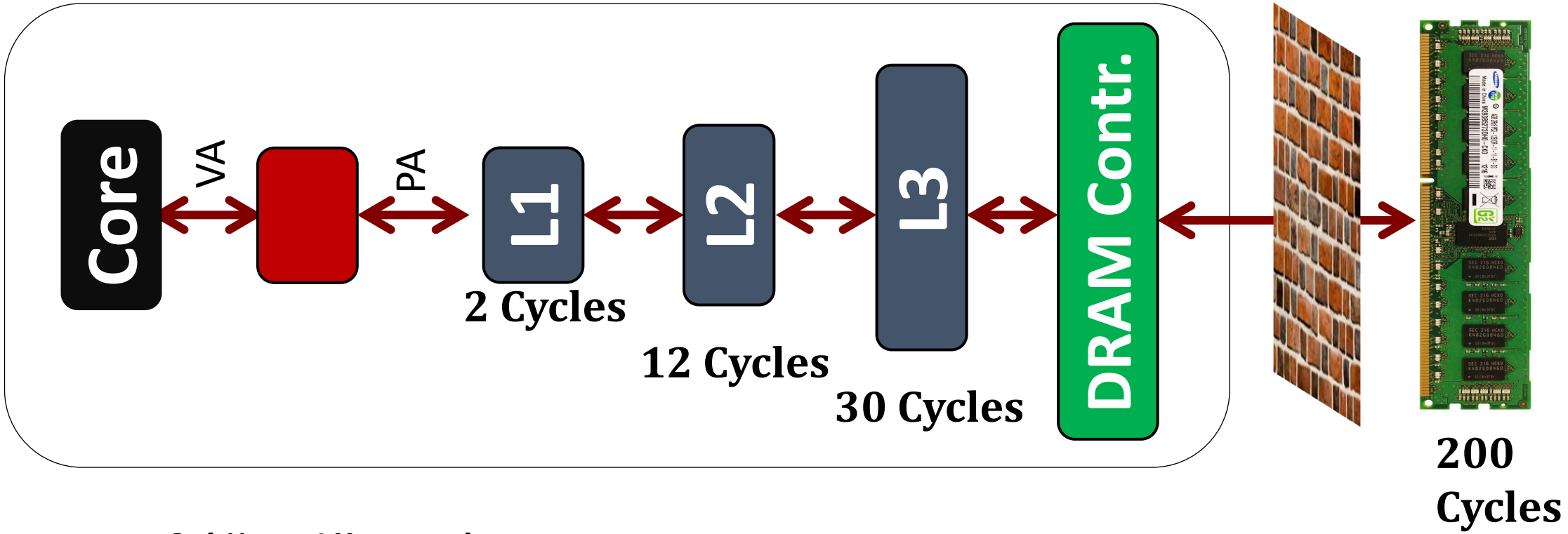
Process: A program that is alive and not-dead (running, waiting ..) ☺

OS creates, manages, schedules them

Allocates memory and initialize CPU state (PC) to kickstart

OS can run multiple processes concurrently even on a single core

Virtual World: Illusion



Printf (“%d”, &a);

Virtual address

Virtual Memory

App. 1

Virtual address space

Printf (“%d”, &a);

App. 2

Virtual address space

Printf (“%d”, &a);

A bit of detour towards OS: Paging

Memory space divided into pages.
Typical page size: 4KB
Huge page: 2MB, 1GB pages

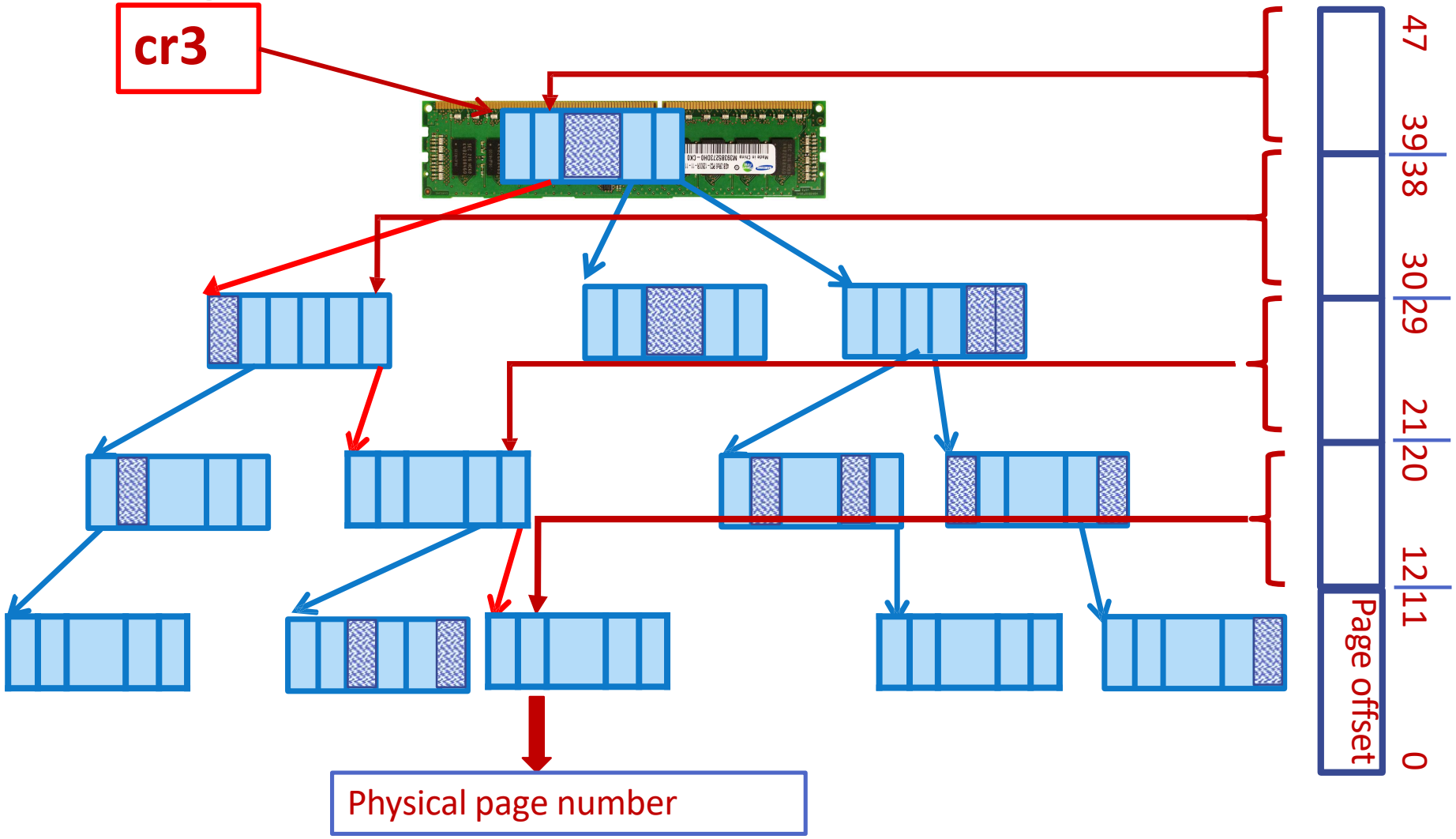
A software table that stores the paging information: Page table

An entry in the page table is known as page-table entry (PTE)

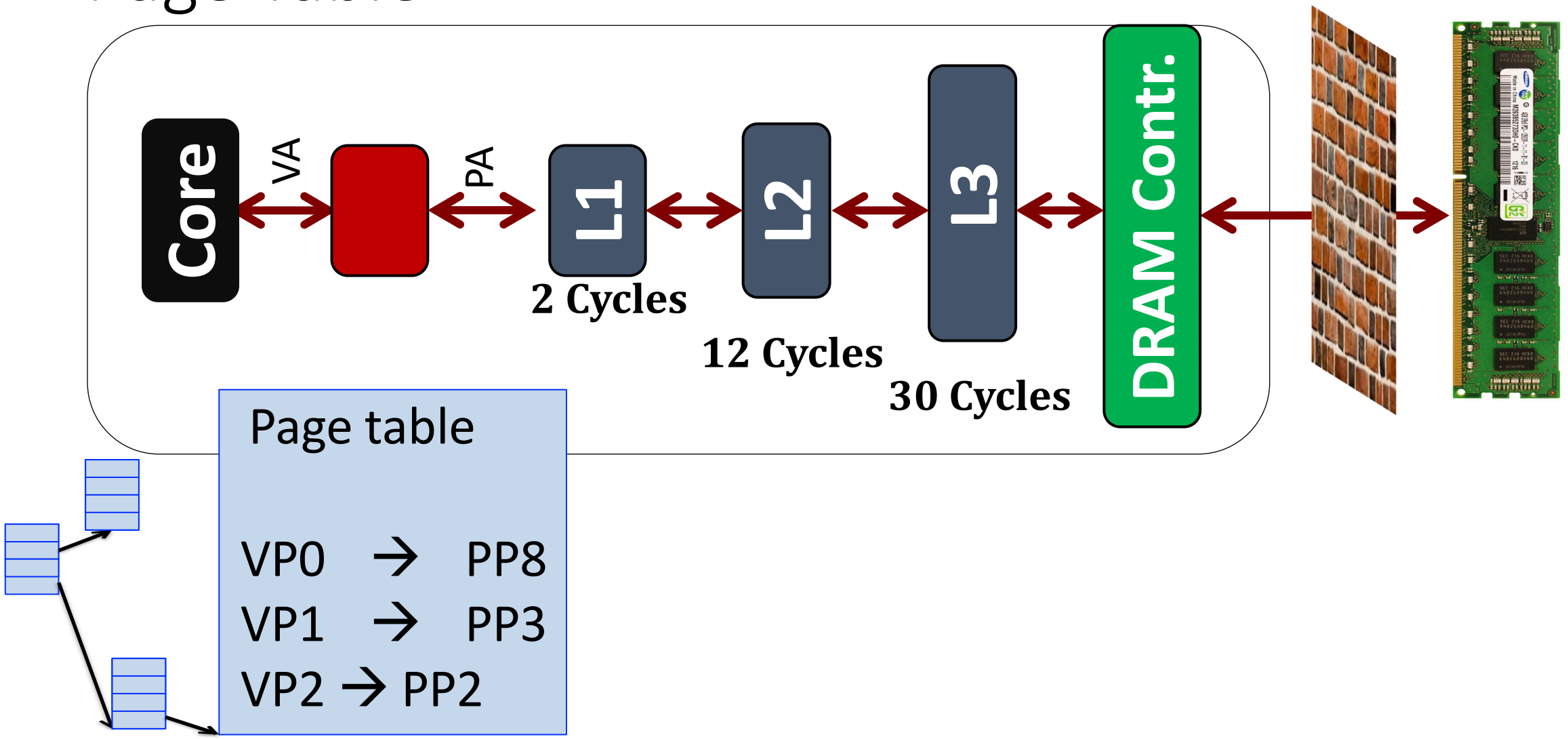
Per process page table (stored in memory)

Virtual page	Physical page

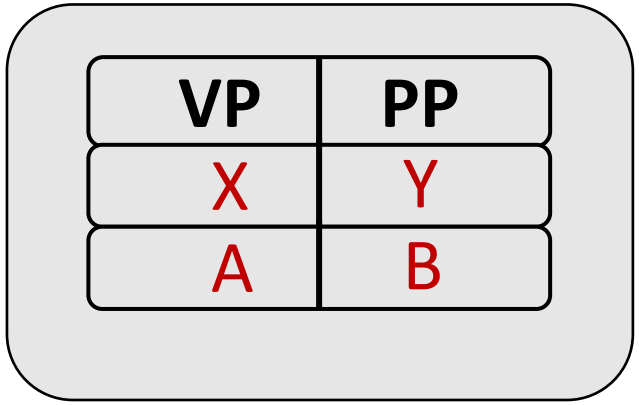
Page Table Walk



Page Table

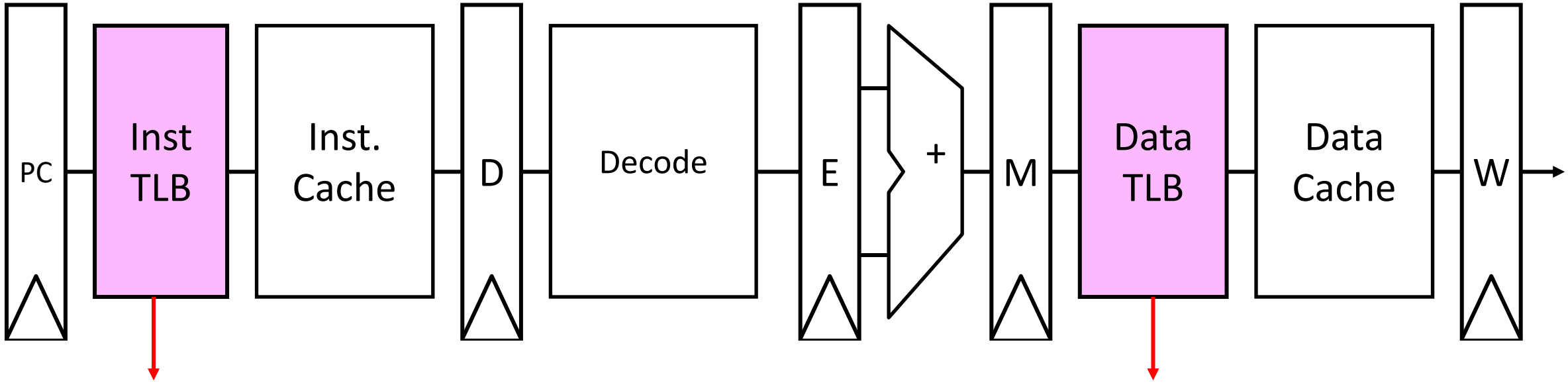

Core
VA
PA
L1
2 Cycles
L2
12 Cycles
L3
30 Cycles
DRAM Contr.
Page table
VP0 → PP8
VP1 → PP3
VP2 → PP2

Can We Cache Translations too?



Translation Look-aside Buffers (TLBs)

The Processor Pipeline with the TLBs

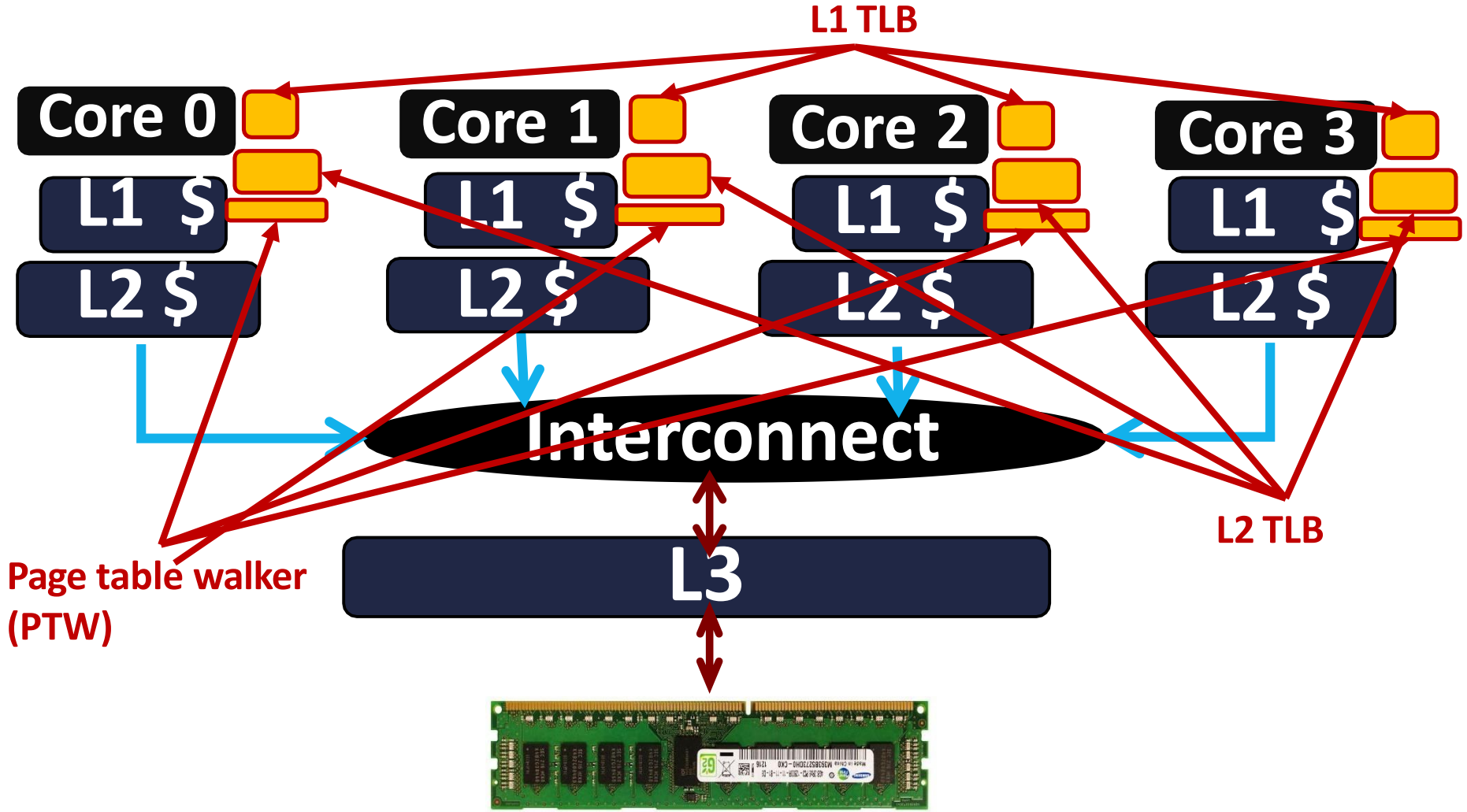


TLB miss? Page Fault?
Protection violation?

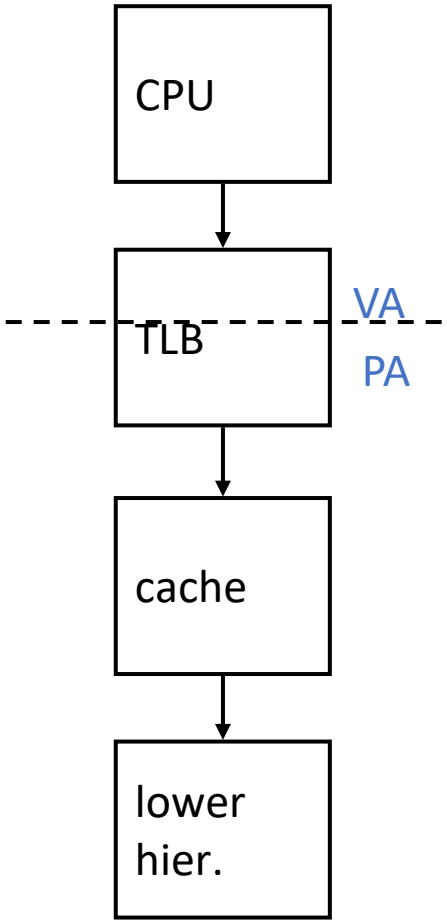
TLB miss? Page Fault?
Protection violation?

Memory Hierarchy with the TLBs

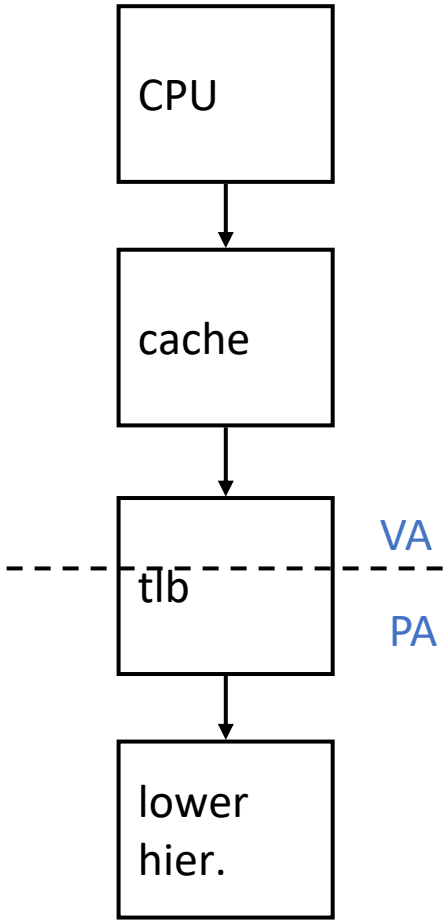
There are Page Walker Caches (PWCs) too ☺



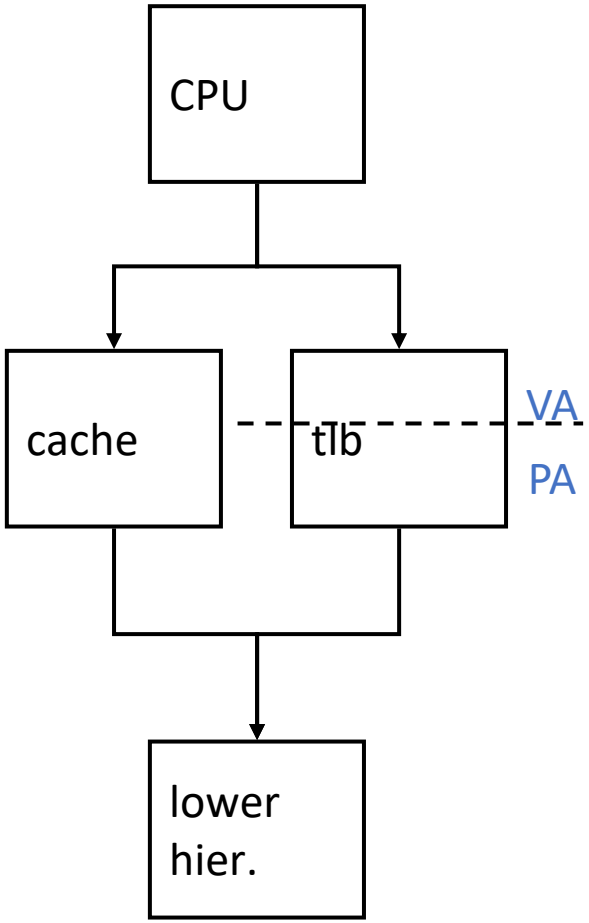
Caches: Virtual or Physical



physical cache



virtual (L1) cache



virtual-physical cache