MOSFET

MosFET Losses

The losses in a switching MosFET are due to

- Conduction losses
  - Losses due to on-state resistance/Rds-on losses
- Switching losses
  - Losses due to output capacitor/Coss losses
  - Turn on losses
  - Turn off losses
  - Gate losses – Gate charge losses and losses on the internal gate resistor

The equations regarding the above losses are expressed below

$$P_{mos} = P_{cond} + P_{sw}$$

Where,

$$P_{sw} = P_{Coss} + P_{on} + P_{off} + P_G$$

Rdson losses

The conduction loss in a MosFET is due to drain to source on-state resistance. Rdson depends upon the gate to source voltage and the junction temperature. In the datasheet of a MosFET, there will be two graphs indicating the variation of Rdson, one with respect to gate-source voltage and drain current, another one with respect to junction temperature.

From the first curve, find the Rdson corresponding to the maximum drain current (RMS) and Vgs or find the multiplier if the curve gives normalized values. Multiply with the maximum Rdson given in table to obtain the actual value.

From the Rdson vs junction temperature curve, find the Rdson or multiplier corresponding to a junction temperature of 75°C or higher as per the maximum external ambient temperature. If the ambient is above 50°C, select the Rdson multiplier corresponding to 125°C og junction temperature. Find the Rdson_hot by multiplying the Rdson obtained from the first curve or table value

The Rdson losses can be found out from equation below

$$P_{cond} = I_{DRMS}^2 \times R_{DSon_{hot}}$$

Where,

I_{DRMS} = RMS value of the current through MosFET

$R_{DSon_{hot}}$ = Rdson at working junction temperature

Coss Losses

Coss is the virtual capacitor across MosFET drain and source. While switch is off, the Coss will be charged to the voltage across drain and source and when the switch turns on Coss discharges first.

Find the Coss from curve showing capacitance vs drain to source voltage, for the working Vds.

The Coss losses can be found from equation below

$$P_{Coss} = \frac{1}{2} \times C_{oss} \times V_{DS}^2 \times f_{sw}$$

Where,

P_{Coss} = Coss losses

C_{oss} = Coss at working V_{DS}

V_{DS} = Drain to source voltage

f_{sw} = Switching frequency

Turn on and Turn off of MosFET

The equivalent circuit below shows the MosFET with components having great effects in switching process.

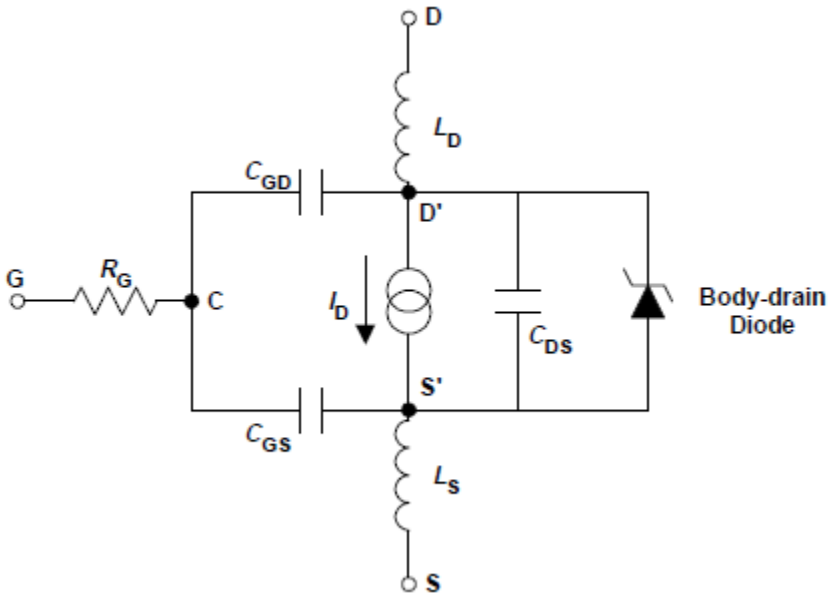

Figure 1. MosFET equivalent circuit

The datasheet of a MosFET shows 3 capacitances,

C_{iss}= Input capacitor

C_{oss}= Output capacitor

C_{rss}= Reverse transfer capacitance

The relation between the datasheet capacitances and equivalent circuit capacitances are as given below

C_{iss}= C_{GS}+C_{GD} with C_{DS} shorted

C_{rss}= C_{GD}

C_{oss}= C_{GS}+C_{GD}

Where,

C_{GS} = Gate to source capacitor

C_{GD} = Gate to drain capacitor

C_{DS} = Drain to source capacitor

Turn-on Process

The graph below shows the MosFET turn on process.

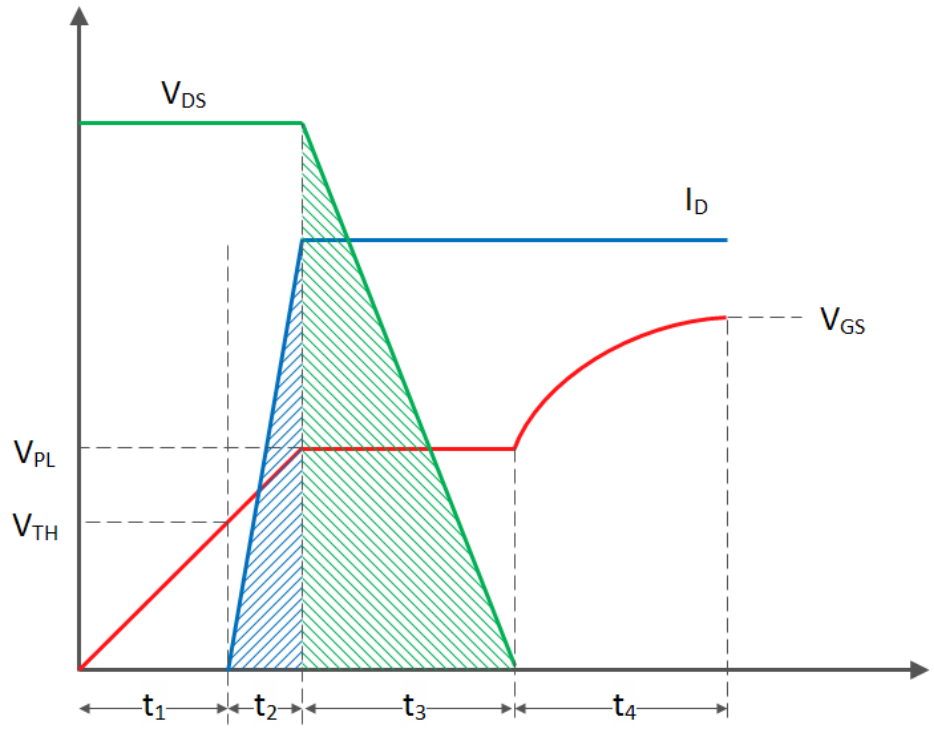

Figure 2 – MosFET turn on curve

t_1 – When a voltage of V_{GS} is applied across MosFET gate, C_{GS} and C_{GD} is charged initially. Until the voltage reaches the threshold value of gate voltage V_{TH}, there is no change in voltage and current across MosFET.

t_2 – Once the gate voltage reaches V_{TH} , the current starts increasing, but drain to source voltage still remains the same. When the gate voltage reaches the plateau voltage V_{PL} , C_{GS} is fully charged and the drain current reaches its final value. This time t_2 is called turn on delay time $t_{d(on)}$.

t_3 – Once gate voltage reaches plateau voltage V_{PL} , the voltage remains at the same level until the capacitor C_{GD} is fully charged. This capacitor is called Miller capacitor and the region is known as Miller plateau. When voltage reaches plateau, V_{DS} starts falling and at the end of plateau region, V_{DS} reaches the minimum value of 10% of maximum V_{DS}. The time t_3 is called rise time t_r.

t_4 – Once C_{GD} is fully charged at the end of plateau, the capacitors C_{GS} and C_{GD} charges up to the final value of applied V_{GS}.

The gate charge parameters in MosFET datasheet Q_{gs} and Q_{gd} are the bare minimum charge required to turn on the MosFET, but an additional charge should be required to keep the MosFET on, thus making the total charge to be Q_g. Power loss will be there when voltage and current changes, this occur at times $t_{d(on)}$ and t_r. The equations for the times can be found out from the capacitor charging equations.

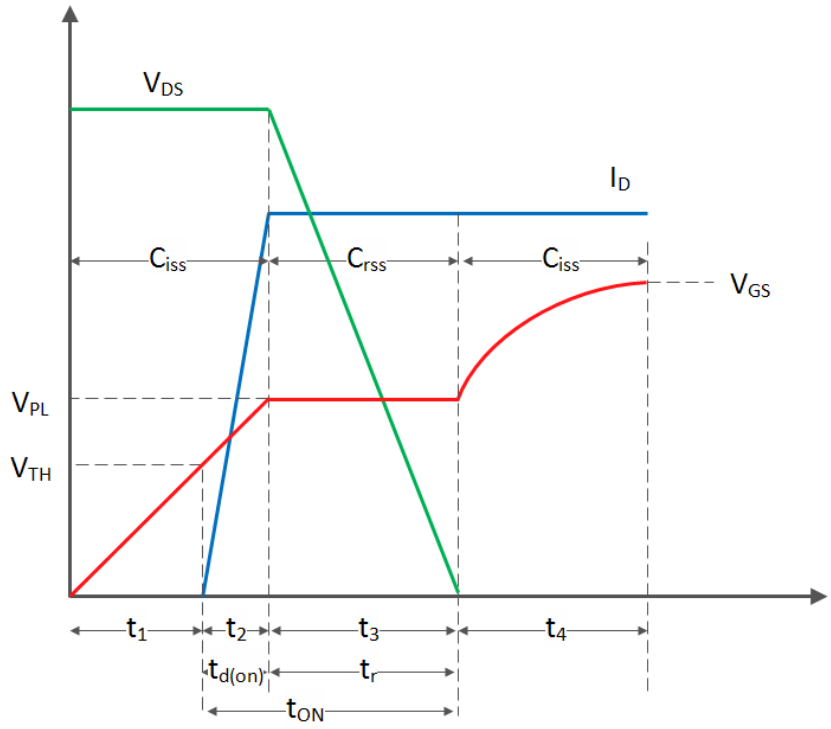

Figure 3 – Turn on times and capacitances

The capacitor charging equation in general is

$$V_c = V_s\left(1 - e^{(-t/RC)}\right)$$

$$t = -RC\ln\left(\frac{V_s - V_c}{V_s}\right)$$

Where,

V_c = Capacitor voltage at the end of time t.

V_s = Source voltage

t = Time taken for the capacitor voltage to rise from 0 to V_c

R = Charging resistor

C =The capacitance

For times t_1 and t_2, the capacitor C_{iss} charges from gate supply through a resistor $R_{G(on)}$, where $R_{G(on)}$ is the sum of internal and external gate resistances in the charging path.

$$t_{d(on)} = t_2 = [(t_1 + t_2) - t_2]$$

Transforming the general equation into MosFET charge parameters, we will get

$$t_1 + t_2 = -R_{G(on)}C_{iss}\ln\left(\frac{V_{GS} - V_{PL}}{V_{GS}}\right)$$

$$t_1 = -R_{G(on)}C_{iss}\ln\left(\frac{V_{GS} - V_{TH}}{V_{GS}}\right)$$

Equation 2 – 1 gives

$$t_{d(on)} = R_{G(on)}C_{iss}\ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{PL}}\right)$$

Where,

$t_{d(on)}$ =Turn on delay time

$R_{G(on)}$ = Sum of internal and external gate resistances in the charging path

C_{iss}= Input capacitor at working V_{DS}, taken from graph

V_{GS} = Gate-source driver supply voltage

V_{TH} = Gate threshold voltage

V_{PL} =Miller plateau voltage

For time t_3, the capacitor C_{rss} charges from gate supply through a resistor $R_{G(on)}$ at a voltage V_{PL}. The rise time t_3 can be found out from the equation below.

$$t_r = R_{G(on)} C_{rss} \left(\frac{V_{DS}}{V_{GS} - V_{PL}}\right)$$

Where,

t_r = Rise time

$R_{G(on)}$ = Sum of internal and external gate resistances in the charging path

C_{rss} = Reverse transfer capacitor at working V_{DS}, taken from graph

V_{GS} = Gate-source driver supply voltage

V_{DS} = Drain to source working voltage

V_{PL} = Miller plateau voltage

The total on time t_{ON} is given by,

$$t_{ON} = t_{d(on)} + t_r$$

$$t_{ON} = R_{G(on)} C_{iss} \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{PL}}\right) + R_{G(on)} C_{rss} \left(\frac{V_{DS}}{V_{GS} - V_{PL}}\right)$$

Turn-off Process

The graph below shows the MosFET turn off process.

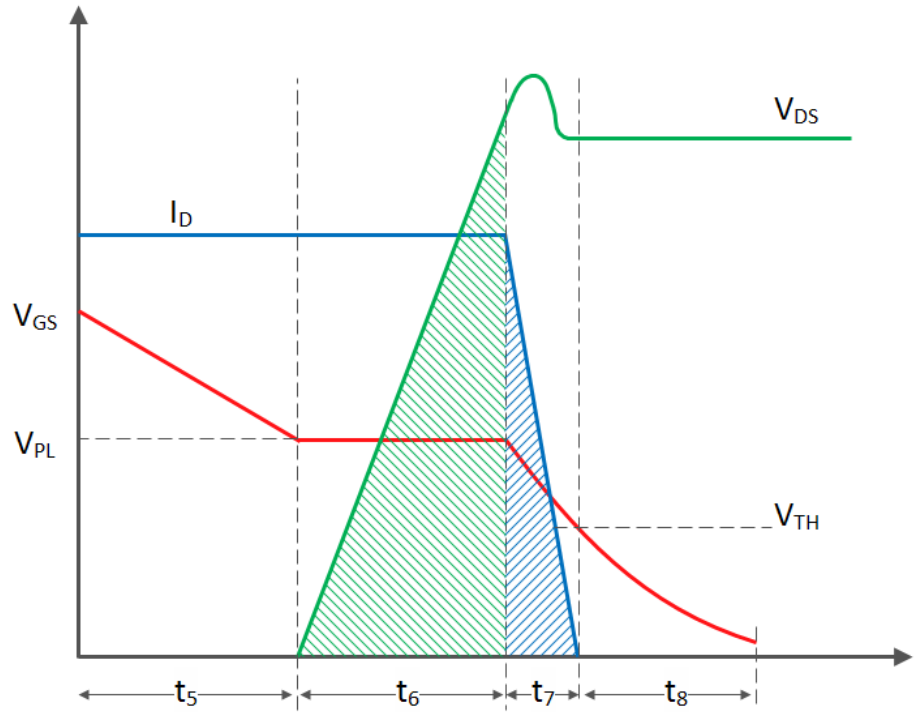

Figure 4 – Mosfet turn off curve

t_5 – When the gate voltage of V_{GS} is made zero from the driver, the voltage across Mosfet gate capacitors starts discharging from the high level value of V_{GS}. Until the voltage reaches the miller plateau voltage V_{PL}, there is no change in voltage and current across MosFET.

t_6 – Once the gate voltage reaches V_{PL} , V_{DS} starts rising and at the end of plateau region V_{DS} reaches the value of 90% of maximum V_{DS}. This time t_6 is called turn off delay time $t_{d(off)}$.

t_7 – At the end of plateau region, the drain current and gate voltage starts falling. Drain current reaches its minimum value, when the gate voltage crosses the threshold value of gate voltage V_{TH}. As the drain current falls, the leakage and stray inductances in the switching path generates a spike in the V_{DS}. The time t_7 is called fall time t_f and at the end of fall time, the mosfet is completely turned off.

t_8 – The remaining gate voltage from V_{TH} discharges to zero at this time period.

Power loss will be there when voltage and current changes, this occur at times $t_{d(off)}$ and t_f. The equations for the times can be found out from the capacitor discharging equations. The figure below shows the turn off times and capacitances.

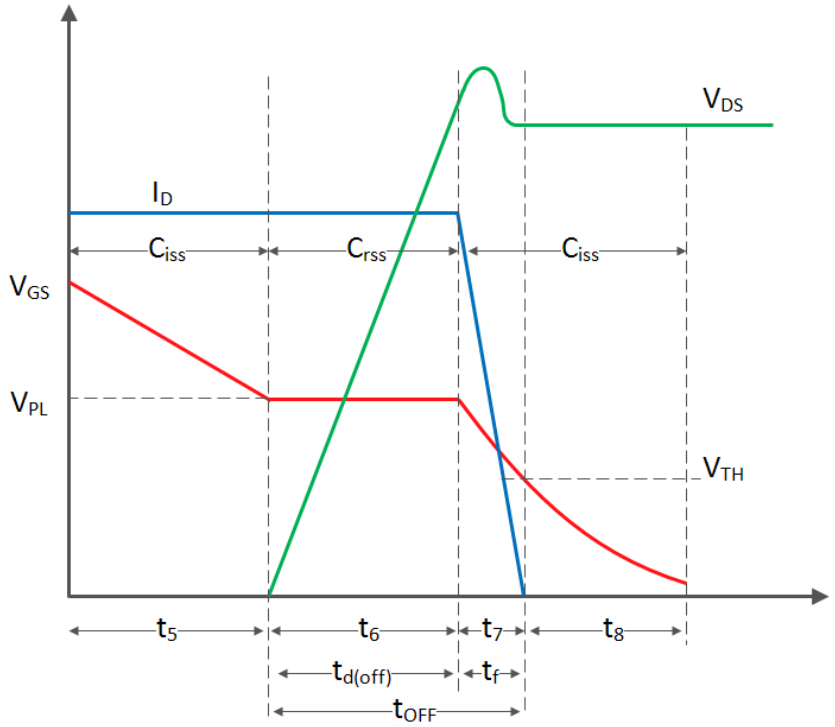

Figure 5 – Mosfet turn off times and capacitances

The capacitor discharging equation in general is

$$V_c = V_s\, e^{(-t/RC)}$$

$$t = -RC \ln\left(\frac{V_c}{V_s}\right)$$

Where,

V_c = Capacitor voltage at the end of time t.

V_s = Initial voltage

t = Time taken for the capacitor voltage to fall from V_s to V_c

R = Discharge resistor

C =The capacitance

For times t_7 and t_8, the capacitor C_{iss} discharges from the plateau voltage V_{PL} through a resistor $R_{G(off)}$, where $R_{G(off)}$ is the sum of internal and external gate resistances in the gate turn off path.

Transforming the general equation into MosFET gate discharge parameters, we will get

$$t_f = R_{G(off)} C_{iss} \ln\left(\frac{V_{PL}}{V_{TH}}\right)$$

Where,

t_f =Fall time

$R_{G(off)}$ = Sum of internal and external gate resistances in the discharging path

C_{iss}= Input capacitor at working V_{DS}, taken from graph

V_{TH} = Gate threshold voltage

V_{PL} =Miller plateau voltage

For time t_6, the capacitor C_{rss} discharges through a resistor $R_{G(off)}$ at a voltage V_{PL}. The turn off delay time t_6 can be found out from the equation below.

$$t_{d(off)} = R_{G(off)} C_{rss} \left(\frac{V_{DS}}{V_{PL}}\right)$$

Where,

$t_{d(off)}$ = Turn off delay time

$R_{G(off)}$ = Sum of internal and external gate resistances in the discharging path

C_{rss}= Reverse transfer capacitor at working V_{DS}, taken from graph

V_{DS} = Drain to source working voltage

V_{PL} = Miller plateau voltage

The total off time t_{OFF} is given by,

$$t_{OFF} = t_{d(off)} + t_f$$

$$t_{OFF} = R_{G(off)} C_{rss} \left(\frac{V_{DS}}{V_{PL}}\right) + R_{G(off)} C_{iss} \ln\left(\frac{V_{PL}}{V_{TH}}\right)$$

Turn on and turn off losses

Now that we have the turn on and turn off time of mosfet, we can find out the losses in these regions.

Turn on losses can be calculated from

$$P_{on} = V_{DS} \times I_{min} \times t_{ON} \times f_{sw}$$

Where,

P_{on} = Turn on losses

V_{DS} = Drain to source voltage excluding and spikes

t_{ON} = Total turn on time

f_{sw} = Switching frequency

I_{min} = The current at which mosfet turns on – For discontinuous and boundary conduction modes, I min will be zero and hence there will not be any turn on losses. For continuous conduction mode, I_{min} will be the difference between the peak current and peak to peak ripple current.

Turn off losses can be calculated from

$$P_{off} = V_{DS(peak)} \times I_{peak} \times t_{OFF} \times f_{sw}$$

Where,

P_{off} = Turn off losses

$V_{DS(peak)}$ = Drain to source voltage including the turn off spike

t_{OFF} = Total turn off time

f_{sw} = Switching frequency

I_{peak} = The current at which mosfet turns off – For all conduction modes, I_{peak} will be the maximum peak current in the mosfet.

Gate losses

Gate losses are due to the gate charge losses and the power loss on the internal gate resistor due to gate current.

$$P_G = P_{Qg} + P_{RG}$$

Where,

P_G = Total gate losses

P_{Qg} = Gate charge losses

P_{RG} = Losses on the internal gate resistance

Gate charge losses

The total gate charge Q_g of the mosfet has to be found out from the datasheet curve for the working gate voltage.

Gate charge losses can be found out from the equation below

$$P_{Qg} = Q_g \times V_{GS} \times f_{sw}$$

Where,

Q_g = Total gate charge from datasheet curve

V_{GS} = Gate-source driver supply voltage

f_{sw} = Switching frequency

Losses in internal gate resistance

When the gate current flows through the internal gate resistance, the ohmic losses contribute a minor portion in the total losses. The total gate charge divided by the time taken for charge and discharge respectively will give the average current while charging and discharging. The figure 6 below explains the charging and discharging characteristics of mosfet.

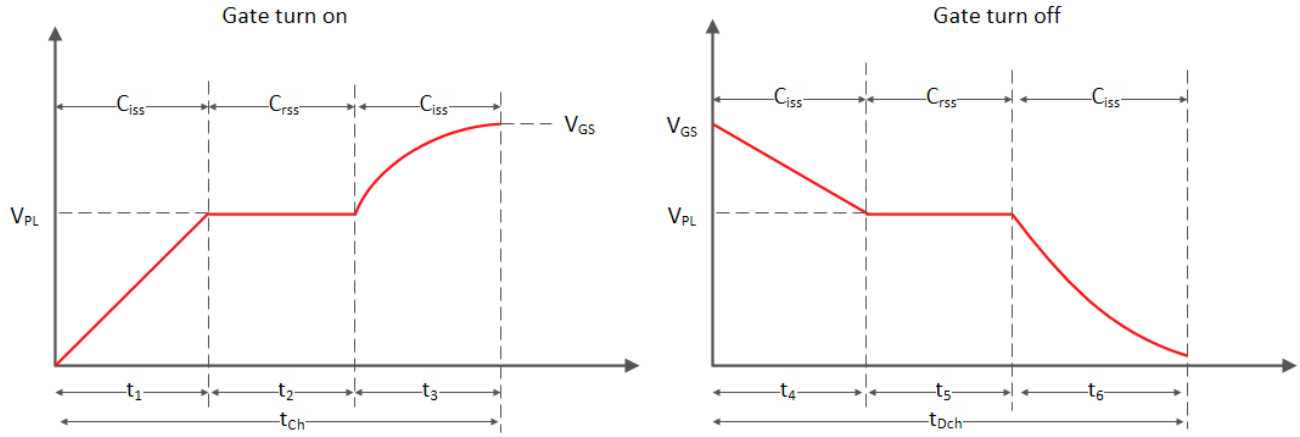

Figure 6 – Mosfet gate characteristics – turn on and turn off

t_1 – At time t_1, input capacitor C_{iss} charges from 0 to gate threshold V_{PL} through $R_{G(on)}$. The time t_1 is given by the equation;

$$t_1 = -R_{G(on)} C_{iss} \ln\left(\frac{V_{GS} - V_{PL}}{V_{GS}}\right)$$

t_2 – At time t_2, capacitor C_{rss} charges at gate threshold V_{PL} through $R_{G(on)}$. The time t_2 is given by the equation;

$$t_2 = R_{G(on)} C_{rss} \left(\frac{V_{DS}}{V_{GS} - V_{PL}}\right)$$

t_3 – At time t_3, capacitor C_{iss} charges from gate threshold voltage V_{PL} to final value of the applied gate voltage V_{GS} through $R_{G(on)}$. The time t_3 can be found out from the capacitor time constant equation considering 98% charge.

$$t_3 = 4 \times R_{G(on)} C_{rss}$$

t_4 – At time t_4, input capacitor C_{iss} discharges from V_{GS} to gate threshold V_{PL} through $R_{G(off)}$. The time t_4 is given by the equation;

$$t_4 = R_{G(off)} C_{iss} \ln\left(\frac{V_{PL}}{V_{GS}}\right)$$

t_5 – At time t_5, capacitor C_{rss} discharges at gate threshold V_{PL} through $R_{G(off)}$. The time t_5 is given by the equation;

$$t_5 = R_{G(off)} C_{rss} \left(\frac{V_{DS}}{V_{PL}}\right)$$

t_6 – At time t_6, capacitor C_{iss} discharges from gate threshold voltage V_{PL} to 0 through $R_{G(off)}$. The time t_6 can be found out from the capacitor time constant equation considering 98% discharge.

$$t_6 = 4 \times R_{G(off)} C_{iss}$$

Total charging time and discharging time is given by

$$t_{Ch} = t_1 + t_2 + t_3$$

$$t_{Dch} = t_4 + t_5 + t_6$$

The average current during turn on and turn off is given by

$$I_{g(on)} = \frac{Q_g}{t_{Ch}}$$

$$I_{g(off)} = \frac{Q_g}{t_{Dch}}$$

Average power loss in gate resistor is given by

$$P_{RG} = \left(I_{g(on)}^2 \times R_{G(on)} \times t_{Ch} \times f_{sw}\right) + \left(I_{g(off)}^2 \times R_{G(off)} \times t_{Dch} \times f_{sw}\right)$$

Where,

$I_{g(on)}, I_{g(off)}$ = The average gate current during on time and off time

t_{Ch}, t_{Dch} = Total charging time and discharging time

MosFET Design Considerations

There are certain things to be considered while selecting a mosfet. The major two things which effect the switching are listed below

- dV/dt protection
- External gate resistor selection
- Gate-source resistor selection

dV/dt Protection

When the mosfet turns on and off, drain to source voltage changes very fast. While this process, there is chance that false turn on may occur or at certain conditions, catastrophic failure may occur if the dV/dt is not limited. While turn on and turn off of the mosfet, the dV/dt can occur. The turn on time dV/dt protection can be given by connecting a resistor across mosfet gate to source and turn off time protection can be given by selecting the external gate resistor properly.

There are two ways dV/dt can occur while turn off. The maximum rate of rise of drain to source voltage is limited by the peak reverse recovery of body diode. While the mosfet is turning off, the drain to source voltage rises, the miller capacitor C_{GD} discharges through the gate resistor and creating a voltage drop across gate to source. If this voltage drop exceeds the gate threshold value, the mosfet turns on again, this may lead into failure. Another mechanism of false turn on is due to the parasitic BJT appears across drain and source of mosfet.

Turn off dV/dt protection can be given by selecting lower turn off impedance $R_{G(off)}$. One common method is to provide a diode to bypass some resistance in the turn on path.

When the mosfet is used in inverter or freewheeling applications, the body diode conducts at some switching times, there the reverse recovery should be considered for maximum dV/dt.

External Gate resistor selection

The external gate resistor has to be selected according to two parameters

- dV/dt Protection
- Gate drive current capability

Gate resistor selection based on dV/dt protection – turn off

The maximum dV/dt limit can be found out by the equation below. One important parameter to consider is the negative temperature coefficient in the gate threshold voltage. At higher temperatures, the gate threshold voltage will considerably reduce due to this negative temperature coefficient.

$$\frac{dV}{dt_{limit}} = \frac{V_{TH}+V_{TC}(T_j\text{-}25°C)}{R_{G(int)}\times C_{GD}}$$

Where,

$\frac{dV}{dt_{limit}}$ = the maximum allowable dV/dt

V_{TH} = Gate threshold voltage

V_{TC} = Gate threshold voltage temperature coefficient

T_j = Mosfet junction temperature

$R_{G(int)}$ = Internal gate resistance

C_{GD} = Gate to drain capacitor = C_{rss}= Reverse transfer capacitor at working V_{DS}

Figure 7 below shows the mosfet turn off equivalent circuit with a gate drive circuitry.

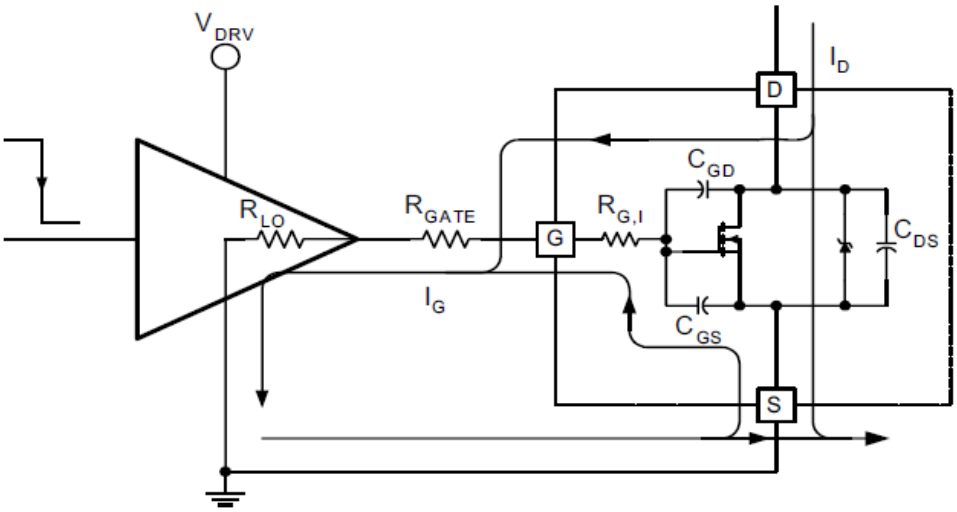

Figure 7 – Mosfet gate turn off path with gate drive

The gate resistance at turn off is the sum of internal gate resistance, external gate resistance and the turn off impedance of gate drive circuitry.

$$R_{G(off)} = R_{G(int)} + R_{G(ext)} + R_{LO}$$

Where,

$R_{G(int)}$ = Internal gate resistance

$R_{G(ext)}$ = External gate resistance

R_{LO} = Gate drive resistance

The maximum possible external gate resistance value depends upon the actual dV/dt present in the circuit. Maximum turn off resistance is given by

$$R_{G(off)max} = \frac{V_{TH} + V_{TC}(T_j\text{-}25°C)}{C_{GD} \times \left(\frac{dV}{dt}\right)_{max}}$$

Where,

$\left(\frac{dV}{dt}\right)_{max}$ = the maximum dV/dt possible in the circuit

$R_{G(ext)}$ has to be selected which is lesser than the maximum value obtained from equation 1 and 2. Another factor to be considered is if the external gate resistor selected is too low, which reduces the fall time where the current falls very fast, which in turn increases the dI/dt and hence the spike in drain source voltage. Thus care should be taken to select the proper gate resistance.

Gate resistor selection based on gate drive current capability – turn on

The on time gate resistor selection is based upon the gate drive current capability. Lower the value of gate resistor, smaller the turn on time, but higher the gate current. While selecting the gate resistor, the gate drive current has to be taken into account. Again higher dV/dt causes switching noises which appear as radiated emission.

The minimum turn on gate resistance is given by

$$R_{G(on)min} = \frac{V_{GS} - V_{PL}}{I_{G(on)max}}$$

Where,

$I_{G(on)max}$ = Maximum on time gate current, which is limited by the gate driver

Gate-Source resistor selection

The gate to source resistor is important in giving dV/dt protection while mosfet turn on. A resistance value lesser than the maximum can be selected which is depending upon the maximum possible dV/dt appearing in the mosfet. The maximum value of gate source resistor is given by the equation below

$$R_{GS(max)} = \frac{V_{TH} + V_{TC}(T_j\text{-}25°C)}{C_{GD} \times \left(\frac{dV}{dt}\right)_{max}}$$

Where,

$R_{GS(max)}$ = The maximum value of Gate to Source resistance

$\left(\frac{dV}{dt}\right)_{max}$ = The maximum dV/dt possible in the circuit

Steps to find the gate resistors

Selecting a gate resistor is an iterative process. Even if theoretically matches also, while doing the EMI EMC tests the gate resistor tuning may be required, as the stray inductance completely depends upon the switching tracing in PCB, mosfet leads, soldering etc.

Steps to find the turn off resistance

STEP 1 : Find the maximum dV/dt limit from the equation (If esr is not given in mosfet datasheet, use the gate source ESR value)

$$\frac{dV}{dt}_{limit} = \frac{V_{TH}+V_{TC}(T_j\text{-}25°C)}{R_{G(int)}\times C_{GD}}$$

STEP 2 : Select a dV/dt lesser than the limit – use approximations like select fall time from datasheet to start with and V_{DS} from design with 20% spike voltage.

STEP 3 : Find the maximum off time gate resistance and hence the maximum external gate resistance possible from the equations below – use available values, omit R_{LO} if not known.

$$R_{G(off)max} = \frac{V_{TH}+V_{TC}(T_j\text{-}25°C)}{C_{GD}\times\left(\frac{dV}{dt}\right)_{max}}$$

$$R_{G(off)} = R_{G(int)} + R_{G(ext)} + R_{LO}$$

STEP 4 : Select nearest standard value for external gate resistance and find the fall time and turn off delay time.

$$t_f = R_{G(off)} C_{iss} \ln\left(\frac{V_{PL}}{V_{TH}}\right)$$

$$t_{d(off)} = R_{G(off)} C_{rss} \left(\frac{V_{DS}}{V_{PL}}\right)$$

STEP 5 : Find the mosfet turn off spike voltage generated by the stray inductances- consider 20nH for approximation.

$$V_{DS(spike)} = 20nH \times \frac{I_{peak}}{t_f}$$

STEP 6 : Find the actual maximum dV/dt from equation below. Check if the dV/dt max is less than the dV/dt limit. If yes, proceed to STEP 7, else go to STEP 3 and substitute lesser value of dV/dt max.

$$\frac{dV}{dt}_{max} = \frac{V_{DS} + V_{DS(spike)}}{t_f + t_{d(off)}}$$

STEP 7 : Find the turn off losses in the mosfet and check whether the value is acceptable or not. If acceptable we have the external gate resistance value, if not acceptable reduce the dV/dt further and repeat the steps from STEP 3 onwards until a satisfactory result is achieved.

$$V_{DS(peak)} = V_{DS} + V_{DS(spike)}$$

$$t_{OFF} = t_{d(off)} + t_f$$

$$t_{OFF} = R_{G(off)} C_{rss} \left(\frac{V_{DS}}{V_{PL}}\right) + R_{G(off)} C_{iss} \ln\left(\frac{V_{PL}}{V_{TH}}\right)$$

$$P_{off} = V_{DS(peak)} \times I_{peak} \times t_{OFF} \times f_{sw}$$

Steps to find the turn on resistance

STEP 1 : Find the maximum gate drive current possible from the driver and find the gate resistance required.

$$R_{G(on)min} = \frac{V_{GS} - V_{PL}}{I_{G(on)max}}$$

STEP 2 : Check if the minimum value obtained from STEP 1 is lesser than the sum of internal and external gate resistors at turn off. If its lesser, use the same external resistance for on time also, else select the nearest standard value and proceed to next step.

STEP 3 : Calculate the turn on delay time, rise time and turn on losses.

$$t_{d(on)} = R_{G(on)} C_{iss} \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{PL}}\right)$$

$$t_r = R_{G(on)} C_{rss} \left(\frac{V_{DS}}{V_{GS} - V_{PL}}\right)$$

$$t_{ON} = t_{d(on)} + t_r$$

$$t_{ON} = R_{G(on)} C_{iss} \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{PL}}\right) + R_{G(on)} C_{rss} \left(\frac{V_{DS}}{V_{GS} - V_{PL}}\right)$$

$$P_{on} = V_{DS} \times I_{min} \times t_{ON} \times f_{sw}$$

Steps to find gate source resistance

STEP 1 : Find the maximum gate source resistor for the turn on dV/dt calculated as below and select the nearest standard value lesser than the maximum.

$$\left(\frac{dV}{dt}\right)_{on-max} = \frac{V_{DS}}{t_r}$$

$$R_{GS(max)} = \frac{V_{TH} + V_{TC}(T_j\text{-}25°C)}{C_{GD} \times \left(\frac{dV}{dt}\right)_{on-max}}$$

Sample calculation

References

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[3]. Power MOSFET Basics By Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

[4]. Fundamentals of MOSFET and IGBT Gate Driver Circuits - Application Report SLUA618A- Texas Instruments

[5]. PowerMOSFET Application Note - AN-080E Rev.1.1- Fuji Power MOSFET

[6]. Understanding power MOSFET data sheet parameters - application note AN11158 – Nexperia

[7]. AN-9010 MOSFET Basics - Fairchild

EMI-EMC

Electro- magnetic interference (EMI) can be defined as the electro magnetic energy which affects the functioning of an electronic device. Electromagnetic compatibility (EMC) is the devices ability to work in noisy environment. The measure of emi generated by the device which is known as emission testing, and the assessing the proper functioning of a device under electro-magnetic energy field is known as susceptibility or immunity.

EMC standards and limits

CISPR11-FCC Part 15C

The measure for emi noise generation is of two types

Conducted emission and radiated emission

Conducted emission is the disturbance produced by the power electronic converter in the ac mains when it is operating. The frequency range for conducted emission measurement is 150kHz to 30MHz.

Radiated emission is the electro magnetic energy waves produced by the power electronic circuit in a near field through air. The frequency range starting from 30mHz to 1GHz.

The equipments are classified into groups and classes as per the CISPR11 standard.

Class A equipment is equipment suitable for use in all establishments other than domestic and those directly connected to a low voltage power supply network which supplies buildings used for domestic purposes

Class B equipment is equipment suitable for use in domestic establishments and in establishments directly connected to a low voltage power supply network which supplies buildings used for domestic purposes

The tables below shoes the conducted and radiated noise levels in class B equipments

Table 2b – Mains terminal disturbance voltage limits for class B equipment measured on a test site

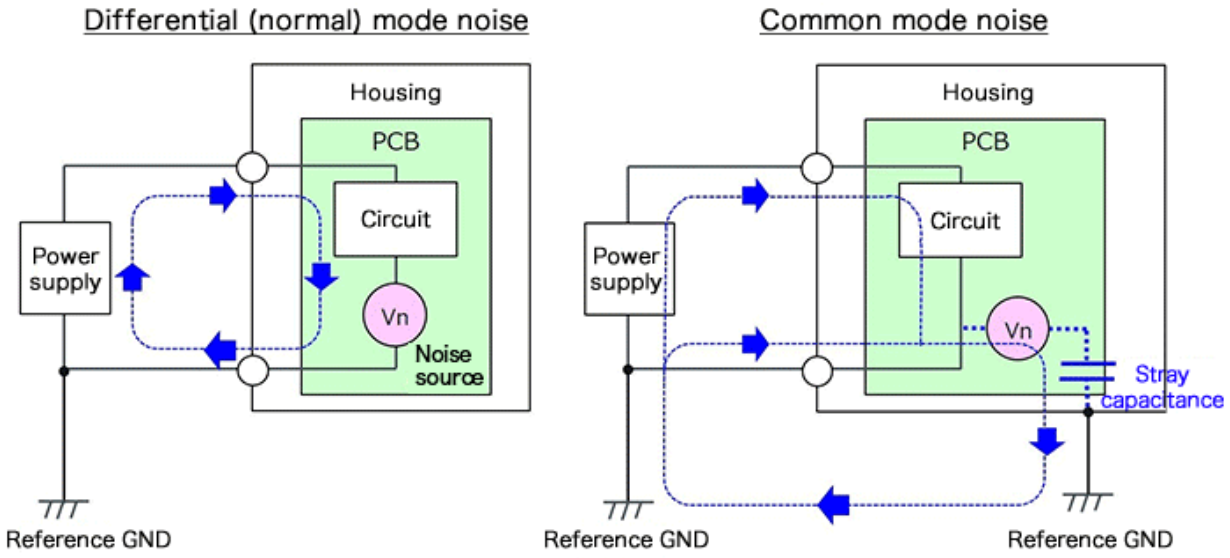
Class B equipment limits dB(μV)		
Frequency band MHz	**Groups 1 and 2**	
	Quasi-peak	**Average**
0,15 – 0,50	66 Decreasing linearly with logarithm of frequency to 56	56 Decreasing linearly with logarithm of frequency to 46
0,50 – 5	56	46
5 – 30	60	50
NOTE Care should be taken to comply with leakage current requirements.		

Table 3 – Electromagnetic radiation disturbance limits for group 1 equipment

Frequency band	Measured on a test site		Measured *in situ*
	Group 1, class A 10 m measurement distance	Group 1, class B 10 m measurement distance	Group 1, class A Limits with measuring distance 30 m from exterior wall outside the building in which the equipment is situated
MHz	dB(µV/m)	dB(µV/m)	dB(µV/m)
0,15 – 30	Under consideration	Under consideration	Under consideration
30 – 230	40	30	30
230 – 1 000	47	37	37

Common mode noise and differential mode noise

The figure below explains the common mode and differential mode noises



- A mode in which a noise current flows on the same path as the power supply current
- Noise voltage occurs across power supply lines

- Noise voltage does not occur across power supply lines
- Noise voltage occurs across power supply line and reference GND
- Noise currents flow in the same direction on the power supply positive and negative sides

In differential mode noise, the noise source appears across power supply lines and is in series with the power supply line, and the noise current flows in the same direction as the power supply current. It is called "differential mode" because the outgoing and return currents are oppositely-directed.

Common mode noise is noise in which a noise current that has leaked via a stray capacitance or the like passes through ground and returns to the power supply line. It is called "common mode" noise because the direction of the noise currents on the positive (+) and the negative (-) sides of the power supply have the same direction. A noise voltage does not appear across the power supply lines.

The noise appearing in switching power supplies can be well explained using figure below.

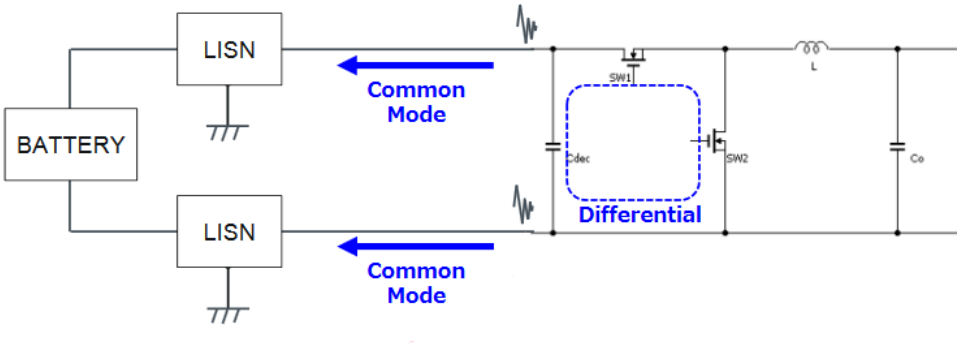


Figure 1 Common mode and differential mode noise

The differential mode noises is due to the high speed turn on and turn off of switching elements which in turn produces the ringing between the trace inductance and stray capacitances. The current and voltage are given by the equations

$$I = C\frac{dV}{dt}$$

$$V = L\frac{dI}{dt}$$

The mosfet turn on and turn off ringing are due to the LC tank circuits appearing for the switching time.

Radiation

The figure below shows the radiation due to differential mode appearing at a point at a distance r from the loop with an area S, which is having a loop current of Id and a frequency f. The equation of electric field intensity is given by the equation in the figure

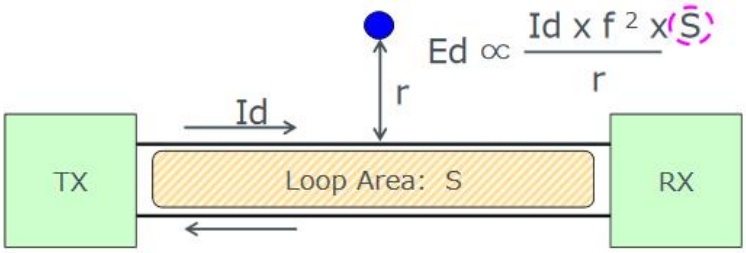


Figure 1 : radiation due to differential mode noise

The figure shows the radiation due to common mode noise which varies depending upon the cable length, common mode current and frequency.

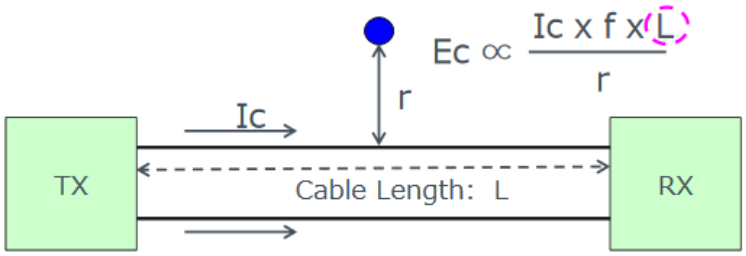


Figure 2 : radiation due to common mode noise

References

[1]. EMC Basics verA2 – Rohm Semiconductor

[2].