

# 1. Description

## 1.1. Project

Project Name	DC-DC
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	09/17/2024

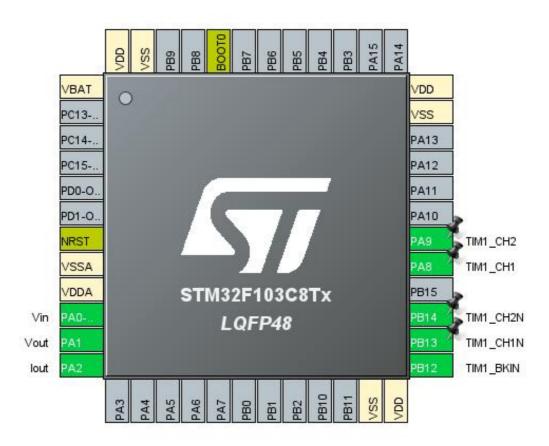
## 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

## 1.3. Core(s) information

Core(s)	Arm Cortex-M3

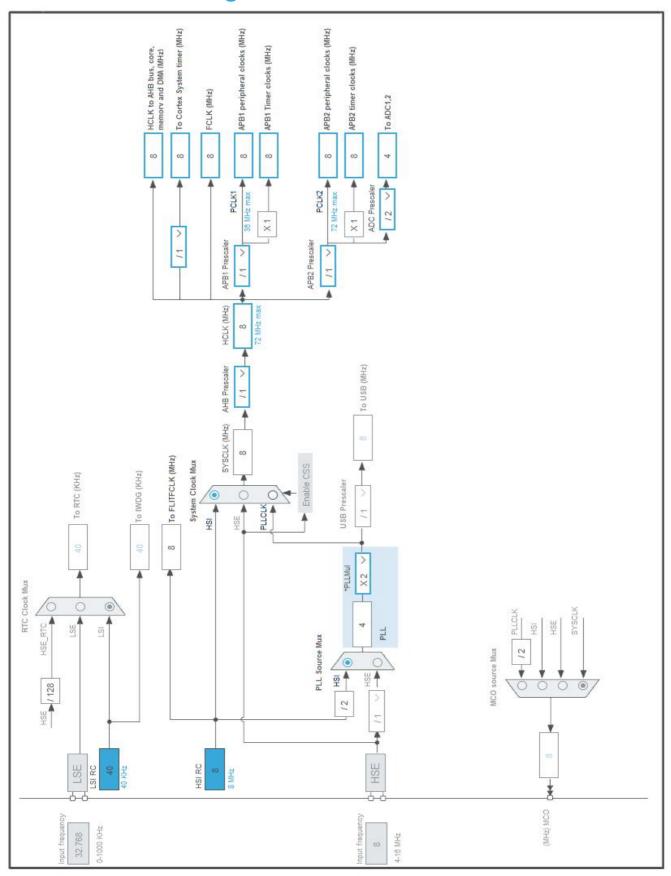
## 2. Pinout Configuration



# 3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	Vin
11	PA1	I/O	ADC1_IN1	Vout
12	PA2	I/O	ADC1_IN2	lout
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	TIM1_BKIN	
26	PB13	I/O	TIM1_CH1N	
27	PB14	I/O	TIM1_CH2N	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
35	VSS	Power		
36	VDD	Power		
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

# 4. Clock Tree Configuration



# 1. Power Consumption Calculator report

#### 1.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	DS5319_Rev17

#### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

## 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

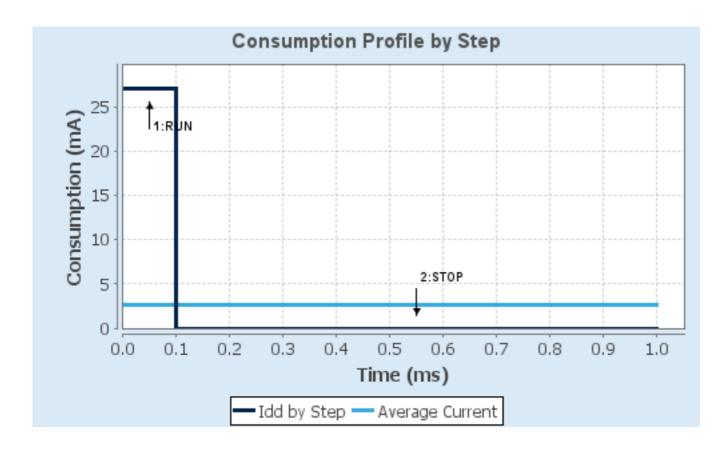
## 1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

## 1.6. Chart



# 2. Software Project

## 2.1. Project Settings

Name	Value
Project Name	DC-DC
Project Folder	C:\Users\mubar\STM32CubelDE\workspace_1.16.0\DC-DC
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.6
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

#### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM1_Init	TIM1
4	MX_ADC1_Init	ADC1

## 3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN0 mode: IN1 mode: IN2

#### 3.1.1. Parameter Settings:

#### ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Data Alignment Right alignment
Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 0
Sampling Time 1.5 Cycles

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

#### 3.2. RCC

#### 3.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

#### 3.3. SYS

**Debug: No Debug** 

Timebase Source: SysTick

#### 3.4. TIM1

**Clock Source : Internal Clock** 

Channel1: PWM Generation CH1 CH1N Channel2: PWM Generation CH2 CH2N

mode: Activate-Break-Input 3.4.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 255 \*

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx\_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State Enable
BRK Polarity High

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

Dead Time 0

#### **PWM Generation Channel 1 and 1N:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CHN Polarity High

CH Idle State Reset
CHN Idle State Reset

#### **PWM Generation Channel 2 and 2N:**

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High
CHN Polarity High
CH Idle State Reset
CHN Idle State Reset

<sup>\*</sup> User modified value

# 4. System Configuration

## 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	Vin
	PA1	ADC1_IN1	Analog mode	n/a	n/a	Vout
	PA2	ADC1_IN2	Analog mode	n/a	n/a	lout
TIM1	PB12	TIM1_BKIN	Input mode	No pull-up and no pull-down	n/a	
	PB13	TIM1_CH1N	Alternate Function Push Pull	n/a	Low	
	PB14	TIM1_CH2N	Alternate Function Push Pull	n/a	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	

## 4.2. DMA configuration

nothing configured in DMA service

## 4.3. NVIC configuration

## 4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Prefetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	15	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
ADC1 and ADC2 global interrupts	unused				
TIM1 break interrupt	unused				
TIM1 update interrupt	unused				
TIM1 trigger and commutation interrupts	unused				
TIM1 capture compare interrupt	unused				

## 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

#### \* User modified value

## 5. System Views

5.1. Category view

5.1.1. Current



## 6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32f1\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1\_svd.zip

Description

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