THE NATIONAL INSTITUTE OF ENGINEERING

Mananthavadi Road, Mysuru-570 008

Phone: 0821-2480475,2481220,4004947 Fax: 0821-2485802,

Email: echod@nie.ac.in

MINOR PROJECT REPORT

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TITLE OF MINOR PROJECCT :Sequential Implementation of Y86-64 Processor Architecture Design using Hardware Coding Language VERILOG

NAME	USN
MUDDUKRISHNA Y	4NI22EC052
MALLAPPA BAGOJI	4NI22EC046
PANNAGA KALKUR	4NI22EC058

Submitted under the supervision of:

Dr. NARASIMHA KAULGUD ,Professor Dept of ECE, NIE, Mysore

ABSTRACT :

The Y86 processor is a simplified, educational processor designed to help students and engineers understand the fundamental concepts of computer architecture and processor design. It serves as a learning tool by modeling the basic principles of instruction set architecture, pipelining, and microarchitecture in a more accessible way than commercial processors.

The Y86 is inspired by the x86 architecture but significantly simplified to include fewer instructions and features. It supports basic instructions such as arithmetic operations, control flow, and memory access, while omitting complex features like floating-point operations and advanced optimizations. Its primary objective is to teach concepts like instruction execution, data dependencies, and control hazards in a manageable context.

Key findings from implementing and studying the Y86 processor often include insights into how pipelined architectures improve performance, the challenges of handling hazards, and the importance of efficient control logic. Through experiments with the Y86, students can gain practical experience debugging and optimizing assembly-level programs, implementing control and data paths, and understanding trade-offs in processor design.

In conclusion, the Y86 processor serves as a valuable educational tool, bridging the gap between theoretical concepts and practical application. By working with the Y86, learners develop a deeper appreciation of how modern processors function while building foundational skills in computer architecture

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CHAPTER 1
INTRODUCTION

Project Description:

The Y86-64 processor's 6 stages for sequential implementation are: Fetch, Decode, Execute, Memory, Writeback, and PC Update. These stages ensure orderly execution of instructions, where one instruction is completed before the next begins.

Overview

1. Fetch (F): Retrieves the instruction from memory using the program counter (PC).
2. Decode (D): Interprets the instruction and identifies required operands.
3. Execute (E): Performs computations or determines memory address calculations via the ALU.
4. Memory (M): Accesses memory for load/store operations or updates flags.
5. Writeback (W): Writes results to registers, completing the instruction's effect.
6. PC Update: Updates the PC to the address of the next instruction.

Purpose

1. Simplified Processor Understanding

- The sequential design breaks down complex processor operations into six clear and distinct stages (Fetch, Decode, Execute, Memory, Writeback, and PC Update).
- It provides an intuitive understanding of how each stage contributes to the execution of an instruction.

2. **Educational Value**

- The sequential model is highly effective for students and beginners in computer architecture, as it avoids the complexities of advanced techniques like pipelining and parallelism.
- Each stage is processed one at a time, offering a step-by-step illustration of the inner workings of a processor.

3. **Debugging and Problem-Solving**

- Sequential execution ensures that only one instruction is active in the processor at any given time, making it easier to trace errors and debug programs.
- This predictability aids in understanding the behavior of specific instructions or machine-level programs.

4. **Platform for Experimentation**

- By providing a straightforward structure, it allows designers to test and prototype new ideas without being overwhelmed by the complexity of modern, highly parallelized architectures.
- Developers can focus on understanding the impact of individual stages and transitions on performance.

5. **Bridge to Advanced Architectures**

- The sequential design serves as a stepping stone to more complex processor architectures.

- It highlights the limitations of sequential execution (e.g., low throughput, high latency), motivating the study of techniques like pipelining, hazard resolution, and superscalar processing.

6. **Demonstration of Control Flow**
   - The sequential stages emphasize how instructions are fetched, decoded, executed, and retired in a linear fashion.
   - This clarity helps in understanding how the Program Counter (PC) is updated, how instructions are stored in memory, and how data flows through the system.

Scope

1. **Educational Use:**
   - The sequential implementation in the Y86-64 processor is ideal for learning the basic concepts of computer architecture and instruction execution.
   - Each stage is designed for clarity, making it easier to understand the specific tasks performed at every step.
2. **Simplified Design:**
   - The absence of parallelism reduces complexity, making it a practical starting point for beginners or for prototyping processor models.
   - Sequential stages align well with software simulators and debugging tools due to predictable, linear execution.
3. **Development and Testing:**
   - Provides a controlled environment to test how individual instructions behave in isolation without the complexities of pipelining or hazards.

Limitations

1. **Performance Constraints:**
   - Sequential execution leads to low throughput, as only one instruction progresses through the processor at a time.
   - High instruction latency becomes a bottleneck in performance-critical systems.
2. **Inefficiency for Complex Systems:**
   - The sequential model does not scale well for real-world applications that require higher performance and parallel processing.
   - Lack of pipelining leads to wasted clock cycles, especially for simple instructions.
3. **Unrealistic for Modern Architectures:**
   - The sequential design oversimplifies the operation of modern processors, which rely heavily on advanced techniques like pipelining, superscalar execution, and out-of-order processing.

CHAPTER 2

LITERATURE SURVEY

Title: *Computer Organization and Design: The Hardware/Software Interface*

Author: Patterson, D., & Hennessy, J. (2014)

Key Observations:

- Introduces the Y86-64 architecture as a simplified version of the x86-64 for educational purposes.
- Describes the components of the processor architecture, such as ALU, registers, control units, and memory.
- Emphasizes the modular nature of the design, making it ideal for educational use.

Key Observed Problems:

- The simplicity of the architecture may not capture the full complexity of real-world processor designs.
- Certain aspects of hardware optimization and performance considerations are left out to maintain educational clarity.

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2. Title: *Verilog HDL: A Guide to Digital Design and Synthesis*

Author: Zhao, M., et al. (2005)

Key Observations:

- Provides comprehensive details on using Verilog to design digital systems.
- Highlights Verilog's role in synthesizing processors and understanding sequential and combinational logic.
- Explores best practices for coding in Verilog to avoid errors and ensure efficient design.

Key Observed Problems:

- Challenges in designing complex systems with Verilog due to the verbosity and potential for errors in large designs.
- Lack of beginner-friendly resources for mastering the advanced aspects of Verilog.

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3. Title: *Computer Organization and Architecture: Designing for Performance*

Author: Stallings, W. (2016)

Key Observations:

- Provides detailed explanations of processor architecture concepts, including the stages of the Y86-64 processor.
- Highlights the role of memory management and pipelining in modern processors.
- Discusses the importance of implementing control units and ALUs in Verilog for simulating processor behavior.

Key Observed Problems:

- The book does not deeply explore optimization strategies for Verilog code.
- Focuses more on architectural principles than the actual HDL design and practical implementation.

4. Title: *Design and Implementation of a Simple Processor Using Verilog*

Author: Ghosal, A., & Chetan, K. (2012)

Key Observations:

- Focuses on sequential processor design using Verilog, outlining step-by-step the process of building a simple processor.
- Explores how each instruction is handled in the processor, with clear insights into the fetch-decode-execute cycle.

Key Observed Problems:

- The simplicity of the design makes it difficult to address complex issues like pipeline hazards, parallelism, and resource sharing.
- Limited discussion of performance optimizations or real-world application of such designs.

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5. Title: *Optimized Verilog Design Techniques for Sequential Processors*

Author: Benker, T., et al. (2019)

Key Observations:

- Focuses on the need for optimization in Verilog designs, particularly in sequential processor implementations.
- Discusses techniques for reducing gate count, minimizing clock cycles, and ensuring synthesis compatibility.

Key Observed Problems:

- Optimization often leads to more complex and harder-to-understand Verilog code.
- Struggling to find the right balance between optimization and maintainability in educational processor designs.

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6. Title: *Educational Use of Processor Design: Implementing a Simple Y86-64 Processor in Verilog*

Author: Kessler, D. (2008)

Key Observations:

- Highlights the educational benefits of building a processor like Y86-64 in Verilog.
- Emphasizes how students gain hands-on experience with state machines, instruction cycles, and memory management.

Key Observed Problems:

- Educational processors may oversimplify important aspects of processor architecture.
- Limited focus on real-world performance issues, such as clock speed and power consumption.

CHAPTER 3

METHODOLOGY

The methodology for implementing the Y86-64 processor in a sequential manner using Verilog focuses on designing and simulating the processor with six stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), Write-back (WB), and Halt (HLT). The process follows a step-by-step approach to simulate the behavior of the processor while ensuring that each stage executes sequentially. Below is the description of the approach used:

1. Design Approach:

- **Sequential Design**: The Y86-64 processor is implemented using a sequential model where each instruction is processed in a single clock cycle. This approach ensures that only one instruction is executed at a time, and no parallel processing or pipelining occurs. The six stages (IF, ID, EX, MEM, WB, and HLT) are implemented sequentially in a clock-driven manner.
- **Verilog Implementation:** The processor's behavior is described using Verilog, a hardware description language, which is suitable for modeling and simulating digital circuits. Each stage (IF, ID, EX, MEM, WB, and HLT) is modeled as a separate block or module in Verilog.

2. Stages Description:

- **Instruction Fetch (IF):** This stage retrieves the next instruction from memory using the Program Counter (PC). The instruction is fetched based on the current value of the PC, and the instruction is passed on to the decode stage. The PC is then incremented.
- **Instruction Decode (ID):** The instruction is decoded to identify the operation to be performed. The operands (such as registers) are retrieved from the register file during this stage. Control signals are generated to guide the subsequent stages.
- **Execute (EX):** The Arithmetic Logic Unit (ALU) performs the required operations (e.g., addition, subtraction, logical operations) on the operands fetched in the ID stage. The result of the operation is passed to the memory stage if needed.
- **Memory Access (MEM):** If the instruction involves memory access (such as a load or store instruction), memory is accessed in this stage. For load instructions, data is read from memory; for store instructions, data is written to memory.
- **Write-back (WB):** This stage writes the result of the operation (either from the ALU or memory) back into the register file, updating the registers as needed.
- **Halt (HLT):** The halt stage is used to indicate when the processor should stop executing instructions. It is a control signal to end the processing.

3. Simulation Approach:

- **Testbench Creation**: A testbench is created to simulate the behavior of the processor. The testbench applies a series of instructions to the processor and verifies that the outputs are correct at each stage.
- **Data Flow Simulation**: The data flow between stages is modeled using registers and wires in Verilog. Each stage's output is connected to the next stage's input, ensuring that data flows sequentially through the processor.
- **Clock-driven Simulation**: The entire processor design is clock-driven, with each clock cycle triggering the execution of the next instruction in the sequence. The simulation is run for a set number of cycles, allowing the processor to process multiple instructions.

4. Data Collection and Analysis:

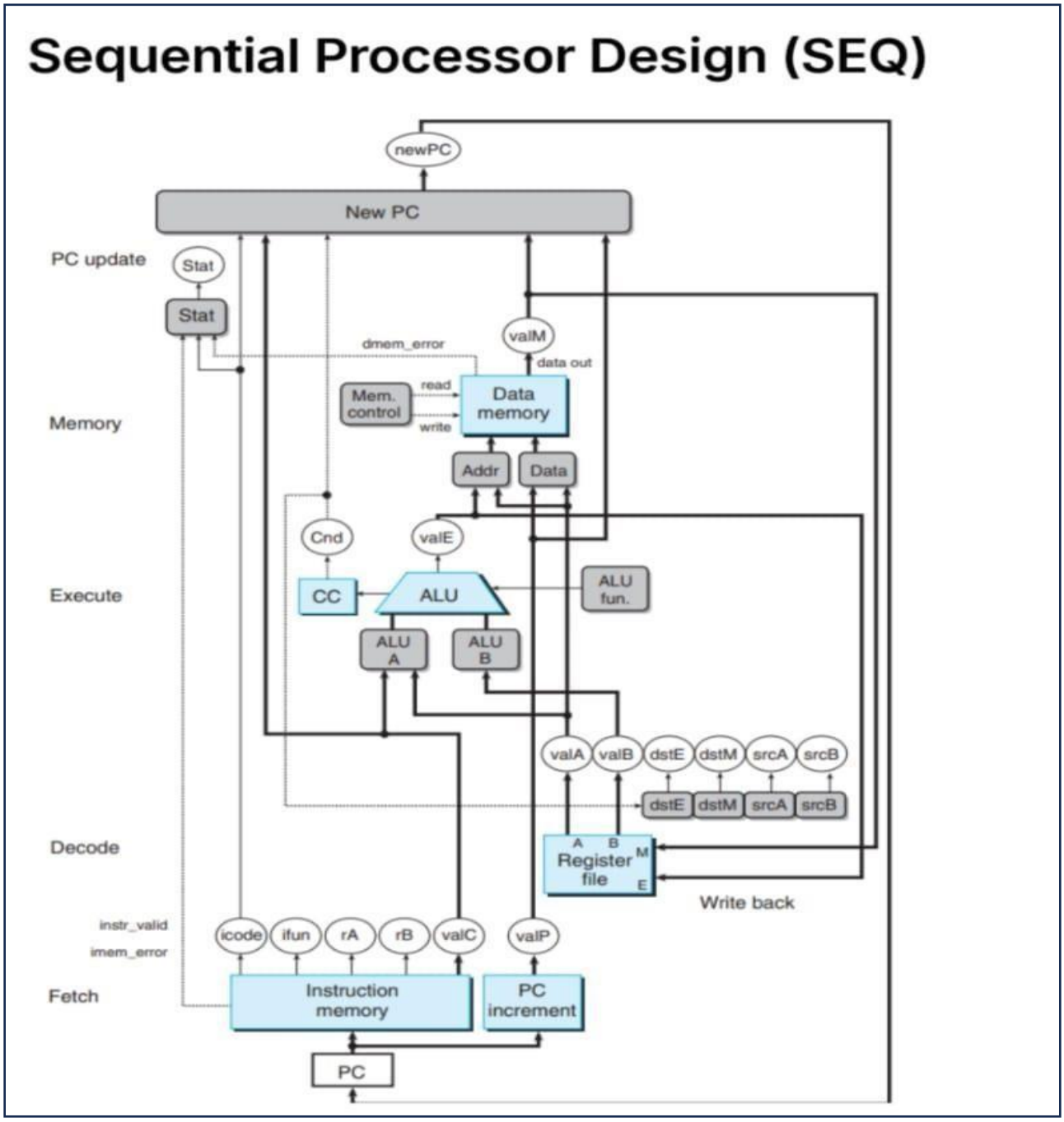
- **Instruction Set Simulation**: A predefined set of Y86-64 instructions is executed to evaluate the correctness of the processor's implementation. The instructions may include arithmetic, logical, load, store, and control flow operations.
- **Execution Trace:** During the simulation, an execution trace is collected to observe the instruction flow through the six stages. This trace helps verify that each stage is functioning correctly and that the correct result is obtained after all stages have completed.
- **Performance Metrics**: Although the design is sequential, basic performance metrics such as instruction cycle count and execution time are measured. This helps to identify any inefficiencies or potential areas for optimization.

5. Verification and Validation:

- **Functional Testing:** The processor is tested with various programs to ensure that it correctly executes all supported instructions. This includes verifying that the instruction fetch, decode, execution, memory access, and write-back stages all perform as expected.
- **Edge Case Testing**: Special test cases, such as invalid instructions or boundary conditions in memory access, are used to check the robustness of the design.
- **Correctness of Results**: The results of the processor's execution are compared with expected results (from manual calculations or reference implementations) to ensure correctness.

CHAPTER 4

MAIN BODY



INSTRUCTIONS SETS OF Y86-64 PROCESSOR

INSTRUCTION	OPCODE	DESCRIPTION
halt	00	Stop program execution
nop	10	Do nothing for one cycle
rrmovq	20	Move register to regisrter
cmovle	21	Conditional move if less than or equal
cmov1	22	Conditional move if less than
cmove	23	Conditional move if equal
cmovne	24	Conditional move if not equal
cmovge	25	Conditional move if greater than or equal
cmovg	26	Conditional move if greater
irmovq	30	Move immediate to register
rmmovq	40	Move register to memory
mrmovq	50	Move memory to register
addq	60	Add rA to rB
subq	61	Subtract rA from rB
andq	62	Bitwise and rA and rB
xorq	63	Bitwise xor of rA and rB
Jmp	70	Unconditional jump to dest
Jle	71	Jump if less than or equL TO Dest
J1	72	Jump if less than dest
je	73	Jump if equal to dest
jne	74	Jump if not equal to dest
Jge	75	Jump if greater than or equal to dest
jg	76	Jump if greater than dest
call	80	Call subroutine at dest
ret	90	Return from subroutine
pushq	A0	Push register rA onto the stack
popq	B0	Pop top of stack into register rA

Y86 -64 Registers

Register Name	Register code	Description
%rax	0	General-purpose register ,often used for function return values (analogous to rax in x86-64)
%rcx	1	General -purpose register, often used as a counter or for loop iterations
%rdx	2	General -purpose register, typically used for input /output operations or as an additional counter
%rbx	3	General -purpose register, sometimes reserved for base pointers or other program data
%rsp	4	Stack pointer register, points to the top of the stack in memory. required for pushq and popq operations
%rbp	5	Base pointer register, used for stack frame references ,though not strictly required in Y86-64 programs
%rsi	6	General- purpose register often used to pass arguments to functions or for source indexing
%rdi	7	General- purpose register commonly used for functions arguments or destination indexing
%r8	8	Additional general -purpose registers like R8 in x 86-64
%r9	9	Additional general -purpose registers, similar to R9 in X 86-64
None	F	Represents no register (used in instructions where a register operand is not applicable)

Stage	HALT	NOP	CMOV	IRMOVQ
Fch	icode:ifun ← M_1[PC] valP ← PC + 1	icode:ifun ← M_1[PC] valP ← PC + 1	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valC ← M_8[PC+2] valP ← PC + 10
Dec			valA ← R[rA]	
Exe	cpu.stat = HLT		valE ← valA Cnd ← Cond(CC,ifun)	valE ← valC
Mem				
WB			Cnd ? R[rB] ← valE	R[rB] ← valE
PC	PC ← 0	PC ← valP	PC ← valP	PC ← valP
Stage	RMMOVQ	MRMOVQ	OPq	jXX
Fch	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valC ← M_8[PC+2] valP ← PC + 10	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valC ← M_8[PC+2] valP ← PC + 10	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	icode:ifun ← M_1[PC] valC ← M_8[PC+1] valP ← PC + 9
Dec	valA ← R[rA] valB ← R[rB]	 valB ← R[rB]	valA ← R[rA] valB ← R[rB]	
Exe	valE ← valB + valC	valE ← valB + valC	valE ← valB OP valA Set CC	Cnd ← Cond(CC,ifun)
Mem	M_8[valE] ← valA	valM ← M_8[valE]		
WB		R[rA] ← valM	R[rB] ← valE	
PC	PC ← valP	PC ← valP	PC ← valP	PC ← Cnd ? valC:valP
Stage	CALL	RET	PUSHQ	POPQ
Fch	icode:ifun ← M_1[PC] valC ← M_8[PC+1] valP ← PC + 9	icode:ifun ← M_1[PC] valP ← PC + 1	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2
Dec	 valB ← R[RSP]	valA ← R[RSP] valB ← R[RSP]	valA ← R[rA] valB ← R[RSP]	valA ← R[RSP] valB ← R[RSP]
Exe	valE ← valB - 8	valE ← valB + 8	valE ← valB - 8	valE ← valB + 8
Mem	M_8[valE] ← valP	valM ← M_8[valA]	M_8[valE] ← valA	valM ← M_8[valA]
WB	R[RSP] ← valE	R[RSP] ← valE	R[RSP] ← valE	R[RSP] ← valE R[rA] ← valM
PC	PC ← valC	PC ← valM	PC ← valP	PC ← valP

1.FETCH STAGE

The Fetch Stage in the Y86 Processor

The fetch stage in the Y86 processor is the first step in executing an instruction. Its primary role is to retrieve the instruction from memory and prepare it for decoding. This stage is critical because it initiates the processing of every instruction in the pipeline. Below, we provide a detailed explanation of the fetch stage, its components, operations, and challenges.

1. Purpose of the Fetch Stage

The fetch stage is responsible for accessing the memory to obtain the instruction to be executed. It determines what operation the processor needs to perform next and retrieves any associated data or operands from the instruction.

- Key Functionality:

- Reads the instruction byte(s) from memory. ○ Updates the program counter (PC) to point to the next instruction. ○ Passes the fetched instruction to the decode stage for further processing.

In a pipelined Y86 processor, this stage operates concurrently with other stages, making its efficient operation crucial for overall performance.

2. Components of the Fetch Stage

Several hardware components work together in the fetch stage to accomplish its tasks. These include:

1. **Program Counter (PC):** ○ Holds the address of the current instruction in memory. ○ Is updated after every fetch to point to the next instruction.
2. **Instruction Memory:** ○ Stores the program instructions.
   - The fetch stage accesses this memory using the PC to retrieve instruction bytes.
3. **Instruction Register** ○ Temporarily holds the fetched instruction before it is passed to the decode stage. ○ In some designs, this register helps in decoupling the fetch and decode stages.
4. **PC Increment Logic:** ○ Determines the new PC value after fetching the current instruction.
   - Accounts for variable instruction lengths, ensuring the PC points to the start of the next instruction.

3. Steps in the Fetch Stage

Step 1: Access Instruction Memory

- The fetch stage uses the value of the PC to access the instruction memory.
- Depending on the instruction format, one or more bytes are retrieved from memory. The first byte is typically the opcode, which specifies the operation to be performed. Step 2: Parse the Instruction Length
- Y86 instructions have variable lengths, ranging from 1 to 6 bytes. After fetching the initial byte, the fetch stage determines how many additional bytes are needed.
- For example:
  - A simple halt instruction is 1 byte.
  - A rrmovq instruction (register-to-register move) is 2 bytes (1 byte for opcode and 1 byte for register specifiers).
  - An irmovq instruction (immediate-to-register move) requires 10 bytes (1 byte opcode, 1 byte register, 8 bytes for the immediate value). Step 3: Update the Program Counter
- After fetching the instruction, the PC is updated to point to the next instruction. The exact update depends on the instruction's length and type.
- For control-flow instructions (e.g., jmp, call), the PC may be updated with a target address instead of incrementing sequentially.

Step 4: Pass Instruction to Decode Stage

- The fetched instruction and its components (e.g., opcode, operands) are forwarded to the decode stage for interpretation and execution preparation.

4. Handling Control-Flow Instructions

Control-flow instructions, such as jumps (jmp), calls (call), and returns (ret), introduce additional complexity to the fetch stage. The fetch stage must:

- Identify whether the current instruction is a control-flow instruction.
- Update the PC with the target address if needed. For example:
  - In a jmp instruction, the PC is set to the specified target address.
  - In a call instruction, the PC is updated after pushing the return address to the stack. When the target address depends on the result of a prior stage (e.g., the execute stage for conditional branches), the fetch stage may need to stall or wait for resolution.

5. Pipeline Considerations

In the Y86 pipelined processor, the fetch stage operates alongside other stages (decode, execute, memory, write-back). This introduces several challenges: Stalls:

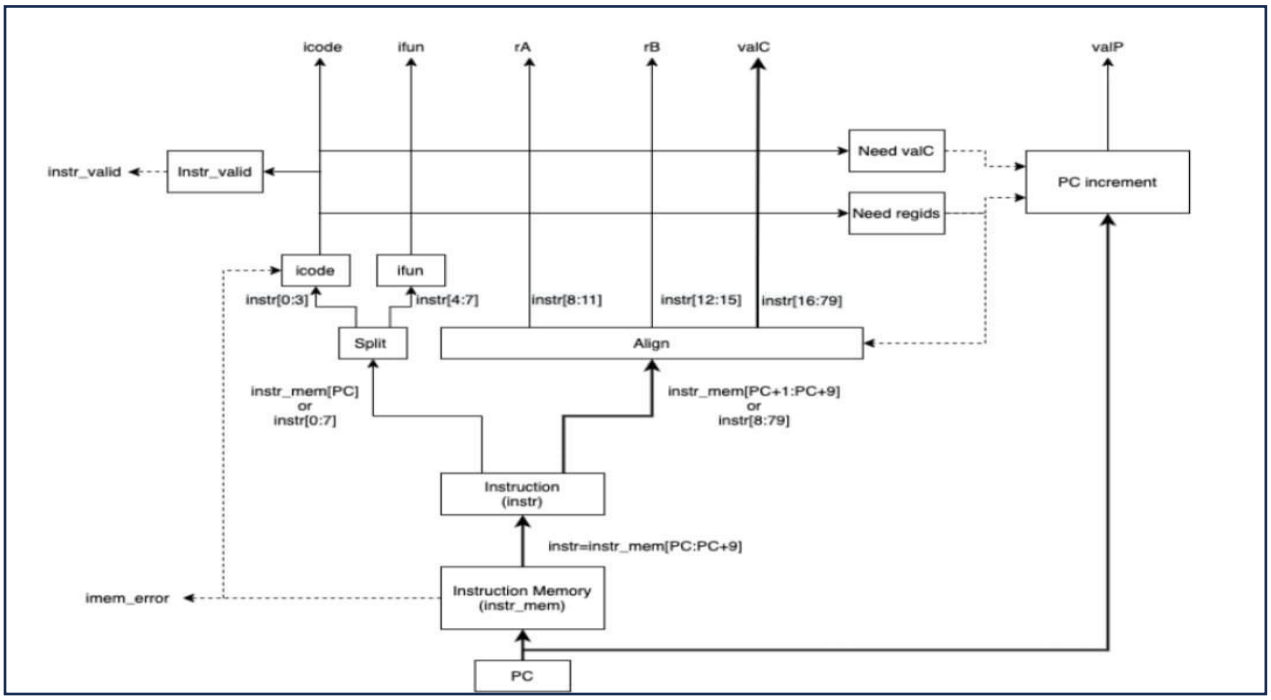
- If a control-flow instruction is encountered, the pipeline may need to pause until the new PC value is calculated.

Instruction Alignment:

- Ensuring that instructions are fetched correctly, especially for variable-length instructions, requires careful management of the PC and memory access.

6. Example of Fetch Stage Operation :

1. **Instruction**: **irmovq $10, %rax** ○
   Opcode: 0x30 (1 byte) ○ Register
   Specifier: 0xF0 (1 byte) ○
   Immediate Value: 10 (8 bytes) ○
   Total Size: 10 bytes The fetch stage:
   - Reads 10 bytes starting from the address in the PC.
   - Updates the PC to point to the next instruction.
2. **Instruction: jmp 0x0040** ○ Opcode:
   0x70 (1 byte) ○ Target Address: 0x0040
   (8 bytes) ○ Total Size: 9 bytes
   The fetch stage:
   - Reads 9 bytes starting from the PC.
   - Updates the PC with the target address (0x0040).



Processes in the fetch block:

1)PC register contains the current instruction to be executed from the instruction memory and passed to the instruction memory.

2)The instruction memory gives an **imem_error** if the PC value obtained is greater than the maximum instruction in instruction memory. In our project we have set our maximum number of instructions to **1024**, i.e: PC can range from **0 to 1023**. If PC is within instruction range memory passes 10 bytes of instruction further.

3)**icode, ifun, valC, Instr_valid, valP** are taken as output of this stage. These values are derived from the instruction passed from Instruction memory according to following rules:

Instruction	Byte offset from PC									
	0	1	2	3	4	5	6	7	8	9
halt	0 0									
nop	1 0									
cmovXX rA, rB	2 fn	rA rB								
irmovq V, rB	3 0	f rB	V							
rmmovq rA, D(rB)	4 0	rA rB	D							
mrmovq D(rB), rA	5 0	rA rB	D							

Instruction	Byte offset from PC								
	0	1	2	3	4	5	6	7	8
OPq rA, rB	6 fn	rA rB							
jXX Dest	7 fn	Dest							
call Dest	8 0	Dest							
ret	9 0								
pushq rA	a 0	rA f							
popq rA	b 0	rA f							

1. **icode, ifun** defines the instructions to be performed.
2. **rA, rB** specifies the registers on which these instructions are being performed.
3. **valC** is initialized with V/d/Dest according to the icode's.

4. **Instr_error** occurs when icode or ifun are not in valid range. Rage of ifun is defined according to the current icode instruction.
5. If halt (icode = 0) is encountered the **HLT** flag is set to 1 and the processor stops running due to a $finish statement.

Fetch module:

```
module fetch(
    output reg [3:0] icode,
    output reg [3:0] ifun,
    output reg [3:0] rA,
    output reg [3:0] rB,
    output reg [63:0] valC,
    output reg [63:0] valP,
    output reg mem_error,
    output reg instr_error,
    input clk,
    input [63:0] PC,
    input [0:79] instr
);

```

Error update:

1.HLT

```
always @(icode) begin
  if(icode==0 )
    $finish;
end

```

2.istr_error, mem_error:

```
always @(mem_error) begin
  if(mem_error == 1 || instr_err == 1)
      $monitor("Wrong instr add\n");
end
```

```
    always @* begin
        if (PC > 1023) begin
            mem_error = 1'b1;
        end
        else begin
            mem_error = 1'b0;
        end

```

2.Decode

The decode stage in the Y86-64 processor plays a critical role in interpreting the instructions fetched from memory and preparing them for execution. This stage involves several key steps, including instruction decoding, operand fetching, and the setting up of control signals needed for the execution phase.

1. Overview of the Decode Stage in the Y86-64 Processor

The Y86-64 architecture is a simplified version of the x86-64 processor, designed for educational purposes. The decode stage follows the fetch stage, where the processor retrieves an instruction from memory. The purpose of the decode stage is to interpret the instruction, extract the necessary information (such as operands and operation codes), and prepare for the execution stage.

This stage typically involves decoding the instruction's operation (opcode), identifying the registers and memory locations involved, and generating control signals for subsequent stages. In a pipelined processor like Y86-64, this step happens concurrently with other stages in different pipeline registers.

2. Structure of an Instruction in Y86-64

Y86-64 instructions are typically 1 to 10 bytes long and follow a specific format. The primary components of the instruction include:

- **Opcode (1 byte)**: Specifies the operation to be performed (e.g., add, mov, jmp).
- **Register identifiers**: Specifies which registers are used in the operation (e.g., rax, rbx).
- **Immediate values**: Some instructions may include immediate values (constants or data) that are used directly in operations.
- **Memory addresses**: For memory operations, instructions may include addresses or offsets to access memory locations.

3. Decoding the Instruction

In the decode stage, the instruction fetched from memory is analyzed, and the control unit begins decoding it. The process involves:

- **Opcode decoding**: The opcode is extracted from the instruction and interpreted. The opcode specifies what operation the processor should perform (e.g., arithmetic, logic, data movement, control flow).
- **Operand decoding**: Y86-64 instructions may require operands, which could be registers, immediate values, or memory locations. The decode stage identifies the operands and their types (register or immediate value). For example, the instruction addq %rax, %rbx means that the value in rax will be added to the value in rbx.
- **Register and Immediate Fetch**: If the instruction involves a register operand, the appropriate registers (from the register file) are identified. For immediate operands, the value is retrieved and passed along.

4. Instruction Types

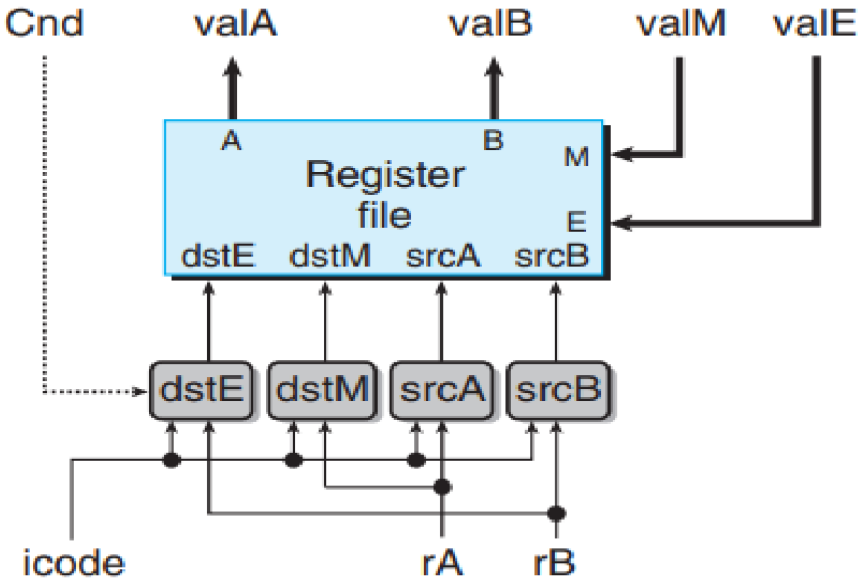
The Y86-64 supports various instruction types, including:

- **Arithmetic operations**: These include instructions like addq, subq, and mulq, which perform arithmetic operations on registers or memory.
- **Data movement**: Instructions like movq and pushq move data between registers and memory. • **Control flow**: Instructions like jmp (unconditional jump) and jz (jump if zero) are used to alter the flow of execution.
- **System calls**: Special instructions that interact with the operating system, such as handling I/O operations.

Key Elements:

- **Opcode extraction**: The opcode is simply a slice of the instruction's bits (typically the first byte or 8 bits). This value identifies the operation to perform (e.g., add, sub).
- **Register Operand Extraction**: The source and destination registers are extracted by selecting the corresponding bits from the instruction.

- **Immediate Value Extraction**: If the instruction includes an immediate value, this is extracted from the lower bits (typically 32 bits) of the instruction.



We have initialized these registers in the testbench as:

```
initial begin
  clk=0;
  PC = 64'd0;

  cf_in = 3'b000;

  reg_file_in[0] = 64'd0;
  reg_file_in[1] = 64'd1;
  reg_file_in[2] = 64'd2;
  reg_file_in[3] = 64'd3;
  reg_file_in[4] = 64'd60;  //stack pointer
  reg_file_in[5] = 64'd5;
  reg_file_in[6] = 64'd6;
  reg_file_in[7] = 64'd7;
  reg_file_in[8] = 64'd8;
  reg_file_in[9] = 64'd9;
  reg_file_in[10] = 64'd10;
  reg_file_in[11] = 64'd11;
  reg_file_in[12] = 64'd12;
  reg_file_in[13] = 64'd13;
  reg_file_in[14] = 64'd14;
```

Decode module declaration:

```
3 module decode(clk,rA,rB,icode,reg0,reg1,reg2,reg3,reg4,reg5,reg6,reg7,reg8,reg9,reg10,reg11,reg12,reg13,reg14,valA,valB);
4 input clk;
5 input [3:0] rA,rB,icode;
6 input [63:0] reg0,reg1,reg2,reg3,reg4,reg5,reg6,reg7,reg8,reg9,reg10,reg11,reg12,reg13,reg14;
7 wire [63:0] reg_file_in [0:14];
8 output reg [63:0] valA,valB;
9
10 assign reg_file_in[0] = reg0;
11 assign reg_file_in[1] = reg1;
12 assign reg_file_in[2] = reg2;
13 assign reg_file_in[3] = reg3;
14 assign reg_file_in[4] = reg4;
15 assign reg_file_in[5] = reg5;
16 assign reg_file_in[6] = reg6;
17 assign reg_file_in[7] = reg7;
18 assign reg_file_in[8] = reg8;
19 assign reg_file_in[9] = reg9;
20 assign reg_file_in[10] = reg10;
21 assign reg_file_in[11] = reg11;
22 assign reg_file_in[12] = reg12;
23 assign reg_file_in[13] = reg13;
24 assign reg_file_in[14] = reg14;
25
```

3.EXECUTE

The **execute stage** in the Y86-64 processor plays a pivotal role in performing the actual operation specified by an instruction. It is the stage where most of the computational work is done, including arithmetic, logical operations, and memory address calculations. The execution can be classified into different categories based on the type of instruction, such as arithmetic and logic operations, control flow changes (e.g., jumps), and memory access (load and store operations). Below is an in-depth explanation of the execute stage in the Y86-64 processor, detailing its functions, components, control flow, and how it integrates with the rest of the pipeline.

1. Overview of the Execute Stage

In the Y86-64 processor, the **execute stage** follows the decode stage. Its primary responsibility is to perform the operations dictated by the decoded instruction. The instruction itself can involve operations such as arithmetic calculations (e.g., addition or subtraction), logical operations (e.g., AND, OR), memory address computations (e.g., for loading or storing data), or control flow changes (e.g., jumps or branches).

The execute stage is essentially where the "work" of each instruction is done, but it also includes handling certain types of instructions such as control flow operations (branching) and preparing for memory operations (load and store). It interacts closely with the Arithmetic Logic Unit (ALU) and other execution units, such as the memory access unit and branch unit.

2. Key Components of the Execute Stage

- **Arithmetic and Logic Unit (ALU)**: The ALU is the heart of the execute stage, performing the majority of operations. It handles arithmetic operations (addition, subtraction, multiplication) and logical operations (AND, OR, XOR, NOT). It also handles comparison operations (e.g., checking if two values are equal for branching purposes).
- **Branch Unit**: For instructions that affect the program counter (PC), such as jumps or conditional branches, the branch unit plays an essential role. It evaluates conditions (e.g., whether a specific register holds a certain value) and calculates the target address for jump instructions.
- **Memory Address Calculation Unit**: For memory-related instructions (like load and store), the execute stage computes memory addresses. For example, in an instruction like movq %rax, 100(%rbx), the effective memory address is calculated by adding the value in the rbx register with an offset of 100.
- **Immediate Value Handling**: Some instructions involve immediate values (constants embedded within the instruction). In this case, the execute stage handles the immediate values, either as operands for arithmetic/logic operations or as part of address computation for memory operations.

3. Operations in the Execute Stage

- **Arithmetic and Logical Operations**: The Y86-64 processor supports a range of arithmetic and logical operations, which are executed in the ALU. These include:

When an arithmetic or logical instruction is decoded, the operands (which might be immediate values or data from registers) are sent to the ALU. The ALU performs the operation and prepares the result, which is then forwarded to the next stage for potential writing back to the register file or memory.

- **Branching**: In the case of control flow instructions, the execute stage calculates the target address for jumps and branches. For conditional branches (e.g., jz, jne), the execute stage evaluates the condition (such as checking if a register contains zero) and determines if the branch should be taken. If a branch is taken, the program counter is updated accordingly.

For example, in a conditional jump, if the condition is met (e.g., the zero flag is set after a comparison), the branch unit will provide the address of the next instruction to execute. Otherwise, the flow continues with the next sequential instruction.

- **Memory Address Calculation**: In memory-related instructions like movq, pushq, and popq, the execute stage calculates the effective memory address by adding the base register and an immediate offset. This address calculation is critical for load and store operations.

For example, in the instruction movq %rax, 100(%rbx), the address of the memory location is computed by adding the contents of the rbx register with the immediate value 100. This calculated address is passed to the memory access stage.

- **Immediate Values**: Some instructions, like addq or subq, use immediate values as operands. These immediate values are extracted from the instruction during the decode stage, and in the execute stage, they are used directly in the ALU. For example, an instruction like addq $5, %rax will add the immediate value 5 to the value stored in the rax register.

5. Memory Access Preparation

While memory access occurs in the subsequent memory stage, the execute stage prepares data for memory operations. For a load instruction, the execute stage calculates the memory address, while for a store instruction, it sends data to the memory stage along with the address computed.

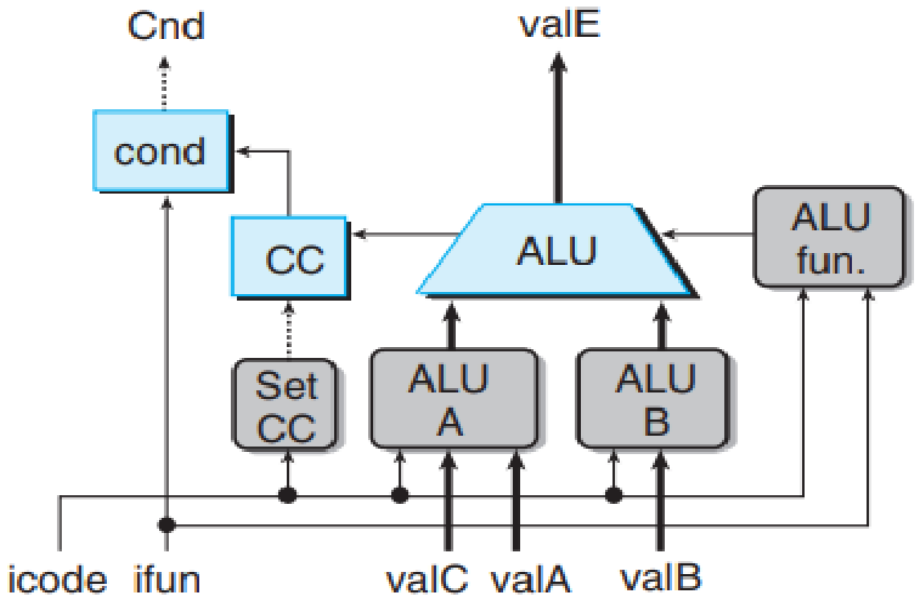
- **Load Operations**: For instructions like movq %rax, (%rbx), the execute stage calculates the effective address by adding the value in rbx to an immediate offset. This address is passed along to the memory stage, where the data will be loaded into the specified register.
- **Store Operations**: For instructions like movq (%rbx), %rax, the execute stage computes the memory address and prepares the value in the register (%rbx) to be written to memory. The memory stage then performs the actual store.

EXECUTE MODULE DECLARATION :

```
 2 module execute(valE,cnd,cf_out,icode,ifun,valC,valA,valB,cf_in);
 3
 4   output reg [63:0] valE;
 5   output reg cnd;
 6   output reg [2:0] cf_out;
 7
 8   input [3:0] icode,ifun;
 9   input [63:0] valC,valA,valB;
10   input [2:0] cf_in;
11
```

ALU MODULE DECLARATION :

```
 2 module execute(valE,cnd,cf_out,icode,ifun,valC,valA,valB,cf_in);
 3
 4   output reg [63:0] valE;
 5   output reg cnd;
 6   output reg [2:0] cf_out;
 7
 8   input [3:0] icode,ifun;
 9   input [63:0] valC,valA,valB;
10   input [2:0] cf_in;
11
```



4.MEMORY

The **memory stage** in the Y86-64 processor is responsible for memory-related operations, including loading data from memory into registers and storing data from registers into memory. It follows the execute stage in the pipeline and is critical for handling instructions that involve memory access. This stage typically handles **load** and **store** instructions, and it also interacts with the register file and the data memory to either read or write data as dictated by the instruction.

In the Y86-64 architecture, memory operations are treated separately from computation operations, allowing for greater flexibility and simpler control mechanisms. The memory stage is relatively straightforward compared to the more complex execute stage but plays a key role in ensuring that the processor handles data correctly, especially for programs that involve frequent memory operations.

1. Overview of the Memory Stage

The memory stage in a pipeline is responsible for performing the actual memory access, either reading data from memory (for **load** instructions) or writing data to memory (for **store** instructions). In the Y86-64 processor, this stage comes after the execute stage and handles the results of address calculations, which were previously computed by the execute stage.

The memory stage performs the following key operations:

- **Load**: Data is fetched from memory based on an address, which was calculated in the execute stage.
- **Store**: Data from a register is written to memory at an address calculated in the execute stage.
- **Memory Address Calculation**: The memory stage may receive the effective address for a memory operation and perform the necessary read/write.

2. Memory Operations in Y86-64

There are two main types of memory operations in Y86-64:

- **Load Operations**: These involve reading data from memory into a register. A load instruction takes an address, retrieves data from that address, and stores the data into a register.
- **Store Operations**: These involve writing data from a register into memory. A store instruction specifies a register that holds the data to be written and an address where the data should be stored.

Example Load Operation:

- **Instruction**: movq 100(%rbx), %rax

- **Function**: The address is calculated by adding the value in register %rbx with an offset of 100. The value at this address in memory is then loaded into %rax.

Example Store Operation:

- **Instruction**: movq %rax, 100(%rbx)
- **Function**: The value in register %rax is stored into memory at the address calculated by adding the value in %rbx to an offset of 100. **3. Steps in the Memory Stage**

Load Instructions:

1. **Address Calculation**: The effective address for a load instruction is calculated in the execute stage, as mentioned earlier. This address is passed to the memory stage to access the correct memory location.
2. **Memory Access**: In the memory stage, the processor performs a memory read at the effective address. This involves fetching data from the data memory (or cache, if implemented) at the computed address.
3. **Load Data**: The data fetched from memory is loaded into the target register specified by the instruction. For example, in the instruction movq 100(%rbx), %rax, the value at memory address 100 + %rbx is loaded into %rax.

Store Instructions:

1. **Address Calculation**: As with load instructions, the address for a store instruction is calculated in the execute stage and passed to the memory stage.
2. **Data Fetch**: The data to be stored is retrieved from the register specified by the instruction (e.g., %rax in movq %rax, 100(%rbx)).
3. **Memory Write**: The fetched data is written into memory at the effective address.

3. Memory Address Calculation

In both load and store instructions, the memory stage relies on an address that was computed earlier in the pipeline, typically in the execute stage. This address calculation involves adding an offset (which could be an immediate value embedded in the instruction) to a base address stored in a register. The result is the effective memory address used to access memory.

Example Address Calculation for Load:

- **Instruction**: movq 200(%rbx), %rax
- **Address Calculation**: The effective address is the sum of the value in the %rbx register and the immediate offset 200. This address is used to fetch the data from memory.

Example Address Calculation for Store:

- **Instruction**: movq %rax, 100(%rbx)
- **Address Calculation**: The effective address is the value in %rbx plus the immediate offset 100. The value in %rax is stored at this address.

4. Memory Access Cycle3

In a basic implementation of the Y86-64 processor, the memory stage involves interacting with a memory system (such as the data cache or main memory). The processor must perform the following steps to access data:

- **Memory Read for Load**: The memory read operation fetches data from the specified memory address.
- **Memory Write for Store**: The memory write operation places the data into the specified memory location.

In a pipelined processor, multiple memory operations may be ongoing at the same time, but they still need to be managed carefully to avoid conflicts or hazards.

5. Interaction with the Data Memory

In real processors, the memory is often divided into levels (L1, L2, and L3 caches, as well as main memory). For educational purposes, the Y86-64 processor typically assumes a simple memory model where data is accessed from a flat memory address space. However, in more complex architectures, caching mechanisms would be involved to speed up memory access. Here's how the memory stage interacts with these different levels:

- **Cache Access**: If the processor employs a cache, the memory stage would first check if the required data is available in the cache (specifically the data cache). If it is, the processor performs a cache hit, and the data is quickly retrieved.
- **Main Memory Access**: If the data is not found in the cache (a cache miss), the memory stage would need to fetch the data from the main memory, which takes longer.

9. Exceptions and Interrupts in the Memory Stage

Exceptions can also occur during the memory stage, especially in the context of invalid memory accesses. Common exceptions in the memory stage include:

- **Segmentation Faults**: These occur if an instruction attempts to access memory that it is not allowed to (e.g., accessing an invalid address or violating memory protection rules).

This is done as:

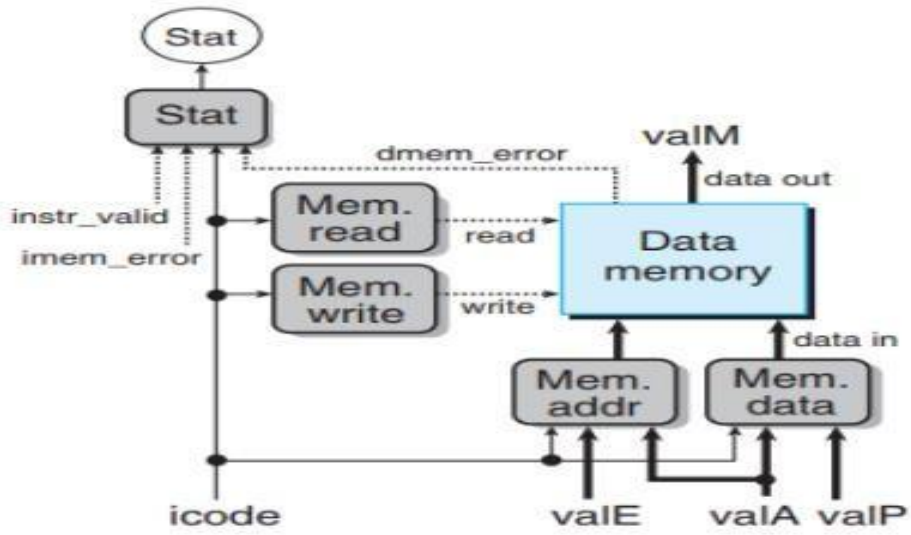
```
data_mem[valA] = 8'd200; //for pop ooperation.
data mem[valE] = 8'd100;
```

Display statement:

```
always@(data_mem[valE])
  $display("mem allocated->%b",data mem[valE]);
```

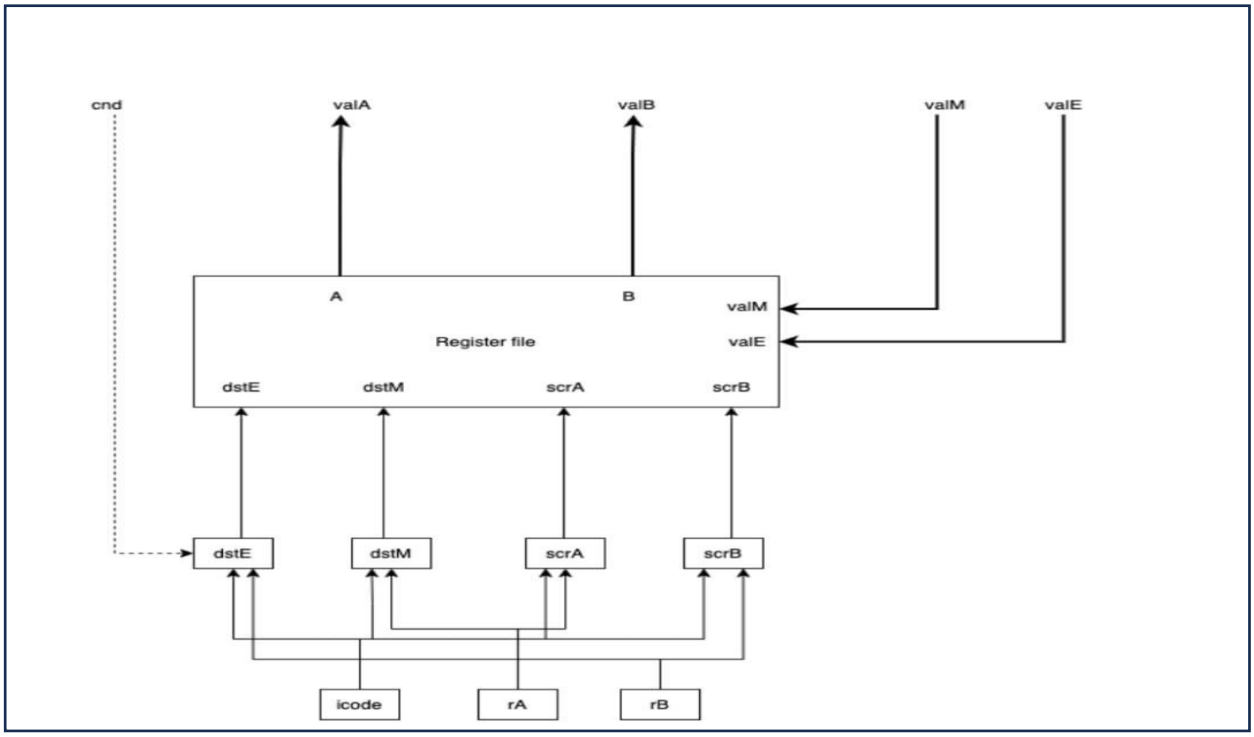
Memory module declaration

```
3 module memory(
4   clk,icode,valA,valE,valP,valM
5 );
6
7   input clk;
8
9   input [3:0] icode;
10  input [63:0] valA;
11  input [63:0] valE;
12  input [63:0] valP;//next instr in row
13
14  output reg [63:0] valM;
15  output reg [63:0] datamem;
16
17  reg [7:0] data_mem[0:1023];
18
```



Figure

5. Write back



The **write-back stage** in the Y86-64 processor pipeline is the final stage where the results of executed instructions are written back into the register file or memory. It follows the memory stage and is crucial for updating the processor's internal state, which is required for the correct execution of future instructions. In a pipelined processor like Y86-64, the write-back stage is responsible for completing the cycle of data flow, where the outcomes of arithmetic operations, load operations, and other computational tasks are saved into registers for future use. This stage also handles forwarding values that may need to be used immediately in subsequent instructions.

1. Overview of the Write-Back Stage

The write-back stage is responsible for the final update to the register file or memory based on the results produced by previous pipeline stages. Specifically, this stage is tasked with:

- Writing results to the **register file** from arithmetic operations and load instructions.
- Handling **memory write-back** when necessary.

Passing data along for any future instructions that depend on these results.

In most processors, the write-back stage serves as a crucial point where the internal state of the processor is updated, which affects the execution of later instructions.

2. Types of Instructions that Involve Write-Back

Not all instructions require the write-back stage, but the following types of instructions will:

- **Arithmetic and Logical Operations**: Instructions like addq, subq, andq, orq, and other operations that perform arithmetic or logic on register values will write their results back to the register file.
- **Load Instructions**: The results of load instructions are written into registers. For instance, in the instruction movq 100(%rbx), %rax, the value loaded from memory is written back into the %rax register.
- **Other Operations**: Instructions like jmp or call might not write to the register file, but they could affect the program counter (PC) and require updating control registers or flags.

In the case of **store** operations, the memory stage handles the writing to memory, so the write-back stage doesn't need to deal with those.

3. Steps in the Write-Back Stage

The main task of the write-back stage is to transfer the results of executed instructions into registers, where they can be used by later instructions. Here's a breakdown of the typical process:

1. **Receiving Results**: The write-back stage receives results from previous stages (either from the memory stage for load operations or from the execute stage for arithmetic/logic operations).
2. **Writing to Registers**: If the instruction modifies a register, the result from the ALU or memory is written into the destination register. For example:
    - In addq %rax, %rbx, the result of the addition is written back to %rbx.
    - In a load instruction like movq 100(%rbx), %rax, the value retrieved from memory is written into %rax.
3. **Handling Immediate Values**: Some instructions may also involve writing immediate values to registers. For example, an instruction like movq $5, %rax would place the immediate value 5 into %rax during the write-back stage.
4. **Program Counter Update**: While the write-back stage generally deals with register updates, certain instructions, like jmp (jump), may modify the program counter, causing a change in control flow. This update happens when necessary, and the new program counter is passed on for fetching the next instruction.

4. Write-Back and Register File

The register file is a crucial component of the write-back stage. It stores the values of general-purpose registers that are used and modified by instructions. In the Y86-64 processor, the register file typically consists of 16 registers (%rax, %rbx, ..., %r15) that can hold 64-bit values.

Process for Writing to the Register File:

- Each instruction that results in a register update has a designated destination register.

- After the execution stage or memory stage processes the instruction, the result is sent to the writeback stage.

After an arithmetic operation like addq %rax, %rbx, the result is written to %rbx.

- After a load instruction like movq 100(%rbx), %rax, the result (value loaded from memory) is written to %rax.

5. Write-Back for Load Instructions

For **load instructions**, the write-back stage is where the data fetched from memory is transferred into a register. The data load operation happens in the memory stage, but the final transfer to the register is done in the write-back stage.

Example:

- **Instruction**: movq 100(%rbx), %rax ○ In the **memory stage**, the value at the address 100 + %rbx is fetched from memory.
  - In the **write-back stage**, this value is written into the %rax register.

The write-back stage is responsible for ensuring that the register file reflects the correct state after a load operation.

6. Write-Back for Arithmetic/Logical Operations

Arithmetic and logical operations performed in the execute stage produce results that need to be written back to the register file. For example, when an addq or subq instruction is executed, the result is stored in the destination register specified by the instruction.

Example:

- **Instruction**: addq %rax, %rbx ○ In the **execute stage**, the sum of %rax and %rbx is computed.
  - In the **write-back stage**, the result is written back into %rbx.

Similarly, logical operations like andq, orq, and xorq also use the write-back stage to store their results into the appropriate registers.

7. Forwarding and Write-Back

In a pipelined processor, forwarding (or bypassing) is essential to avoid data hazards. Forwarding allows the processor to send data directly from one pipeline stage to another without having to wait for the result to be written to the register file first.

In the context of the write-back stage:

If an instruction depends on a value produced by another instruction that hasn't yet been written back to the register file, the processor may forward the result directly from the execute stage or memory stage to the input of the dependent instruction.

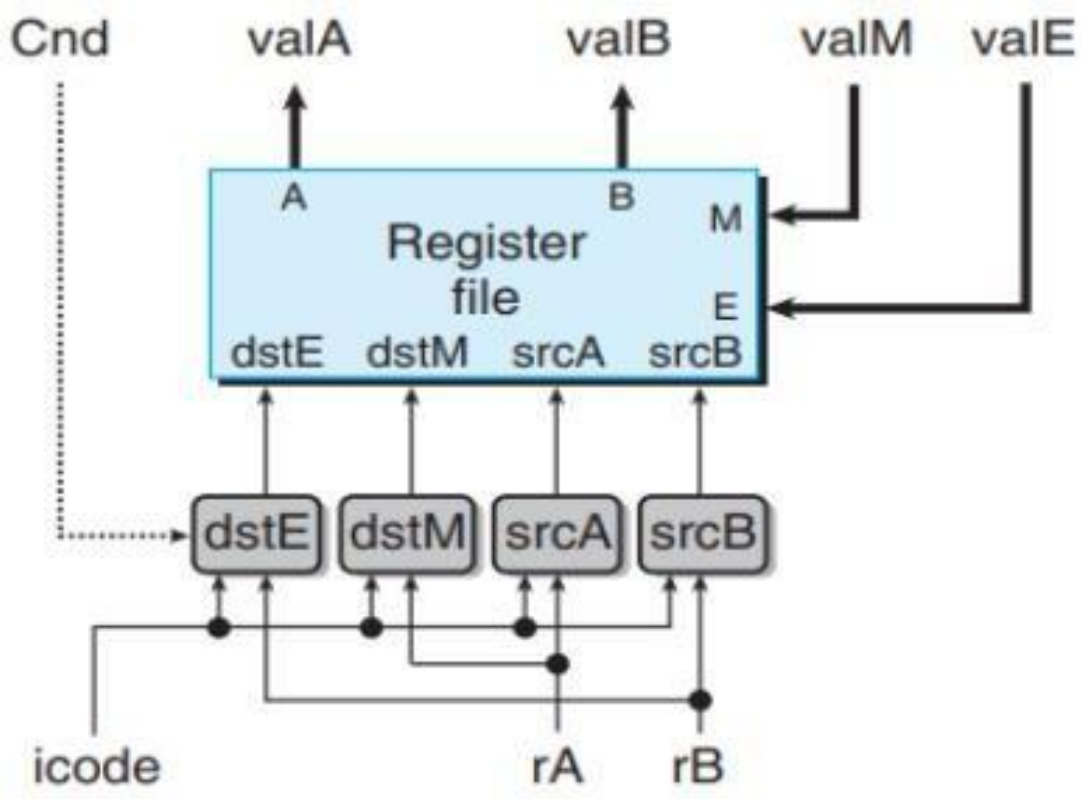
- This ensures that data is available when needed without waiting for the write-back to complete.

8. Exceptions and Interrupts in the Write-Back Stage

The write-back stage is generally the final step in handling an instruction. However, exceptions or interrupts can occur during this stage, which would prevent a value from being written back to the register file or memory. Common exceptions in the write-back stage include:

- **Invalid Write**: If the processor attempts to write to an invalid or protected register, an exception may be raised.
- **Memory Access Violations**: If an issue arises during the write-back of data (e.g., trying to write to a non-existent address or accessing a restricted memory area), an exception may occur.

When exceptions or interrupts are raised during write-back, the processor will typically trigger an exception handler, which may involve saving the state and handling the fault condition before resuming normal execution



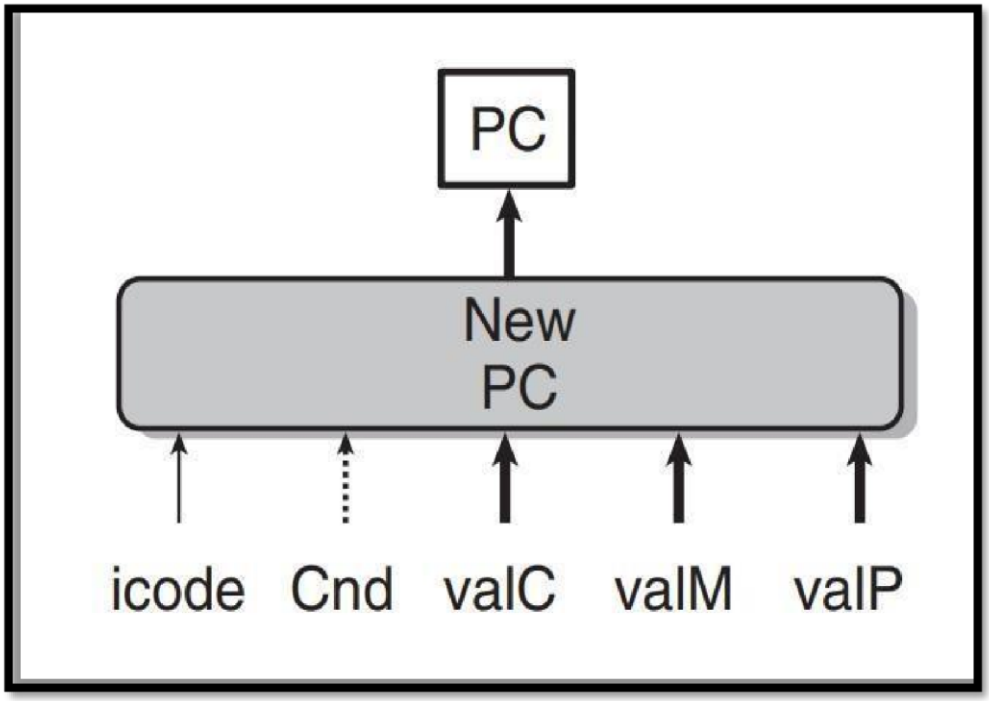
Writeback module declaration:

```
module write_back(clk,icode,ifun,rA,rB,valA,valB,valE,valM,
reg_in0,reg_in1,reg_in2,reg_in3,reg_in4,reg_in5,reg_in6,reg_in7,reg_in8,reg_in9,reg_in10,reg_in11,reg_in12,reg_in13,reg_in14,
reg_out0,reg_out1,reg_out2,reg_out3,reg_out4,reg_out5,reg_out6,reg_out7,reg_out8,reg_out9,reg_out10,reg_out11,reg_out12,reg_out13,reg_out14
);

input clk;
input [3:0] icode,ifun,rA,rB;
input [63:0] valA,valB,valE,valM;
input [63:0] reg_in0,reg_in1,reg_in2,reg_in3,reg_in4,reg_in5,reg_in6,reg_in7,reg_in8,reg_in9,reg_in10,reg_in11,reg_in12,reg_in13,reg_in14;
output[63:0]
  reg_out0,reg_out1,reg_out2,reg_out3,reg_out4,reg_out5,reg_out6,reg_out7,reg_out8,reg_out9,reg_out10,reg_out11,reg_out12,reg_out13,reg_out14;
reg [63:0] reg_file [0:14];


```

6.PC update



The **PC Update Stage** in the Y86-64 processor is a crucial part of the instruction execution pipeline. It is responsible for updating the **Program Counter (PC)**, which points to the memory address of the next instruction to be executed. The PC Update stage ensures that instructions are fetched in the correct sequence, except when control flow is altered by instructions like **branches**, **jumps**, **calls**, and **returns**. This stage is vital for maintaining the flow of program execution and ensuring that the correct instructions are fetched at each clock cycle.

1. Overview of the PC Update Stage

•

The Program Counter (PC) is a special register in the CPU that holds the address of the next instruction to be executed. The primary role of the PC Update stage is to modify the PC according to the behavior of the instruction currently being executed. In a pipeline, this stage occurs after the execute stage and sometimes interacts with both the execute and memory stages to adjust the program counter when necessary.

The main tasks in the PC Update stage include:

- **Sequential Execution**: In most cases, the next instruction is fetched sequentially, which means the PC is simply incremented by the size of the instruction (usually 8 bytes for Y8664).
- **Branching and Control Flow Changes**: For control flow instructions such as jumps, branches, calls, or returns, the PC is updated based on the instruction's behavior (such as jumping to a new address or returning from a function).
- **Exception Handling**: If an exception or interrupt occurs, the PC must be updated to point to the appropriate handler.

2. Types of Instructions That Modify the PC

There are several types of instructions in Y86-64 that modify the program counter: **a.**

Sequential Execution:

- **Normal Instructions**: The typical instruction increments the program counter by the size of the instruction (usually 8 bytes). For example, after the current instruction is fetched, the PC is updated to point to the next instruction in memory.
- **Example**:
    - Instruction: addq %rax, %rbx
    - After execution, the PC is incremented by 8 (the size of the addq instruction), pointing to the next instruction.

b. Branching Instructions:

- **Conditional Jumps**: Instructions like jmp and je (jump and jump if equal) cause the PC to change based on the result of a condition. If the condition is met, the PC is set to a new address.
- **Unconditional Jumps**: Instructions like jmp directly set the PC to a new value, irrespective of any condition.
- **Example**:
    - Instruction: jmp label
    - The PC is updated to the address of label (which could be a label defined elsewhere in the program).

•

c. Calls and Returns:

- **Call Instructions**: The call instruction is used for function calls. It saves the current PC (i.e., the address of the instruction following the call) to the stack and then updates the PC to the address of the function being called.
- **Return Instructions**: The ret instruction retrieves the saved return address from the stack and loads it into the PC, so the execution continues after the function call.
- **Example**:
    - Instruction: call my_function
    - The address of my_function is loaded into the PC, and the return address (the next instruction after call) is saved on the stack.

d. Branch and Link Instructions:

- **Linking Instructions**: These include the call instruction which saves the address of the next instruction (the return address) into the stack before jumping to the target function.
- **Return Address Loading**: The ret instruction pops the saved return address from the stack and sets the PC to that address, effectively returning to the calling function.

3. Handling Sequential Execution in the PC Update Stage

In the majority of cases, after an instruction is executed, the next instruction to be fetched is the instruction immediately following the current one. In the Y86-64 processor, this is done by incrementing the PC by the size of the instruction, typically 8 bytes.

- **Normal Instruction Execution**: If the instruction does not modify the PC (i.e., it is not a branch, jump, or call), the PC is simply incremented to the next instruction address.
- **Example**:
    - Instruction: movq %rax, %rbx ○ The address of the next instruction is simply

      the current PC plus 8.

4. Handling Branches and Jumps in the PC Update Stage

Branch and jump instructions require more complex updates to the PC. These instructions change the program's flow based on conditions or unconditionally, and the PC is modified to point to the target address.

a. Unconditional Jumps:

For unconditional jump instructions (like jmp), the PC is set to the target address specified by the instruction. This means that the next instruction executed will be at the new target address, and normal sequential execution is bypassed.

- **Example**:
    - Instruction: jmp 0x1000 ○ The PC is directly set to 0x1000, and execution continues from there. **b. Conditional Jumps:**

- Conditional jump instructions (like je, jne, jg, etc.) update the PC if a certain condition is met, usually based on flags (such as zero, carry, or sign flags) set by previous instructions.

- **Example**:
    - Instruction: je 0x1000
    - The PC is set to 0x1000 if the condition specified (e.g., if the Zero flag is set) is true. If the condition is not met, the PC is incremented normally to the next sequential address.

c. Branch Prediction:

- While not explicitly a feature of the basic Y86-64 processor, in real-world processors, branch prediction helps anticipate the target of a jump or branch. This speeds up the execution of programs by reducing the delay associated with branches. However, in Y8664, branches are generally resolved during execution, and the PC is updated accordingly.

5. Call and Return Instructions in the PC Update Stage

The **call** and **return** instructions involve significant changes to the PC and require additional handling. These instructions not only change the flow of control but also deal with saving and restoring the return address. **a. Call Instruction:**

The ret instruction loads the return address from the stack and sets the PC to that address, causing the processor to return to the location of the instruction following the original call.

- **Example**:
    - Instruction: ret
    - The PC is updated to the value popped from the stack, which is the return address saved during the call.

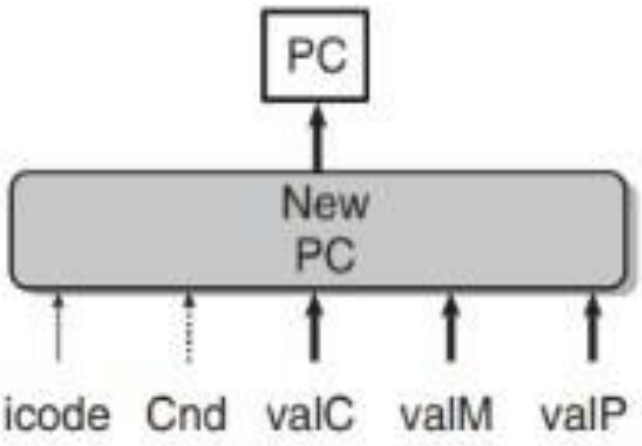
```
module pcupdate(clk,icode,cnd,valC,valM,valP,pcnxt);

input [3:0] icode;
input cnd,clk;
input [63:0] valC,valM,valP;
output reg [63:0] pcnxt;
```

Working of sequential implementation:

Execution of following instruction is shown below:

cmov0 1 3
irmov F 2 17
rmmov 5 2 1
mrmov 7 0 1 opq 0
2 3
cmov 3 4
cmovge 5 3



Testbench instructions:

```
  //cmovxx
instr_mem[0]=8'b00010000;
  instr_mem[1]=8'b00100000; //2 fn
  instr_mem[2]=8'b00010011; //rA rB **/

//irmovq
  instr_mem[3]=8'b00110000; //3 0
  instr_mem[4]=8'b00000010; //F rB
  instr_mem[5]=8'b00000000; //V
  instr_mem[6]=8'b00000000; //V
  instr_mem[7]=8'b00000000; //V
  instr_mem[8]=8'b00000000; //V
  instr_mem[9]=8'b00000000; //V
  instr_mem[10]=8'b00000000; //V
  instr_mem[11]=8'b00000000; //V
  instr_mem[12]=8'b00010001; //V=17

//rmmovq
  instr_mem[13]=8'b01000000; //4 0
  instr_mem[14]=8'b01010010; //rA rB
  instr_mem[15]=8'b00000000; //D
  instr_mem[16]=8'b00000000; //D
  instr_mem[17]=8'b00000000; //D
  instr_mem[18]=8'b00000000; //D
  instr_mem[19]=8'b00000000; //D
  instr_mem[20]=8'b00000000; //D
  instr_mem[21]=8'b00000000; //D
  instr_mem[22]=8'b00000001; //D

//mrmovq
  instr_mem[23]=8'b01010000; //5 0
  instr_mem[24]=8'b01110000; //rA rB
  instr_mem[25]=8'b00000000; //D
  instr_mem[26]=8'b00000000; //D
  instr_mem[27]=8'b00000000; //D
  instr_mem[28]=8'b00000000; //D
  instr_mem[29]=8'b00000000; //D
  instr_mem[30]=8'b00000000; //D
  instr_mem[31]=8'b00000000; //D
  instr_mem[32]=8'b00000001; //D
```

CHAPTER 5

7.Results

```
test_bench.v:415: $finish called at 75000 (1ps)
mem_allocated->01100100
                75
clk:1
rA: 5 rB: 3 icode: 0 ifun: 0 valC:                1 valP:               40 mem_error:0
 valA:               5 valB:                0
cf_in:0 valE:                0 cnd:0 cf_out:0
valM:              100
r0:              0
r1:              1
 r2:             17
 r3:              5
 r4:             18
 r5:              5
 r6:              6
 r7:            100
 r8:              8
 r9:              9
 r10:             10
 r11:             11
 r12:             12
 r13:             13
 r14:             14
PC:              39
```

CHAPTER 6

FUTURE SCOPE:

The Y86-64 processor, a simplified model for educational purposes, lays the foundation for exploring key concepts of modern processor design. However, there are several areas where enhancements and optimizations can be made to improve performance, functionality, and efficiency. Below are the potential future scopes for extending and evolving the Y86-64 processor:

1. Pipeline Enhancements

- **Superscalar Architecture:**
  - The Y86-64 processor uses a simple 6-stage pipeline. A natural extension would be to implement superscalar architecture, where multiple instructions are executed in parallel in the pipeline. This would allow for higher instruction throughput and better utilization of available resources, especially in the Execute (EX) and Memory Access (MEM) stages.
- **Out-of-Order Execution**:
  - Implementing out-of-order execution allows the processor to continue executing independent instructions while waiting for data or resolving dependencies. This would significantly improve performance, especially in complex workloads.
- **Deep Pipelines:**
  - The current 6-stage pipeline could be extended to more stages (e.g., 8 or 10 stages), which can allow for higher clock speeds and more fine-grained control over instruction processing. However, this comes with the challenge of managing increased complexity and potential delays from pipeline stalls.

2. Improvement of Hazard Handling

- **Data Forwarding/Bypassing:**
  - Currently, the Y86-64 processor may experience data hazards due to dependencies between instructions. Implementing data forwarding or bypassing will reduce the need for pipeline stalls by forwarding data directly from later stages to earlier stages without writing it back to the register file.
- **Branch Prediction:**
  - Branch hazards can cause delays in the pipeline, especially when branch instructions like jmp or beq are encountered. The implementation of branch prediction (static or dynamic) can help predict the outcome of a branch instruction and avoid pipeline flushing, leading to more efficient execution.
- **Speculative Execution:**
  - A speculative execution mechanism can be implemented to predict the path of branch instructions before they are resolved. If the prediction is correct, the processor can continue execution without waiting for the branch resolution. If the prediction is wrong, the processor can discard the speculative execution and fetch the correct instruction.

3. Memory Management Improvements

- Cache Implementation:
  - In the Y86-64 processor, memory access is handled directly. To improve performance, an on-chip cache (L1, L2 cache) can be implemented to reduce the latency of memory accesses. This would reduce the time spent on memory operations, which are typically slower than register accesses.
- **Memory Management Unit (MMU):**
  - Implementing an MMU would allow the processor to support virtual memory and paging, which would enable it to run more complex programs that require memory protection and larger address spaces.

4. Instruction Set Architecture (ISA) Extension

- **New Instructions:**
  - The current set of instructions in the Y86-64 is minimal for simplicity. There is scope to extend the instruction set by adding more complex operations like:
    - Floating-point operations (e.g., addf, subf).
    - Advanced string or vector operations for multimedia and signal processing tasks.
    - Atomic instructions for multithreading and parallel processing.
- **Support for Multithreading:**
  - To enable efficient multitasking, the processor can be extended with instructions for thread synchronization (e.g., lock, sync) or atomic operations to improve the performance of multi-core processors or multi-threaded applications.

5. Multi-Core Processor Design

- The Y86-64 processor can be extended to a multi-core design, where multiple instances of the processor run in parallel. This can help handle more computational tasks simultaneously, offering better performance for tasks like parallel processing, multitasking, and high-performance computing.
- Multi-core processors would require modifications to the cache coherence protocol (e.g., MESI) and an efficient way to communicate between cores (e.g., using a bus or network-on-chip).

6. Energy Efficiency and Low-Power Design

- With the increase in the complexity of processors, energy consumption has become a major concern, especially in mobile and embedded systems. The Y86-64 processor can be modified to implement dynamic voltage and frequency scaling (DVFS) or power gating to reduce power consumption during low-activity periods.
- Low-power design techniques can be implemented, such as reducing the clock frequency in idle states or optimizing the pipeline for low-energy consumption without sacrificing performance.

CHAPTER 7

Conclusion:

The Y86 processor is a simplified educational tool designed to teach fundamental concepts of computer architecture, including instruction set design, pipelining, and microarchitecture. Its reduced complexity allows learners to focus on core principles like instruction execution, data and control hazards, and pipeline performance. Through hands-on experience, students gain insights into design trade-offs, debugging, and optimization at the assembly level. Overall, the Y86 serves as a practical platform for building a strong foundation in processor design and operation.

The Y86-64 processor architecture is an invaluable educational framework that simplifies the complexities of modern x86-64 systems, making it accessible for learning and exploration. By maintaining a balance between functionality and simplicity, it provides a clear understanding of key processor design concepts, such as instruction sets, control flow.

Key Takeaways:

1. **Instruction Set Design:**
    - The streamlined instruction set emphasizes fundamental operations, enabling learners to understand the building blocks of assembly programming and processor operation.
2. **Microarchitecture Implementation:**
    - Sequential and pipelined designs allow for step-by-step exploration of how processors handle instruction execution, from basic fetch-decode-execute cycles to overlapping stages in a pipeline.
    - The introduction of control and data hazard resolution mechanisms showcases the engineering challenges and solutions in modern processor design.
3. **Performance Insights:**
    - The contrast between sequential and pipelined implementations highlights the impact of architectural enhancements, like pipelining, on performance metrics such as throughput and cycles per instruction (CPI).
    - Practical simulations provide hands-on experience with real-world performance trade-offs.
4. **Educational Impact:**

- Y86-64 bridges the gap between theoretical instruction and practical application, equipping students with a foundational understanding of how real-world processors operate.
- It encourages critical thinking about design trade-offs, including complexity, cost, and performance.

5. **Preparation for Advanced Topics:**
    - The concepts learned through Y86-64 prepare learners to delve deeper into advanced computer architecture topics, such as out-of-order execution, branch prediction, and memory hierarchy.

REFERENCES:

BOOKS

1. **computer organisation and architecture** by smruti ranjan sarangi.
2. **Computer Systems A Programmer's Perspective**, Author :Randal E. Bryant (Carnegie Mellon University), David R. O'Hallaron (Carnegie Mellon University).
3. **"Computer Organization and Design: The Hardware/Software Interface"** by David A. Patterson and John L. Hennessy
4. **"Computer Architecture: A Quantitative Approach"** by John L. Hennessy and David A. Patterson
5. **"Digital Design and Computer Architecture"** by David Money Harris and Sarah L. Harris
6. **"Structured Computer Organization"** by Andrew S. Tanenbaum
7. **"Introduction to Computing Systems: From Bits and Gates to C and Beyond"** by Yale N. Patt and Sanjay Patel

WEBSITES

Y86-64 Processor Description (from the University of Texas)

- https://www.ece.utexas.edu/~pattis/ue/y86/y86-64.pdf

Digital Design Resources - Verilog Tutorials

- https://www.asic-world.com/

RESEARCH PAPERS:

1. "A Study of Processor Architectures: The Y86 and Y86-64"
2. "Design and Implementation of a 32-bit Microprocessor in Verilog"
3. **"The Y86-64 Simulator and Processor Design"** by Bill Roscoe
4. "Improvement of Processor Performance Using Superscalar Architecture"
5. "An Analysis of Pipelining in Computer Architecture"
6. "Design of an Optimized Processor with Branch Prediction and Out-of-Order Execution"

ADDITIONAL RESOURCES

Google Scholar: Search for research papers related to the Y86-64 processor, pipeline optimization, Verilog implementations, and microprocessor design.

- https://scholar.google.com

IEEE Xplore Digital Library: Explore articles and research papers on processor architectures, including pipeline designs and processor optimizations.

- https://ieeexplore.ieee.org

ACM Digital Library: Another repository for academic papers, including those on microprocessor design and architecture.

- https://dl.acm.org