Lehrstuhl für Schaltungsentwurf

Technische Universität München

Prof. Dr. rer. nat. Franz Kreupl

CMOS Analog Circuit Design Lab
Final Report

January 31, 2020

Group: analog4
Authors:

- Muhammad Farhan: 03708828
- Armaghan Saleem: 03709824

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1 Abstract

A Band-gap voltage reference circuit maintains same level of voltage irrespective of the temperature or supply voltage variations present. In this report, we will implement voltage reference circuit with Kuijk topology and further ensure its proper working by trying to approach the desired benchmark ranges of performance parameters as closely as possible. The entire setup will be designed first with ideal Op-amp and characterized Transistors, and then subsequently moving to real Op-Amp while optimizing Gain, Power Supply Rejection Ratio, Common Mode Rejection Ratio and Power Consumption.

2 Introduction

2.1 Motivation

A Band-gap voltage reference is a circuit used for providing a consistent reference voltage for the subsequent design of analog components. Reference voltages are important in ICs, for example, for generating reference currents that are used to bias amplifier stages.

The circuit is designed to withstand not only the changes in temperature but also show robustness in power supply rejection ratio (a measure of immunity of output to the abrupt changes in power supply) which should ideally approach infinity whereas also taking into account the common mode rejection ratio (a measure of amplification of small signal common to both terminal of Op-Amp) which should ideally approach zero while at the same time keeping the power consumption as minimum as possible. Simple circuits like use of Zener diode or a single biased transistors lack the ability to work as a reference signal owing to large variation which occurs in the their bias point owing to supply fluctuations or temperature changes. Hence most Band-gap circuits works by using two voltage that have opposite temperature coefficients, and add them to cancel out the overall temperature dependence and make up for the sudden changes in bias voltages.

In this lab, we will implement a band-gap reference circuit based on Kujik topology using two stage Op-Amp and Bipolar Junction transistors with opposite temperature coefficients to annul the impact of temperature changes and further measure the effectiveness of the scheme by tests to determine Power Supply Rejection Ratio, Common Mode Rejection Ratio, Settling Behaviour of reference temperature and the stability behaviour of the system. All these steps would be performed for the case of using an ideal Operational amplifier and then implementing circuit with real two-stage CMOS amplifier with tests modelling real-life scenario as will be discussed in task description. The design parameters to be followed are given in the table

Specification	**Condition**	**Note**
V_{DD}	$1.8\,\mathrm{V}$	positive supply voltage
V_{SS}	$0\,\mathrm{V}$	negative supply voltage
V_{ref}	$1.2\,\mathrm{V}$	reference voltage
PSRR	$\geq 80\,\mathrm{dB}$	power supply rejection ratio
TC(V_{ref})	$\leq 30\,\mu\mathrm{V\,K^{-1}}$	temperature coefficient
P	minimize	($\leq 100\,\mu\mathrm{W}$)

Table 1: The specification to be met by the circuit

2.2 Task Description

In this Lab, we will divide our progress and the overall task into four steps or sub-tasks to ensure that the overall designed is tuned and optimized as much as possible. The tasks, their description and chronology is as below:

1 **Parameter Extraction and CMOS Characterization**
In this step, we abstract the physics behind the device and develop an empirical model of a CMOS transistor in its Triode region to be utilized subsequently in the amplifier design. Important model parameters such as oxide thickness, electron mobility, channel length parameter and V_{th} are extracted by both graphical and numerical techniques using the large signal model of amplifier which is linearized in Triode region using linear regression. The linear model developed is then compared with the simulated one in Cadence.

2 **Topology Selection and Exploration of alternatives**
In this step, we describe and develop the topology (Kuijk in our case) for the Band-gap reference circuit to be used later in the design. We will further view some alternative designs to show their shortcomings and in-applicability when being used in pragmatic designs due to lack of consistency or robustness.

3 **Ideal Implementation and Verification with Simulator**
In this step, we will carry-out an idealized analysis of the Band-gap circuit (by assuming that the operational amplifier is ideal) to gauge out the robustness and correctness of our topology. The behaviour studied will include the PSRR (Power Supply Rejection Ratio) of the reference circuit, temperature dependence of the circuit alongside varying supply voltage, as well as the settling time of the ideal Op-Amp output voltage V_{ref}.

4 **Real Implementation and Verification with Simulator**
In this step, a complete real-life scenario is constructed so as to model the behaviour of circuit in real-life. A two-stage CMOS based operational amplifier is constructed and its evaluation as in previous step is carried out for PSRR, Temperature dependence and settling time. Furthermore, the inconsistencies which are probable during fabrication are also evaluated including the variation in resistance of the design, inherent voltage imbalance between the transistor in first stage of transistor due to process variations, load current variations and the transience in the supply voltage of the setup as it is ramped-up from zero (this also calls for start-up circuit as we will see, to ensure that start-up is smooth and enables circuit to reach right operational point)

3 Parameter Extraction and CMOS Characterization

In order to develop a circuit using a NMOS or a PMOS, it is important to abstract the physics behind the device and develop an empirical model of an amplifier on its linear region to be utilized subsequently in the design. Imporant model parameters must be extracted in order to achieve proper device modelling. Model parameters can be extracted by both graphical and numerical techniques. In this experiment, we will use the voltage- current characteristics of the transistor to first extract its different parameters that play a key role in its operation in the saturation region. Then we develop its linear model based on regression, and compare it to the simulated one.

3.1 Large Signal Model Linearization

The behavior of a transistor is explained by the models developed by abstracting physics, one such model for CMOS is a specified by the Equation 1, which gives the operation of the transistor in the saturation region

$$i_d = K\left(\frac{W_{eff}}{2L_{eff}}\right)(v_{gs} - V_T)^2(1+\lambda_{ds}) \tag{1}$$

In Equation 1 if we assume that vds is small then we can ignore the channel length modulation. Next we take the square root of the entire equation.

$${i_d}^{1/2} = \left(\frac{KW_{eff}}{2L_{eff}}\right)^{1/2} v_{gs} - (\frac{KW_{eff}}{2L_eff})^{1/2} v_{Th} \tag{2}$$

We obtain Equation 2. If we compare Equation 2 to the equation of a straight line $y = mx + b$, we see that

$$y = {i_d}^{1/2}$$

$$m = \left(\frac{KW_{eff}}{2L_{eff}}\right)^{1/2} v_{gs}$$

$$b = \left(\frac{KW_{eff}}{2L_{eff}}\right)^{1/2} v_{Th}$$

Therefore, if we have a curve between $v_{gs} - {i_d}^{1/2}$, we can use the slope of a linearly fitted line in the saturation region to find K, and we can use the y-intercept to find the threshold voltage v_{th}.

In a similar manner, if we now take Equation 1 again and now with the assumption that $v_{\text{ds}} \neq 0$, the equation can be re-written as

$$i_d = {i_d}'\lambda v_{ds} + {i_d}' \tag{3}$$

and again comparing Equation 3 to the equation of a straight line, we have

$$y = i_d$$

$$x = V_{ds}$$

We can use the linear portion of the v_ds-i_d curve to find the value of λ.

3.2 Analysis

Tables 2 and 3 show the value for the parameters K, V_{Th}, and λ for the NMOS and the PMOS transistors respectively. A overview of their trends is given in the following paragraph.

Dimensions	K	V_{th}	λ
L_{min},W_{min}	20.60	0.7570	1.9888
L_{min},$2W_{min}$	30.60	0.7570	3.1617
L_{min},$5W_{min}$	41.20	0.7570	7.8287
$2L_{min}$,W_{min}	28.01	0.5600	0.4736
$2L_{min}$,$2W_{min}$	33.10	0.3272	0.7029
$2L_{min}$,$5W_{min}$	34.42	0.2907	0.6927
$5L_{min}$,W_{min}	32.50	0.5830	0.1481
$5L_{min}$,$2W_{min}$	35.51	0.4270	0.2016
$5L_{min}$,$5W_{min}$	35.54	0.4426	0.1904

Table 2: The table for N-18-MM

Dimensions	K	V_{th}	λ
L_{min}, W_{min}	9.94	0.2200	0.5972
L_{min}, $2W_{min}$	9.16	0.2620	0.7416
L_{min}, $5W_{min}$	8.06	0.3194	0.8356
$2L_{min}$, W_{min}	10.87	0.0305	0.1373
$2L_{min}$, $2W_{min}$	9.649	0.0585	0.1327
$2L_{min}$, $5W_{min}$	8.343	0.122	0.1361
$5L_{min}$, W_{min}	12.000	0.0062	0.0521
$5L_{min}$, $2W_{min}$	10.41	0.0287	0.0499
$5L_{min}$, $5W_{min}$	8.90	0.102	0.0505

Table 3: The table for P-18-MM

First we see the parameter $K = \mu_n C_{ox}$, depends on the electron mobility and the oxide thickness. We see that for the NMOS increasing the width of the device increases K, do to more electrons being injected into a wider area. However it goes down with the increase in the channel length because the electrons now have to cover a longer distance. For the PMOS however we see that there is a opposite effect and the values do not show any identifiable trends. Also as the hole mobility is less than the electron mobility, the value of K for a PMOS is less than that for an NMOS.

V_{th} is a complex function of the length and width of a CMOS device. We see that for a constant length, for an NMOS increasing the width decreases the threshold voltage and the opposite holds for the PMOS. V_{th} variations can occur due to both short channel and narrow channel effects and sometimes they tend to cancel each other out.

For the channel length parameter λ, its value depends on the process technology as well as the transistor channel length, that is in the control of the designer. In general, λ is inversely proportional to the channel length L. Similar trends can be seen in the NMOS and PMOS data tables.

3.3 Conclusion

We saw from the data we gathered that different MOSFET parameters are effected in different ways due to the variation of the geometrical properties of the transistor. Usually with a few data points no clear dependence can be drawn as these parameters often exhibit complicated dependence on the MOSFET geometry as well as other parameters. Controlled values of these parameters can only be obtained by using tightly controlled processes and having in depth design knowledge.

4 The Topology Selection and Alternatives

In this section,we will describe the working principle of a Band-gap Voltage Reference circuit, and why it is used. It will explain the circuit design necessary to get a stable reference voltage, as well as explain the topology that we have chosen to implement in this lab.

4.1 Explanation

A Band-gap voltage reference is a circuit used for providing a temperature independent reference voltage. Reference voltages are important in ICs, for example, for generating reference

currents that are used to biase amplifier stages.

Most Band-gap circuits works by using two voltage that have opposite temperature coefficients, and add them to cancel out the overall temperature dependence.

For example, the base-emitter voltage of a BJT is given as

$$V_{\mathrm{BE}} = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) \tag{4}$$

and the temperature coefficient of the base-emitter voltage is given as

$$\frac{\partial V_{\mathrm{BE}}}{\partial T} = -2\,\mathrm{mV}/^{\circ}\mathrm{C}$$

We see that the base-emitter voltage is **Complementary To Absolute Temperature (CTAT)**, i.e it decreases with the increase in temperature. We also know that the thermal voltage is dependent on the temperature and its temperature coefficient is given as

$$\frac{\partial V_{\mathrm{T}}}{\partial T} = \frac{k}{q} = 0.086\,\mathrm{mV}/^{\circ}\mathrm{C}$$

and this is **Proportional To Absolute Temperature (PTAT)**. The basic idea behind the bandgap voltage reference is to add multiples of the PTAT source to a CTAT source such that temperature independence is achieved. It is for this reason that a single diode cannot be used as a stable reference.

The CTAT is normally taken from a diode connected transistor. The PTAT voltage can be generated by taking the difference of the base-emmiter voltages of two transistors that have similar scale and collector currents but can differ in their emitter area.

Consider Figure 1. Two transistors Q1 and Q2 are shown. Both are biased by the same current source I, and thus have the same collector currents. The emitter area of Q2 is n times that of Q1. The voltage difference ΔV_{BE} is

$$\Delta V_{\mathrm{BE}} = V_{\mathrm{BE1}} - V_{\mathrm{BE2}} = \frac{kT}{q} \ln(n)$$

where the parameter n can be chosen by the designer.

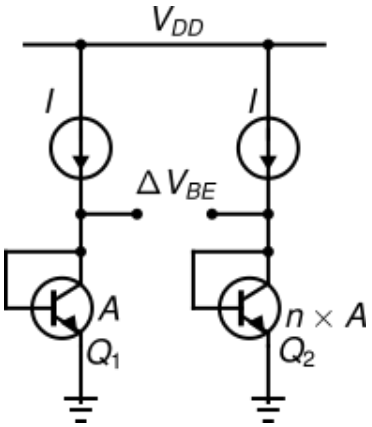

Figure 1: A circuit to obtain the difference between the base emitter voltages ΔV_{BE}

If we now add the multiples of PTAT and the CTAT

$$V_{\mathrm{BG}} = kV_{\mathrm{T}} + V_{\mathrm{BE}}$$

We require that $\frac{\partial V_{\mathrm{BG}}}{\partial T} = 0$, which implies

$$0 = k(0.086) - 2$$

$$k = 24.4$$

Assume at room temperature we have $V_{\mathrm{BE}} = 650\,\mathrm{mV}$ and $V_{\mathrm{T}} = 25\,\mathrm{mV}$, we have a bandgap voltage of

$$V_{\mathrm{BG}} = (24.4)(25) + 650 = 1.26\,\mathrm{V} \tag{5}$$

The bandgap voltage is not always independent of the temperature, it shows a curvature due to the temperature coefficient of V_{BE} which is not constant.

In a CMOS process, the bandgap reference is usually made with the help of parasitic BJTs that are formed during the fabrication. Figure 2 shows an example. The pnp transistor formed by the three different layers. The p+ region serves as the emitter, the n-well as the thin base, and the p-substrate acts as the collector of the transistor.

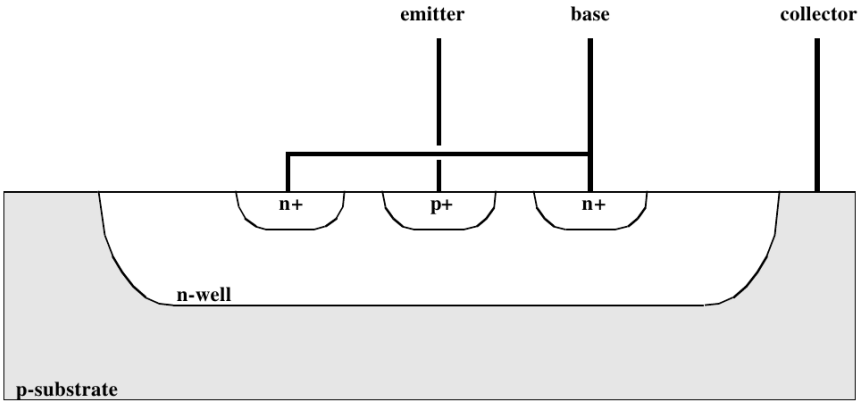

Figure 2: Different layers that are part of a CMOS process.

4.2 Design

Different typologies exist for the design of a Band-gap voltage reference. The topology that we selected for our design was the Brokaw Band-gap reference. The circuit uses and operational amplifier connected in a feedback configuration to force the same current through two transistors with different emitter areas. Figure 3 shows the circuit. The collectors of both PNP transistors are tied to ground. Applying KVL to the loop containing V_{out}, we have:

$$V_{\mathrm{out}} = V_{\mathrm{EB2}} + V_{\mathrm{R2}} + V_{\mathrm{R}}$$

If we consider the operational amplifier as ideal, then both of its input pins should be at an equal voltage, therefore

$$V_{\mathrm{EB1}} = V_{\mathrm{EB2}} + V_{\mathrm{R2}}$$

$$V_{\mathrm{R2}} = V_{\mathrm{EB1}} - V_{\mathrm{EB2}}$$

we also know that

$$V_{\mathrm{R}} = I_2 R = R\frac{V_{\mathrm{R2}}}{R_2}$$

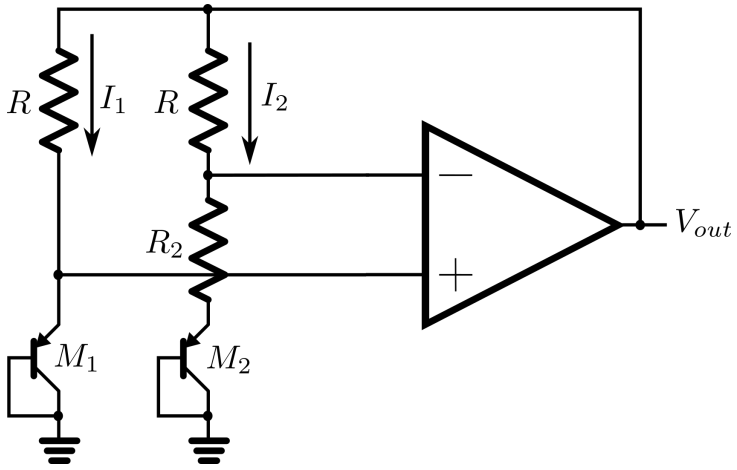

Figure 3: A Brokaw Bandgap reference circuit implemented with PNP transistors.

If we take the area of M_2 to be N times that of M_1 and further assume that $I_1 = I_2$ i.e. the operational amplifier forces the same current through the emitters of both transistors, then

$$V_{\mathrm{R2}} = V_{\mathrm{T}} \log(N)$$

Now

$$V_{\mathrm{out}} = V_{\mathrm{EB2}} + V_{\mathrm{R}} + V_{\mathrm{R2}}$$

$$V_{\mathrm{out}} = V_{\mathrm{EB2}} + V_{\mathrm{R2}} \left(\frac{R}{R_2} + 1 \right)$$

Finally we have

$$V_{\mathrm{out}} = V_{\mathrm{EB2}} + \left(\frac{R}{R_2} + 1 \right) V_{\mathrm{T}} \log(N) \tag{6}$$

For our purpose we are required to have an output voltage $V_{\mathrm{out}} = 1.2\,\mathrm{V}$. From this we can find the required ratio of the resistances. Assume a certain transistor operating at $V_{\mathrm{EB}} = 650\,\mathrm{mV}$ and the area difference to be $N = 10$

$$1.2 - 0.65 = \left(\frac{R}{R_2} + 1 \right) V_{\mathrm{T}} \log(N)$$

$$\frac{1.2 - 0.65}{0.025 \log(10)} - 1 = \frac{R}{R_2}$$

$$\frac{R}{R_2} = \frac{6}{5} = 21 \tag{7}$$

Therefore two possible choices are $R = 2.1\,\mathrm{k\Omega}$ and $R_2 = 100\,\Omega$.

The Brokaw reference is more stable than the classic Widlar reference because collector current sensing is used to fix the ratio of the current density in the two transistors. Also if different currents are flowing then we can have temperature drifts.

4.3 Alternatives

The reference design considered as alternatives comprised of both active and passive devices considered. The most simple passive topology considered was that of voltage divider but the bias point was highly dependant on the variation in power supply, although the temperature

could be accounted for by picking exact same resistors (albeit process variations might have lead to a slight difference). Second passive topology studied was the Zener diode based circuit operating in reverse bias and again this circuit was sensitive to both temperature and DC bias since the Zener diode large signal model is dependant on variations in both. The designs of using active elements like MOS transistors and BJT were rejected again due to explicit dependence on the temperature when considering their large signal models

4.4 Conclusion

In short report highlighted the operating principle of a Bandgap reference circuit and presented a simple topology for the implentation of the circuit. The output voltage and temperature dependence of a reference are not always stable and hence more optimization will be needed in the circuit, however, this simple topology is very popular and is very often used in practical CMOS circuits.

5 Ideal Band-gap Circuit

We will describe the simple topology of a Band-gap Voltage Reference circuit using PNP transistors, which was designed and simulated using Cadence IC Design tools. It will also examine the trends in the reference voltage with respect to temperature as well as input voltage variations.

5.1 Explanation

The circuit of a simple Band-gap reference employing PNP transistors is shown in Figure 4. The PNP transistors are usually parasitics formed during the process. For this schematic all the components used are ideal. So it can be assumed that the Operation Transconductance Amplifier (OTA) has an infinite gain, input impedance and bandwidth and zero output impedance.

The resistors used are also ideal. The positive supply of the OTA is connected to V_{DD} and the negative supply to ground. The working of the circuit was already explained in the previous report.

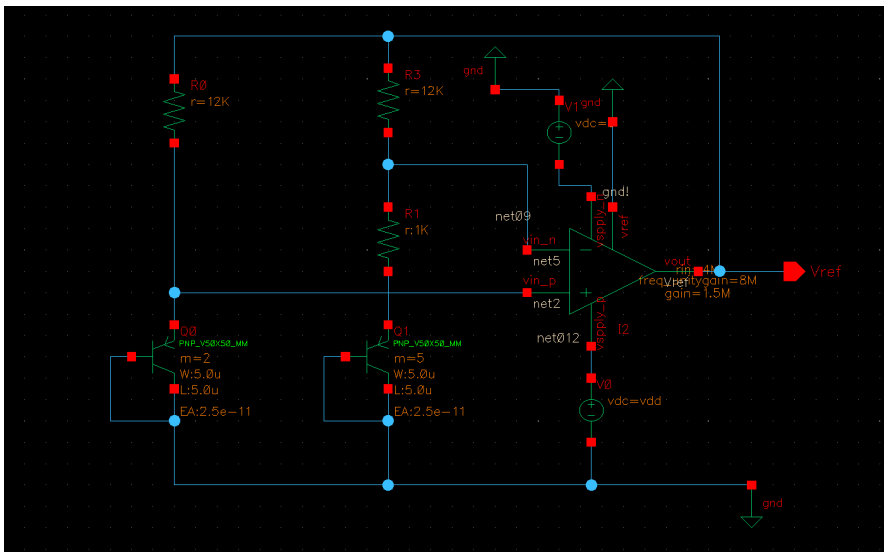

Figure 4: The circuit of the bandgap reference employing PNP transistors.

We will now examine the different properties of this Bandgap reference using simulation tools.

5.2 Power Supply Rejection Ratio (PSRR)

The Power Supply Rejection Ratio (PSRR) is used to express changes in the output with respect to changes or ripples in the supply voltage of an operation amplifier. If a change of X volts in the power supply produces a change Y in the output voltage, then the PSRR will be X/Y. This is the PSRR referred to the output. The PSRR is often expressed in decibels (dB).

Figure 5 show the plot of the output voltage of the reference versus the power supply voltage. The power supply that was connected to the positive supply pin of the OTA is swept from 0 to 3.4 V.

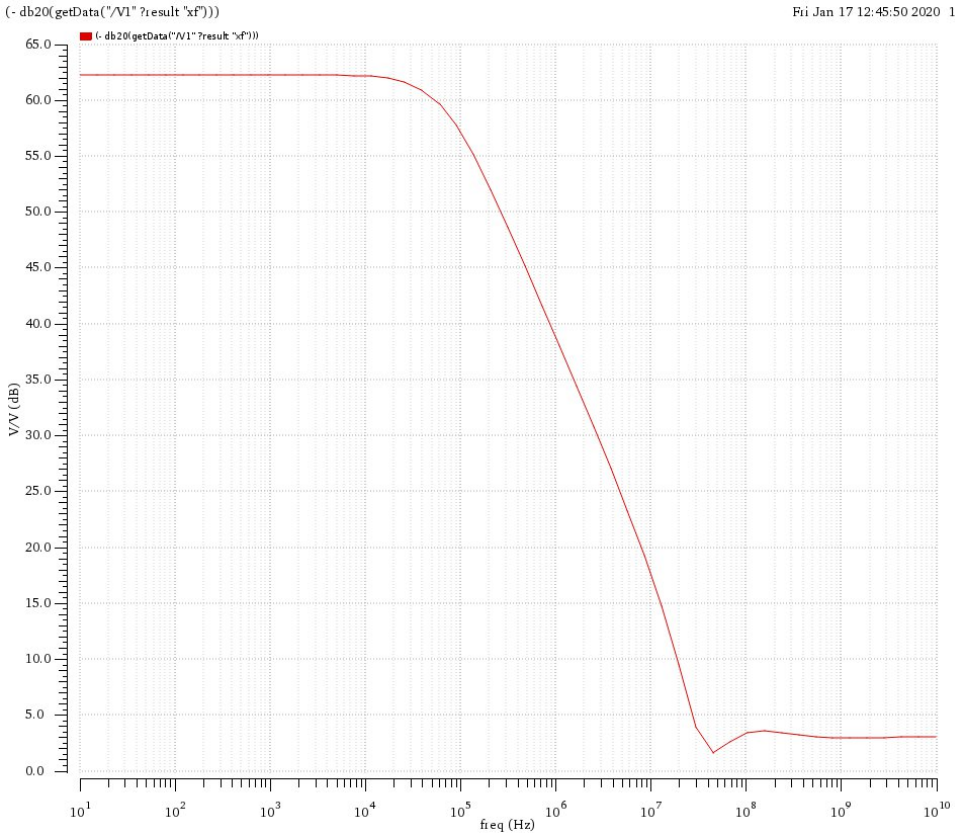

Figure 5: A plot of the voltage output with respect to the power supply voltage.

We see that after the reference voltage has settled to a final value, it is almost a constant value. Therefore it does not change with a change in the input voltage. If this is the case then we can say that the PSRR is ∞dB. This is due to the fact that the OTA is ideal and it resists any changes in the power supply voltage.

5.3 Temperature Dependence

The voltage of an ideal Bandgap reference should remain constant with the change in temperature however in reality this is not often the case. The output of a real Band-gap is a bow shaped curved that varies slowly with temperature.

Figure 6 shows the variation of the output reference voltage with respect to the temperature. The temperature sweep was ran from 25 °C to 100 °C.

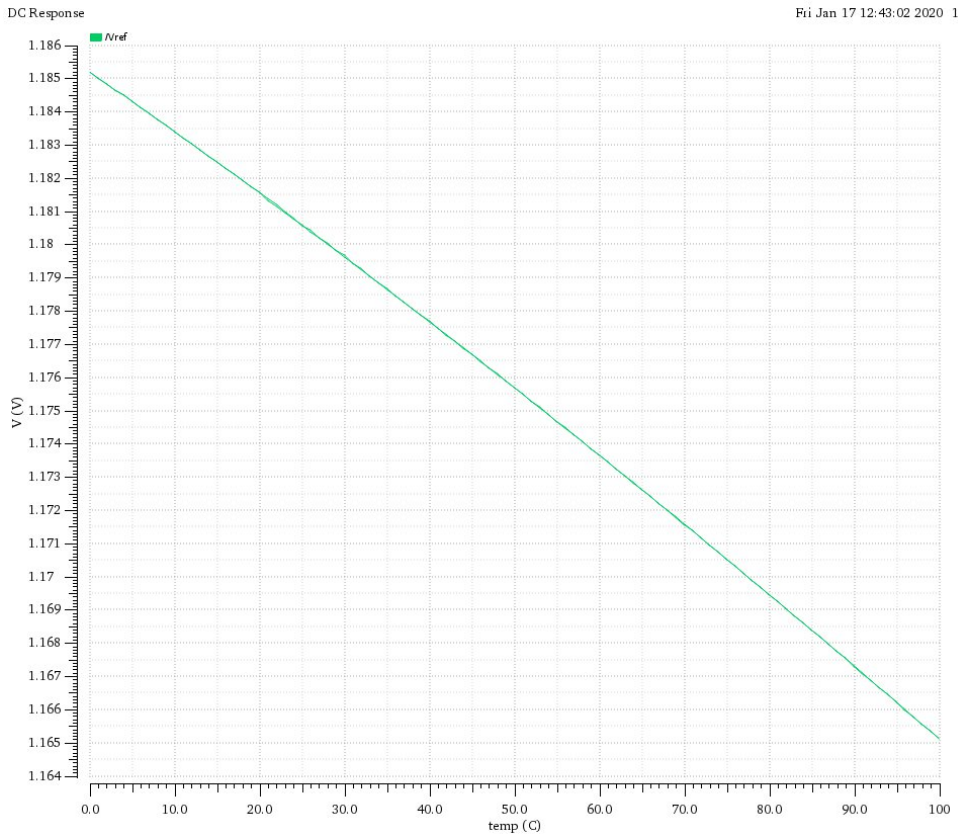

Figure 6: The plot of the output reference voltage versus the temperature.

The red line in Figure 6 shows the variation of the output voltage, whereas the green line shows the slope of the red line. It can be seen that the slope is around $-36\,\mu V°C^{-1}$. This means that the output voltage decreases with the increase in temperature.

Running a sample sweep, we see that at 25 °C, the reference voltage is $V_{REF} = 1.4866\,V$ and at 100 °C the reference voltage is $V_{REF} = 1.4456\,V$. A general trend that can be seen is that at higher temperatures and with an increase in the supply voltage, the reference voltage increases.

5.4 Settling Behaviour

The settling behavior refers to when the output reference voltage attains a constant value and maintains that value. From Figure 7 we can see that when the power supply voltage $V+ = 2\,V$, then the output voltage is $V_{REF} = 1.4825\,V$. Therefore the output voltage settles to a constant value as soon as the supply voltages reaches 2 V. We see that no ringing or oscillating behavior is visible in the output response, and this is due to the OTA being ideal.

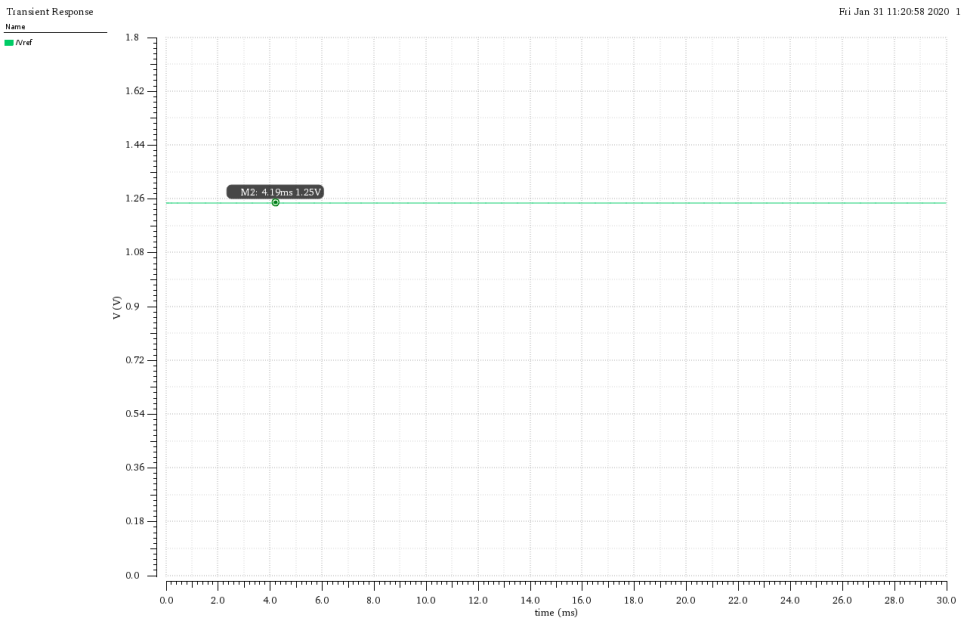

Figure 7: The transient behaviour of ideal Op-Amp V_{Ref} obtained

5.5 Conclusion

We saw the different properties of the Bandgap reference such as the temperature dependence, PSRR and settling behavior of the output voltage. We saw that our designed reference exhibits good properties in many respects, and this is due to the fact that our OTA was ideal. When we employ a realistic amplifier then these properties will obviously deviate to show the impact of parasitic components as well as internal mismatches.

6 Two stage Operational Amplifier Design

6.1 Introduction to Multi-Stage Design

The concept of multi-stage amplifier is used to compensate for the inadequacies faced by the amplifier when designed using discrete devices. Hence it is amalgam of several typologies which make up for the inadequacy of one another (i.e low-open-circuit voltage gain, low input resistance,high output resistance) and can be typically described as having three stages:

1 The Input Stage – This section has one purpose, to provide the multi-stage amplifier with a high input resistance. For differential amplifiers, this stage must also be a differential amplifier (e.g., a differential pair).

2 The Gain Stages - This section consists of one or more amplifiers (stages) with high open-circuit voltage gain (e.g., common emitter, common source). This section thus provides the required voltage gain for the multi-stage amplifier.

3 The Output Stage - The third and final section of the multi-section amplifier likewise has one purpose: to provide the multi-stage amplifier with a low output resistance. As such, this stage is often a common collector (emitter follower), or common drain (source follower).

6.2 Designed Amplifier

The Op-Amp which we will implemented consists of two stages as shown in the figure, which can further be divide into 4 distinct regions on the schematic to make it easier to understand. The parts of the amplifier can be described as follows:

1 Current mirror based reference current
A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of the circuit, keeping the output current constant regardless of loading. The current being "copied" can be, and sometimes is, a varying signal current.The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist). In our circuit it comprises of M8 and M7 and is used to provide bis current to the remaining circuitry.

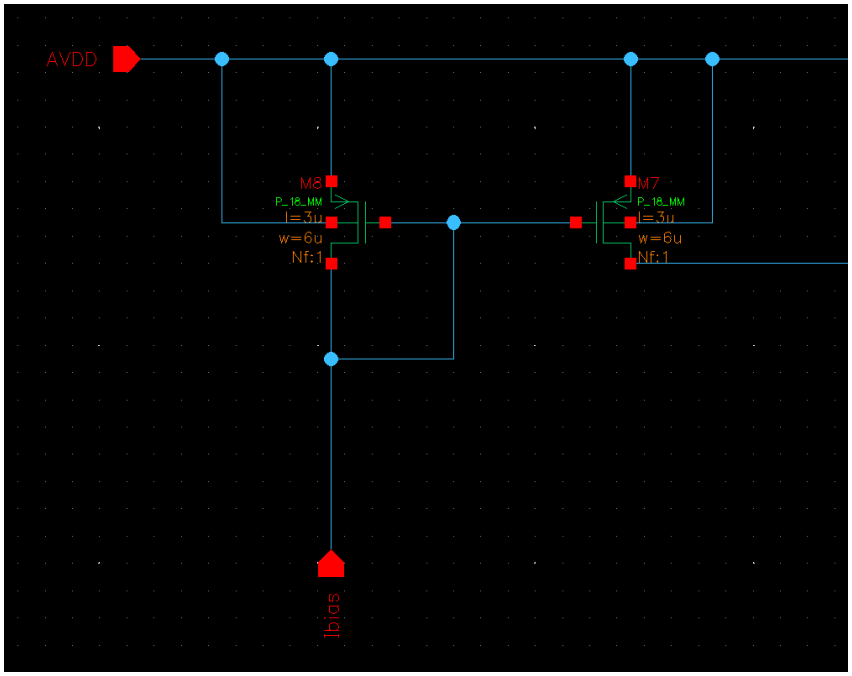

Figure 8: Current Reference Circuit Model

2 Differential Pair with Active load and bias network (First Stage)
The Differential stage consists of two NMOS transistor operated in inverting and non-inverting modes respectively, followed by current mirror based active load on the top and current mirror based biasing network connected at common drain of the two NMOS of differential stage to keep the transistor in right bias point.

In our circuit as shown, M0 and M1 are the differential pairs in inverting and non inverting modes respectively with the active load comprising of M2 and M3. This stage also performs the function of offering high input impedance thereby moving the Op-Amp closer to ideal behaviour. The overall

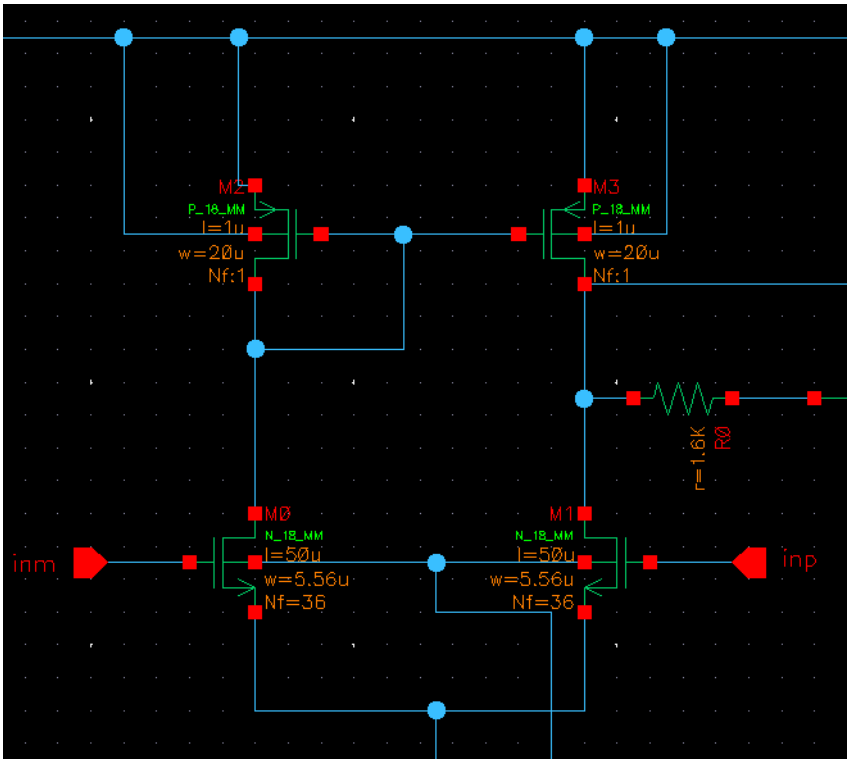

Figure 9: First Stage Two-Port and Small-Signal Model

The two port small signal model of differential pair is as shown in the diagram below, with the parameters being $Z_{i12} = \frac{1}{s(C_{gs1}/2}$,$G_{m1} = g_{m2} = g_{m3}$ and $R_{out1} = r_{01}||r_{03}$

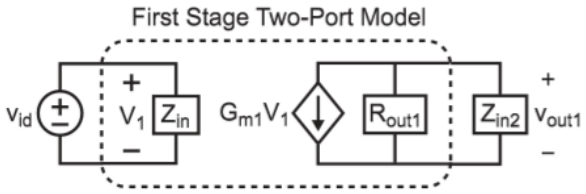

Figure 10: First Stage Two-Port and Small-Signal Model

3 Miller compensation network

The purpose of miller compensation network is to provide stability to the setup by shifting the pole of the overall transfer function given as

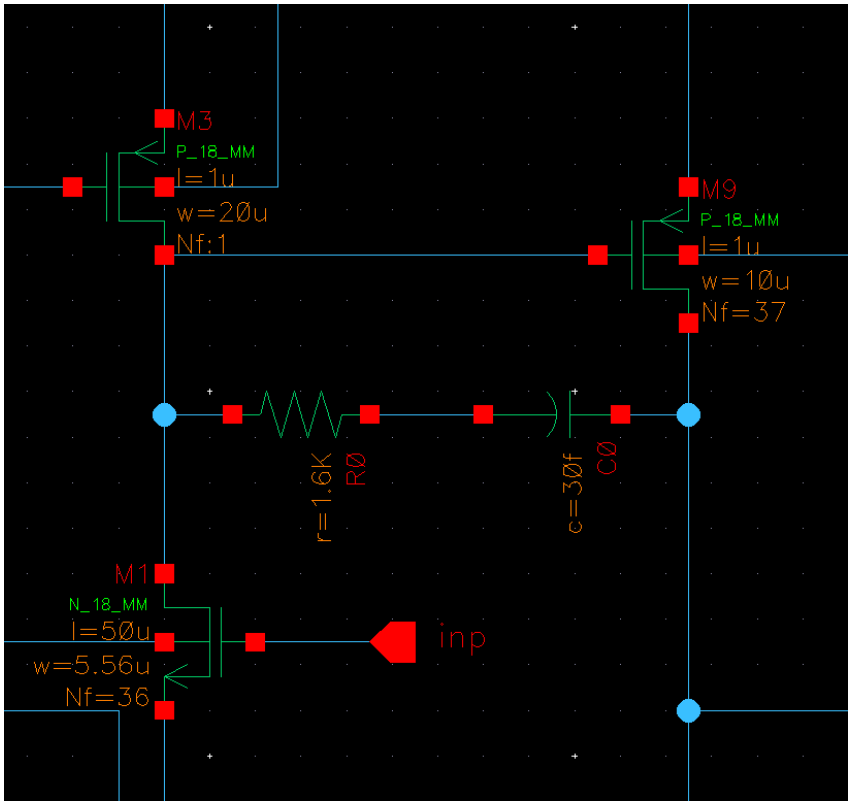

Figure 11: Miller Compensation Branch

The passive components (capacitor and resistor) in there can be use to adjust the phase margin and hence the stability of the overall scheme by moving the poles of the transfer function.

4 Source follower amplifier with load biasing (Second Stage)
This setup constitutes as the second stage The transistor is used as a load for the common source second stage of the amplifier and the gain depends on the resistance of this NMOS transistor as well. In our circuit, the transistors M9 and M6 are used for this purpose with the M6 acting as the load of the amplifier and the trans-conductance of the M9 providing amplification. The purpose of this stage is to reduce the output impedance of the operational amplifier and hence move its behaviour closer to ideal scenario.

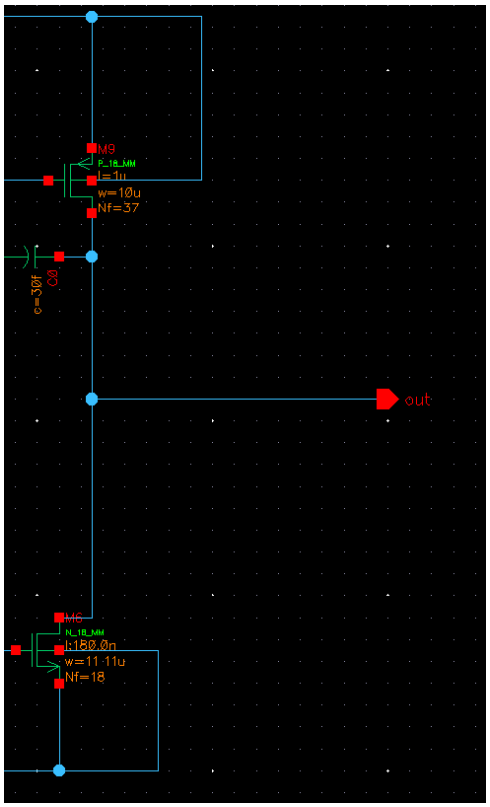

Figure 12: Second Stage Two-Port and Small-Signal Model

The two port small signal model of differential pair is as shown in the diagram below, with the parameters being $Z_{in2} = \frac{1}{s(C_{gs6}/2}$,$G_{m2} = g_{m6}$ and $R_{out2} = r_{09}||r_{06}$

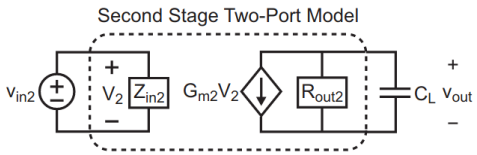

Figure 13: Second Stage Two-Port and Small-Signal Model

6.3 Overall Gain

The overall gain of the amplifier can be stated as being $A_v = A_1 * A_2$, which in this case can be stated as being $K = g_{m2}\left(r_{01}||r_{03}\right) g_{m6}\left(r_{09}||r_{06}\right)$

7 Operational Amplifier parameters

In this section we shall take a look at the performance of the designed Operational Amplifier. The different parameters of the OpAmp will indicate how well it will perform in our designed Bandgap circuit.

7.1 Stability

The first analysis that will be carried out is the stability analysis. This will show us how the OpAmp will behave in a feedback configuration. We wish to avoid oscillations when we close the loop. For this reason we characterize the stability. Stability is characterized by two parameters, the **Gain Margin (GM)** and the **Phase Margin (PM)**. Both these parameters indicate the amount of gain or phase change we can tolerate in the closed loop system before it becomes unstable.

Figure 14 shows the circuit used to find the frequency response of the operational amplifier.

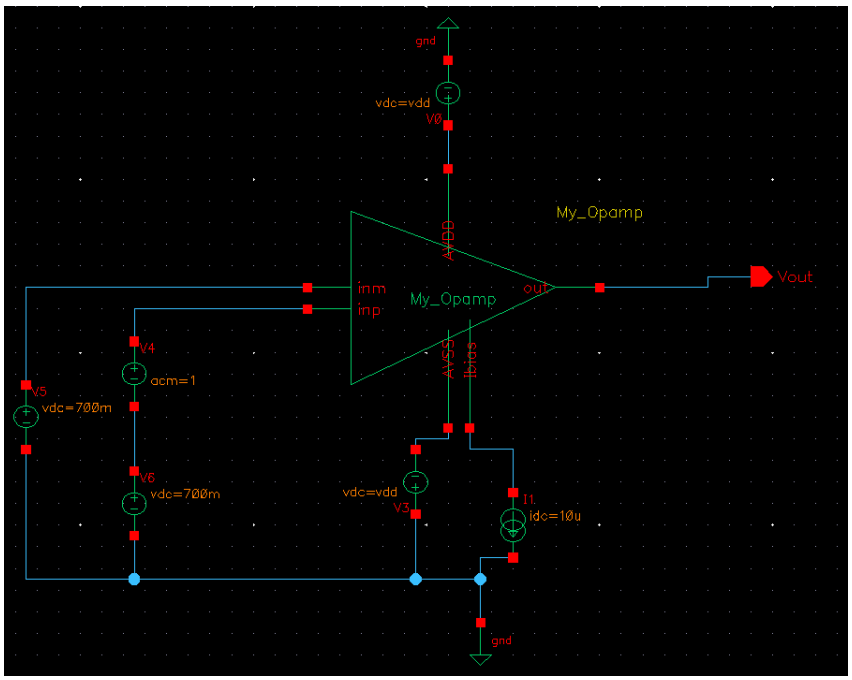

Figure 14: Circuit used for obtaining the Bode plot of the operational amplifier.

Figure **??** shows the output plot of the OpAmp's frequency response. The midband gain of the OpAmp is around 47.8 dB. The gain margin is calculated at the frequency where the phase response becomes -180 deg. In figure 15 the gain margin is $0 - 17.27 = 17.3$ dB.

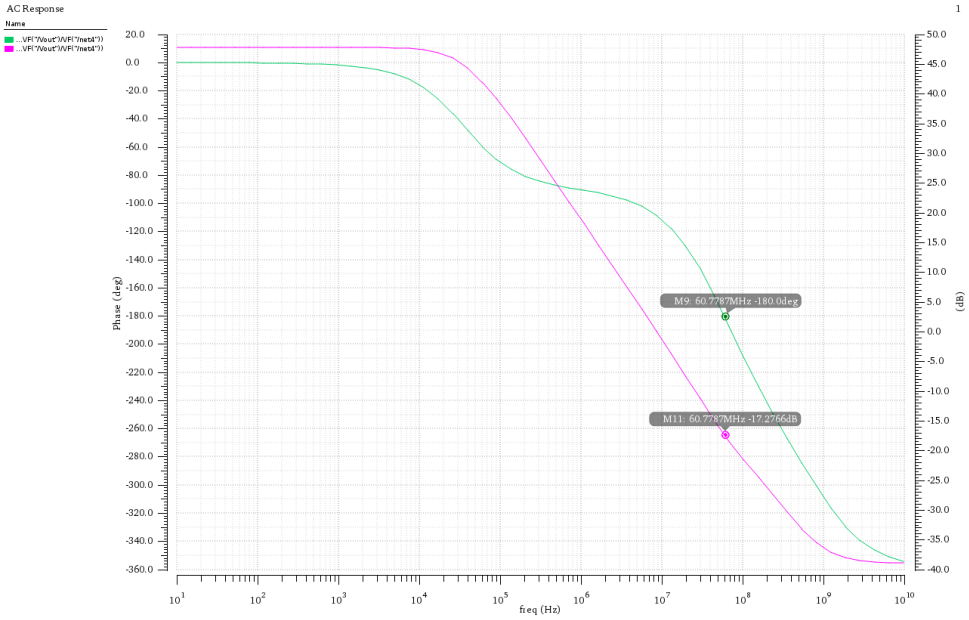

Figure 15: Bode Plot of the OpAmp output indicating the Gain Margin.

In a similar manner, figure 16 is used for indicating the phase margin of the OpAmp. The Phase Margin is calculated at the point where the gain is equal to 0 dB. In figure 16 the phase margin is $-108.5.8 + 180 = 71.5\,\text{deg}$.

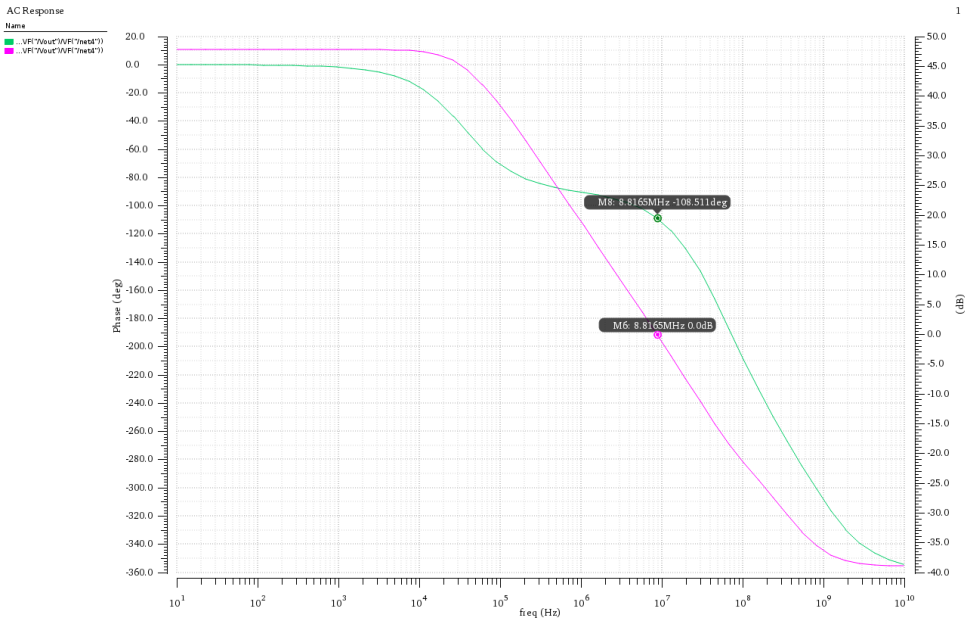

Figure 16: Bode Plot of the OpAmp output indicating the Phase Margin.

Both the gain margin and the phase margin are expressly used to indicate how stable the amplifier will be in a closed loop configuration. The higher these margins are, the better the stability.

7.2 Power Supply Rejection Ratio (PSRR)

The Power Supply Rejection Ratio (PSRR) is an indicator of the isolation between the supply terminals of the amplifier and the output terminal. If the voltage of the power supply changes by XV and this change causes a voltage YV at the output terminal, then the PSRR is given as $\frac{X}{Y}$. The PSRR is normally expressed in dB's.

In order to find the PSRR, we need to connect a pulse DC source to the positive voltage pin and perform and XF analysis of the circuit. The XF analysis can be used to find the transfer function from different inputs to the output of the amplifier. In this case, the input was selected to be the positive supply voltage pin. The result is obtained as a frequency sweep. Figure 17 shows the curve obtained by the XF analysis. It can be seen that in the passband the PSRR of the OpAmp circuit is nearly 92.2 dB.

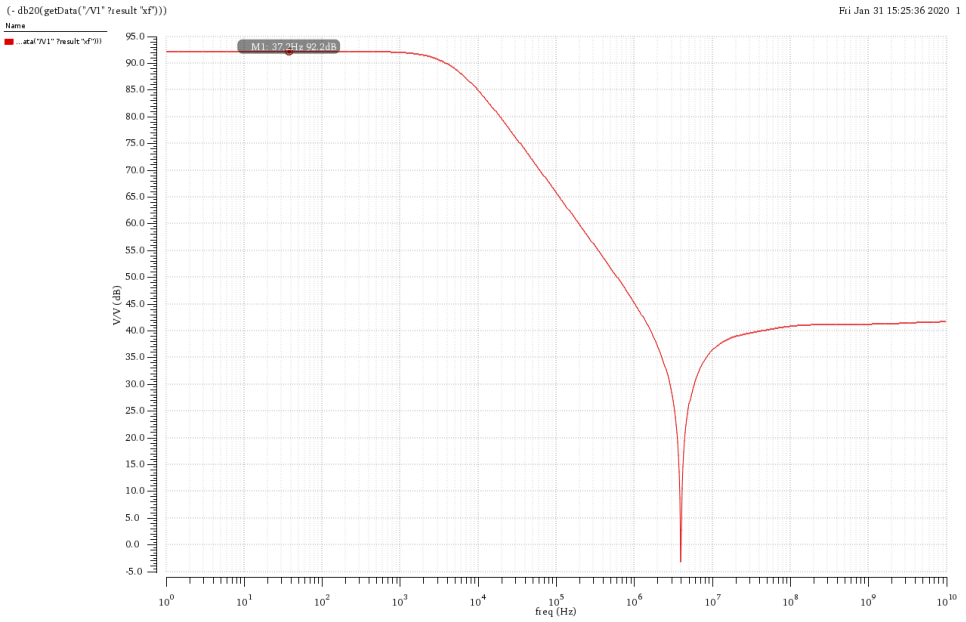

Figure 17: The PSRR of the OpAmp in the passband.

7.3 Common Mode Rejection Ratio (CMRR)

An ideal operational amplifier only amplifies the differential signal that is applied to its inputs and rejects all common mode signals. However due to inherent mismatches as well as differences in the currents some common mode signals also appear at the output. The Common Mode Rejection Ratio (CMRR) is defined as the ratio of the gain of the differential output to the gain of the common mode output. The higher the CMRR, the better the amplifier will be in rejecting common mode signals.

Figure 18 shows a plot of the common mode output of the OpAmp. The same signal was applied to both the inputs in order to see how much of the output is obtained. It can be seen from here that the common mode gain is -34.11 dB. In order to calculate the CMRR, we subtract this from the differential gain, since the CMRR is a ratio. Hence the CMRR is $47.8 - (-34.11) = 81.9$ dB.

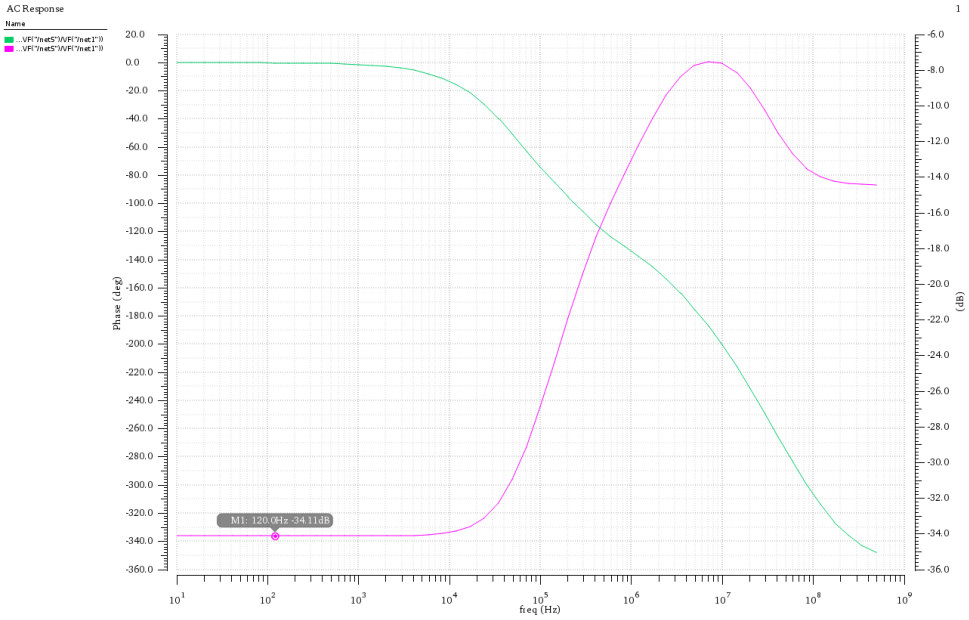

Figure 18: The common mode output of the OpAmp.

7.4 Summary

Table 4 summarizes all the performance parameters of the operational amplifier. By optimizing the lenght/width of the transistors further performance can be improved but as in all cases of analog design there are inherent tradeoffs. The gain can be increased by increasing the trans conductance of the differential transistors or the output resistance of the first stage, for example.

Parameter	Value
Open Loop Gain	47.8 dB
Gain Bandwidth Product	8.82 MHz
Gain Margin	17.3 dB
Phase Margin	71.5 deg
PSRR	92.2 dB
CMRR	81.9 dB

Table 4: A summary of all the simulated parameters of the designed operational amplifier.

8 Real Bandgap circuit

The circuit for the Bangap reference is implemented using the designed operational amplifier as shown in Figure 19.

We will now examine the circuit and analyze its performance.

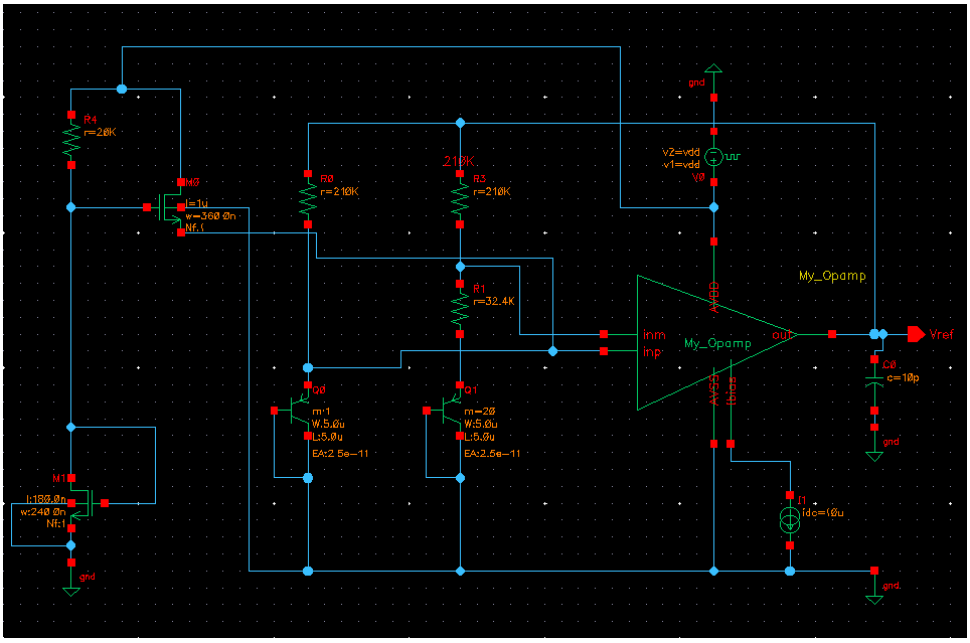

Figure 19: The circuit of the Bandgap reference implemented using the designed operational amplifier.

8.1 Startup circuit

Included in the circuit for the Bandgap is the startup circuit which is implemented by the transistors M0 and M1. The purpose of the startup circuit is to help assign two stable operating points to the main core. The current and voltage sources in the circuit can resist turning on and therefore need startup circuits. The startup ensures that the circuit works up to the supply voltage. Once the circuit is in running state, the startup circuit turns off.

When the supply voltage is initially applied, the transistor M0 turns on and provides an input to the positive terminal of the operational amplifier. This causes a differential voltage between the amplifier inputs and the circuit starts up. However soon after the transistor M1 turns on which causes the gate of M0 to be grounded, hence turning it off and removing its connection from the amplifier input. Afterwards the startup circuit plays no role and the bandgap core functions normally as intended.

8.2 Performance

The output voltage of the Bandgap reference is shown in Figure 20. It provides an output voltage of 1.23 V, as required. The remaining parameters will be examined next.

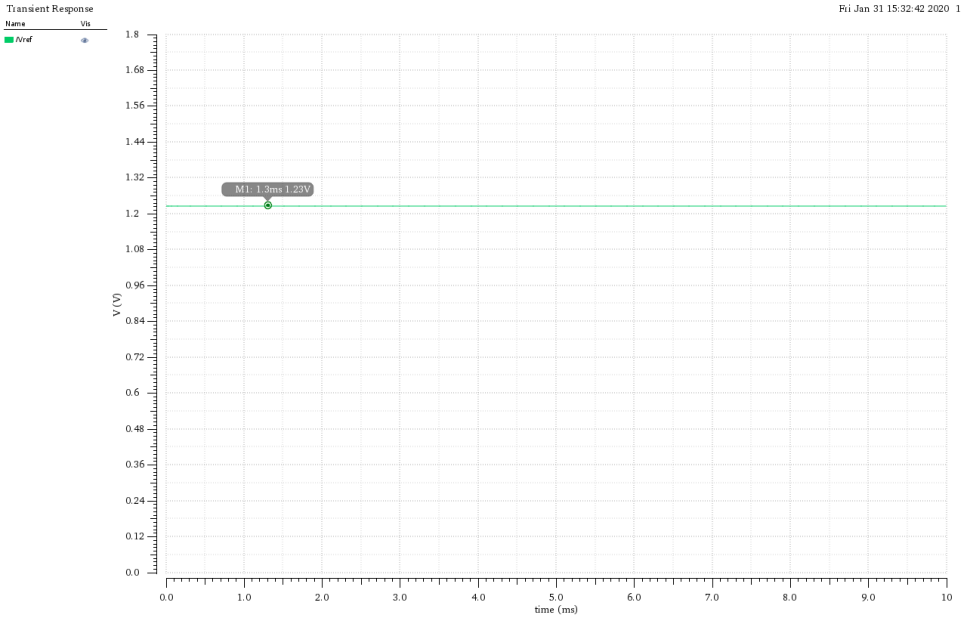

Figure 20: The steady state output voltage of the bandgap reference.

8.2.1 Power Supply Rejection Ratio

The PSRR of the entire bandgap circuit was obtained in a similar manner as of the operational amplifier and is shown in figure 21. The PSRR is 81.1 dB.

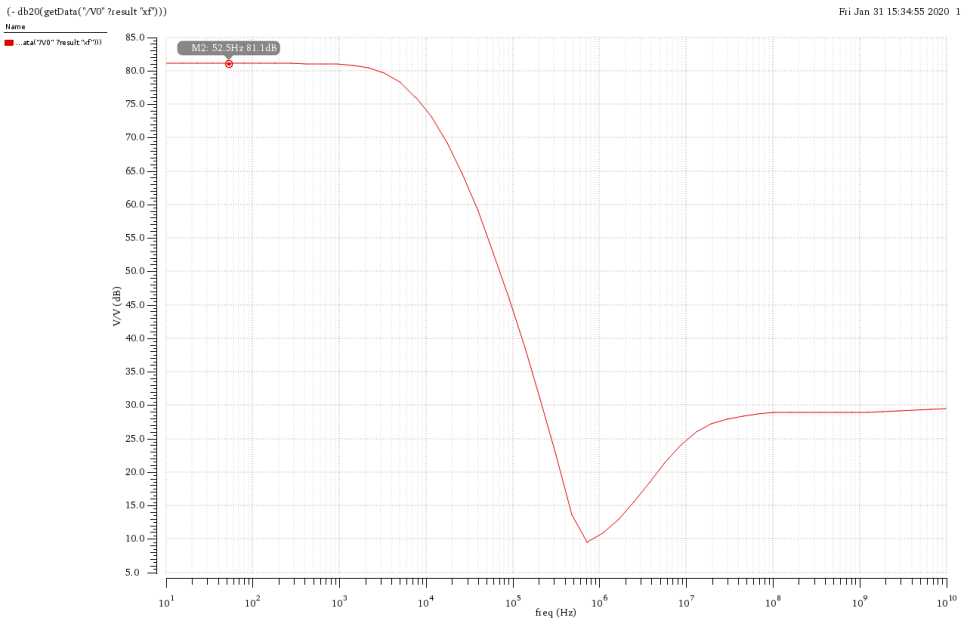

Figure 21: The PSRR of the bandgap reference.

8.2.2 Temperature dependence

Figure 22 shows the variation of the bandgap voltage with temperature. The magenta curve is the output voltage and the red curve is its derivative. It can be seen that the slope is nearly a straight line, which means there is very little change in the voltage with the operating temperature. At 100 °C the change of temperature is only 27.7 µV °C^{-1}

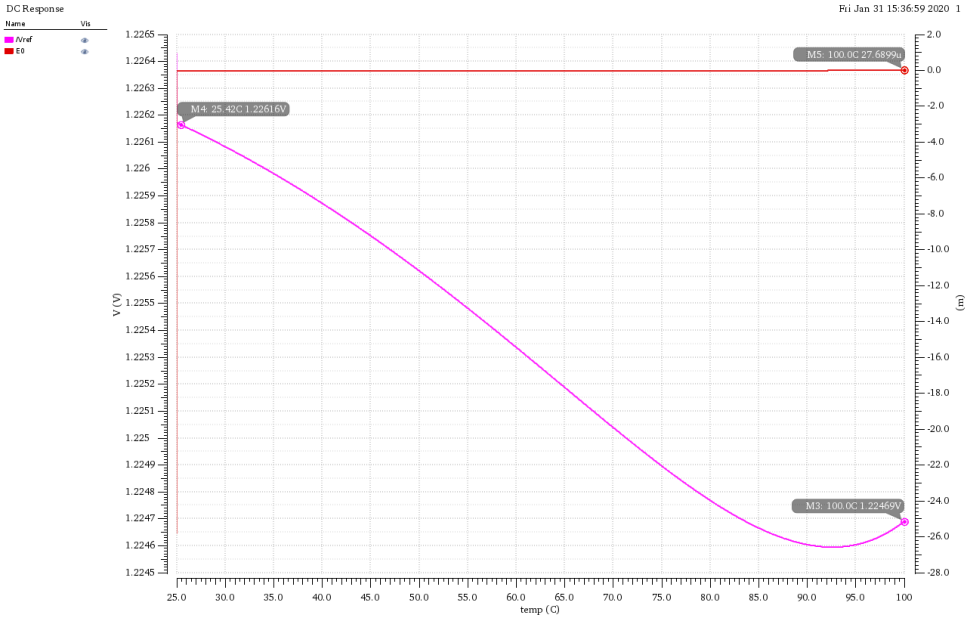

Figure 22: The dependence of the output voltage on the operating temperature.

8.2.3 Output and supply voltage

Figure 23 shows how the output voltage of the bandgap varies with changes in the supply voltage. It can be seen that at lower supply voltage the circuit is not providing a reasonable output. However at a voltage of 0.55 V the circuit immediately starts up and quickly reaches to the value of 1 V. We can see that the bandgap output becomes a constant 1.2 V after a supply voltage of 1.3 V

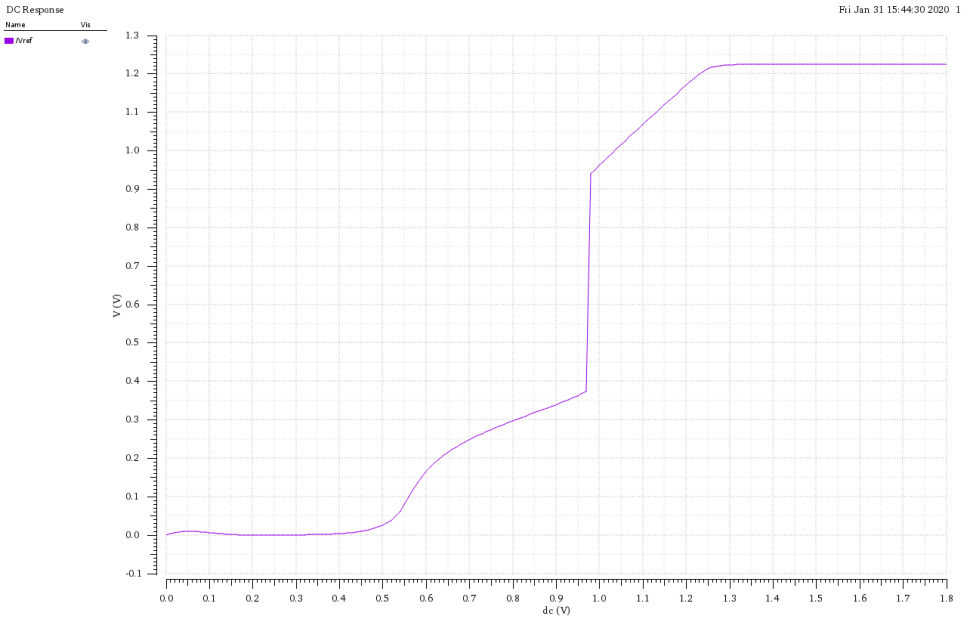

Figure 23: The dependence of the output voltage on the supply voltage.

8.2.4 V_{TH} mismatch

A mismatch between the threshold voltages of the two transistors in the input differential stage of the operational amplifier is introduced. This mismatch is modeled as a 5 mV voltage source between the gates of the two transistors. Figure 24 shows how the output voltage changes due to this mismatch. It can be seen that the output voltage rises up to 1.71 V.

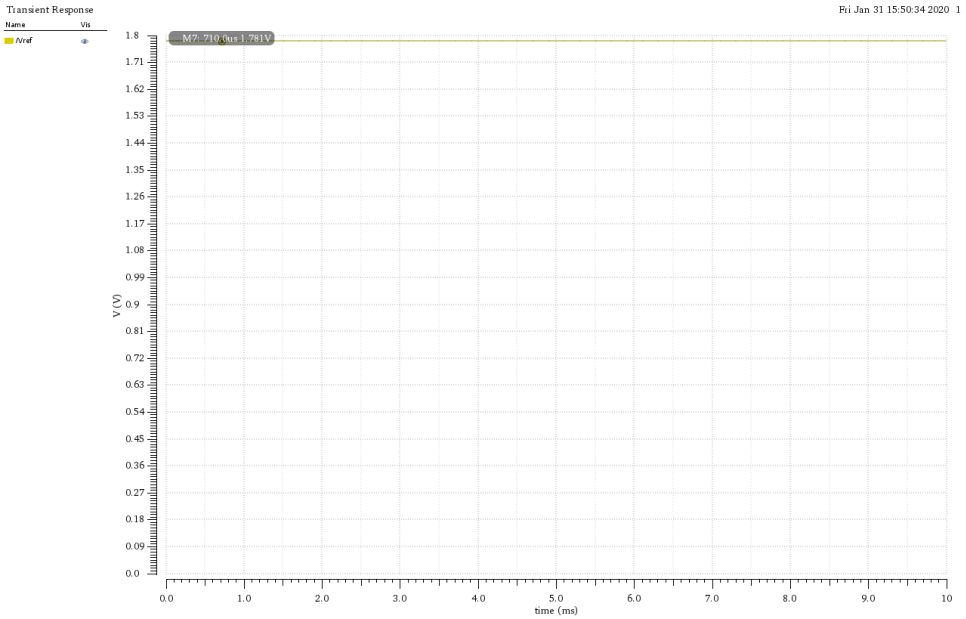

Figure 24: The change in the output voltage with the introduction of the V_{TH} mismatch.

8.2.5 Resistor variation

By introducing a change of 15% around the center values of the resistors employed, we obtain figure 25. It can be seen from the figure that the process variations can introduce significant changes to the performance of the circuit and this must be kept in mind when designing. Specific resistor layout techniques can help mitigate this problem to some extent.

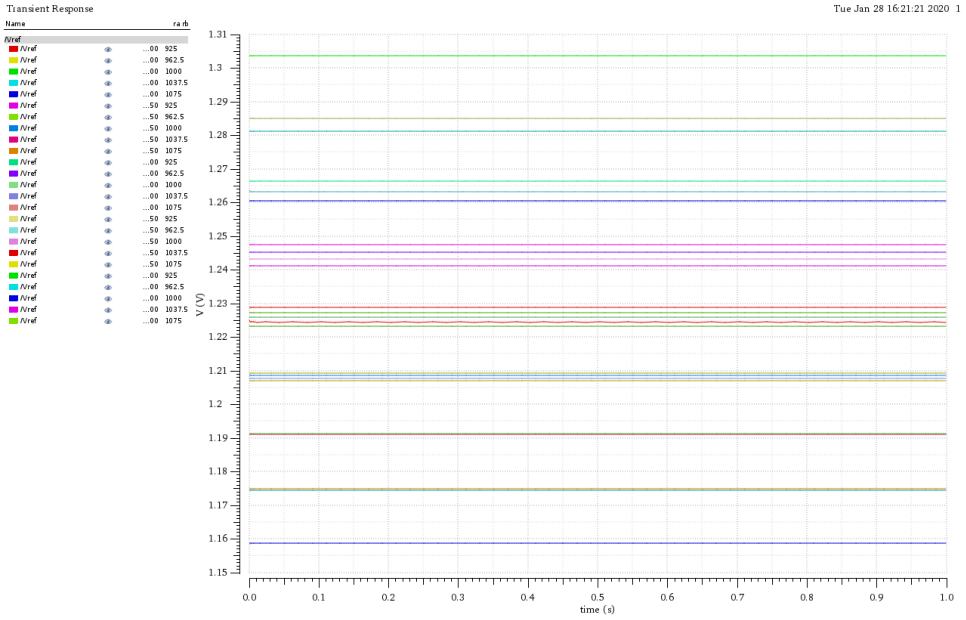

Figure 25: The change in the output voltage with a variation in the values of the resistors employed in the bandgap circuit.

8.2.6 Current draw

If a 100 µA current is drawn from the output of the bandgap circuit its voltage drops down to 1.22 V as shown in figure 26. This indicates that the design is suitable to drive a 100 µA load.

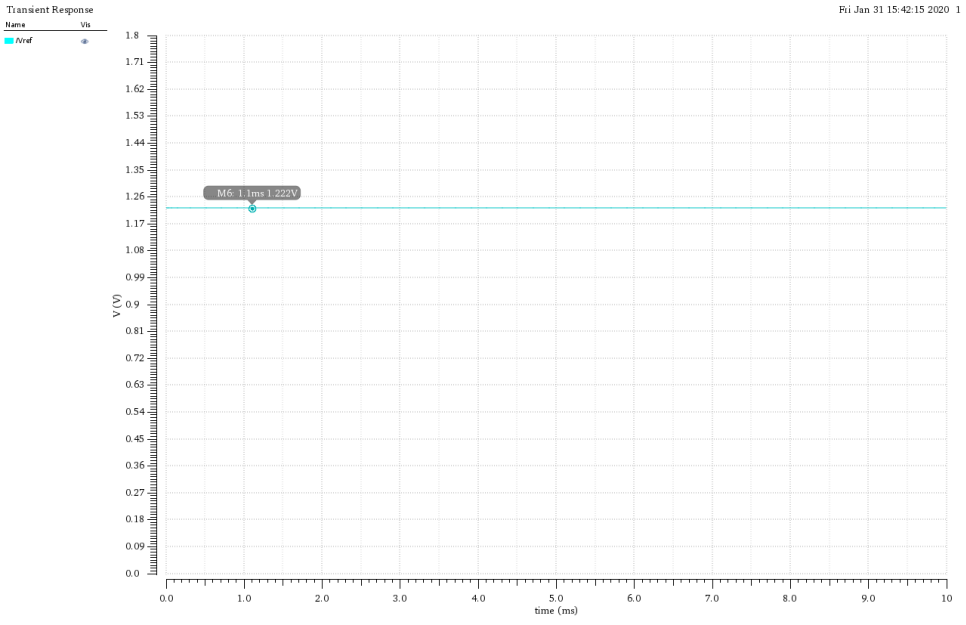

Figure 26: The change in the output voltage when a load current of 100 µA is drawn from the output .

8.2.7 Settling behaviour

The settling behaviour of the circuit can be visualized by providing a delayed pulse on the positive voltage supply of the amplifier and taking a look at the output. This is shown in

figure 27. It can be seen that the amplifier does not deal well with impulsive changes in the power supply voltage.

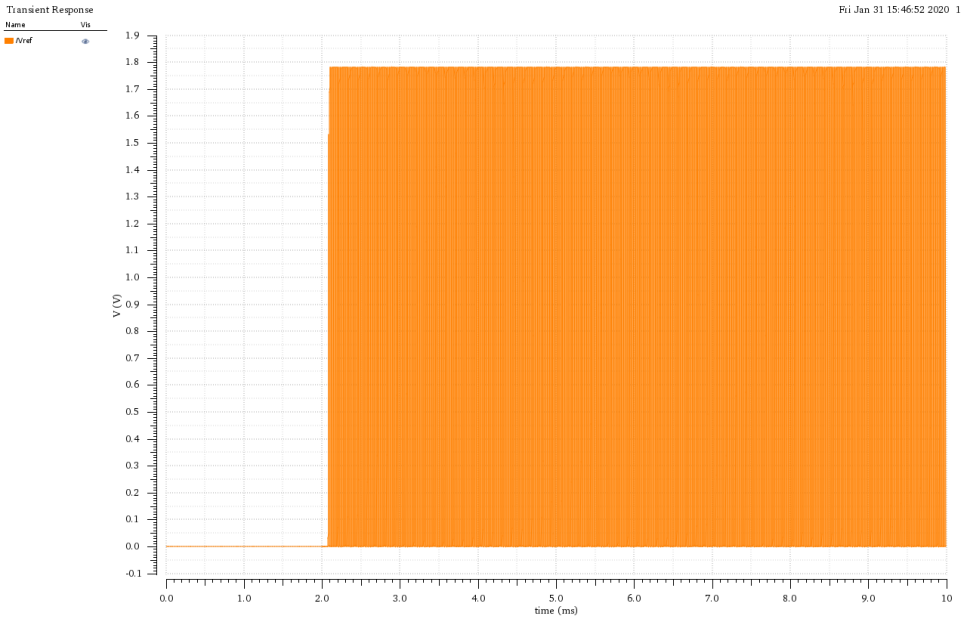

Figure 27: The response of the circuit to a delayed pulse voltage applied at the positive power supply pin of the amplifier .

8.2.8 Power consumption

The power consumption of the circuit can be visualized by performing a simple DC operating point analysis and taking a look at the power supplied by the source as figure 28 shows. The power consumption of the circuit is 362.5 µW.

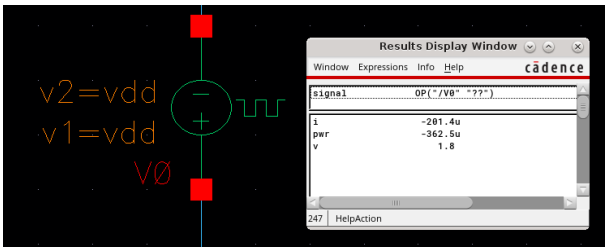

Figure 28: The response of the circuit to a delayed pulse voltage applied at the positive power supply pin of the amplifier .

8.3 Summary

Table 5 summarizes all the performance metrics of the designed bandgap circuit.

Parameter	Value
Output voltage	1.23 V
PSRR	81.1 dB
Temperature dependence	$27.7\,\mu V\,^{\circ}C^{-1}$
Output voltage with V_{TH} mismatch	1.78 V
Output voltage with 100 µA current draw	1.22 V
Power Consumption	362.5 µW

Table 5: A summary of all the simulated parameters of the designed operational amplifier.

9 Conclusion

This report details the design of a Bandgap voltage reference that is temperature independent and provides a constant voltage of 1.23 V. It is designed in a 0.18 µm process. The lab illustrates the design flow of a typical analog circuit and what tradeoffs must be made in the circuit in order to get the required performance. The process variations and parasitics also play a role in the yield of the fabricated design and knowledge of the process technology is also a pre-requisite for the designer.

Concering this particular not all the requirements were met but certain tradeoffs and fine tuning can ensure that the circuit performs in accordance with the given requirements. For example the power consumption can be reduced by effectively selecting a value for the bias currents as well as tuning the $\frac{W}{L}$ ratio of the output stage. The temperature sensitivity of the circuit can also be improved by desiging a suitable curvature compensation circuit. The settling behaviour of the circuit can be improved by making the amplifier more stable in the feedback configuration.

Overall this lab provides a fundamental overview on how to proceed circuit design from a practical standpoint. All these design steps require careful effort as well as experience and intuition which are the attributes of a great design engineer.