

6

IC MOSFET Amplifiers

Syllabus

IC amplifiers- IC biasing current steering circuit using MOSFET- MOSFET current sources- PMOS and NMOS current sources. Amplifier with active loads - Enhancement load, Depletion load and PMOS and NMOS current sources load- CMOS common source and source follower- CMOS differential amplifier- CMRR.

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6.1 IC Biasing

In integrated circuit designs biasing circuits use constant-current sources. Here, the constant d.c. current called **reference current** is generated at one location and is then replicated at various other locations for biasing the various stages of amplifier present in the circuit. This process is known as **current steering**.

Advantages of current steering process

- The external components such as precision resistors required to generate a predictable and stable reference current, need not be repeated for every amplifier stage.
- The bias currents of the various stages track each other when there is any change due to power-supply voltage or temperature.

Review Questions

- Define current steering.
- State the advantages of current steering.

6.2 MOSFET Current Sources

Fig. 6.2.1 shows the circuit of a MOSFET constant-current source. It uses two MOSFETs T_1 and T_2 . Since the drain and gate of MOSFET T_1 is shorted, it is operated in saturation region. Neglecting channel length modulation ($\lambda = 0$), the drain current of T_1 is given by

$$\begin{aligned} I_{\text{REF}} &= I_{D1} \\ &= \frac{1}{2} K'_{n1} \left(\frac{W_1}{L_1} \right) (V_{GS} - V_{T1})^2 \quad \dots(6.2.1) \\ &= K_{n1} (V_{GS} - V_{T1})^2 \\ V_{GS} &= V_{T1} + \sqrt{\frac{I_{\text{REF}}}{K_{n1}}} \end{aligned}$$
...(6.2.2)

Looking at circuit in Fig. 6.2.1 we can also write

$$I_{D1} = I_{\text{REF}} = \frac{V_{DD} - V_{GS}}{R} \quad \dots(6.2.3)$$

where I_{REF} is a reference current of the current source.

The MOSFET T_2 has the same V_{GS} as T_1 ; thus, if we assume that it is operating in saturation we have,

$$\begin{aligned} I_o &= I_{D2} = \frac{1}{2} K'_{n2} \left(\frac{W_2}{L_2} \right) (V_{GS} - V_{T2})^2 \\ &= K_{n2} (V_{GS} - V_{T2})^2 \end{aligned} \quad \dots(6.2.4)$$

Since $V_{GS1} = V_{GS2}$ and substituting value of V_{GS} from equation (6.2.2) we have,

$$I_o = K_{n2} \left(V_{T1} + \sqrt{\frac{I_{REF}}{K_{n1}}} - V_{T2} \right)^2$$

Here also we have neglected the effect of channel length modulation ($\lambda = 0$).

Taking ratio of equations (6.2.1) and (6.2.4) we have

$$\frac{I_o}{I_{REF}} = \frac{I_{D2}}{I_{D1}} = \frac{(W_2 / L_2)}{(W_1 / L_1)} \quad \dots(6.2.5)$$

For identical MOSFETs, $(W_2 / L_2) = (W_1 / L_1)$ and hence $I_o = I_{REF}$. In such situation, the circuit simply replicates or mirrors the reference current in the output terminal. For this reason, when two MOSFETs are identical, the circuit shown in Fig. 6.2.1 is known as **MOSFET current mirror circuit**.

Effect of V_o on I_o

- To ensure that, T_2 is operated in saturation,

$$V_o \geq V_{GS} - V_T \quad \dots(6.2.6)$$

or $V_o \geq V_{ov}$... (6.2.7)

where V_{ov} is the **override voltage**.

- In the initial analysis we have neglected the effect of channel length modulation. However, it has significant effect on the operation of the current source circuit.
- For identical MOSFETs, $I_o = I_{REF}$ and $V_o = V_{GS}$. As V_o increases above this value, I_o also increases according to the incremental output resistance r_{o2} of T_2 . It is given by

$$R_o = r_{o2} = \frac{\Delta V_{DS2}}{\Delta I_o} = \frac{\Delta V_o}{\Delta I_o} = \frac{V_{A2}}{I_o} = \frac{1}{\lambda_2 I_o} \quad \dots(6.2.8)$$

where V_{A2} is the early voltage of T_2 and is proportional to the channel length of the MOSFET. λ is the channel length modulation parameter and $\lambda = \frac{1}{V_A}$.

- For ideal current source $R_o \rightarrow \infty$. To keep R_o as high as possible, MOSFETs used for current source have relatively long channels. Finally, the output current of current source circuit is given by

$$I_o = \frac{(W_2 / L_2)}{(W_1 / L_1)} I_{REF} \left(1 + \frac{V_o - V_{GS}}{V_{A2}} \right)$$

Example 6.2.1 Design the MOSFET current source circuit for following specifications :

$V_{DD} = 4$ V, $I_{REF} = 120 \mu A$, $L_1 = L_2 = 1 \mu m$, $W_1 = W_2 = 10 \mu m$, $V_T = 0.7$ V and $K'_n = 200 \mu A/V^2$. Find the value of R , calculate the lowest possible value of V_o and calculate r_{o2} if early voltage $V'_{A2} = 20$ V/ μm . Also, find the change in the output current if change in V_o is + 2 V.

Solution : Since $L_1 = L_2$ and $W_1 = W_2$ MOSFETs are identical and $I_o = I_{REF} = 120 \mu A$

$$I_{D1} = I_{REF} = \frac{1}{2} K'_n \left(\frac{W_1}{L_1} \right) (V_{GS} - V_T)^2$$

$$120 = \frac{1}{2} \times 200 \times 10 (V_{GS} - V_T)^2$$

$$\therefore (V_{GS} - V_T)^2 = V_{ov}^2 = 0.12$$

$$\therefore V_{ov} = 0.3464 \text{ V}$$

$$\therefore V_{GS} = V_T + V_{ov} = 0.7 + 0.3464 = 1.0464 \text{ V}$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{4 - 1.0464}{120 \times 10^{-6}} = 24.61 \text{ k}\Omega$$

$$V_{omin} = V_{ov} = 0.3464 \text{ V}$$

$$V_{A2} = V'_{A2} \times L_2 = 20 \times 1 = 20 \text{ V}$$

$$\therefore r_{o2} = \frac{V_{A2}}{I_o} = \frac{20}{120 \mu A} = 166.67 \text{ k}\Omega$$

$$\Delta I_o = \frac{\Delta V_o}{r_{o2}} = \frac{2 \text{ V}}{166.67 \text{ k}\Omega} = 12 \mu A$$

Example 6.2.2 Design a MOSFET current source amplifier for following specifications :

$V_{DD} = + 5$ V, $K'_n = 40 \mu A/V^2$, $V_T = 1$ V, $\lambda = 0$, $I_{REF} = 0.2$ mA, $I_o = 0.1$ mA and

$V_{DS2(sat)} = 0.8$ V

Solution : Given : $V_{DS2(sat)} = V_{ov} = 0.8$ V

$$\therefore V_{GS2} = V_{ov} + V_T = 0.8 + 1.0 = 1.8 \text{ V}$$

We have,

$$I_o = \frac{1}{2} K'_n \left(\frac{W_2}{L_2} \right) (V_{GS2} - V_T)^2$$

$$\therefore \frac{W_2}{L_2} = \frac{I_o}{\frac{1}{2} K'_n (V_{GS2} - V_T)^2} = \frac{0.1 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (1.8 - 1)^2} = 7.81$$

$$I_{REF} = \frac{1}{2} \left(\frac{W_1}{L_1} \right) K'_n (V_{GS1} - V_T)^2$$

$$\therefore \frac{W_1}{L_1} = \frac{I_{REF}}{\frac{1}{2} K'_n (V_{GS1} - V_T)^2}$$

Since $V_{GS1} = V_{GS2}$ we have,

$$\frac{W_1}{L_1} = \frac{0.2 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (1.8 - 1)^2} = 15.62$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{5 - 1.8}{0.2 \times 10^{-3}} = 16 \text{ K}$$

Replacing R by another MOSFET

Fig. 6.2.2 shows the MOSFET constant current source circuit with R replaced by another MOSFET. Here, MOSFET is configured like a resistor.

Since T_1 and T_3 are connected in series $I_{D1} = I_{D3}$. Neglecting channel length modulation ($\lambda = 0$) we can write,

$$K_n (V_{GS1} - V_{T1})^2 = K_{n3} (V_{GS3} - V_{T3})^2 \quad \dots (\text{i})$$

From the circuit we have

$$V_{GS1} + V_{GS3} = V_{DD} \quad \dots (\text{ii})$$

Load current I_o with $\lambda = 0$ can be given by

$$I_o = \frac{K'_n}{2} \left(\frac{W_2}{L_2} \right) (V_{GS2} - V_T)^2$$

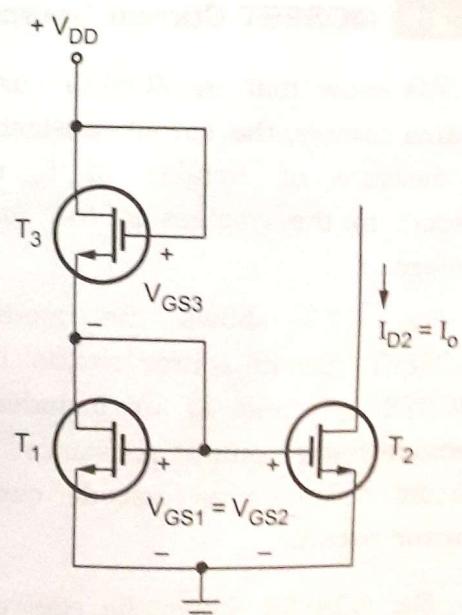


Fig. 6.2.2 MOSFET constant current source

Example 6.2.3 For MOSFET constant current source shown in Fig. 6.2.2, $V_{DD} = 5$ V, $V_T = 1$ V, $K_n' = 40 \mu A/V^2$, $I_{REF} = 0.4$ mA and $I_o = 0.2$ mA. Assuming $\lambda = 0$ and T_2 remains biased in the saturation region for $V_{DS2} \geq 1$ V, design the circuit.

Solution : Given : $V_{DS2(sat)} = 1$ $\therefore V_{GS2} = V_{GS2} + V_T = 1 + 1 = 2$ V

$$\frac{W_2}{L_2} = \frac{I_o}{\frac{K_n'}{2}(V_{GS2} - V_T)^2} = \frac{0.2 \times 10^{-3}}{\frac{40 \times 10^{-6}}{2}(2-1)^2} = 10$$

$$I_{REF} = \frac{1}{2} \left(\frac{W_1}{L_1} \right) K_n' (V_{GS1} - V_T)^2$$

Since $V_{GS1} = V_{GS2} = 2$ V, we have

$$\frac{W_1}{L_1} = \frac{0.4 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (2-1)^2} = 20$$

$$V_{GS3} = V_{DD} - V_{GS1} = 5 - 2 = 3 \text{ V}$$

Since $I_{D1} = I_{D3} = I_{REF}$ we have

$$\frac{W_3}{L_3} = \frac{I_{REF}}{\frac{1}{2} K_n' (V_{GS3} - V_T)^2} = \frac{0.4 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (3-1)^2} = 5$$

6.2.1 MOSFET Current Source Circuit - Cascode Current Mirror

We know that, in MOSFET current source circuits, the output resistance is a measure of stability of I_o with respect to the changes in the output voltage.

Fig. 6.2.3 shows the modified MOSFET current source circuit. Here MOSFETs T_3 and T_4 are included to provide higher output resistance. This circuit is known as **cascode current mirror circuit**.

Fig. 6.2.4 (a) shows the equivalent circuit of the MOSFET cascode current mirror to obtain the output resistance.

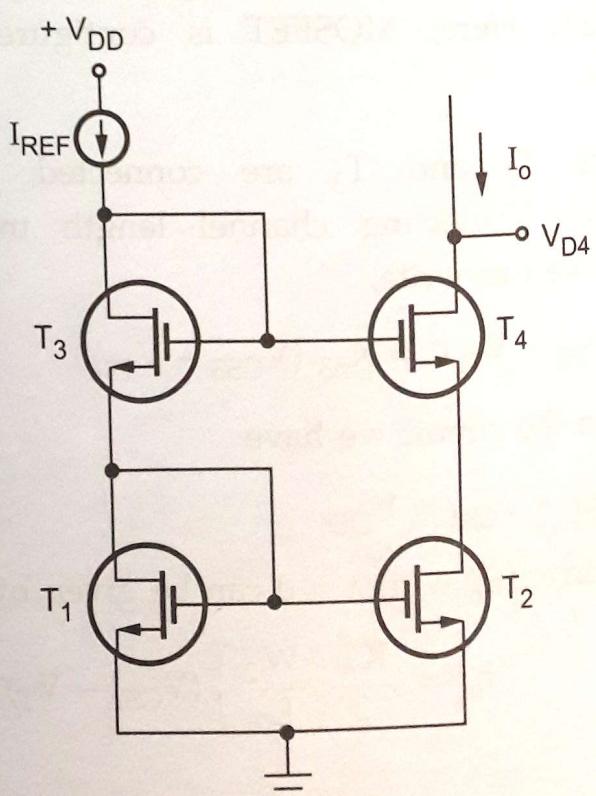


Fig. 6.2.3 MOSFET cascode current mirror circuit

Since gate voltages for T_1 and T_3 and hence for T_2 and T_4 are constant, they are shown grounded for a.c. circuits.

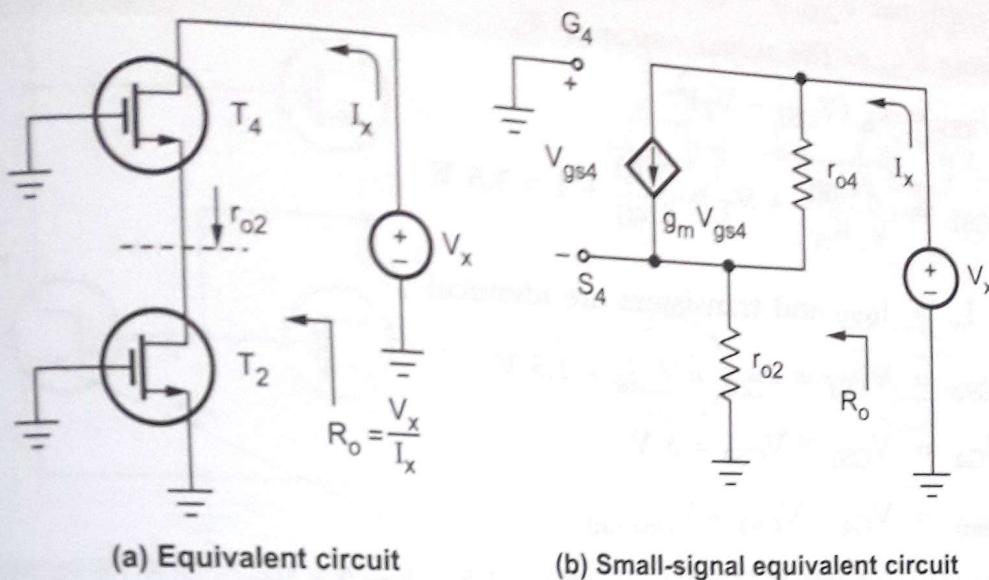


Fig. 6.2.4

Fig. 6.2.4 (b) shows the small-signal equivalent circuit to obtain R_o . Here T_2 is replaced by equivalent resistance, r_{o2} .

Applying KCL to output node we have

$$I_x = g_m V_{gs4} + \frac{V_x - (-V_{gs4})}{r_{o4}} \quad \dots(6.2.9)$$

Looking at the Fig. 6.2.4 (b) we can write,

...(6.2.10)

$$V_{gs4} = -I_x r_{o2}$$

Substituting value of V_{gs4} from equation (6.2.10) in equation (6.2.9), we have

$$I'_o = -g_m I_x r_{o2} + \frac{V_x - (I_x r_{o2})}{r_{o4}} \quad \dots(6.2.11)$$

$$\therefore I_x + g_m I_x r_{o2} + \frac{I_x r_{o2}}{r_{o4}} = \frac{V_x}{r_{o4}}$$

$$\begin{aligned} R_o &= \frac{V_x}{I_x} = r_{o4} + g_m r_{o2} r_{o4} + r_{o2} \\ &= r_{o4} + (1 + g_m r_{o4}) r_{o2} \end{aligned} \quad \dots(6.2.12)$$

Since $g_m r_{o2} \gg 1$, the output resistance of the cascode current mirror is much greater than basic two MOSFET current source.

Example 6.2.4 In the MOSFET cascode current source, all transistors are identical and, transistor and circuit parameters are as follows : $V_T = 1V$, $K_n = 40 \mu A/V^2$, $\lambda = 0.02 V^{-1}$, $I_{REF} = 10 \mu A$ and $V_{DD} = + 10 V$. Find : a) V_{GS} of each MOSFET b) The lowest possible voltage value V_{D4} c) The output resistance R_o .

Solution : $I_{REF} = K_n (V_{GS1} - V_T)^2$

$$\therefore V_{GS1} = \sqrt{\frac{I_{REF}}{K_n}} + V_T = \sqrt{\frac{10}{40}} + 1 = 1.5 \text{ V}$$

Since $I_o = I_{REF}$ and transistors are identical

$$V_{GS2} = V_{GS1} = V_{GS3} = V_{GS4} = 1.5 \text{ V}$$

$$V_{G4} = V_{GS1} + V_{GS3} = 3 \text{ V}$$

$$V_{D4(\min)} = V_{G4} - V_{GS4} + V_{DS4(\text{sat})}$$

$$\text{where, } V_{DS4} = V_{GS4} - V_T = 1.5 - 1 = 0.5 \text{ V}$$

$$\therefore V_{D4(\min)} = 3 - 1.5 + 0.5 = 2 \text{ V}$$

$$r_o = \frac{1}{\lambda I_{REF}} = \frac{1}{0.02 \times 10 \times 10^{-6}} = 5 \text{ M}\Omega$$

For cascode circuit we have,

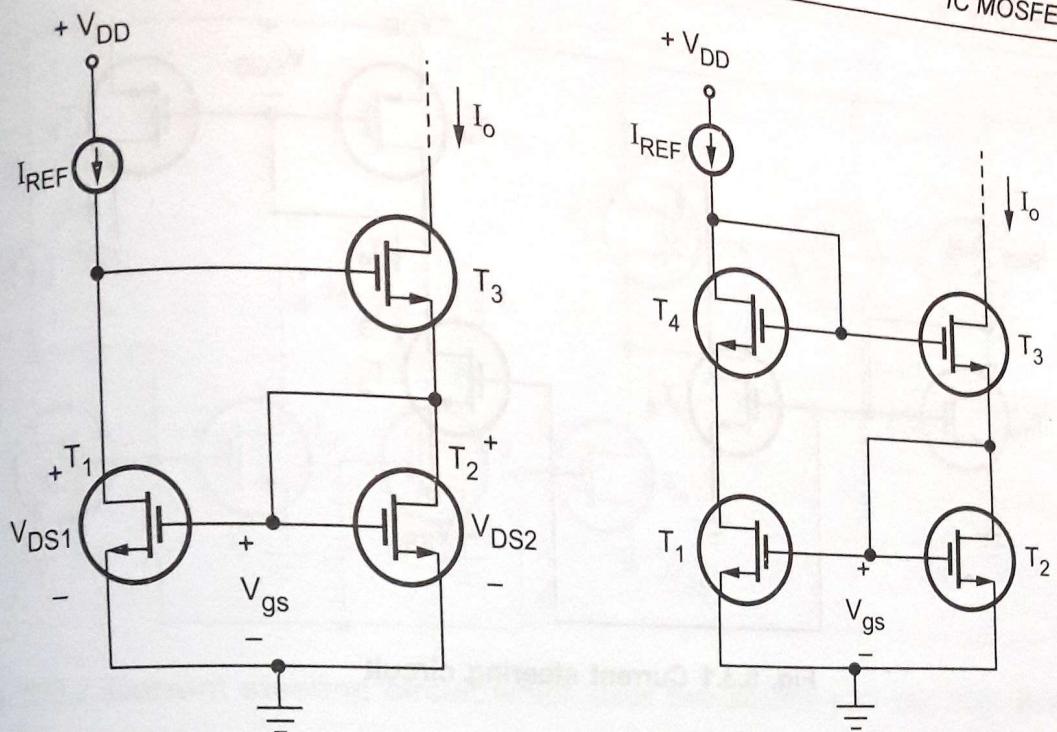
$$r_o = r_{o2} = r_{o4} = 5 \text{ M}\Omega$$

$$g_m = 2 \sqrt{K_n I_D} = 2 \sqrt{40 \times 10^{-6} \times 10 \times 10^{-6}} = 0.04 \text{ mA/V}$$

$$\begin{aligned} \therefore R_o &= r_{o4} + (1 + g_m r_{o4}) r_{o2} \\ &= 5 \times 10^6 + (1 + 0.04 \times 10^{-3} \times 5 \times 10^6) \times 5 \times 10^6 \\ &= 1010 \text{ M}\Omega \end{aligned}$$

6.2.2 Wilson Current Mirror

Fig. 6.2.5 shows MOSFET Wilson current source and modified MOSFET Wilson current source circuits. In MOSFET Wilson current source, the V_{DS} values of T_1 and T_2 are not equal. Since λ is not zero, the ratio I_o/I_{REF} is slightly different from the aspect ratio. The modified MOSFET Wilson current circuit solves this problem by including T_4 . The advantages of these circuits is the increase in output resistance and hence to increase the stability of output current.



(a) MOSFET Wilson current source

(b) Modified MOSFET Wilson current source

Fig. 6.2.5

Review Questions

1. Draw and explain the basic constant current source circuit using MOSFET.
2. Define override voltage.
3. Derive the expression for I_o of current source circuit using MOSFET.
4. Draw and explain MOSFET constant current source circuit with active load.
5. Draw and explain the cascode current mirror circuit using MOSFETs.
6. Derive the expression for output resistance of cascode current mirror circuit.
7. State the advantage of cascode current mirror circuit.
8. Draw and explain the Wilson current mirror circuit.
9. State the advantage of Wilson current mirror circuit.

Dec.-14

6.3 MOSFET Current Steering Circuit

The constant current source can be replicated to provide dc bias currents for the various amplifier stages. Fig. 6.3.1 shows a simple current steering circuit. Here, T_1 together with R determines the reference current I_{REF} and transistors T_1 , T_2 and T_3 form a two-output current mirror.

From equation (6.2.5) we have

$$I_2 = I_{REF} \frac{(W_2 / L_2)}{(W_1 / L_1)} \quad \dots(6.3.1)$$

$$I_3 = I_{REF} \frac{(W_3 / L_3)}{(W_1 / L_1)} \quad \dots(6.3.2)$$

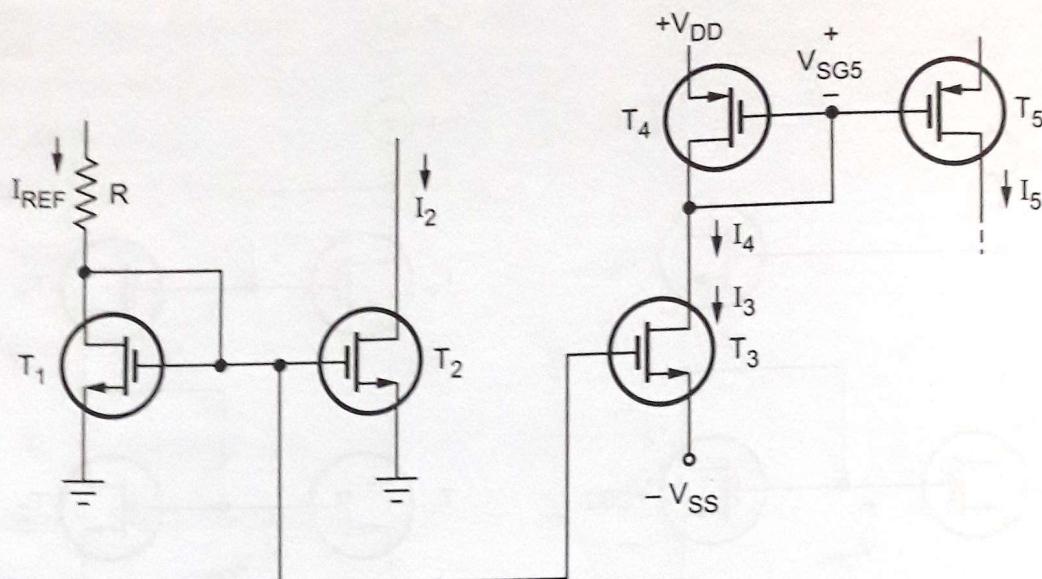


Fig. 6.3.1 Current steering circuit

For T_2 and T_3 to operate in saturation

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_T \quad \dots(6.3.3)$$

$$\text{or } V_{D2}, V_{D3} \geq -V_{SS} + V_{ov1} \quad \dots(6.3.4)$$

Look at Fig. 6.3.1 we see that current I_3 is fed to the input side of a current mirror formed by PMOS transistors T_4 and T_5 . For this mirror

$$I_5 = I_4 \frac{(W_5 / L_5)}{(W_4 / L_4)}$$

where $I_4 = I_3$ and to keep T_5 in saturation,

$$V_{D5} \leq V_{DD} - |V_{ov5}|$$

where V_{ov5} is the override voltage at which T_5 is operating.

In the above current steering circuit T_2 pulls the current I_2 from the load and hence acts as a **current sink**. On the other hand, T_5 pushes the current I_5 into a load and hence acts as a **current source**.

A single reference current can be replicated to bias several amplifiers stages in a multistage amplifiers, as shown in Fig. 6.3.2. Here, the current I_4 is used to generate bias voltage V_{SG} using diode connected MOSFET T_5 . This voltage, in turn, is used to bias T_6 and T_7 to generate the drain currents from these two MOSFETs. These currents from the positive supply can be used to drive active loads and hence T_6 and T_7 act as a current source. MOSFETs T_2 and T_3 pull the current I_2 and I_3 , respectively from the load and hence act as a current sink.

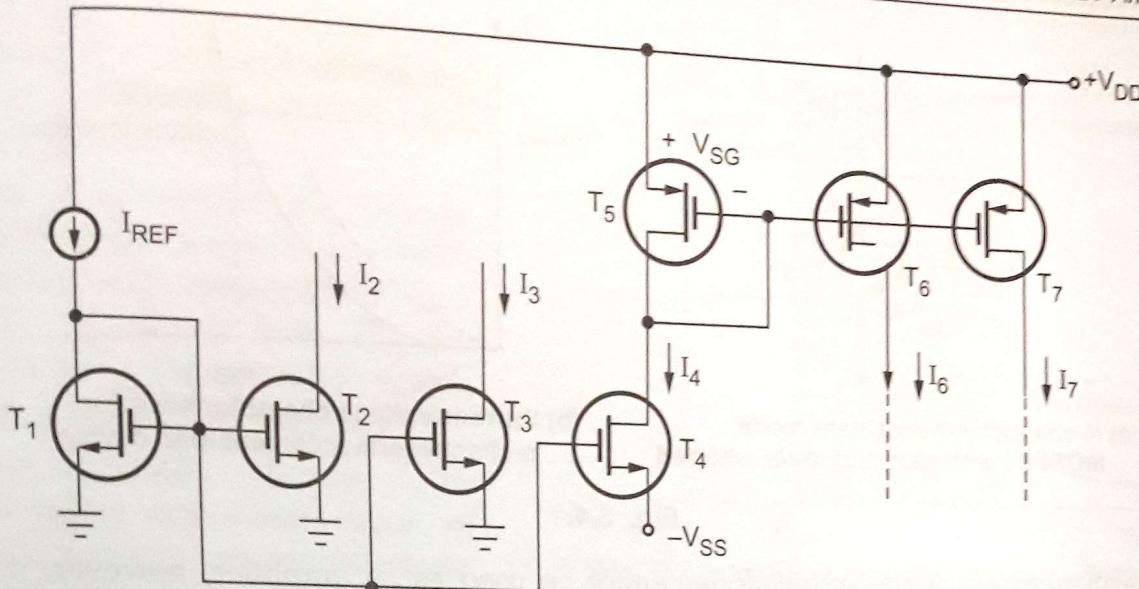


Fig. 6.3.2 Current steering circuit which uses two source and two sink terminals

Review Questions

1. Draw and explain the MOSFET current steering circuit.
2. Draw a MOS current steering circuit with two sink and two source terminals. Write the expression for the terminal currents in terms of reference current.

Dec.-14, Marks 16

6.4 Amplifiers with Active Load

Dec.-14

When MOSFET itself is used as a load device, it is referred to as **active load**. There are three types of load devices :

- n-channel enhancement mode device
- n-channel depletion-mode device
- p-channel enhancement mode device

6.4.1 NMOS Amplifier with Enhancement Load

Fig. 6.4.1 (a) shows an n-channel enhancement mode MOSFET with gate and drain shorted. In this connection, MOSFET acts as a non-linear resistor and is called **enhancement load device**. Since MOSFET is in enhancement mode $V_T > 0$. For this circuit $V_{DS(sat)} = V_{GS} - V_T$ which means that the MOSFET is always biased in the saturation region.

Fig. 6.4.1 (b) shows the current-voltage characteristics for n-channel enhancement load device. The characteristics is a plot of equation

$$i_D = K_n (V_{GS} - V_T)^2$$

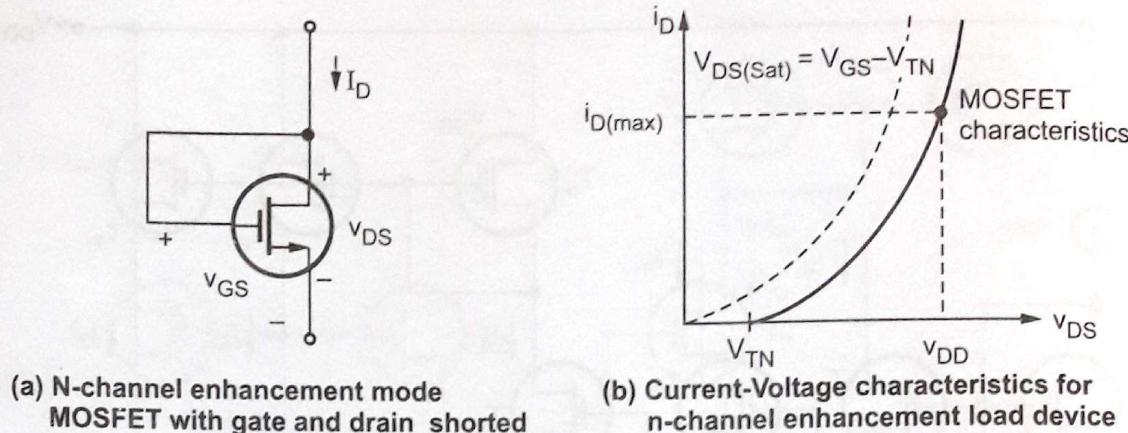


Fig. 6.4.1

The enhancement load circuit alone cannot be used as an amplifier, however, if it is connected in a circuit with another MOSFET in the configuration shown in Fig. 6.4.2 (a), the circuit can be used as an amplifier or as an inverter in a digital circuit.

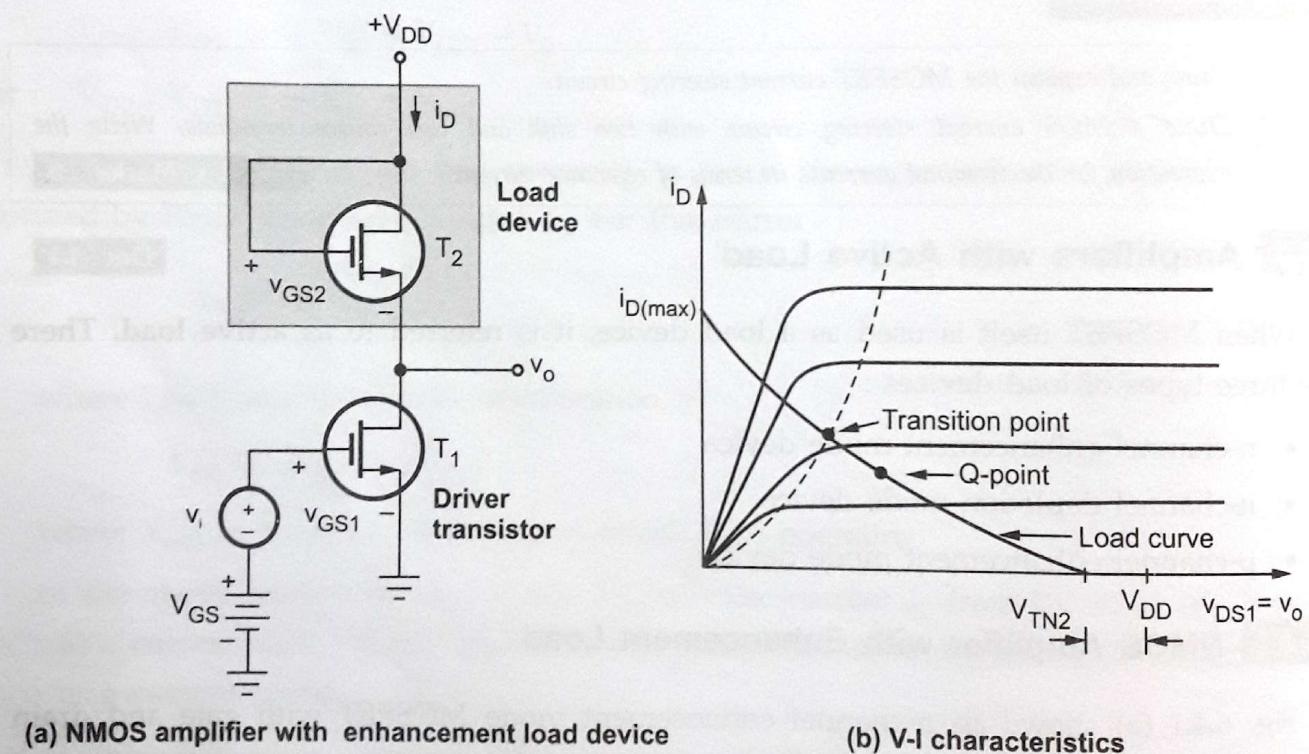


Fig. 6.4.2

Here, MOSFET T_2 is used as a load and MOSFET T_1 is used as a driver transistor. The load device T_2 is always biased in the saturation region. The characteristics of driver transistor T_1 and the load curve are shown in Fig. 6.4.2 (b). Since the i - v characteristics of the load device (See Fig. 6.4.1 (b)) is non-linear, the load curve is also non-linear.

At $V_{DD} - V_{TN2}$, the load curve intersects the voltage axis and the current in the enhancement load device goes to zero.

Fig. 6.4.3 shows the voltage transfer characteristics of NMOS amplifier with enhancement load device. It shows that, Q-point should be in the saturation region to use circuit as an amplifier.

Fig. 6.4.4 shows the small-signal equivalent circuit of NMOS inverter with enhancement load device.

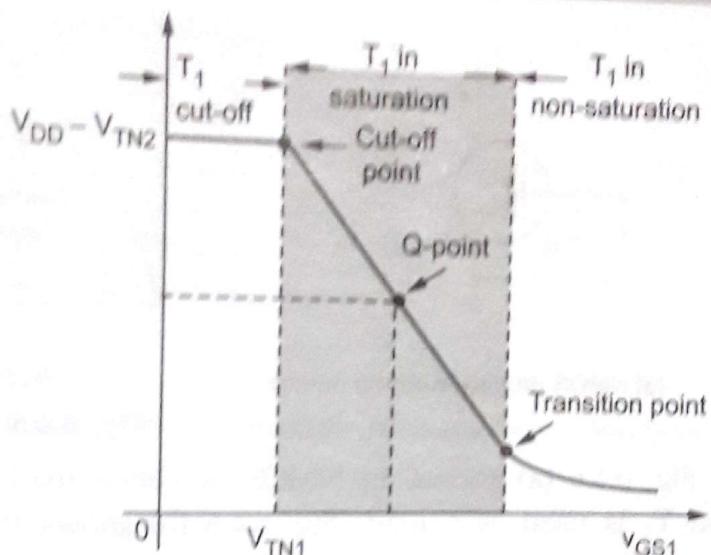


Fig. 6.4.3 Voltage transfer characteristics

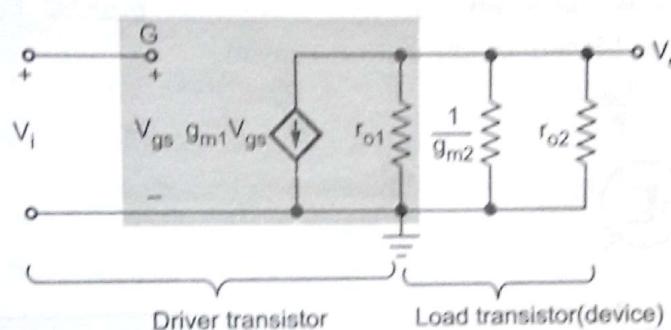


Fig. 6.4.4 Small signal equivalent circuit

For the circuit shown in Fig. 6.4.4,

$$R_i = \infty \quad \dots(6.4.1)$$

$$R_o = \frac{1}{g_m 2} \parallel r_{o2} \quad \dots(6.4.1)$$

$$A_v = \frac{V_o}{V_i} = - g_m 1 \left(r_{o1} \parallel \frac{1}{g_m 2} \parallel r_{o2} \right) \quad \dots(6.4.2)$$

Since, $\frac{1}{g_m 2} \ll r_{o2}$ and $\frac{1}{g_m 1} \ll r_{o1}$, the equation for voltage gain can be approximated as

$$A_v = \frac{-g_m 1}{g_m 2} = - \sqrt{\frac{K_{n1}}{K_{n2}}} = - \sqrt{\frac{(W_1 / L_1)}{(W_2 / L_2)}} \quad \dots(6.4.3)$$

The above equation shows that the voltage gain is related to the size of the transistor. Since, the voltage gain is related to the size of the transistor with a square root function, it is limited. To obtain larger voltage gain we can use depletion-mode MOSFET.

6.4.2 NMOS Amplifier with Depletion Load

Fig. 6.4.5 (a) shows the NMOS depletion mode transistor connected as a load device and Fig. 6.4.5 (b) shows current-voltage characteristics. Here, threshold voltage V_{TN2} is negative, which means that the value of V_{DS} at transition point is positive. Non-zero slope in the saturation region indicates that a finite resistance r_o exists in this region.

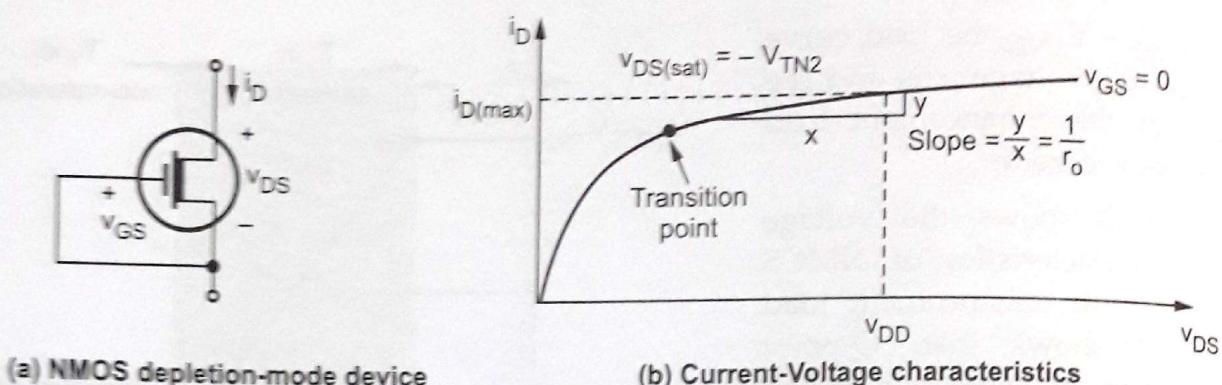


Fig. 6.4.5

Fig. 6.4.6 (a) shows an NMOS depletion load amplifier. Here, T_1 is used as a driver and T_2 is used as a load. Fig. 6.4.6 (b) shows the characteristics of T_1 and load curve. Since the i-v characteristics of the load device is non-linear, the load curve is also non-linear. Points A and B are transition points for T_1 and T_2 , respectively. The Q-point is approximately midway between the two transition points. For amplifier operation, both MOSFET should be biased in saturation region.

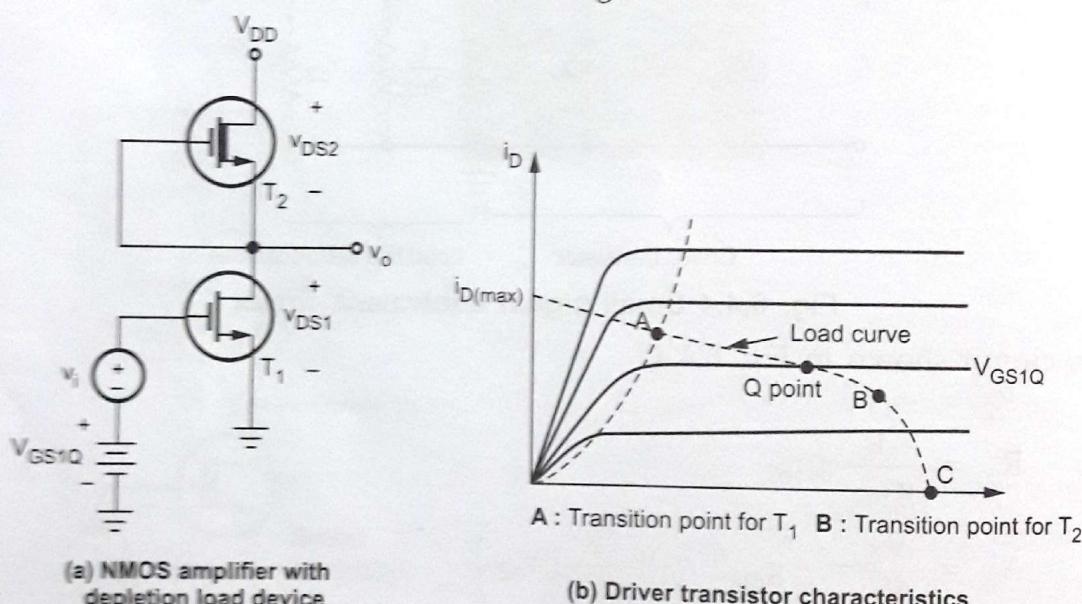


Fig. 6.4.6

Fig. 6.4.7 shows the voltage transfer characteristics for NMOS amplifier. As shown in the Fig. 6.4.7, the Q point lies in the saturation region.

Fig. 6.4.8 shows the small-signal equivalent circuit of NMOS inverter with depletion load device. Since the gate to source voltage for depletion load (T_2) is zero, $g_m V_{gs2} = 0$.

Looking at Fig. 6.4.8, we have

$$V_o = -g_m V_{gs} (r_{o1} \parallel r_{o2})$$

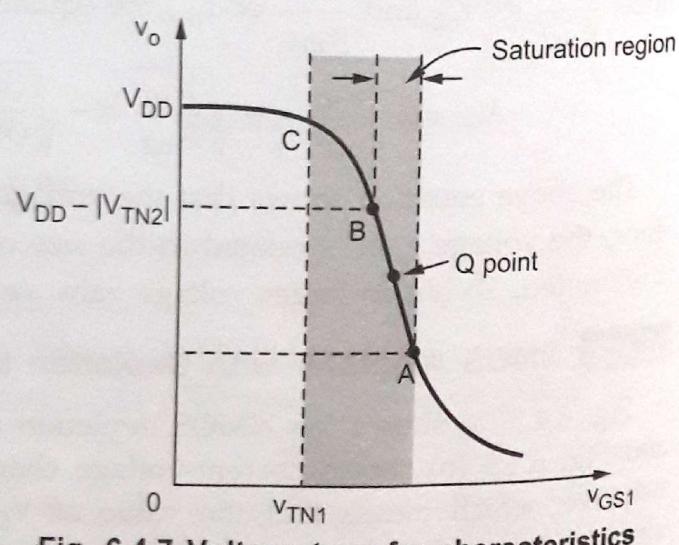


Fig. 6.4.7 Voltage transfer characteristics

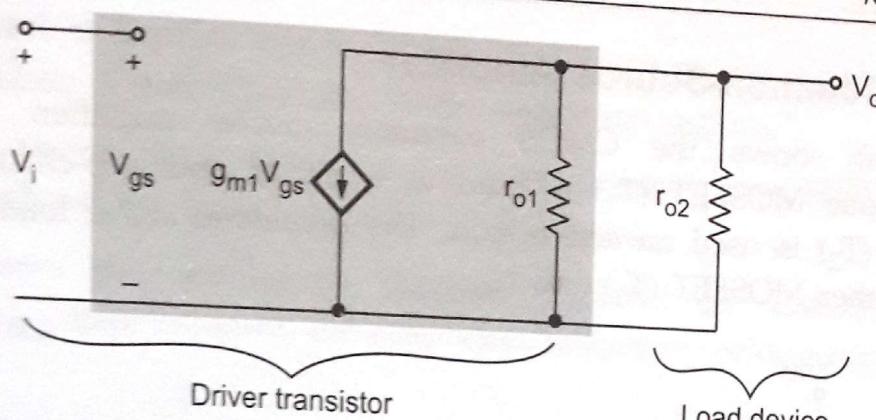


Fig. 6.4.8 Small-signal equivalent circuit of NMOS inverter with depletion load device

$$\therefore A_v = \frac{V_o}{V_i} = -g_{m1} (r_{o1} \parallel r_{o2}) \quad \therefore V_i = V_{gs} \quad \dots(6.4.4)$$

Thus, for this circuit, the voltage gain is directly proportional to the output resistances of two transistors.

Example 6.4.1 For NMOS amplifier with depletion load, $V_{TN1} = 0.8 \text{ V}$, $V_{TN2} = -1.0 \text{ V}$, $K_{n1} = 2 \text{ mA/V}^2$, $K_{n2} = 0.2 \text{ mA/V}^2$, $I_{DQ} = 0.2 \text{ mA}$ and $\lambda_1 = \lambda_2 = 0.01 \text{ V}^{-1}$, calculate the small-signal voltage gain.

Solution : Transconductance of driver transistor T_1 is given by

$$g_{m1} = 2\sqrt{K_{n1} I_{DQ}} = 2\sqrt{(2 \times 10^{-3})(0.2 \times 10^{-3})} = 1.265 \text{ mA/V}$$

Since $\lambda_1 = \lambda_2$, the output resistances are

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2 \times 10^{-3})} = 500 \text{ k}\Omega$$

$$A_v = -g_{m1} (r_{o1} \parallel r_{o2}) = -1.265 \times 10^{-3} (500 \text{ k}\Omega \parallel 500 \text{ k}\Omega) = -316.25$$

Note The voltage gain of the NMOS amplifier with depletion load is significantly larger than that with the enhancement load. However, like NMOS amplifier with enhancement load, the body effect lowers the small-signal voltage gain.

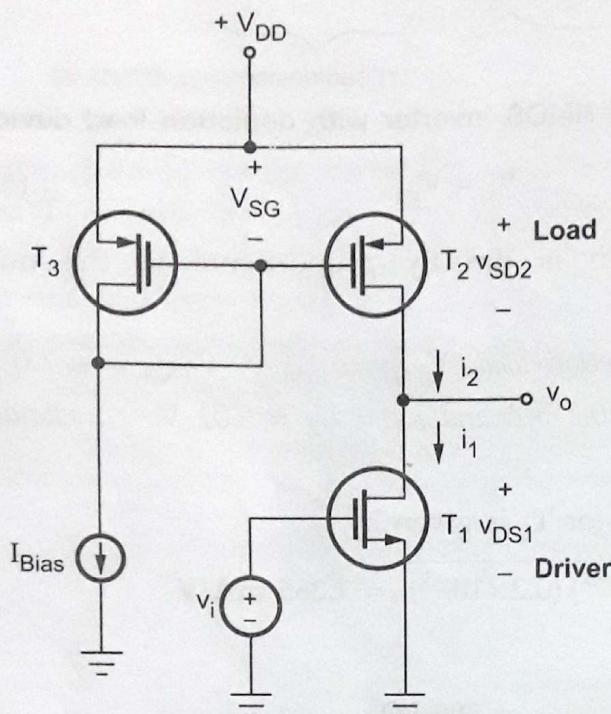
Review Questions

1. List the various types of active loads.
2. Draw and explain the NMOS amplifier with enhancement load.
3. Draw the voltage transfer characteristics of NMOS amplifier with enhancement load.
4. Derive the expression for A_v and R_o for NMOS amplifier with enhancement load.
5. State the limitation of the NMOS amplifier with enhancement load.
6. Draw and explain the NMOS amplifier with depletion load.
7. Draw the voltage transfer characteristics of NMOS amplifier with depletion load.
8. Derive the expression for small-signal voltage gain of NMOS amplifier with depletion load.
9. State the advantage of NMOS amplifier with depletion load over enhancement load.
10. Derive gain, input and output impedance of common source amplifier with NMOS diode connected active load.

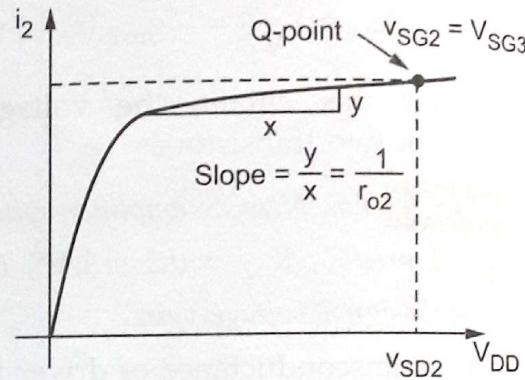
Dec.-14, Marks 16

6.5 CMOS Common-Source Amplifier

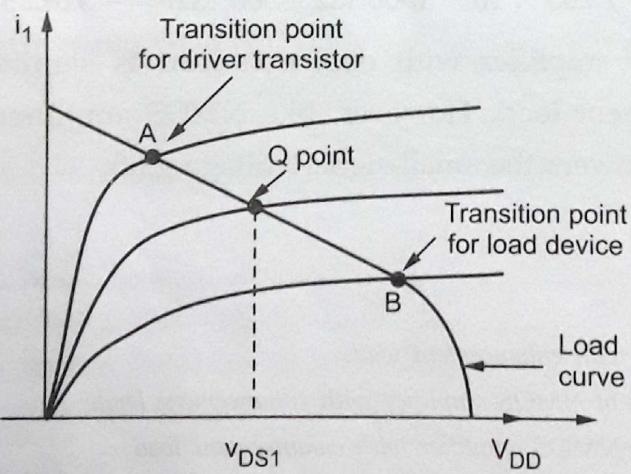
Fig. 6.5.1 (a) shows the CMOS common source amplifier. Here, n-channel enhancement mode MOSFET (T_1) is used as a driver and a p-channel enhancement mode MOSFET (T_2) is used as an active load. The p-channel active load MOSFET (T_2) is biased from another MOSFET (T_3) and I_{Bias} .



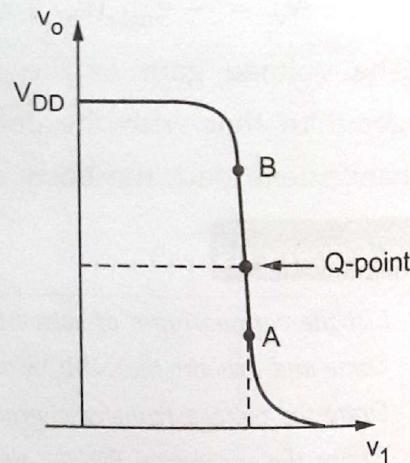
(a) CMOS common-source amplifier



(b) PMOS active-load i-v characteristics



(c) Driver transistor (T1) characteristics with load curve



(d) Voltage transfer characteristics

Fig. 6.5.1

Fig. 6.5.1 (b) shows the i-v characteristics for PMOS active load transistor (T_2). The MOSFET (T_3) and I_{Bias} is used to keep the source to gate voltage of T_2 constant. Fig. 6.5.1 (c) shows the driver transistor (T_1) characteristics with the load curve. In which point A and point B are the transition points for T_1 and T_2 , respectively. For amplifier

action, the Q-point is kept at approximately halfway between points A and B. This ensures the operation of both transistors in the saturation regions.

Fig. 6.5.1 (d) shows the voltage transfer characteristics for CMOS common-source amplifier. It also shows the transition points and Q-point.

Fig. 6.5.2 shows the small-signal equivalent circuit for CMOS common-source amplifier. With v_{SG2} kept constant, the equivalent resistance looking into the drain of T_2 is r_{o2} .

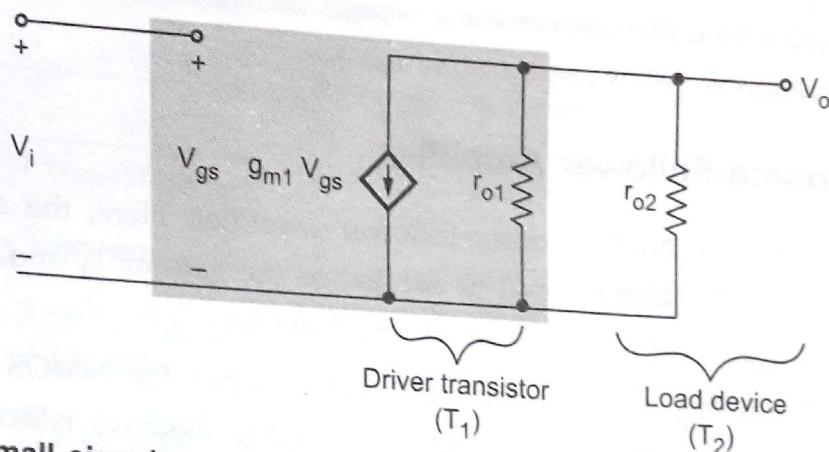


Fig. 6.5.2 Small signal equivalent circuit for the CMOS common-source amplifier

Looking at Fig. 6.5.2, we have

$$V_o = -g_{m1} V_{gs} (r_{o1} \parallel r_{o2})$$

$$\therefore A_v = \frac{V_o}{V_i} = -g_{m1} (r_{o1} \parallel r_{o2})$$

$$\dots \because V_i = V_{gs}$$

Example 6.5.1 For CMOS common-source amplifier, $K'_n = 80 \mu A/V^2$, $K'_p = 20 \mu A/V^2$, $V_{TN} = + 0.8 V$, $V_{TP} = - 1.0 V$, $(W/L)_n = 10$, $(W/L)_p = 20$, $I_{BIAS} = 0.2 mA$ and $\lambda_1 = \lambda_2 = 0.01$, find the small-signal voltage gain.

Solution : Transconductance for NMOS driver (T_1)

$$\begin{aligned} g_{m1} &= 2 \sqrt{K_n I_{DQ}} = 2 \sqrt{\left(\frac{K'_n}{2}\right) \left(\frac{W}{L}\right)_n I_{Bias}} \\ &= 2 \sqrt{\frac{80 \times 10^{-6}}{2} \times 10 \times 0.2 \times 10^{-3}} = 0.566 \text{ mA/V} \end{aligned}$$

As $\lambda_1 = \lambda_2$, the output resistances are

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_{DQ}} = \frac{1}{0.01 \times 0.2 \times 10^{-3}} = 500 \text{ k}\Omega$$

$$\therefore A_v = -g_{m1} (r_{o1} \parallel r_{o2}) = 0.566 \times 10^{-3} (500 \text{ k}\Omega \parallel 500 \text{ k}\Omega) = -141.5$$

Advantages of CMOS Common-Source Amplifier

1. Like NMOS amplifier with depletion load, CMOS common-source amplifier also provides large small-signal voltage gain.
2. CMOS amplifier does not suffer from body effect.

Review Questions

1. Draw and explain the CMOS common-source amplifier with the help of various characteristics.
2. State the advantages of CMOS common-source amplifier.

6.6 NMOS Source-Follower Amplifier

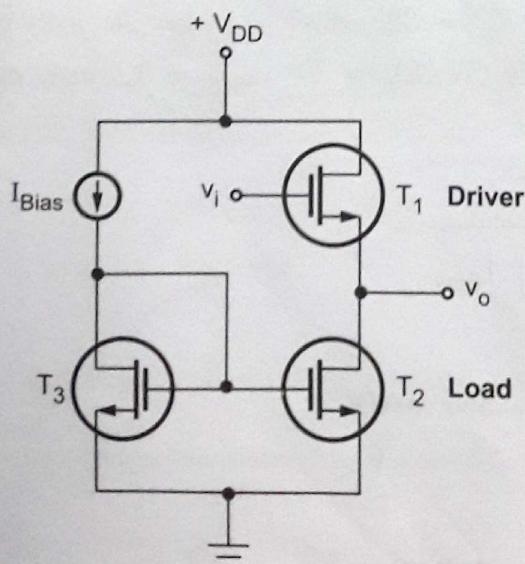
Fig. 6.6.1 (a) shows the NMOS source-follower amplifier. Here, the active load is T_2 and driver is n-channel T_1 . Input signal is applied to the gate of T_1 and output is at the source of T_1 . T_3 and I_{Bias} provides bias for the load device.

Fig. 6.6.1 (b) shows the small signal equivalent circuit for NMOS source-follower amplifier. The same equivalent circuit is redrawn in Fig. 6.6.1 (c) which combines two signal grounds. (See Fig. 6.6.1 on next page)

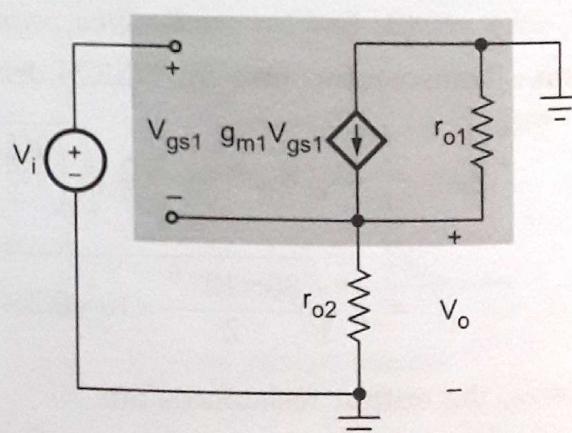
Voltage gain

Look at Fig. 6.6.1 (c) we have

$$V_o = g_{m1} V_{gs1} (r_{o1} \parallel r_{o2}) \quad \dots(6.6.1)$$



(a) NMOS source-follower amplifier



(b) Small signal equivalent circuit

Fig. 6.6.1

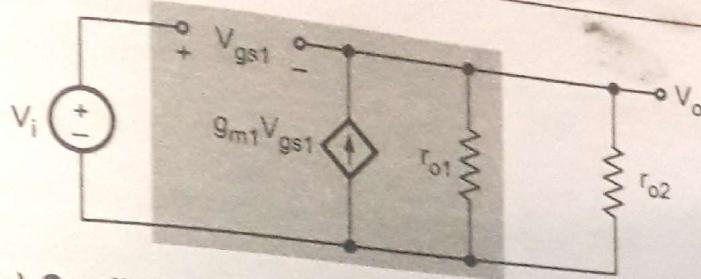


Fig. 6.6.1 (c) Small signal equivalent circuit for NMOS source follower

Applying KVL to the outer loop, we have

$$\begin{aligned} V_i &= V_{gs1} + V_o = V_{gs1} + g_{m1} V_{gs1} (r_{o1} \parallel r_{o2}) \\ V_{gs1} &= \frac{V_i}{1 + g_{m1}(r_{o1} \parallel r_{o2})} \end{aligned} \quad \dots(6.6.2)$$

Substituting V_{gs1} from equation (6.6.2) in equation (6.6.1), we have

$$V_o = \frac{g_{m1} V_i (r_{o1} \parallel r_{o2})}{1 + g_{m1}(r_{o1} \parallel r_{o2})} \quad \dots(6.6.3)$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{g_{m1} (r_{o1} \parallel r_{o2})}{1 + g_{m1}(r_{o1} \parallel r_{o2})} \quad \dots(6.6.4)$$

Output resistance

Fig. 6.6.1 (d) shows the small signal equivalent circuit to determine output resistance.

Looking at Fig. 6.6.1 (d), the currents at output node are I_x , $g_{m1} V_{gs1}$ and $V_x / (r_{o1} \parallel r_{o2})$. Applying KCL at output node,

we have

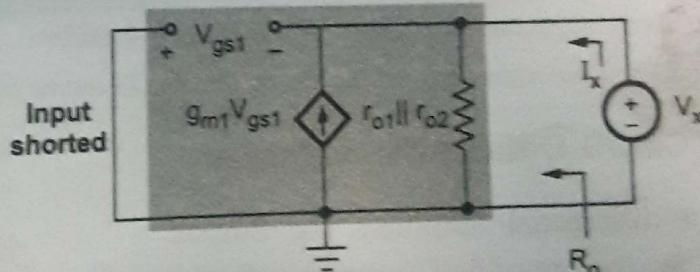
$$I_x + g_{m1} V_{gs1} = \frac{V_x}{(r_{o1} \parallel r_{o2})} \quad \dots(6.6.5)$$

From the Fig. 6.6.1 (d) we have

$$V_{gs1} = -V_x$$

Substituting value of V_{gs1} from equation (6.6.6) in equation (6.6.5), we have

$$I_x - g_{m1} V_x = \frac{V_x}{(r_{o1} \parallel r_{o2})}$$

Fig. 6.6.1 (d) Small signal equivalent circuit to obtain R_o

$$I_S = V_S \left(g_m 1 + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)$$

$$R_o = \frac{V_S}{I_S} = \frac{1}{g_m 1 || r_{o1} || r_{o2}}$$

Example 6.6.1 For NMOS source follower amplifier, $I_{Bias} = 0.4 \text{ mA}$, $V_{DD} = 5 \text{ V}$, $V_{TN} = 0.8 \text{ V}$, $K_n = 0.4 \text{ mA/V}^2$ and $\lambda = 0.01 \text{ V}^{-1}$. Calculate the voltage gain and output resistance.

Solution :

$$g_{m1} = 2 \sqrt{K_n I_D} = 2 \sqrt{0.4 \times 10^{-3} \times 0.4 \times 10^{-3}} = 0.8 \text{ mA/V}$$

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 0.4 \times 10^{-3}} = 250 \text{ k}\Omega$$

$$A_v = \frac{g_{m1} (r_{o1} || r_{o2})}{1 + g_{m1} (r_{o1} || r_{o2})} = \frac{0.8 \times 10^{-3} (250 \text{ k}\Omega || 250 \text{ k}\Omega)}{1 + 0.8 \times 10^{-3} (250 \text{ k}\Omega || 250 \text{ k}\Omega)} = 0.99$$

$$R_o = \frac{1}{g_{m1}} || r_{o1} || r_{o2} = \frac{1}{0.8 \times 10^{-3}} || 250 \text{ k}\Omega || 250 \text{ k}\Omega = 1.2376 \text{ k}\Omega$$

Review Questions

1. Draw and explain the NMOS source follower amplifier.
2. Derive the expressions for A_v and R_o for NMOS source follower amplifier.

6.7 CMOS Differential Amplifier

In a differential amplifier the output signal is the amplified version of the difference of two inputs of the amplifier.

Fig. 6.7.1 shows the CMOS differential amplifier in which a current mirror circuit is employed as an active load for the source-coupled pair. Here, transistors T_1 and T_2 are n-channel devices and forms the differential pair biased with I_Q . The load circuit consists of transistors T_3 and T_4 , both p-channel devices.

Here, (T_1, T_2) and also (T_3, T_4) are mutually identical with each other thus

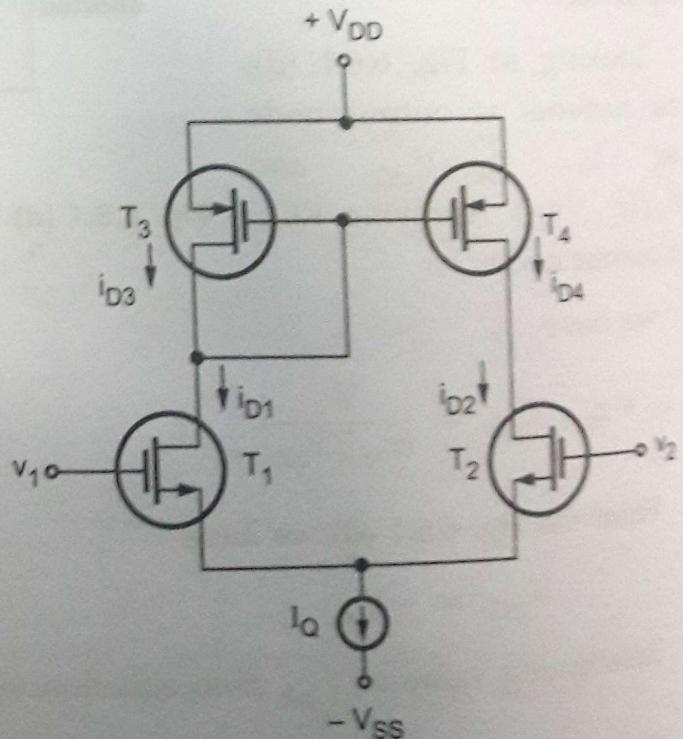


Fig. 6.7.1 CMOS differential amplifier with active load

the tail current I_Q is equally divided between $T_1(T_3)$ and $T_2(T_4)$ when a common-mode voltage of $v_1 = v_2 = v_{cm}$ is applied.

$$i_{D1} = i_{D2} = I_Q/2$$

Since gate currents are zero, $i_{D1} = i_{D3}$ and $i_{D2} = i_{D4}$(6.7.1)

When small differential-mode input voltage $v_d = v_1 - v_2$ is applied, we have

$$i_{D1} = \frac{I_Q}{2} + i_d$$

$$\text{and } i_{D2} = \frac{I_Q}{2} - i_d \quad \dots(6.7.2)$$

$$\text{where } i_d \text{ is the signal current.} \quad \dots(6.7.3)$$

Since T_1 and T_3 , and T_2 and T_4 are in series we have

$$i_{D3} = i_{D1} = \frac{I_Q}{2} + i_d \quad \dots(6.7.4)$$

$$\text{and } i_{D4} = i_{D2} = \frac{I_Q}{2} - i_d \quad \dots(6.7.5)$$

For small values of v_d , we have $i_d = g_m v_d / 2$.

Fig. 6.7.2 shows the a.c. equivalent circuit and the small-signal equivalent circuit at the drain node of T_2 and T_4 .

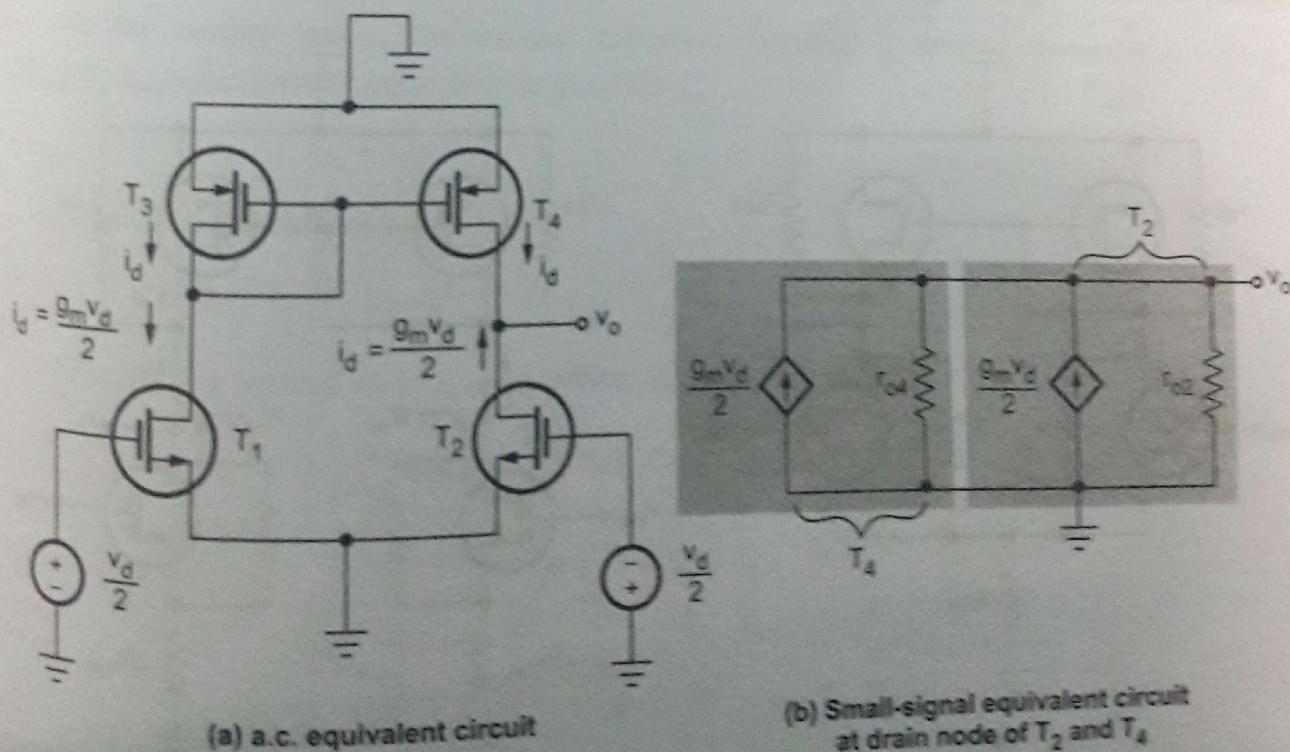


Fig. 6.7.2

Differential gain (A_d)

Looking at Fig. 6.7.2 (b) we have

$$v_o = \left(\frac{g_m v_d}{2} + \frac{g_m v_d}{2} \right) (r_{o2} \parallel r_{o4})$$

$$\therefore A_d = \frac{v_o}{v_d} = g_m (r_{o2} \parallel r_{o4}) = \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}} \quad \dots(6.7.6)$$

We have, $g_m = 2 \sqrt{K_n I_D} = \sqrt{2 K_n I_Q}$ $\therefore I_D = I_Q/2$

$$g_{o2} = \lambda_2 I_{DQ2} = \lambda_2 I_Q/2$$

$$g_{o4} = \lambda_4 I_{DQ4} = \lambda_4 I_Q/2$$

Substituting the values of g_m , g_{o2} and g_{o4} in equation (6.7.6), we have

$$A_d = \frac{\sqrt{2 K_n I_Q}}{\frac{\lambda_2 I_Q}{2} + \frac{\lambda_4 I_Q}{2}} = \frac{2 \sqrt{2 K_n I_Q}}{I_Q (\lambda_2 + \lambda_4)} = 2 \sqrt{\frac{2 K_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4} \quad \dots(6.7.7)$$

Common-mode gain (A_{cm})

Fig. 6.7.3 (a) shows the circuit with v_{cm} (common-mode voltage) applied. Here, resistance R_{SS} is the output resistance of the bias-current source I . We can split R_{SS} equally between T_1 and T_2 as shown in Fig. 6.7.3 (b).

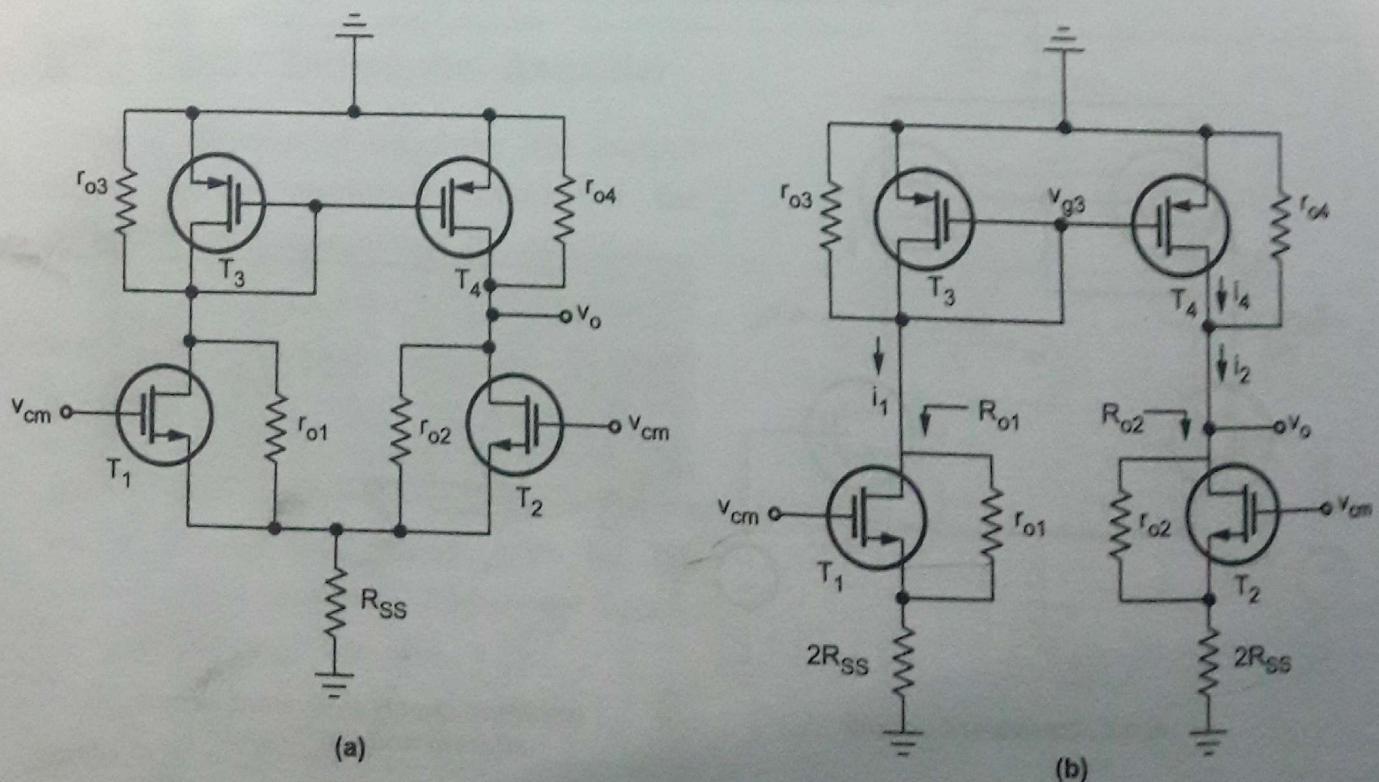


Fig. 6.7.3 Determining common-mode gain

For circuit in Fig. 6.7.3 (b) we can write

$$i_1 = i_2 \approx \frac{v_{cm}}{2R_{SS}}$$

The output resistance of each of T_1 and T_2 is given by

$$R_{o1} = R_{o2} = r_o + 2R_{SS} + 2g_m r_o R_{SS}$$

where $r_{o1} = r_{o2} = r_o$ and $g_{m1} = g_{m2} = g_m$

It is important to note that

$$R_{o1} \gg \left(r_{o3} \parallel \frac{1}{g_{m3}} \right) \quad \text{and} \quad R_{o2} \gg \left(r_{o4} \parallel \frac{1}{g_{m4}} \right)$$

Thus we can neglect R_{o1} and R_{o2} in finding the total resistance between each of the drain nodes and ground.

The current i_1 is passed through the parallel resistance of T_3 to produce voltage v_{g3} as

$$v_{g3} = -i_1 \left(\frac{1}{g_{m3}} \parallel r_{o3} \right)$$

The transistor T_4 senses this voltage and produces

$$i_4 = -g_{m4} v_{g3} = i_1 g_{m4} \left(\frac{1}{g_{m3}} \parallel r_{o3} \right)$$

At the output node, the current difference between i_4 and i_2 passes through r_{o4} ($R_{o2} \gg r_{o4}$ and hence neglected) to provide v_o .

$$\therefore v_o = (i_4 - i_2) r_{o4}$$

Substituting value of i_4 we have,

$$v_o = \left[i_1 g_{m4} \left(\frac{1}{g_{m3}} \parallel r_{o3} \right) - i_2 \right] r_{o4}$$

Substituting values of i_1 , i_2 and setting $g_{m3} = g_{m4}$ we have,

$$\begin{aligned} v_o &= \left[\frac{v_{cm}}{2R_{SS}} g_{m3} \left(\frac{1}{g_{m3}} \parallel r_{o3} \right) - \frac{v_{cm}}{2R_{SS}} \right] r_{o4} \\ &= \frac{v_{cm}}{2R_{SS}} \left[g_{m3} \left(\frac{\frac{r_{o3}}{g_{m3}}}{\frac{r_{o3}}{g_{m3}} + \frac{1}{g_{m3}}} \right) - 1 \right] r_{o4} \end{aligned}$$

... (6.7.8)

$$= \frac{v_{cm}}{2R_{SS}} \left[\frac{-1}{g_{m3} r_{o3} + 1} \right] r_{o4}$$

$$A_{cm} = \frac{V_o}{V_{cm}} = \frac{-1}{2R_{SS}} \cdot \frac{r_{o4}}{g_{m3}r_{o3} + 1}$$

... (6.7.9)

Considering the fact $g_{m3} r_{o3} \gg 1$ and $r_{o3} = r_{o4}$ we have,

$$A_{cm} \approx \frac{-1}{2R_{SS}} \cdot \frac{1}{g_{m3}} = \frac{-1}{2R_{SS}g_{m3}}$$

... (6.7.10)

Since R_{SS} is very large; common-mode gain is very small.

Common-Mode Rejection Ratio (CMRR)

$$CMRR = \frac{|A_d|}{|A_{cm}|} = [g_m (r_{o2} \parallel r_{o4})] [2R_{SS} g_{m3}]$$

... (6.7.11)

When $r_{o2} = r_{o4} = r_o$ and $g_m = g_{m3}$ we have

$$CMRR = \frac{|A_d|}{|A_{cm}|} = (g_m r_o) (R_{SS} g_m)$$

... (6.7.12)

Review Questions