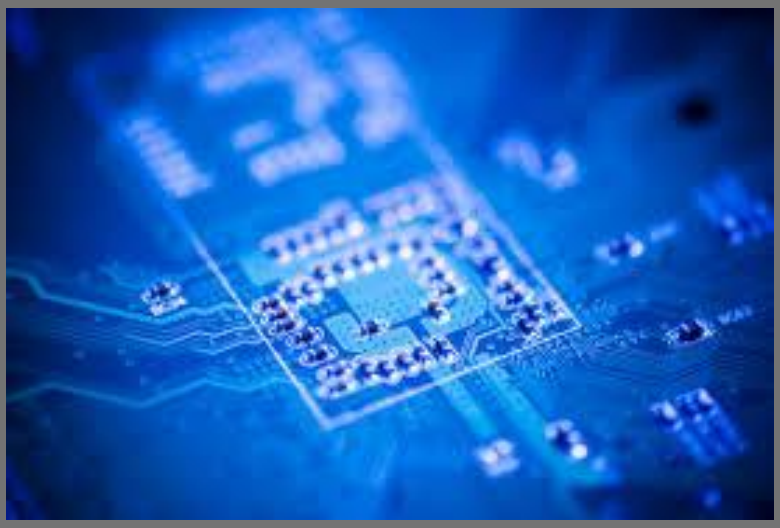
1151EC301

Analog Integrated Circuits Lab Manual



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Analog Integrated Circuit Lab Manual

DESIGN AND ANALYSIS OF VOLTAGE DIVIDER BIAS

Aim: To design and analyze the voltage divider bias.

EQUIPMENT AND COMPONENTS REQUIRED:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107 , Function Generator (0-3MHz),Resistor _____,Capacitor _____Breadboard, Connecting wires.

THEORY:

Biasing is to fix the Q – point in the middle of the active region we go for Biasing. The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.

When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable. The following are the factors that affect the stability of the operating point,

a. Transistor current gain factor - Change of hfe/β due to replacement of transistors.

b. Thermal variations - I_{CO}, V_{BE}, βdc

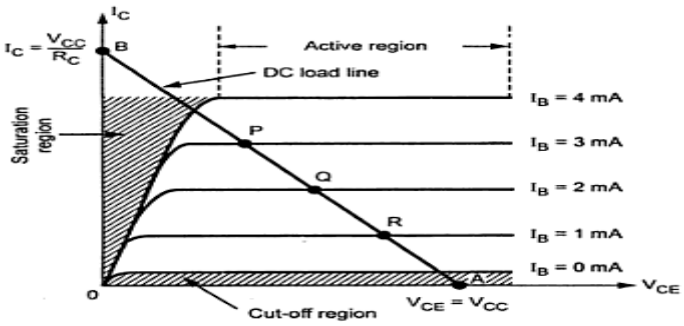

Fig 1.1 : Operating point fixed at the center of active region

In the circuit diagram

1. R1 , R2 – Potential divider
2. If Ic increases , I_E also increases it reduces the voltage drop across base and emitter (V_{BE})
3. Due to reduction in V_{BE} , base current and collector current get reduced.
4. Negative feedback exists in the emitter bias circuit.

DESIGN:

Given specifications:

V_{CC}=_____, I_C=_____, A_V= _____, f_I = _____,h_{FE}= _____,, β=_____,

The feedback factor, β= - 1/R_F= _____,

(i) To calculate RC:

The voltage gain is given by,

A_V= -hfe (R_C|| R_F) / hie

h ie = β re

re = 26mV / I_E = 26mV / 1.2mA = 21.6

hie = _____, x 21.6 =_____,

Apply KVL to output loop,

V_{CC}= I_C R_C + V_{CE}+ I_E R_E ----- (1)

Where V_E = I_E R_E (I_C= I_E)

V_E= V_{CC} / 10=_____,

Therefore R_E= V_E /I_E = _____

V_{CE}= V_{CC}/2= _____

From equation (1), RC= _____ KΩ

(ii) To calculate R_1&R_2:

R_B= R $_1R_2$ / R_1+ R_2------- (2)

V_B= V_{BE} + V_E = 0.7+ _____= _____

V_B= V_{CC} R_2 / R_1+ R_2 ------- (3)

Solving equation (2) & (3),

R_1= _____KΩ & R_2= _____KΩ

(iii) To calculate Resistance:

Output resistance is given by,

$R_O = R_C \,||\, R_F$

R_O= 1.3KΩ

input impedance is given by,

$R_i = (R_B || R_F) \,||\, hie$ = _____KΩ

Trans-resistance is given by,

R_m= -hfe (R_B|| R_F)(R_C || R_F) / (R_B|| R_F)+ hie

R_m= 0.06KΩ

AC parameter with feedback network:

(i) Input Impedance:

$R_{if} = R_i / D$ (where D= 1+β Rm)

Therefore D = _____

R_{if}= _____

Input coupling capacitor is given by,

Xci= R_{if} / 10= _____ (since X_{Ci} << R_{if})

Ci = 1/ 2πfX_{Ci} =66μf

(ii) Output impedance:

R_{Of}= R_O/ D = _____

Output coupling capacitor:

X_{CO}= Rof /10= 5.2

C_O = 1/ 2πfX_{CO}= _____

(iii) Emitter capacitor:

X_{CE} << R'$_E$ = R'/10

$R'_E = R_E || \{(hie + R_B) / (1+hfe)\}$

X_{CE}= _____

Therefore C_E= _____

EXPERIMENT PROCEDURE:

- Connections are made as per circuit diagram.
- Keep the input voltage constant at 20mV peak-peak and 1 kHz frequency. For different values of load resistance, note down the output voltage and calculate the gain by using the expression
  - $A_v = 20\log(V_0 / V_i)$ dB
- Add the emitter bypass capacitor and repeat STEP 2.And observe the effect of Feedback on the gain of the amplifier
- For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
- 5. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression

  $A_v = 20 \log(V_0 / V_i)$ dB
- A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph sheet
- The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.
- Where f_1 is lower cut off frequency of CE amplifier
  - f_2 is upper cut off frequency of CE amplifier
- The gain-bandwidth product of the amplifier is calculated by using the expression
  - Gain-Bandwidth Product = 3-dB mid band gain X Bandwidth.

CIRCUIT DIAGRAM:

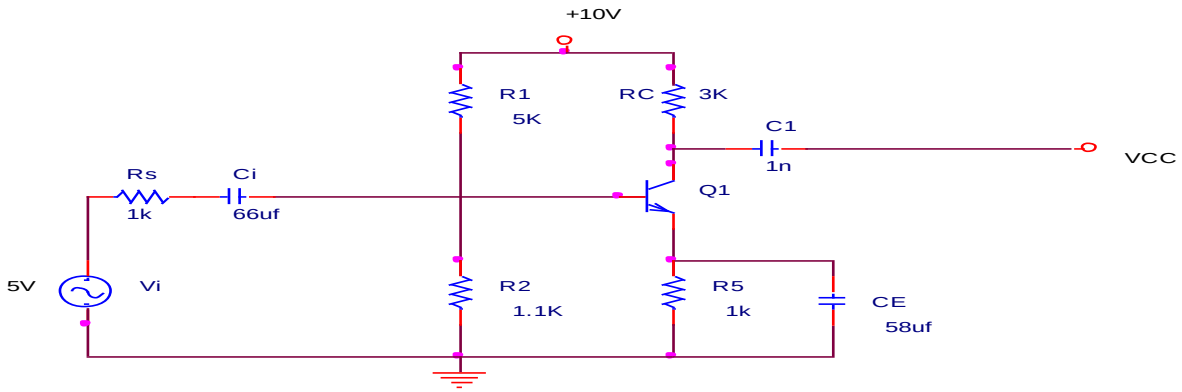

Fig 1.2:Voltage divider Bias Circuit

WORKSHEET

Frquency Response: V_i = ------V

S.NO	Frequency (Hz)	Output Voltage (V_o)	Gain A = V_o/V_i	Gain in dB $20\log(V_o/V_i)$

MODEL WAVEFORMS:

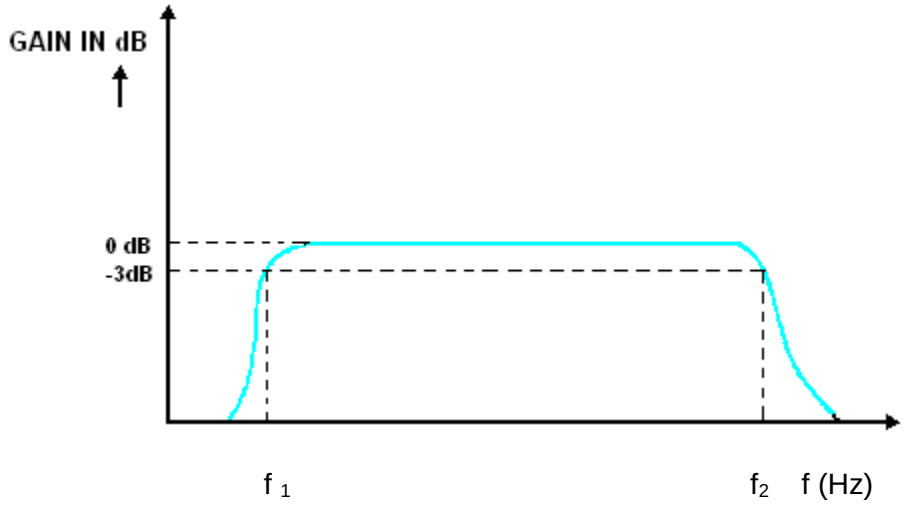

Fig1.3: Frequency response of Self Biasing

V-I characteristics of Voltage divider bias:

CONCLUSION:

……

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Viva Questions:

1. Compare the bandwidth of feedback amplifier.
2. Give the stability of gain with feedback.
3. Which sampling and mixing network is used in Voltage shunt feed back amplifier,
4. Calculate the input impedance for with feed back.
5. What type of feedback is used in amplifier?
6. Does VC increase or decrease if R1 is increased?
7. Does IC increase or decrease if β(hFE) is reduced?
8. What happens to VCE if the transistor is replaced one with larger β (hFE)?
9. What happens to VCE if the transistor EB junction fails by becoming open?
10. If the transistor collector junction becomes open, what will happen to VE?

Practical Applications of Self bias

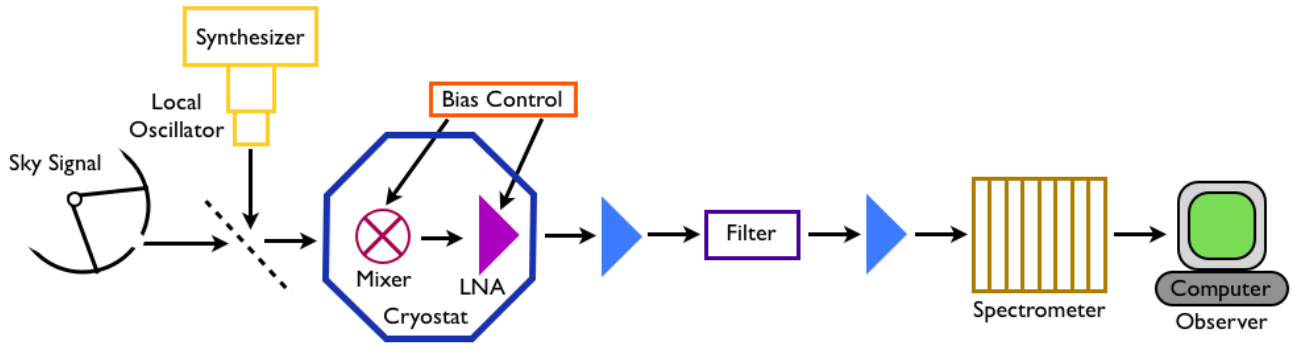


Fig : A block diagram of a heterodyne receiver. The sky signal is mixed with a local oscillator signal generated in the lab. In astronomy, we often use superconducting mixers for their extremely high sensitivity. The intermediate frequency is amplified using a low-noise amplifier (LNA) and then filtered and amplified as needed to match the power desired by the spectrometer

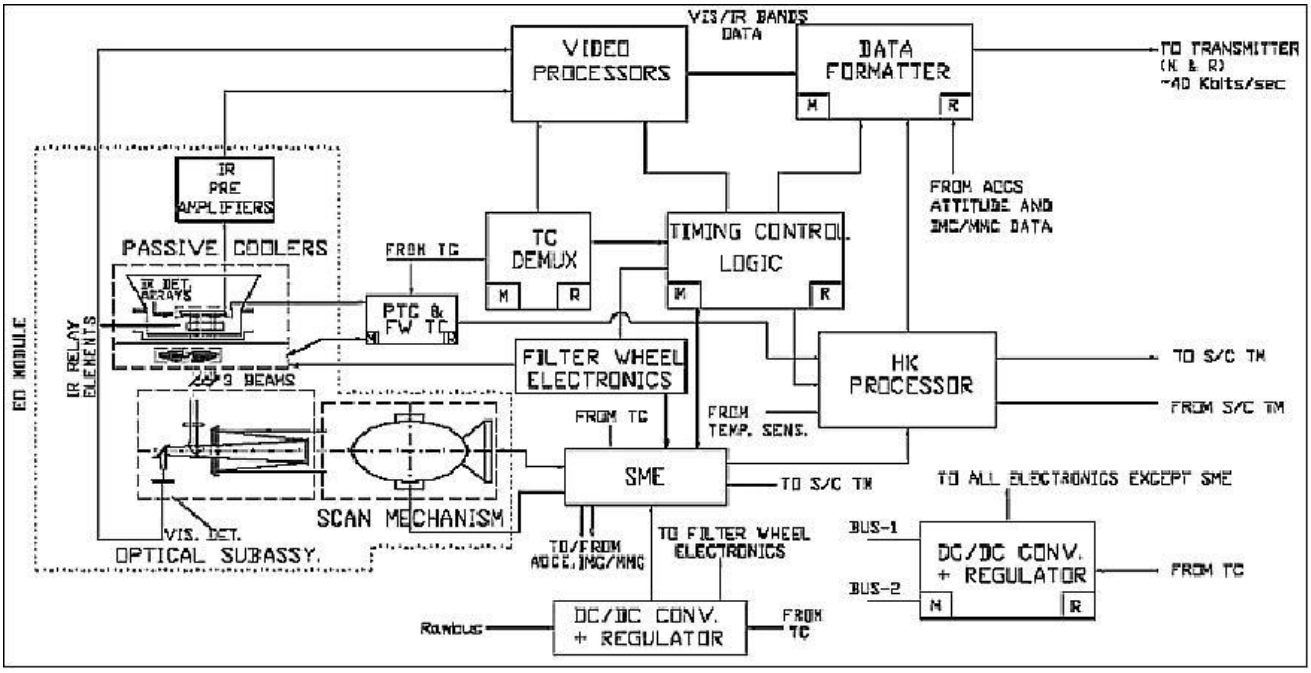


Fig : INSAT 3D

Experiment No: …….

Date: ……. /……. /……

DESIGN AND ANALYSIS OF RC PHASE SHIFT OSCILLATOR

***Aim**: To design and analyze the RC Phase Shift Oscillator.*

EQUIPMENT AND COMPONENTS REQUIRED:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107 , Resistor s--------Ω, Capacitor --------, Breadboard, Connecting wires, CRO Connecting Probes.

THEORY:

The RC phase shift oscillators basically consist of an amplifier and feedback network. The feedback network consists of resistors and capacitors arranged in cascade to produce oscillations. For a circuit to act as an oscillator certain criteria's need to be satisfied. This criterion is called Barkhausen Criteria. According to this criteria an amplifier stage will act as an oscillator.

1) The signal feedback from the output to the input is in same phase with the actual input.

2) The factor Aβ =1, where A is the amplifier gain and β is the feedback factor

The resistors R1 and R2 form the voltage divider network. Rc is used for providing collector bias and it act as the load the Re resistor provide thermal stabilization. The capacitor Ce is called the bypass capacitor as it is used to bypass frequency components produced at the emitter terminal to the ground. This capacitor have a great role in gain stability because if frequency components were allowed to pass through Re resistor then the drop in Re increases and this could result in negative feed backing and can reduce the gain of the amplifier.

When the Vcc is provided any circuit imbalance could produce small base current and this will be amplified at the collector terminal with 180^0 phase shift. The collector terminal is connected with 3 phase shift networks (RC) which produce approximately 60^0 phase shift each and to their combined effect produces another 180 degree phase shift. The last resistor R is connected to the base of the amplifier. This act as the feedback path so the signal feedback from the phase shift stage is now (360^0 phase different or) in phase with the input hence the Barkhausen Criterion 1 is satisfied. The phase feedback network is

designed to make the product Aβ=1 and hence both the criteria's were satisfied and the circuit act as an oscillator.From the derivations the frequency of an RC oscillator can be obtained as f =1/(2∏RC√ (6+4Rc/R)) and the h_{FE} of the transistor required is given by hFE >= 23+29(Rc/R)+4(R/Rc) from this equation the minimum h_{FE} required is 29.

DESIGN:

Output requirement:
Sine wave with ------Vpp and frequency ------Hz

Selection of BJT : Select transistor BC 107 as its minimum h_{fe} is 100

Design of Rc and Re : Let the Vcc is chosen to be 20% more than the required output swing therefore Vcc=12v . Let this voltage be divided as follows 40% across Rc, 50% across BJT and 10% across Re therefore VRc=-------V ,VRe=-------V, VCE=-------V , Ic =2mA(collector current from datasheet)

Rc=VRc/Ic=-------

Re=VRe/Ie=VRe/Ic=-------

Design of R1 and R2: Let the current through R1 be 10 Ib and current through R2 be 9 Ib this assumption is made in order to prevent loading of the voltage divider by the base current
Ib=Ic/hfe=-------
V_{R2}=VBE+VRe=.-------
V_{R1}=Vcc-VR2=-------
R1=V_{R1}/10Ib=-------
R2=V_{R2}/9Ib=-------

Design of Ce: Ce is the bypass capacitor let the lowest frequency that it bypass should be 100Hz
The impedance of the capacitor X_{Ce}<=Re/10 (standard rule) The resonant frequency of any RC network is given by

f=1/(2πRC)
Here R=Re/10=-------,F=100Hz so from this C=Ce>=1/(2πfRe) =1/(2π*100*-------)=-------

Design of Phase shift network:

Since our required frequency of oscillation is -------Hz the phase shift network should provide 180 degree phase shift to this frequency.

From the frequency equation of the phase shift network f=1/(2∏RC√ (6+4Rc/R)) where F=-------Hz , Take R =4.7K to limit collector current from this equation C can be found out

$C=1/(2\pi Rf\sqrt{(6+4Rc/R)})=1/(2\pi 4.7K*500Hz\sqrt{(6+4*2.2K/4.7K)})$ $=0.024\mu F$ use $0.022\mu F$ standard

EXPERIMENT PROCEDURE:

- Connect the circuit as per the circuit diagram.
- Measure the frequency of oscillation (f_o) and the amplitude of the output voltage.
- Measure and draw the waveforms
- Observe the effect of variation of the potentiometer on the frequency of oscillation.
- Observe the effect of the variation of R_E and R_B on f_o.

CIRCUIT DIAGRAM :

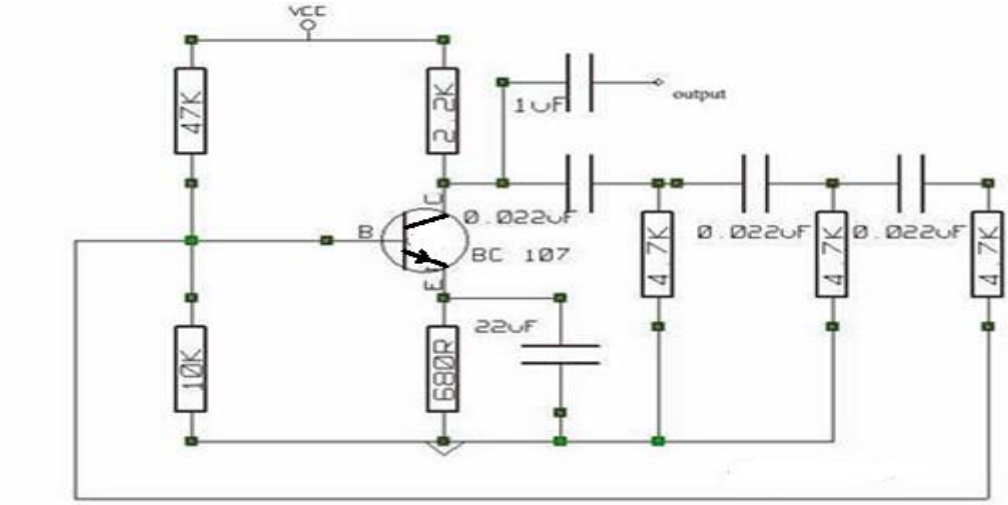


Fig 2.1: Circuit diagram of RC Phase Shift Oscillator

MODEL GRAPH:

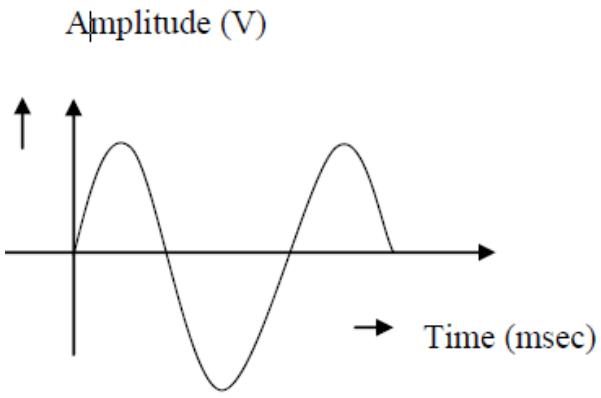


Fig 2.2: Output Wave for RC Phase Shift Oscillator

WORKSHEET

Amplitude (V)	Time (m sec)

V-I characteristics of RC phase shift oscillator:

Conclusion:

RC phase shift oscillator designed and output waveform is plotted.

Frequency of oscillation: -------

……

Viva Questions:

1. What are the general oscillation conditions in feedback amplifiers?
2. Drive an expression for the frequency of oscillation in both phase shift and Wein bridge oscillators.
3. Compare between phase shift and Wein Bridge oscillators.
4. What is Oscillator?
5. Discuss the effect of changing R_B and R_E on fo.
6. Say the Barkhausion Criteria
7. What is the frequency range of RC Oscillators ?
8. Draw the Circuit of Twin T oscillator.
9. List out the Advantages and Disadvantages of RC Oscillators
10. Write down the general applications of oscillators

Practical Applications of RC phase shift oscillator

RC phase shift oscillators are used for musical instruments, oscillators, voice synthesis, and GPS units. They work at all audio frequencies.

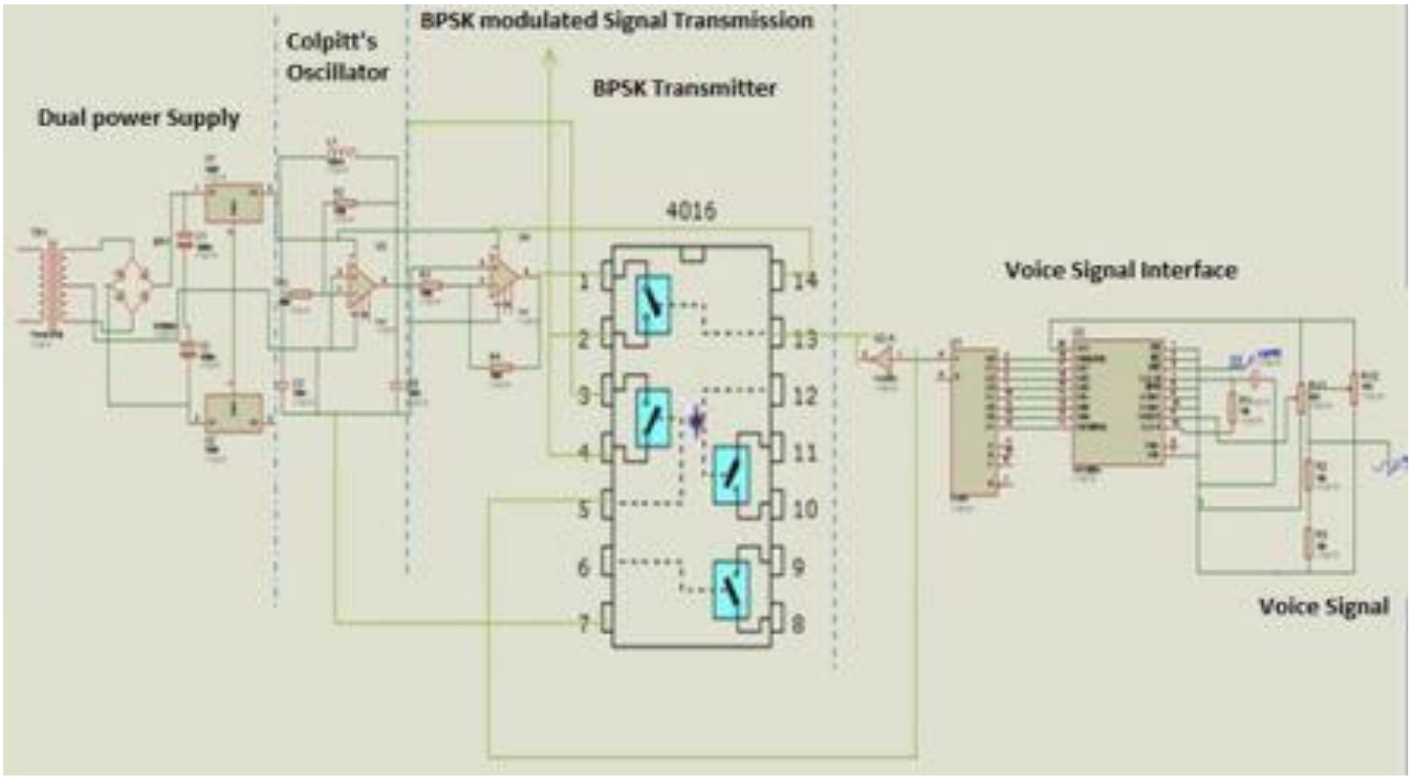


Fig 2.3: Arrangement of Binary Phase Shift Keying (BPSK) Transmitter Using Voice signal interfacing

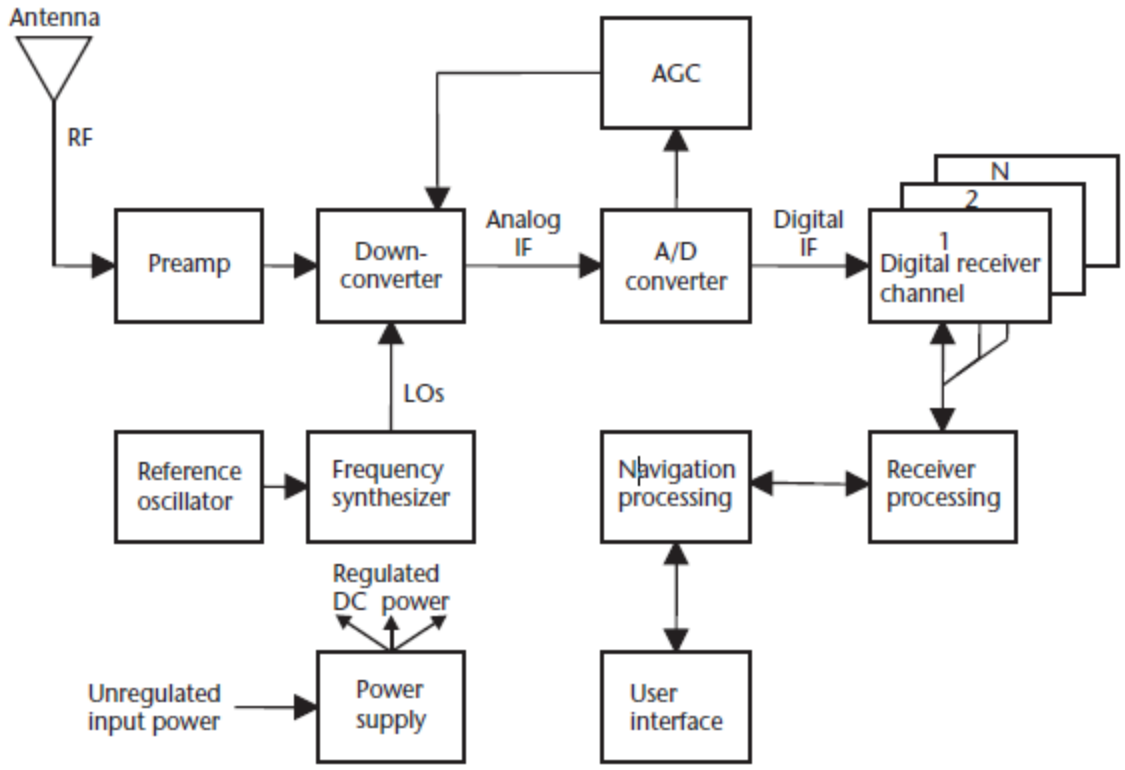


Fig 2.4: General digital GPS receiver block diagram.

DESIGN AND *ANALYSIS* OF HARTLEY OSCILLATOR

***Aim**: To construct Hartley oscillator using a transistor, to find out the frequency of Oscillation and comparing it to that of theoretical frequency.*

EQUIPMENT AND COMPONENTS REQUIRED:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107, Resistor s-------- , Capacitor --------, Breadboard, Connecting wires, CRO Probes.

THEORY:

The Hartley oscillator is an electronic oscillator circuit in which the oscillation frequency is determined by a tuned circuit consisting of capacitors and inductors, that is, an LC oscillator. Hartley oscillator is a one type of sine wave generator. Hartley Oscillator have two major parts namely – amplifier part and feedback part. The amplifier part has a typically CE amplifier with voltage divider bias. In the feedback path, there is a LCL network. The feedback network generally provides a fraction of output as feedback. It is a high frequency generator.

When the collector supply voltage Vcc is switched on, collector current starts rising and charges the capacitor C. When this capacitor is fully charged, it discharges through coils L1 and L2, setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltage across L1 which *is* applied to the base emitter junction of the transistor and appears in the amplified form in the collector circuit. Feedback of energy from output (collector emitter circuit) to input (base-emitter circuit is) accomplished through auto transformer action. The output of the amplifier is applied across the inductor L1, and the voltage across L2 forms the feedback voltage. The coil L1, is inductively coupled to coil L2, and the combination acts as an auto-transformer. This energy supplied to the tank circuit overcomes the losses occurring in it. Consequently the oscillations are sustained in the circuit. The energy supplied to the tank circuit is in phase with the generated oscillations. The phase difference between the voltages across L1 and that across L2 is always 180°because the centre of the two is grounded. A further phase of 180° is introduced between the input and output voltages by the transistor itself. Thus the total phase shift becomes 3600 (or zero), thereby making the feedback positive or regenerative which is essential for oscillations.

DESIGN: ***:***

Output requirement:
Sine wave with -----Vpp and frequency -----Hz

Selection of BJT : Select transistor BC 107 as its minimum h_{fe} is 100

Design of feed back Network:

Given L_1= L_2=--------mH, f=----KHz, V_{CC}=12V, I_C=3mA, S=12

$$f = 1/2\prod\sqrt{(L1+L2)C}$$

C= -----

Amplifier design:

(i) Selection of R_C:

Gain formula is,

A_V= - h_{fe} R_{Leff} / h_{ie}

Assume V_{CE}=V_{CC}/2 (Transistor active)

V_{CE}= ------

V_E=$I_E R_E$= V_{CC}/10=1.2V

V_{CC}=$I_C R_C$ + V_{CE} + $I_E R_E$

R_C= (V_{CC}- V_{CE} -$I_E R_E$) / I_C

Therefore R_C = ------

(ii) Selection of R_E:

I_C= I_E=------Ma

R_E= V_E/I_E

R_E= ------

(iii) Selection of R_1 & R_2:

Stability factor S=12

S=1+ (R_B/ R_E)

R_B=------

Using potential divider rule,

$R_B=R_1R_2 / R_1+R_2$ & $V_B= (R2/ R_1+R_2) V_{CC}$

$R_B /R_1= R_2/ R_1+R_2$

Therefore $R_B/R_1= V_B/V_{CC}$

$V_B=V_{BE}+ V_E$= ------

$R_1= (V_{CC}/ V_B)R_B$

R_1= ----------

$V_B/V_{CC} =R_2 / R_1+R_2$

R_2=---------

(iv)Output capacitance (C_O):

$X_{CO}=R_C/10$=----------

$1/2\prod fC_O$=----------

C_O=----------

(v) Input capacitance (C_i):

$X_{Cin}= R_B/10$=----------

$1/2\prod fC_{in}=1.1x10^3$

C_{in}= ----------

(vi) By pass Capacitance (C_E):

$X_{CE}=R_E/10$=----------

$1/2\prod fC_E=100$

C_E =----------

EXPERIMENT PROCEDURE:

- Connect the circuit as per the circuit diagram.
- Set V_{CC} = 12V.

- For the given supply the amplitude and time period is measured from CRO.
- Frequency of oscillation is calculated by the formula f=1/T
- Verify it with theoretical frequency, f= $1/2\prod$ ($\sqrt{(L1+L2)C}$) Amplitude Vs time graph is drawn.

CIRCUIT DIAGRAM :

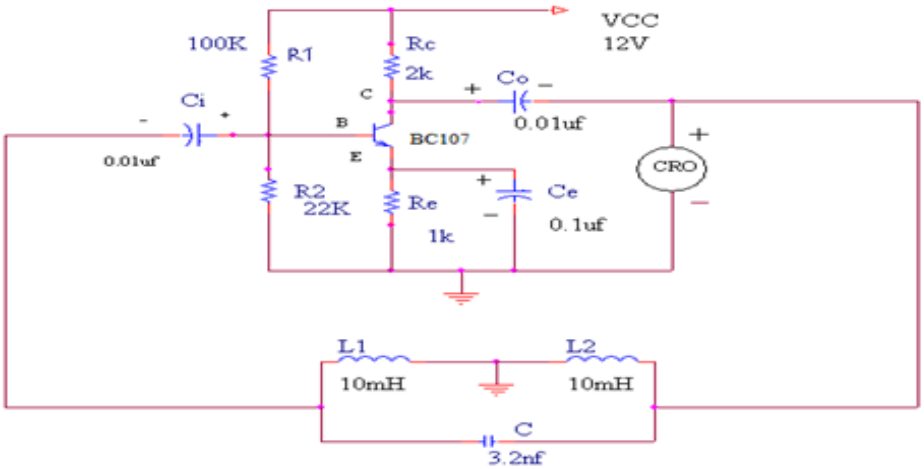
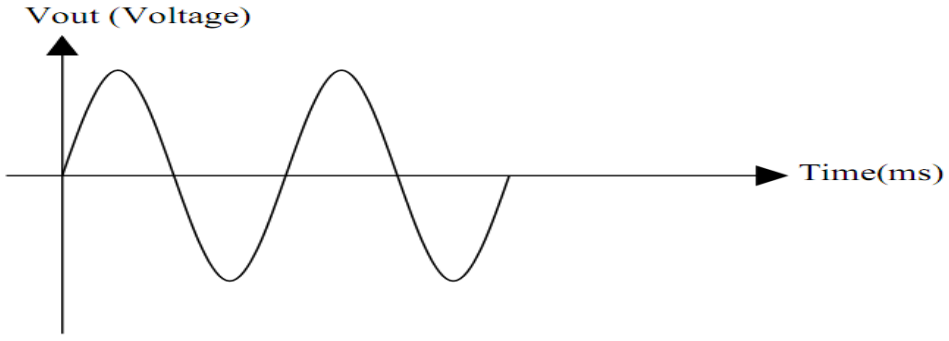


Fig 2.5 Hartley Oscillator-Circuit digram

WORKSHEET

Amplitude (V)	Time(µs)	Frequency (Hz)

MODEL GRAPH:



V-I characteristics of RC phase shift oscillator:

Conclusion:

Thus the Hartley oscillator is designed and constructed for the given frequency.

Theoretical frequency:

Practical frequency **:**

……

Viva Questions:

1. How does an oscillator differ from an amplifier?
2. What is the approximate value of h_{fe} in a Hartley oscillator using BJT?
3. Mention the expression for frequency of oscillation?
4. Mention the reasons why LC oscillator is preferred over RC oscillator at radio frequency?
5. How the Hartley oscillator satisfy the barkhausen criterion
6. Is Hartley oscillator is better than Colpitts oscillator

Practical Applications of LC phase shift oscillator

Sinusoidal oscillators have a wide range of applications including usage in radios, televisions, communication systems, computers, industrial controlled applications, and laboratories. They work as a function or signal generator. Hartley oscillators are mainly used in radio receivers

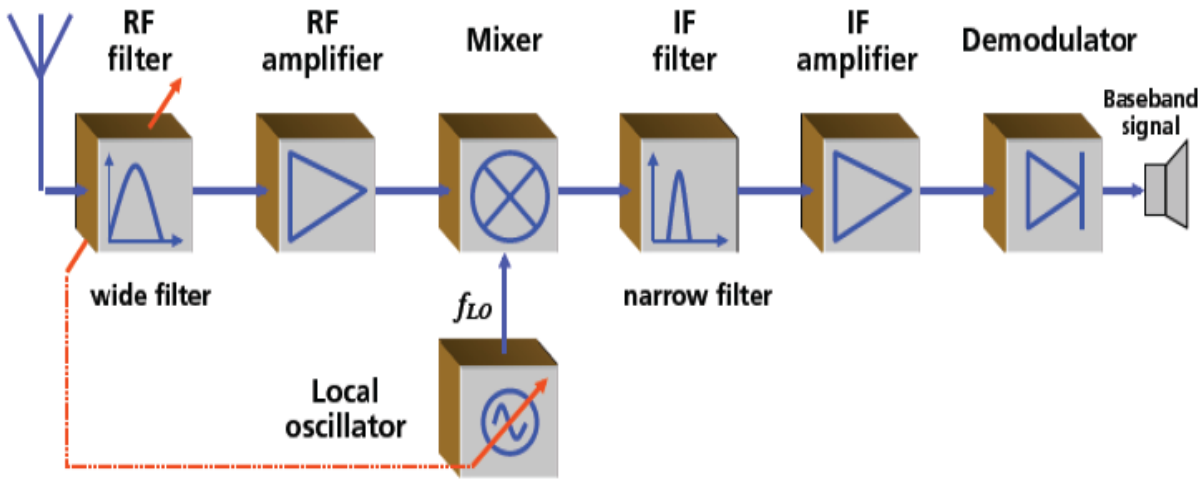


Figure The superheterodyne receiver

Fig 2.6:The superhetrodyne reciver

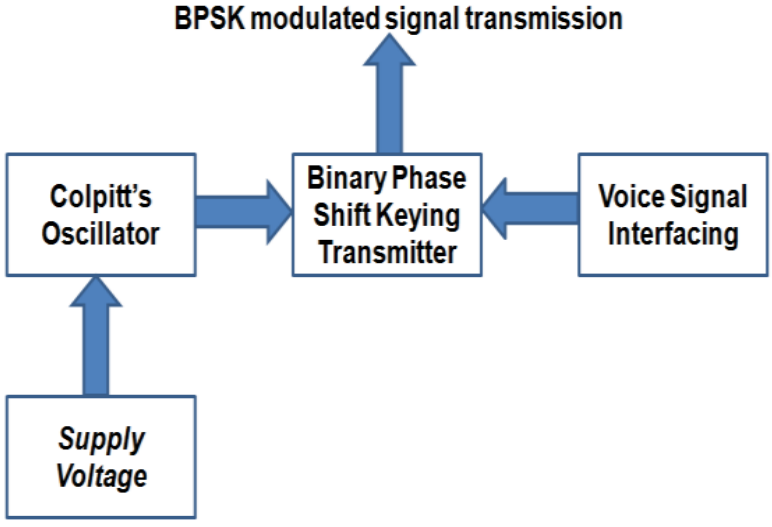


Fig2.7. Block diagram of BPSK transmitter

MONOSTABLE MULTIVIBRATOR

***Aim**: To design an monostable multivibrator using transistor*

EQUIPMENT AND COMPONENTS REQUIRED:
Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107, Resistors , Capacitors , Breadboard, Connecting wires,Probes

THEORY:
A monostable multivibrator often called a one-shot multivibrator is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand-by state the output of the circuit is approximately zero or at logic low level. When an external trigger pulse is applied, the output is forced to go high (approx. V_{cc}). The time during which the output remains high is given by,

$$t_p = 1.1\ R_1\ C$$

At the end of the timing interval, the output automatically reverts back to its logic low state. The output stays low until a trigger pulse is applied again. Then the cycle repeats.
Thus the monostable state has only one stable state hence the name monostable

EXPERIMENT PROCEDURE:

1. Get the required components
2. Give the connections as per circuit diagram. DEFINCENCY
3. A negative trigger pulse of 5V, 2 KHz is applied
4. Check the output using CRO
5. Measure the width and time period of the wave

CIRCUIT DIAGRAM :

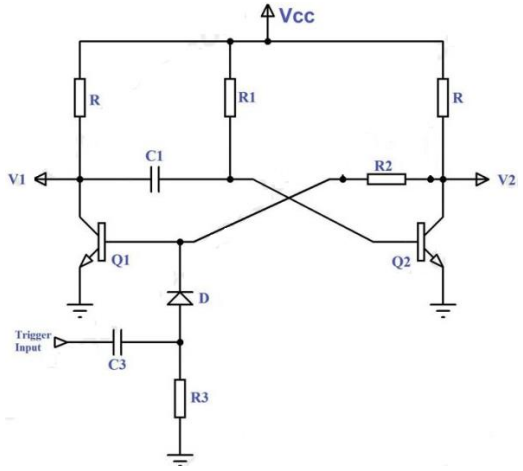


Fig 3.1: Monostable Multivibrator Circuit

WORKING:

- When the circuit is switched ON, transistor Q1 will be OFF and Q2 will be ON.
- Capacitor C1 gets charged during this state.
- When a positive trigger is applied to the base of transistor Q1 it turns ON, which turns OFF the transistor Q2 due the the negative voltage from the capacitor C1.
- Capacitor C1 starts discharging during this state.
- Transistor Q1 remains in ON state due the positive voltage from the collector of transistor Q2 which is in OFF state.
- Transistor Q2 remains in OFF state until the capacitor C1 discharges compleatly.
- When the capacitor C1 discharged completly, transistor Q2 turns ON, which turns transistor Q1 OFF.

DESIGN:

Given f= ------ KHz,

R – Collector Resistor:

Rc should be calculated depending upon the collector current requirement.

$$\mathbf{Rc = (Vcc – Vce (sat)) / Ic}$$

R1 – Base Resistor:

R1 should be chosen such that it will provide enough collector current during saturation to the transistor Q2.

- Min. base current required, Ib_{min} = Ic / β, where β is the hFE of the transistor
- Safe base current, Ib = 3 Ib_{min} = 3Ic / β

$$\mathbf{R1 = (Vcc – Vbe) / Ib}$$

R2 – Base Resistor Q1:

R2 should be chosen such that it should provide enough saturation collector current to the transistor Q1.

$$\mathbf{R2 = ((Vcc – Vbe) / Ib) – R}$$

T – Pulse Time Period:

$$\mathbf{T = 0.693R1C1}$$

From this we can find the value of capacitor C.

C3 Capacitor:

Assume R3=1KΩ

R3C3 << 0.0016T

MODEL GRAPH:

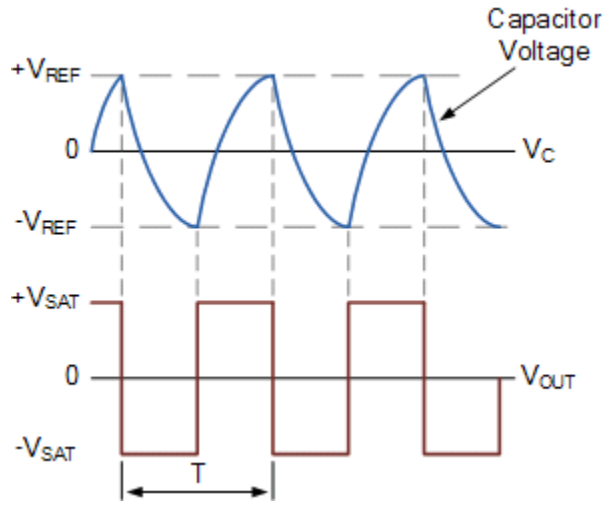


Fig 3.2: Output of Monostable Multivibrator

TABULAR COLUMN:

S.no	Observation	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)	
			t_{on}	t_{off}
1	Trigger input			
2	Output Voltage , V_o			

Conclusion:

ASTABLE MULTIVIBRATOR

***Aim**: To design an astable multivibrator using transistor*

EQUIPMENT AND COMPONENTS REQUIRED:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107, Resistors , Capacitors , Breadboard, Connecting wires,Probes.

THEORY:

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. This circuit does not require an external trigger to change the state of the output. The time during which the output is either high or low is determined by two resistors and a capacitor, which are connected externally to the 555 timer. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by,

$$t_c = 0.69 (R_1 + R_2) C$$

Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by,

$$t_d = 0.69 (R_2) C$$

Thus the total time period of the output waveform is,

$$T = t_c + t_d = 0.69 (R_1 + 2 R_2) C$$

The term duty cycle is often used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed in percentage. In equation form,

$$\% \text{ duty cycle} = [(R_1 + R_2) / (R_1 + 2 R_2)] \times 100$$

EXPERIMENT PROCEDURE:

1. Get the required components
2. Give the connections as per circuit diagram
3. Check the out put using CRO
4. Measure the width and time period of the wave

DESIGN:

Given f= 4 KHz,

Therefore, Total time period, T = 1/f = _____

We know, duty cycle = t_c/ T

$$D = \frac{\text{Ton}}{\text{Ton} + \text{Toff}}$$

Therefore, t_c = ----------

and t_d = _____ We also know for an astable multivibrator

$t_d = 0.69 (R_2) C$

Therefore, R_2 = _____

$t_c = 0.69 (R_1 + R_2) C$

Therefore, R_1 = _____

CIRCUIT DIAGRAM :

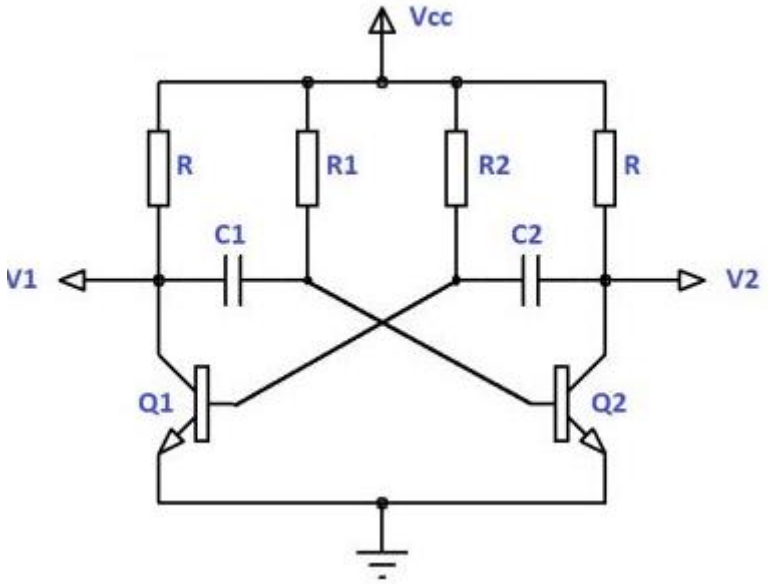


Fig 3.3: Astable Multivibrator

MODEL GRAPH:

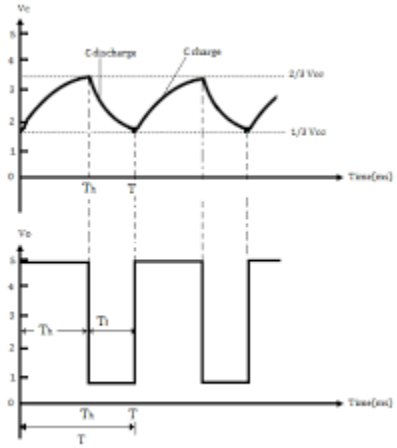


Fig 3.3: Astable Multivibrator output wave form

TABULAR COLUMN:

S.no	Waveforms	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)	
			t_c	t_d
1	Output Voltage , V_o			

Conclusion:

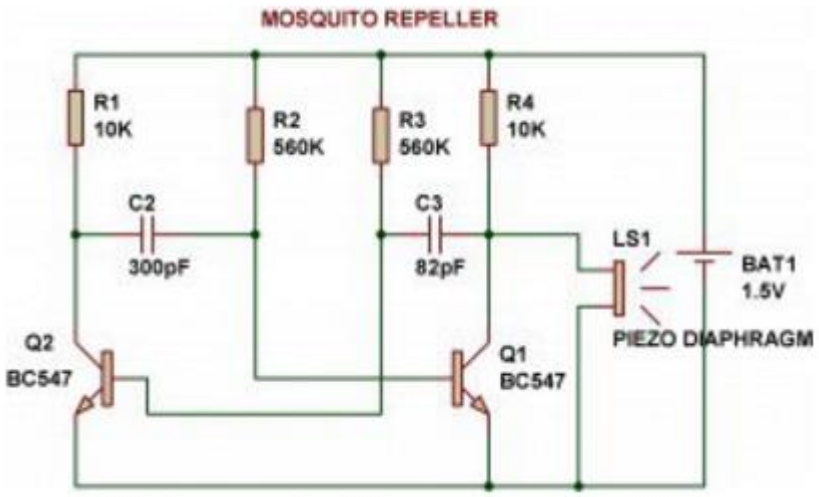
Viva Voce Questions:

What is a multivibrator ?

1. What is the purpose of multivibrator ?
2. What is an astable multivibrator called so ?
3. Why is an monostable multivibrator called so ?
4. What is an astable multivibrator ?
5. What is a monostable multivibrator ?
6. What is the purpose of monostable multivibrator ?
7. Give some examples of multivibrator.
8. Mention the applications of multivibrator.
9. What is the principle of monostable multivibrator ?
10. How does a monostable multivibrator work in terms of the astable multivibrator?
11. What is the disadvantage of an astable multivibrator ?
12. What are the different types of multivibrator circuits?

Application of Multivibrator : Mosquito repeller

When Q1 is conducting, Q2 is off and when Q2 is conducting, Q1 is off. The capacitors C2 and C3 contribute decisively to this ON/OFF cycles for the transistors Q1 and Q2. Another important factor in the operation of the circuit is the fact that the transistor goes into conduction only when the base-emitter voltage exceeds 0.7V(for silicon transistors).From the basic knowledge we can visualize how the transistors exchange their roles and the how the voltage on the collector of each transistor jumps between the upper and lower level, producing a rectangular waveform. If we take a close look at the circuit, we will see that C2 and C3 are not equal. They differ in the values by a factor of four.The output signal will thus be a nonsymmetrical waveform. Such a non- symmetrical signal contains more high frequency harmonics compared to normal square wave signal. The output of our circuit will have the basic frequency of 5Khz along with the harmonics of 10,15 and 20Khz. If some insects are deaf to frequencies upto 5Khz, they may react to 10Khz or 15Khz or even 20Khz.



BJT Differential Amplifier

***Aim**: To Study and Construct a differential amplifier using BJT and determine its CMRR.*

EQUIPMENT AND COMPONENTS REQUIRED:

DC Power supply (0-30V), Resistors, BJT, Breadboard, Connecting wires,CRO,Probes

THEORY:

The differential amplifier, or differential pair, is an essential building block in all integrated amplifiers. In general, the input stage of any analog integrated circuit with more than one input consists of a differential pair or differential amplifier. The basic differential pair circuit consists of two-matched transistors Q1andQ2 , whose emitters are joined together and biased a constant current source.Three important characteristics of the differential input stage are: the common-mode rejection ratio CMRR, the input differential resistance Rid , and the differential-mode gain Ad .

WORKING PRINCIPLE:

When input signal V_{s1} is applied to the transistor Q_1, there will be a high voltage drop across the collector resistance R_{C1} , and thus the collector of Q_1 will be less positive. When V_{s1} is negative Q_1 is turned OFF, and the voltage drop across R_{C1} becomes very low and thus the collector of Q_1 will be more positive. Thus we can conclude than an inserted output appears at Q_1 collector for applying signal at V_{s1}. When Q_1 is turned ON by the positive value of V_{s1}, the current through the emitter resistance R_E increases as the emitter current is almost equal to the collector current ($I_E I_C$). Thus the voltage drop across R_E increases and makes the emitter of both transistors going in a positive direction. Making Q_2's emitter positive is the same as making the base of Q_2 negative. In such a condition the transistor Q_2 will conduct less current which in turn will cause less voltage drop in R_{C2} and thus the collector of Q_2 will go in a positive direction for positive input signal. Thus we can conclude that the non-inverting output appears at the collector of transistor Q_2 for input at base of Q_1.The amplification can be driven differentially by taking output between the collector of Q_1 and Q_2

EXPERIMENT PROCEDURE:

1. Connections are given as per the circuit diagram.

2. Set the input Voltages V1 = 50mV & V2 =40mV.

3. Note down the Output Voltage

4. Vary the input Voltages and note down the output voltages.

CIRCUIT DIAGRAM:

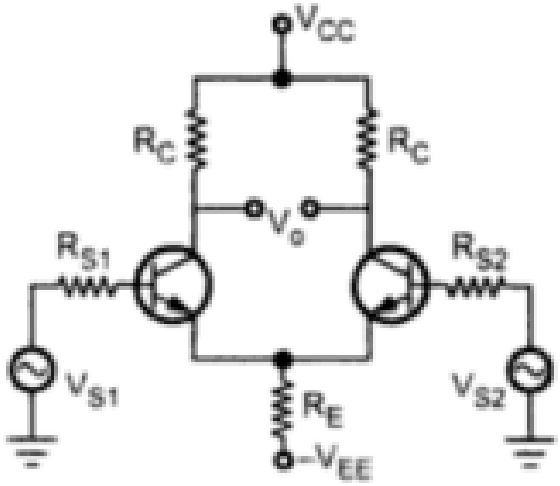


Fig4.1: BJT Differential Amplifier

DESIGN:

Assume R_c=4.7KΩ, R_{s1}=R_{s2}=100Ω, R_E=6.8KΩ, h_{ie}=2.8KΩ, h_{fe}=100
Differential Gain:

$$A_d = \frac{h_{fe} R_C}{R_S + h_{ie}}$$

Common Mode Gain:

$$A_c = \frac{h_{fe} R_C}{2 R_E (1 + h_{fe}) + R_S + h_{ie}}$$

CMRR:

$$\text{CMRR} = \frac{A_d}{A_c}$$

CMRR in db= 20 log CMRR

Output Voltage:

$$V_o = A_d V_d + A_c V_c$$
$$V_d = V_{S1} - V_{S2}$$
$$V_c = \frac{V_{S1} + V_{S2}}{2}$$

WORKSHEET :

SL NO	VI(V)	V2(V)	VO(V)

Conclusion:

VIVA QUESTIONS

1. What is Differential amplifier?
2. Define CMRR.
3. What are the ideal characteristics for Differential amplifier?
4. How the emitter resistance R_E affects the CMRR?
5. What are the advantages of differential amplifier using FET than differential amplifier using BJT?
6. What are the applications of differential amplifier?

WORKING OF CLASS C TUNED AMPLIFIER

***Aim**: To design and find the frequency response of class c single tuned amplifier.*

EQUIPMENT AND COMPONENTS REQUIRED:

DC Power supply (0-30V), Voltmeter (0-30V), Ammeter (μA & mA range), Transistor BC107, Resistors, Capacitors, Inductor, Breadboard, Connecting wires

THEORY:

Class C power amplifier is a type of amplifier where the active element (transistor) conduct for less than one half cycle of the input signal. Less than one half cycle means the conduction angle is less than 180° and its typical value is 80° to 120°. The reduced conduction angle improves the efficiency to a great extend but causes a lot of distortion. Theoretical maximum efficiency of a Class C amplifier is around 90%.
Due to the huge amounts of distortion, the Class C configurations are not used in audio applications. The most common application of the Class C amplifier is the RF (radio frequency) circuits like RF oscillator, RF amplifier etc where there are additional tuned circuits for retrieving the original input signal from the pulsed output of the Class C amplifier and so the distortion caused by the amplifier has little effect on the final output. Input and output waveforms of a typical Class C power amplifier is shown in the figure below.

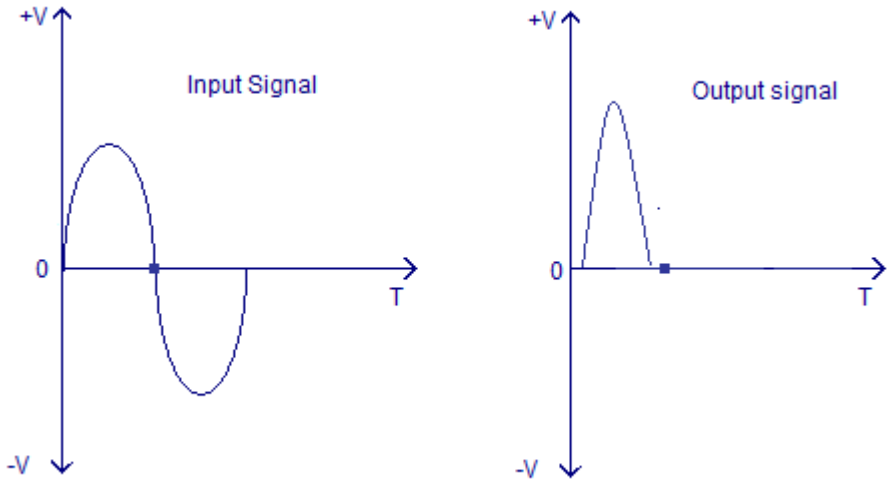


Fig 5.1: input and output wave forms of Class C Power Amplifier

From the above figure it is clear that more than half of the input signal is missing in the output and the output is in the form of some sort of a pulse.

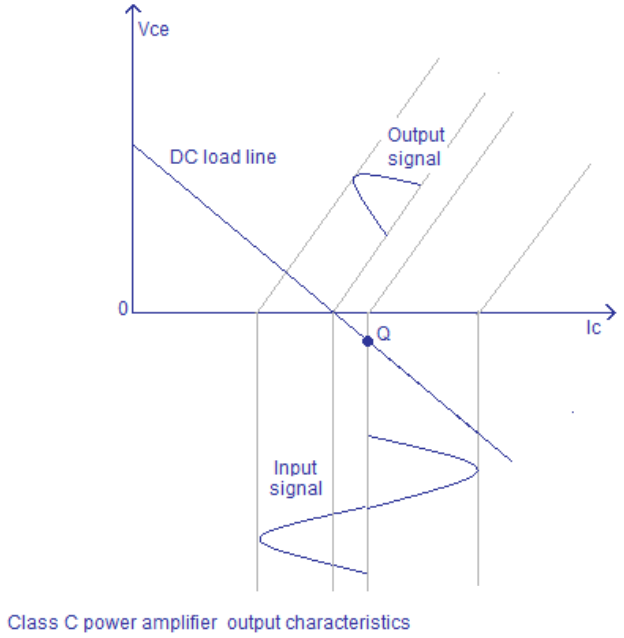


Fig5.2: Output characteristics of Class C power amplifier.

In the above figure you can see that the operating point is placed some way below the cut-off point in the DC load-line and so only a fraction of the input waveform is available at the output.

CIRCUIT DIAGRAM:

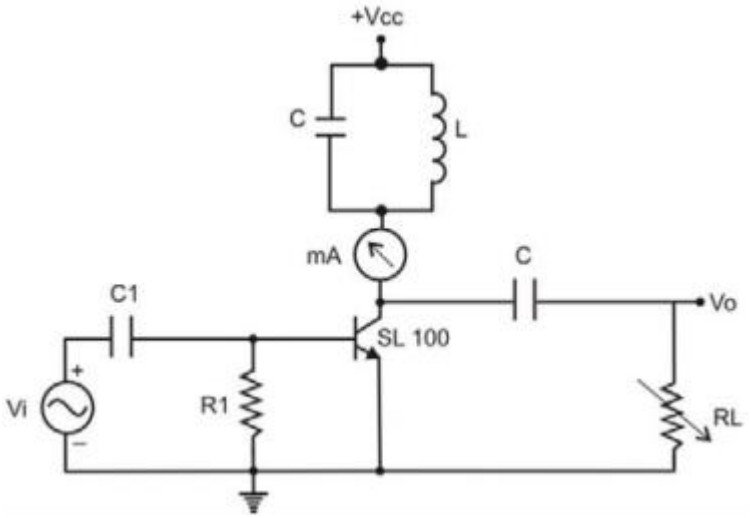


Fig5.3: Class C power amplifier.

Biasing resistor Rb pulls the base of Q1 further downwards and the Q-point will be set some way below the cut-off point in the DC load line. As a result the transistor will start

conducting only after the input signal amplitude has risen above the base emitter voltage (Vbe~0.7V) plus the downward bias voltage caused by Rb. That is the reason why the major portion of the input signal is absent in the output signal.

Inductor L1 and capacitor C1 forms a tank circuit which aids in the extraction of the required signal from the pulsed output of the transistor. Actual job of the active element (transistor) here is to produce a series of current pulses according to the input and make it flow through the resonant circuit. Values of L1 and C1 are so selected that the resonant circuit oscillates in the frequency of the input signal. Since the resonant circuit oscillates in one frequency (generally the carrier frequency) all other frequencies are attenuated and the required frequency can be squeezed out using a suitably tuned load. Harmonics or noise present in the output signal can be eliminated using additional filters. A coupling transformer can be used for transferring the power to the load.

Advantages of Class C power amplifier.

- High efficiency.
- Excellent in RF applications.
- Lowest physical size for a given power output.
-

Disadvantages of Class C power amplifier.

- Lowest linearity.
- Not suitable in audio applications.
- Creates a lot of RF interference.
- It is difficult to obtain ideal inductors and coupling transformers.
- Reduced dynamic range.

EXPERIMENT PROCEDURE:

- Connect the power supply, voltmeter, current meter with the diode as shown in the figure for forward bias diode. You can use two multimeter (one to measure current through diode and other to measure voltage across diode)
- Increase voltage from the power supply from 0V to 20V in step as shown in the observation table
- Measure voltage across diode and current through diode. Note down readings in the observation table. **BC107**
- Reverse DC power supply polarity for reverse bias
- Repeat the above procedure for the different values of supply voltage for reverse bias
- Draw VI characteristics for forward bias and reverse bias in one graph

DESIGN:

Frequency

$R_1C_1 >> t,$

i.e, $R_1C_1 = 100\ t$

$t = 6.66$ usec

Choose

$C_1 = 0.01\mu f,$

$R_1 = 68\ K\Omega$

Tank ckt:

If $C = 0.001\mu f,$

then $L = 1.125$ mH ~1mH.

$$f_r = 1/(2\pi\sqrt{LC})$$

$F_{actual} = 159$ KHz.

R1 = 68KΩ, C1 = 0.01μf, C= 0.001μf, L = 1mH

- CHECK POINTS :

1. Adjust input frequency exactly equal to tuned frequency.

WORKSHEET

Observation table:

S.No	Input frequency (Hz)	Input Voltage (mV)	Output Voltage (V)	**Voltage Gain** $V_{gain}=20\log\left(\frac{V_o}{V_i}\right)$ (db)
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				
12.				
13.				
14.				
15.				

MODEL GRAPH:

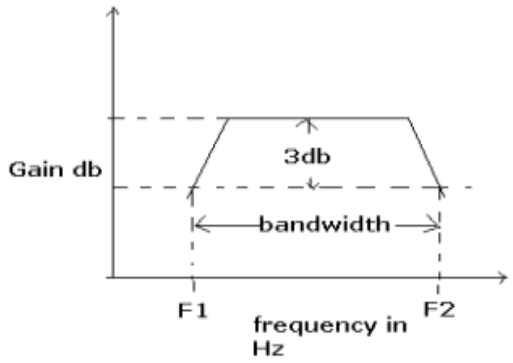


Fig5.4: frequency response of Class C power amplifier.

Conclusion:

……

Viva Questions:

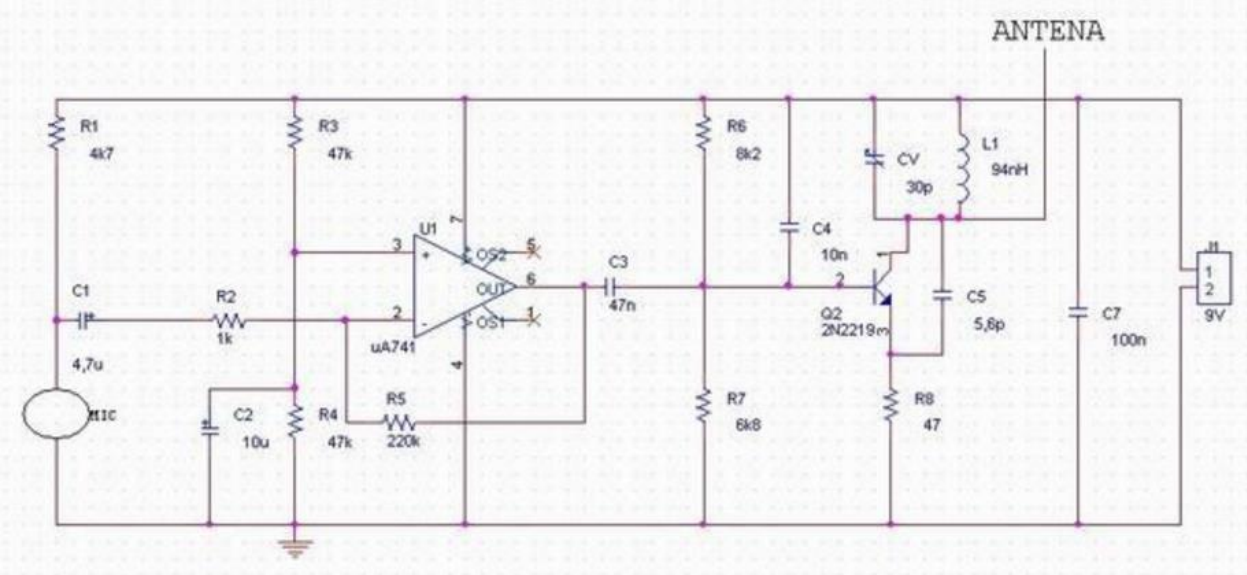
1. What is meant by tuned amplifiers?
2. Classify tuned amplifiers.
3. What are the advantages of double tuned amplifier?
4. What is the other name for tuned amplifier?

PRACTICAL APPLICATIONS OF CLASS C TUNED AMPLIFIER :

1KM FM TRANSMITTER CIRCUIT 741 OP AMP:

Fm transmitter circuit 741 op-amp integrated based on a simple, stable FM transmitter circuit 9-volt battery is working with the adapter, can be used but 9v battery to a cleaner source .. author 30cm tall telescopic antenna used instead of electronics store located in the radio antenna used L1 coil of a pen on the 1 mm wire windings to be wound round 2 of 4 .3 mm range will be all ranges must be the same ….

Our aim is the construction of an FM transmitter circuit for the range of commercial radio frequencies between 88 MHz and 108 MHz using class C tuned amplifier. This provides a high power transmitter mainly in open areas and with its huge sensitivity is able to capture the minimum sound, and could even be used to carry out espionage.



DESIGN OF INVERTING, NON-INVERTING AMPLIFIERS AND ADDERS USING OP-AMPs

***Aim**: To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

DC Power supply (0-30V), Voltmeter (0-30V), OP-amp IC741Resistors, Capacitors, Inductor, Breadboard, Connecting wires

THEORY:

The inverting amplifier is shown in the following Fig1.1. The input signal drives the invertinginput of the op-amp through resistor *R*1 . The op-amp has an open-loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 180o out-of-phase with the input signal. This means that the feed back signal opposes the input signal and the feedback is negative or degenerative.

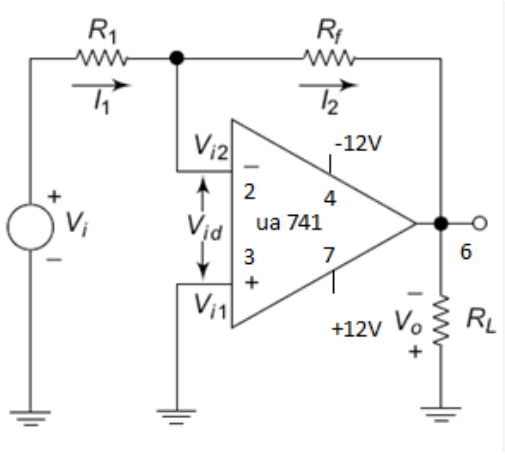


Fig 6.1: Basic Inverting Amplifier

PIN DIAGRAM:

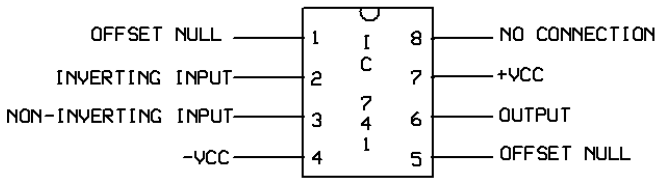


Fig 6.2: Pin diagram of IC 741

DESIGN:

We know for an inverting Amplifier
$A_{CL} = R_F / R_1$

Assume R_1 *(approx. 10 KΩ) and find* R_f

Hence $V_o = - A_{CL} V_i$.

- *Design the Inverting amplifier with different resistors:*
  1. R_1*=5 KΩ,*
  2. R_1*=2 KΩ and*
  3. R_1*=22 KΩ*

CIRCUIT DIAGRAM:

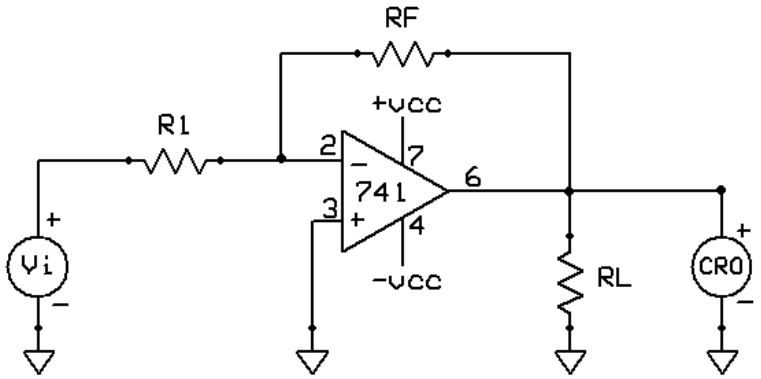
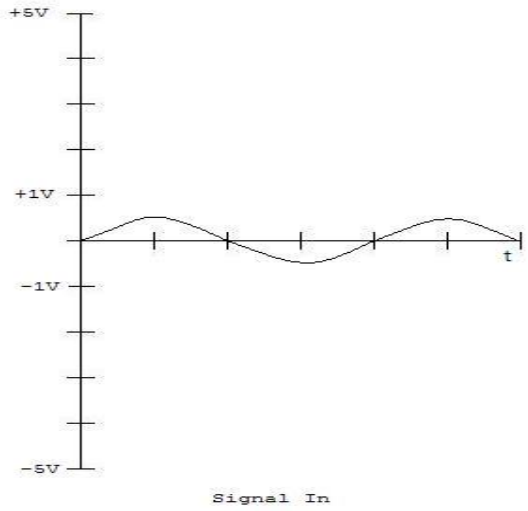


Fig 6.3:Inverting Amplifier Connection Diagram

EXPERIMENT PROCEDURE :

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

MODEL GRAPH:



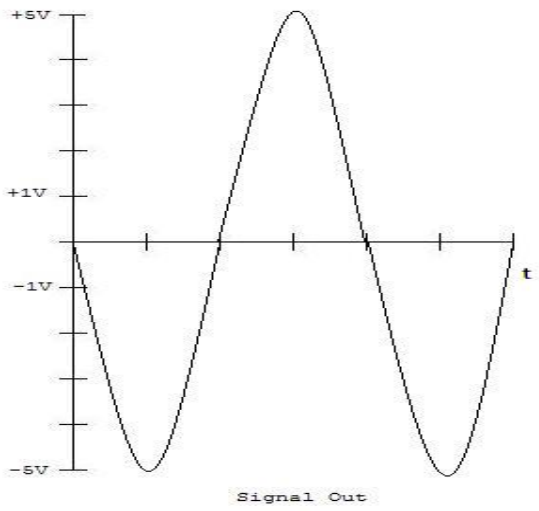


Fig 6.4(a) :Input wave form ***Fig 6.4(b): Output Wave forms***

WORKSHEET

Observation table:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

Conclusion:

……

***Aim**: To design an Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

DC Power supply (0-30V), Voltmeter (0-30V), OP-amp IC741Resistors, Capacitors, Inductor, Breadboard, Connecting wires.

THEORY:

A typical non-inverting amplifier with input resistor R1 and a feedback resistor Rf is shown in the following figure 1.5 . The input voltage is given to the positive terminal.

$V_o=(1+(R_f/R_1))V_{id}$

DESIGN:

We know for a Non-inverting Amplifier

$A_{CL} = 1 + (R_F / R_1)$

Assume R_1 (approx. 10 KΩ) and find R_f,

Hence $V_o = A_{CL} V_i$

- Design the Non Inverting amplifier with the specifications:
  1. R_1=5 KΩ,
  2. R_1=2 KΩ and
  3. R_1=22 KΩ

CIRCUIT DIAGRAM:

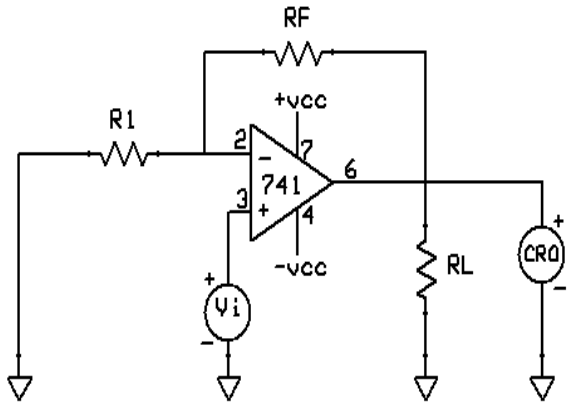
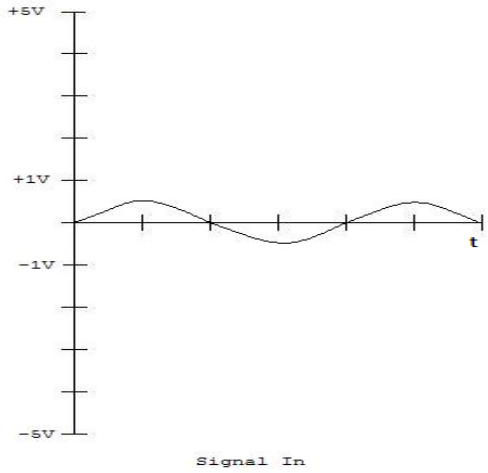


Fig 6.5:Non Inverting Amplifier Connection diagram

EXPERIMENT PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

MODEL GRAPH:



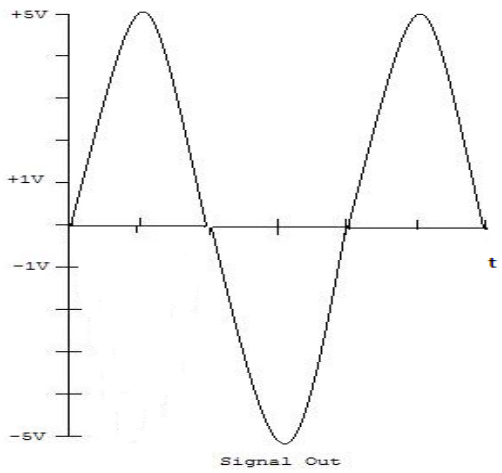


Fig 6.6(a): Input wave form ***Fig 6.6(b): Output wave form***

WORKSHEET

Observation table:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

Conclusion:

The design and testing of the non- inverting amplifier is done and the input and output waveforms were drawn.

……

***Aim**: To design an Adder for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

DC Power supply (0-30V), Voltmeter (0-30V), OP-amp IC741Resistors, Capacitors, Inductor, Breadboard, Connecting wires

THEORY:

The gain for each input to the adder depends upon the ratio of the feedback resistance of the circuit to the value of the resistor at that input. The adder is sometimes called a weighted adder because it provides a means of multiplying each of the inputs by a separate constant before adding them all together. It can be used to add any number of inputs and multiply each input by a different constant. This makes it useful in applications like audio mixers.

CIRCUIT DIAGRAM:

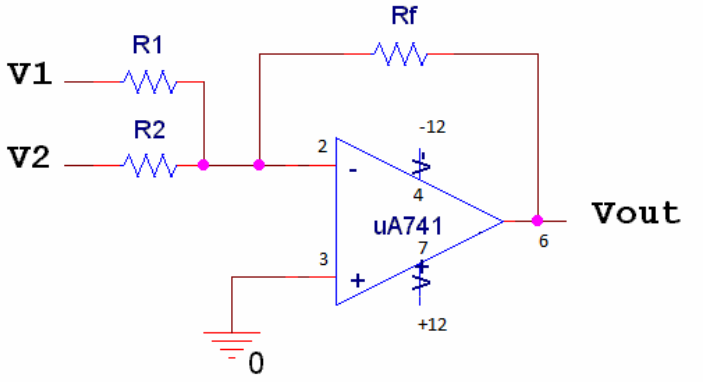


Fig 6.7: Circuit diagram for Adder

Its behavior is governed by the following equation:

$$V_{out} = -Rf\left(\frac{V1}{R1} + \frac{V2}{R2}\right).$$

EXPERIMENT PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

WORKSHEET

Observation table:

S.No	Input		Output	
			Practical	Theoretical
1.				
2.				
3.				
4.				
5.				

Input wave form ***Output wave form***

Conclusion:

The Adder circuit is constructed and their functions are verified.

……

PRACTICAL APPLICATIONS OF ADDER:

SUMMING AMPLIFIER APPLICATIONS :

If the input resistances of a summing amplifier are connected to potentiometers the individual input signals can be mixed together by varying amounts. For example, measuring temperature, you could add a negative offset voltage to make the display read "0" at the freezing point or produce an audio mixer for adding or mixing together individual waveforms (sounds) from different source channels (vocals, instruments, etc) before sending them combined to an audio amplifier.

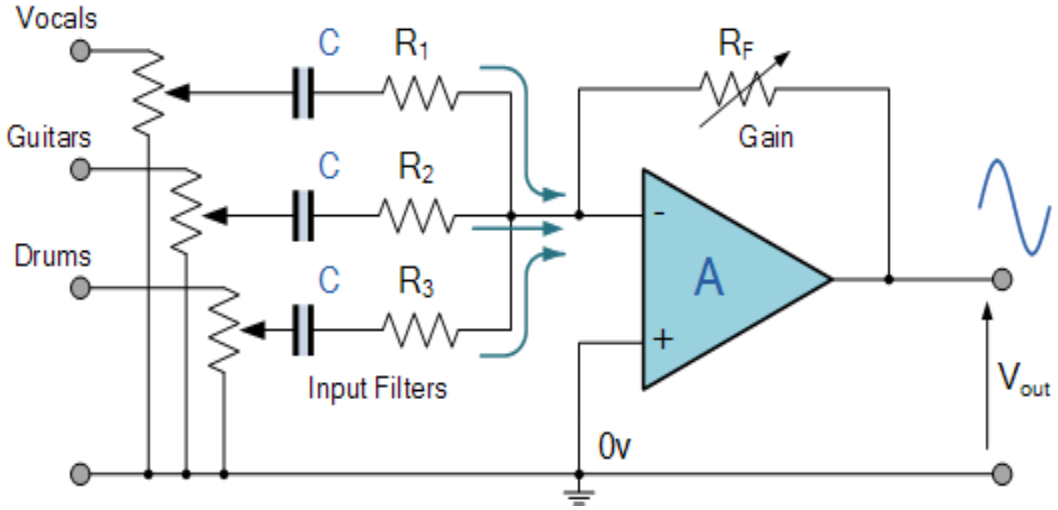


Fig 6.8 . Summing Amplifier Audio Mixer

Another useful application of a **Summing Amplifier** is as a weighted sum digital-to-analogue converter. If the input resistors, Rin of the summing amplifier double in value for each input, for example, 1kΩ, 2kΩ, 4kΩ, 8kΩ, 16kΩ, etc, then a digital logical voltage, either a logic level "0" or a logic level "1" on these inputs will produce an output which is the weighted sum of the digital inputs. Consider the circuit below.

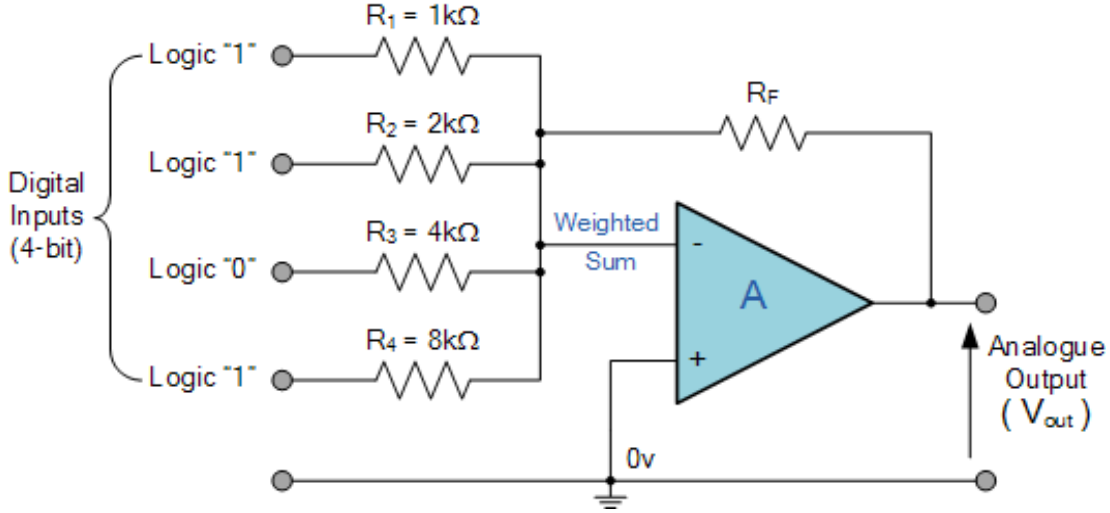


Fig 6.9 . Digital to Analog converter

Of course this is a simple example. In this DAC summing amplifier circuit, the number of individual bits that make up the input data word, and in this example 4-bits, will ultimately determine the output step voltage as a percentage of the full-scale analogue output voltage. Also, the accuracy of this full-scale analogue output depends on voltage levels of the input bits being consistently 0V for "0" and consistently 5V for "1" as well as the accuracy of the resistance values used for the input resistors, Rin. Fortunately to overcome these errors, commercial available Digital-to Analogue and Analogue-to Digital devices are available.

In the next tutorial about Operational Amplifiers, we will examine the effect of the output voltage, Voutwhen a signal voltage is connected to the inverting input and the non-inverting input at the same time to produce another common type of operational amplifier circuit called a Differential Amplifier which can be used to "subtract" the voltages present on its inputs

DESIGN OF DIFFERENTIATOR AND INTEGRATOR USING OPAMP

***Aim**: To design a Differentiator for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V),IC 741, Resistors, Capacitor, Breadboard, Connecting wires,probes.

Theory: Differentiator

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.

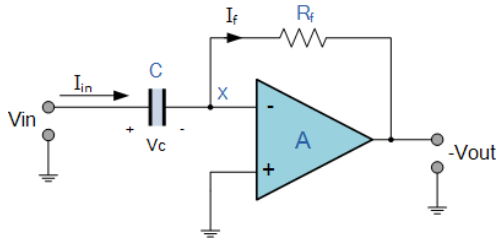


Fig: 7.1: Basic differentiator

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (Rf/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor Rf.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

Improved Op-amp Differentiator Amplifier:

The basic single resistor and single capacitor op-amp differentiator circuit is not widely used to reform the mathematical function of **Differentiation** because of the two inherent faults mentioned above, "Instability" and "Noise". So in order to reduce the overall closed-loop gain of the circuit at high frequencies, an extra resistor, Rin is added to the input as shown below circuit diagram.

Adding the input resistor Rin limits the differentiators increase in gain at a ratio ofRf/Rin. The circuit now acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies giving much better noise rejection. Additional attenuation of higher frequencies is accomplished by connecting a capacitorCf in parallel with the differentiator feedback resistor, Rf.

DESIGN:

- Design steps:

1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of C_{in}< 1 µF, calculate the value of R_f.
2. Choose f_b= 20 f_a and calculate the values of R_{in} and C_f so that $R_{in}C_1 = R_f C_f$.

EXPERIMENT PROCEDURE:

- Connections are given as per the circuit diagram.
- + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
- By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
- The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

CIRCUIT DIAGRAM OF DIFFERENTIATOR:

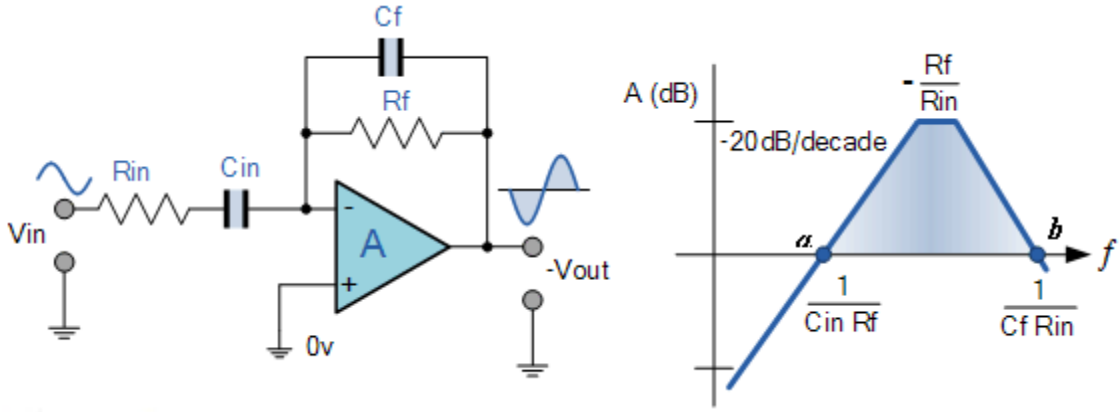


Fig: 7.2 Improved Op-amp Differentiator Amplifier and frequency responce

Model Graph: Differentiator Output:

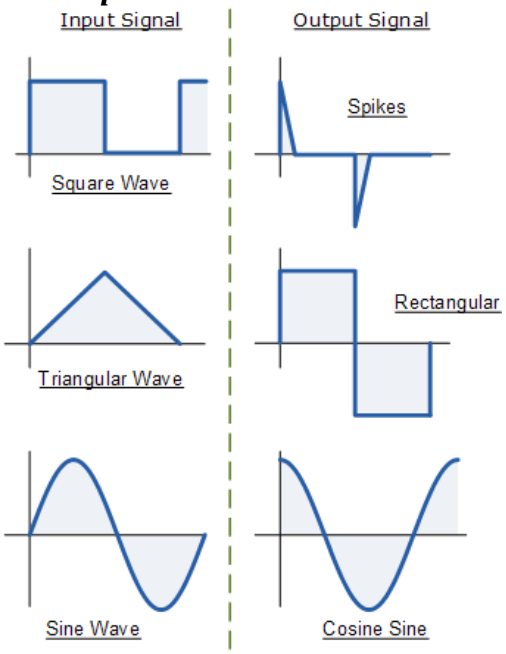


Fig:7.3 Input and output signals of Differentiator

WORKSHEET

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

Draw input and output of differentiator:

Conclusion:

……

Aim*: To verify integrator circuit for the given input specifications.(using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V),IC 741, Resistors, Capacitor, Breadboard, Connecting wires, probes.

THEORY: Integrator

As its name implies, the **Op-amp Integrator** is an operational amplifier circuit that performs the mathematical operation of **Integration** that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage*.

In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain

ratio of Xc/Rin is also very small giving an overall voltage gain of less than one, (voltage follower circuit).

As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, (τ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.

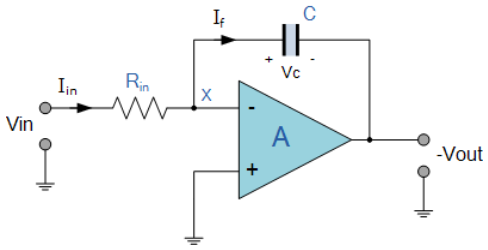


Fig:7.4 Basic Integrator

Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage, Vcdeveloped across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor (Xc/Rin) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed.

We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, Rin is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

The AC or Continuous Op-amp Integrator

If we changed the above square wave input signal to that of a sine wave of varying frequency the **Op-amp Integrator** performs less like an integrator and begins to behave more like an active "Low Pass Filter", passing low frequency signals while attenuating the high frequencies.

At 0Hz or DC, the capacitor acts like an open circuit blocking any feedback voltage resulting in very little negative feedback from the output back to the input of the amplifier. Then with just the feedback capacitor, C, the amplifier effectively is connected as a normal open-loop amplifier which has very high open-loop gain resulting in the output voltage saturating.

This circuit connects a high value resistance in parallel with a continuously charging and discharging capacitor. The addition of this feedback resistor, R_2 across the capacitor, Cgives the circuit the characteristics of an inverting amplifier with finite closed-loop gain of R_2/R_1. The result is at very low frequencies the circuit acts as an standard integrator, while at higher frequencies the capacitor shorts out the feedback resistor, R_2 due to the effects of capacitive reactance reducing the amplifiers gain.

Unlike the DC integrator amplifier above whose output voltage at any instant will be the integral of a waveform so that when the input is a square wave, the output waveform will be triangular. For an AC integrator, a sinusoidal input waveform will produce another sine wave as its output which will be 90^o out-of-phase with the input producing a cosine wave.

$$\text{D.C. Voltage Gain, } (Av_0) = -\frac{R_2}{R_1}$$

$$\text{A.C. Voltage Gain, } (Av) = -\frac{R_2}{R_1} \times \frac{1}{(1+2\pi f C R_2)}$$

$$\text{Corner Frequency, } (f_0) = \frac{1}{2\pi C R_2}$$

DESIGN:

- Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is,

$$T \geq R_f C_f$$

- *Example:* $R_1 C_f$ =1 second, and the input is a step (dc) voltage,2V. Determine the output voltage.
- Let the input function is constant beging at t=0 second ,0<=t<=4

Given Vin=2V

$V_0 = -\int 2\, dt$ (t=0 to 4)

=(2+2+2+2) =-8V

EXPERIMENT PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

CIRCUIT DIAGRAM OF INTEGRATOR:

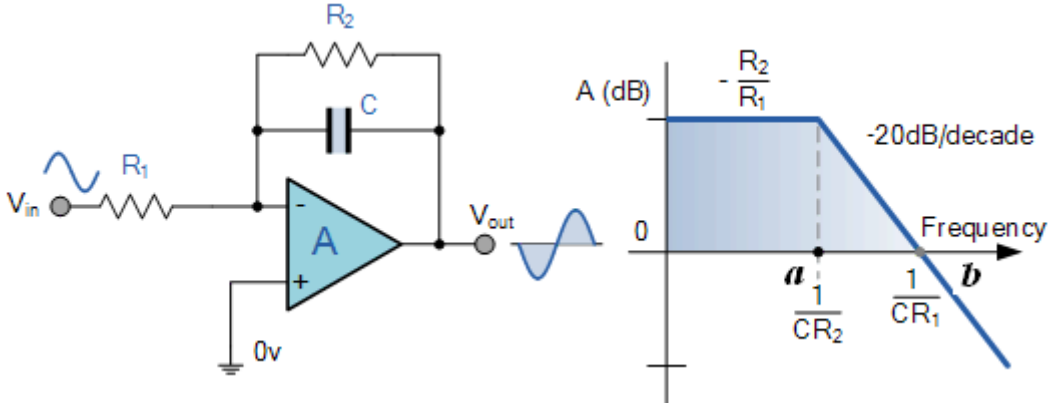


Fig: 7.5 AC or Continuous Op-amp Integrator and frequency response

MODEL GRAPH: Integrator output

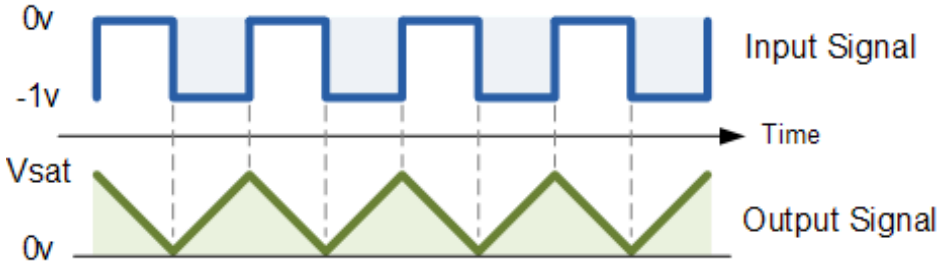


Fig: 7.6 input and output of integrator circuit

WORKSHEET

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

Draw input and output of integrator:

Conclusion:

……

Questions:

1. What is integrator?
2. Write the disadvantages of ideal integrator?
3. What is differentiator?
4. What will happen if R1 not present?
5. Write the application of differentiator?
6. Why compensation resistance is needed in differentiator.?
7. Why integrators are preferred over differentiators in analog comparators?

Application Activity: Function or signal generator

Function or signal generator is one of the most important component used in designing electronics circuits especially for practical or experimental applications. I think you are already aware of the importance of a function generator.

However, here we are going to discuss about Signal generators. A function generator is a signal source that has the capability of producing different types of waveforms as its output signal. The most common out of them are

- Sine waves
- Triangular waves
- Square waves
- Sawtooth waves

The frequencies of all these waveforms can be adjusted from a fraction of a hertz to megahertz range. Actually the function generators are very versatile instruments as they are capable of producing a wide variety of waveforms and frequencies. In fact each of these waveforms are suitable for specific applications.

All the function generators are capable of producing two different waveforms simultaneously from two different outputs. This may find helpful for certain application which requires more than one output waveforms at a time. For instance, by providing a square wave for linearity measurements in an audio system, a simultaneous sawtooth output may be used to drive the horizontal deflection amplifier of an oscilloscope, providing visual display of the measurement result.

Another important feature of some function generator is their capability of phase locking to an external signal source. One function generator may be used to phase lock a second function generator, and the two output signals can be displaced in phase by an adjustable amount. In addition, one function generator may be phase locked to a harmonic of the sine wave of another function generator. By adjusting the phase and amplitude of the harmonics almost any waveform may be produced by the summation of the fundamental frequency generated by one signal generator and the harmonic generated by the other. The signal generator can also be phase locked to an accurate frequency standard, and all its output waveforms will have the same frequency, stability, and accuracy as the standard.

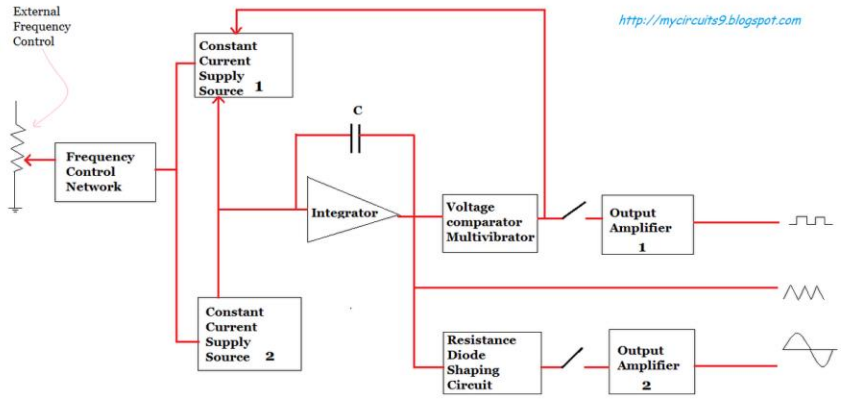


Fig:7.7: Block Diagram of Function Generator

Working of Signal generator

Here in this instrument the frequency is controlled by varying the magnitude of current that drives the integrator. It provides different types of waveforms at its output with a frequency range of 0.01 Hz to 100 kHz.

The frequency controlled voltage regulates two current supply sources. Current supply source one supplies constant current to the integrator whose output voltage rises linearly with time according to the output signal voltage. An increase or decrease in the current increase or reduce the slope of the output voltage and thus controls the frequency.

The voltage comparator multivibrator changes state at a predetermined maximum level, of the integrator output voltage. This change cuts off the current supply from source 1 and switches to supply source 2. The current supply 2 supplies a reverse current to the integrator so that its output drops linearly with time. When the output attains a predetermined level the voltage comparator again changes its state and switches on to the current supply source 1.

- The output of the integrator is a triangular wave whose frequency depends on the current supplied by the constant current supply sources.
- The comparator output provides a square wave of the same frequency as output.
- The resistance diode network changes the slope of the triangular wave as its amplitude changes and produces a sinusoidal wave with less than 1% distortion.

DESIGN OF ACTIVE LOW PASS AND HIGH PASS FILTER USING OPAMP

***Aim**: To design a Active Low pass and High pass filters for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V), IC 741, Resistors, Capacitor, Breadboard, Connecting wires.

THEORY: Active Low pass Filter

The most common and easily understood active filter is the **Active Low Pass Filter**. Its principle of operation and frequency response is exactly the same as those for the previously seen passive filter, the only difference this time is that it uses an op-amp for amplification and gain control. The simplest form of a low pass active filter is to connect an inverting or non-inverting amplifier.

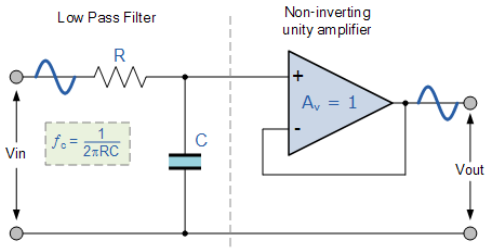


Fig:8.1 First order low pass filter

This first-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer) giving it a DC gain of one, Av = +1 or unity gain as opposed to the previous passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

While this configuration provides good stability to the filter, its main disadvantage is that it has no voltage gain above one. However, although the voltage gain is unity the power gain is very high as its output impedance is much lower than its input impedance. If a voltage gain greater than one is required we can use the following filter circuit.

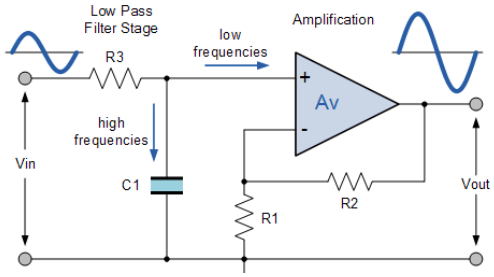


Fig: 8.2 Low pass Active filter with amplification

The frequency response of the circuit will be the same as that for the passive RC filter, except that the amplitude of the output is increased by the pass band gain, A_F of the amplifier. For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor (R_2) divided by its corresponding input resistor (R_1) value and is given as:

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

Therefore, the gain of an active low pass filter as a function of frequency will be:

Gain of a first-order low pass filter

$$Voltage\ Gain, (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{fc}\right)^2}}$$

Where:

A_F = the pass band gain of the filter, (1 + R2/R1)

f = the frequency of the input signal in Hertz, (Hz)

fc = the cut-off frequency in Hertz, (Hz)

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < fc$

$$\frac{Vout}{Vin} \cong A_F$$

2. At the cut-off frequency, $f = fc$

$$\frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$$

3. At very high frequencies, $f > fc$

$$\frac{Vout}{Vin} < A_F$$

Thus, the **Active Low Pass Filter** has a constant gain A_F from 0Hz to the high frequency cut-off point, f_C. At f_C the gain is $0.707A_F$, and after f_C it decreases at a constant rate as the frequency increases. That is, when the frequency is increased tenfold (one decade), the voltage gain is divided by 10.

In other words, the gain decreases 20dB (= 20log 10) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

Magnitude of Voltage Gain in (dB)

$$Av(dB) = 20\log_{10}\left(\frac{Vout}{Vin}\right)$$

$$\therefore -3dB = 20\log_{10}\left(0.707\,\frac{Vout}{Vin}\right)$$

DESIGN:

- Design steps:

1. Choose a value of high cutoff frequency f_H.

2. Select a value of *C* less than or equal to 1μF.

3. Caluclate the value of R using

$$R = \frac{1}{2\Pi fHC}$$

4.Finally select the value of R_i and R_F depending on the desired passband gain $A_F=1+(R_F/R_I)$

EXPERIMENT PROCEDURE:

1. The connections are made as shown in the circuit diagram.
2. The signal which has to be made sine is applied to the RC filter pair circuit with the non-inverting terminal.
3. The supply voltage is switched ON and the o/p voltages are recorded through CRO by varying different frequencies and tabulate the readings.
4. Calculating Gain through the formula and plotting the frequency response characteristics using Semi-log graph sheet and finding out the 3 dB line for f_c.

MODEL GRAPH: Frequency Response Curve

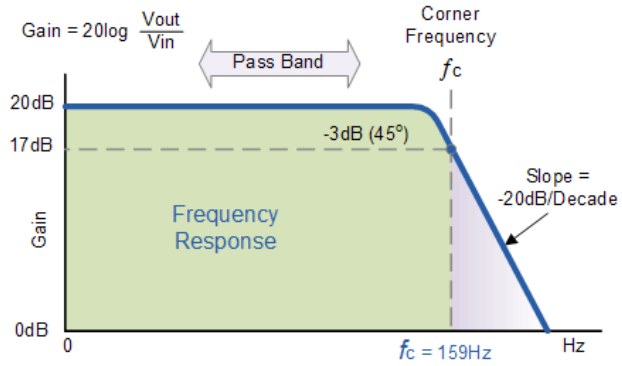


Fig 8.3 Low pass filter frequency response

THEORY: Active High pass Filter

A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuates low frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

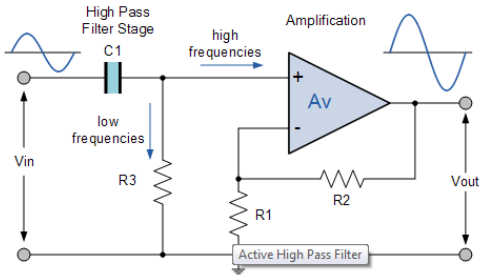


Fig 8.4 Active high pass filter with Amplification

This *first-order high pass filter*, consists simply of a passive filter followed by a non-inverting amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier.

For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor (R2) divided by its corresponding input resistor (R1) value and is given as:

Gain for an Active High Pass Filter

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

Where:

A_F = the Pass band Gain of the filter, (1 + R2/R1)

f = the Frequency of the Input Signal in Hertz, (Hz)

fc = the Cut-off Frequency in Hertz, (Hz)

Just like the low pass filter, the operation of a high pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < fc$

$$\frac{\text{Vout}}{\text{Vin}} < A_F$$

2. At the cut-off frequency, $f = fc$

$$\frac{\text{Vout}}{\text{Vin}} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$$

3. At very high frequencies, $f > fc$

$$\frac{\text{Vout}}{\text{Vin}} \cong A_F$$

Then, the **Active High Pass Filter** has a gain A_F that increases from 0Hz to the low frequency cut-off point, f_C at 20dB/decade as the frequency increases. At f_C the gain is$0.707A_F$, and after f_C all frequencies are pass band frequencies so the filter has a constant gain A_F with the highest frequency being determined by the closed loop bandwidth of the op-amp.

When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

Magnitude of Voltage Gain in (dB)

$$\text{Av(dB)} = 20\log_{10}\left(\frac{\text{Vout}}{\text{Vin}}\right)$$

$$\therefore\ -3\text{dB} = 20\log_{10}\left(0.707\,\frac{\text{Vout}}{\text{Vin}}\right)$$

For a first-order filter the frequency response curve of the filter increases by 20dB/decade or 6dB/octave up to the determined cut-off frequency point which is always at -3dB below the maximum gain value. As with the previous filter circuits, the lower cut-off or corner frequency (fc) can be found by using the same formula:

$$fc = \frac{1}{2\pi RC}\ Hz$$

The corresponding phase angle or phase shift of the output signal is the same as that given for the passive RC filter and **leads** that of the input signal. It is equal to **+45º** at the cut-off frequency fc value and is given as:

$$Phase\ Shift\ \ \phi = tan^{-1}\left(\frac{1}{2\pi fRC}\right)$$

A simple first-order active high pass filter can also be made using an inverting operational amplifier configuration as well, and an example of this circuit design is given along with its corresponding frequency response curve. A gain of 40dB has been assumed for the circuit.

MODEL GRAPH: Frequency response curve

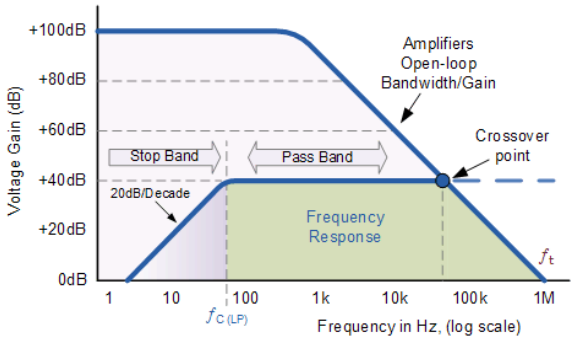


Fig 8.5 Frequency response of active high pass filter

WORKSHEET

V_{IN} = Volts

S.No.	FREQUNCY Hz	O/P voltage (V_O)Volts	Av=20 log Vo/Vi **dB**

Conclusion:

……

1. What is a low-pass filter ?
2. What has to be done in the circuit, if you want your filter to exactly follow the cut-off frequency?
3. Can a Band pass filter be constructed just by coupling a low pass filter and high pass filter, how?
4. Why do we draw a line at 3 dB below the peak gain to calculate the pass band of a filter?
5. What is difference between an ideal and a practical low pass filter ?
6. What does “roll-off” mean ?
7. What are passive filters ?
8. Why is butterworth filter used most often ?
9. What are band reject circuits?
10. Name the types of band rejection filters.

Application Activity: RFID System

RFID (radio frequency identification) is a technology that enables the tracking and/or identification of objects. Typically, an RFID system contains an *RFID tag* that consists of an IC chip that transmits data about the object, an *RFID reader* that receives transmitted data from the tag, and a *data-processing system* that processes and stores the data passed to it by the reader. A basic block diagram is shown in Figure.

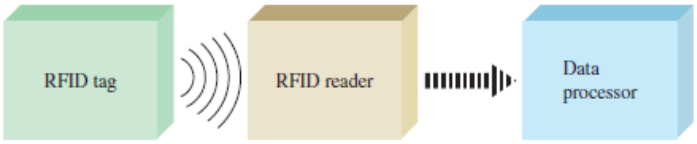


Fig.8.6 Basic block diagram of an RFID system.

The RFID Tag

RFID tags are tiny, very thin microchips with memory and a coil antenna. The tags listen for a radio signal sent by an RFID reader. When a tag receives a signal, it responds by transmitting its unique ID code and other data back to the reader.

Passive RFID Tag This type of tag does not require batteries. The tag is inactive until powered by the energy from the electromagnetic field of an RFID reader. Passive tags can be read from distances up to about 20 feet and are generally read-only; meaning the data they contain cannot be altered or written over.

Active RFID Tag This type of tag is powered by a battery and is capable of communicating up to 100 feet or more from the RFID reader. Generally, the active tag is larger and more expensive than a passive tag, but can hold more data about the product and is commonly used for identification of high-value assets. Active tags may be read-write, meaning the data they contain can be written over.

Tags are available in a variety of shapes. Depending on the application, they may be embedded in glass or epoxy, or they may be in label or card form. Another type of tag, often called the *smart label,* is a paper (or similar material) label with printing, but also with the RF circuitry and antenna embedded in it.

Some advantages of RFID tags compared to bar codes are

- Non-line-of-sight identification
- More information can be stored
- Coverage at greater distances
- Unattended operations are possible
- Ability to identify moving objects that have tags embedded
- Can be used in diverse environments

Disadvantages of RFID tags are that they are expensive compared to the bar code and they are bulkier because the electronics is embedded in the tag.

RFID tags and readers must be tuned to the same frequency to communicate. RFID systems use many different frequencies, but generally the most common are low frequency (125 kHz), high frequency (13.56 MHz), and ultra-high frequency, or UHF (850–900 MHz). Microwave (2.45 GHz) is also used in some applications. The frequency used depends on the particular type of application.

Low-frequency systems are the least expensive and have the shortest range. They are most commonly used in security access, asset tracking, and animal identification applications.

High-frequency systems are used for applications such as railroad car tracking and automated toll collection.

Some typical RFID application areas are

- Metering applications such as electronic toll collection
- Inventory control and tracking such as merchandise control
- Asset tracking and recovery
- Tracking parts moving through a manufacturing process
- Tracking goods in a supply chain

The RFID Reader

Data is stored on the RFID tag in digital form and is transmitted to the reader as a modulated signal. Many RFID systems use ASK (amplitude shift keying) or FSK (frequency shift keying). In ASK, the amplitude of a carrier signal is varied by the digital data. In FSK, the frequency of a carrier signal is varied by the digital data. Examples of these forms of modulation are shown Figure 15–30. In this system, the carrier is 125 kHz, and the modulating signal is a digital waveform at the rate of 10 kHz, representing a stream of 1s and 0s.

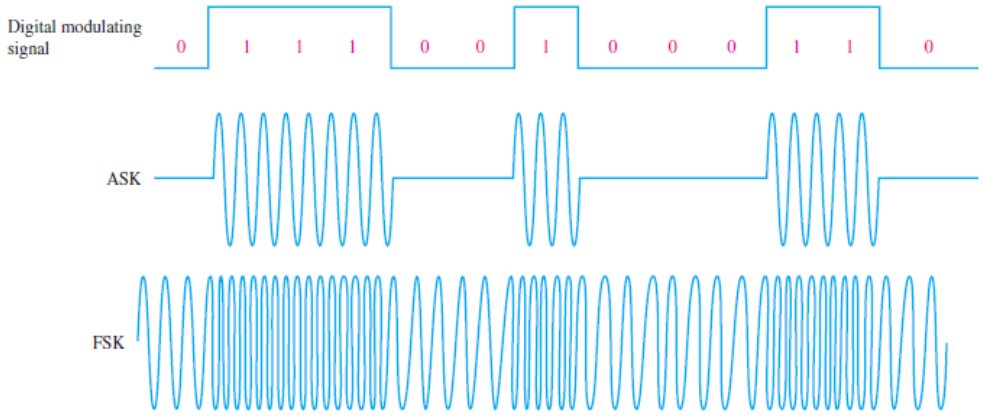


Fig 8.7 Examples of ASK and FSK modulation transmitted by an RFID tag.

DESIGN OF SCHMITT TRIGGER USING OPAMP

***Aim**: To design a Schmitt Trigger for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V),IC 741, Resistors, Capacitor, Breadboard, Connecting wires,probes.

THEORY:

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages.

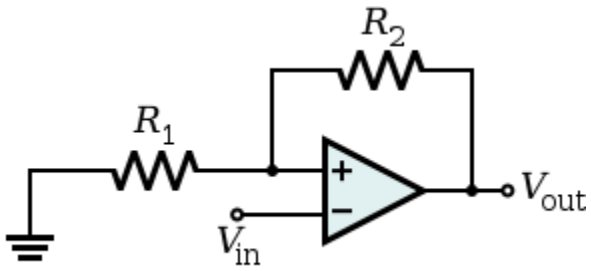


Fig9.1 Basic feedback circuit

WORKING PRINCIPLE:

- The Schmitt trigger is a comparator with positive feedback. It converts slowly varying waveforms into square wave.
- The input voltage is applied to the inverting terminal and the feedback circuit is connected to the non-inverting terminal. The input voltage triggers the output every time it exceeds certain voltage levels.
- These voltage levels are called as upper threshold voltage (VUT) and lower threshold voltage (VLT). As long as the input voltage is less than VUT the output remains at +Vsat.
- When Vi is just greater than VUT, the output regenerative switches to - Vsat and remains at this level. When the input voltage becomes lesser than VLT, the output switches from -Vsat + Vsat.

EXPERIMENT PROCEDURE:

- The connections are made as shown in the circuit diagram.
- The signal which has to be made square is applied to the inverting terminal.
- The i/p is a sine waveform. The supply voltage is switched ON and the o/p waveform is recorded through CRO.
- The UTP and LTP are also found and the theoretical and practical values are verified.
- LTP = R1/ (R1 + R2) X(-Vsat).
- UTP = R2 /(R1 + R2) X(+Vsat).

DESIGN:

Vsat=0.9Vcc=0.9X12V=10.8V

To find R1 and R2 values

Let Choose R2 = 1KΩ

$$\frac{R_1}{R_2} = \frac{V_{sat}}{V_{UT}} - 1$$

⇒ R1 = 47KΩ for VUT = 0.225V

CIRCUIT DIAGRAM and Model Waveform:

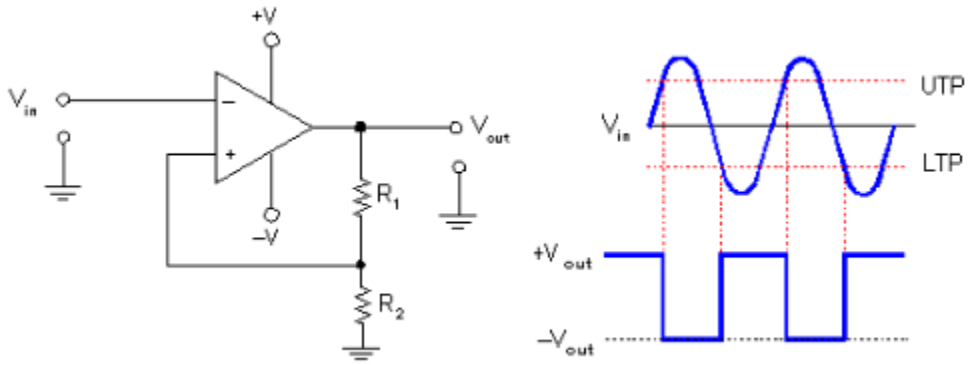


Fig.9.2 Circuit diagram for Schmitt trigger

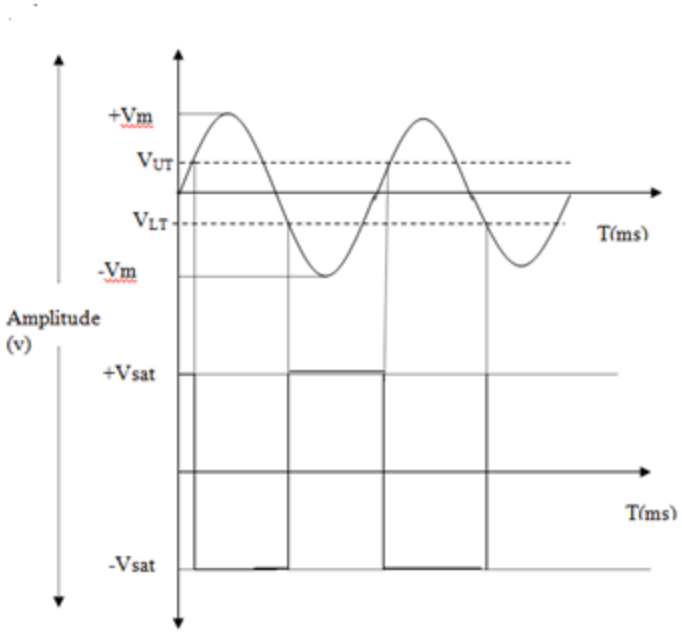


Fig.9.3 Model graph for Schmitt trigger

WORKSHEET

Waveform	**Nature**	**Amplitudes(Volts)**	**Time period(ms)**
Input waveform	Sine wave		
Output waveform	Square wave		

Conclusion:

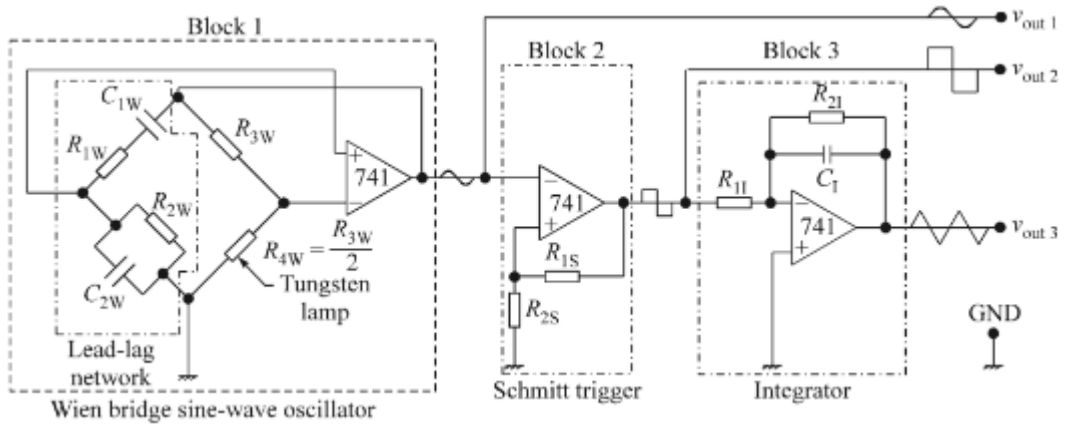
……

Viva Questions:

1. What is comparator?
2. What are the types of comparators?
3. What is the limiting factor of op-amp comparator?
4. Mention some applications of op-amp comparator
5. Explain the operation of zero crossing comparator.
6. Which feedback is employed in Schmitt trigger?
7. What is the other name for Schmitt trigger?
8. What is hysteresis?
9. What parameters determine the hysteresis?

Application of Schmitt trigger

Function Generator Using 741 op amp:



A function generator is a versatile instrument that delivers a choice of different waveforms whose frequencies are adjustable over a wide range. The most common outputs are the sine, triangular, square and sawtooth waveforms. The frequencies of these waveforms may be adjusted from a fraction of Hz to several hundred kHz. Figure 9.3 shows the circuit of a basic function generator that consists of three blocks: (1) Wien bridge sine wave oscillator, (2) Schmitt trigger, and (3) Integrator.

DESIGN OF RC PHASE SHIFT OSCILLATOR USING OPAMP

***Aim**: To design a RC Phase shift Oscillator for the given specifications using Op-Amp IC 741.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V),IC 741, Resistors, Capacitor, Breadboard, Connecting wires,probes.

THEORY:

Phase-shift oscillator is a simple electronic oscillator. It contains an inverting amplifier, and a feedback filter which 'shifts' the phase of the amplifier output by 180 degrees at the oscillation frequency. The filter produces a phase shift that increases with frequency. It must have a maximum phase shift of considerably greater than 180° at high frequencies, so that the phase shift at the desired oscillation frequency is 180°.

The most common way of achieving this kind of filter is using three identical cascaded resistor- capacitor filters, which together produce a phase shift of zero at low frequencies, and 270 degrees at high frequencies. At the oscillation frequency each filter produces a phase shift of 60 degrees and the whole filter circuit produces a phase shift of 180 degrees.

WORKING PRINCIPLE:

- The feedback network offers 180 degrees phase shift at the oscillation frequency and the op amp is configured as an Inverting amplifier, it also provide 180 degrees phase shift. Hence to total phase shift around the loop is 360=0degrees, it is essential for sustained oscillations.
- At the oscillation frequency each of the resistor capacitor filters produces a phase shift of 60° so the whole filter circuit produces a phase shift of 180°.
- The energy storage capacity of capacitor in this circuit produces a noise voltage which is similar to a small sine wave, it is then amplified using op amp inverting amplifier.
- By taking feedback, the output sine wave also attenuates 1/29 times while passing through the RC network, so the gain of inverting amplifier should be 29 in order to keep loop gain as unity.
- The unity loop gain and 360 degree phase shift are essential for the sustained oscillation.

- RC Oscillators are stable and provide a well shaped sine wave output with the frequency being proportional to 1/RC and therefore, a wider frequency range is possible when using a variable capacitor.
- However, RC Oscillators are restricted to frequency applications because at high frequency the reactance offered by the capacitor is very low so it acts as a short circuit.

EXPERIMENT PROCEDURE:

- Design the circuit for given frequency and calculate R1,R2,and Rf
- Connect the circuit as shown in the figure with the designed values.
- Switch on the power supply and observe the waveform.
- Note down the amplitude and time period.
- Plot the waveforms on a graph sheet.

DESIGN:

Let C=0.1μf, Then $f=\frac{1}{2\pi RC\sqrt{6}}$

R= (0.065)/(200*0.1μf)=3.25KΩ

To prevent the loading of amplifier R_1>10R, therefore R_1=10R=33KΩ;

$R_f=29R_1$

$R_f=29(33)=957K\Omega$

CIRCUIT DIAGRAM:

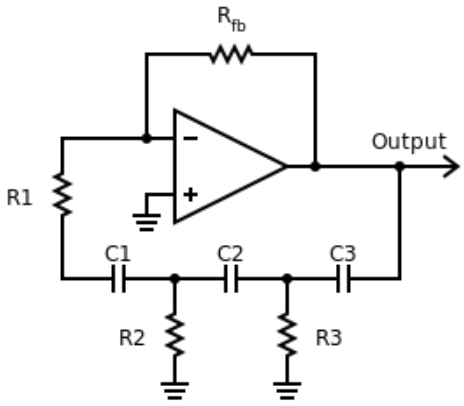


Fig.9.4. Circuit Diagram for RC Phase oscillator

MODEL GRAPH:

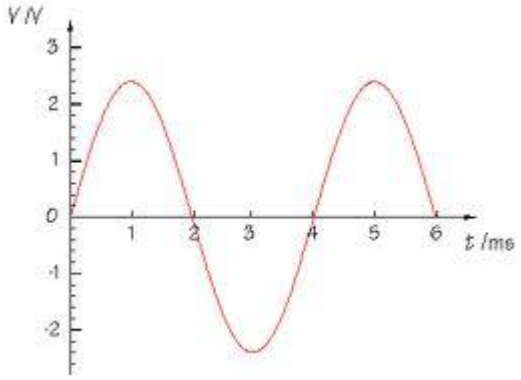


Fig.9.5. Model Graph for RC Phase oscillator

WORKSHEET

Waveform	Amplitude (V)	Time Period(sec)	Frequency(Hz)

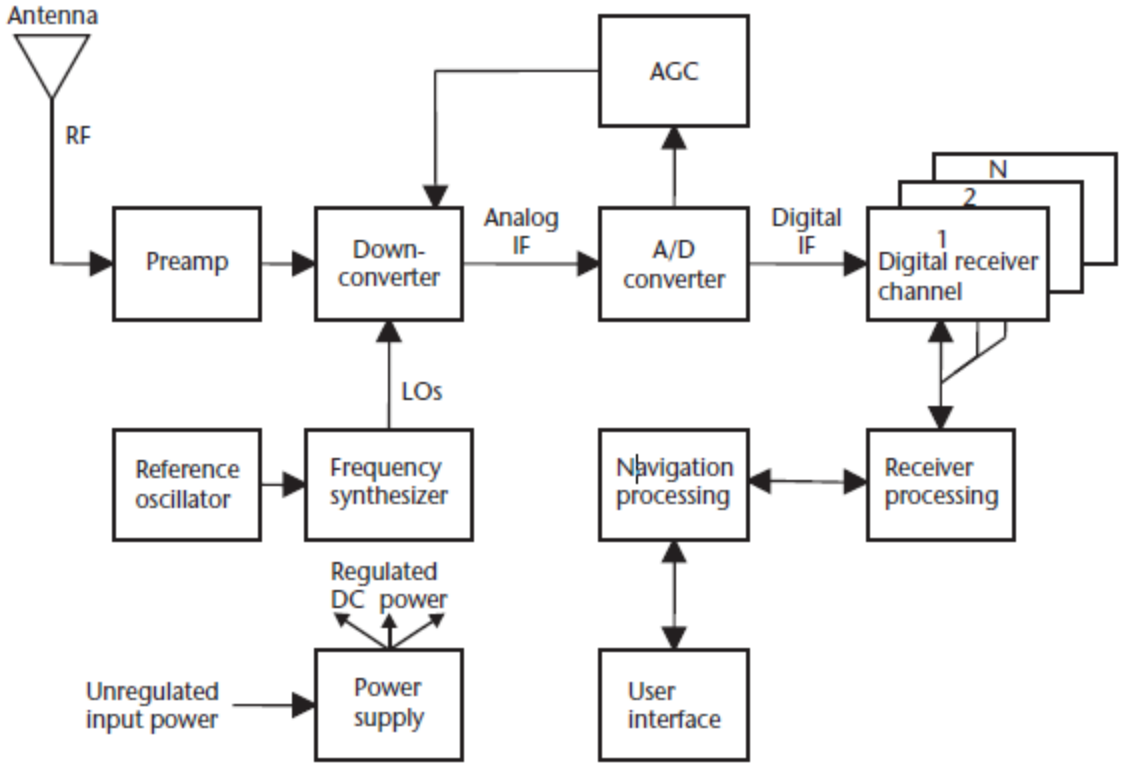
Conclusion:

……

Viva Question:

1. What happens at the output if R_f is changed?
2. How is phase shift oscillator different from RC phase shift oscillator?
3. What are the applications of phase shift oscillator?
4. What is the difference between relaxation oscillator and RC oscillator?
5. Why RC oscillators cannot generate high frequency oscillations
6. Why we need a phase shift between input and output signal?
7. How can we get a maximum phase angle of 90 degrees in RC phase shift oscillator.
8. How is phase angle determined in RC phase shift oscillator?

APLLICATION:



General digital GPS receiver block diagram.

STUDY OF FREQUENCY MULTIPLIER USING PLL IC

***Aim**: To Study the operation of NE565 PLL as a Frequency Multiplier.*

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO (30 MHz), Dual RPS Voltmeter (0-30V), NE565 IC, 7490 IC,2N3391, Resistors, Capacitor, Breadboard, Connecting wires, probes.

EQUIPMENT AND COMPONENTS REQUIRED:

Function Generator (3MHz), CRO(30 MHz), Dual RPS(0-30V),IC 741,Resistors, Capacitor,Breadboard, Connecting wires.

THEORY:

Figure shows the block diagram of a frequency multiplier using the 565 PLL. The frequency counter is inserted between the VCO and the phase comparator. Since the output of the divider is locked to the input frequency f_{IN}, the VCO is actually running at a multiple of the input frequency.

The desired amount of multiplication can be obtained by selecting a proper divide by N network, where N is an integer. For example, to obtain the output frequency $f_{OUT} = 5 f_{IN}$, a divide by N = 5 network is needed. The 4 bit binary counter (7490) is configured as a divide by 5 circuit. The transistor Q is used as a driver stage to increase the driving capability of the NE 565. C3 is used to eliminate possible oscillation. C2 should be large enough to stabilize the VCO frequency.

WORKING PRINCIPLE:

The block diagram of a frequency muliplier (or synthesizer) is shown in figure. In this circuit, a frequency divider is inserted between the output of the VCO and the phase comparator (PC) so that the loop signal to the PC is at frequency fOUT while the output of VCO is N fOUT. This output is a multiple of the input frequency as long as the loop is in lock. The desired amount of multiplication can be obtained by selecting a proper divide- by N network where N is an integer. Figure shows this function performed by a 7490 configured as a divide-by-4 circuit.

In this case the input Vin at frequency /in is compared with the output frequency fOUT at pin 5. An output at N fOUT (4 fOUT in this case) is connected through an inverter circuit to give an input at pin 14 of the 7490, which varies between 0 and + 5 V. Using the output at pin 9, which is one-fourth of that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock.
Since the VCO can be adjusted over a limited range from its centre frequency, it may become necessary to change the VCO frequency whenever the divider value is changed.

For verification of the circuit operation, one must determine the input frequency range and then adjust the free running fOUT of the VCO by means of R1 and *C*1 so that the output frequency of the 7490 divider is midway within the predetermined input frequency range. The output of VCO should now be equal to 4 *fin.*

EXPERIMENT PROCEDURE:

1. Connect the circuit as shown in figure.

2. The free running frequency f_{OUT} of VCO is varied by adjusting R1 and C1 and the output frequency is determined and it should be 5 times the input frequency.

3. Determine the output frequency for different input frequency of 1 KHz and 1.5 KHz.

CIRCUIT DIAGRAM:

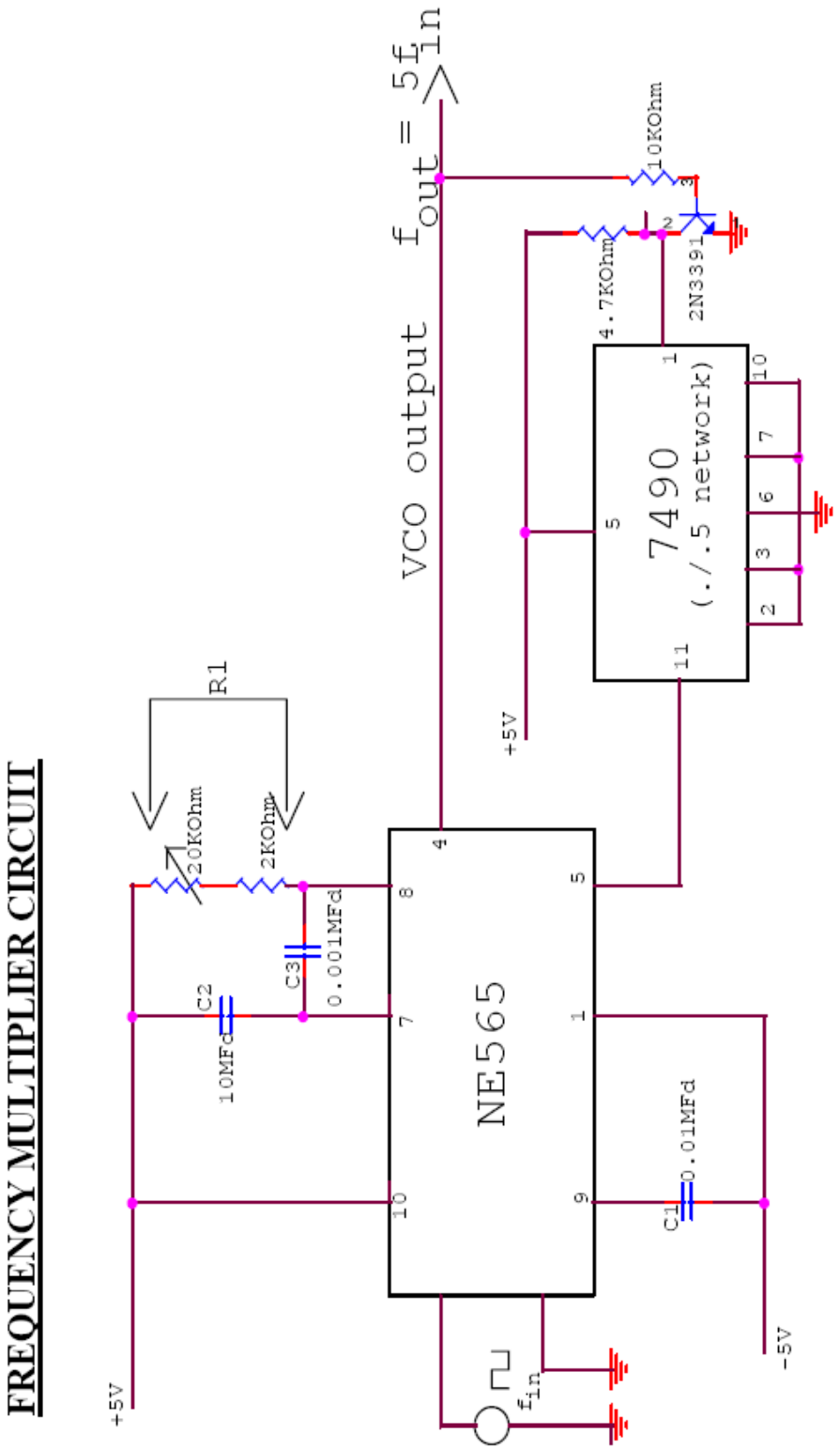


Fig.10.1. Circuit Diagram for Frequency Multiplier

TABULATION:

INPUT		OUTPUT	
AMPLITUDE	**FREQUENCY**	**AMPLITUDE**	**FREQUENCY**

Conclusion:

……

Viva Question:

1. What are the other applications of PLL?
2. Explain the working of the transistor 2N3391?
3. What is VCO? Explain its working.
4. What are the characteristics of PLL?
5. What is IC 7490?