

## Analysis of the Circuit in Figure A

### 1. Overview

The circuit in Figure A represents a high-speed operational amplifier-based amplifier with a push-pull output stage. The design ensures stability, high gain, and the ability to drive significant loads with minimal distortion.

### 2. Components and Their Functions

#### (A) Input Stage

- **R8 (1kΩ) & R13 (100kΩ):** Form a voltage divider to set the input bias.
- **D3 & D4 (1N5235, 6.8V Zener Diodes):** Provide voltage regulation and set the biasing for the transistors.
- **R7 & R12 (10kΩ each):** Provide biasing for Q5 and Q6.
- **Q5 (PN2222A, NPN) & Q6 (PN2907A, PNP):** Act as current sources for the input differential amplifier.
- **U1 (AD8610 Op-Amp):** High-speed precision operational amplifier used for voltage gain and error correction.

#### (B) Frequency Compensation

- **C1 (100pF) & C2 (22pF):** Stabilize high-frequency response and improve phase margin.
- **R6 (90kΩ):** Works with C2 for frequency compensation.

#### (C) Gain Setting & Feedback Network

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**R1 (4.99kΩ) & R2 (499Ω):** Set the gain of the amplifier. The gain is given by:

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$$G = 1 + R1/R2 = 1 + 4.99\text{k}\Omega / 499\Omega \approx 1.1\text{Gohm}$$

#### (D) Output Stage (Push-Pull Configuration)

- **Q1 - Q3 (ZDT751 Dual NPN Transistors) & Q2 - Q4 (ZDT651 Dual PNP Transistors):** Act as a push-pull class AB amplifier for delivering high current to the load.
- **R4 & R3 (39.2Ω each):** Provide emitter degeneration for better linearity.
- **R9 & R10 (10Ω each):** Improve stability and current sharing in the push-pull stage.
- **R14 (100Ω):** Ensures proper biasing at the output stage.

### (E) Power Supply Decoupling

- **C3 & C2 (10 $\mu$ F each):** Provide decoupling to stabilize power supply rails (+24V and -24V).
- **R11 (10k $\Omega$ ):** Works with D3 and D4 for proper biasing.

### (F) Load Considerations

- **R<sub>L</sub> ( $\geq 500\Omega$ ):** The circuit is designed to drive a load of at least 500 $\Omega$ . If more power is required, a buffer stage may be needed.

## 3. Performance Analysis

- **Voltage Gain:**  $\sim 11$  (set by R1 and R2)
- **Output Swing:** Close to  $\pm 24V$  but limited by transistor saturation.
- **Frequency Response:** Determined by C1, C2, and associated resistances.
- **Output Impedance:** Low, ensuring it can drive moderate loads with minimal distortion.

## 4. Enhancements for 20V Sine Wave Output

- **Increase supply voltage (if components allow) to ensure full 20V swing.**
- **Add a buffer stage (e.g., Class AB MOSFET amplifier) for higher current drive.**
- **Use a transformer at the output for voltage scaling and isolation if required.**

## Conclusion

This circuit effectively amplifies the input signal with low distortion and stable operation. By adding a buffer stage, it can be adapted to drive higher power loads and achieve a 20V sine wave output.

The circuit diagram shows a precision current source. An input voltage  $V_{IN}$  is connected to a network of resistors  $R_8$  (1k $\Omega$ ) and  $R_{13}$  (100k $\Omega$ ). The non-inverting input (pin 3) of the AD8610 op-amp is connected to the junction of  $R_8$  and  $R_{13}$ . The inverting input (pin 2) is connected to the base of transistor  $Q_5$  (PN2222A) and the emitter of transistor  $Q_6$  (PN2907A). Transistor  $Q_5$  has its emitter connected to  $+V_s$  (+24V) through resistor  $R_4$  (39.2 $\Omega$ ) and its collector connected to the base of transistor  $Q_1$  (\*Q1). Transistor  $Q_6$  has its emitter connected to  $-V_s$  (-24V) through resistor  $R_3$  (39.2 $\Omega$ ) and its collector connected to the base of transistor  $Q_2$  (\*Q2). The op-amp output (pin 6) is connected to the base of transistor  $Q_4$  (\*Q4) and the emitter of transistor  $Q_3$  (\*Q3). Transistor  $Q_4$  has its emitter connected to  $-V_s$  (-24V) through resistor  $R_{10}$  (10 $\Omega$ ) and its collector connected to the base of transistor  $Q_2$ . Transistor  $Q_3$  has its collector connected to  $+V_s$  (+24V) through resistor  $R_9$  (10 $\Omega$ ) and its emitter connected to the base of transistor  $Q_1$ . The output current  $I_{OUT}$  is taken from the collector of transistor  $Q_2$  through resistor  $R_1$  (4.99k $\Omega$ ) to ground. The output voltage  $V_{OUT}$  is measured across  $R_1$ . The circuit is biased with  $+V_s$  (+24V) and  $-V_s$  (-24V). Compensation capacitors  $C_1$  (100pF) and  $C_2$  (22pF) are connected between the op-amp output and the bases of  $Q_3$  and  $Q_4$ . Resistor  $R_2$  (499 $\Omega$ ) is connected between the op-amp output and ground. Resistor  $R_6$  (90k $\Omega$ ) is connected between the bases of  $Q_1$  and  $Q_2$ . Resistor  $R_{14}$  (100k $\Omega$ ) is connected between the base of  $Q_2$  and the output node. Diodes  $D_3$  (1N5235, 6.8V) and  $D_4$  (1N5235, 6.8V) are connected between the bases of  $Q_5$  and  $Q_6$  and the input network. Capacitors  $C_3$  (10 $\mu$ F) and  $C_4$  (10 $\mu$ F) are connected between the  $+V_s$  and  $-V_s$  rails and ground.

\* Q1- Q3 = ZDT751 dual,  
or paired and thermally linked  
ZTX753s

\* Q2 - Q4 = ZDT651 dual,  
or paired and thermally linked  
ZTX653s

