IRIS Labs Hardware Assignment I

Q1.

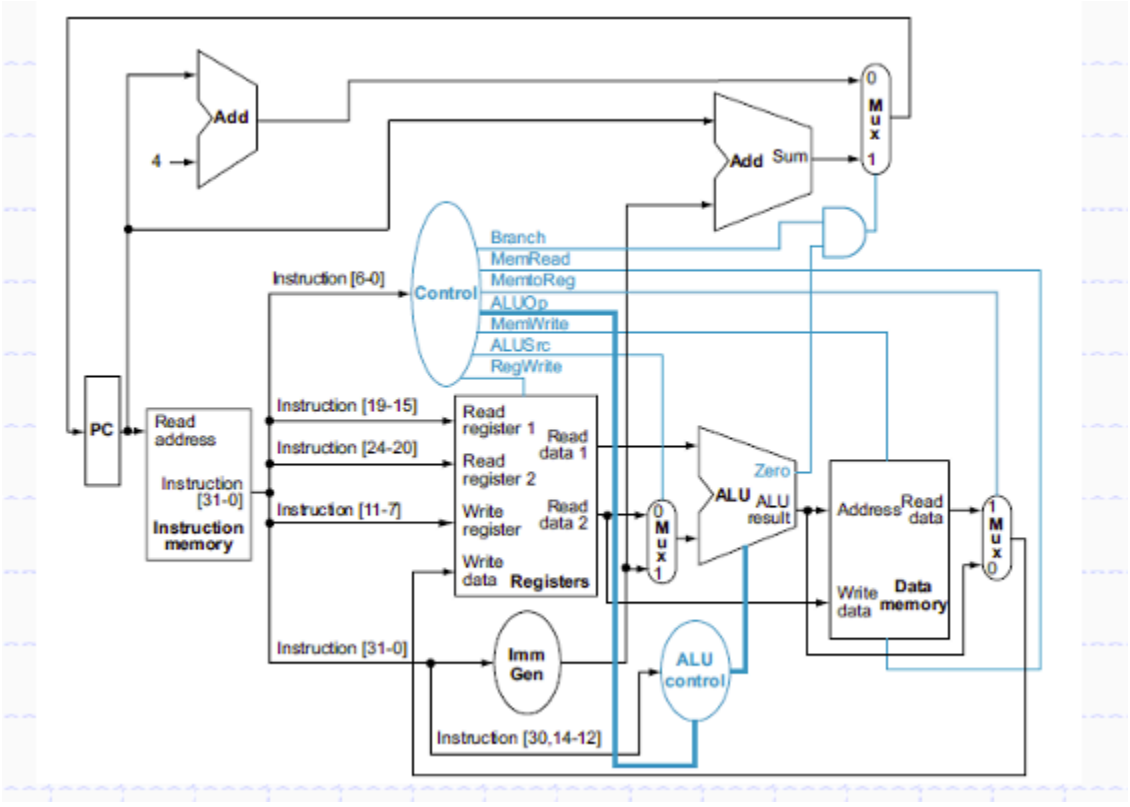
Complete the design of a single-cycle RISC-V processor that supports the following instructions: `ADD`, `SUB`, `LW`, `SW`, `BEQ`, `BGT`, `ADDI`, `SLLI`,ORI and `JAL`. You are provided with a Verilog boilerplate that includes the basic structure of the processor. Your task is to complete the missing components, ensuring that all instructions execute correctly within a single clock cycle. Implement the necessary data path and control logic, and verify your design using the provided testbench.

Deliverables:

1. Complete Verilog code for the processor.
2. Functional simulation results demonstrating correct execution of the given instructions.
3. Explanation of your design choices, including any optimizations or assumptions made.

[Files for Question 1]

Q2.



Consider the above datapath for all the questions

a) Write down the values of all the control signals for beq, sw and lw instructions. Use "x" for don't care.

b) Consider the following RISC-V assembly code:

```
loop: slt x2,x0,x1
        beq x2,x0,DONE
        addi x1,x1,-1
        addi x2,x2,2
        j loop
 done:
```

Assume the register x1 is initialized to the value 8. What is the final value in register x2 assuming the x2 is initially 2?

c) Modify the single cycle RISC V datapath to add a custom instruction, that counts the number of trailing zeros, in register rs1

What are the new control signals required?

Q3.(Whoever delivers it gets a cookie from ~~vinit~~🍪🍪) :) Bonus

a) **Add the entire RV32I support to your RISC-V processor**
b) **Make the processor pipelined (The more pipelining stages you add, the more pizza slices 🍕you get)**

Submission instructions will be forwarded in the whatsapp group soon….