H11H4-AM V:1.1

SCHEMATICS TABLE:

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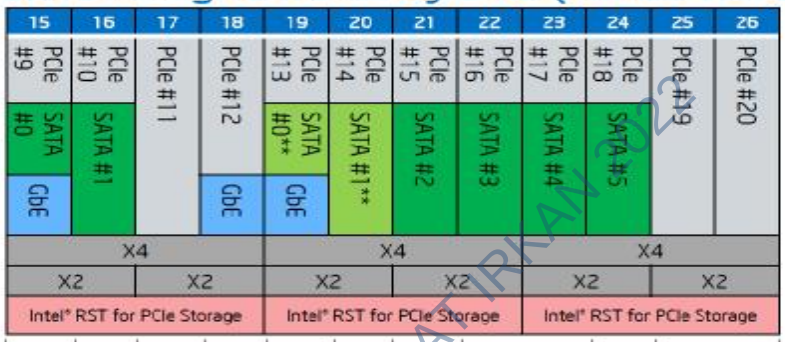
HSIO Lane Assignements by SKU (Lanes 1-14)

HSIO Lane Assignements by SKU (Lanes 15-26)



Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

Elitegroup Computer Systems

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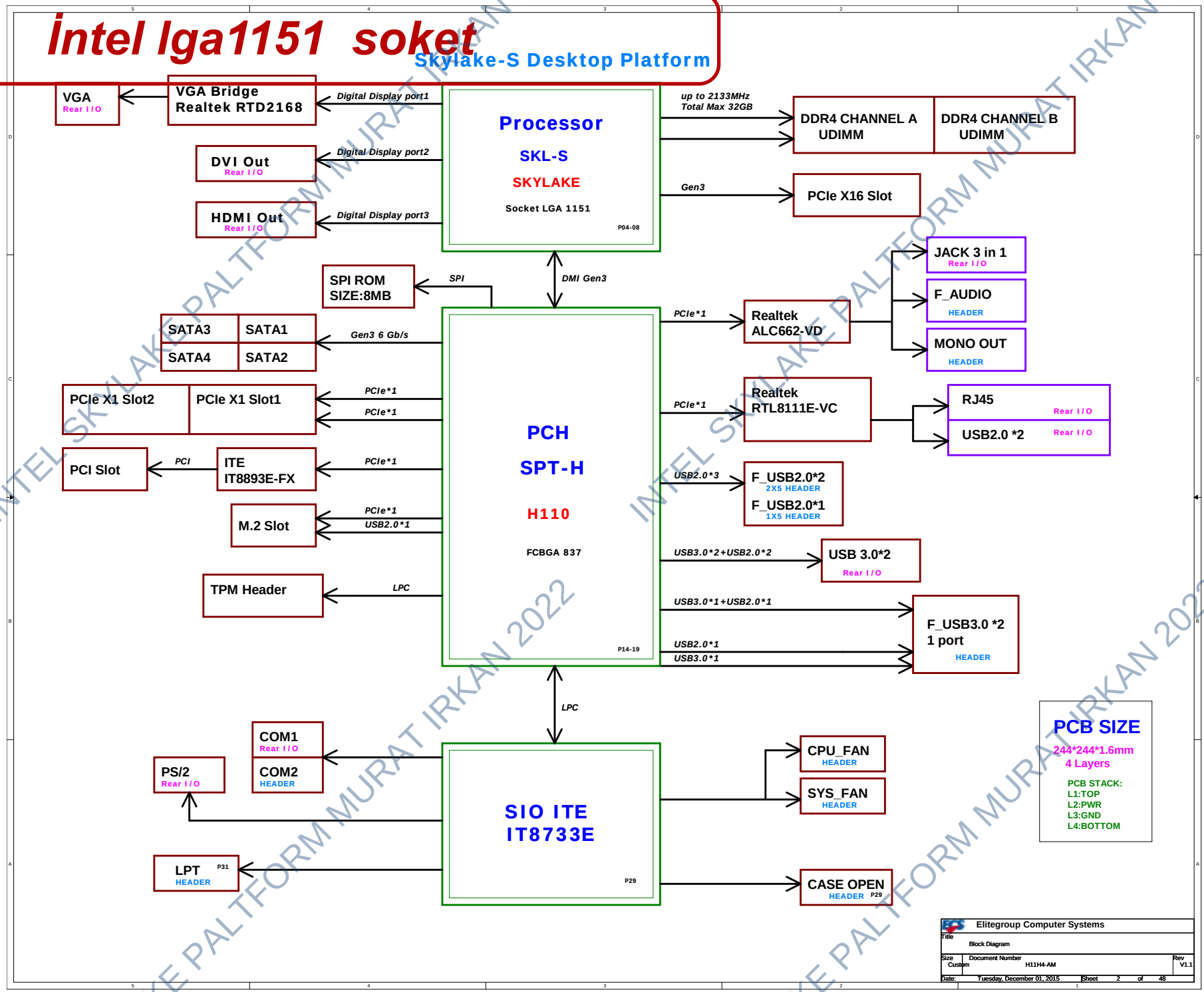
İntel lga1151 soket

Skylake-S Desktop Platform



PCH-GPIO function

Data:2014/10/02

Pin Name	Power Well	Usage	Default Status	Boot Set(BIOS Check)
GPP_A11	3VSB	PME_L	PME#	PME#
GPP_G13	VCC3	HDPANEL_DETECT	GPI	GPI
GPP_G14	VCC3	on-board TPM detect	GPI	GPI
GPP_E7	VCC3	THERMAL_SD	GPI	GPI
GPP_B3	3VSB	BT_DIS_L	GPI	GPO-->Hi
GPP_H15	3VSB	for ACER reserve	GPI	GPI
GPP_H14	3VSB	for ACER reserve	GPI	GPI
GPP_E9	3VSB	BIOS WP Jumper	GPI	GPI
GPP_F16	3VSB	USB_EN	GPI	GPO-->Hi
GPP_F17	3VSB	LPC_PME_L	GPI	GPI
GPP_E0	VCC3	OBR	GPI	GPI
GPD11	DSW	LAN_DIS_L	LANPHYPC	LANPHYPC
GPD9	DSW	PCH_RI_L	SLP_WLAN#	GPI
GPD10	DSW	ME Disable	SLP_S5#	GPO-->Low
GPD0	DSW	RLAN_PWR_EN	BATLOW#	GPO-->Hi
GPP_F22	VCC3	PCH_GPP_F22	GPI	PCH_GPP_F22
GPP_G22	VCC3	TP_VGA	GPI	TP_VGA
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPI	CLK_REQ1_M.2_WLAN_L
GPP_B17	3VSB	M.2_DIS_L_R	GPI	M.2_DIS_L_R

SIO-GPIO function

Data:2013/10/01

Pin Name	Power Well	Usage	Default SET

Interrupt mapping

Data:2014/11/10

Function	INT# port	PCIe*1 port	Device

Elitegroup Computer Systems	
Title	GPIO Function/INT# Mapping
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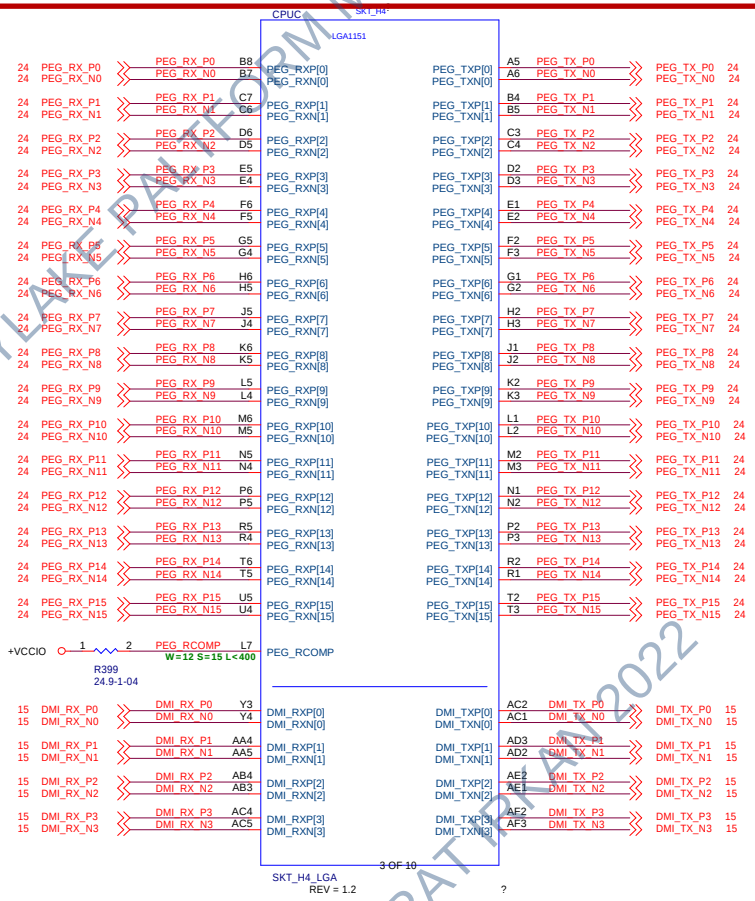
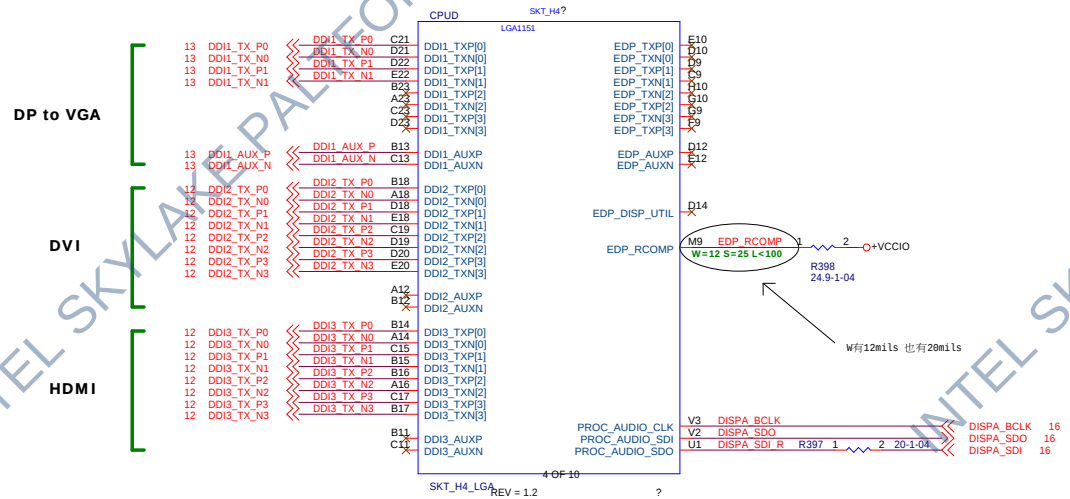
INTEL LGA1151 SOKET PLATFORM





Elitegroup Computer Systems	
Title	CPU-PEG/DMI/DDI/EDP
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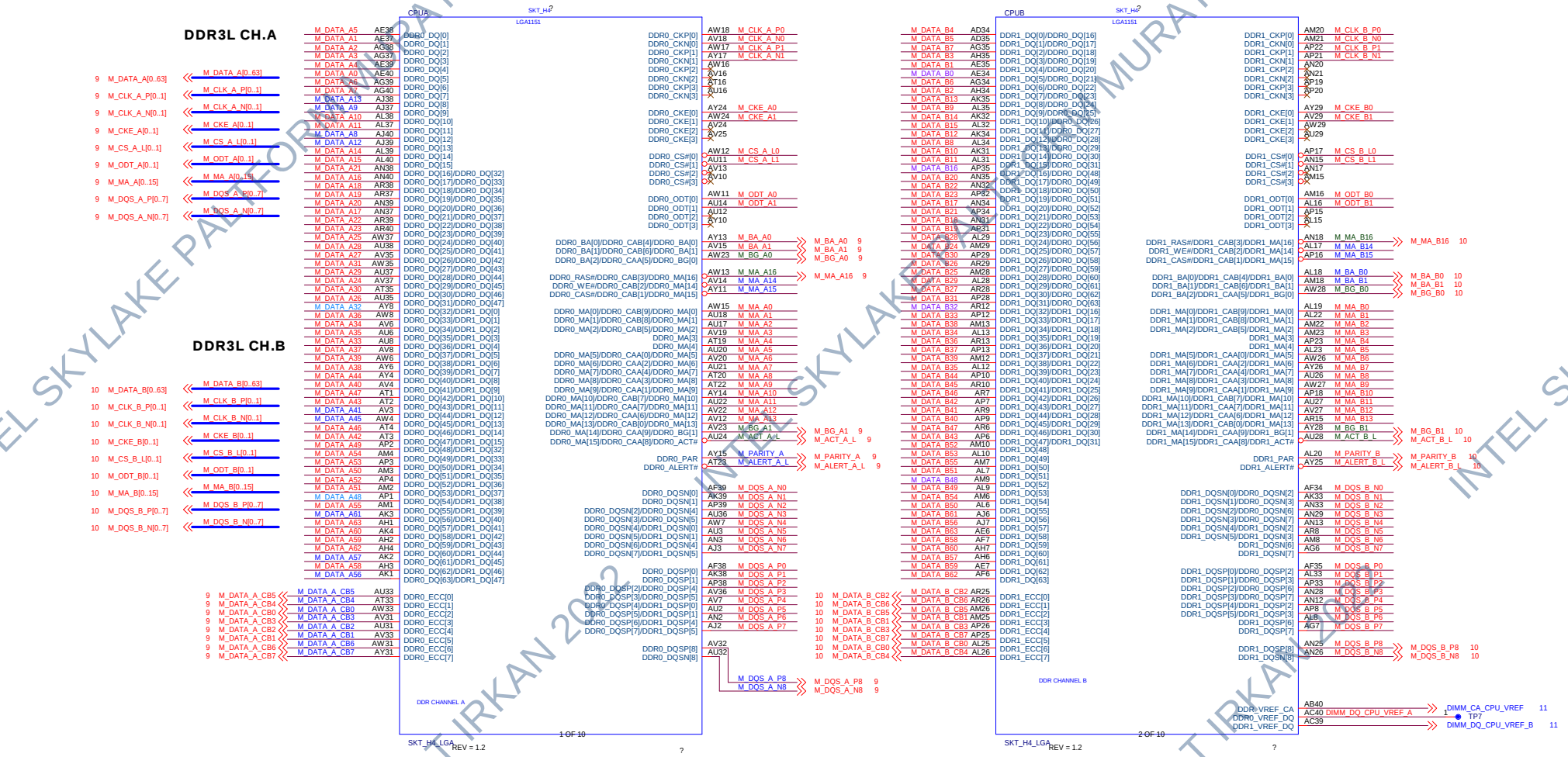
INTEL LGA1151 SOKET PLATFORM



Elitegroup Computer Systems	
Title	DDR4
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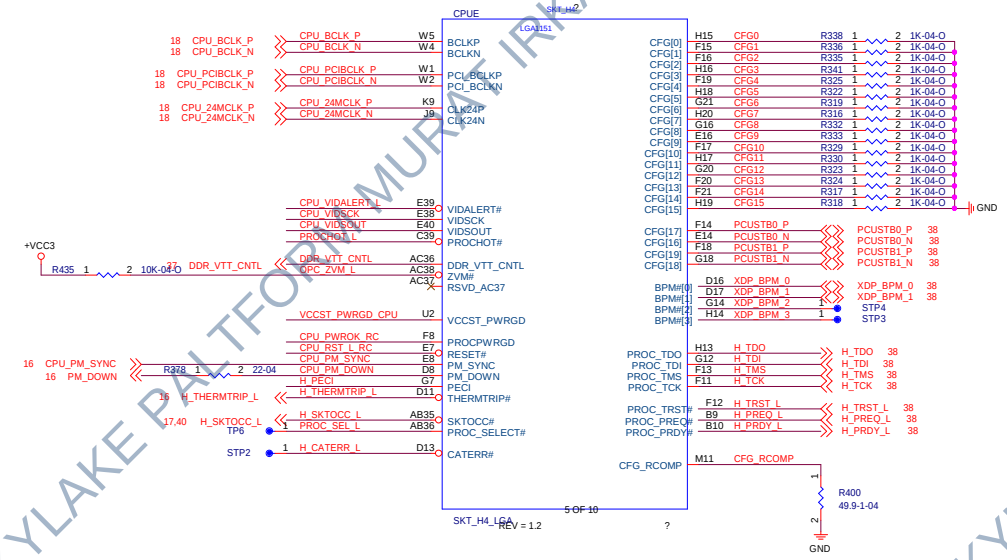
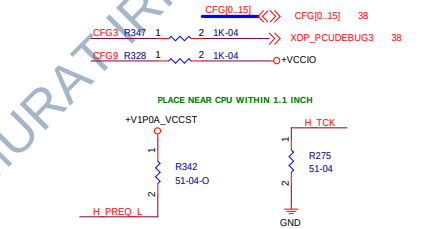
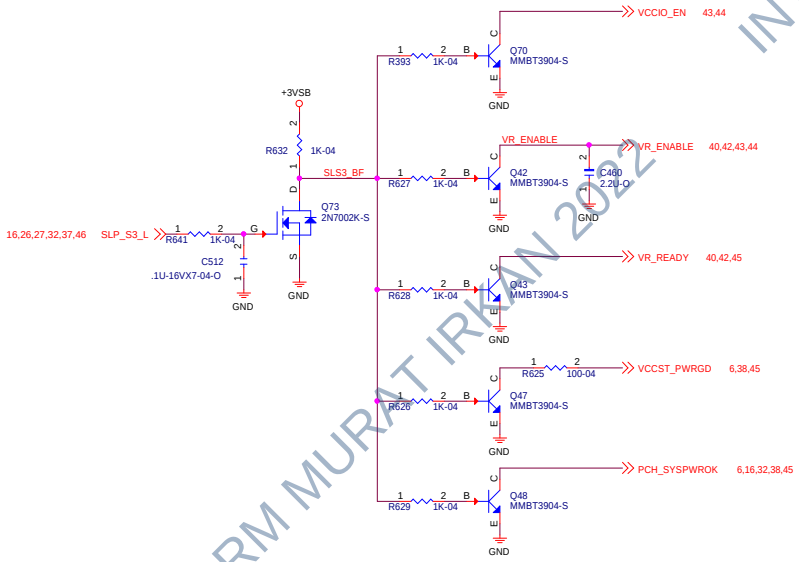


CFG[0:15] Configuration note

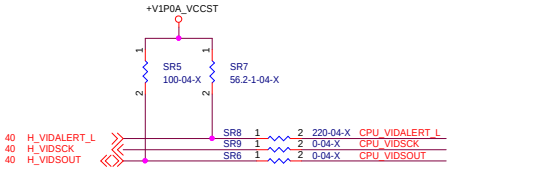
- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 0 = Disabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x16, 2 x8 PCI Express*
  - 01 = Reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x8, 2 x4 PCI Express*
- **CFG[7]:** PEG Training:
  - 0 = Disable PEG Train Immediately following RESET# de-assertion.
  - 1 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

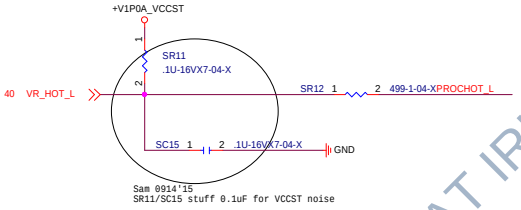


Sequencing Circuit

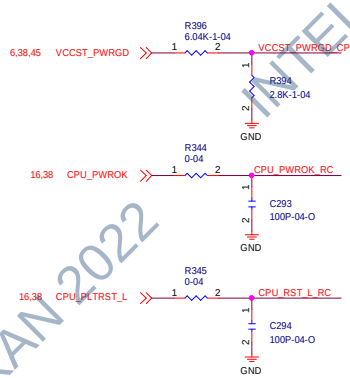


Asynchronous & Sideband Signal

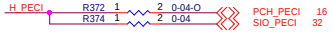




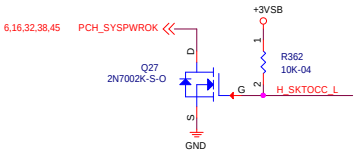
Processor Power Good



PECI



SKTOCC#



Elitegroup Computer Systems		
Title: CPU-MISC		
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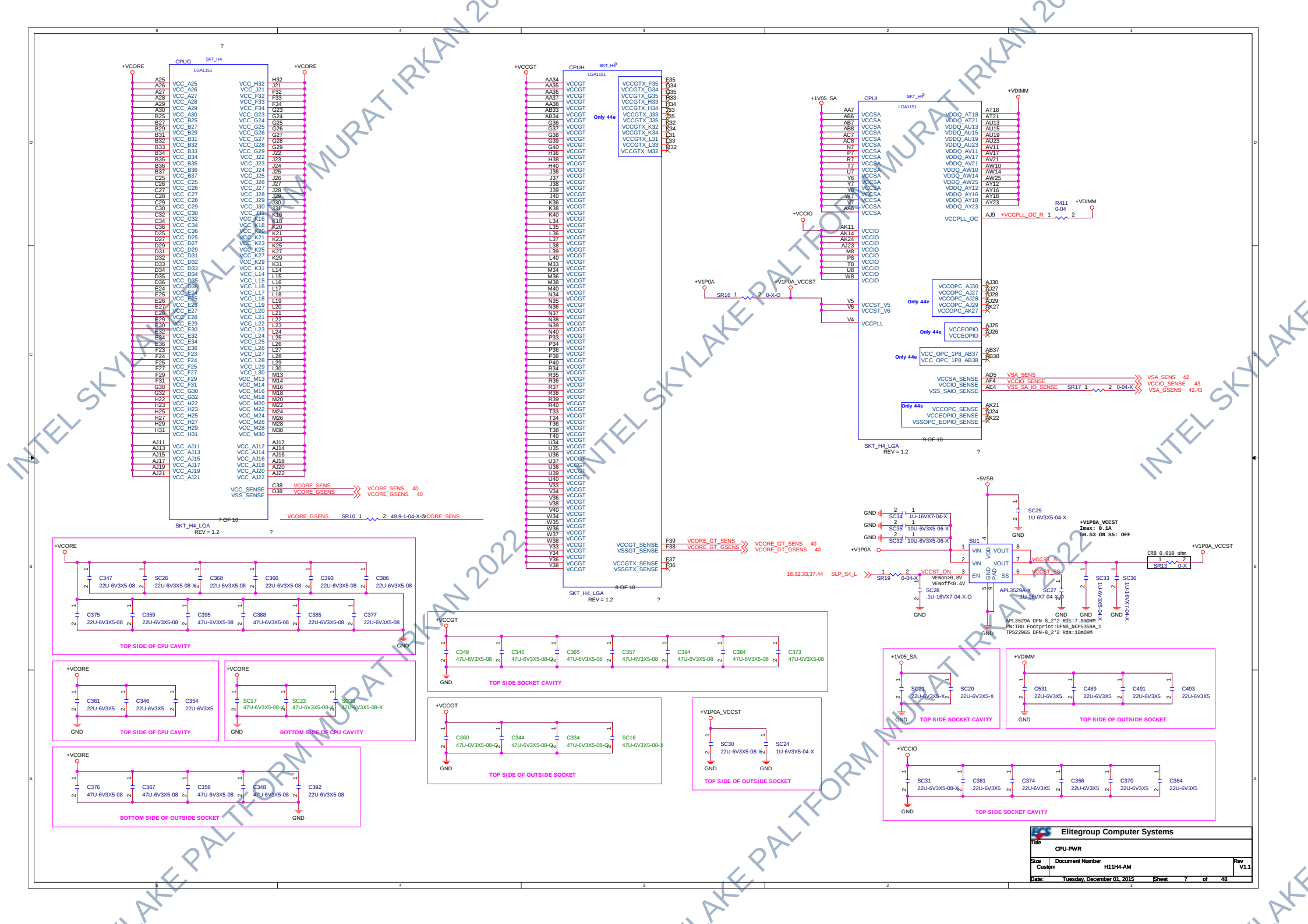
CPUG
SKT_H4
LGA1151
+VCORE
VCC_SENSE
VSS_SENSE
VCORE_SENS
VCORE_GSENS
VCORE_SENS 40
VCORE_GSENS 40
SR10 49.9-1-04-X-O
7 OF 10
SKT_H4_LGA
REV = 1.2
CPUH
+VCCGT
VCCGTX_SENSE
VSSGTX_SENSE
VCCGT_SENSE
VSSGT_SENSE
VCORE_GT_SENS
VCORE_GT_GSENS
VCORE_GT_SENS 40
VCORE_GT_GSENS 40
8 OF 10
CPUI
+1V05_SA
+VDIMM
+VCCIO
+V1P0A
+V1P0A_VCCST
SR16 0-X-O
VCCPLL_OC
VCCOPC_AJ30
VCCOPC_AJ27
VCCOPC_AJ28
VCCOPC_AJ29
VCCOPC_AK27
VCCEOPIO
VCC_OPC_1P8_AB37
VCC_OPC_1P8_AB38
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VSA_SENS
VCCIO_SENSE
VSS_SA_IO_SENSE
SR17 0-04-X
VSA_SENS 42
VCCIO_SENSE 43
VSA_GSENS 42,43
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
9 OF 10
R411 0-04
+VCCPLL_OC_R
Only 44e
+5VSB
SU1
APL3529A-X
1U-16VX7-04-X-O
SC28 .1U-16VX7-04-X-O
SC25 1U-6V3X5-04-X
SC33 1U-6V3X5-04-X
SC36 1U-16VX7-04-X
SC27
SC34 1U-16VX7-04-X
SC35 10U-6V3X5-06-X
SC32 10U-6V3X5-06-X
VCCST_ON
VCCST_S
VCCST_SS
SLP_S4_L
16,32,33,37,44
VENon>0.8V
VENoff<0.4V
+V1P0A_VCCST
Imax: 0.1A
S0.S3 ON S5: OFF
CRB 0.010 ohm
SR13 0-X
APL3529A DFN-8_2*2 Rds:7.8mOHM
PN:TBD Footprint:DFN8_NCP5359A_1
TPS22965 DFN-8_2*2 Rds:16mOHM
TOP SIDE OF CPU CAVITY
TOP SIDE SOCKET CAVITY
TOP SIDE OF OUTSIDE SOCKET
BOTTOM SIDE OF CPU CAVITY
BOTTOM SIDE OF OUTSIDE SOCKET
Elitegroup Computer Systems
CPU-PWR
H11H4-AM
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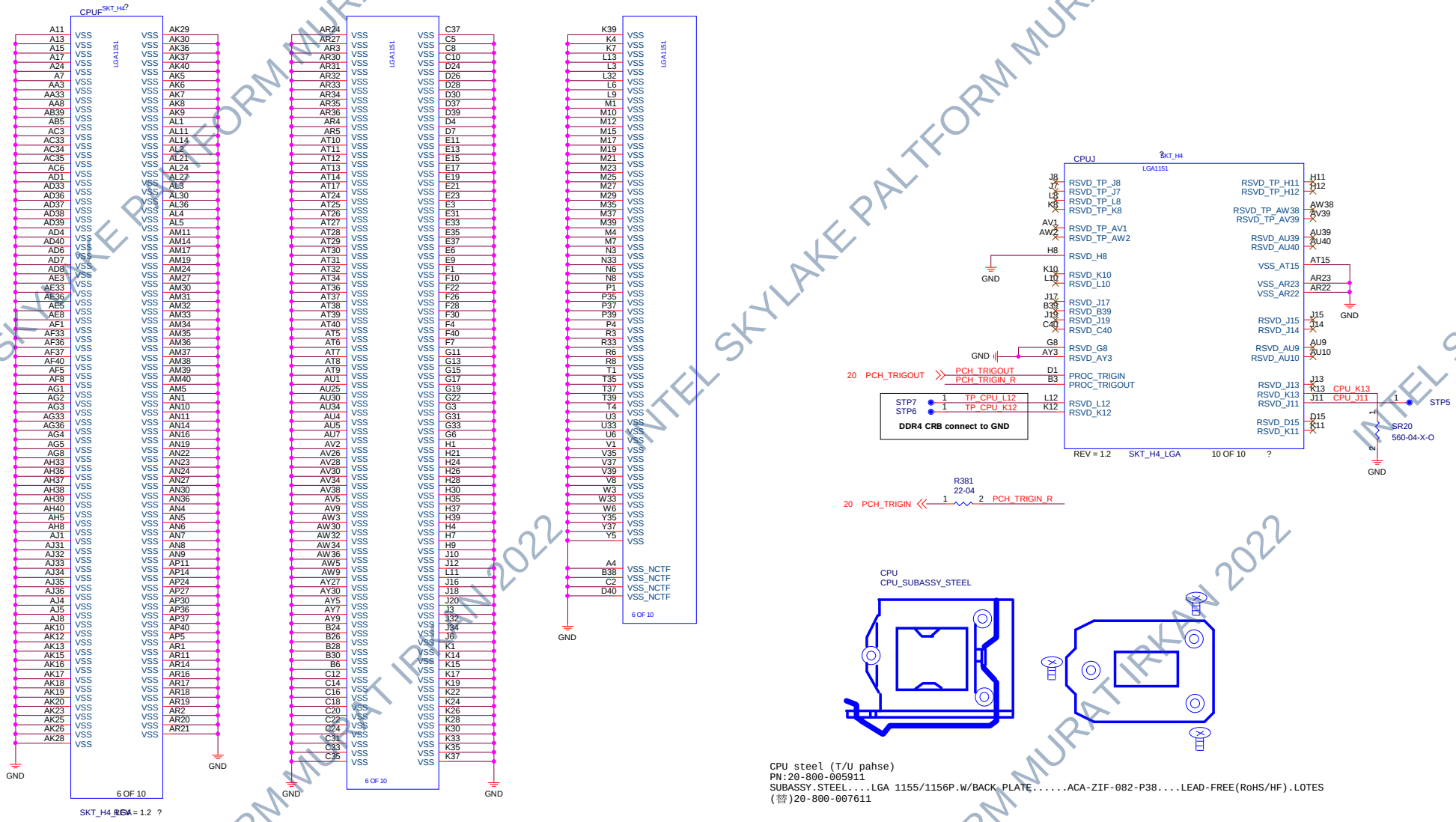
7
48



CPU steel (T/U pahse)
PN:20-800-005911
SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES
(替)20-800-007611

Elitegroup Computer Systems		
Title: CPU-GND		
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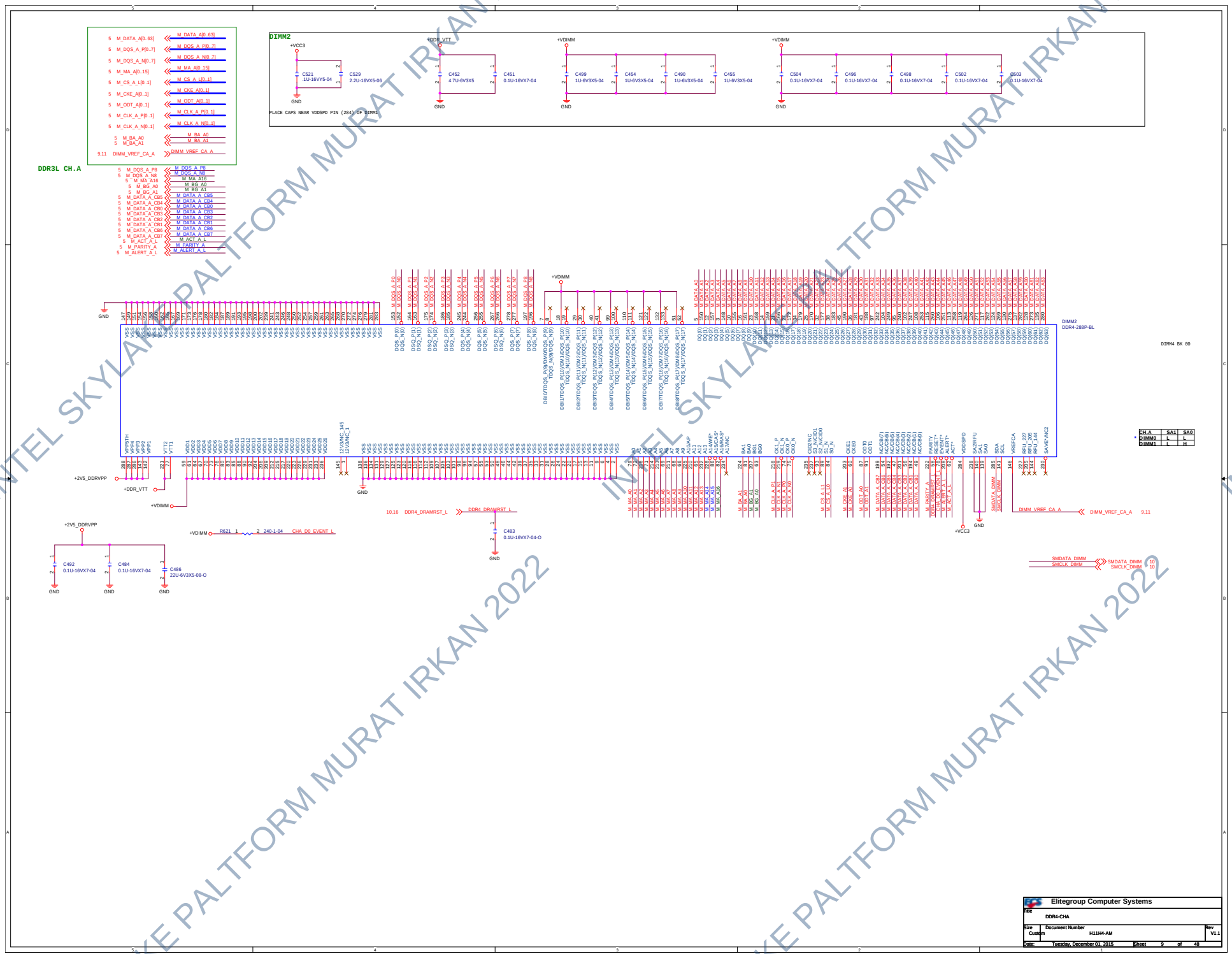

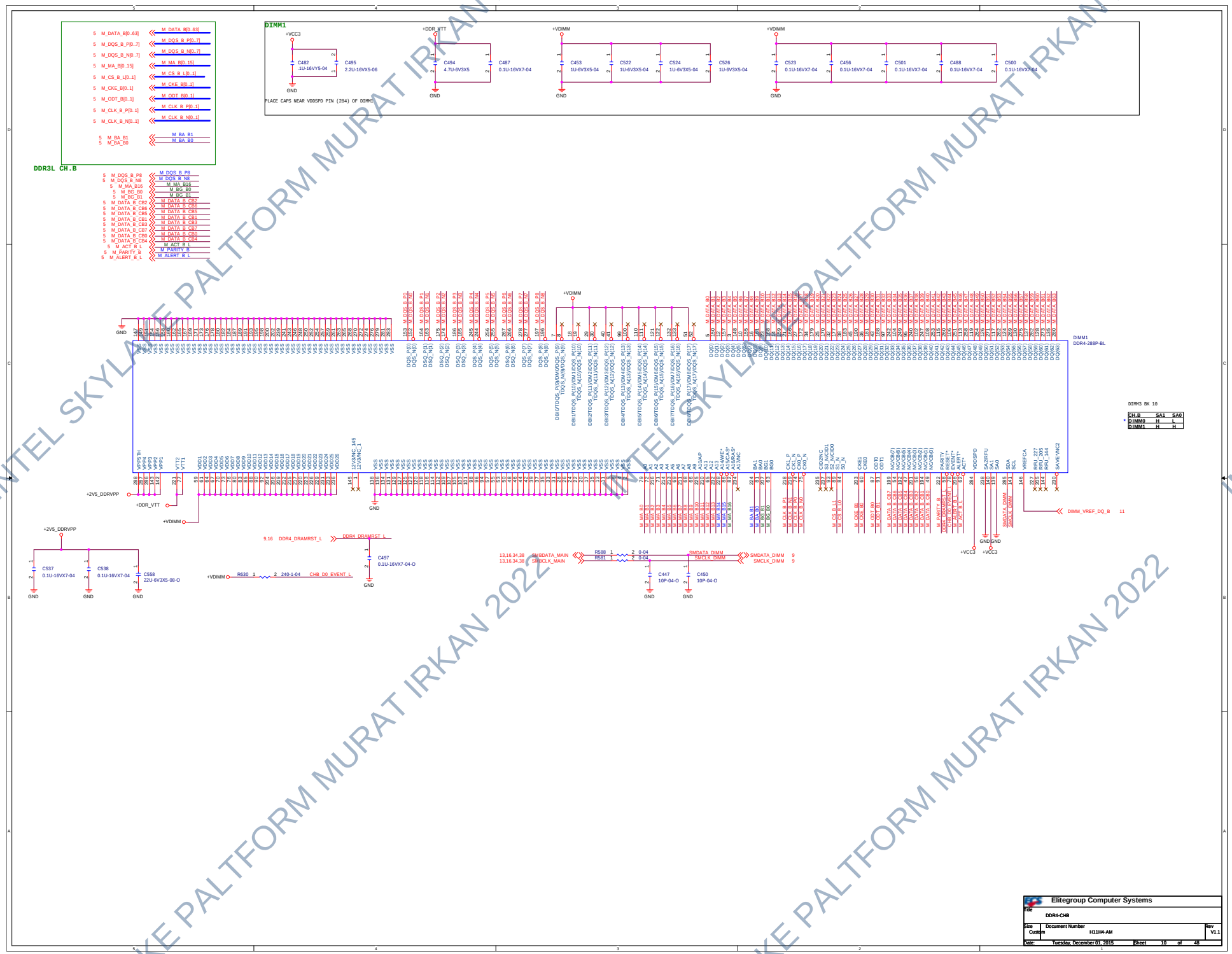

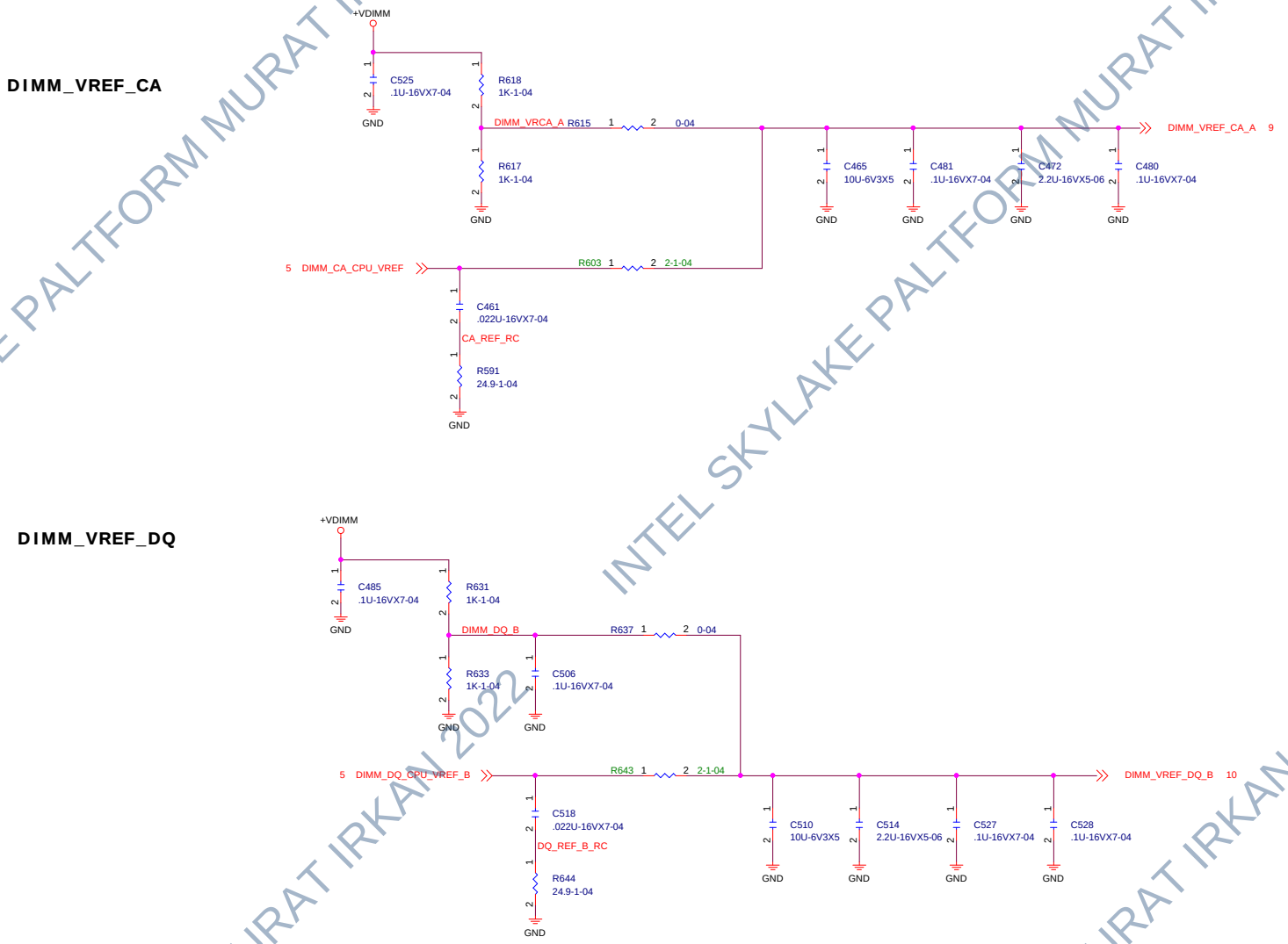

Elitegroup Computer Systems			
Title: DDR3L-CHB			
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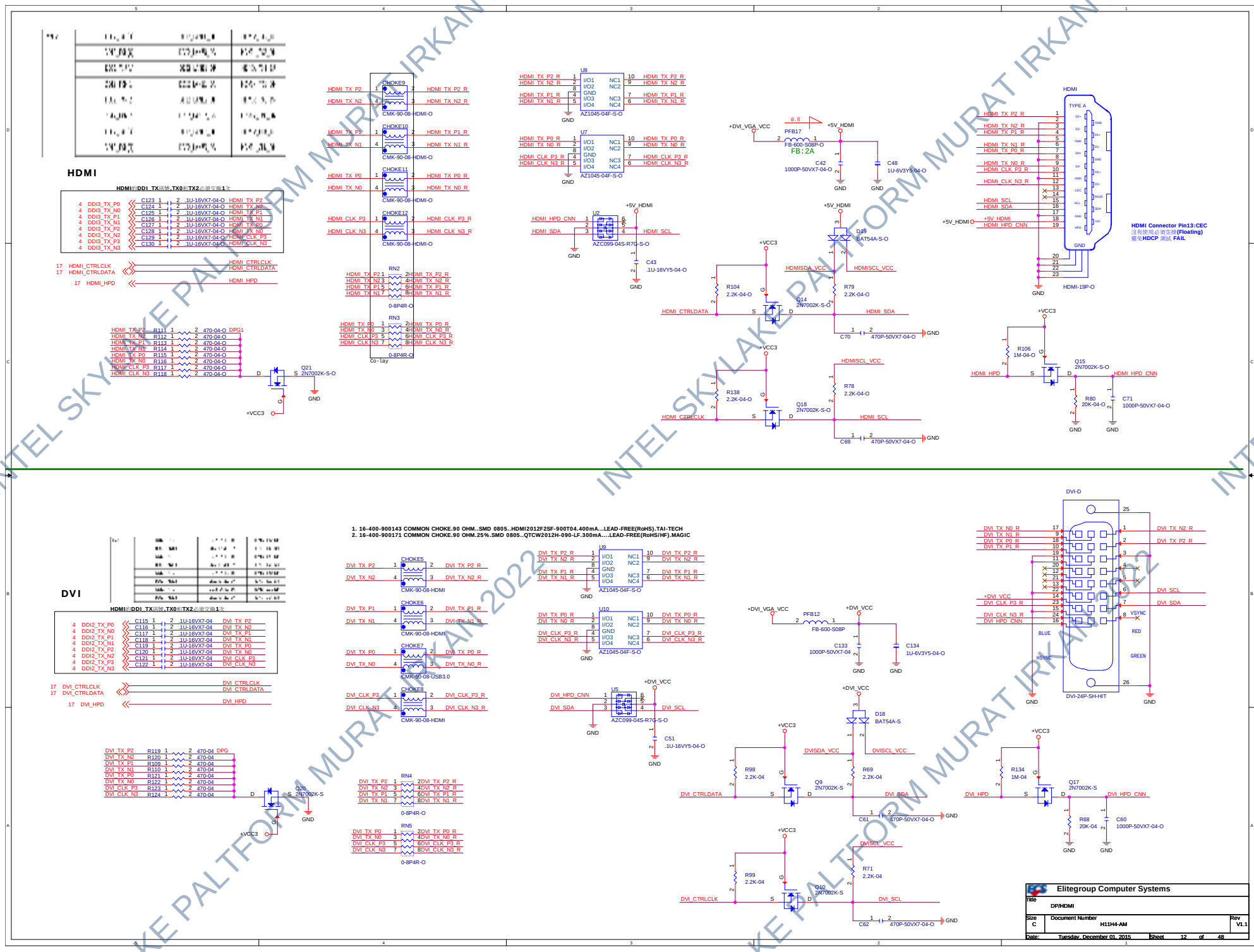

Power

+VCC3 L38 1 2 AVCC33
FB-60-04-B

+VCC3 L39 1 2 VDD_DAC_33
FB-60-04-B

Note: When connected to non-EDID monitor,
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.
XO Pin Pull High : Enable RTD2168 embedded EDID.

10,16,34,38 SMBDATA_MAIN
10,16,34,38 SMBCLK_MAIN

IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

RTD2168

U51

AVCC_12, AUX_P, AUX_N, RRX, LANE0P, LANE0N, LANE1P, LANE1N, EPAD_GND
AVCC_33, POL2_SCL, POL1_SDA, LDO_EN, DVCC_33, VCCK_12, XO, XI/CKIN
RED_N, RED_P, GND_DAC, GREEN_N, GREEN_P, BLUE_N, BLUE_P, VDD_DAC_33
HPD, SMB_SCL, SMB_SDA, VGA_SCL, DVCC_33, VGA_SDA, VSYNC, HSYNC

DDI1_AUX_P, DDI1_AUX_N, DDI1_TX_P0, DDI1_TX_N0, DDI1_TX_P1, DDI1_TX_N1
DP_AUX_P, DP_AUX_N, DP_TX_P0, DP_TX_N0, DP_TX_P1, DP_TX_N1

VGA_RED, VGA_GREEN, VGA_BLUE
DPVGA_HPD, SMBCLK_MAIN, SMBDATA_MAIN, DPVGA_DDCCLK, DPVGA_DDCSDA, VGA_VSYNC, VGA_HSYNC

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.

R812 4.7K-04 POL2_SCL
R813 4.7K-04 POL1_SDA

DPVGA_DDCCLK R132 VGA_DDCCLK_CNN
DPVGA_DDCSDA R136 VGA_DDCSDA_CNN

VGA_VSYNC
VGA_HSYNC

Elitegroup Computer Systems			
Title: DP to VGA(RTD2168)			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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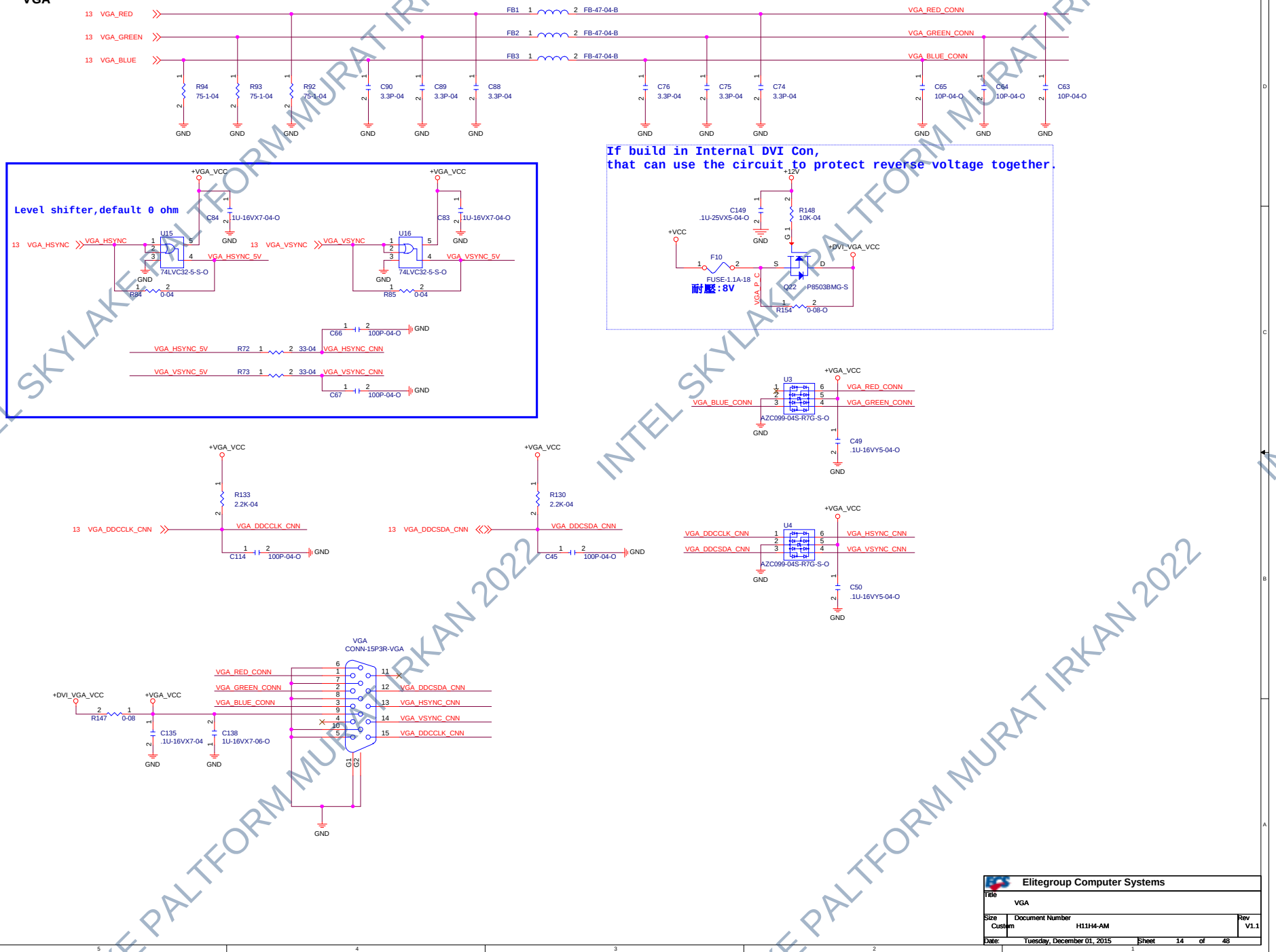
VGA



Elitegroup Computer Systems		
Title: VGA		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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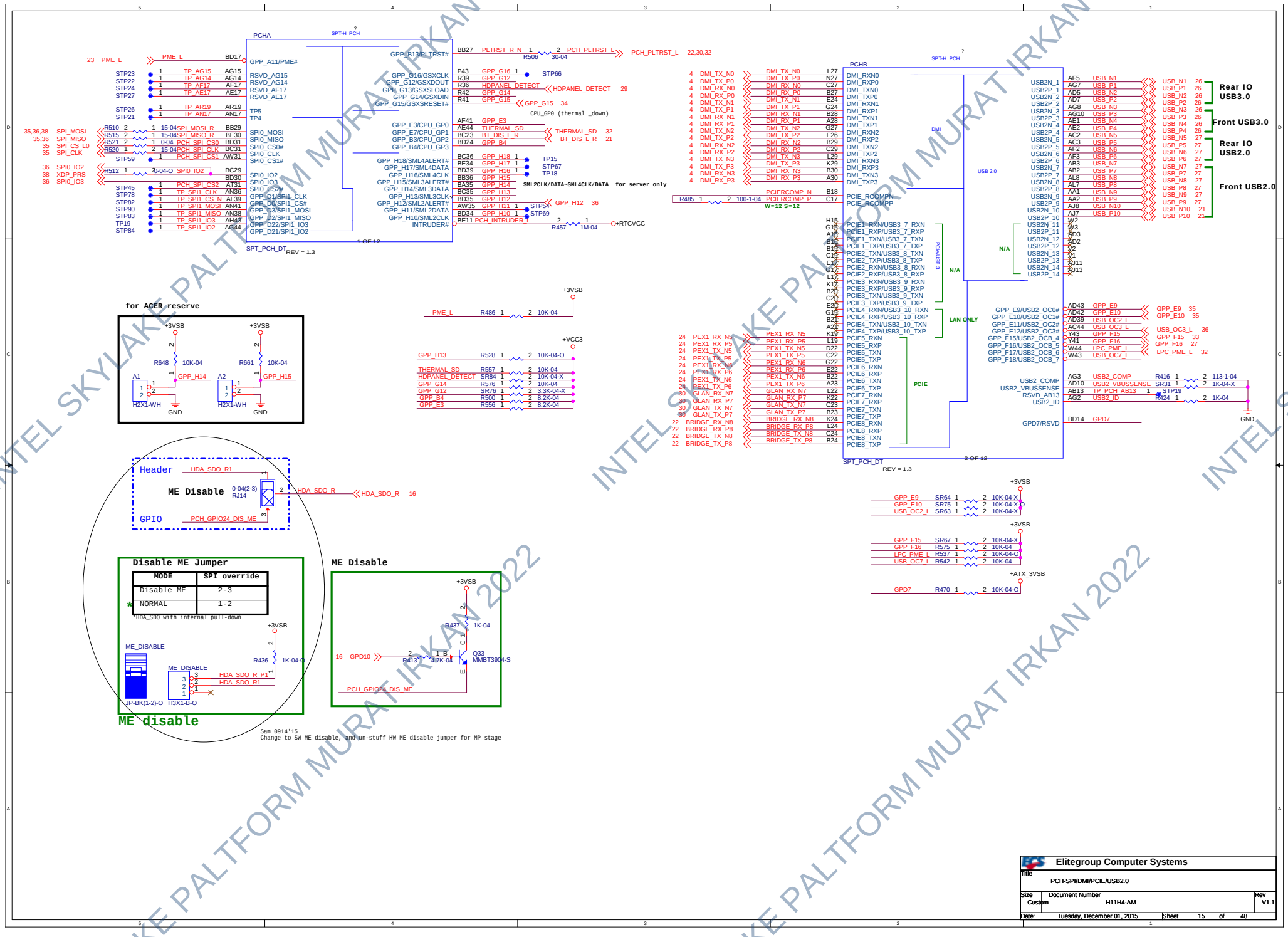

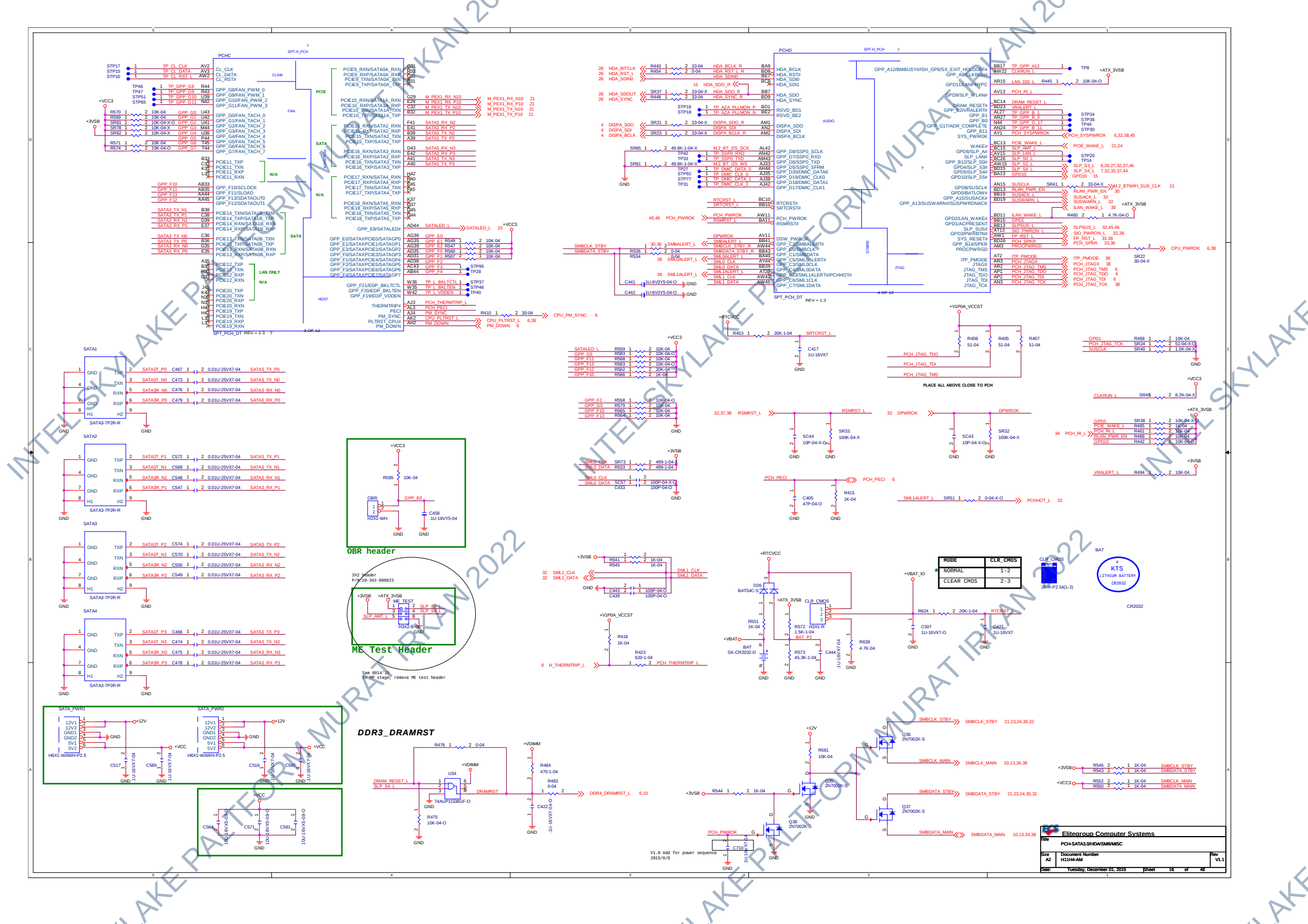

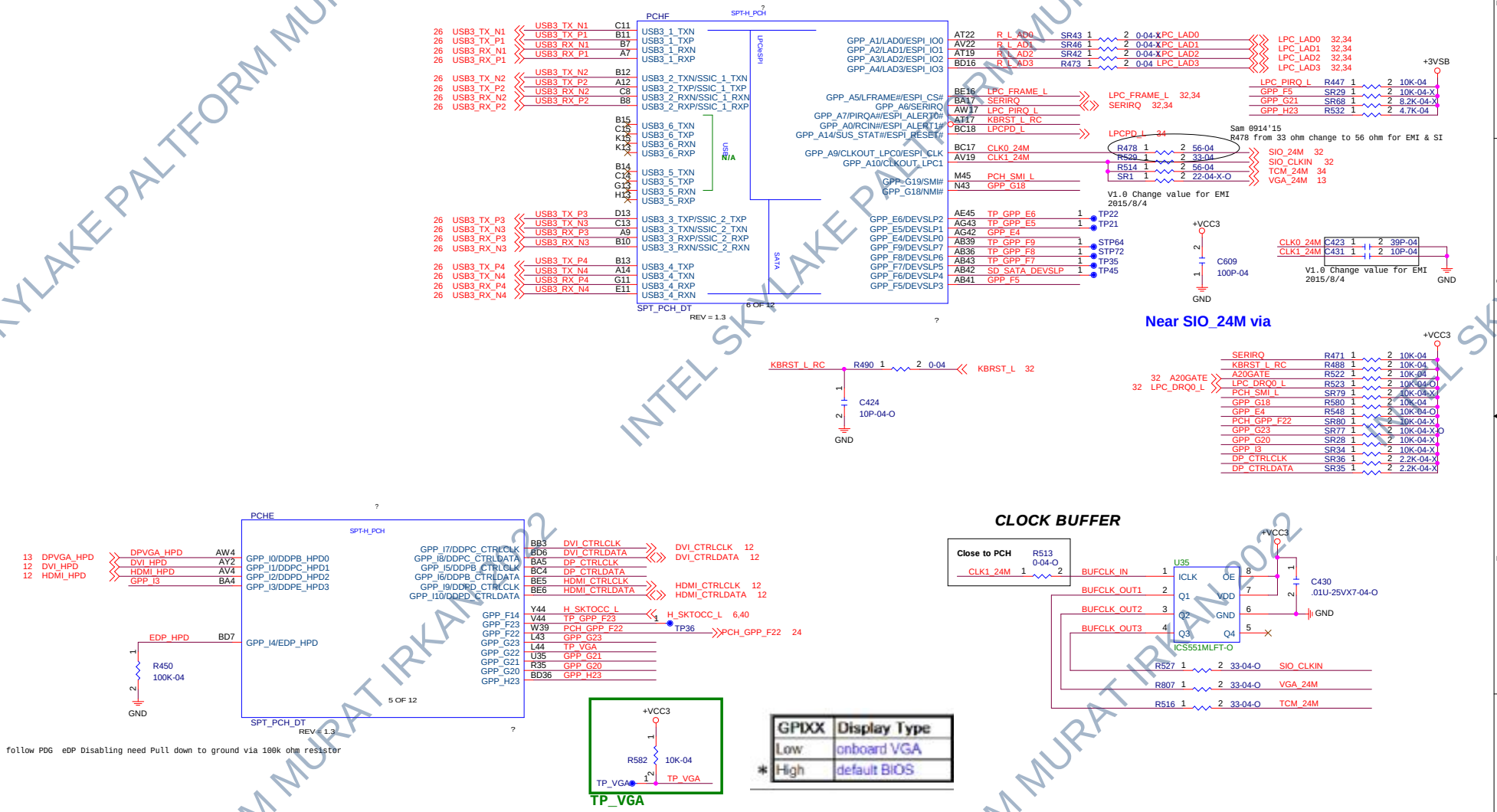

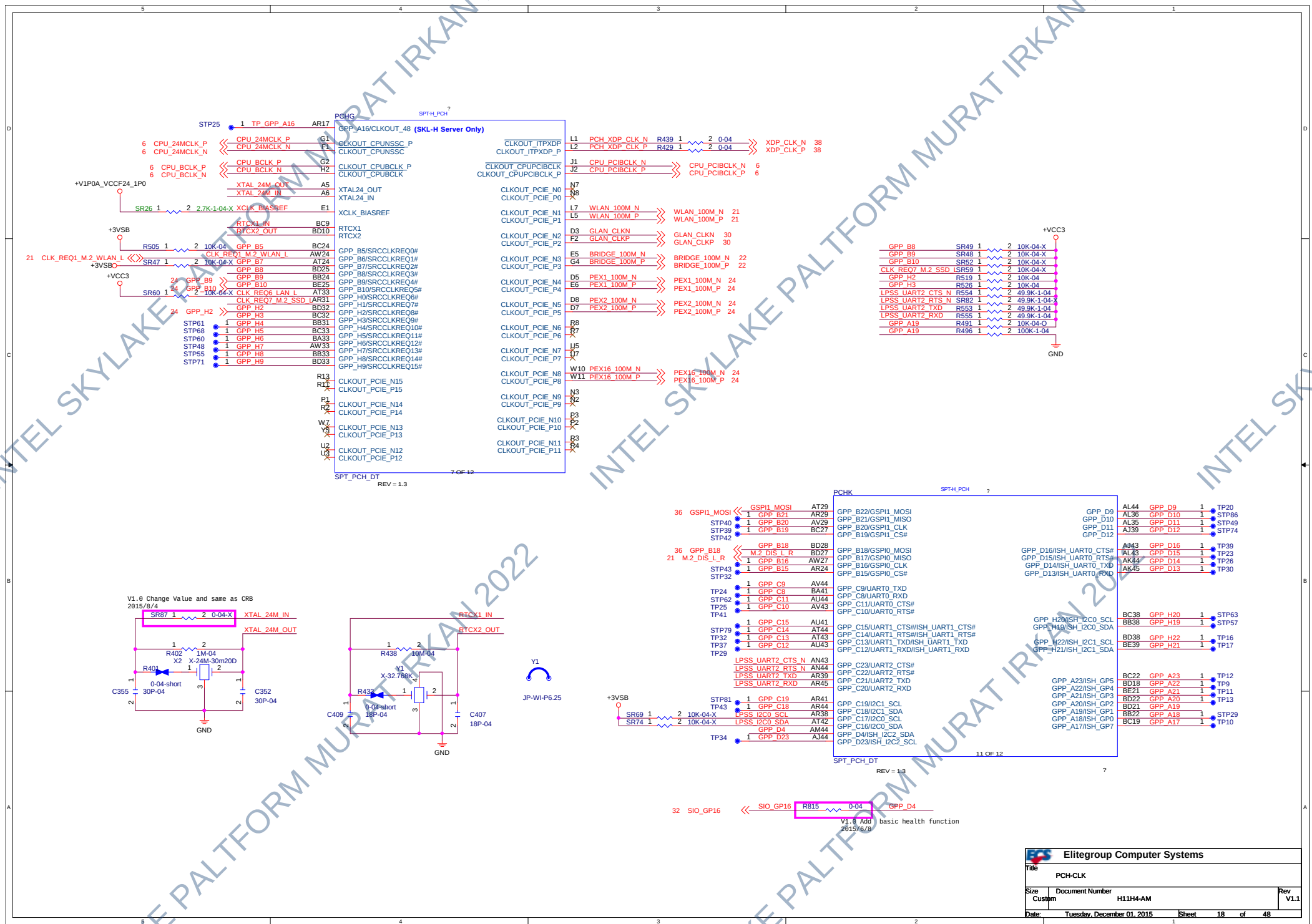
PCHG
SPT-H_PCH
GPP_A16/CLKOUT_48 (SKL-H Server Only)
SPT_PCH_DT
REV = 1.3
7 OF 12
PCHK
SPT-H_PCH
SPT_PCH_DT
REV = 1.3
11 OF 12
V1.0 Change Value and same as CRB
2015/8/4
V1.0 Add basic health function
2015/6/8
GND
JP-WI-P6.25
Elitegroup Computer Systems
PCH-CLK
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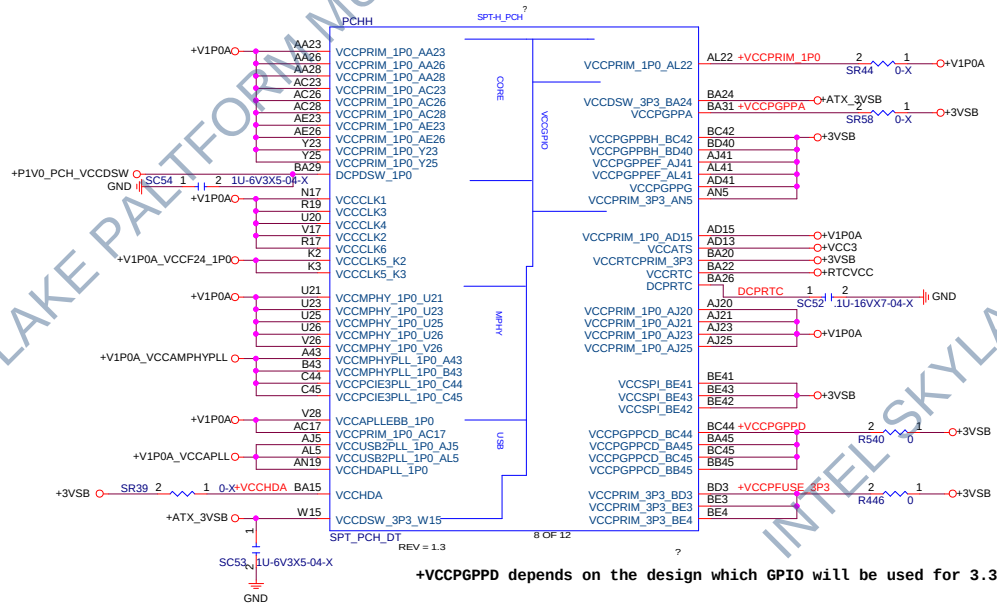
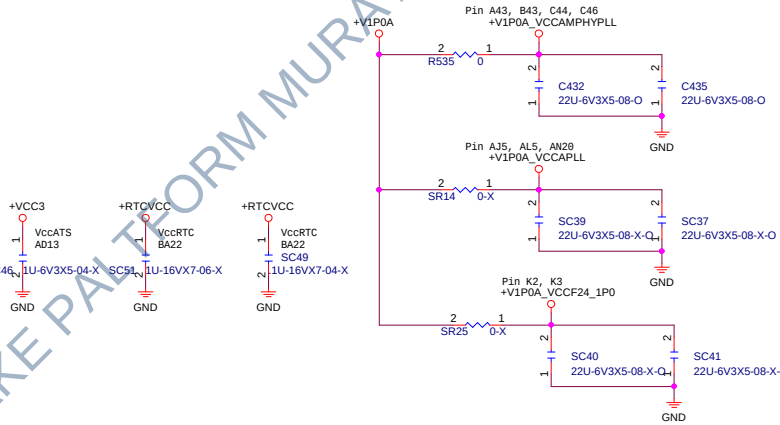
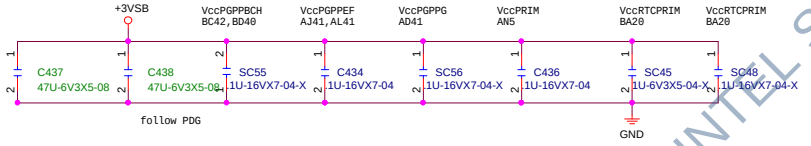
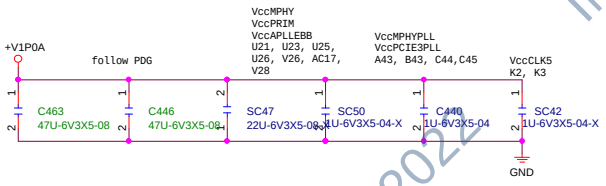
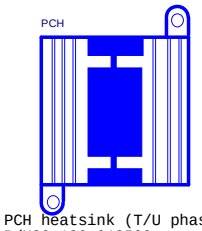


+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.



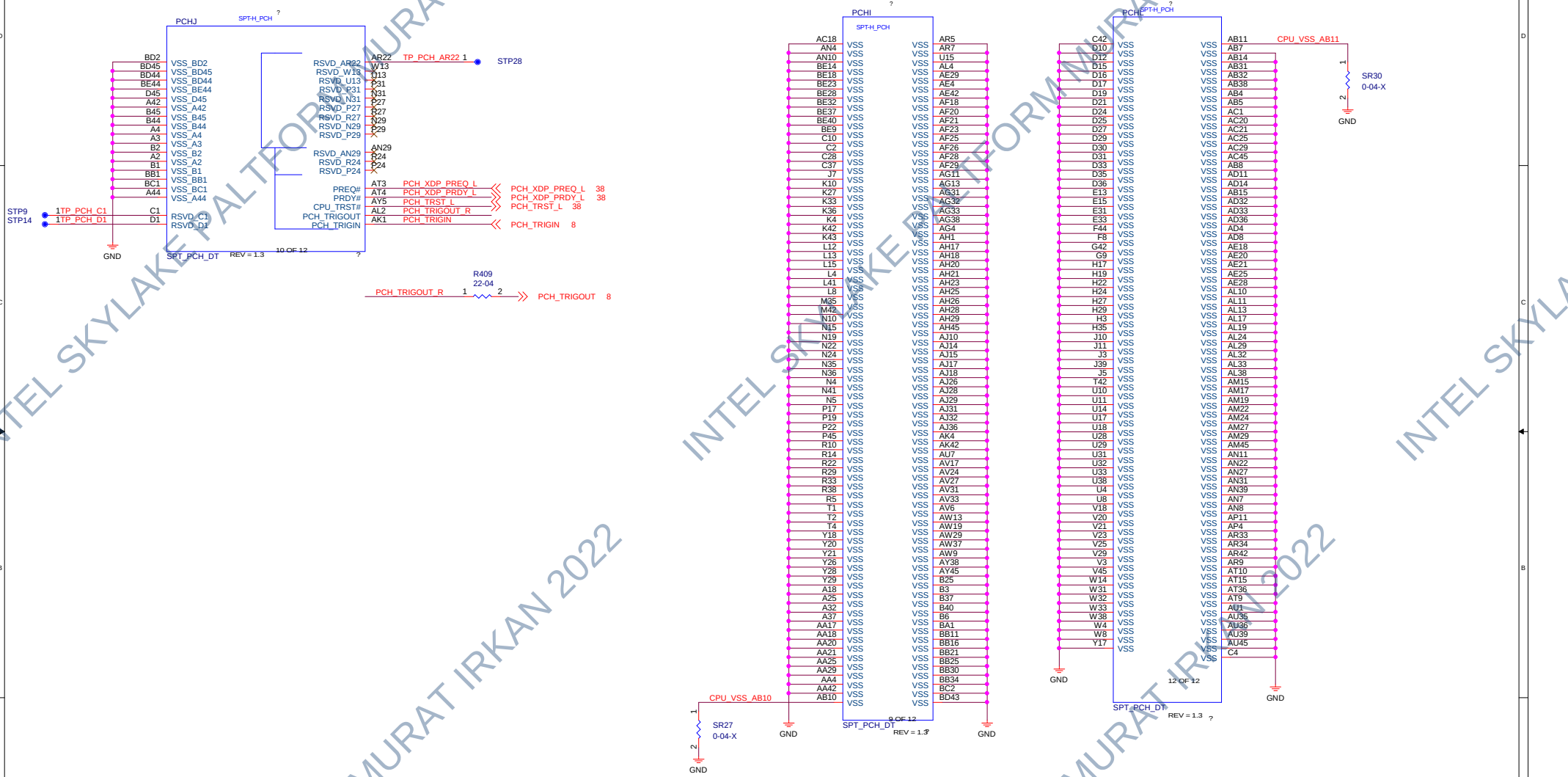






PCH heatsink (T/U phase)
P/N20-120-013580
20-120-013581
V1.0 Change
2015/6/8

Elitegroup Computer Systems			
Title: PCH-PWR			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 19 of 48		



Elitegroup Computer Systems		
Title: PCH-GND		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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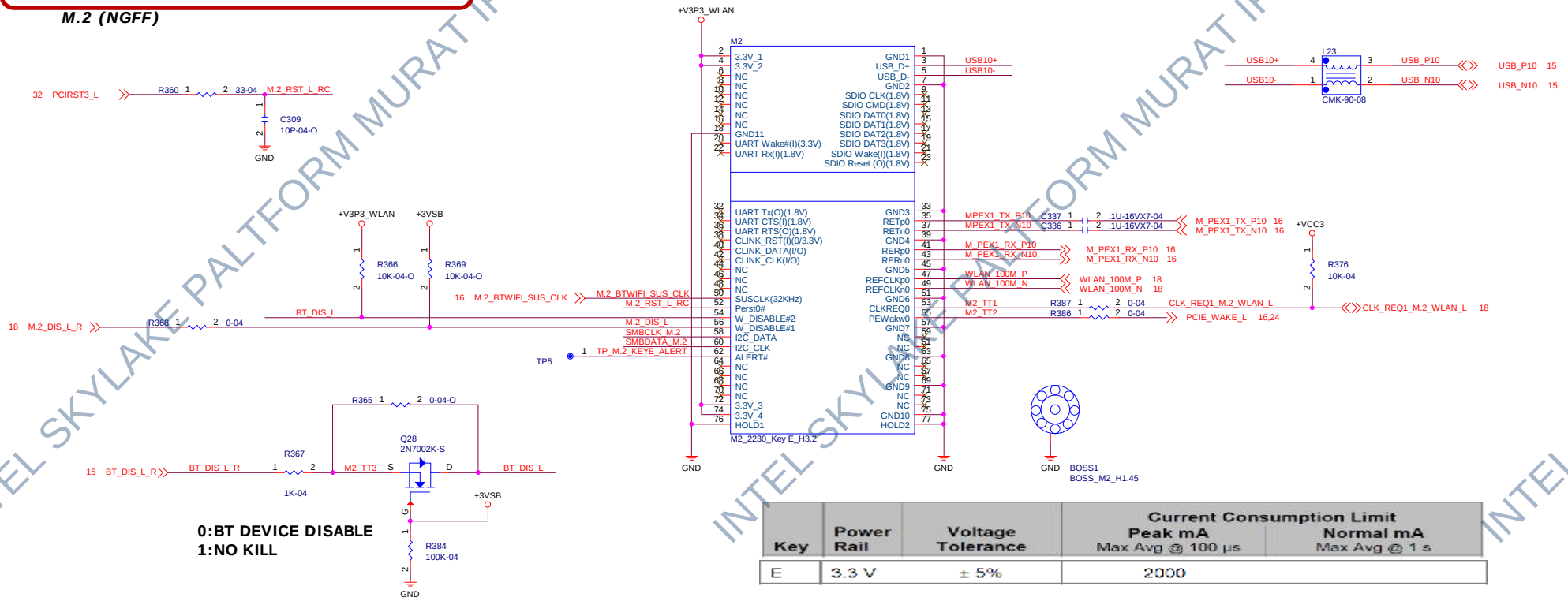
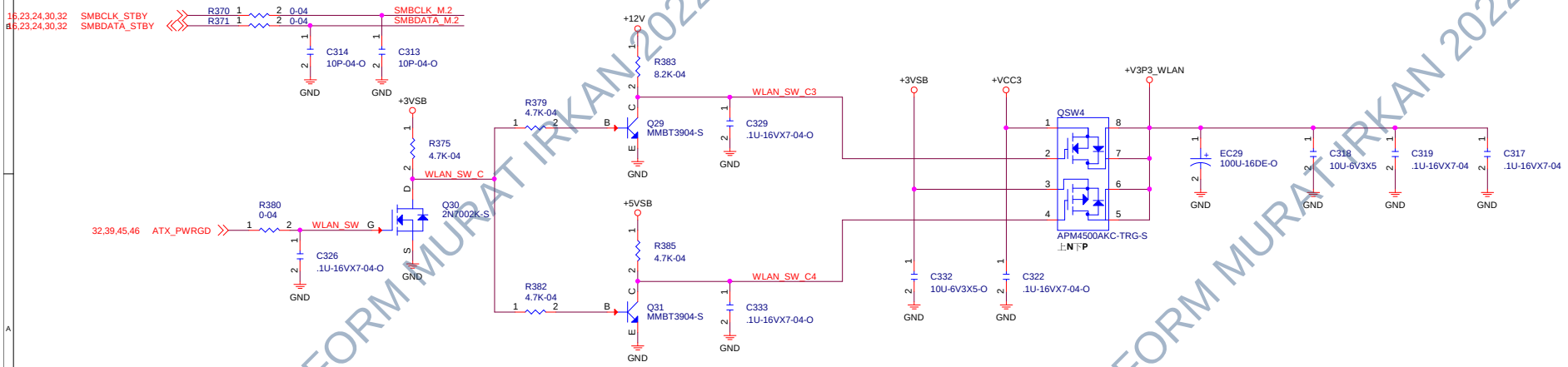
INTEL LGA1151 SOKET M.2 SSD DISK

M.2 (NGFF)



0:BT DEVICE DISABLE
1:NO KILL

Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak mA Max Avg @ 100 µs	Normal mA Max Avg @ 1 s
E	3.3 V	± 5%	2000	



	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB

Elitegroup Computer Systems	
Title	M.2 Slot
Size: Custom	Document Number: H11H4-AM
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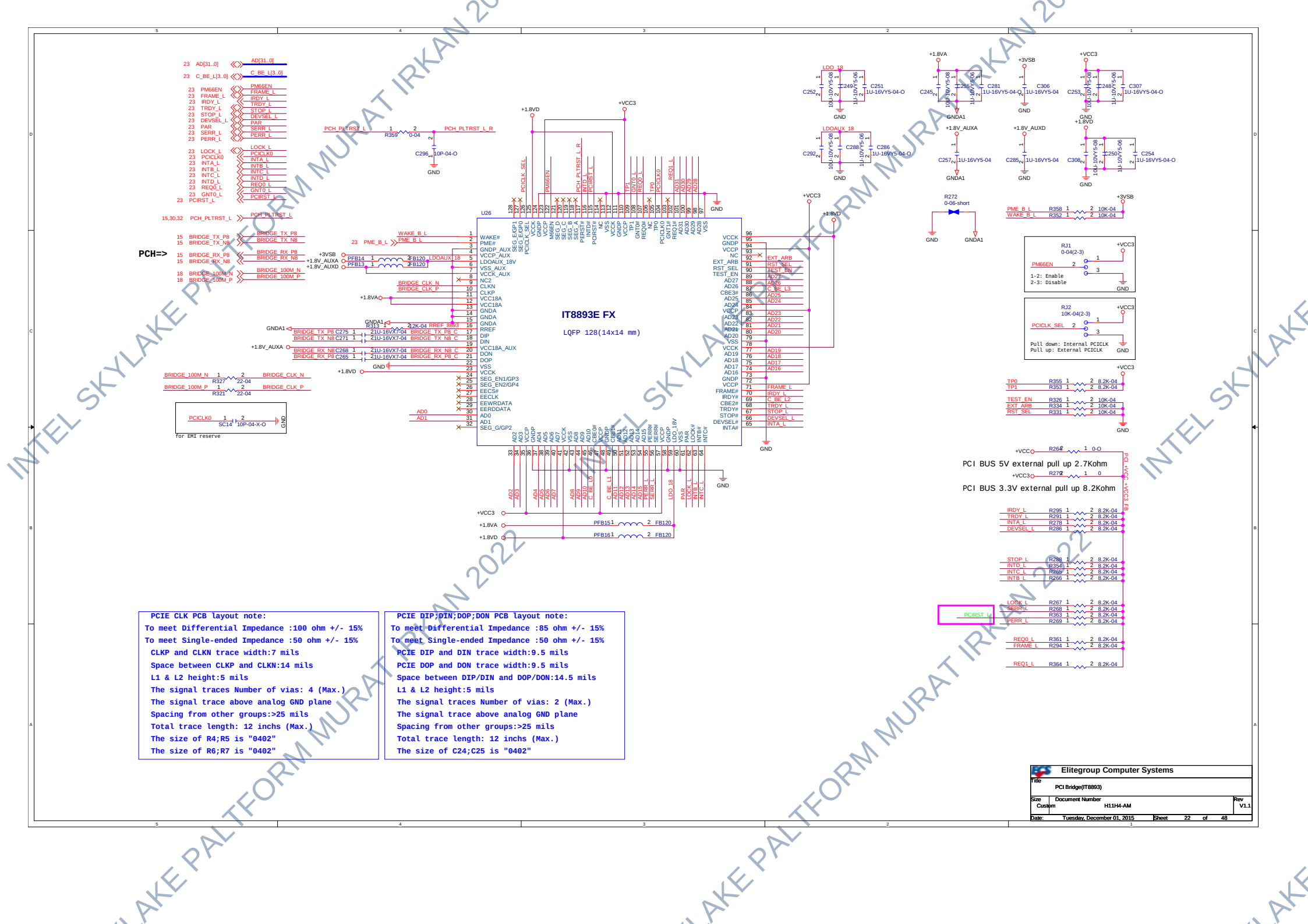

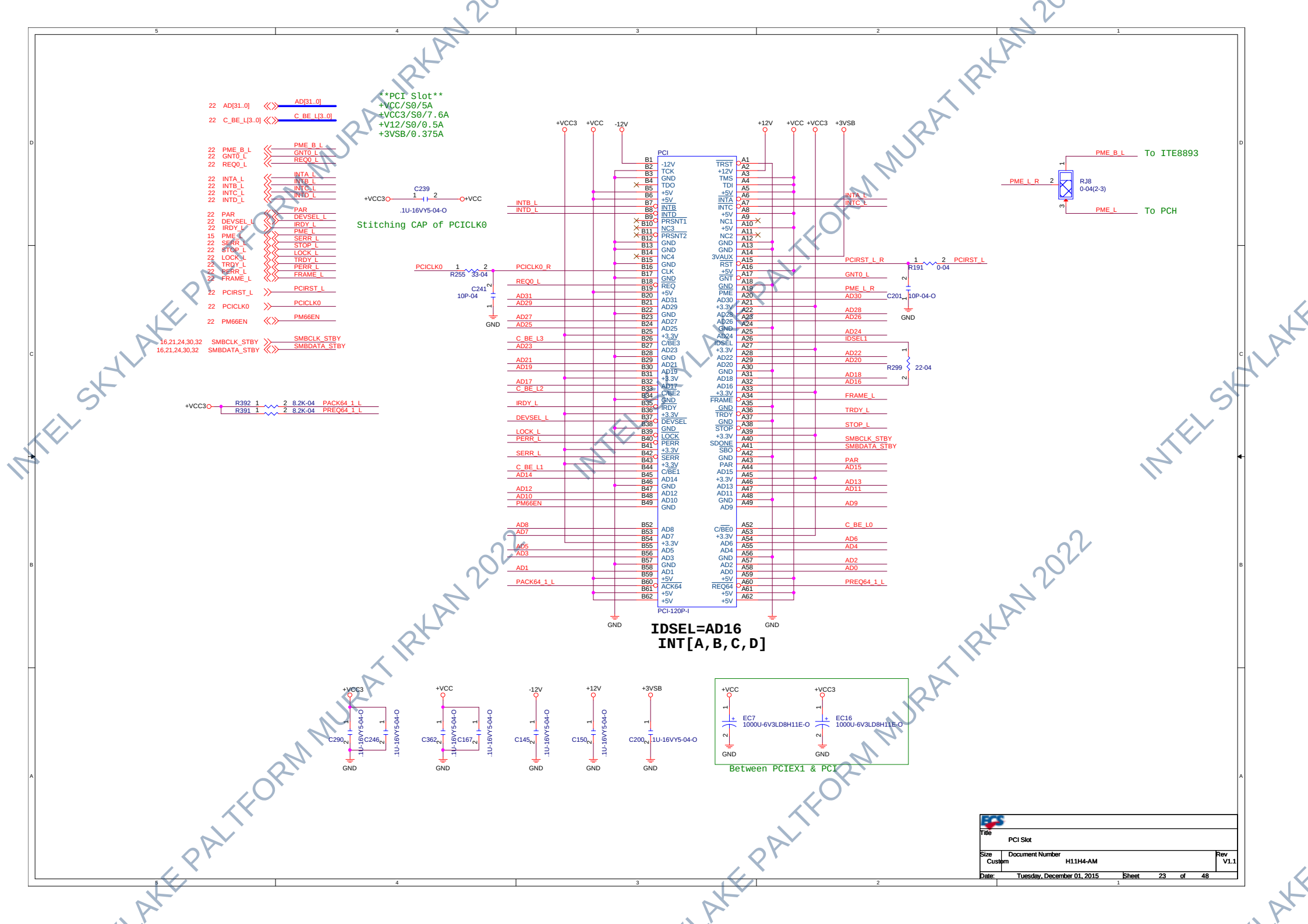

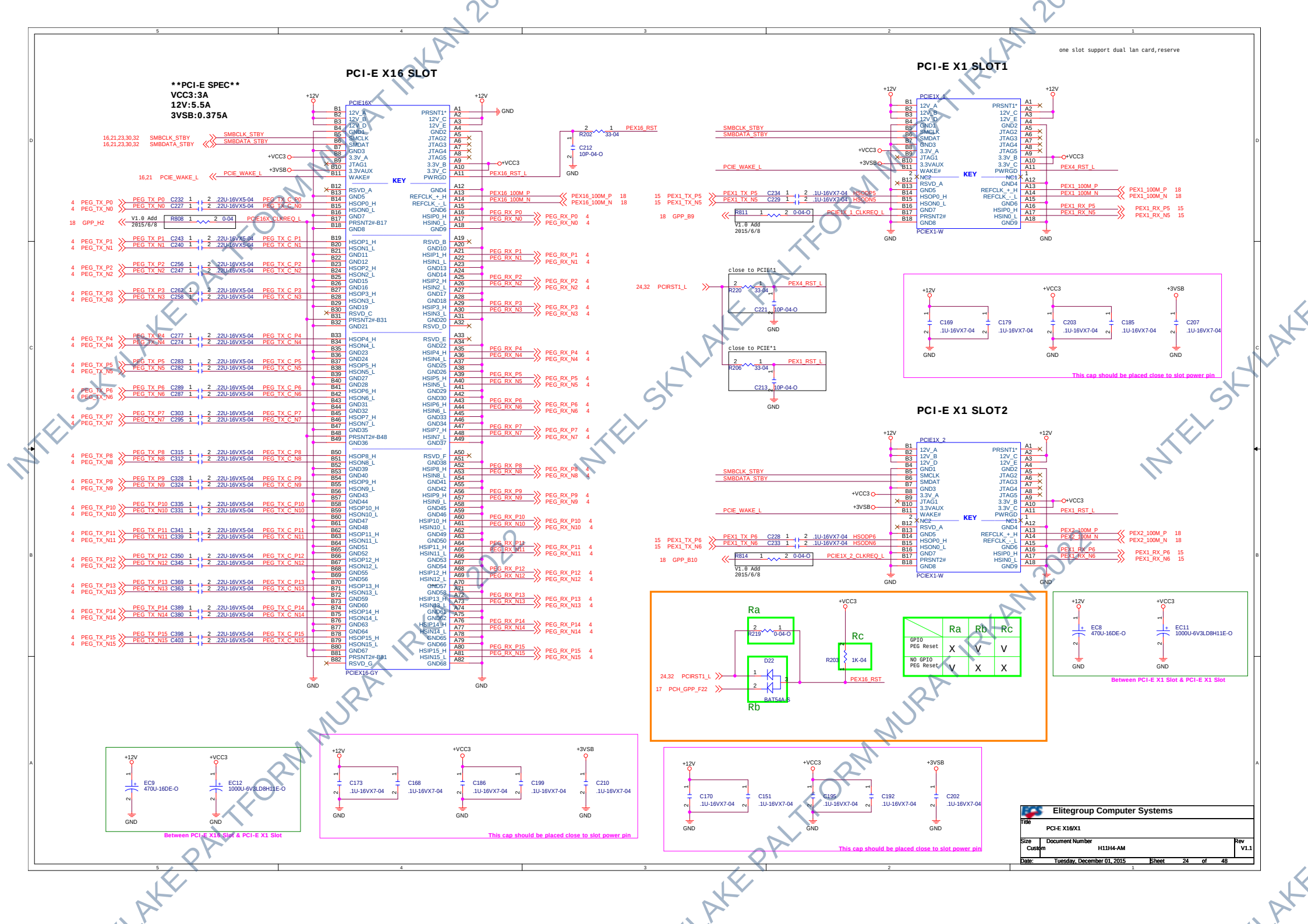
PCI-E X16 SLOT
PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A
PCIE16X
PCIEX16-GY
KEY
PCI-E X1 SLOT1
PCIE1X_1
PCIEX1-W
PCI-E X1 SLOT2
PCIE1X_2
one slot support dual lan card,reserve
close to PCIE*1
Ra
Rb
Rc
GPIO PEG Reset
NO GPIO PEG Reset
Between PCI-E X16 Slot & PCI-E X1 Slot
Between PCI-E X1 Slot & PCI-E X1 Slot
This cap should be placed close to slot power pin
Elitegroup Computer Systems
PCI-E X16/X1
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Title	Reserved		
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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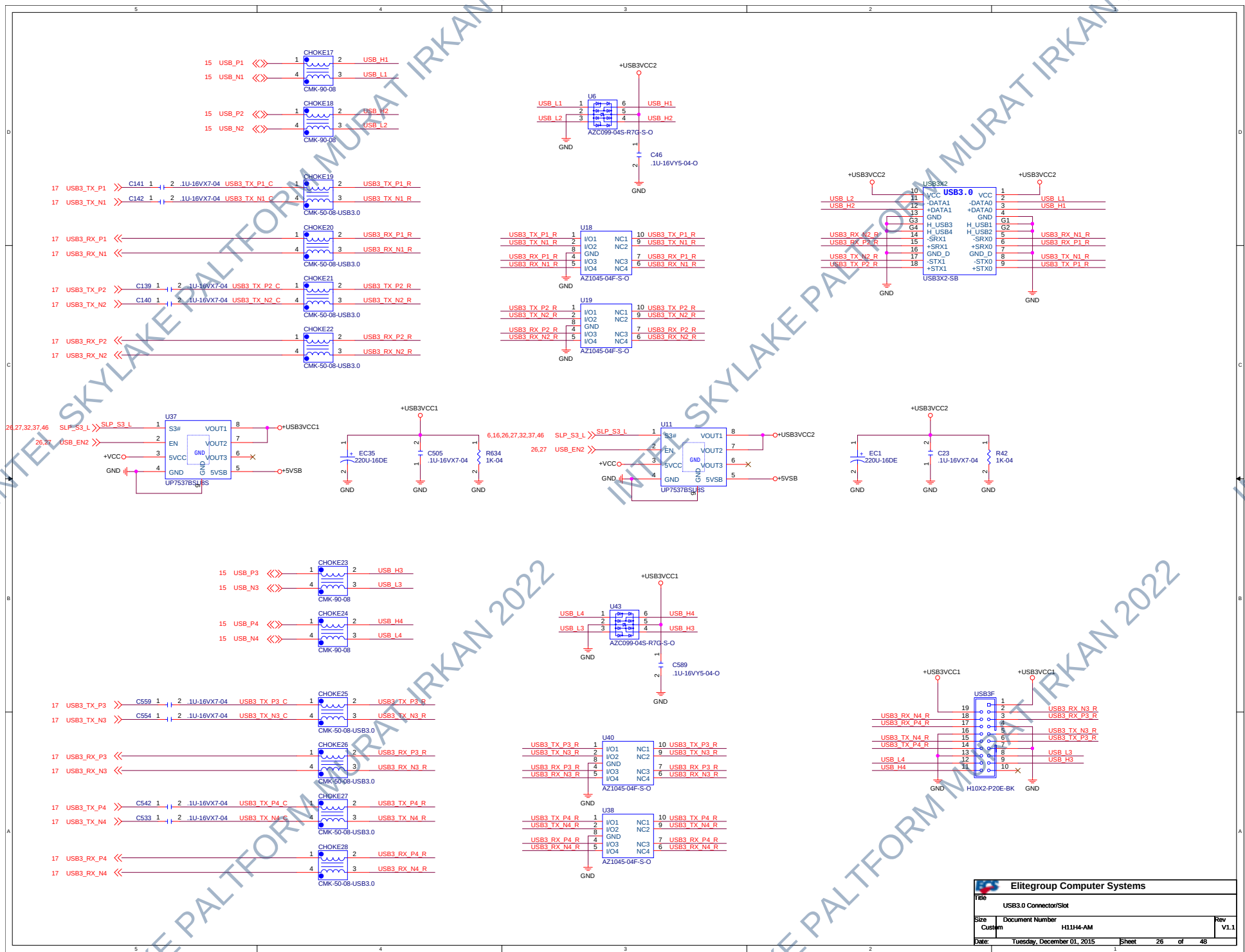
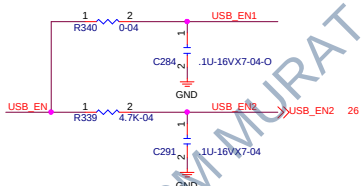
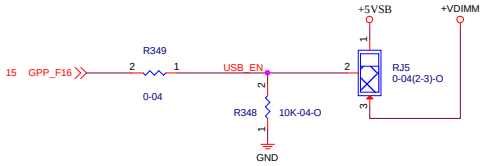
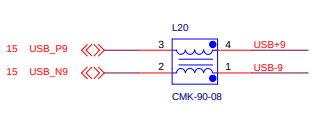
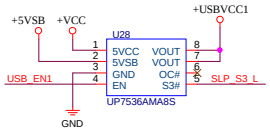


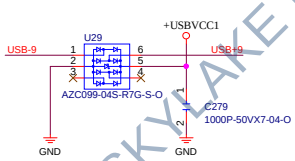


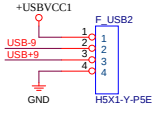


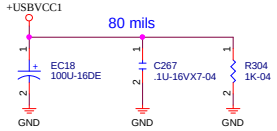
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

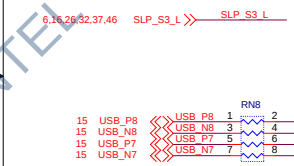


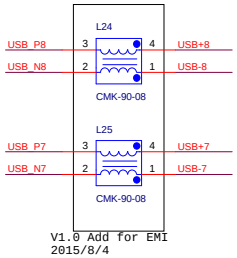


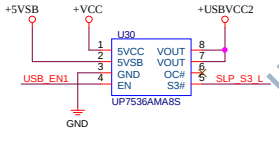


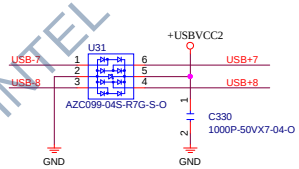


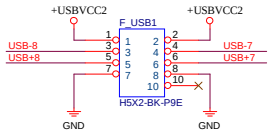


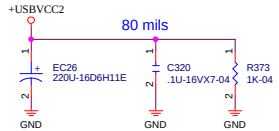






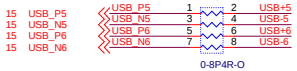


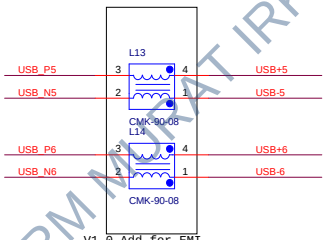


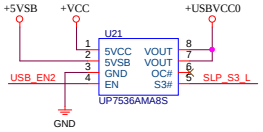


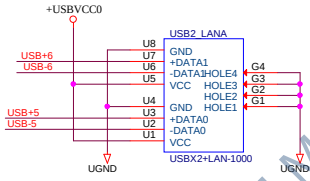
USB2.0 header

USB2.0 connecter

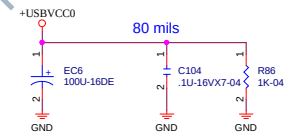


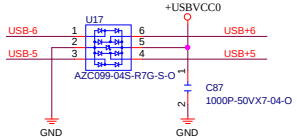






Lan + USB2.0





Elitegroup Computer Systems	
Title	USB2.0 Connector/Header
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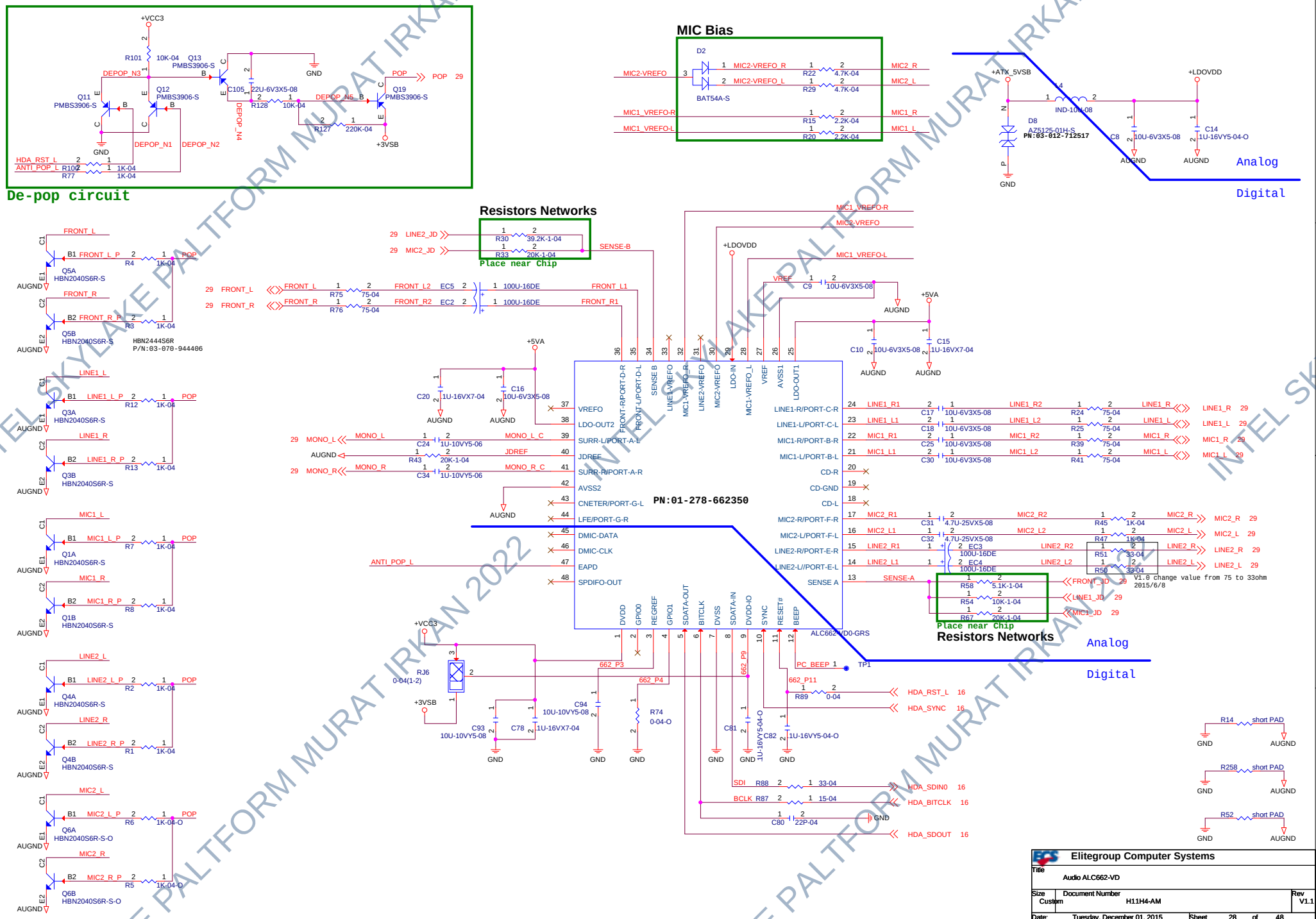
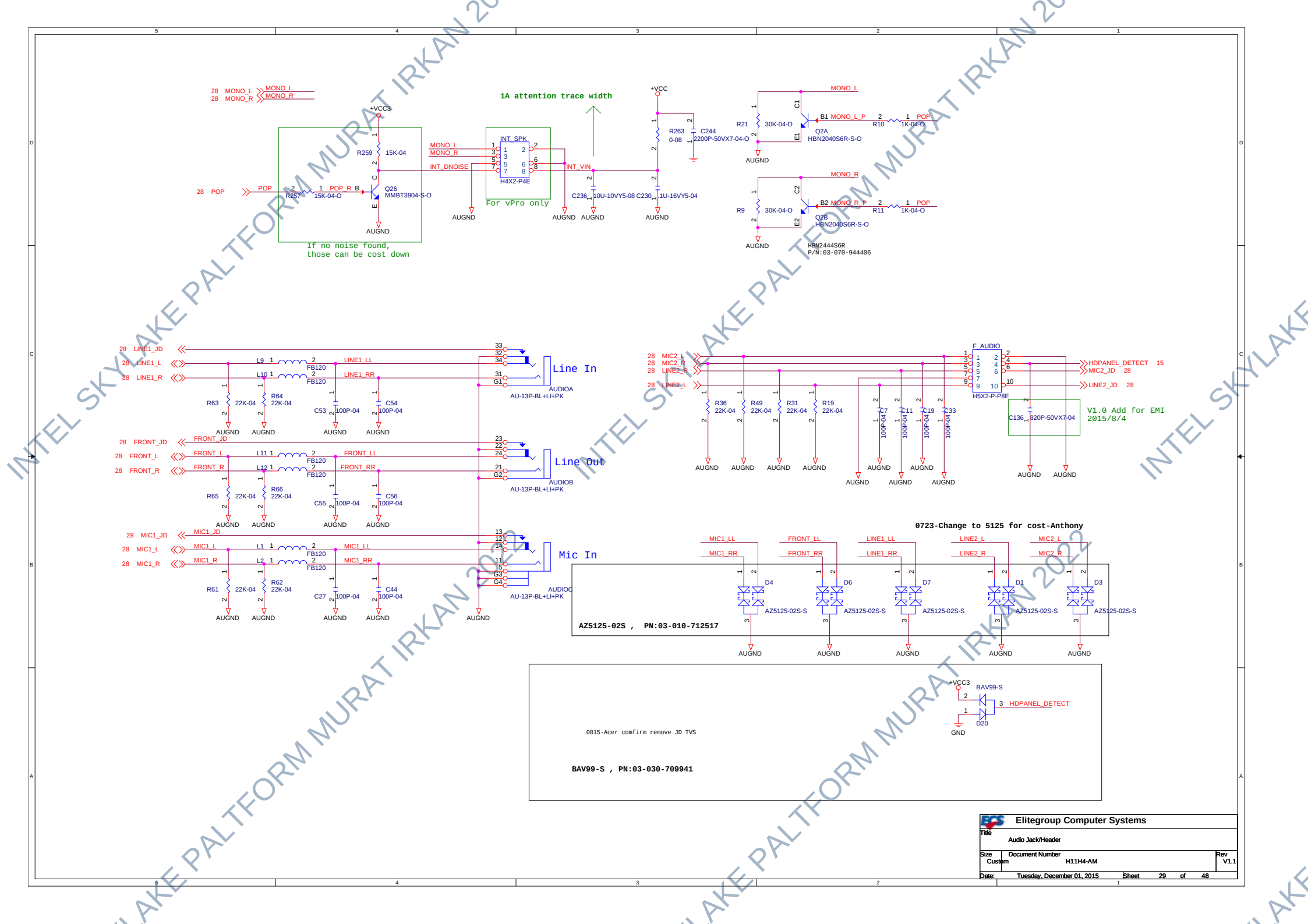
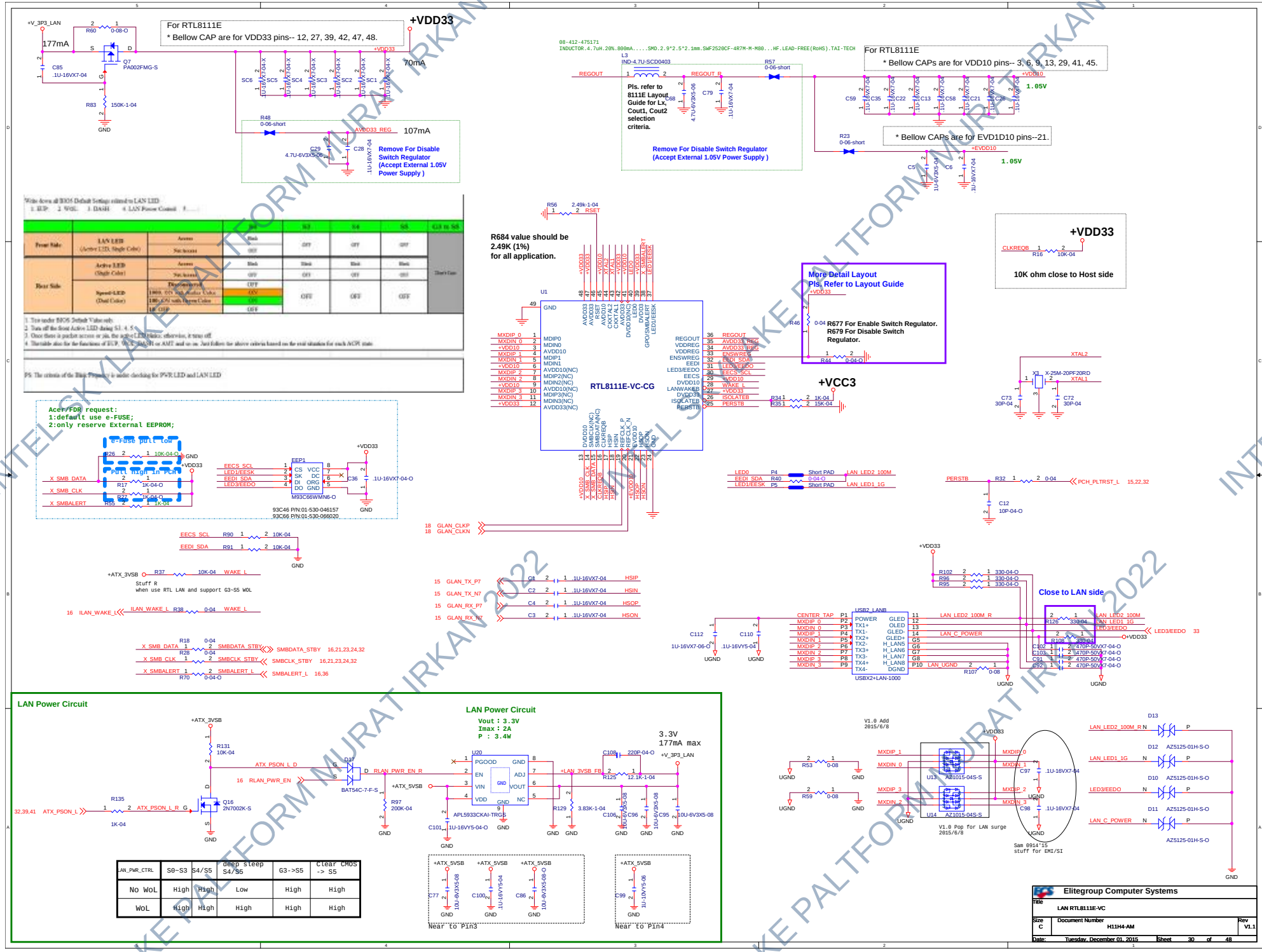
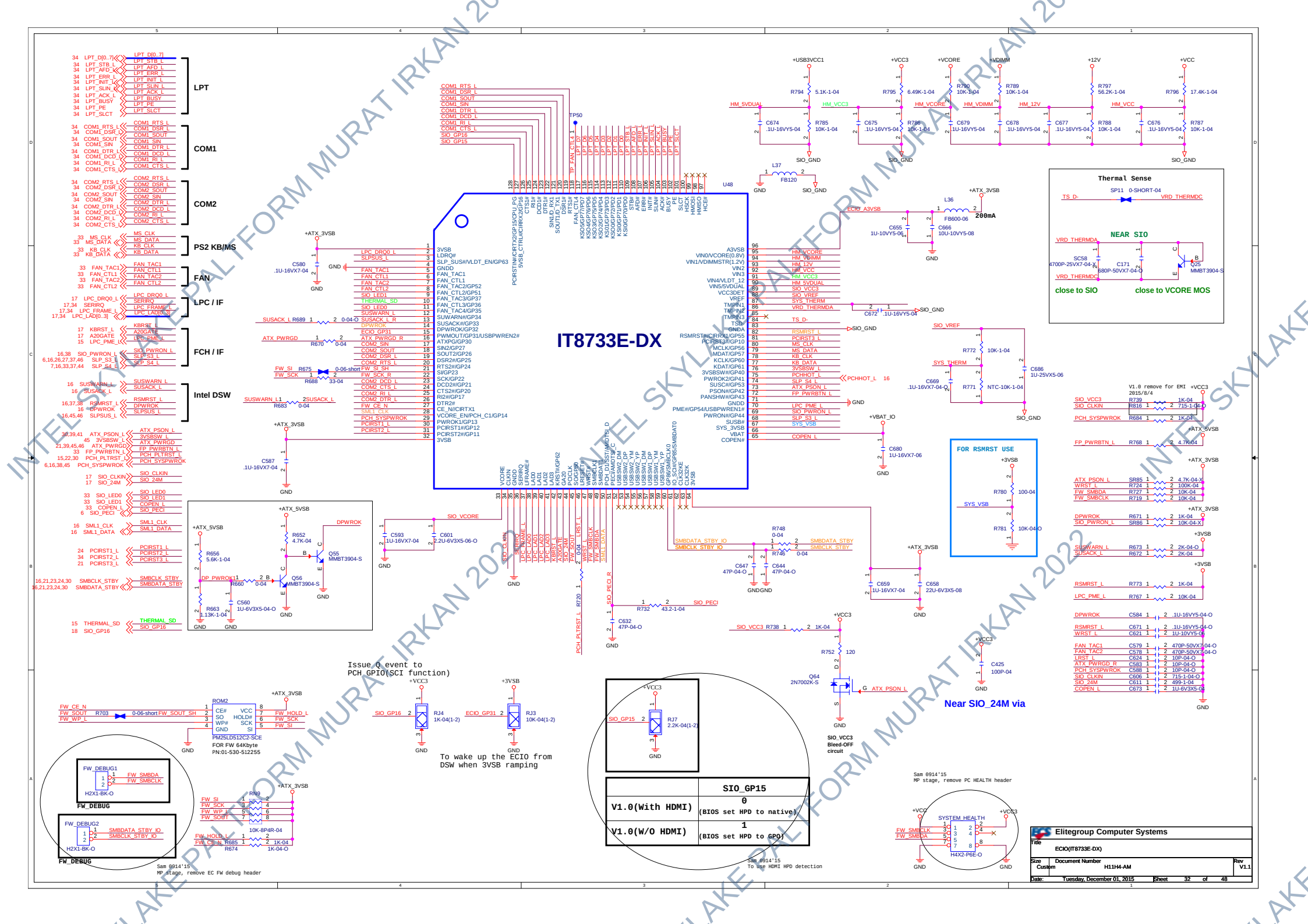

De-pop circuit
MIC Bias
Resistors Networks
Place near Chip
Analog
Digital
PN:01-278-662350
ALC662-VD0-GRS
Elitegroup Computer Systems
Audio ALC662-VD
H11H4-AM
V1.1
Tuesday, December 01, 2015
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022





Elitegroup Computer Systems			
Title: Reserved			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 31 of 48		


IT8733E-DX
LPT
COM1
COM2
PS2 KB/MS
FAN
LPC / IF
FCH / IF
Intel DSW
U48
TP50
Thermal Sense
NEAR SIO
close to SIO
close to VCORE MOS
FOR RSMRST USE
Near SIO_24M via
Issue Q event to
PCH_GPIO(SCI function)
To wake up the ECIO from
DSW when 3VSB ramping
SIO_VCC3
Bleed-OFF
circuit
FW_DEBUG
FW_DEBUG
ROM2
PM25LD512C2-SCE
FOR FW 64Kbyte
PN:01-530-512255
Sam 0914'15
MP stage, remove EC FW debug header
Sam 0914'15
To use HDMI HPD detection
Sam 0914'15
MP stage, remove PC HEALTH header
V1.0 remove for EMI
2015/8/4
SIO_GP15
V1.0(With HDMI) 0 (BIOS set HPD to native)
V1.0(W/O HDMI) 1 (BIOS set HPD to GPO)
Elitegroup Computer Systems
ECIO(IT8733E-DX)
H11H4-AM
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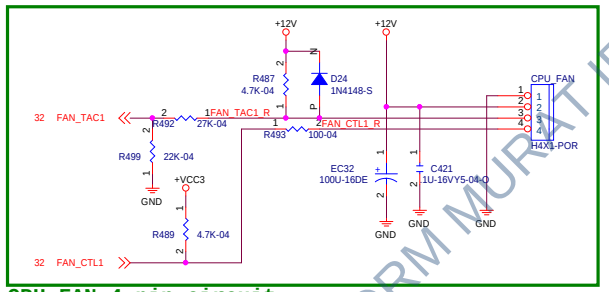
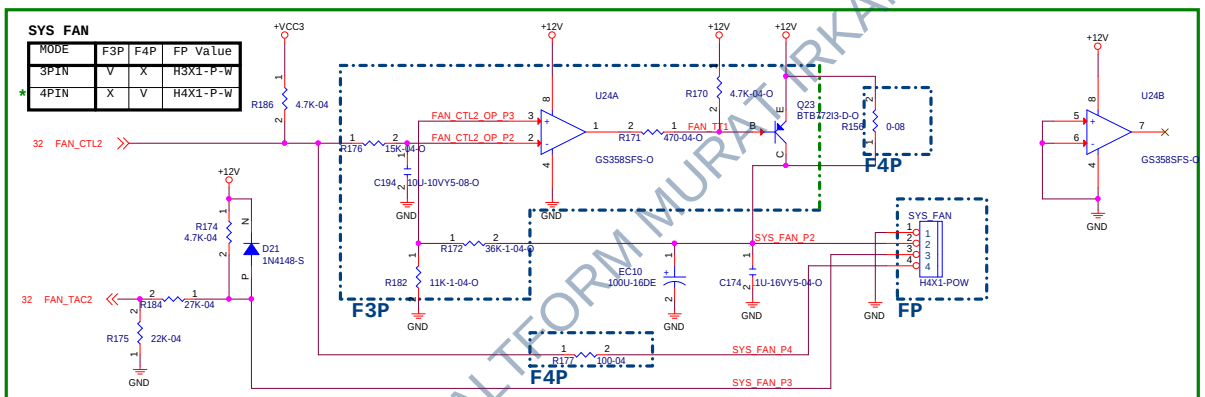


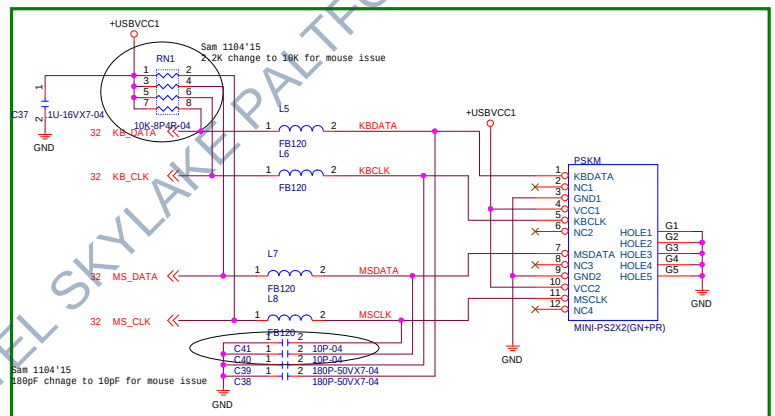
CPU_FAN 4 pin circuit

SYS FAN

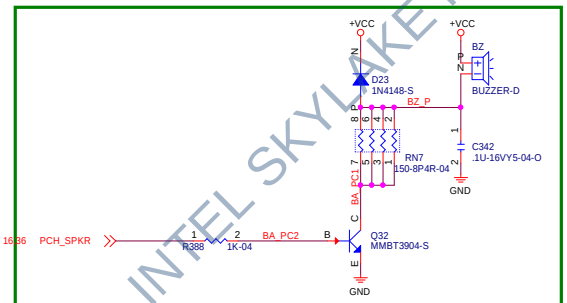
MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
* 4PIN	X	V	H4X1-P-W



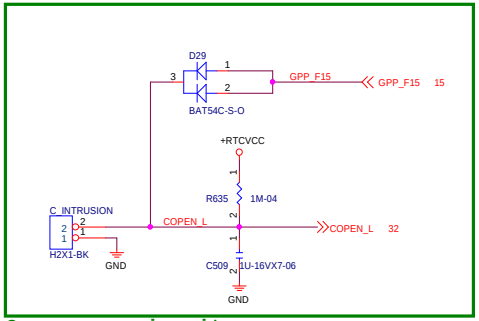
SYS_FAN 3/4 pin co-layout circuit



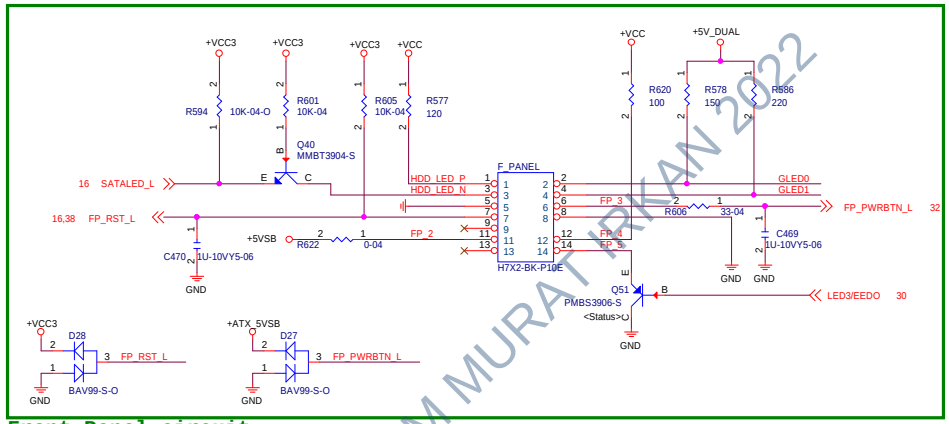
PS2 circuit



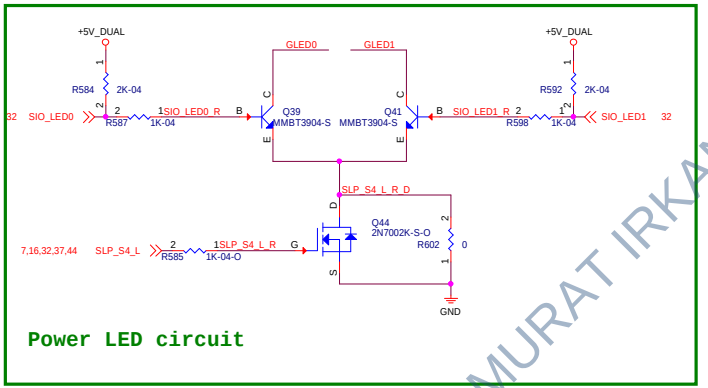
Buzzer circuit



Case open circuit



Front Panel circuit



Power LED circuit

Elitegroup Computer Systems			
Title: FAN/Buzzer/PS2/Front Panel			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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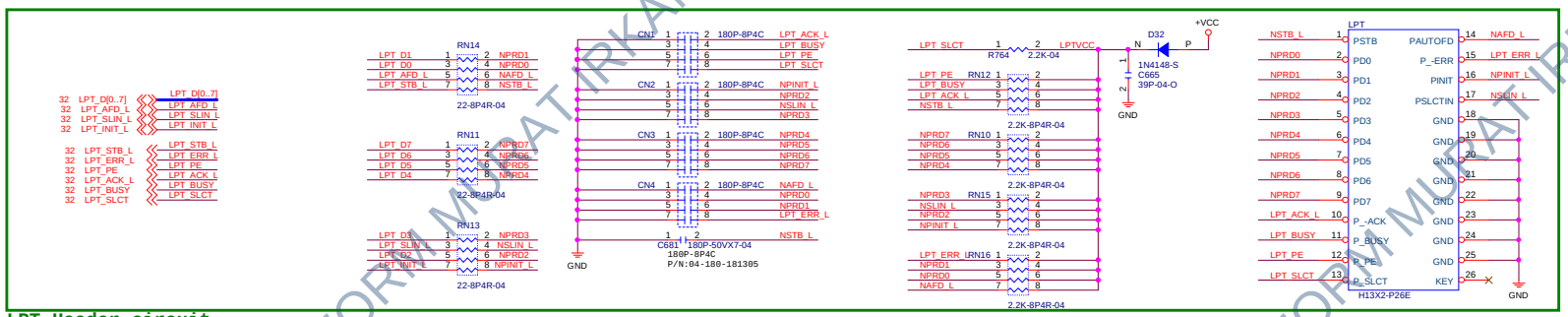

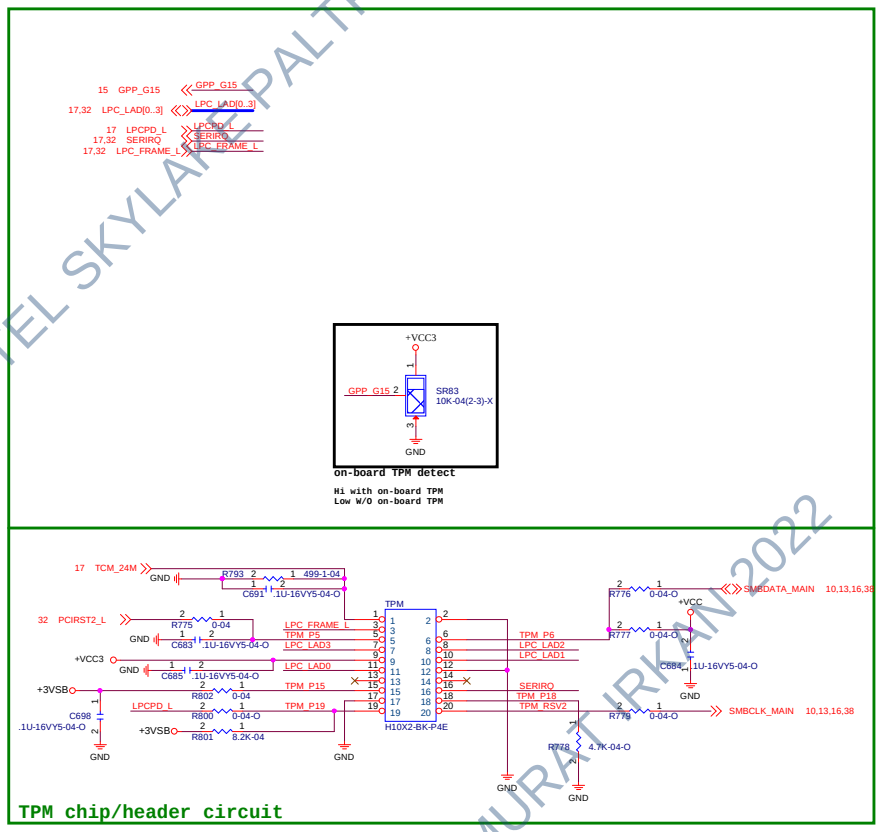

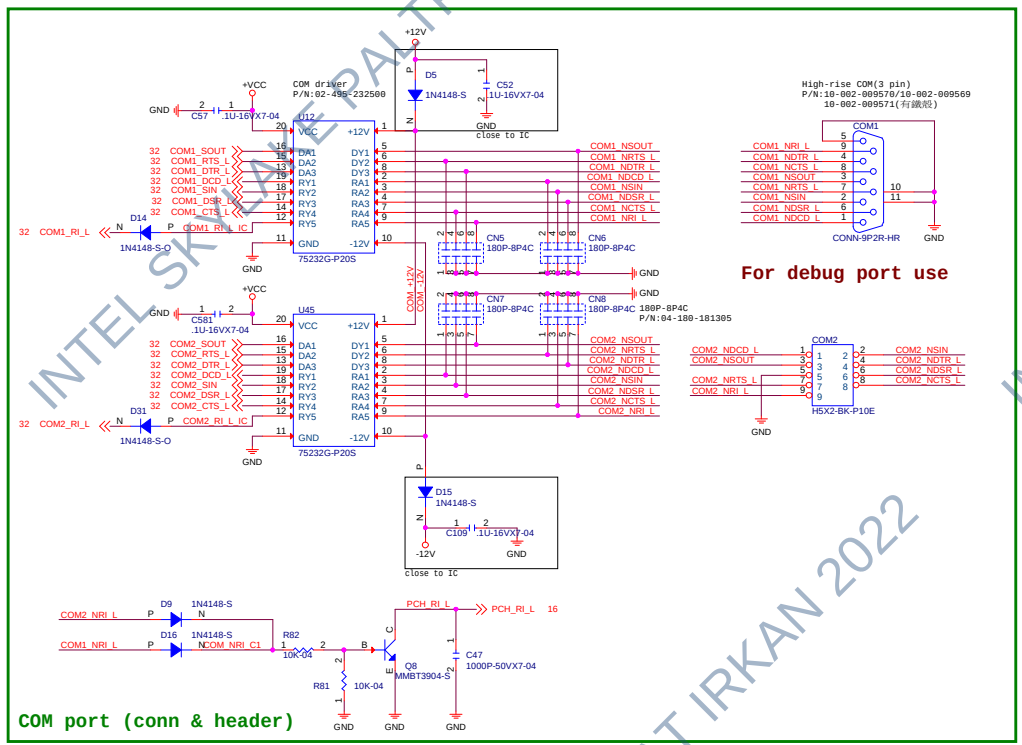

Elitegroup Computer Systems		
Title: TPM/TCM/LPT/COM/Asset ID		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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15,36,38 SPI_MOSI
15,36 SPI_MISO
SPI_MOSI R474 2 1 0-04 SPI_MOSI0
SPI_MISO R451 2 1 0-04 SPI_MISO0

15 SPI_CLK
SPI_CLK R455 2 1 0-04 SPI_CLK0

15 SPI_CS_L0
SPI_CS_L0 1 2 ROM_CS_L0
R463 0-04
Re

Sam 0914'15
In MP stage, remove SPI debug header

SPI_MOSI0 C419 1 2 12P-04-O GND
SPI_MISO0 C418 1 2 12P-04-O
ROM_CS_L0 C414 1 2 12P-04-O
C420 12P-04-O

SPIROM1
ROM_CS_L0 1 CS# VCC 8
SPI_MISO0 2 SO HOLD# 7
SPI_IO2_0 3 WP# SCK 6
4 GND SI 5
SPI-64M-WINBOND
GND
+SPI_3P3V
SPI_IO3_0
SPI_CLK0
SPI_MOSI0
C426 2 10U-10VY5-08 C427 2 1U-16VX7-04
GND GND
close
ROM1

+SPI_3P3V
SPI_IO3_0 R462 2 1 1K-04
SPI_IO2_0 R472 2 1 0-04 SPI_WP

+3VSB +SPI_3P3V
R501 short PAD
D25
1 3
2
BAT54C-S-O

A3 stuff BAT54C for debug and reserve 0 ohm
A4 0 ohm change to SH

SPI ROM

BIOS_WP JP-R(2-3)
BIOS_WP 1 2 3 H3X1-R
GPP_E9 15
GND

+SPI_3P3V
R495 10K-04
SPI_WP
R504 0-04
Q34 PMBS3906-S-O
B E C
<Status>
GPP_E10 15
GND

BIOS WP Jumper:

MODE	WP
BIOS WP	1-2
* NORMAL	2-3

BIOS WP

Sam 0914'15
In MP stage, remove SPI debug header

Ra
Rc
Rb
Rd
Re

SPI_MISO0 2 1 R456 0-04-O
SPI_DEBUG
ROM_CS_L0
SPI_CS_L0
SPI_MISO0_R
SPI_WP
+SPI_3P3V
SPI_IO3_0_R
SPI_CLK0
SPI_MOSI0_R
H6X2-BK-P2E-P1.27-O
GND
6*2 SMD header
PN:10-382-012820

2 1 R458 0-04-O SPI_IO3_0
2 1 R449 0-04-O SPI_MOSI0

SPI_DEBUG
JP-P1.27(1-3)-O
1.27mm jumper
PN:10-611-002144

	Ra	Rb	Rc	Rd	Re
A3~A5	0	0	0	0	X
MP	X	X	X	X	0

Title	SPI ROM		
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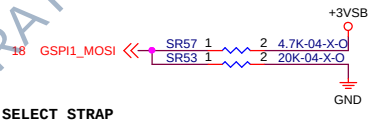
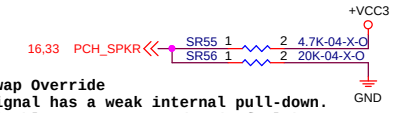
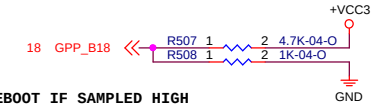


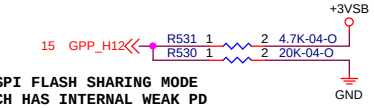
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



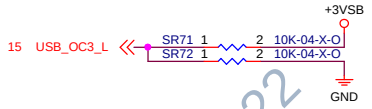
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



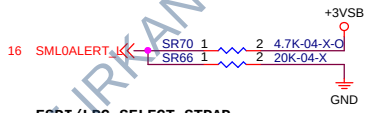
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING

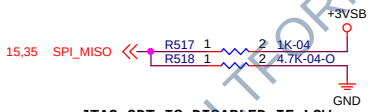


DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL

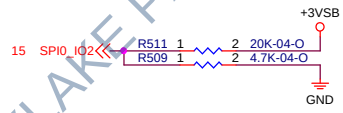


ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

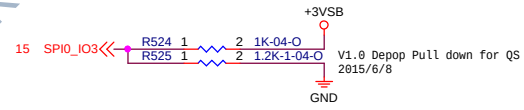
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



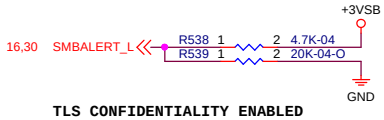
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



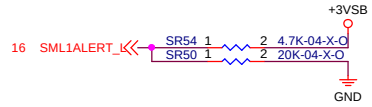
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1/ES2 only)



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD



EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

Title: Strap Pin		
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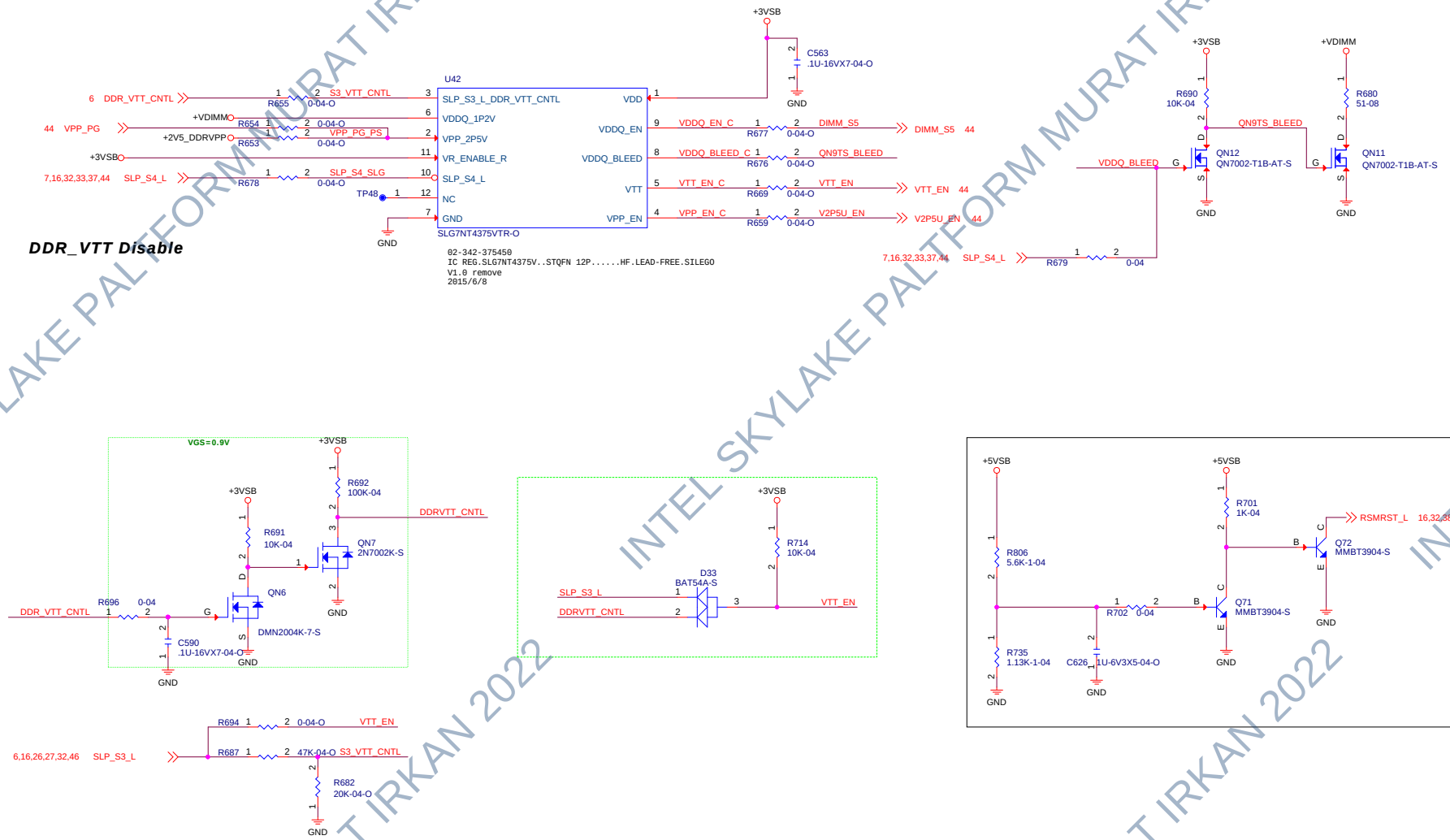

Title	DP SWITCH	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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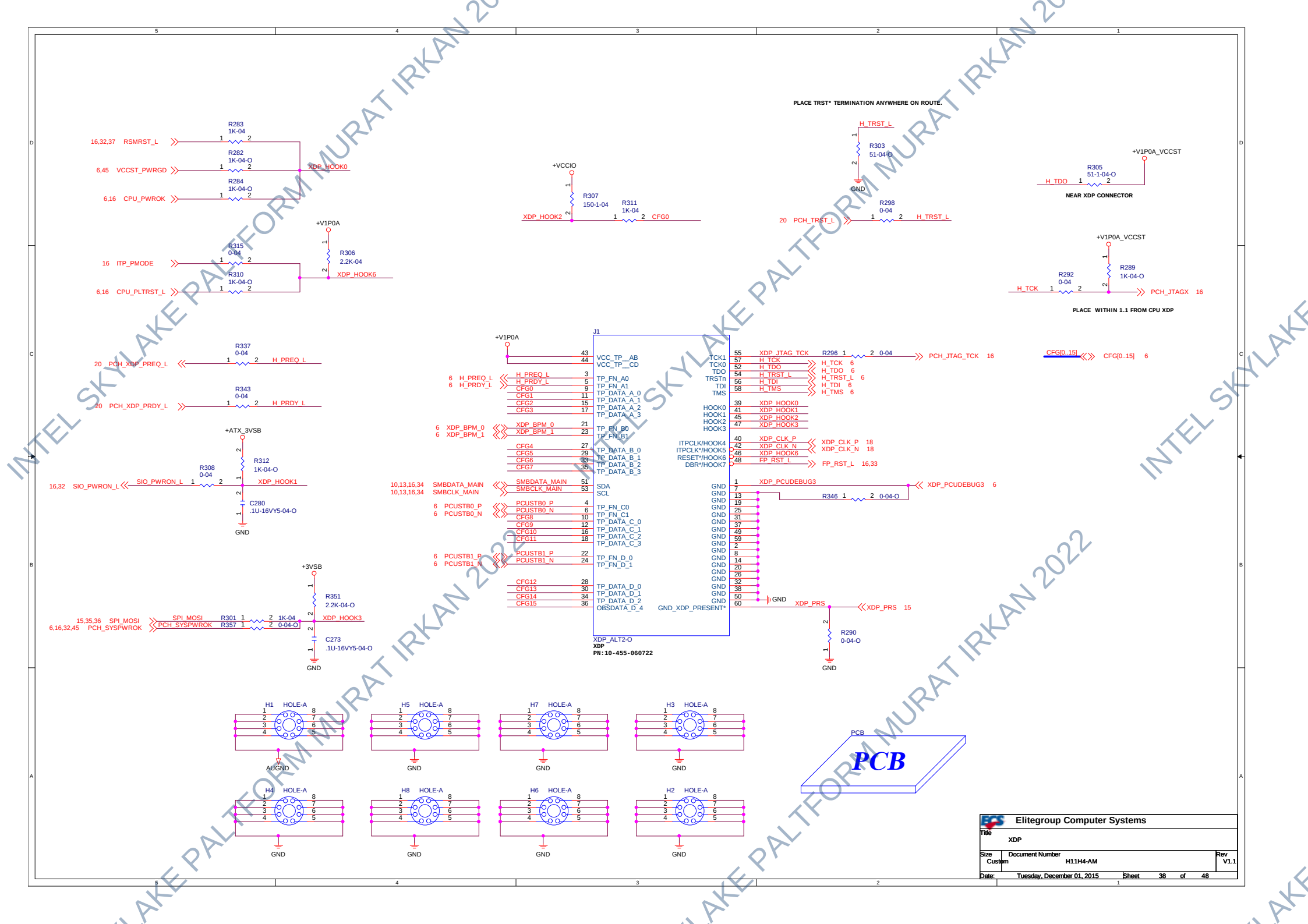
PLACE TRST* TERMINATION ANYWHERE ON ROUTE.
NEAR XDP CONNECTOR
PLACE WITHIN 1.1 FROM CPU XDP
J1
XDP_ALT2-O
XDP
PN:10-455-060722
PCB
PCB
Elitegroup Computer Systems
Title
XDP
Size
Custom
Document Number
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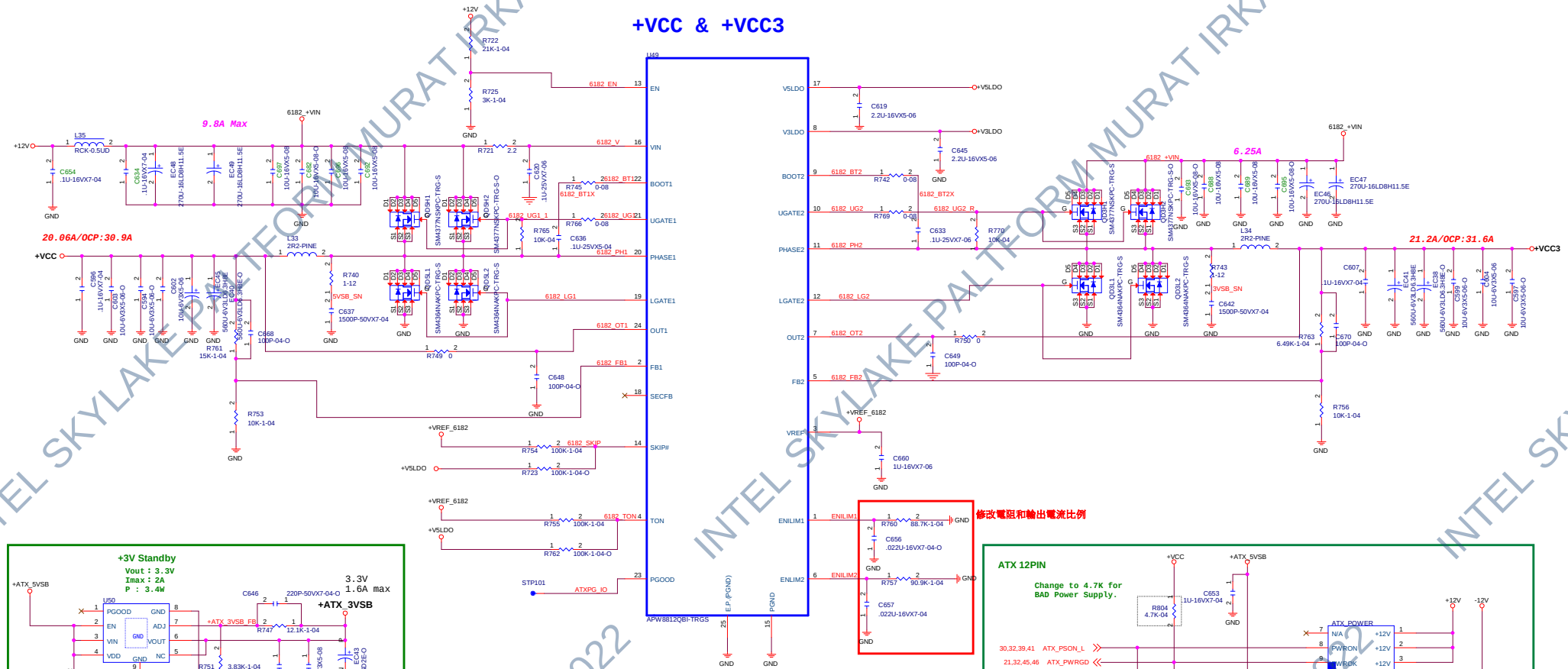
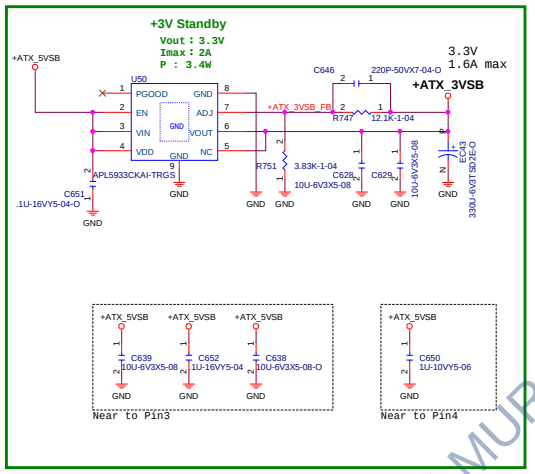
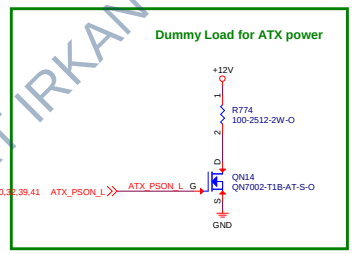
48

+VCC & +VCC3







Elitegroup Computer Systems		
Title: +VCC AND +VCC3		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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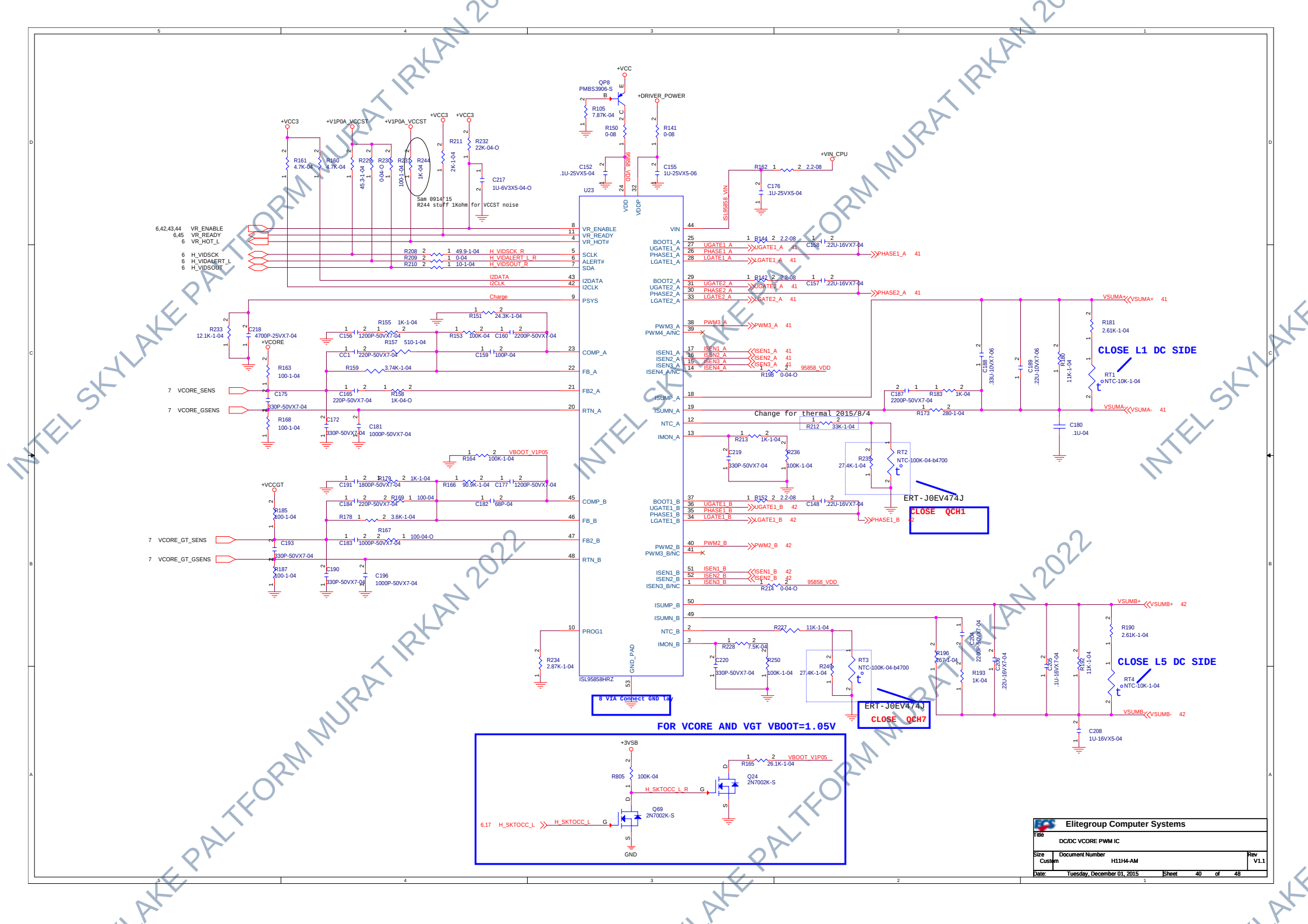
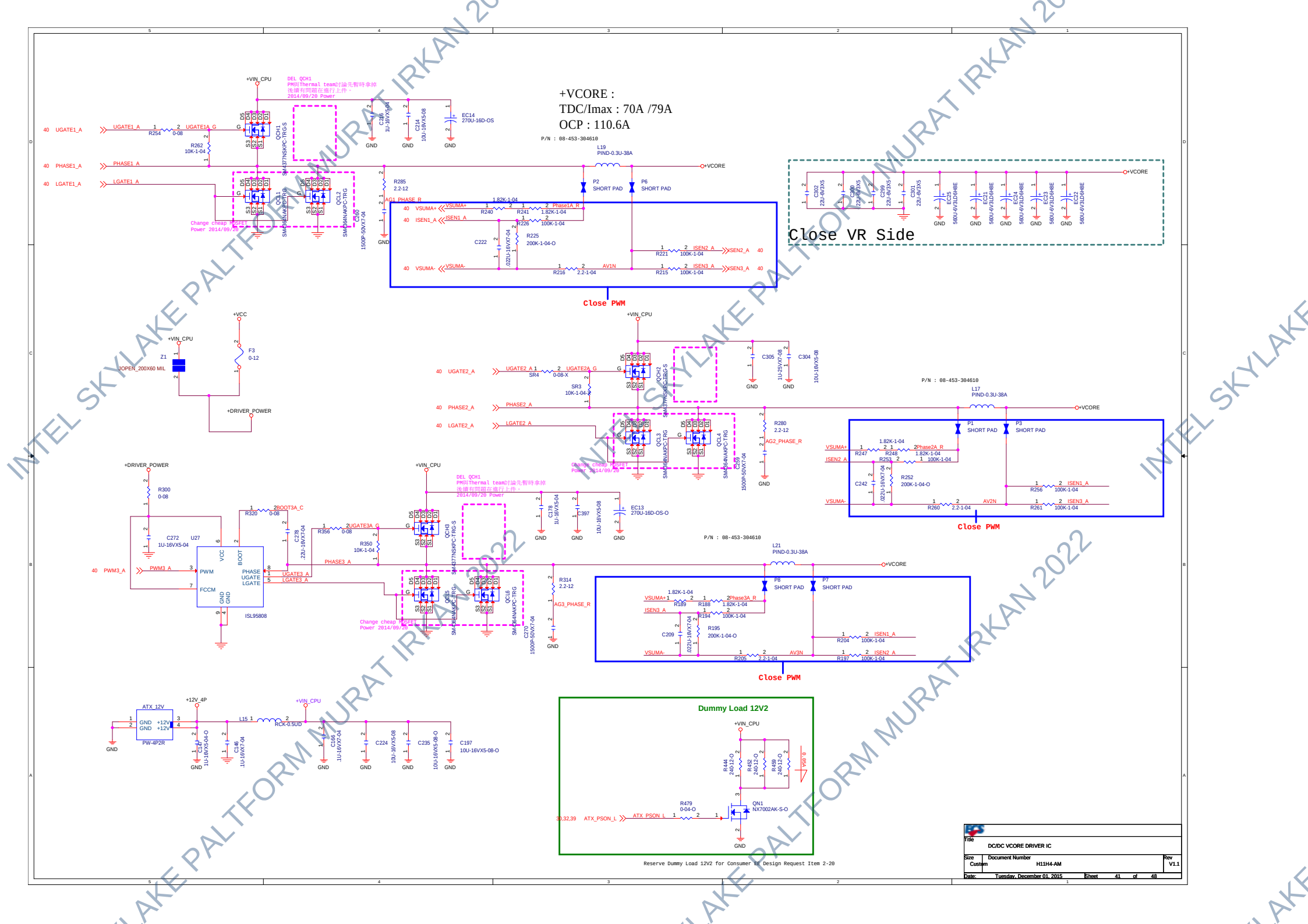
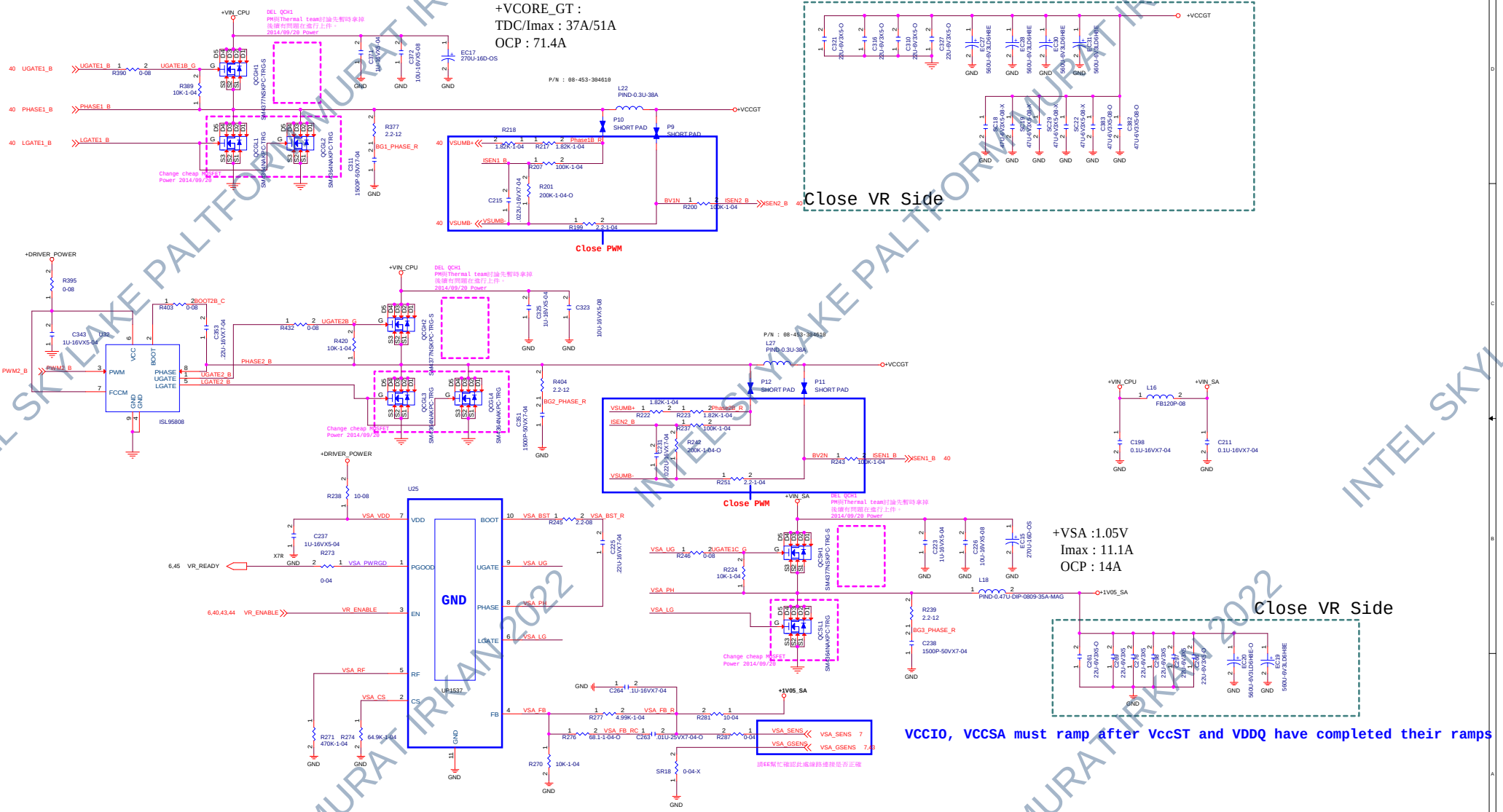
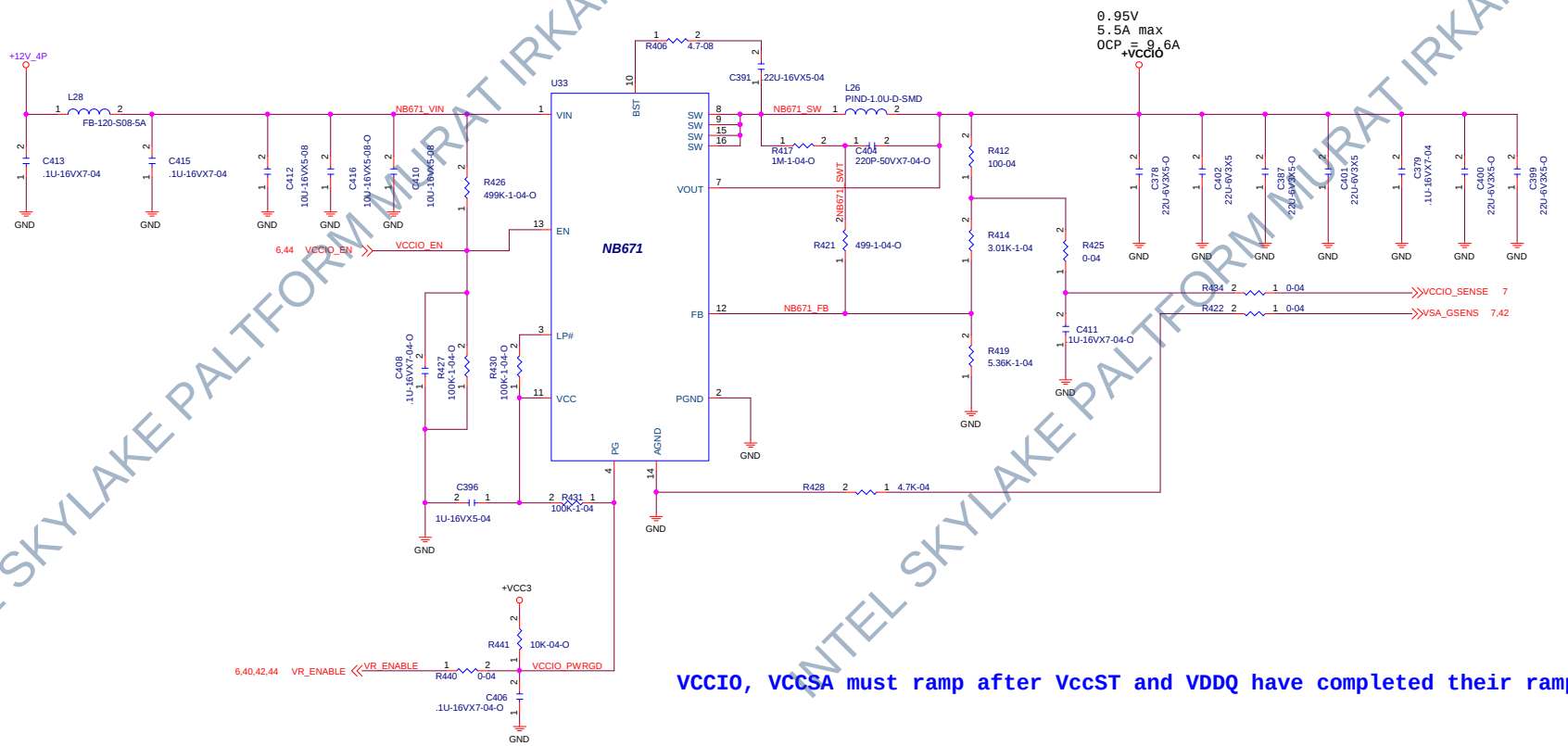

+VCC
+DRIVER_POWER
+VIN_CPU
+VCC3
+V1P0A_VCCST
+3VSB
+VCCGT
QP8
PMBS3906-S
U23
ISL95858HRZ
VR_ENABLE
VR_READY
VR_HOT#
H_VIDSCK
H_VIDALERT_L
H_VIDSOUT
I2DATA
I2CLK
Charge
PSYS
SCLK
ALERT#
SDA
COMP_A
FB_A
FB2_A
RTN_A
COMP_B
FB_B
FB2_B
RTN_B
PROG1
GND_PAD
VIN
BOOT1_A
UGATE1_A
PHASE1_A
LGATE1_A
BOOT2_A
UGATE2_A
PHASE2_A
LGATE2_A
PWM3_A
PWM4_A/NC
ISEN1_A
ISEN2_A
ISEN3_A
ISEN4_A/NC
ISUMP_A
ISUMN_A
NTC_A
IMON_A
BOOT1_B
UGATE1_B
PHASE1_B
LGATE1_B
PWM2_B
PWM3_B/NC
ISEN1_B
ISEN2_B
ISEN3_B/NC
ISUMP_B
ISUMN_B
NTC_B
IMON_B
VCORE_SENS
VCORE_GSENS
VCORE_GT_SENS
VCORE_GT_GSENS
VBOOT_V1P05
H_SKTOCC_L_R
H_SKTOCC_L
Sam 0914'15
R244 stuff 1Kohm for VCCST noise
Change for thermal 2015/8/4
CLOSE L1 DC SIDE
CLOSE L5 DC SIDE
CLOSE QCH1
CLOSE QCH7
ERT-J0EV474J
8 VIA Connect GND tab
FOR VCORE AND VGT VBOOT=1.05V
Elitegroup Computer Systems
DC/DC VCORE PWM IC
H11H4-AM
Tuesday, December 01, 2015

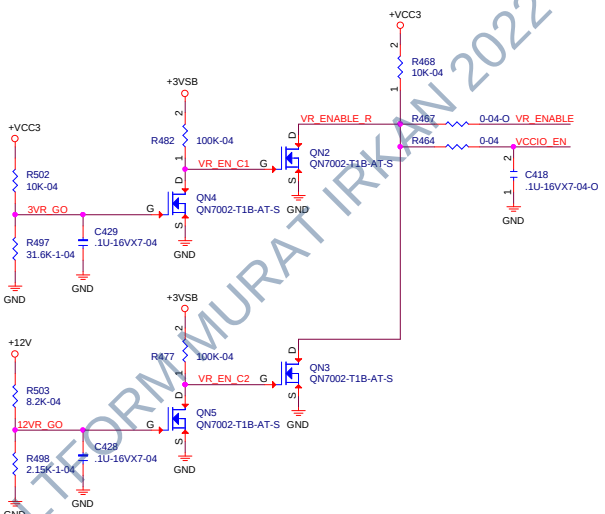






VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

VCCIO & VR ENABLE



Title	DC/DC VCCIO		
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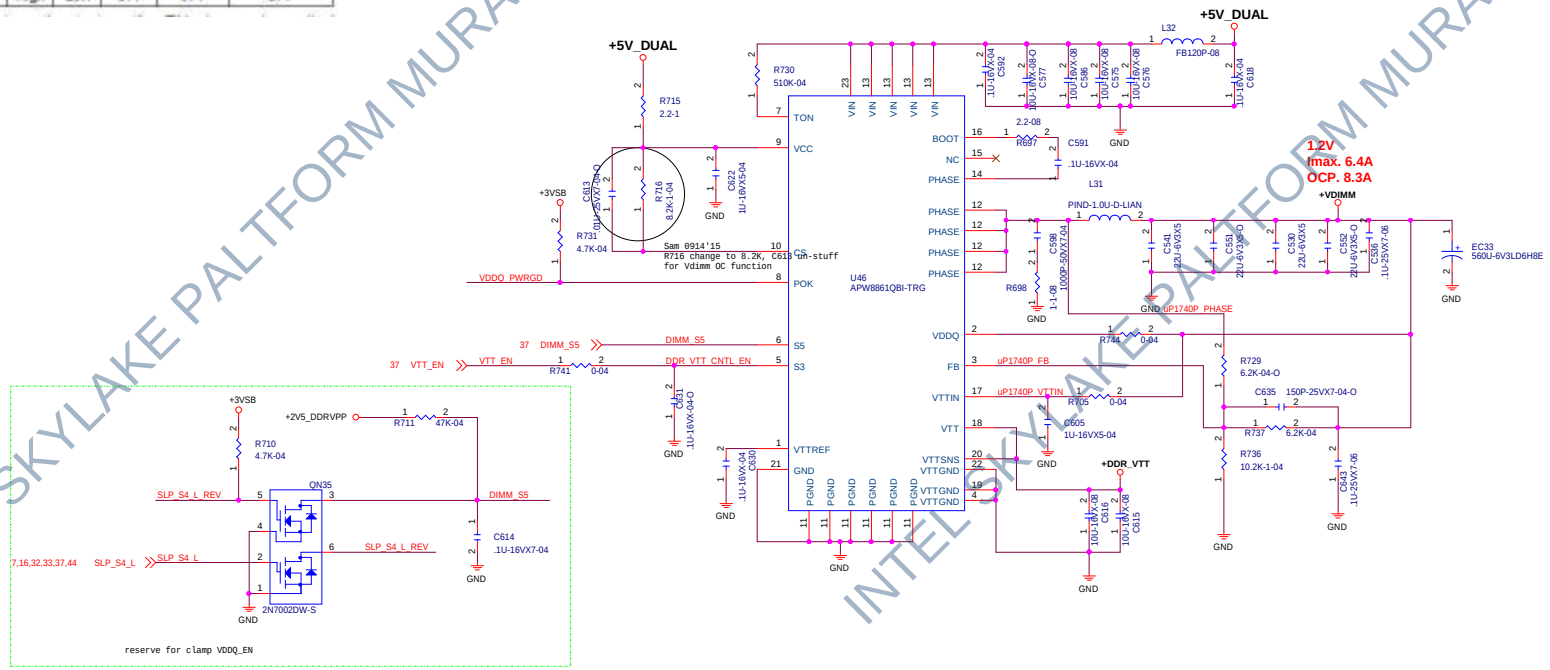
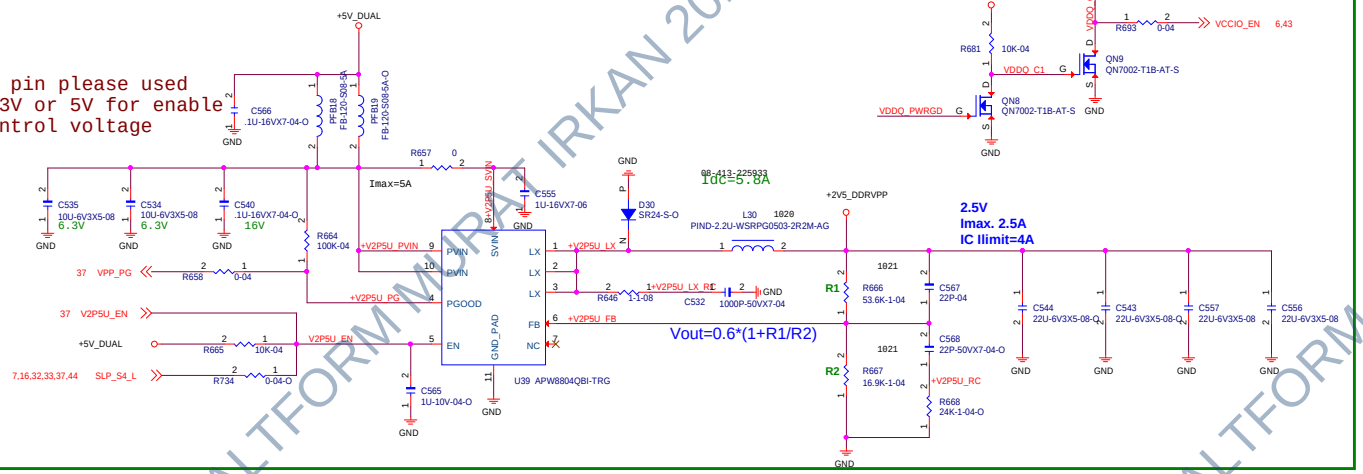
VDIMM Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



V2P5U

EN pin please used
3.3V or 5V for enable
control voltage



Title	DC/DC VDIMM & DDRVTT	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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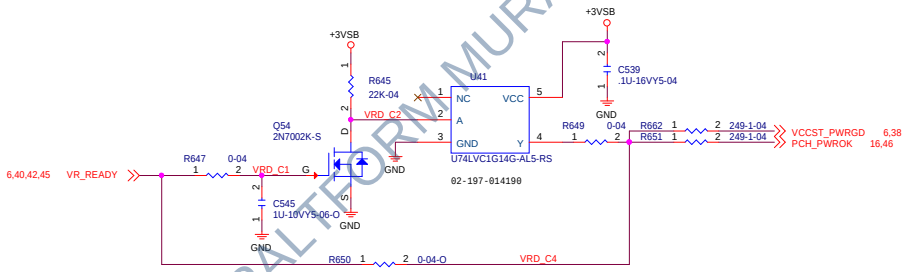
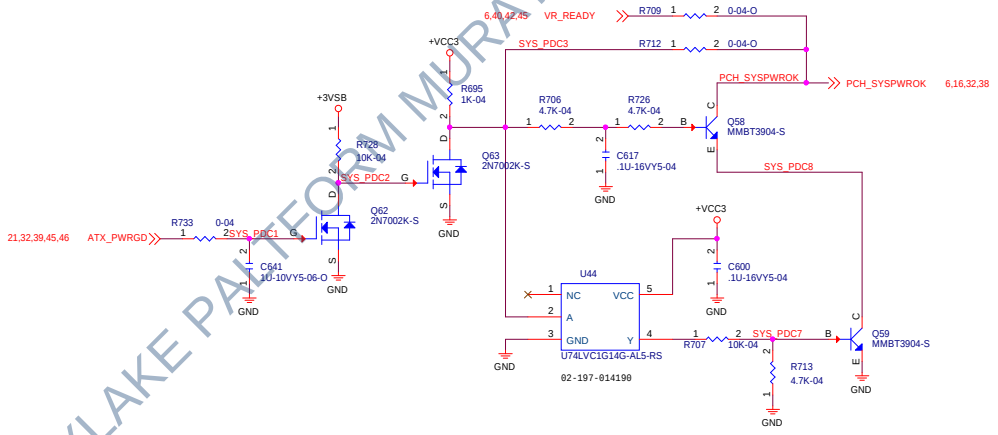
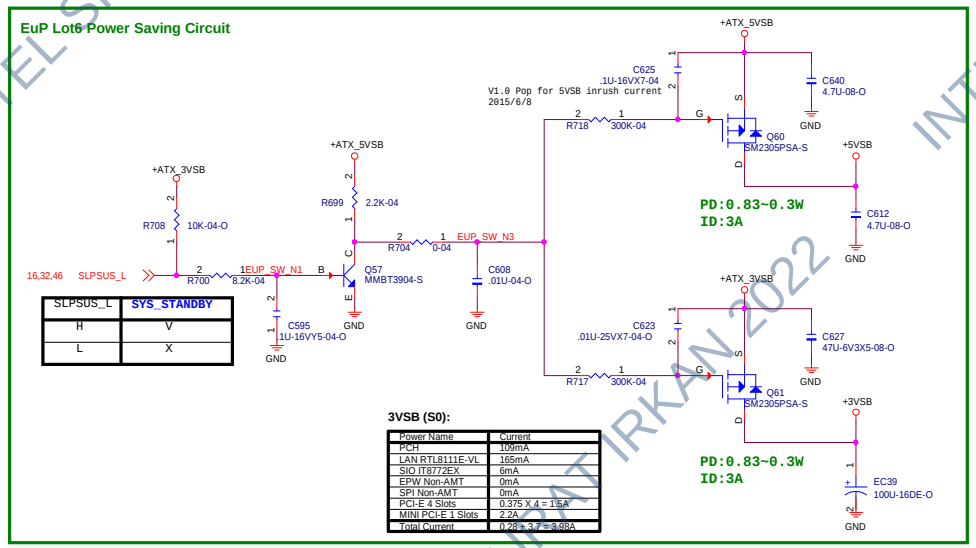
PCH & VCCST PWROK



SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit

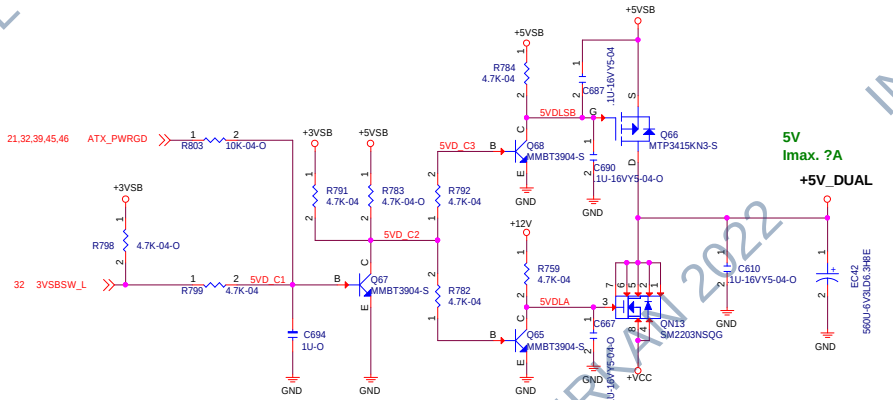


SLPSUS_L	SYS_STANDBY
H	V
L	X

3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A

5VDUAL



Title	DC/DC DDRVPP & 5VDUAL	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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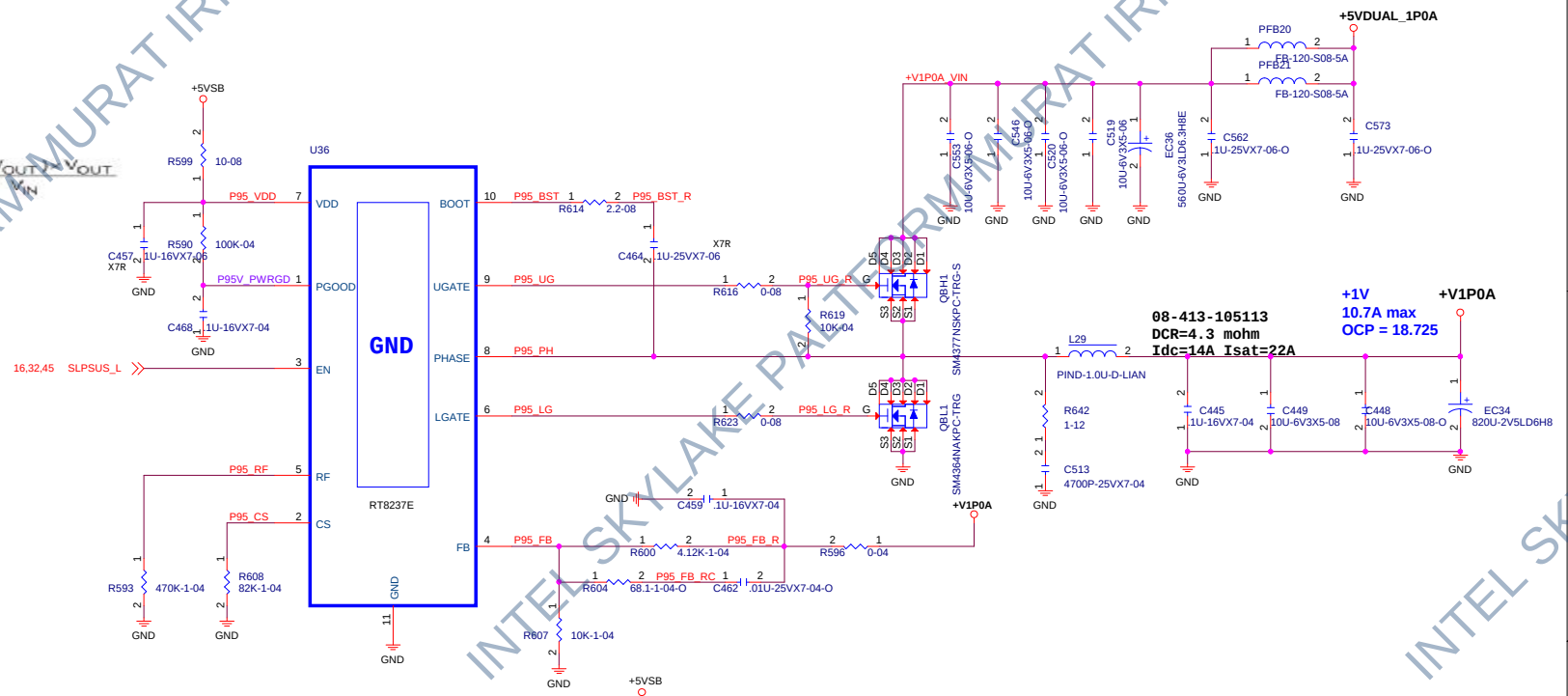
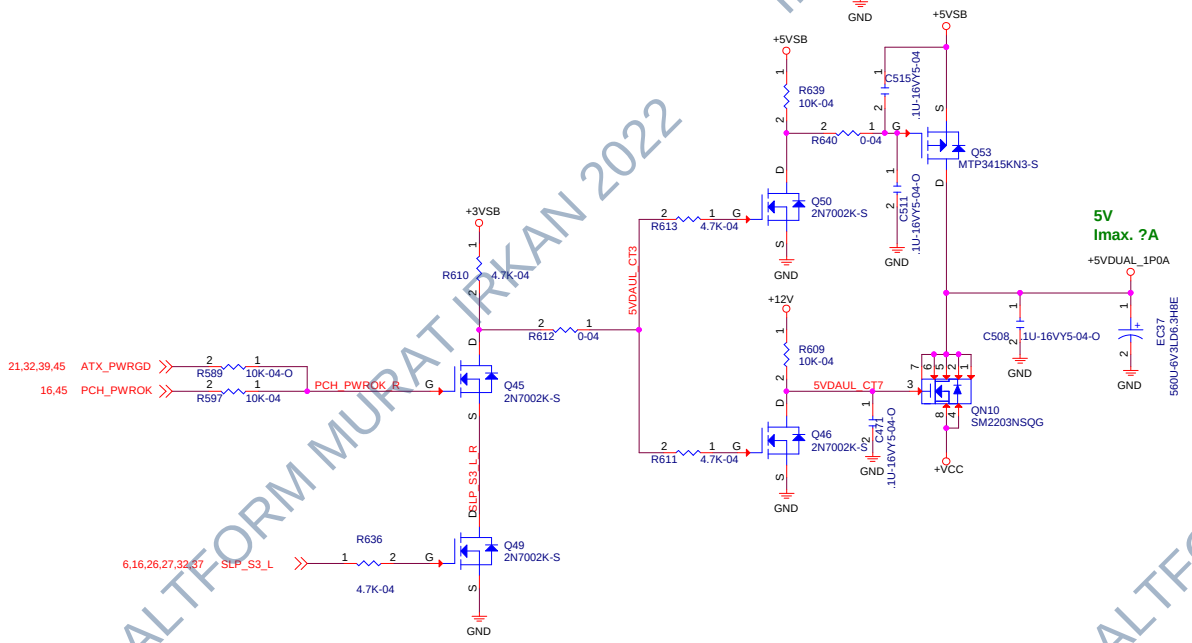
V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$





Title	V1P0A		
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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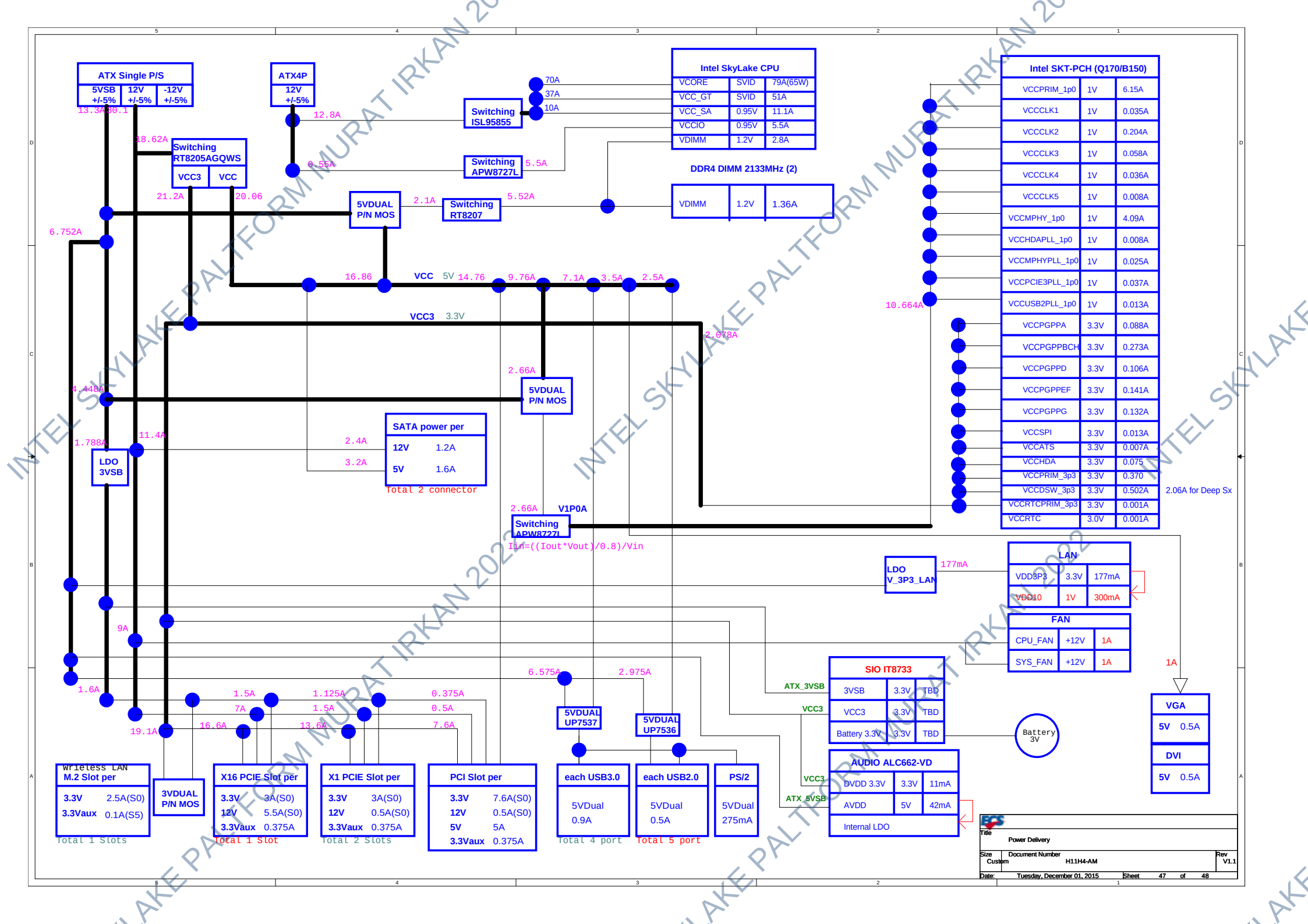


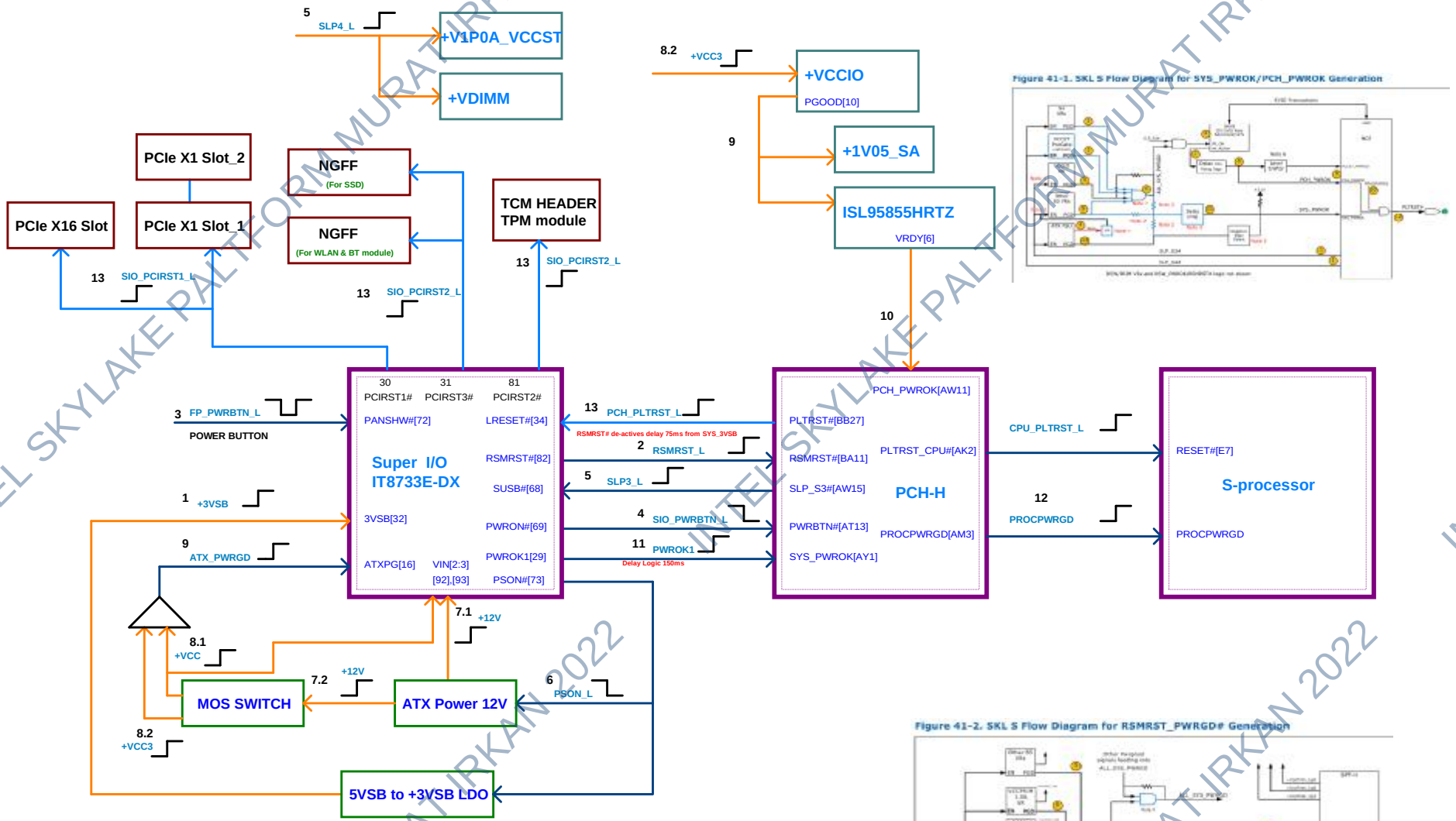
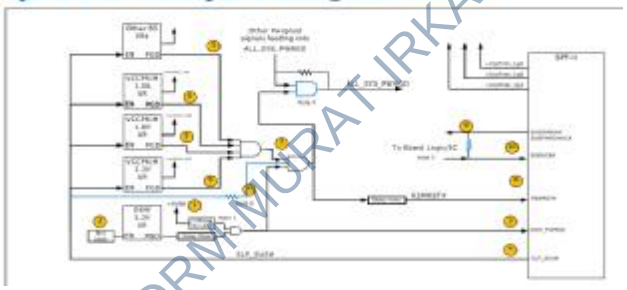


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



Title	Power Sequence MAP	
Size C	Document Number H11H4-AM	Rev V1.1
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