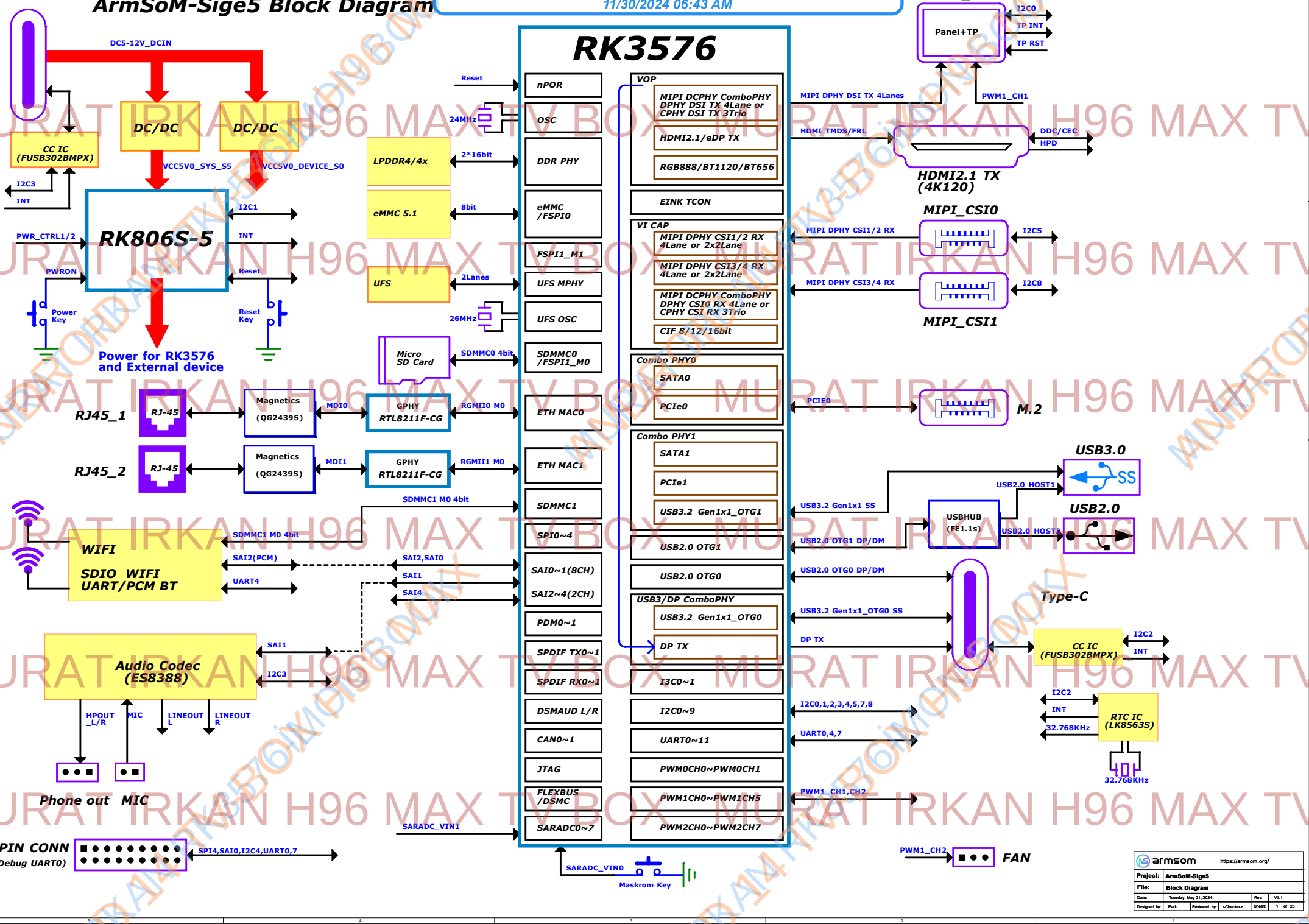
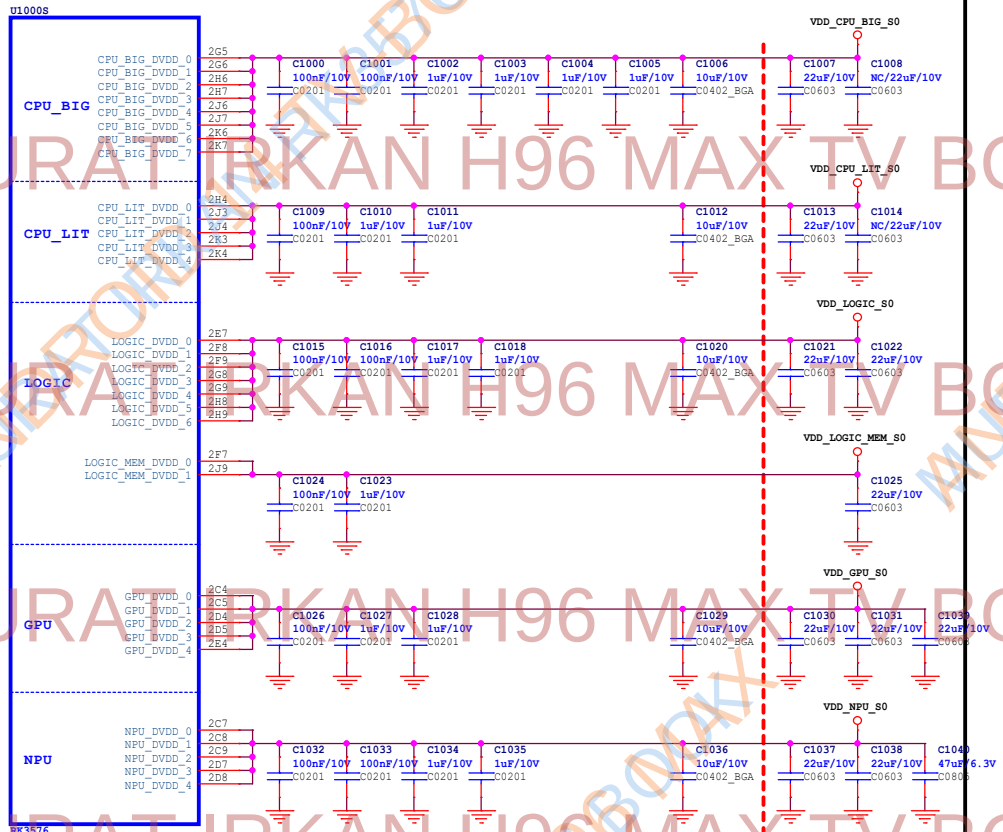
ArmSoM-Sige5 Block Diagram

MURAT IRKAN SİSTEM KONTROL-1
11/30/2024 06:43 AM



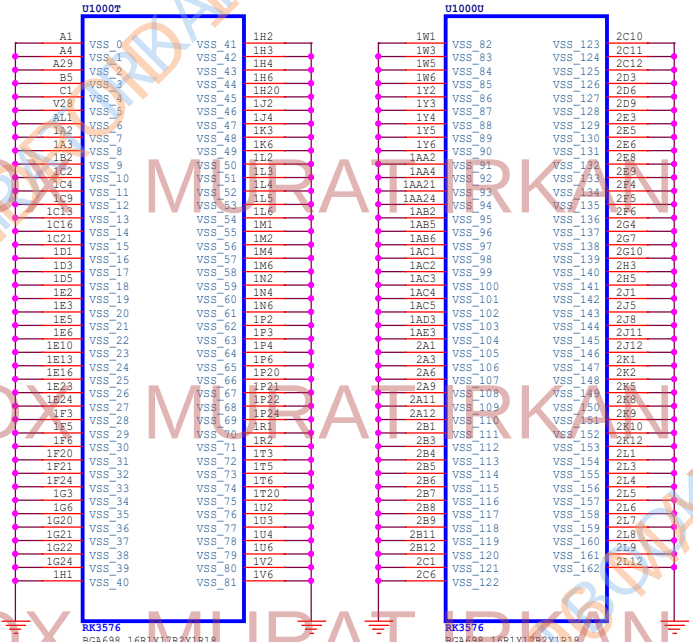
armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	Block Diagram
Date:	Tuesday, May 21, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	1 of 25

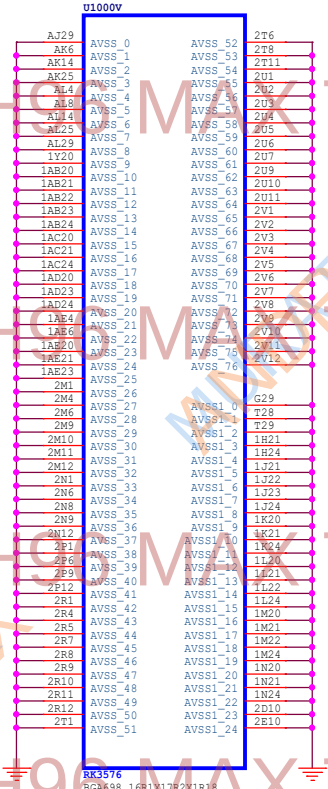
RK3576_S (Power)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_T/U/V (GND)





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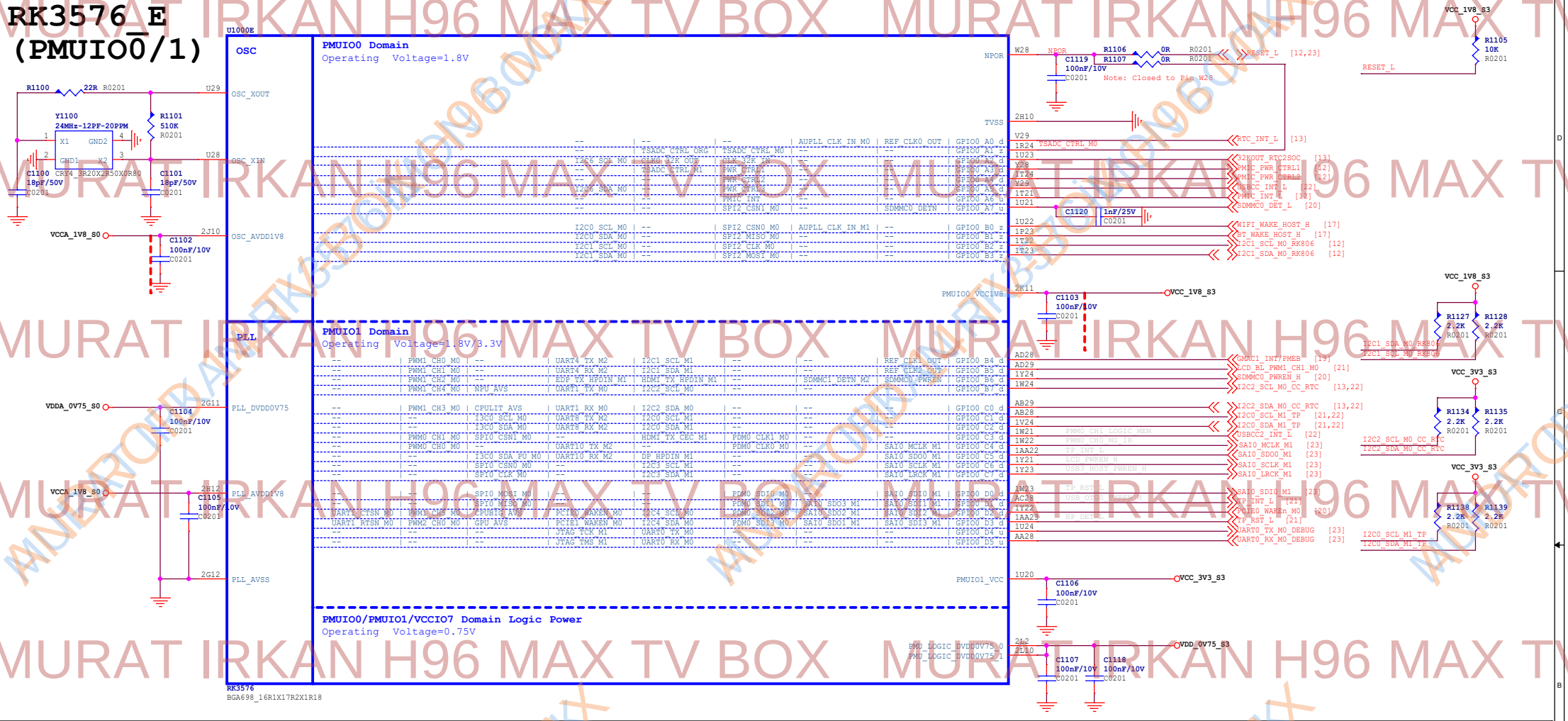
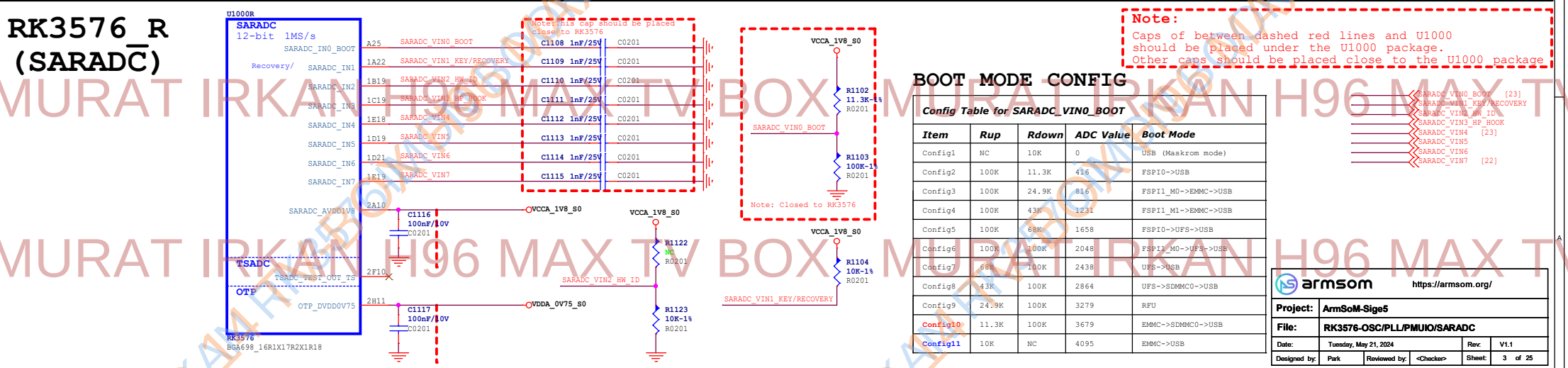
Project:	ArmSoM-Sige5				
File:	RK3576-Power/GND				
Date:	Tuesday, May 21, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 25

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package.

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

SARADC_VIN0_BOOT [23]
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_HW_ID
SARADC_VIN3_HP_HOOK
SARADC_VIN4 [23]
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7 [22]

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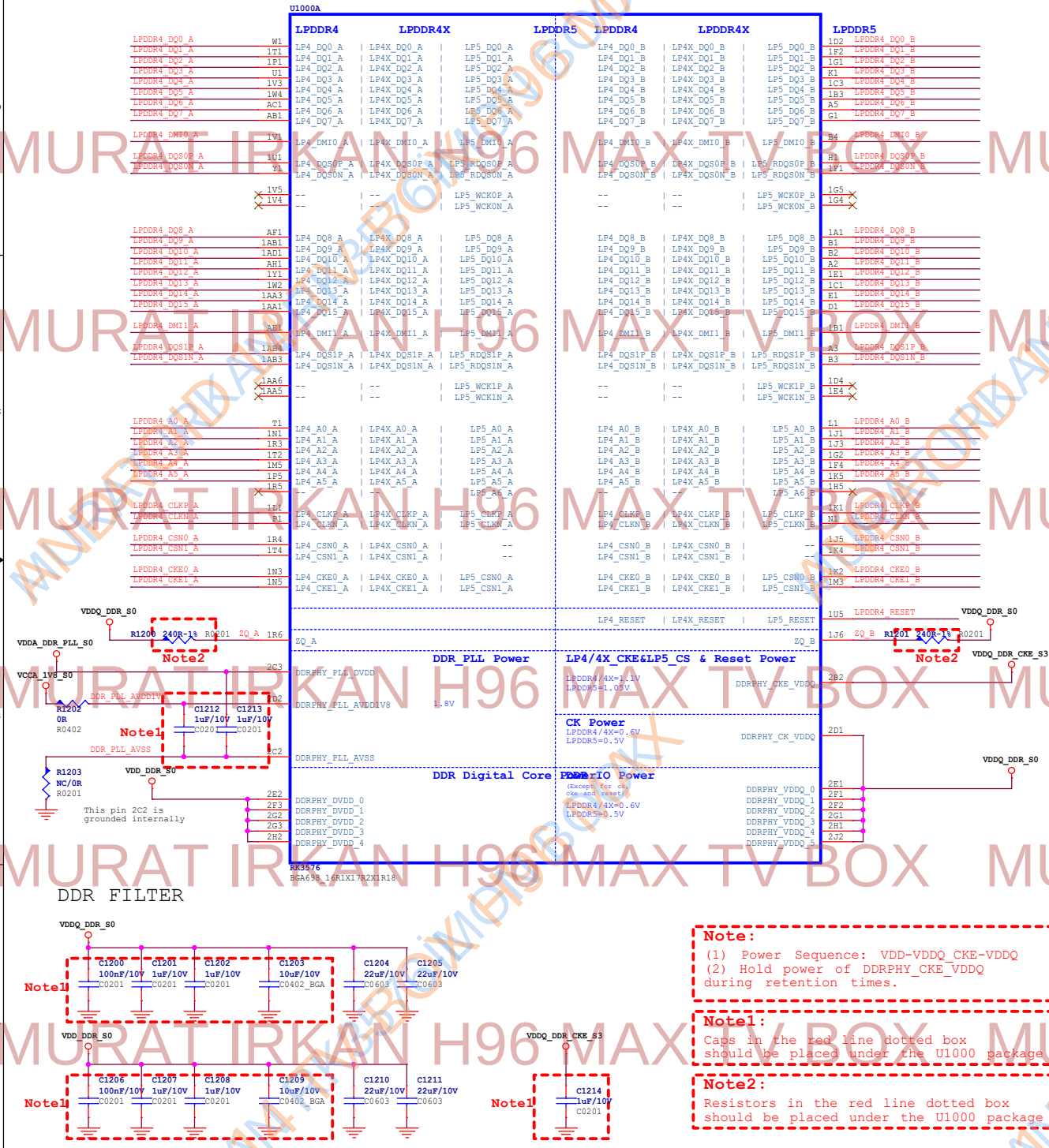
Project:	ArmSoM-Sige5				
File:	RK3576-OSC/PLL/PMUIO/SARADC				
Date:	Tuesday, May 21, 2024			Rev.	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	3 of 25

RK3576_A(DDRPHY)



LPDDR4 Signal

Note:

(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:

Caps in the red line dotted box should be placed under the U1000 package

Note2:

Resistors in the red line dotted box should be placed under the U1000 package

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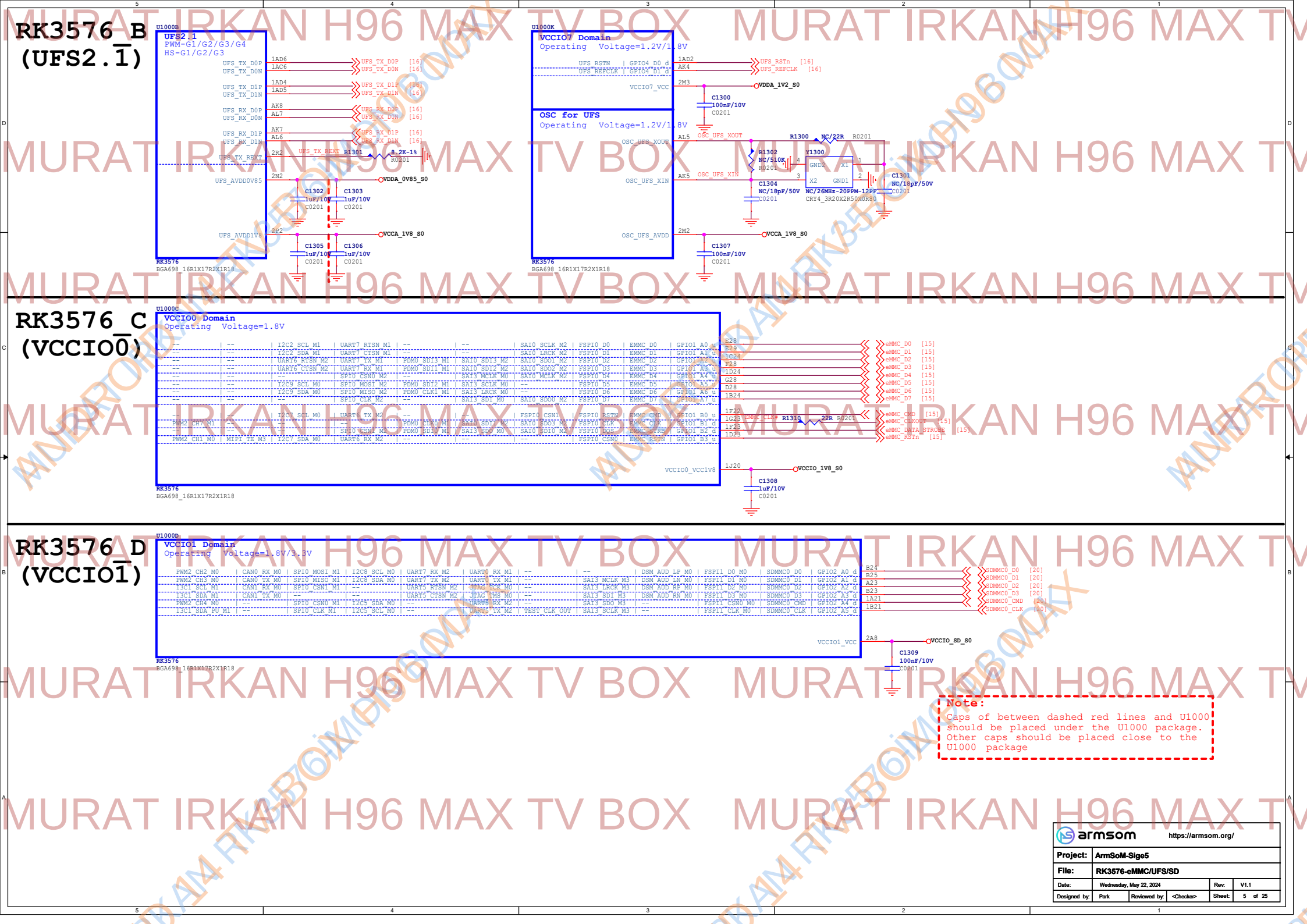
Project:	ArmSoM-Sige5			
File:	RK3576-DDR PHY			
Date:	Tuesday, May 21, 2024		Rev.	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	4 of 25


RK3576_B
(UFS2.1)
U1000B
UFS2.1
PWM-G1/G2/G3/G4
HS-G1/G2/G3
UFS_TX_D0P
UFS_TX_D0N
UFS_TX_D1P
UFS_TX_D1N
UFS_RX_D0P
UFS_RX_D0N
UFS_RX_D1P
UFS_RX_D1N
UFS_TX_REXT
UFS_AVDD0V85
UFS_AVDD1V8
R1301
8.2K-1%
R0201
C1302
C1303
C1305
C1306
1uF/10V
C0201
VDDA_0V85_S0
VCCA_1V8_S0
RK3576
BGA698_16R1X17R2X1R18
U1000K
VCCIO7 Domain
Operating Voltage=1.2V/1.8V
UFS_RSTN
UFS_REFCLK
GPIO4_D0_d
GPIO4_D1_d
VCCIO7_VCC
VDDA_1V2_S0
C1300
100nF/10V
OSC for UFS
Operating Voltage=1.2V/1.8V
OSC_UFS_XOUT
OSC_UFS_XIN
OSC_UFS_AVDD
R1300
NC/22R
R1302
NC/510K
Y1300
C1304
NC/18pF/50V
C1301
NC/26MHz-20PPM-12PF
CRY4_3R20X2R50X0R80
C1307
RK3576_C
(VCCIO0)
U1000C
VCCIO0 Domain
Operating Voltage=1.8V
VCCIO0_VCC1V8
VCCIO_1V8_S0
C1308
1uF/10V
eMMC_D0
eMMC_D1
eMMC_D2
eMMC_D3
eMMC_D4
eMMC_D5
eMMC_D6
eMMC_D7
eMMC_CMD
eMMC_CLKOUT
eMMC_DATA_STROBE
eMMC_RSTn
EMMC_CLK#
R1310
22R
RK3576_D
(VCCIO1)
U1000D
VCCIO1 Domain
Operating Voltage=1.8V/3.3V
VCCIO1_VCC
VCCIO_SD_S0
C1309
100nF/10V
SDMMC0_D0
SDMMC0_D1
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package
armsom
https://armsom.org/
Project: ArmSoM-Sige5
File: RK3576-eMMC/UFS/SD
Date: Wednesday, May 22, 2024
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 5 of 25

RK3576_L (USB3/DP)

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R18

Support:
Type-C With Displayport Alternate Mode

2T2 DP_TX_AUXP [22]
2T3 DP_TX_AUXN [22]
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P [22]
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N [22]
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P [22]
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N [22]
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P [22]
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N [22]
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P [22]
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N [22]
2T7 USB3_OTG0_DP_TX_REXT R1400 8.2K-1% R0201
2M5 2N5 VDDA_0V85_S0
C1400 1uF/10V C0201
C1401 NC/1uF/10V C0201
2N4 VCCA_1V8_S0
C1402 1uF/10V C0201
C1403 NC/1uF/10V C0201

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

RK3576
BGA698_16R1X17R2X1R18

AK9 USB2_OTG0_DP [22]
AL9 USB2_OTG0_DM [22]
2R6 USB2_OTG0_ID Note: There is an internal pull-up resistor connected to 1.8V TP18 TP_0R7
2P3 USB2_OTG0_VBUSDET [22]
2R3 USB2_OTG0_REXT R1401 200R-1% R0201
C1404 100nF/10V C0201
2T4 USB2_HOST1_DP [22]
2T5 USB2_HOST1_DM [22]
2T9 USB2_OTG1_ID TP19 TP_0R7
2T10 USB2_OTG1_VBUSDET
2U8 USB2_OTG1_REXT R1402 200R-1% R0201
2P5 VDDA_0V75_S0
C1405 100nF/10V C0201
2P4 VCCA_1V8_S0
C1406 100nF/10V C0201
C1407 NC/1uF/10V C0201
2P7 VCC_3V3_S0
C1408 100nF/10V C0201

The USB2_OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

VCC_3V3_S0
C1409 NC/100nF/10V C0201
R1406 NC/20K R0201
R1405 NC/4.7K R0201

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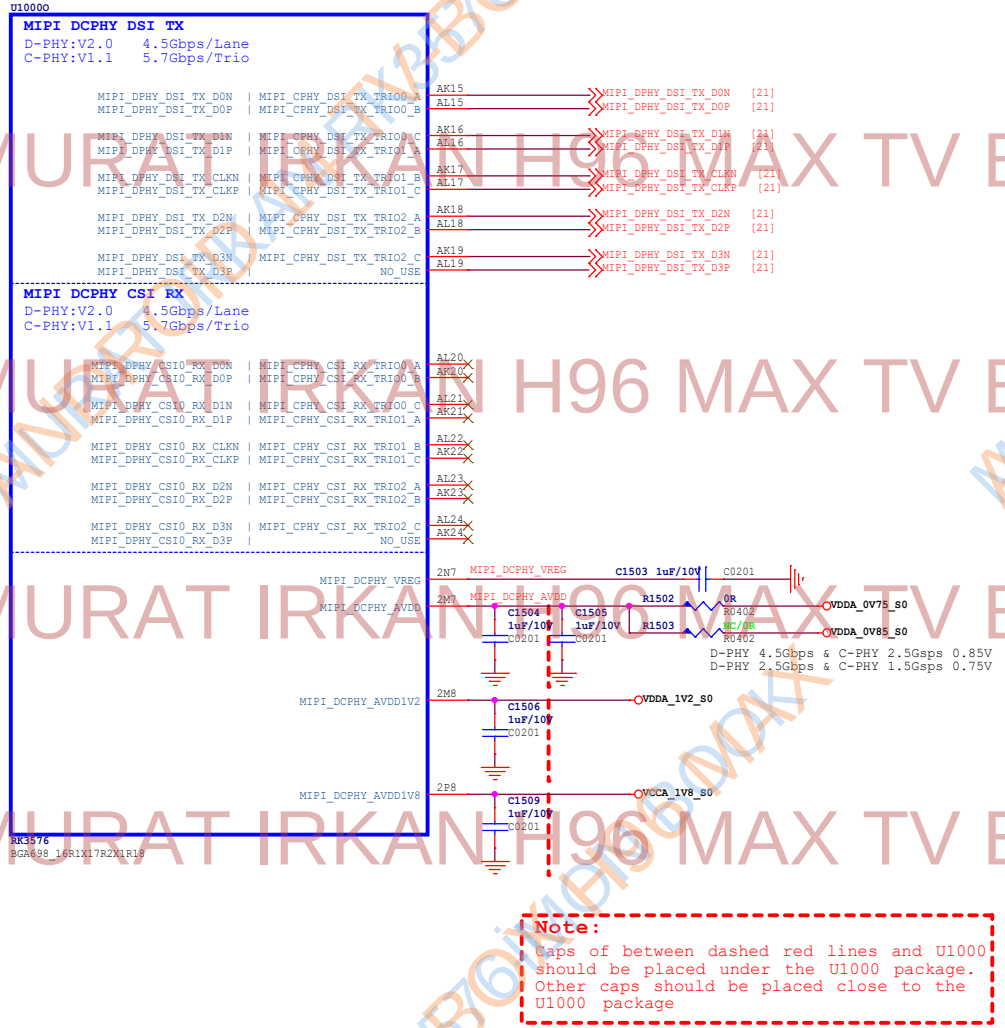
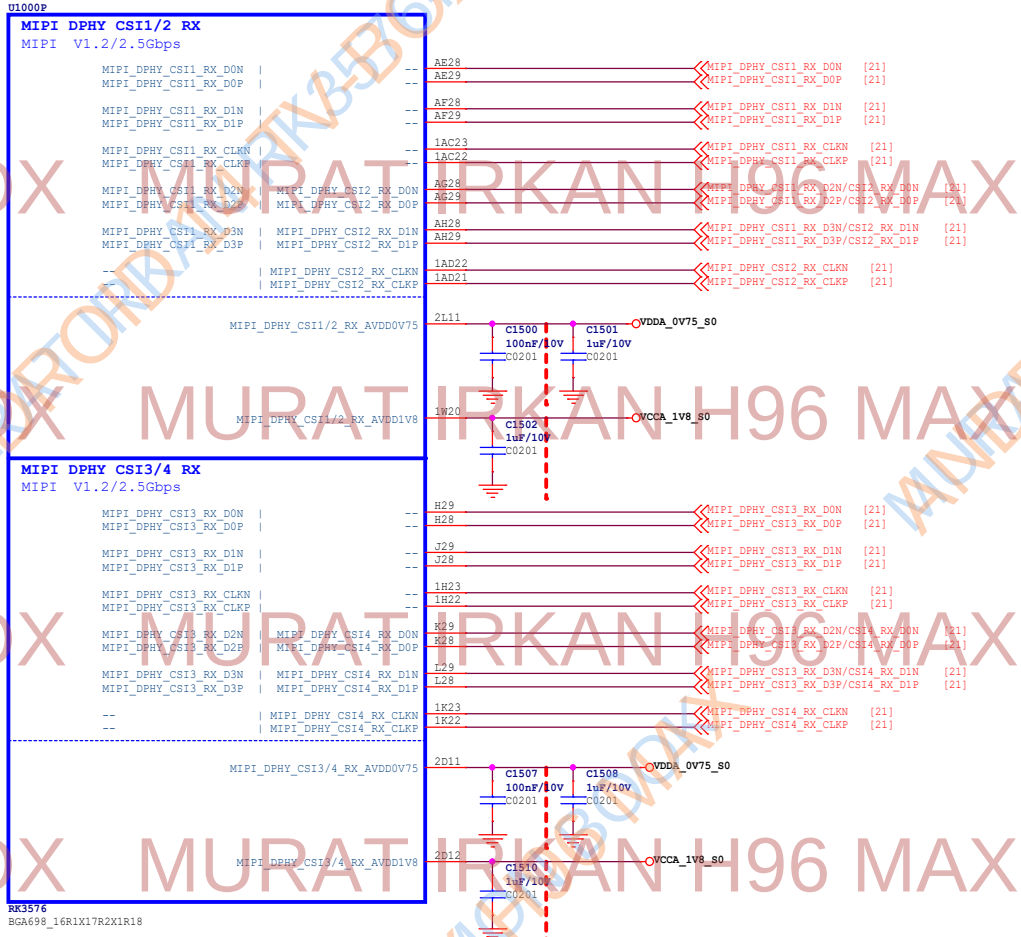
Project:	ArmSoM-Sige5				
File:	RK3576-TypeC/USB				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 25

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

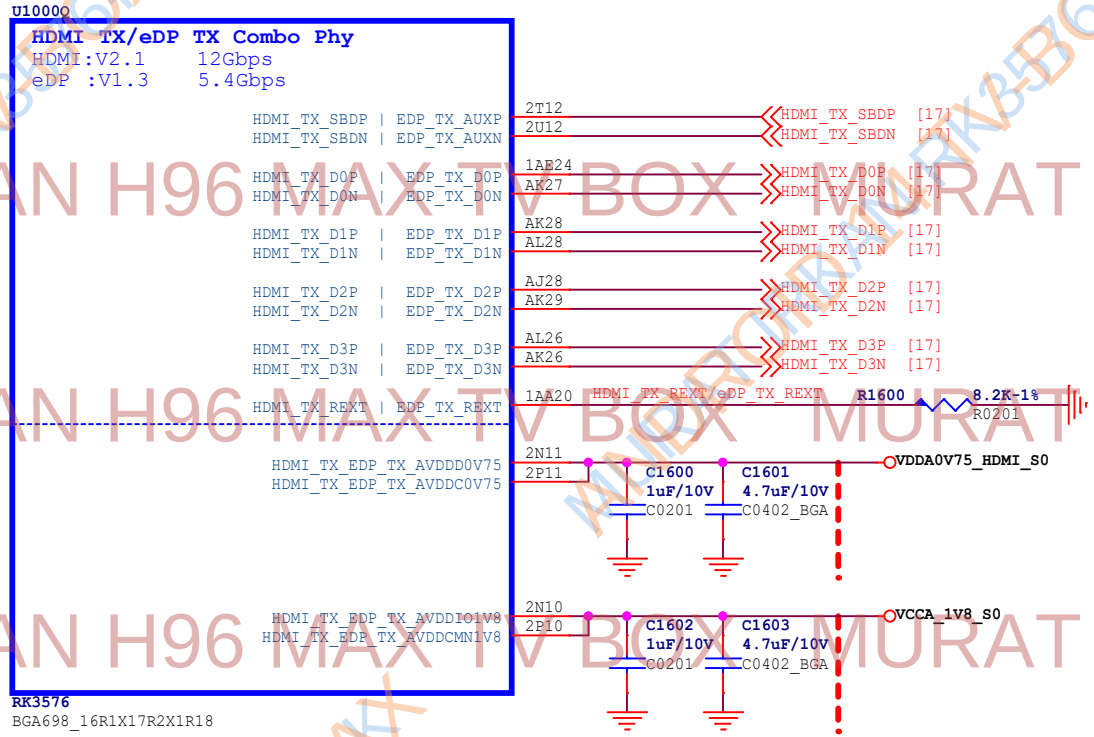


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	RK3576-MIPI DSI/CSI				
Date:	Tuesday, May 21, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 25

RK3576_Q(HDMI/eDP)

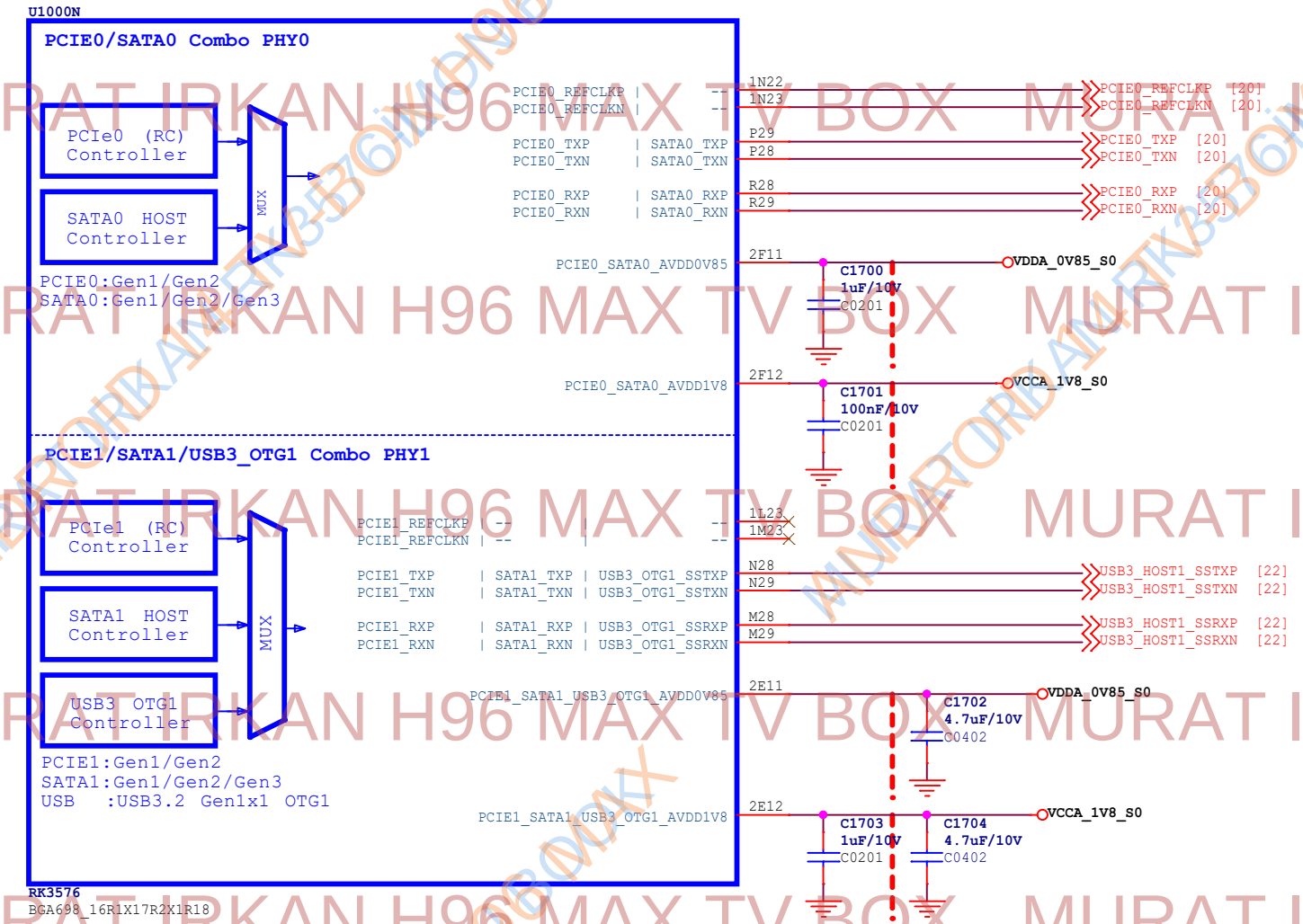
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ArmSoM-Sige5				
File:	RK3576-MIPI DSI/CSI				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 25

RK3576_N(PCIe/SATA/USB3)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/				
Project:	ArmSoM-Sige5			
File:	RK3576-PCIe/SATA/USB3			
Date:	Tuesday, May 21, 2024		Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	9 of 25

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain
Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d	1D6
PWM2_CH4_M1	PCIE1_WAKEN_M2	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d	1C6
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d	1C5
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS0_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d	1B6
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d	1B5
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d	A7
--	--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d	1A5
--	--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d	B7
PWM2_CH7_M0	--	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d	B6
CAN1_RX_M2	PCIE0_WAKEN_M2	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d	1A6
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d	B8
									1A4

VCCIO2_VCC 2A2 — C1800 100nF/10V C0201 — VCCIO_AUDIO

RK3576
BGA698_16R1X17R2X1R18

SAI1_MCLK_M0 [23]
SAI1_SCLK_M0 [23]
USB3_HOST_PWREN_H [22]
SAI1_LRCK_M0 [23]
USB_OTG0_PWREN_H [22]
SAI1_SDO0_M0 [23]
HP_DET_L [23]
LED_RED_EN [23]
LED_GREEN_EN [23]
SAI1_SDI0_M0 [23]
I2C3_SDA_M0_Audio [23]
I2C3_SCL_M0_Audio [23]

VCCIO_AUDIO
R1800 2.2K R0201
R1801 2.2K R0201
I2C3_SDA_M0_Audio
I2C3_SCL_M0_Audio

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d	A28
PWM1_CH1_M1	PCIE1_WAKEN_M1	SPI1_MOST_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d	B27
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d	1A23
--	PCIE0_WAKEN_M1	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d	A27
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d	B26
--	--	--	--	UART3_RX_M2	PDM0_SDI3_M2	--	SAI3_MCLK_M1	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d	1B22
PWM0_CH1_M1	--	SPI2_CLK_M1	I2C6_SCL_M1	UART4_RTSN_M1	--	--	SAI3_CSN0_M1	SDMMC1_DET_L	ETH1_RXDV_M1	GPIO1_C2_d	B29
--	--	SPI2_CSN0_M1	I2C6_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M0	SDMMC1_PWREN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d	1C23
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d	1B23
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d	B28
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_TXCTL_M1	GPIO1_C6_d	A26
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d	1C22
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	FSPI1_D4_M1	--	ETH1_RXD1_M1	GPIO1_D0_d	C29
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	FSPI1_D5_M1	--	ETH1_RXCTL_M1	GPIO1_D1_d	1D22
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	FSPI1_D6_M1	--	ETH1_MDC_M1	GPIO1_D2_d	1A24
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	FSPI1_D7_M1	--	ETH1_MDIO_M1	GPIO1_D3_d	C28
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	FSPI1_DQS_M1	--	ETH1_MCLK_M1	GPIO1_D4_d	1E21
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d	1E22

VCCIO3_VCC 2B10 — C1801 100nF/10V C0201 — VCCIO_WL

RK3576
BGA698_16R1X17R2X1R18

SDMMC1_D0_M0 [17]
SDMMC1_D1_M0 [17]
SDMMC1_D2_M0 [17]
SDMMC1_D3_M0 [17]
SDMMC1_CMD_M0 [17]
SDMMC1_CLK_M0 [17]
UART4_RTSN_M1 [17]
UART4_CTSN_M1 [17]
UART4_TX_M1 [17]
UART4_RX_M1 [17]
WIFI_REG_ON_H [17]
BT_REG_ON_H [17]
For BT

SAI2_SDO_M0 [17]
SAI2_SCLK_M0 [17]
SAI2_LRCK_M0 [17]
SAI2_SDI_M0 [17]
HOST_WAKE_BT_H [17]
LCD_PWREN_H [21]
For BT

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	PCIE1_WAKEN_M3	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d	AK3
PWM2_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d	AL2
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	--	--	HDMI_TX_SCL	--	--	DSM_AUD_RF_M1	GPIO4_C2_d	1AE2
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d	AL3
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d	AK1
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	PCIE0_WAKEN_M3	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d	1AE1
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d	AJ1
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d	

VCCIO6_VCC 2N3 — C1802 100nF/10V C0201 — VCC_3V3_S0

RK3576
BGA698_16R1X17R2X1R18

HDMI_TX_CEC_M0 [17]
HDMI_TX_HPDIN_M0 [17]
HDMI_TX_SCL [17]
HDMI_TX_SDA [17]
SPI4_CSN0_M0 [23]
SPI4_MOSI_M0 [23]
SPI4_MISO_M0 [23]
SPI4_CLK_M0 [23]

armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	RK3576-GPIO VCCIO2/3/6		
Date:	Tuesday, May 21, 2024	Rev:	V1.1
Designed by: Park	Reviewed by: <Checker>	Sheet:	10 of 25

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d
--	--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d
--	--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d
--	--	PCIE0_CLKREQn_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXCLK_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d
--	--	PCIE1_CLKREQn_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d
PWM1_CH1_M2	--	--	--	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d
PWM1_CH2_M2	--	--	--	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d
PWM0_CH0_M2	--	--	--	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C3_d
PWM1_CH3_M2	--	--	--	UART11_TX_M1	PDM1_SDO_M0	SAI2_SDO_M1	--	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C4_d
PWM0_CH1_M2	--	--	--	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d
PWM0_CH2_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d
PWM0_CH3_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d
PWM2_CH4_M2	--	I2C7_SCL_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	VI_CIF_PRELIGHT_TRIG_M0	GPIO2_D4_d
PWM2_CH5_M2	--	I2C7_SDA_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	DSP_FLASH_TRIGOUT_M0	GPIO2_D5_d
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH1_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d
--	MIPI_TE_M2	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d

RK3576
BGA698_16R1X17R2X1R18

VCCIO4_VCC

2A7

C1900 NC/100nF/10V C0201

C1901 1uF/10V C0201

VCC_3V3_S0

R1909 10K R0201

R1910 10K R0201

B22 TYPEC_DPTX_AUX_PUPDCTL1 [22]

B20 TYPEC_DPTX_AUX_PUPDCTL2 [22]

B19 HDMI_TX_ON_H [17]

1A18 SPK_CTL_H

LCD_BL_EN_H [21]

1A17 PCIE0_CLKREQn_M0 [20]

1B16 PCIE1_CLKREQn_M0

LCD_RESET_L [21]

A19 PCIE0_PERSTn [20]

1C18 GMAC0_RSTn [18]

A21 I2C8_SCL_M2/UART7_TX_M0 [23]

B21 I2C8_SDA_M2/UART7_RX_M0 [23]

A17 GMAC1_RXD2_M0 [19]

1A15 GMAC1_RXD3_M0 [19]

1D15 GMAC1_RXCLK_M0 [19]

A15 GMAC1_TXD2_M0 [19]

1A13 GMAC1_TXD3_M0 [19]

1C15 GMAC1_TXCLK_M0 [19]

1A14 GMAC1_TXD0_M0 [19]

B15 GMAC1_TXD1_M0 [19]

B16 GMAC1_TXCTL_M0 [19]

1A16 GMAC1_RXD0_M0 [19]

B17 GMAC1_RXD1_M0 [19]

B18 GMAC1_RXCTL_M0 [19]

1B13 GMAC1_MDC_M0 [19]

1B15 GMAC1_MDIO_M0 [19]

1D18 GPIO2_D6_d/PWM2_CH6_M2 [23]

1E15 MIPI_DPHY_CSI2_CAM_CLKOUT [21]

R1923 0R R0201

R1918 NC/0R R0201

GMAC1_MCLKINOUT_M0 [19]

PWM2_CH7_M2/SPDIF_TX0_M2 [23]

GPIO3_A0_D [23]

1D16 GMAC0_INT/PMEB [18]

1B18 MIPI_DPHY_CSI4_CAM_CLKOUT [21]

1A20 GPIO3_A3_D

1A19 GMAC1_RSTn [19]

R1919 0R R0201

VCC_3V3_S0

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d
PWM1_CH3_M3	--	SPI2_CSN0_M2	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_RXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDOE15	VO_LCDC_D15	GPIO3_B4_d
PWM0_CH1_M3	--	SPI3_CSN0_M1	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDOE14	VO_LCDC_D14	GPIO3_B5_d
--	--	--	--	--	--	FLEXBUS0_D9	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDOE13	VO_LCDC_D13	GPIO3_B6_d
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDOE12	VO_LCDC_D12	GPIO3_B7_d
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDOE11	VO_LCDC_D11	GPIO3_C0_d
CAN0_RX_M3	I2C3_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH0_PTP_REFCLK_M0	VO_EBC_SDDOE10	VO_LCDC_D10	GPIO3_C1_d
PWM3_CH0_M3	I2C3_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D7	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDOE9	VO_LCDC_D9	GPIO3_C2_d
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDOE8	VO_LCDC_D8	GPIO3_C3_d
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D6	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDOE7	VO_LCDC_D7	GPIO3_C4_d
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D5	DSMC_DATA4	SAI1_LRCK_M1	--	VO_EBC_SDDOE6	VO_LCDC_D6	GPIO3_C5_d
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D4	DSMC_DATA3	SAI1_SCLK_M1	--	VO_EBC_SDDOE4	VO_LCDC_D5	GPIO3_C6_d
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA2	SAI1_MCLK_M1	--	VO_EBC_SDDOE3	VO_LCDC_D4	GPIO3_C7_d
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D2	DSMC_DATA1	SAI1_MCLK_M2	--	VO_EBC_SDDOE2	VO_LCDC_D3	GPIO3_D0_d
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	UART4_TX_M2	--	FLEXBUS0_CSN_M2	FLEXBUS1_D13_M0	DSMC_CSN1	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDOE1	VO_LCDC_D2	GPIO3_D1_d
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART4_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D13_M1	FLEXBUS0_D12	DSMC_CSN0	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDOE0	VO_LCDC_D1	GPIO3_D2_d
PWM2_CH5_M3	I3C1_SCL_M2	--	UART4_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDOE0	VO_LCDC_D0	GPIO3_D3_d
--	I2C5_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d
--	I2C5_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKP	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS0_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS1_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d

RK3576
BGA698_16R1X17R2X1R18

VCCIO5_VCC_0
VCCIO5_VCC_1

2A4
2A5

C1902 NC/100nF/10V C0201

C1903 1uF/10V C0201

VCCIO_1V8_S0

1D13 PWM_CH0_M3/GPIO3_A4_1V8 [23]

A9 GMAC0_MDIO_M0 [18]

1A7 GMAC0_MDC_M0 [18]

B13 GMAC0_RXCTL_M0 [18]

B14 GPIO3_B0_D_1V8 [23]

R1920 NC/0R R0201

1A11 GMAC0_MCLKINOUT_M0 [18]

A13 GMAC0_RXD1_M0 [18]

A11 GMAC0_RXD0_M0 [18]

B10 GMAC0_TXCTL_M0 [18]

1A9 GMAC0_TXD1_M0 [18]

B11 GMAC0_TXD0_M0 [18]

1D12 GMAC0_TXCLK_M0 [18]

I2C4_SDA_M3_MIPI_CSI3 [21,23]

1E9 I2C4_SCL_M3_MIPI_CSI3 [21,23]

1B10 I2C5_SDA_M3_MIPI_CSI1 [21]

B9 GMAC0_TXD3_M0 [18]

1A8 GMAC0_TXD2_M0 [18]

1D9 I2C5_SCL_M3_MIPI_CSI1 [21]

1B9 MIPI_DPHY_CSI3/4_RST [21]

1D7 MIPI_DPHY_CSI1/2_RST [21]

1C7 MIPI_DPHY_CSI2_PDN_H [21]

R1921 0R R0201

1C12 GPIO3_C7_D_1V8 [23]

1A12 MIPI_DPHY_CSI1_PDN_H [21]

1A10 GMAC0_RXCLK_M0 [18]

B12 GMAC0_RXD3_M0 [18]

1E12 GMAC0_RXD2_M0 [18]

R1922 0R R0201

1D10 MIPI_DPHY_CSI3_PDN_H [21]

1C10 PCIe_PWR_EN [20]

1E7 FAN_PWM2_CH7_M3 [23]

1B12 MIPI_DPHY_CSI1_CAM_CLKOUT [21]

1B7 MIPI_DPHY_CSI3_CAM_CLKOUT [21]

R1926 2.2K R0201

R1927 2.2K R0201

I2C4_SDA_M3_MIPI_CSI3

I2C4_SCL_M3_MIPI_CSI3

R1934 2.2K R0201

R1935 2.2K R0201

I2C5_SDA_M3_MIPI_CSI1

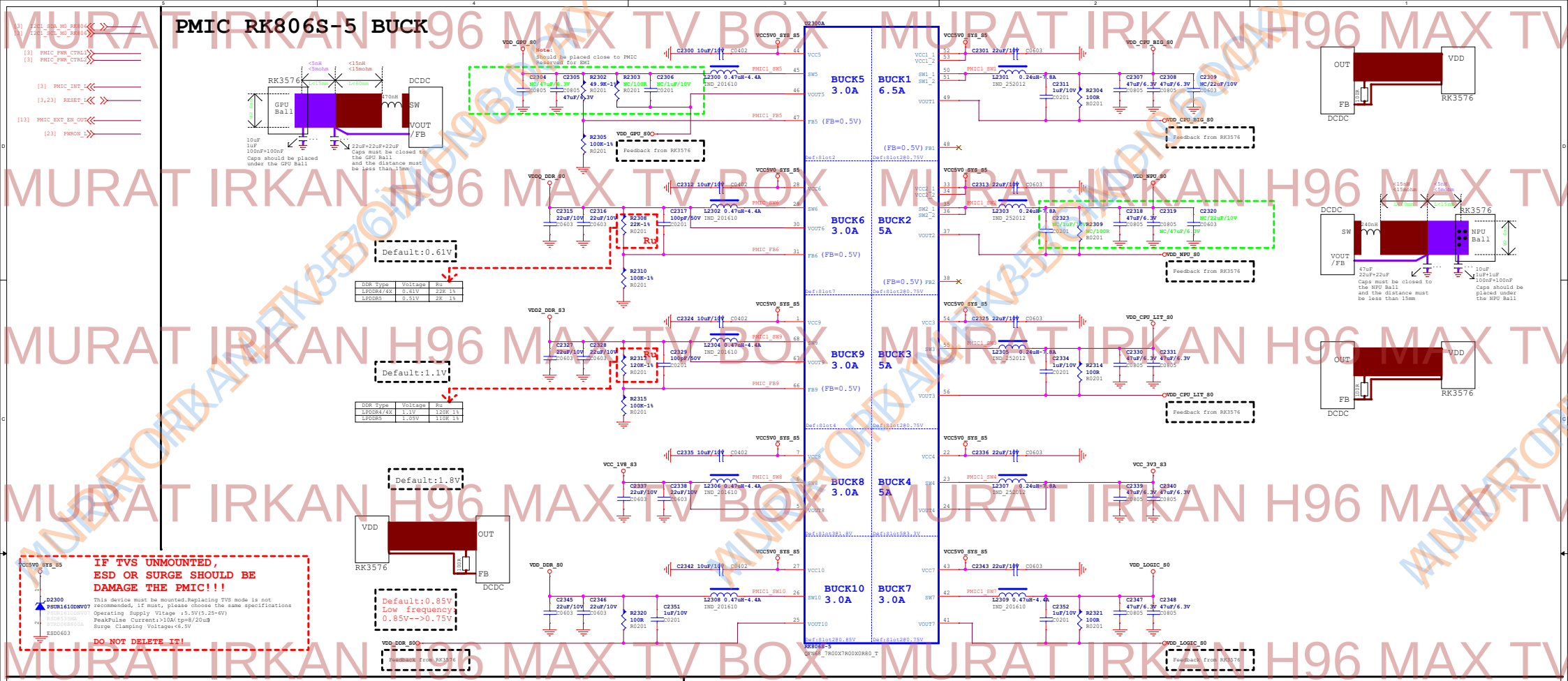
I2C5_SCL_M3_MIPI_CSI1

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

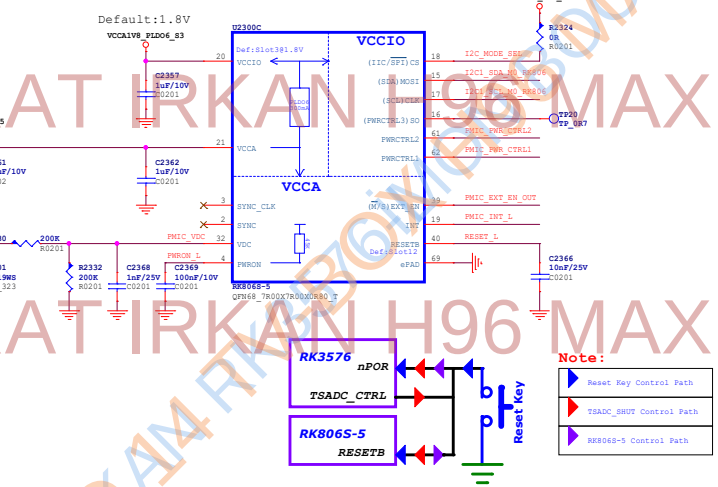
armsom	https://armsom.org/			
Project:	ArmSoM-Sige5			
File:	RK3576-GPIO VCCIO4/5			
Date:	Wednesday, May 22, 2024		Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	11 of 25

PMIC RK806S-5 BUCK



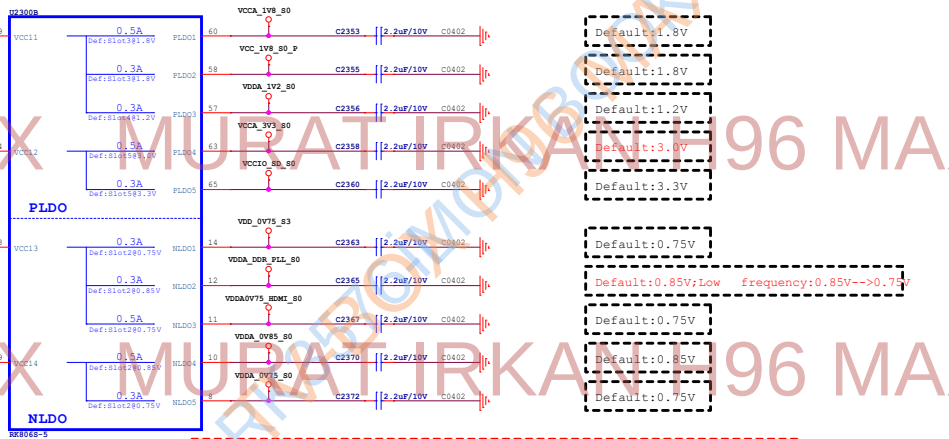
PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806S-5 Control Path

PMIC RK806S-5 LDO



Default:1.8V
Default:1.2V
Default:3.0V
Default:3.3V
Default:0.75V
Default:0.85V;Low frequency:0.85V-->0.75V
Default:0.75V
Default:0.85V
Default:0.75V

Note:
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	Power-PMIC RK806S-5
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
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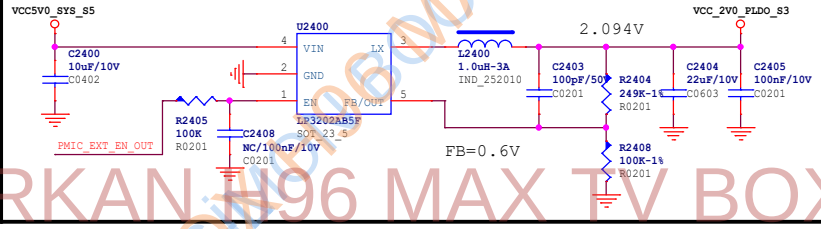
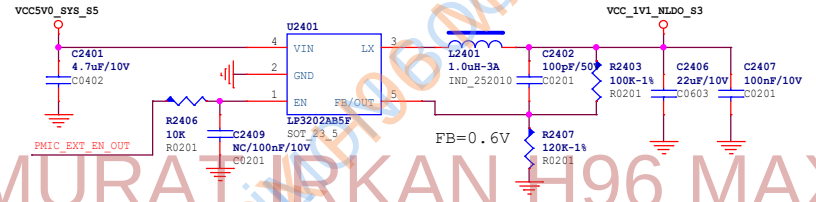
[5,22] I2C2_SCL_M0_CC_RTC
[5,22] I2C2_SDA_M0_CC_RTC
[3] RTC_INT_L
[3] 32KOUT_RTC2SOC
[17] 32KOUT_RTC2WIFI
[12] PMIC_EXT_EN_OUT

VCC_2V0_PLDO_S3

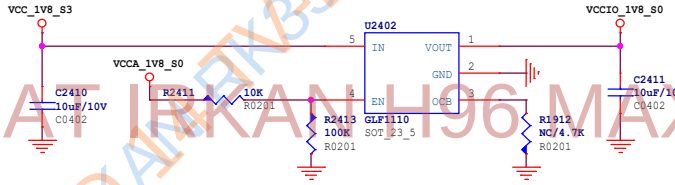


VCC_1V1_NLDO_S3



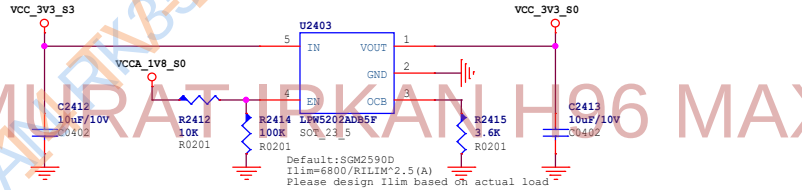
VCCIO_1V8_S0

Note: Need quick output discharge

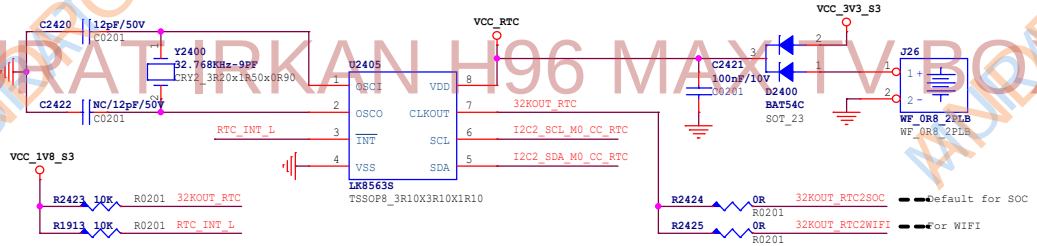


VCC_3V3_S0

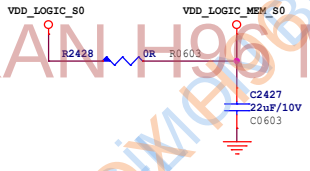
Note: Need quick output discharge



RTC



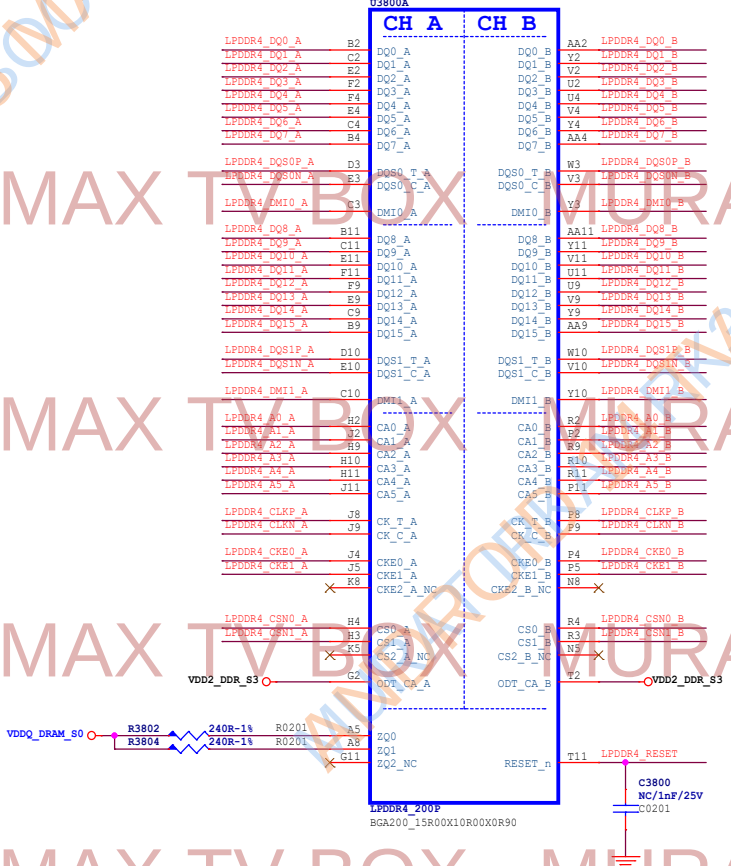
VDD_LOGIC_MEM EXT(Option for test)

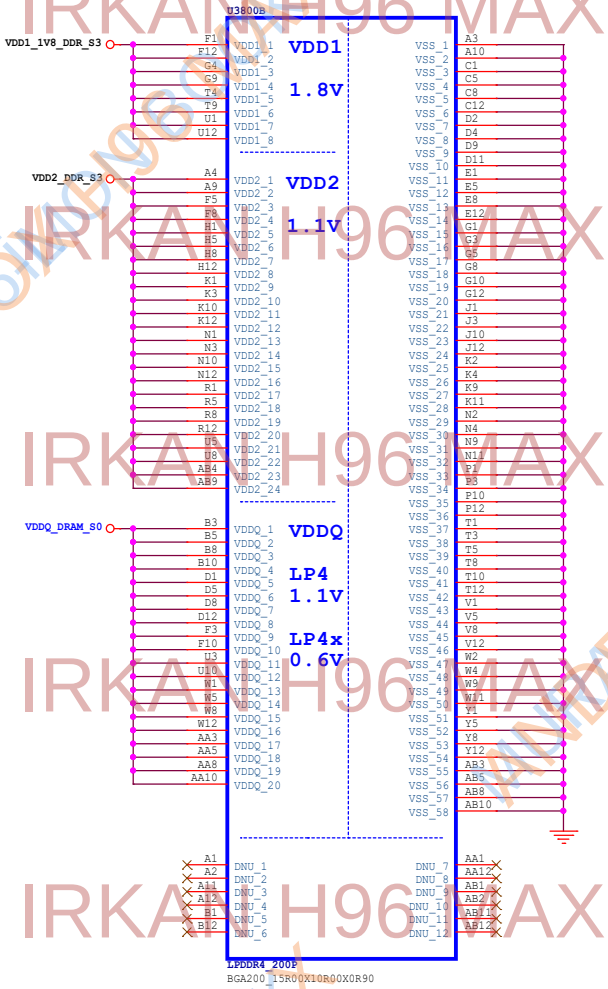


armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	Power-Ext Discrete/RTC				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	13 of 25

LPDDR4/4X

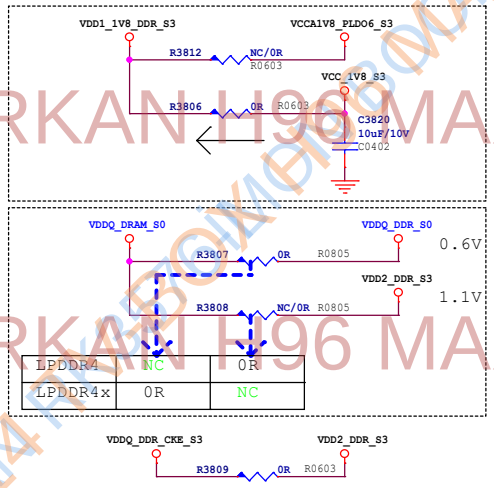


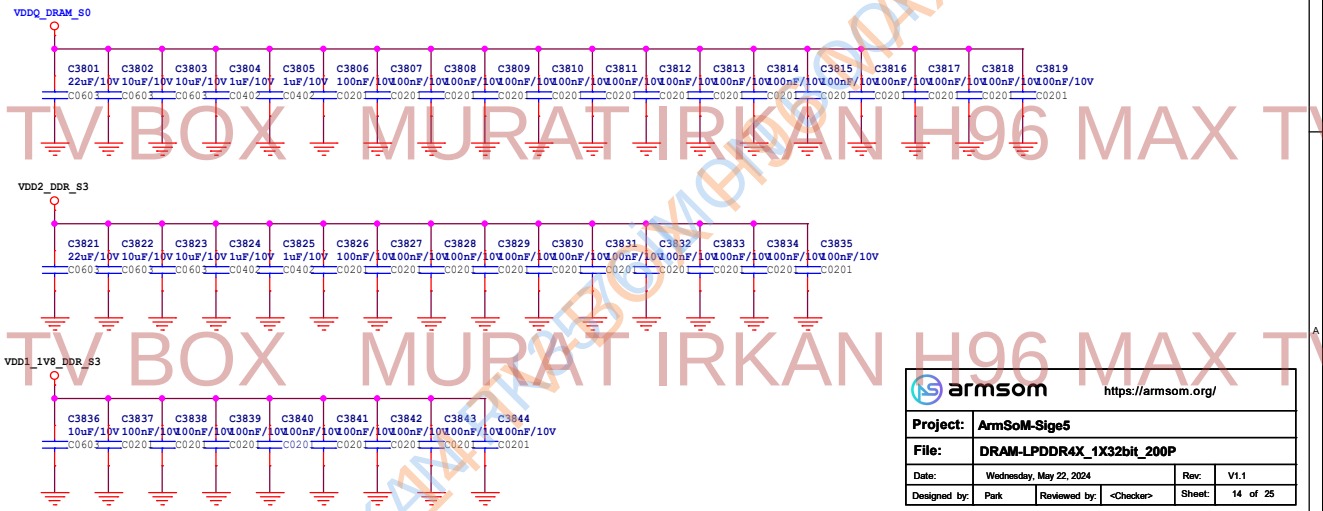


Note:

Sequence:VDD1-VDD2-VDDQ

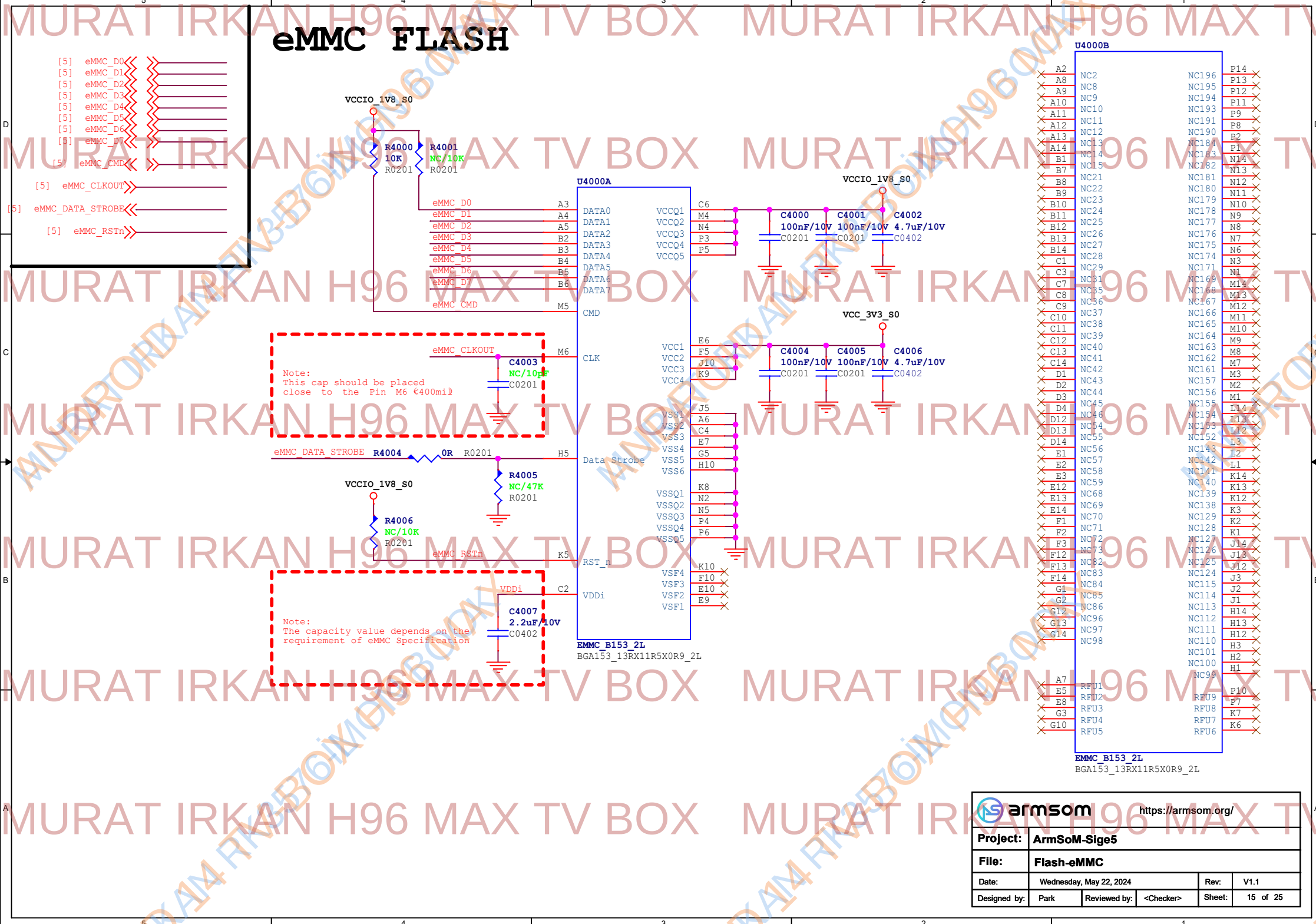
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65





armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	DRAM-LPDDR4X_1X32bit_200P		
Date:	Wednesday, May 22, 2024	Rev:	V1.1
Designed by: Park	Reviewed by: <Checker>	Sheet:	14 of 25

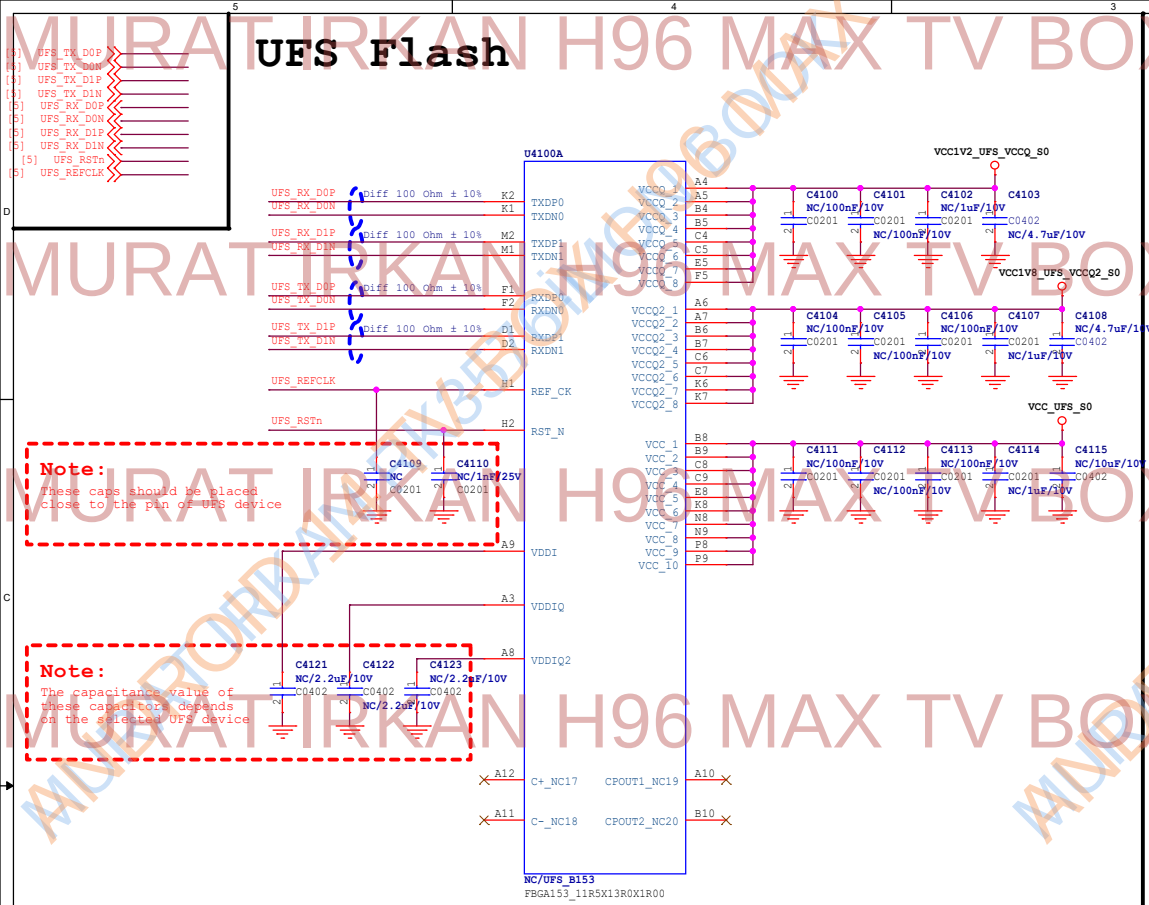
eMMC FLASH



armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	Flash-eMMC				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 25

UFS Flash



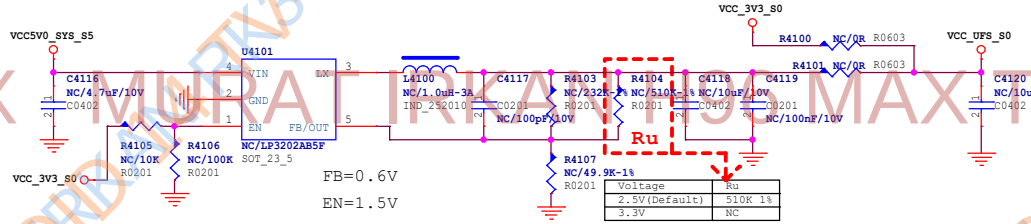
UFS POWER

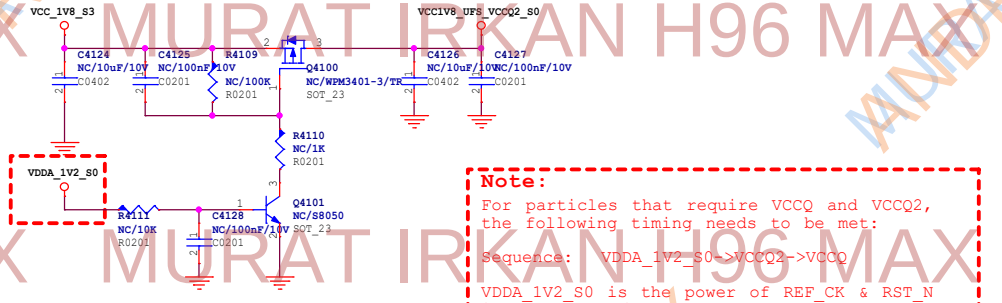
	VCCQ	VCCQ2	VCC
UFS2.0	1.2V	1.8V	3.3V
UFS2.1	No Connect	1.8V	3.3V
UFS2.2	No Connect	1.8V	3.3V
UFS3.0	1.2V	No Connect	2.5V/3.3V
UFS3.1	1.2V	No Connect	2.5V/3.3V
UFS4.0	1.2V	No Connect	2.5V

Default UFS device: UFS2.2

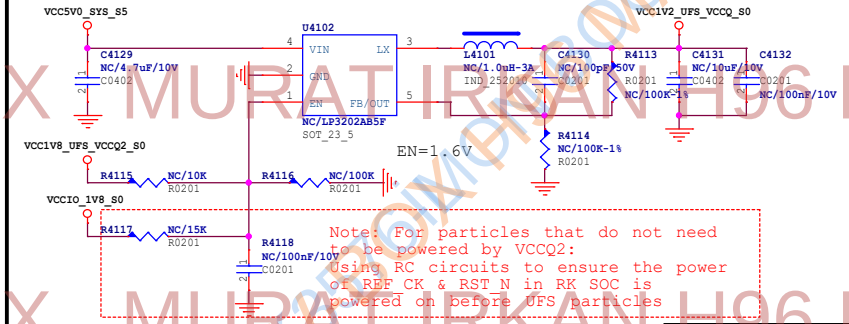
Sequence: VCCQ2->VCCQ, VCC is independent

Note: Do not support UFS4.0 Device!
The power ball that is not used at the particle must be kept floating.



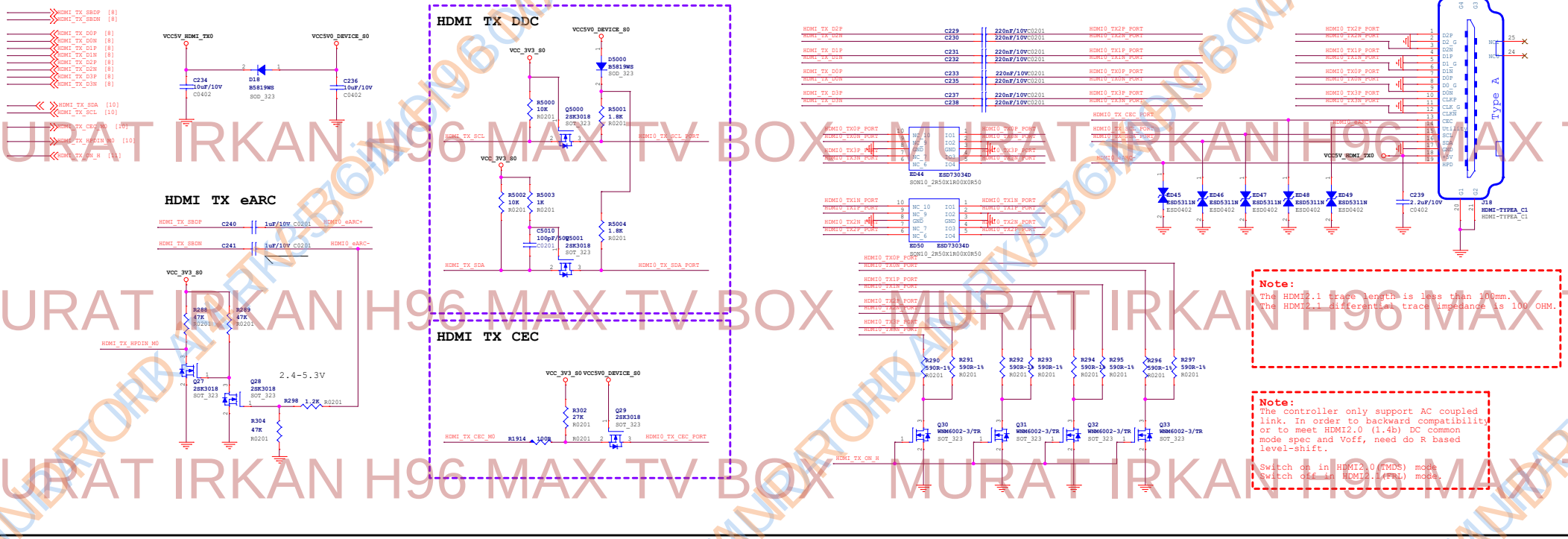


Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:
Sequence: VDDA_1V2_S0->VCCQ2->VCCQ
VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles



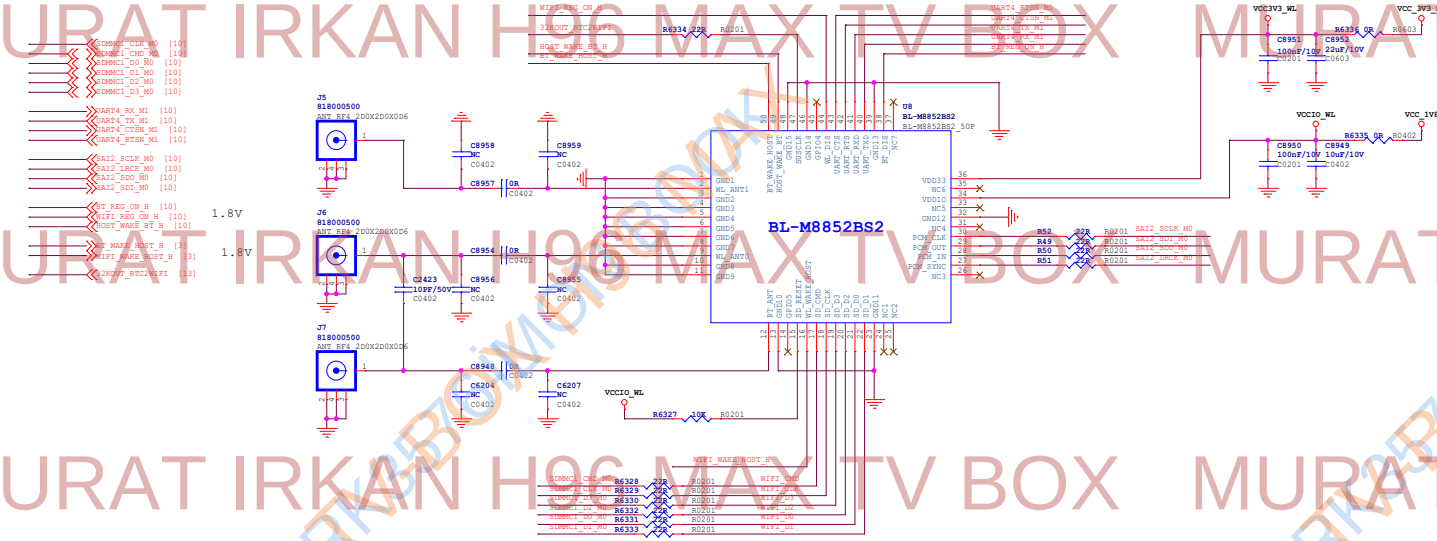
armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	Flash-UFS				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 25

HDMI TX0



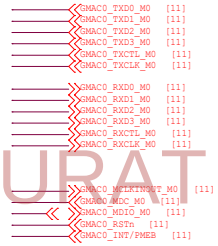
SDIO WIFI6/BT Module-2T2R

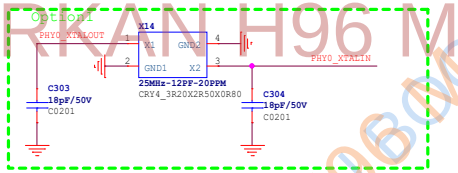
VBAT:(3.1-3.5V)/1.0A
VDDIO:(1.70-1.90V)/300mA.

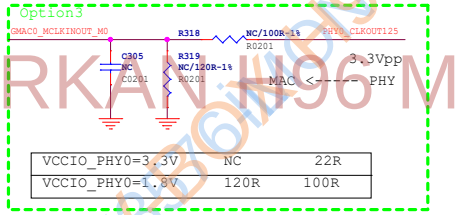


armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	HDMI_TX0_WIFI
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	17 of 25

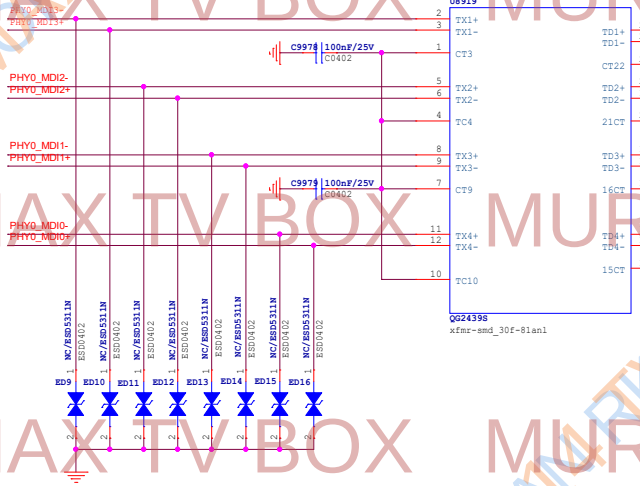
GPHY To JR45

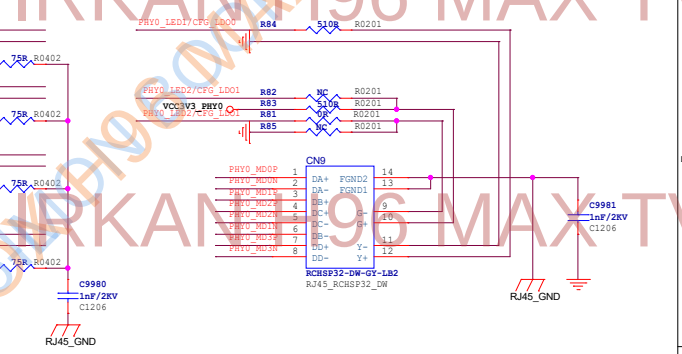


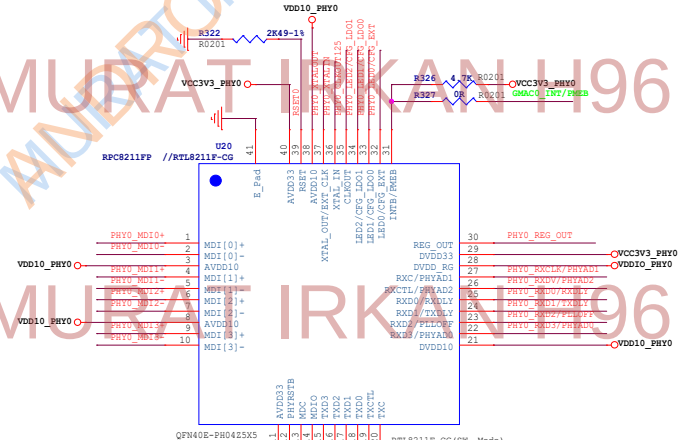


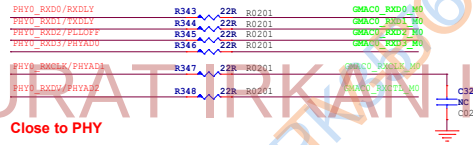


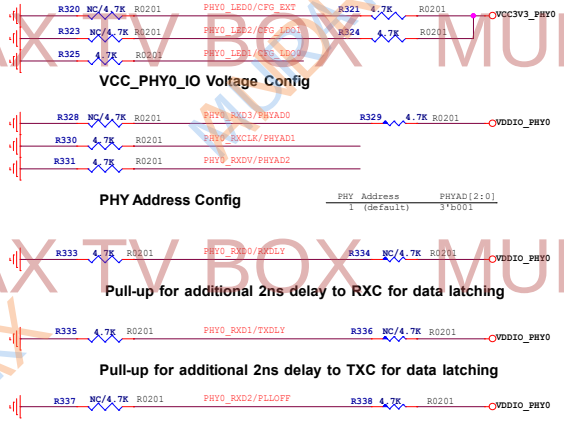
RK SOC clock mode recommended	
RK3576	mode1

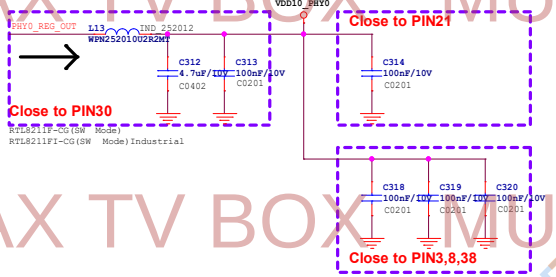


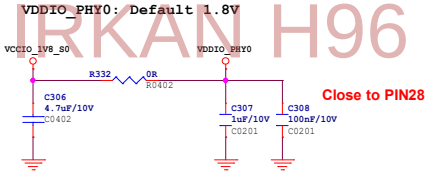


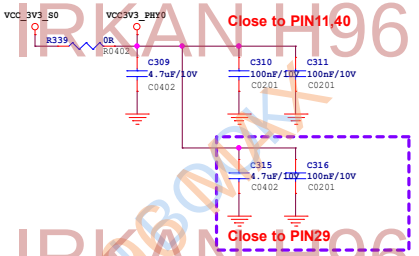






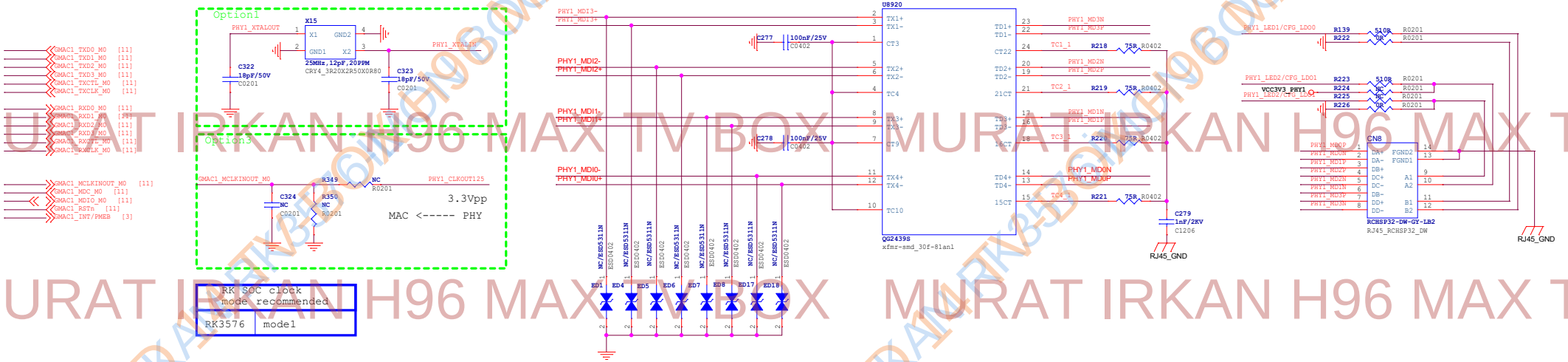


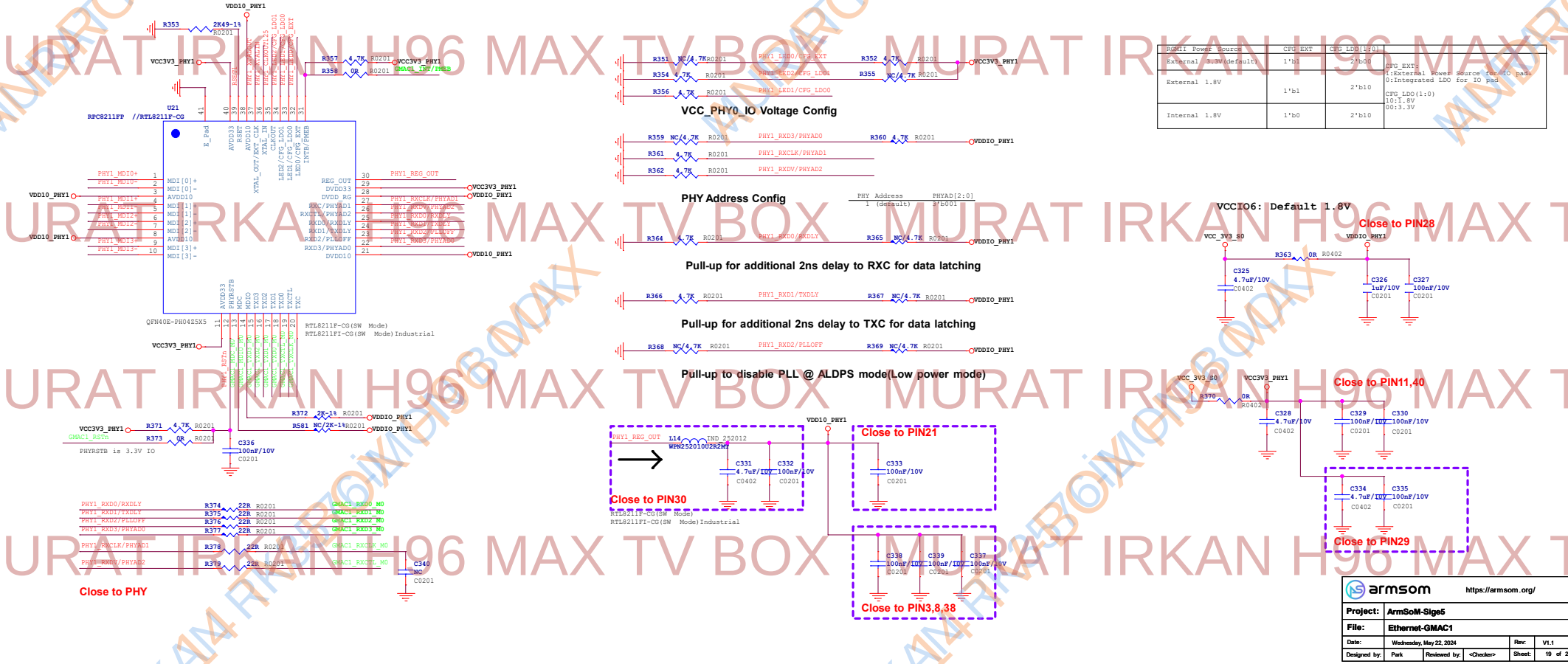




armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	Ethernet-GPHY		
Date:	Wednesday, May 22, 2024	Rev:	V1.1
Designed by: Park	Reviewed by: <Checker>	Sheet:	18 of 25

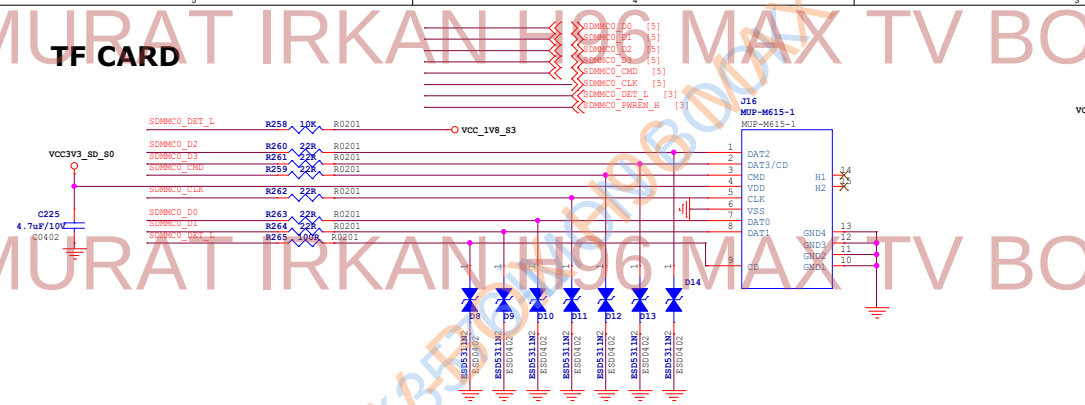
Giga PHY1_WAN

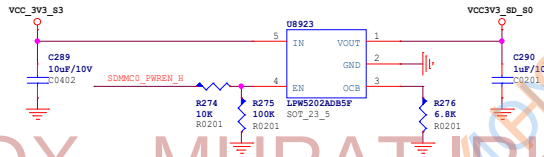




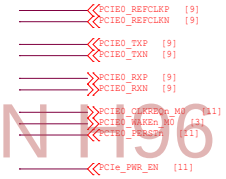
armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	Ethernet-GMAC1
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	19 of 25

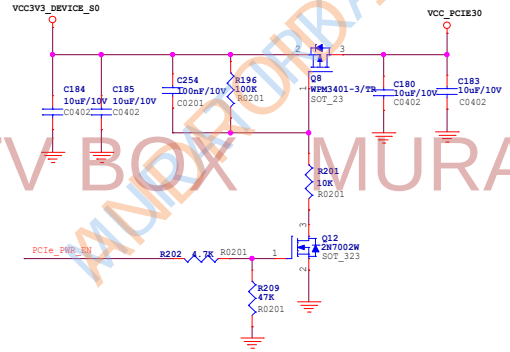
TF CARD

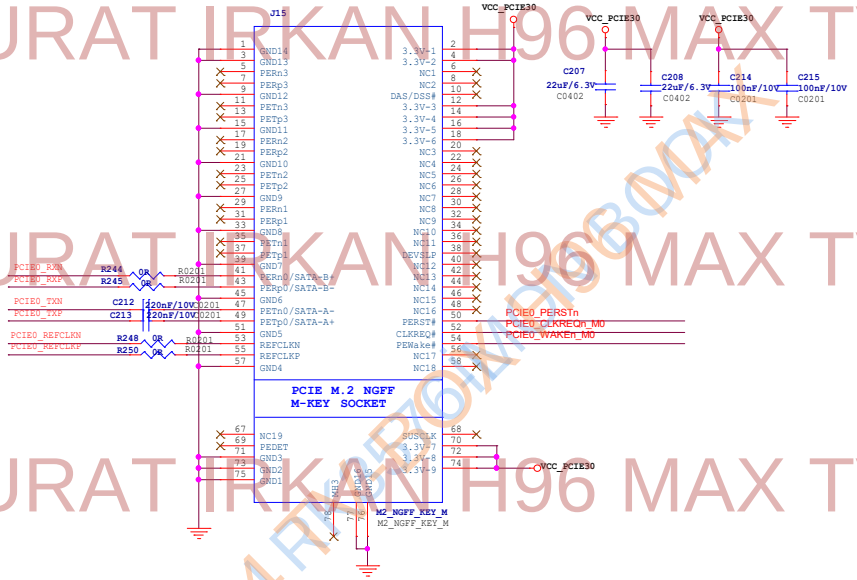




M.2_PCIE

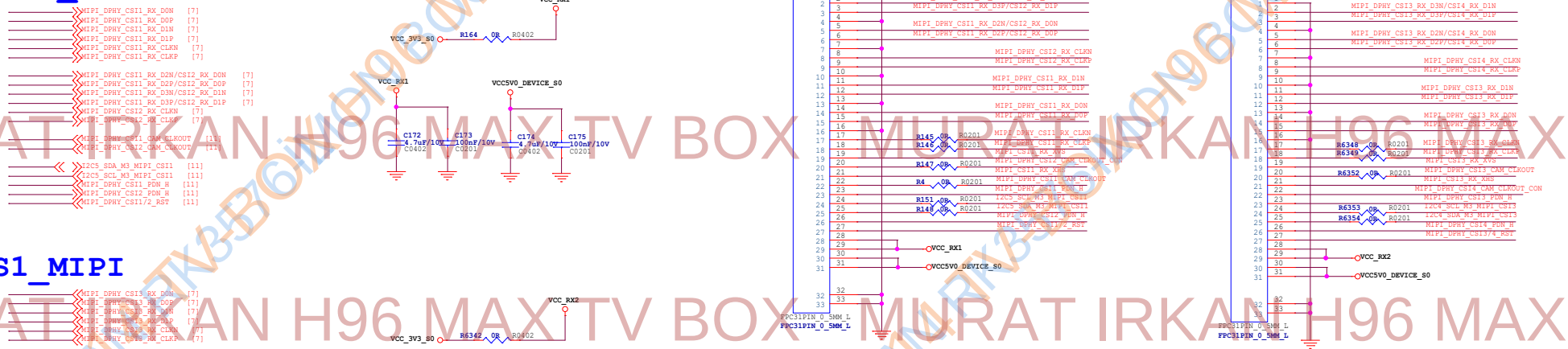






armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	M2_TF		
Date:	Wednesday, May 22, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 20 of 25

CSI0_MIPI



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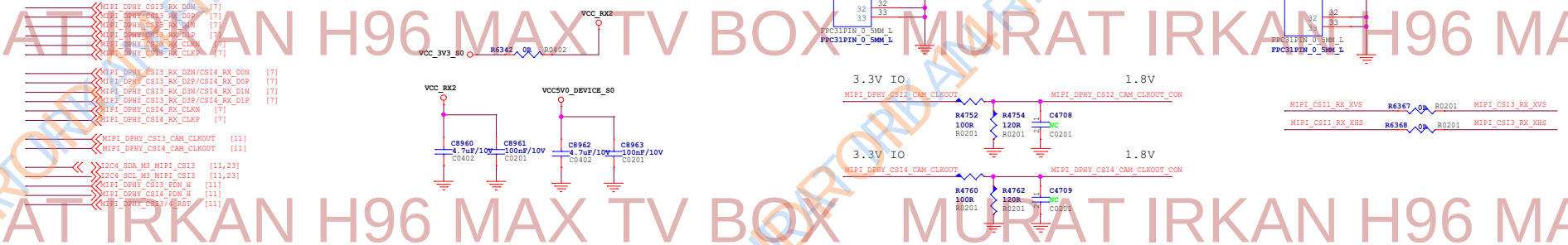
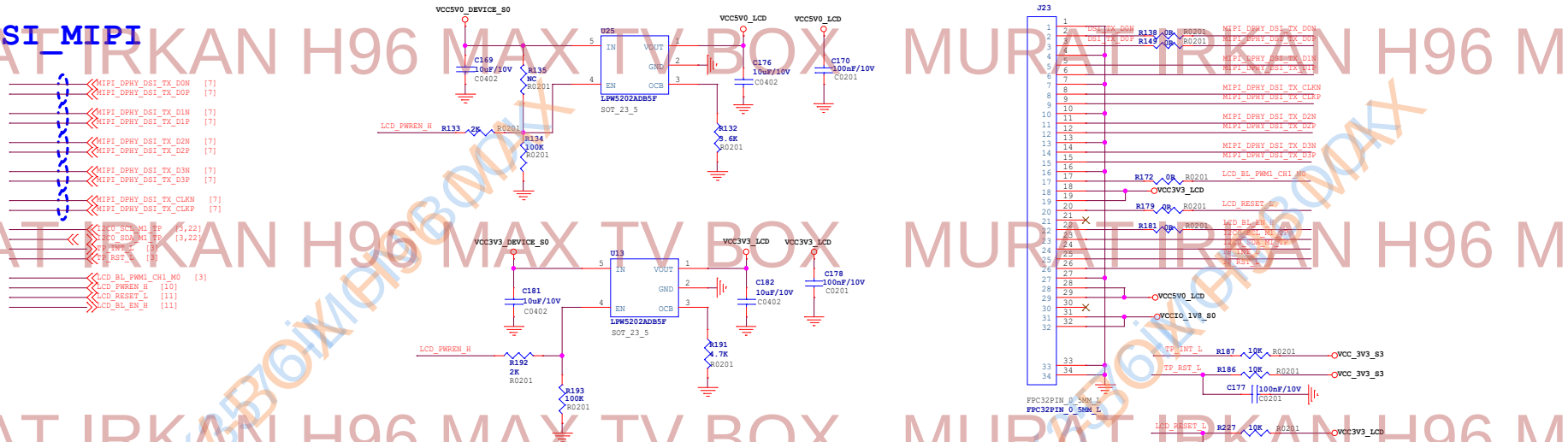
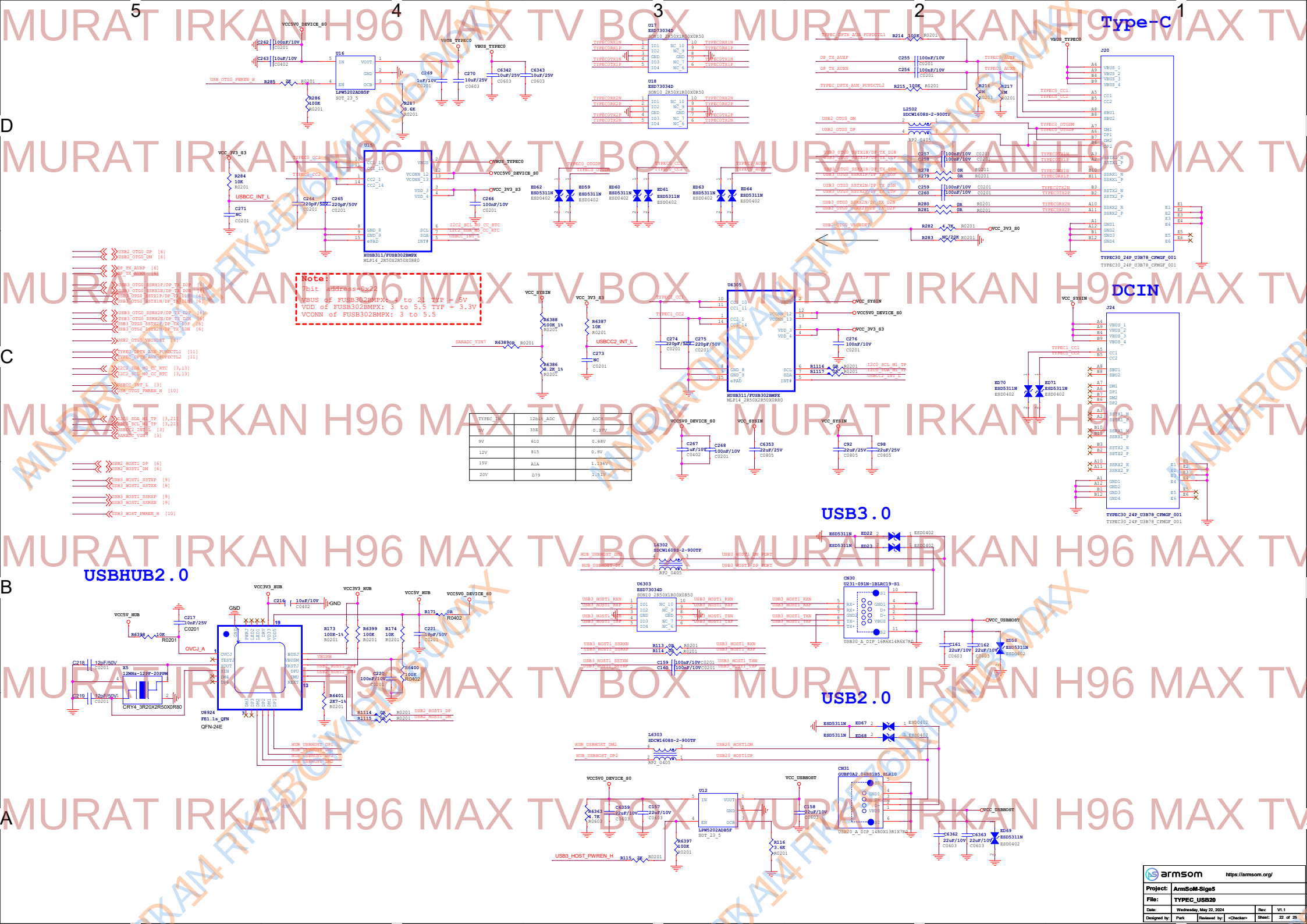


DSI_MIPI



armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	MIPI_RX_CSI/MIPI_DSI				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	21 of 25



KEY

PWR_KEY

RESET_Key

MASKROM_Key

AUDIO CODEC

FAN

40PIN_GPIO

RGB LED

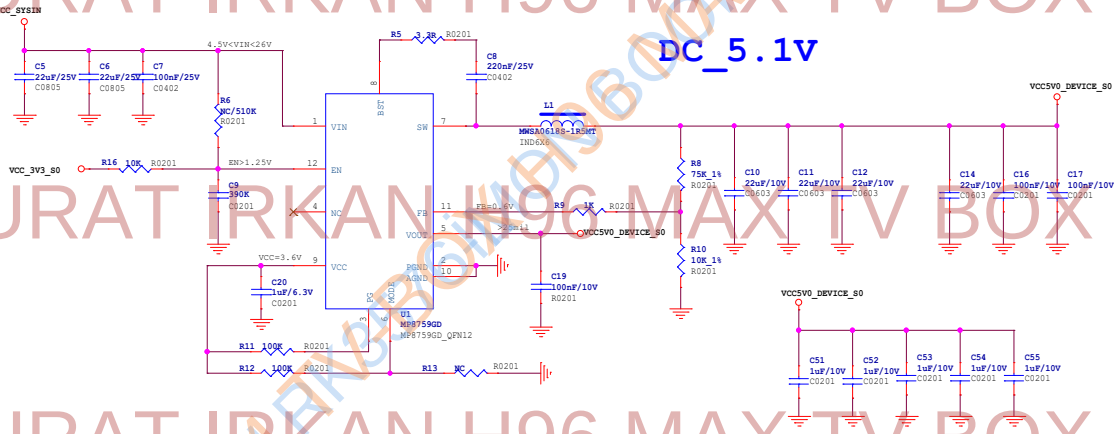
CHOOSE ONE

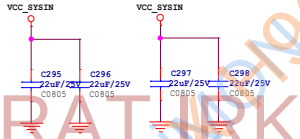
Differential routing

7_bit Address:
Addr(CE) = H -->0x11
Addr(CE) = L -->0x10

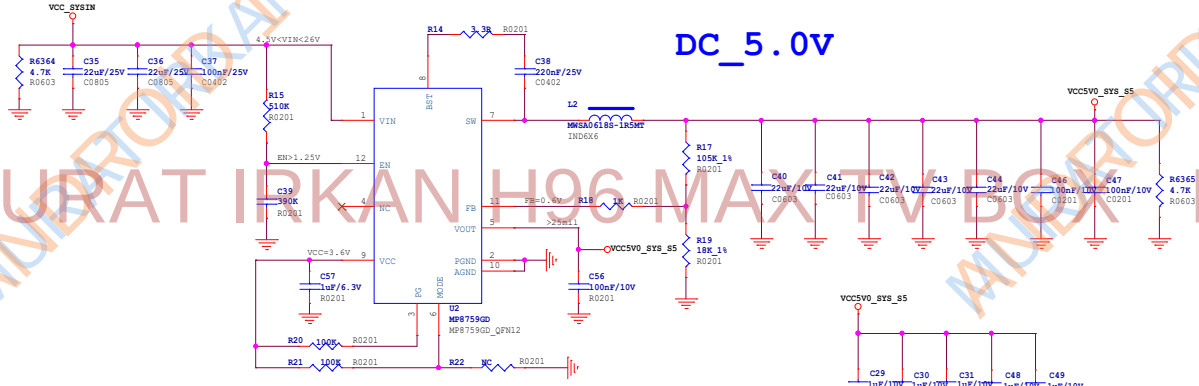
armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	Audio_40PIN
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	23 of 25

DC_5.1V

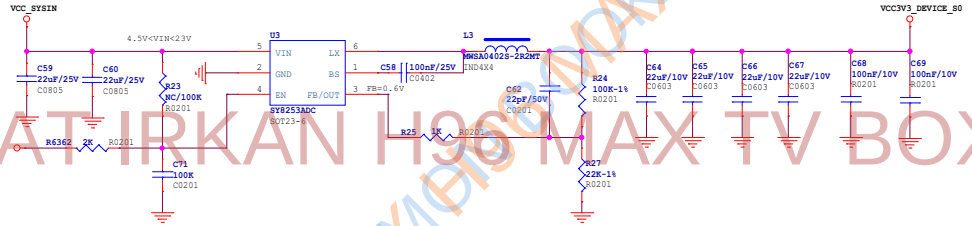


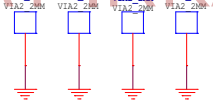


DC_5.0V



DC_3.3V





armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	Power				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	24 of 25

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2024-03-27	SL Chen	First release;	
V1.1	2024-05-15	SL Chen	1.U1/U2 Pin5 connect to output; TF_DET_L connect to VCC_1V8_S3; J23 Pin2&Pin3 change position; 2.J25 MIPI_DPHY_CSI3_CAM_CLKOUT&MIPI_DPHY_CSI4_CAM_CLKOUT_CON change position;	

armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	Revision History				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	25 of 25