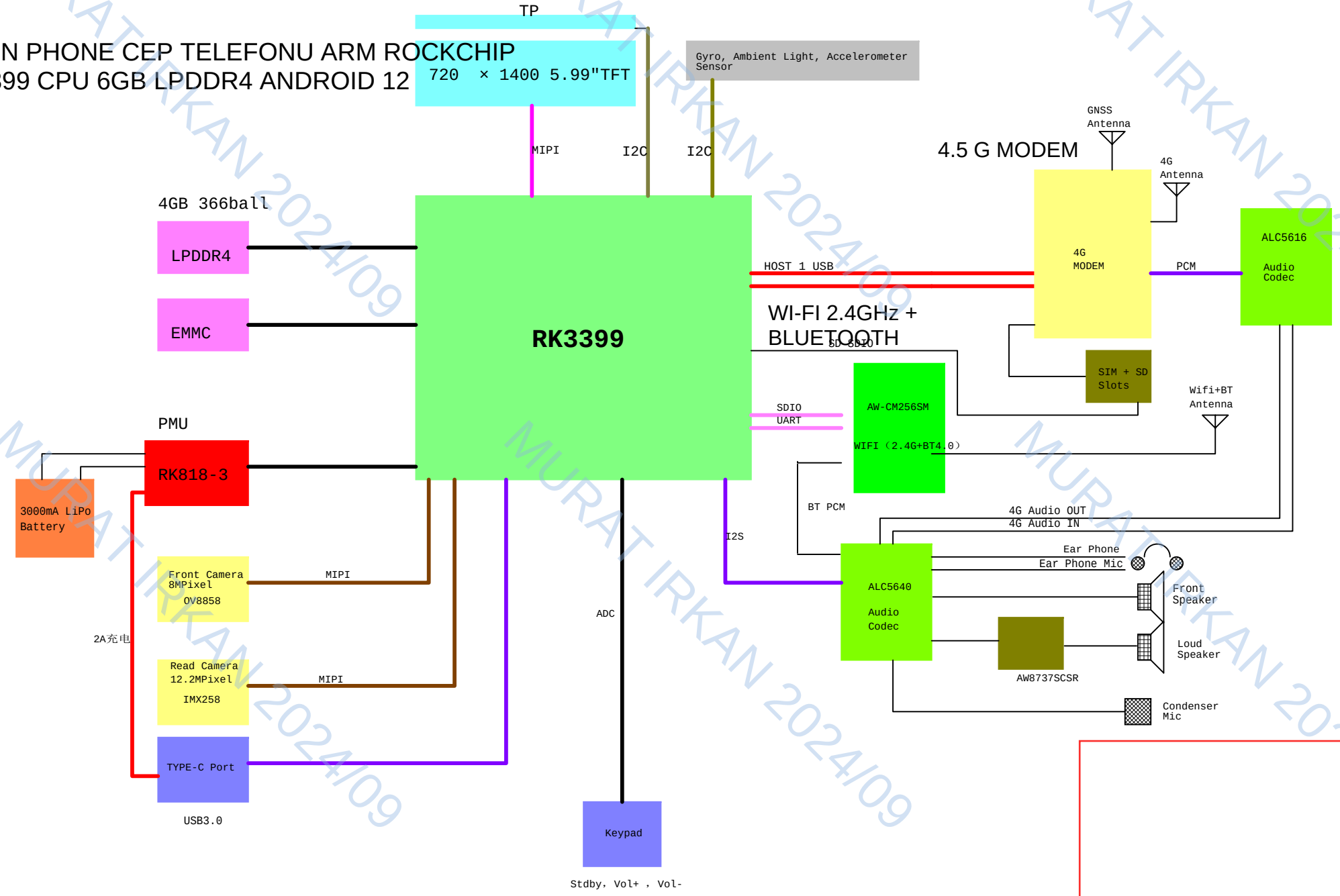
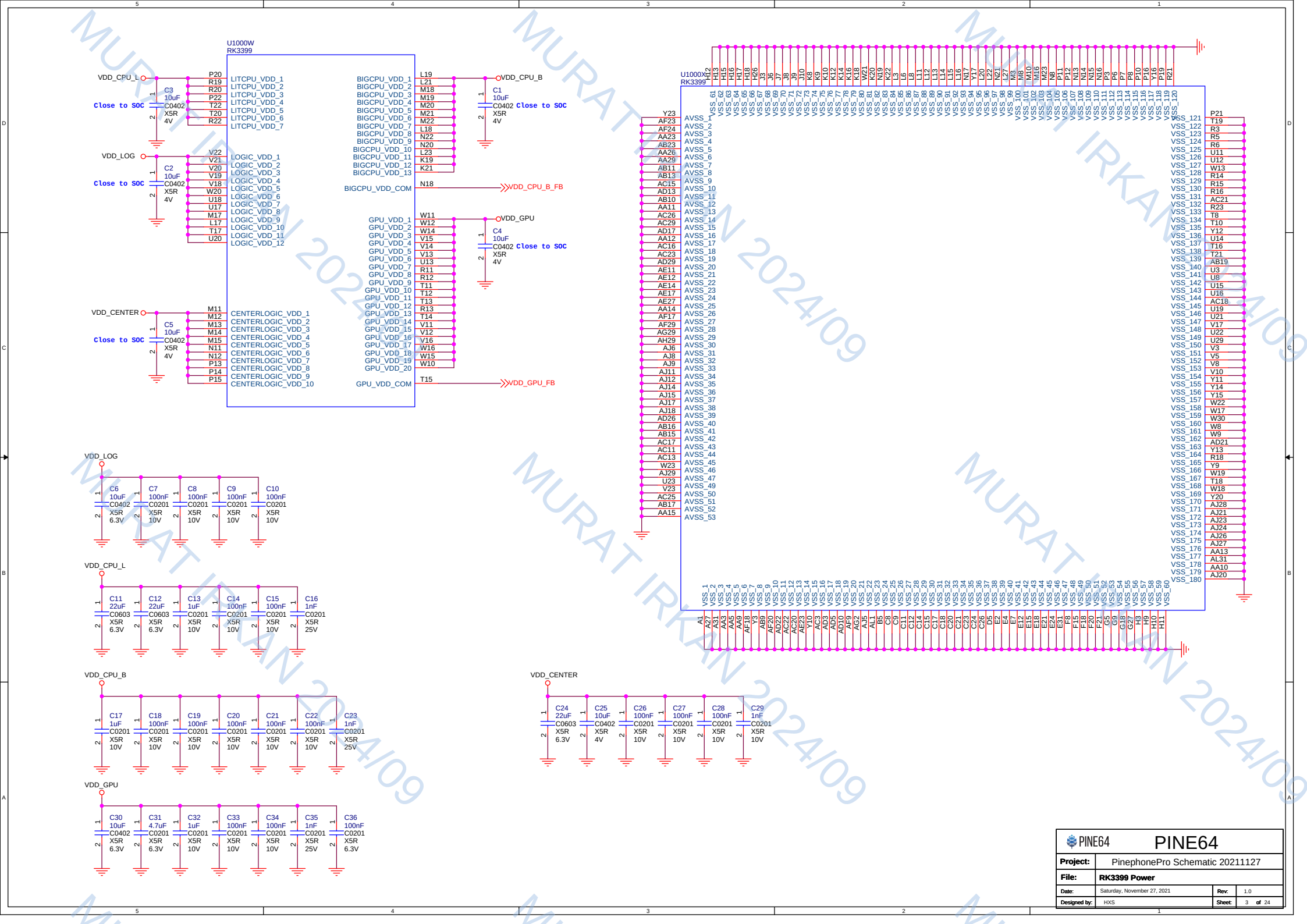
Version	Date	Author	Change Note	Approved
V0.2	20210315		Pilot Production	
V1.0	20211127		Explorer Edition	

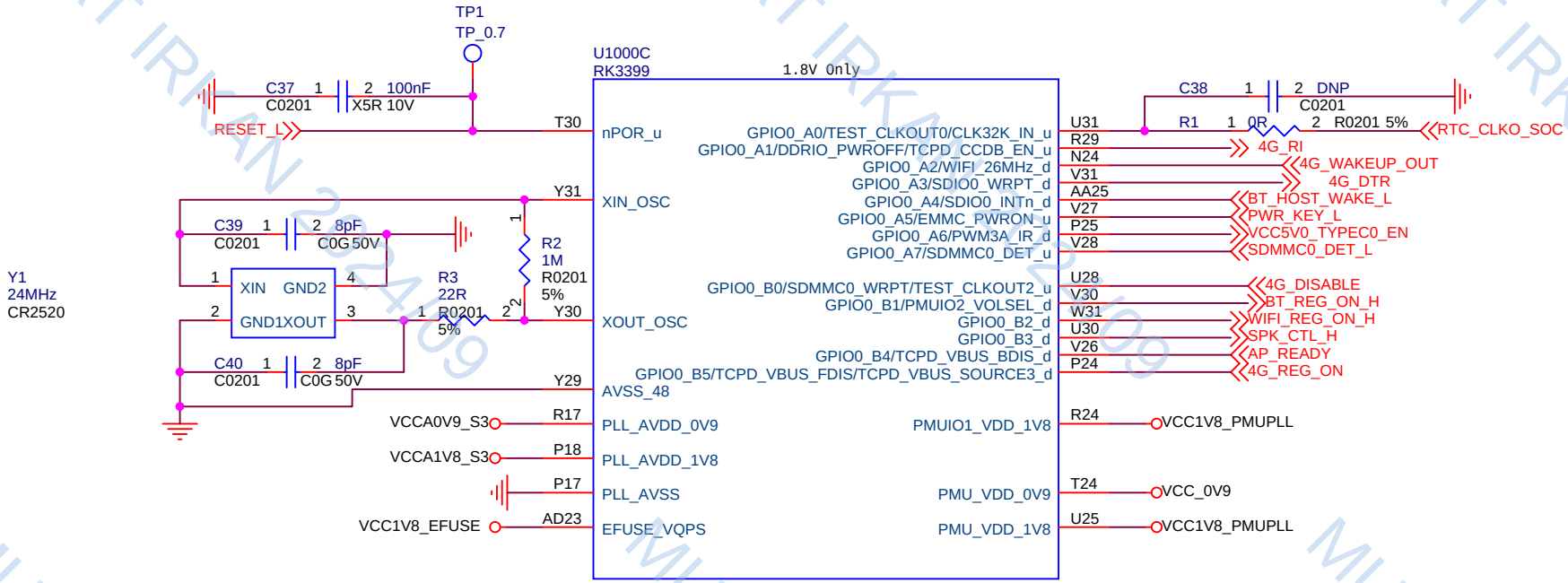
PINE64

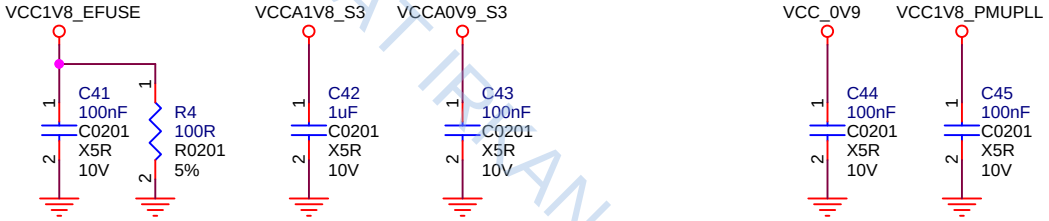
PINE64			
Project:	PinephonePro Schematic 211127		
File:	**Change List**		
Date:	Saturday, November 27, 2021	**Rev:**	02
Designed by:	HXS	**Sheet:**	1 **of** 24

LIMON PHONE CEP TELEFONU ARM ROCKCHIP RK3399 CPU 6GB LPDDR4 ANDROID 12



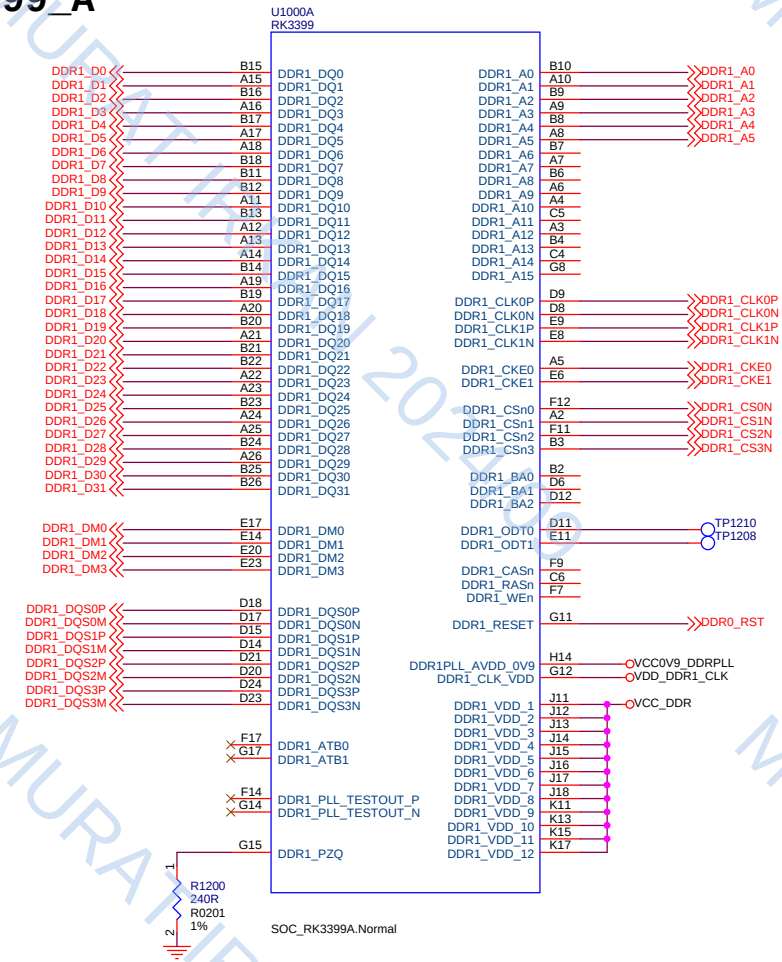




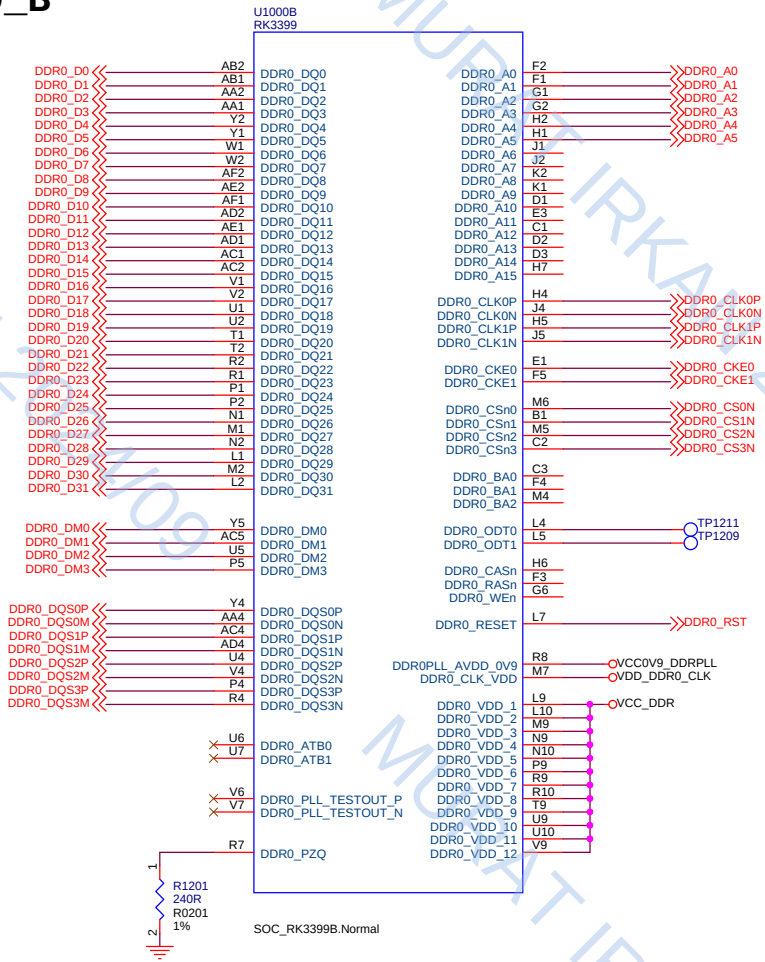


PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 PMU Controler**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	HXS	**Sheet:**	4 of 24

RK3399_A

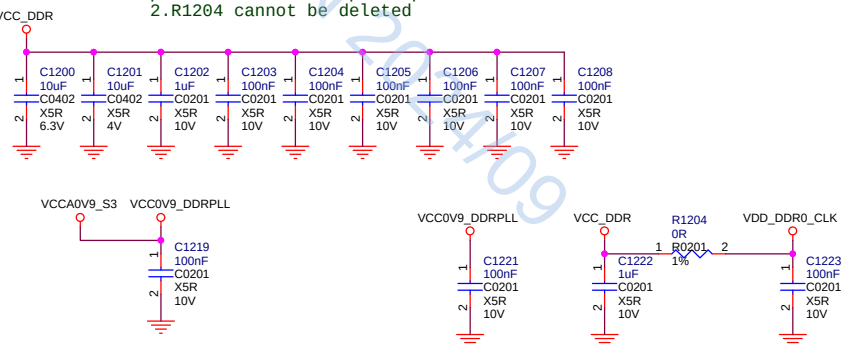


RK3399_B



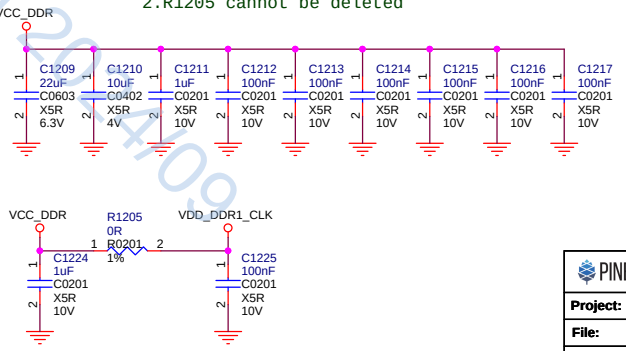
DDR FILTER

Note:
1.All the Power filter capacitor should be place close to the power pin of RK3399
2.R1204 cannot be deleted

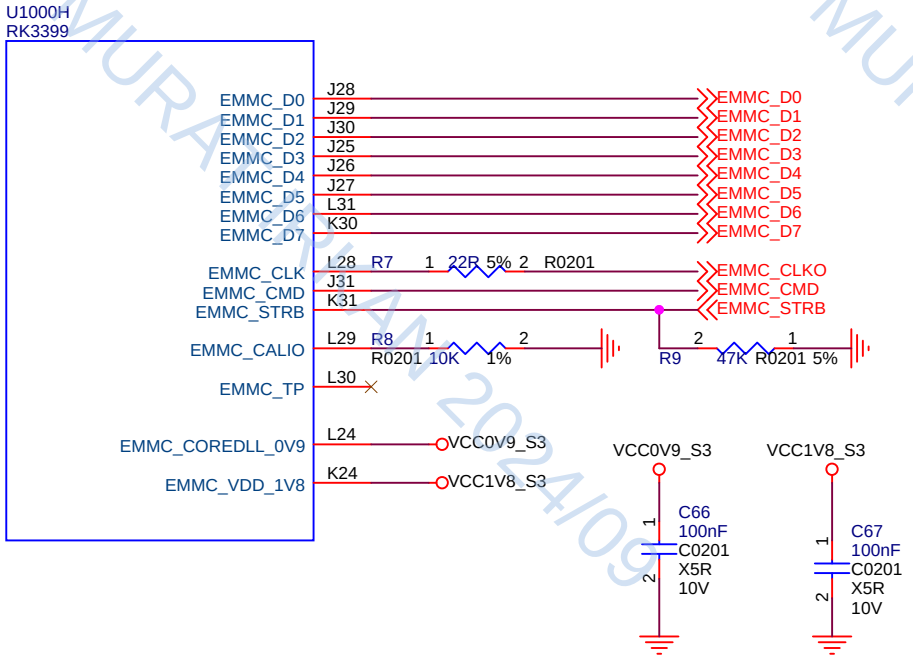


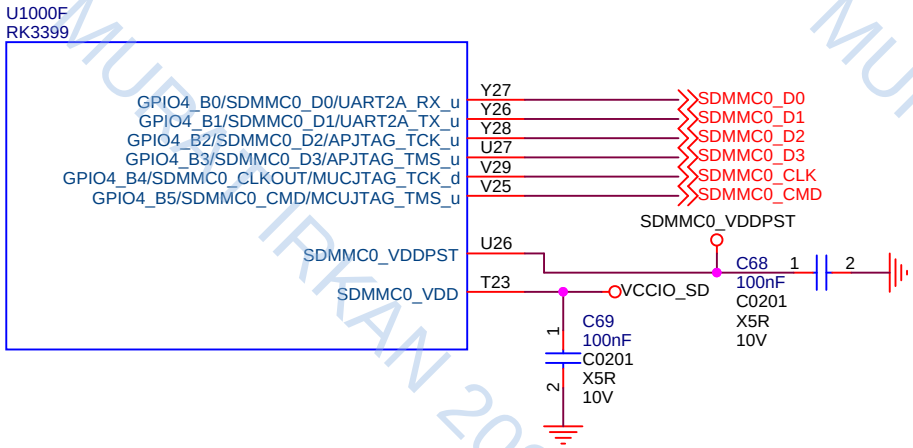
DDR FILTER

Note:
1.All the Power filter capacitor should be place close to the power pin of RK3399
2.R1205 cannot be deleted

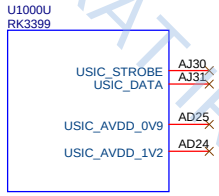


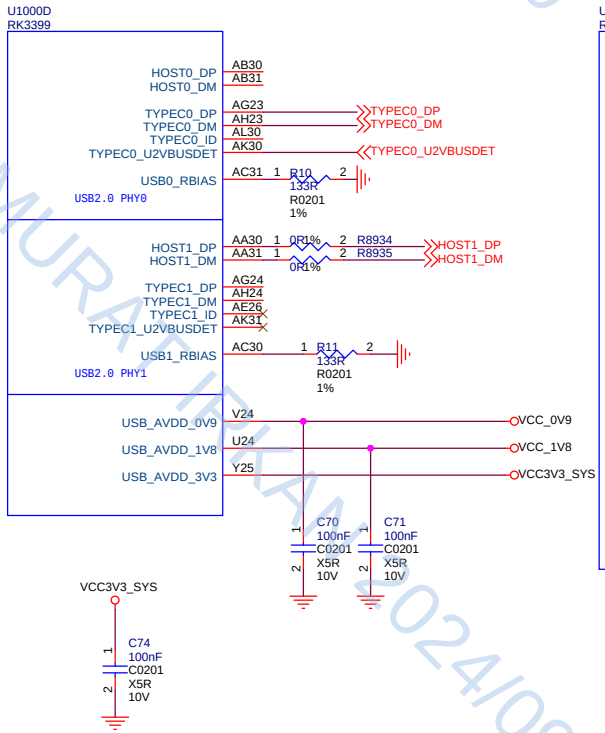
PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 DDR Controller**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	Linus	**Sheet**	5 of 24

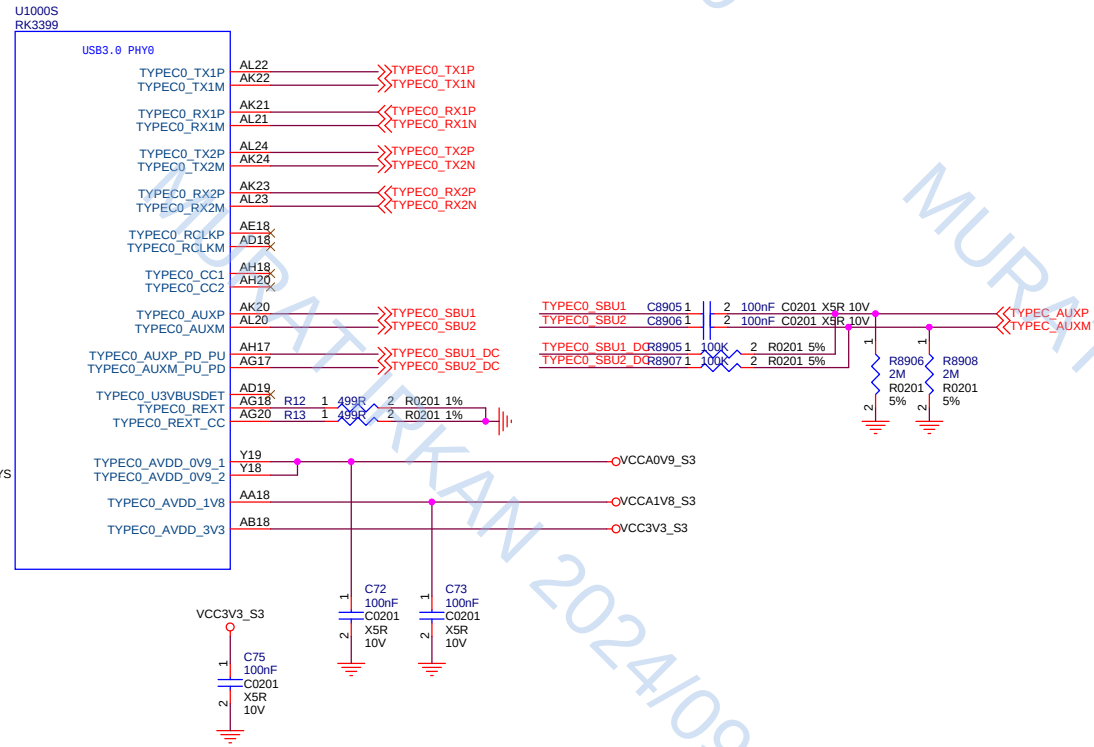


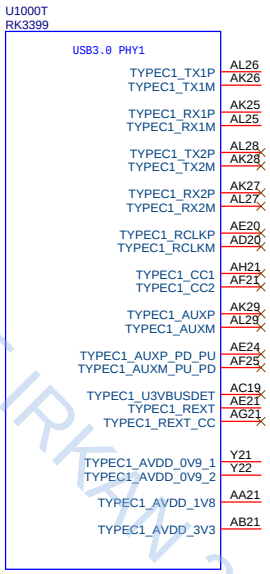


PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 Flash&SDMMC Controler**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	HXS	**Sheet:**	6 **of** 24







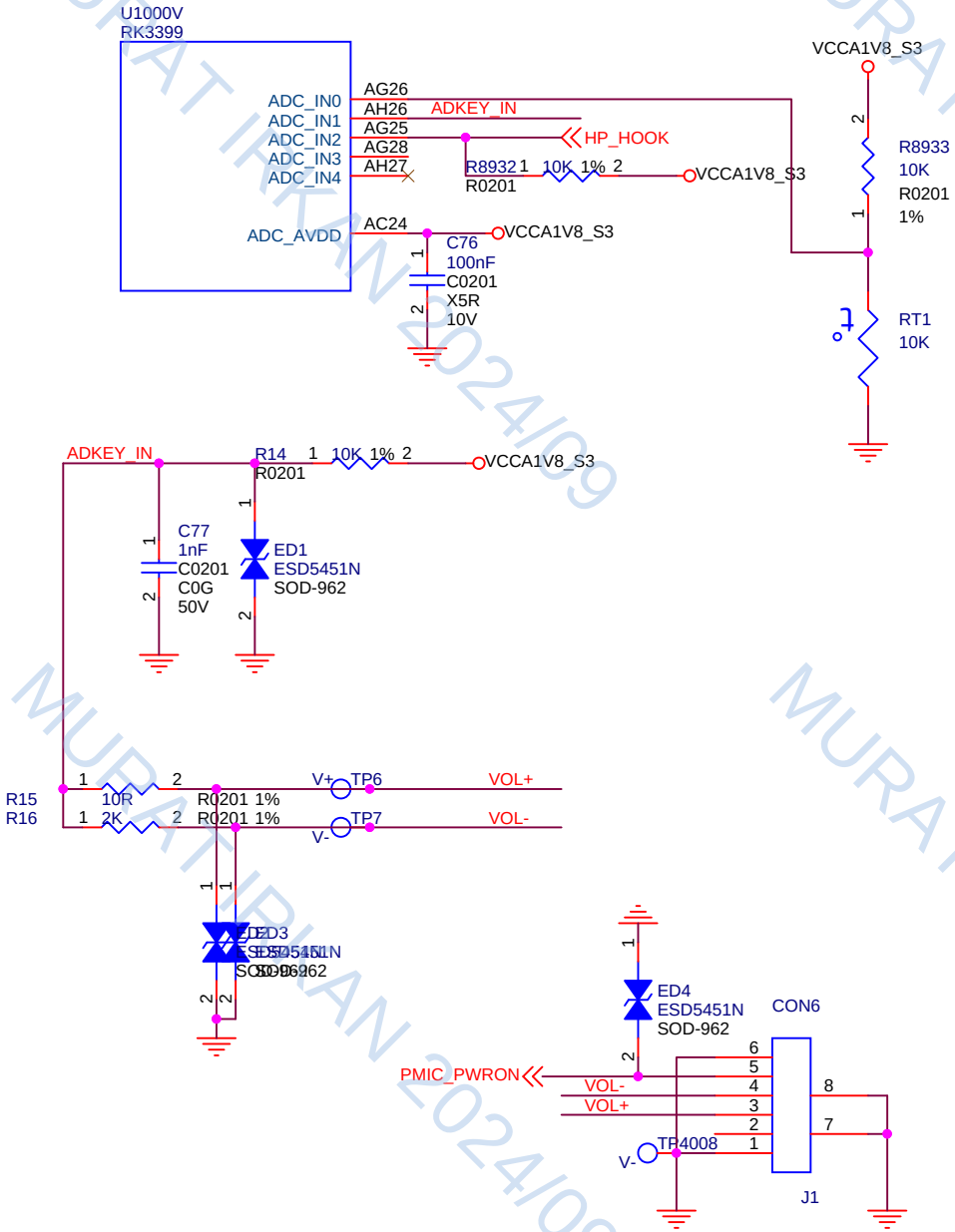


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;

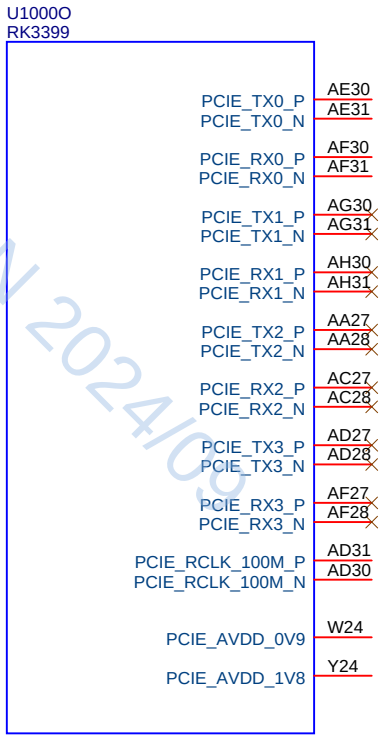
USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and RX < 1.6 ns;
3.Max trace length < 6 inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;

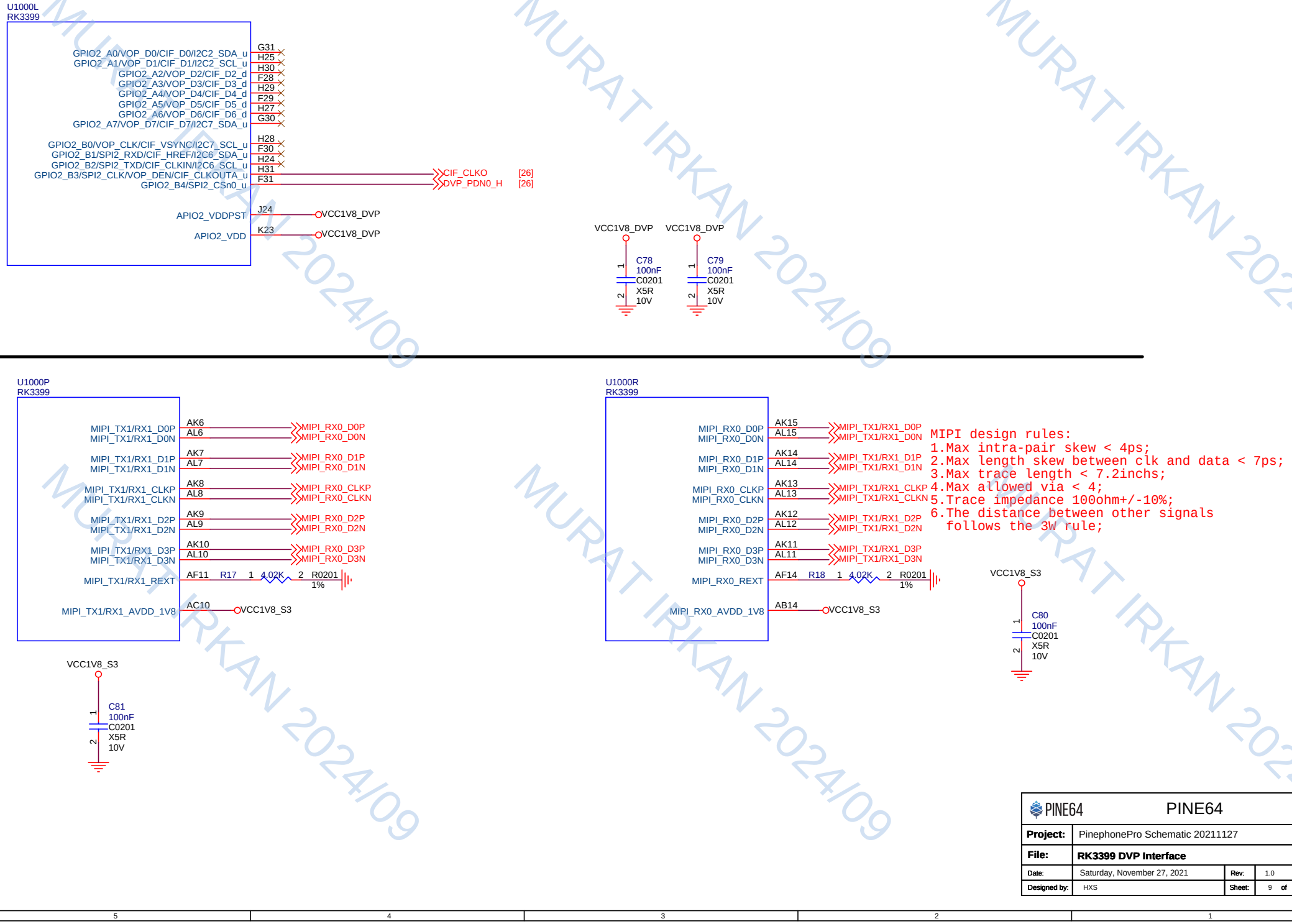
PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 USB/USIC Controler**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	HXS	**Sheet:**	7 of 24

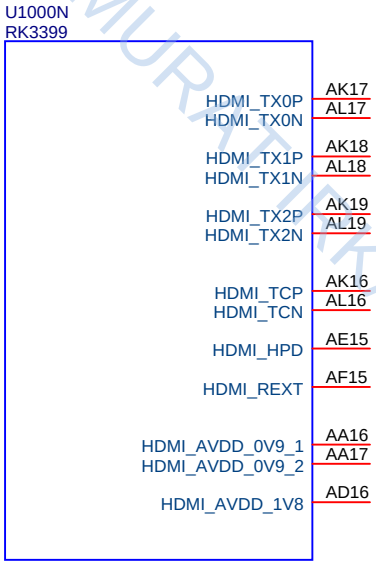


KEY BAORD V+/V-/Stdby

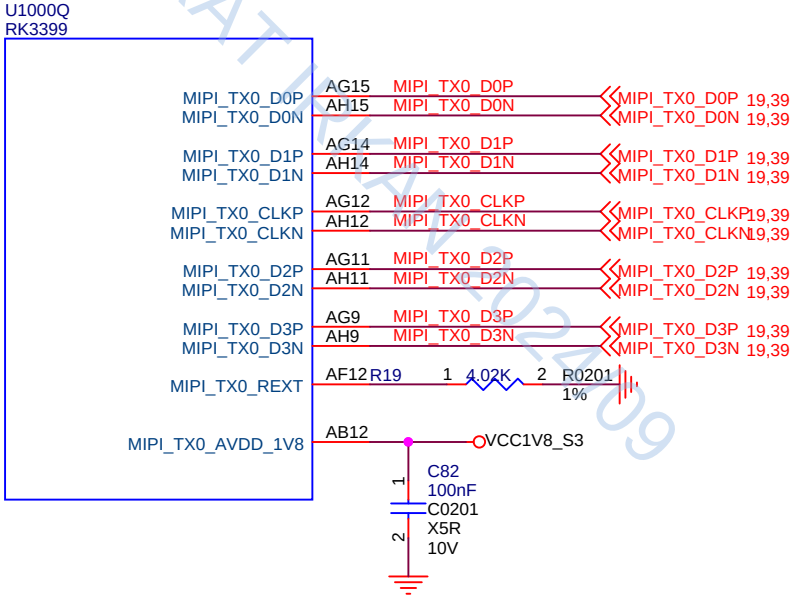


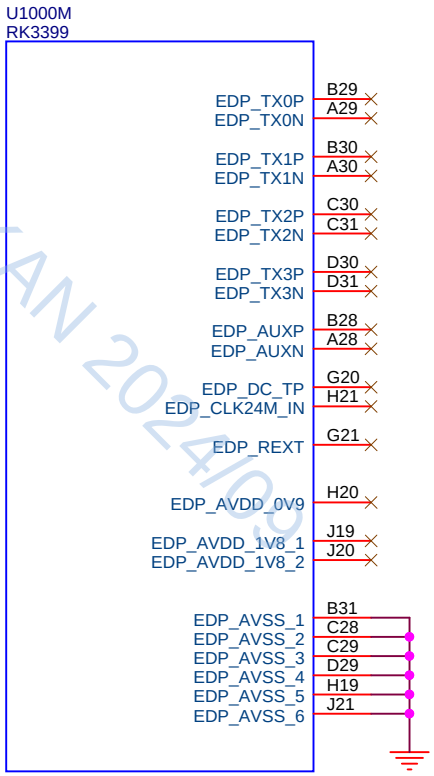
PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 SARADC/keyBoard**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	HXS	**Sheet:**	8 of 24





HDMI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 80 ps;
3.Max trace length < 9.8 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;

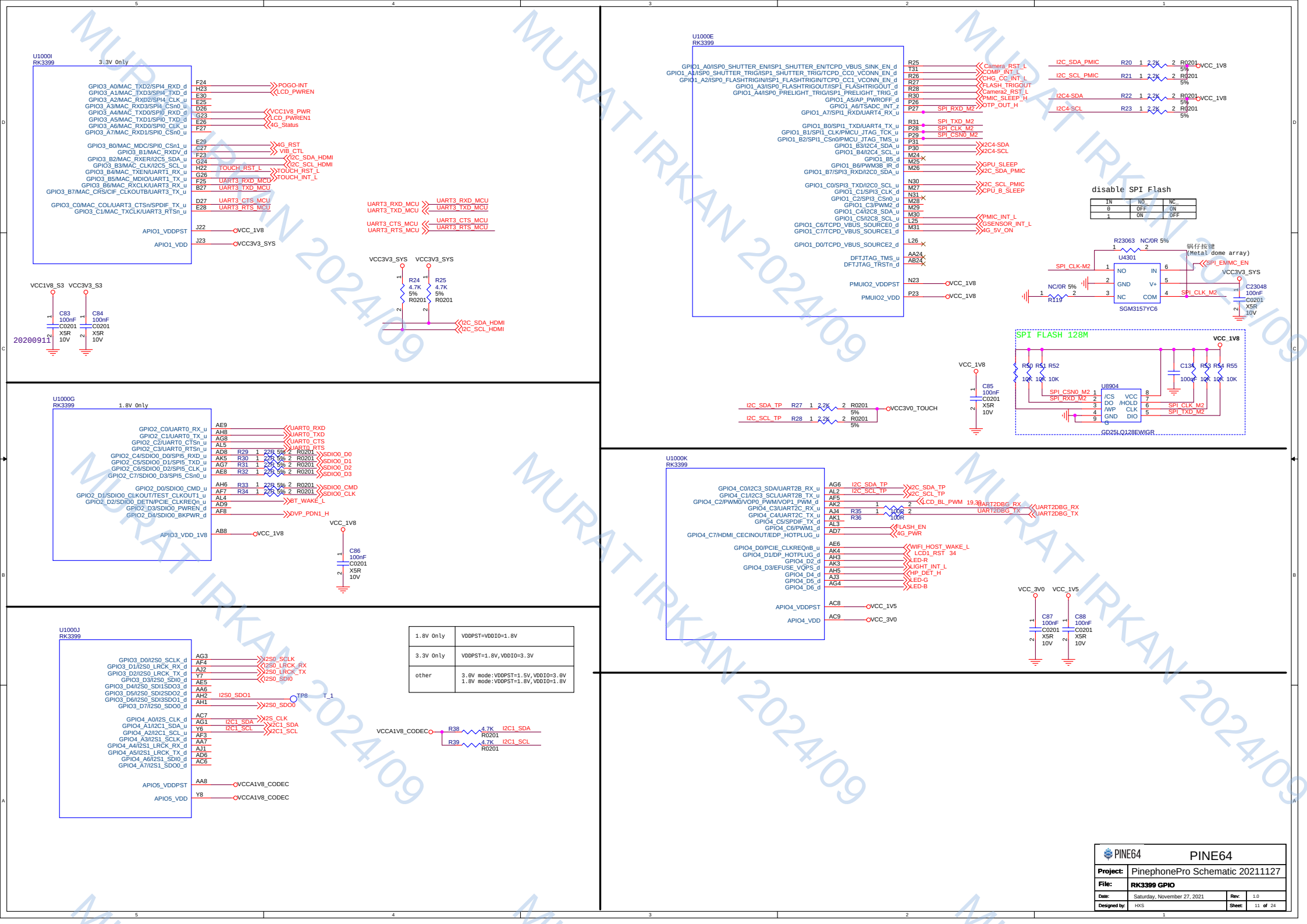




eDP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;

MIPI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;

PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**RK3399 Display Interface**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
Designed by:	HXS	**Sheet:**	10 **of** 24


U1000I
RK3399
3.3V Only
GPIO3_A0/MAC_TXD2/SPI4_RXD_d
GPIO3_A1/MAC_TXD3/SPI4_TXD_d
GPIO3_A2/MAC_RXD2/SPI4_CLK_u
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u
GPIO3_A4/MAC_TXD0/SPI0_RXD_d
GPIO3_A5/MAC_TXD1/SPI0_TXD_d
GPIO3_A6/MAC_RXD0/SPI0_CLK_u
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u
GPIO3_B0/MAC_MDC/SPI0_CSn1_u
GPIO3_B1/MAC_RXDV_d
GPIO3_B2/MAC_RXER/I2C5_SDA_u
GPIO3_B3/MAC_CLK/I2C5_SCL_u
GPIO3_B4/MAC_TXEN/UART1_RX_u
GPIO3_B5/MAC_MDIO/UART1_TX_u
GPIO3_B6/MAC_RXCLK/UART3_RX_u
GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_u
GPIO3_C0/MAC_COL/UART3_CTSn/SPDIF_TX_u
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u
APIO1_VDDPST
APIO1_VDD
F24
H23
E30
E25
D26
G23
E26
F27
E29
C27
F23
G24
H22
G26
F25
B27
D27
E28
J22
J23
POGO-INT
LCD_PWREN
VCC1V8_PWR
LCD_PWREN1
4G_Status
4G_RST
VIB_CTL
I2C_SDA_HDMI
I2C_SCL_HDMI
TOUCH_RST_L
TOUCH_INT_L
UART3_RXD_MCU
UART3_TXD_MCU
UART3_CTS_MCU
UART3_RTS_MCU
VCC_1V8
VCC3V3_SYS
UART3_RXD_MCU
UART3_TXD_MCU
UART3_CTS_MCU
UART3_RTS_MCU
VCC3V3_SYS
VCC3V3_SYS
R24
4.7K
5%
R0201
R25
4.7K
5%
R0201
I2C_SDA_HDMI
I2C_SCL_HDMI
VCC1V8_S3
VCC3V3_S3
C83
100nF
C0201
X5R
10V
C84
100nF
C0201
X5R
10V
20200911
U1000E
RK3399
GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_d
GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN_d
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d
GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d
GPIO1_A5/AP_PWROFF_d
GPIO1_A6/TSADC_INT_z
GPIO1_A7/SPI1_RXD/UART4_RX_u
GPIO1_B0/SPI1_TXD/UART4_TX_u
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u
GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS_u
GPIO1_B3/I2C4_SDA_u
GPIO1_B4/I2C4_SCL_u
GPIO1_B5_d
GPIO1_B6/PWM3B_IR_d
GPIO1_B7/SPI3_RXD/I2C0_SDA_u
GPIO1_C0/SPI3_TXD/I2C0_SCL_u
GPIO1_C1/SPI3_CLK_d
GPIO1_C2/SPI3_CSn0_u
GPIO1_C3/PWM2_d
GPIO1_C4/I2C8_SDA_u
GPIO1_C5/I2C8_SCL_u
GPIO1_C6/TCPD_VBUS_SOURCE0_d
GPIO1_C7/TCPD_VBUS_SOURCE1_d
GPIO1_D0/TCPD_VBUS_SOURCE2_d
DFTJTAG_TMS_u
DFTJTAG_TRSTn_d
PMUIO2_VDDPST
PMUIO2_VDD
R25
T31
R26
R27
R28
R30
P26
P27
R31
P28
P29
P31
P30
M24
M25
M26
N30
M27
N31
M28
M29
M30
L25
M31
L26
AA24
AB24
N23
P23
Camera_RST_L
COMP_INT_L
CHG_CC_INT_L
FLASH_TRIGOUT
Camera2_RST_L
PMIC_SLEEP_H
OTP_OUT_H
SPI_RXD_M2
SPI_TXD_M2
SPI_CLK_M2
SPI_CSN0_M2
I2C4-SDA
I2C4-SCL
GPU_SLEEP
I2C_SDA_PMIC
I2C_SCL_PMIC
PMIC_INT_L
GSENSOR_INT_L
G_5V_ON
I2C_SCL_PMIC
CPU_B_SLEEP
VCC_1V8
VCC_1V8
I2C_SDA_PMIC
I2C_SCL_PMIC
I2C4-SDA
I2C4-SCL
R20 1 2.2K 2 R0201 5%
R21 1 2.2K 2 R0201 5%
R22 1 2.2K 2 R0201 5%
R23 1 2.2K 2 R0201 5%
VCC_1V8
VCC_1V8
disable SPI Flash
IN | NO | NC
0 | OFF | ON
1 | ON | OFF
R23063 NC/0R 5%
U4301
SGM3157YC6
NO
GND
NC
IN
V+
COM
SPI_CLK-M2
NC/0R 5%
R119
SPI_EMMC_EN
SPI_CLK_M2
VCC3V3_SYS
C23048
100nF
C0201
X5R
10V
锅仔按键
(Metal dome array)
SPI FLASH 128M
VCC_1V8
U8904
/CS
DO
/WP
GND
VCC
/HOLD
CLK
DIO
GD25LQ128EWIGR
R50 R51 R52
10K 10K 10K
C134
100nF
R53 R54 R55
10K 10K 10K
SPI_CSN0_M2
SPI_RXD_M2
SPI_CLK_M2
SPI_TXD_M2
VCC_1V8
C85
100nF
C0201
X5R
10V
I2C_SDA_TP
I2C_SCL_TP
R27 1 2.2K 2 R0201 5%
R28 1 2.2K 2 R0201 5%
VCC3V0_TOUCH
U1000G
RK3399
1.8V Only
GPIO2_C0/UART0_RX_u
GPIO2_C1/UART0_TX_u
GPIO2_C2/UART0_CTSn_u
GPIO2_C3/UART0_RTSn_u
GPIO2_C4/SDIO0_D0/SPI5_RXD_u
GPIO2_C5/SDIO0_D1/SPI5_TXD_u
GPIO2_C6/SDIO0_D2/SPI5_CLK_u
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u
GPIO2_D0/SDIO0_CMD_u
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQn_u
GPIO2_D3/SDIO0_PWREN_d
GPIO2_D4/SDIO0_BKPWR_d
APIO3_VDD_1V8
AE9
AH8
AG8
AL5
AD8
AK5
AG7
AE8
AH6
AF7
AL4
AD9
AF8
AB8
R29 1 22R 5% 2 R0201
R30 1 22R 5% 2 R0201
R31 1 22R 5% 2 R0201
R32 1 22R 5% 2 R0201
R33 1 22R 5% 2 R0201
R34 1 22R 5% 2 R0201
UART0_RXD
UART0_TXD
UART0_CTS
UART0_RTS
SDIO0_D0
SDIO0_D1
SDIO0_D2
SDIO0_D3
SDIO0_CMD
SDIO0_CLK
BT_WAKE_L
DVP_PDN1_H
VCC_1V8
VCC_1V8
C86
100nF
C0201
X5R
10V
U1000K
RK3399
GPIO4_C0/I2C3_SDA/UART2B_RX_u
GPIO4_C1/I2C3_SCL/UART2B_TX_u
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d
GPIO4_C3/UART2C_RX_u
GPIO4_C4/UART2C_TX_u
GPIO4_C5/SPDIF_TX_d
GPIO4_C6/PWM1_d
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u
GPIO4_D0/PCIE_CLKREQnB_u
GPIO4_D1/DP_HOTPLUG_d
GPIO4_D2_d
GPIO4_D3/EFUSE_VQPS_d
GPIO4_D4_d
GPIO4_D5_d
GPIO4_D6_d
APIO4_VDDPST
APIO4_VDD
AG6
AL2
AF5
AK2
AJ4
AK1
AL3
AD7
AE6
AK4
AH3
AK3
AH5
AJ3
AG4
AC8
AC9
I2C_SDA_TP
I2C_SCL_TP
LCD_BL_PWM 19.3K
R35 1 100R 2 100R
R36
FLASH_EN
4G_PWR
WIFI_HOST_WAKE_L
LCD1_RST 34
LED-R
LIGHT_INT_L
HP_DET_H
LED-G
LED-B
VCC_1V5
VCC_3V0
UART2DBG_RX
UART2DBG_TX
UART2DBG_RX
UART2DBG_TX
VCC_3V0
VCC_1V5
C87
100nF
C0201
X5R
10V
C88
100nF
C0201
X5R
10V
U1000J
RK3399
GPIO3_D0/I2S0_SCLK_d
GPIO3_D1/I2S0_LRCK_RX_d
GPIO3_D2/I2S0_LRCK_TX_d
GPIO3_D3/I2S0_SDI0_d
GPIO3_D4/I2S0_SDI1SDO3_d
GPIO3_D5/I2S0_SDI2SDO2_d
GPIO3_D6/I2S0_SDI3SDO1_d
GPIO3_D7/I2S0_SDO0_d
GPIO4_A0/I2S_CLK_d
GPIO4_A1/I2C1_SDA_u
GPIO4_A2/I2C1_SCL_u
GPIO4_A3/I2S1_SCLK_d
GPIO4_A4/I2S1_LRCK_RX_d
GPIO4_A5/I2S1_LRCK_TX_d
GPIO4_A6/I2S1_SDI0_d
GPIO4_A7/I2S1_SDO0_d
APIO5_VDDPST
APIO5_VDD
AG3
AF4
AJ2
Y7
AE5
AA6
AH2
AH1
AC7
AG1
Y6
AF3
AA7
AJ1
AD6
AC6
AA8
Y8
I2S0_SCLK
I2S0_LRCK_RX
I2S0_LRCK_TX
I2S0_SDI0
I2S0_SDO1
TP8
T_1
I2S0_SDO0
I2S_CLK
I2C1_SDA
I2C1_SCL
I2C1_SDA
I2C1_SCL
VCCA1V8_CODEC
VCCA1V8_CODEC
1.8V Only | VDDPST=VDDIO=1.8V
3.3V Only | VDDPST=1.8V,VDDIO=3.3V
other | 3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V
VCCA1V8_CODEC
R38 4.7K I2C1_SDA R0201
R39 4.7K I2C1_SCL R0201
PINE64
PINE64
Project: PinephonePro Schematic 20211127
File: RK3399 GPIO
Date: Saturday, November 27, 2021
Rev: 1.0
Designed by: HXS
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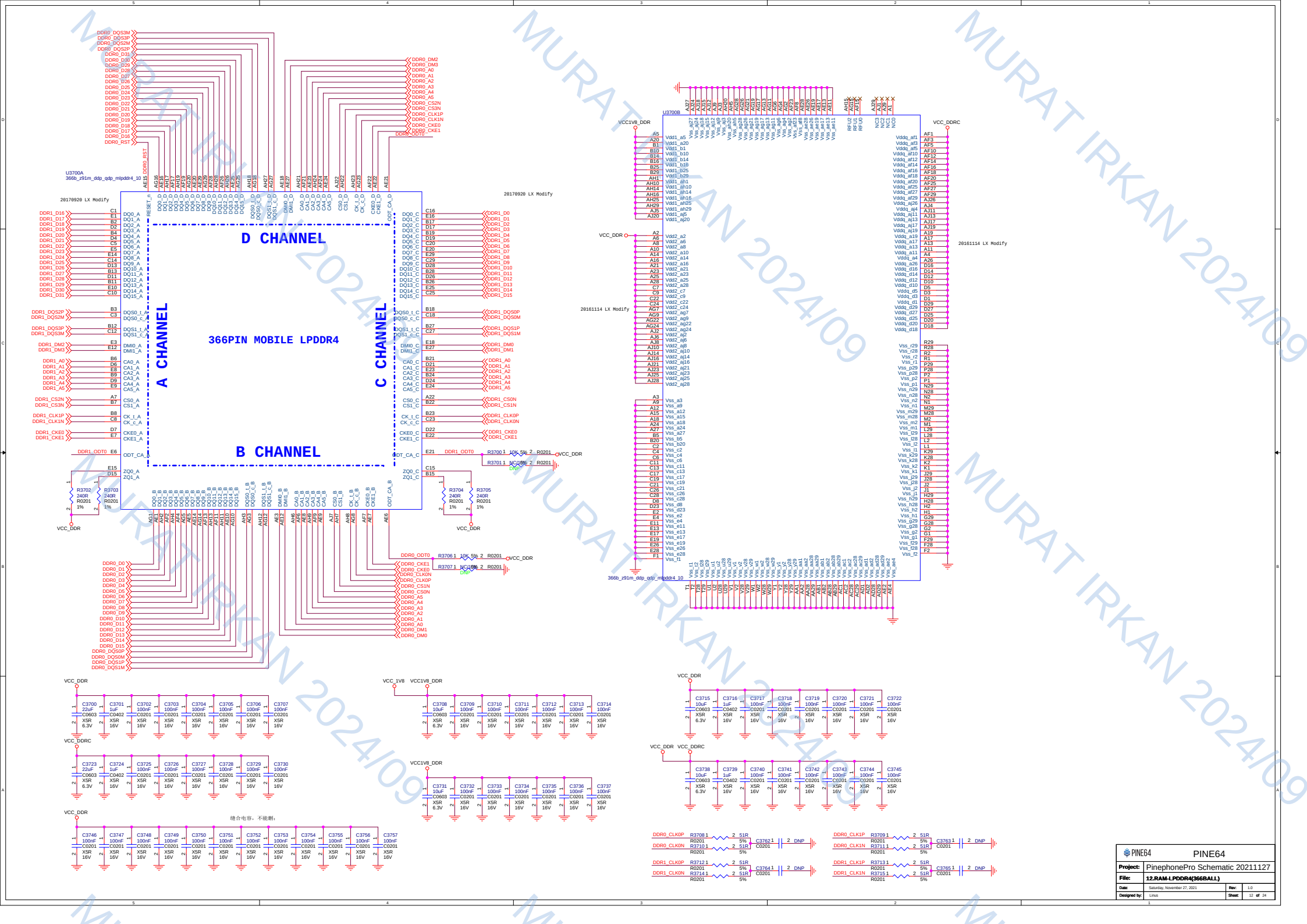
A CHANNEL
B CHANNEL
C CHANNEL
D CHANNEL
366PIN MOBILE LPDDR4
U3700A
366b_z91m_ddp_qdp_mlpddr4_15
U3700B
366b_z91m_ddp_qdp_mlpddr4_10
20170920 LX Modify
20170930 LX Modify
20161114 LX Modify
20161114 LX Modify
VCC_DDR
VCC_DDRC
VCC1V8_DDR
VCC_1V8
VCC1V8_DDR
DNP
PINE64
PinephonePro Schematic 20211127
12.RAM-LPDDR4(366BALL)
Saturday, November 27, 2021
Linus
1.0
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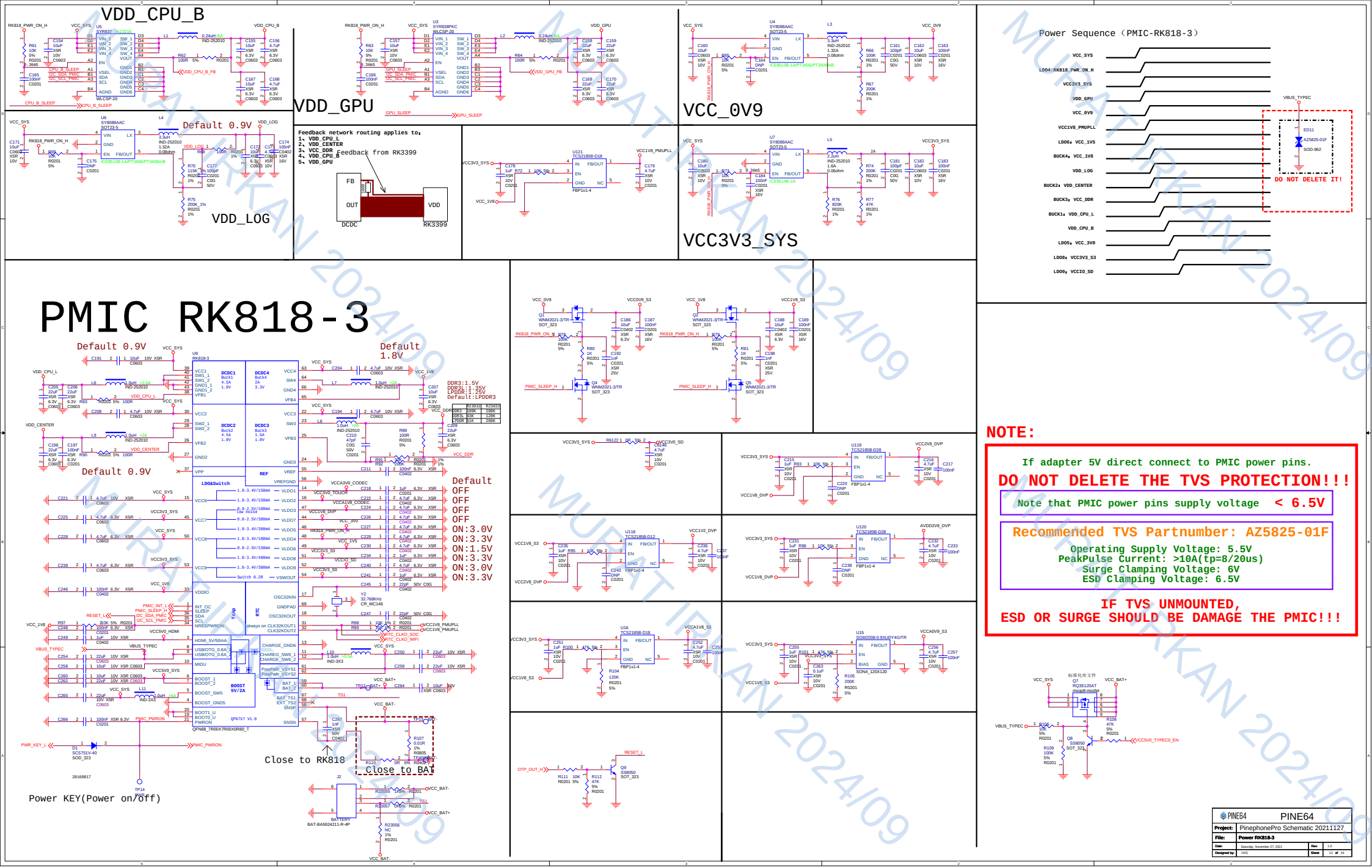
VDD_CPU_B
VDD_GPU
VCC_0V9
VDD_LOG
Default 0.9V
VCC3V3_SYS
Feedback network routing applies to,
1、VDD_CPU_L
2、VDD_CENTER
3、VCC_DDR Feedback from RK3399
4、VDD_CPU_B
5、VDD_GPU
FB
OUT
VDD
DCDC
RK3399
PMIC RK818-3
Default 0.9V
Default 1.8V
DDR3:1.5V
DDR3L::1.35V
LPDDR:1.25V
Default:LPDDR3
Default
OFF
OFF
OFF
OFF
ON:3.0V
ON:3.3V
ON:1.5V
ON:3.3V
ON:3.0V
ON:3.3V
Close to RK818
Close to BAT
Power KEY(Power on/off)
Power Sequence（PMIC-RK818-3）
VCC_SYS
LDO4:RK818_PWR_ON_H
VCC3V3_SYS
VDD_GPU
VCC_0V9
VCC1V8_PMUPLL
LDO6: VCC_1V5
BUCK4: VCC_1V8
VDD_LOG
BUCK2: VDD_CENTER
BUCK3: VCC_DDR
BUCK1: VDD_CPU_L
VDD_CPU_B
LDO5: VCC_3V0
LDO8: VCC3V3_S3
LDO9: VCCIO_SD
VBUS_TYPEC
ED11
AZ5825-01F
SOD-962
DO NOT DELETE IT!
NOTE:
If adapter 5V direct connect to PMIC power pins.
DO NOT DELETE THE TVS PROTECTION!!!
Note that PMIC power pins supply voltage < 6.5V
Recommended TVS Partnumber: AZ5825-01F
Operating Supply Voltage: 5.5V
PeakPulse Current: >10A(tp=8/20us)
Surge Clamping Voltage: 6V
ESD Clamping Voltage: 6.5V
IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!
PINE64
Project: PinephonePro Schematic 20211127
File: Power RK818-3
Date: Saturday, November 27, 2021
Rev: 1.0
Designed by: WKS
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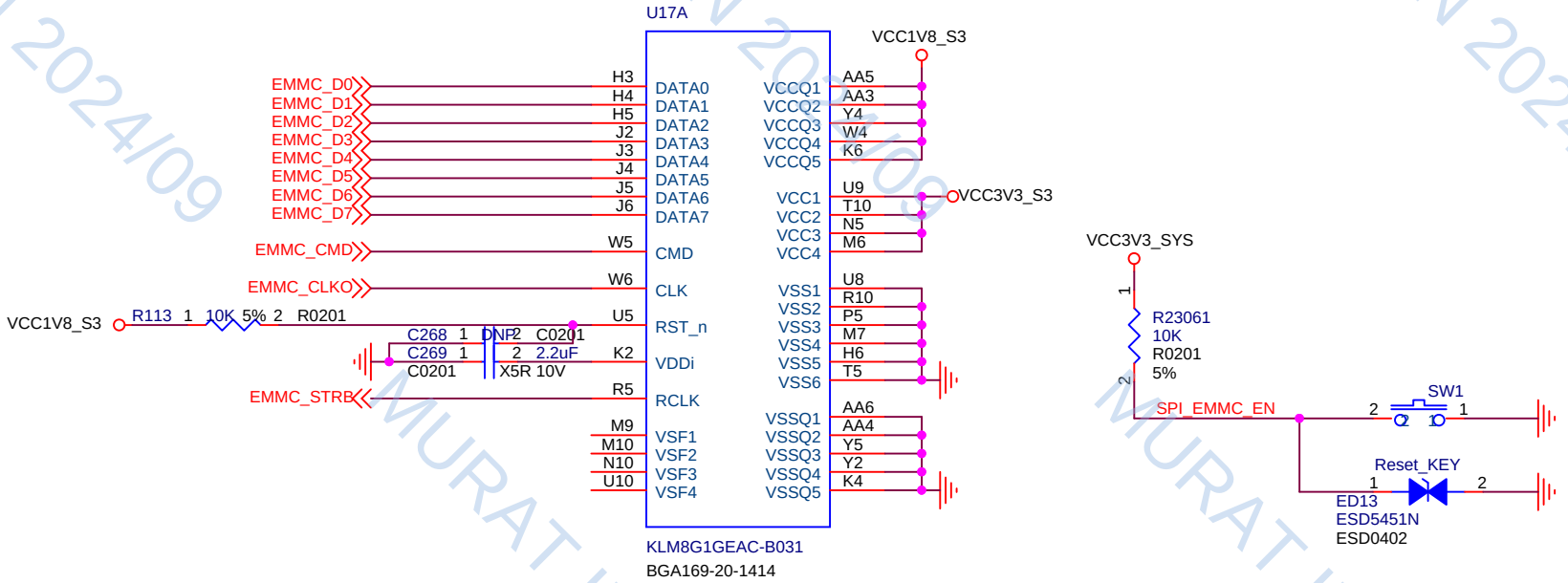
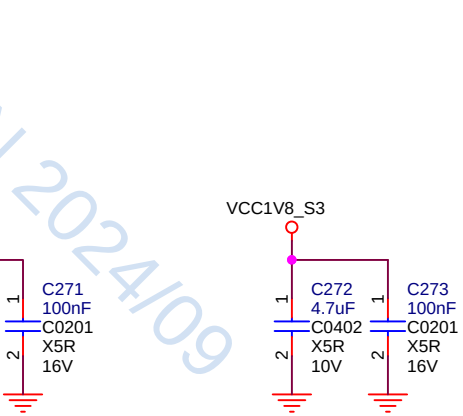
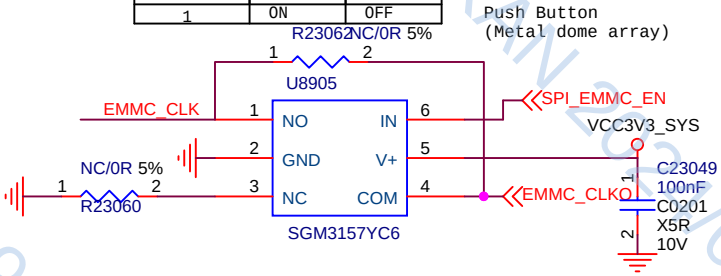
eMMC FLASH





disable eMMC

IN	NO_	NC_
0	OFF	ON
1	ON	OFF



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Project:	PinephonePro Schematic 20211127		
File:	**Memory-eMMC**		
Date:	Saturday, November 27, 2021	**Rev:**	1.0
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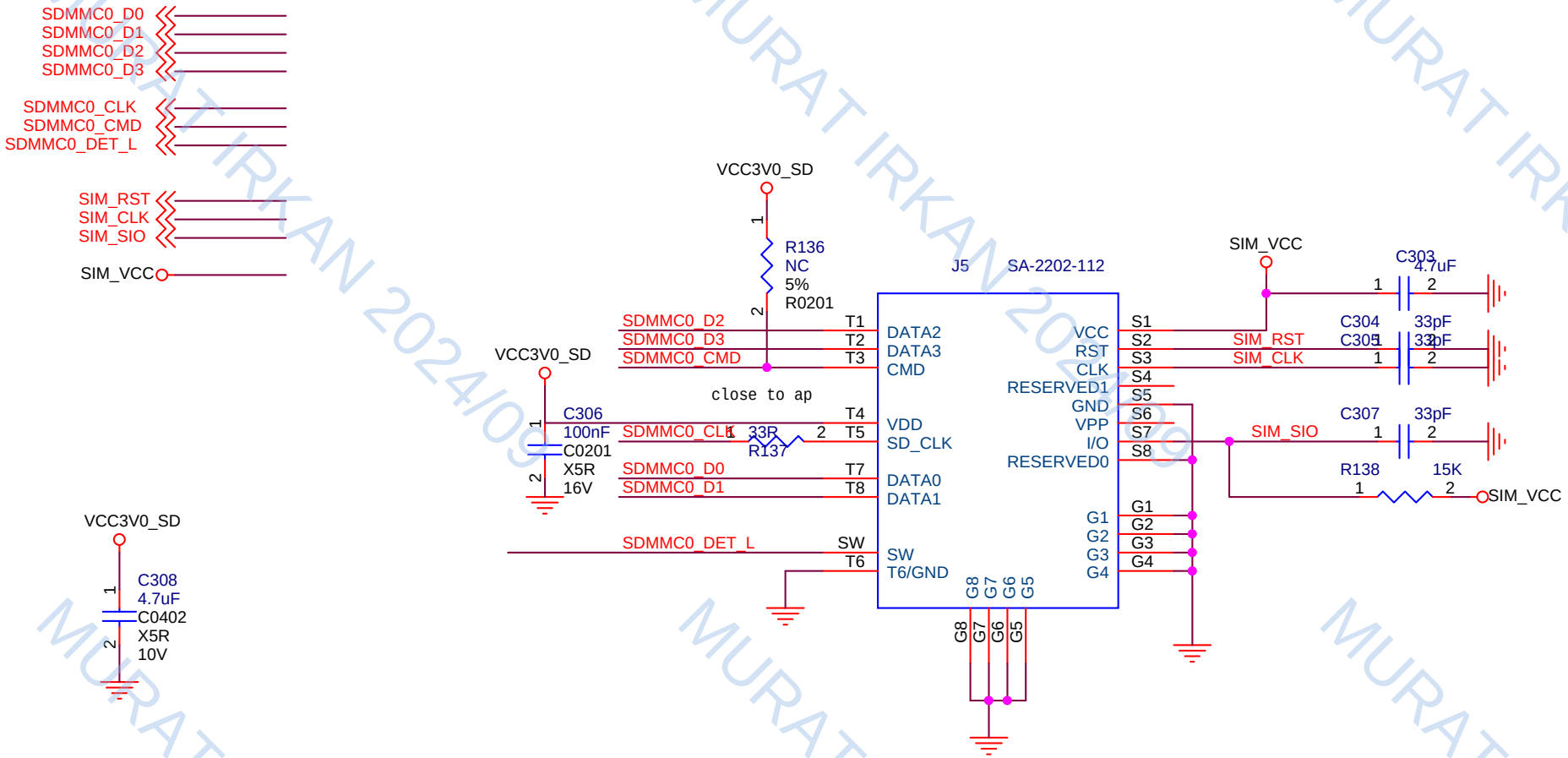

PINE64	PINE64
Project:	PinephonePro Schematic 20211127
File:	**TF Card**
Date:	Saturday, November 27, 2021
Rev:	1.0
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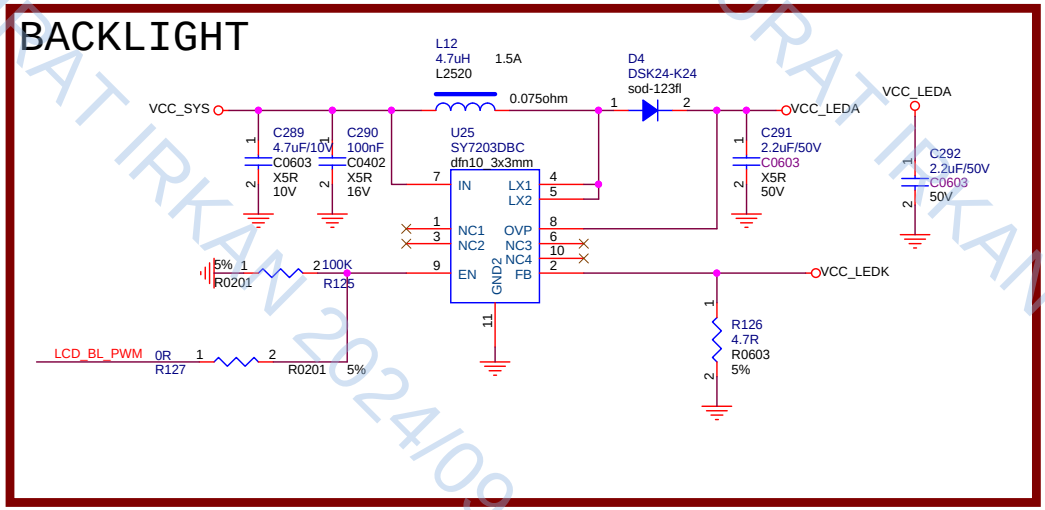
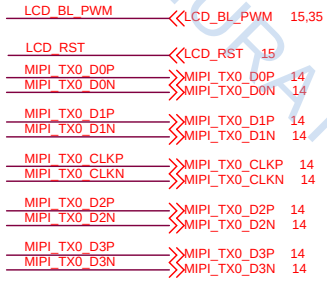
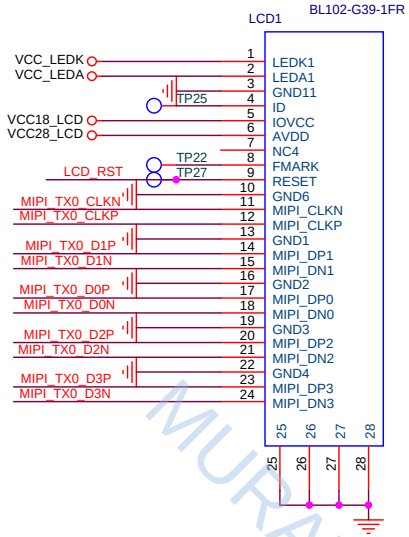
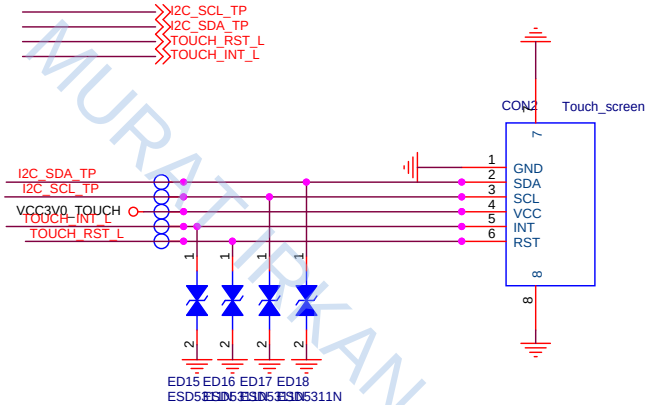
MIPI Panel

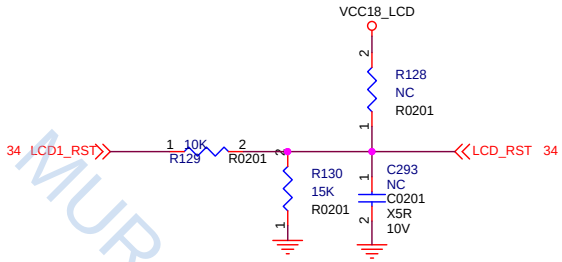
BACKLIGHT

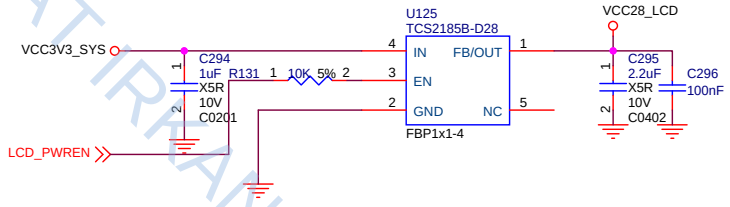


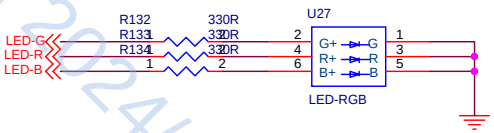


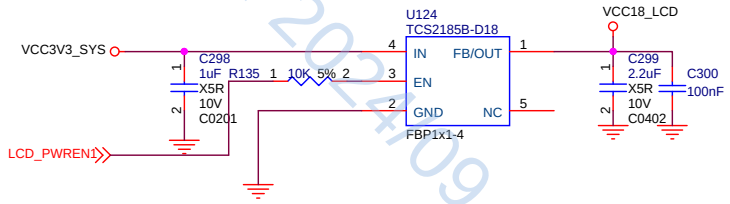












PINE64 PINE64

Title

LCD panel/Touch Panel

Size	File	Rev
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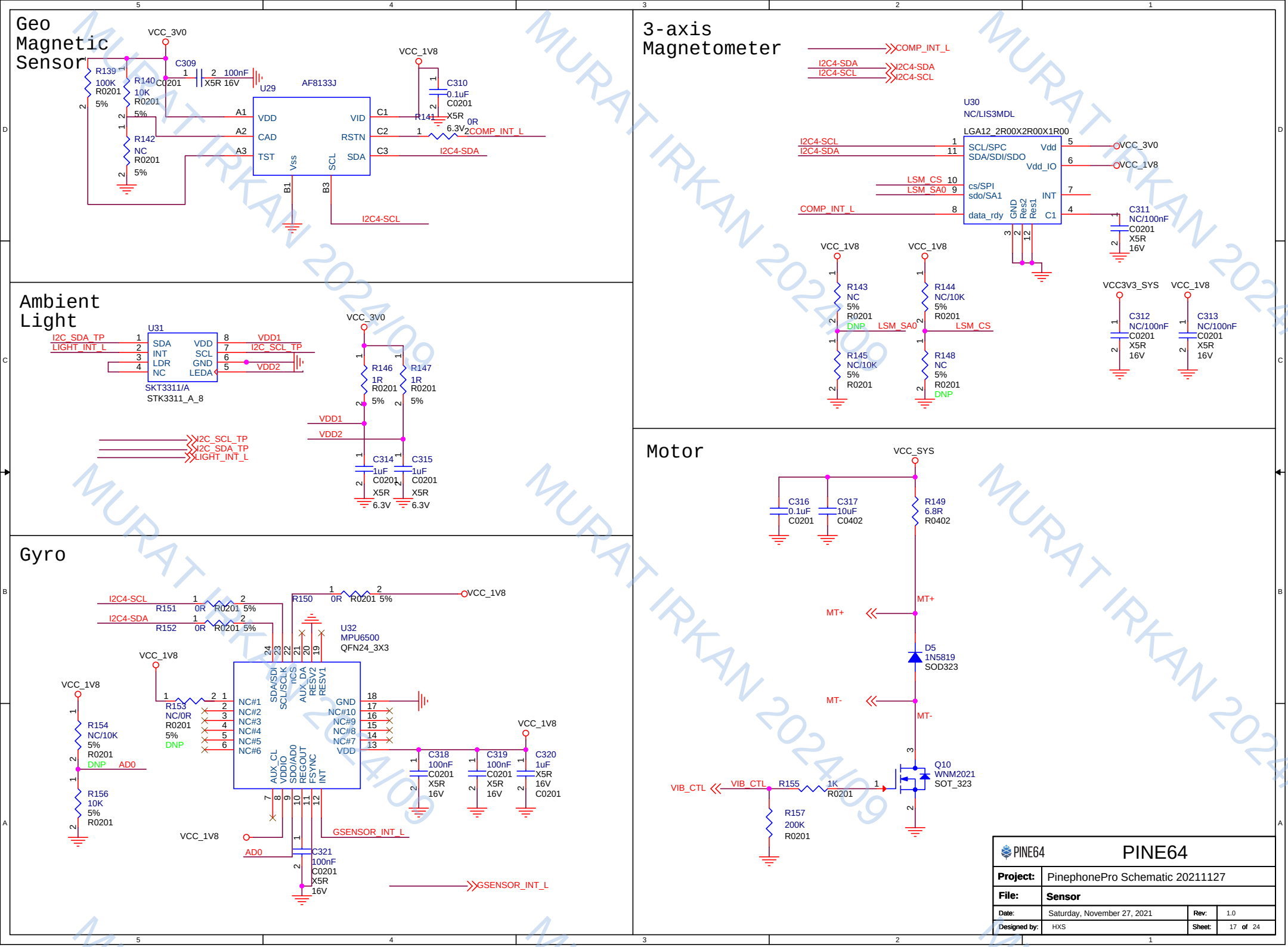
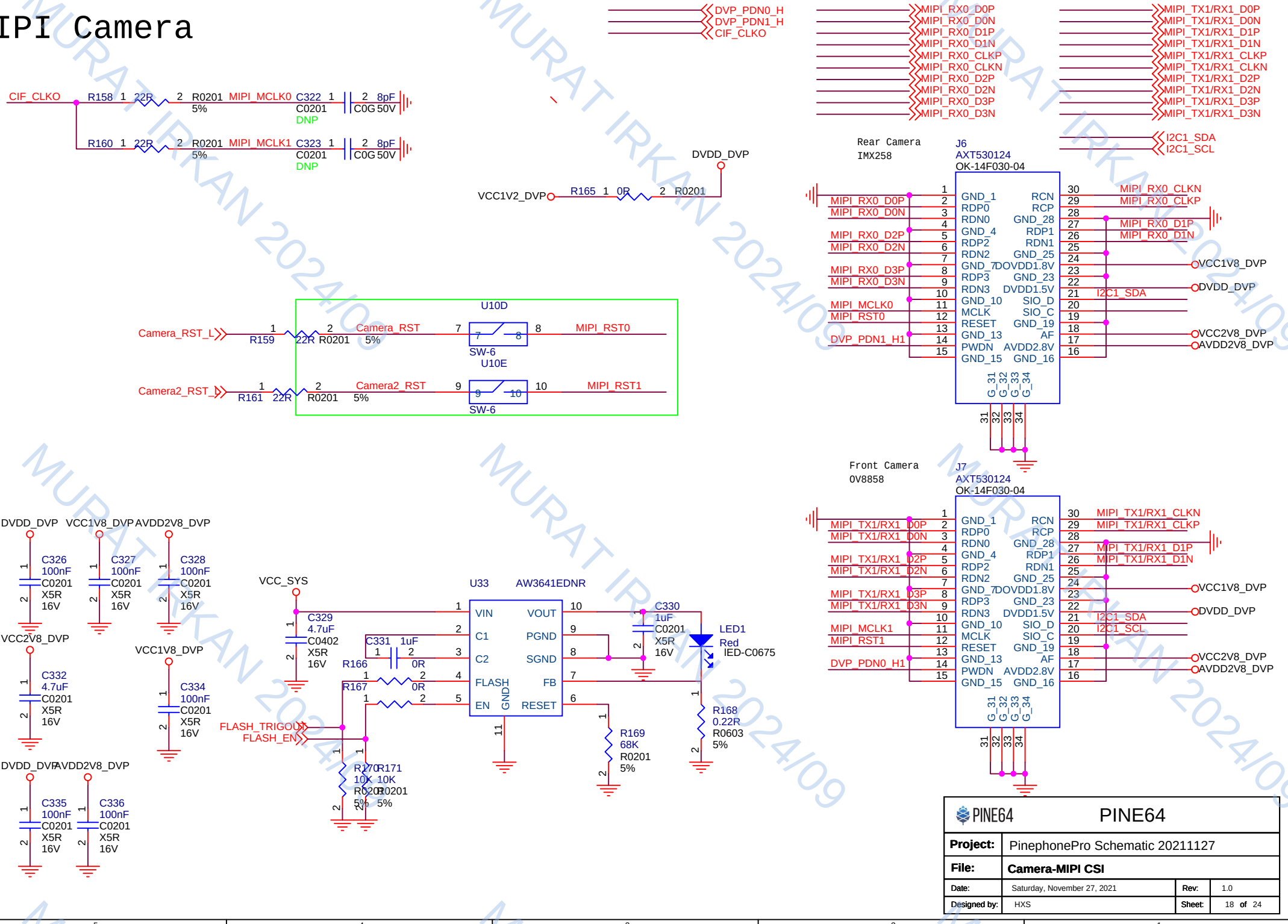


MIPI Camera



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Project:	PinephonePro Schematic 20211127
File:	**Camera-MIPI CSI**
Date:	Saturday, November 27, 2021
Rev:	1.0
Designed by:	HXS
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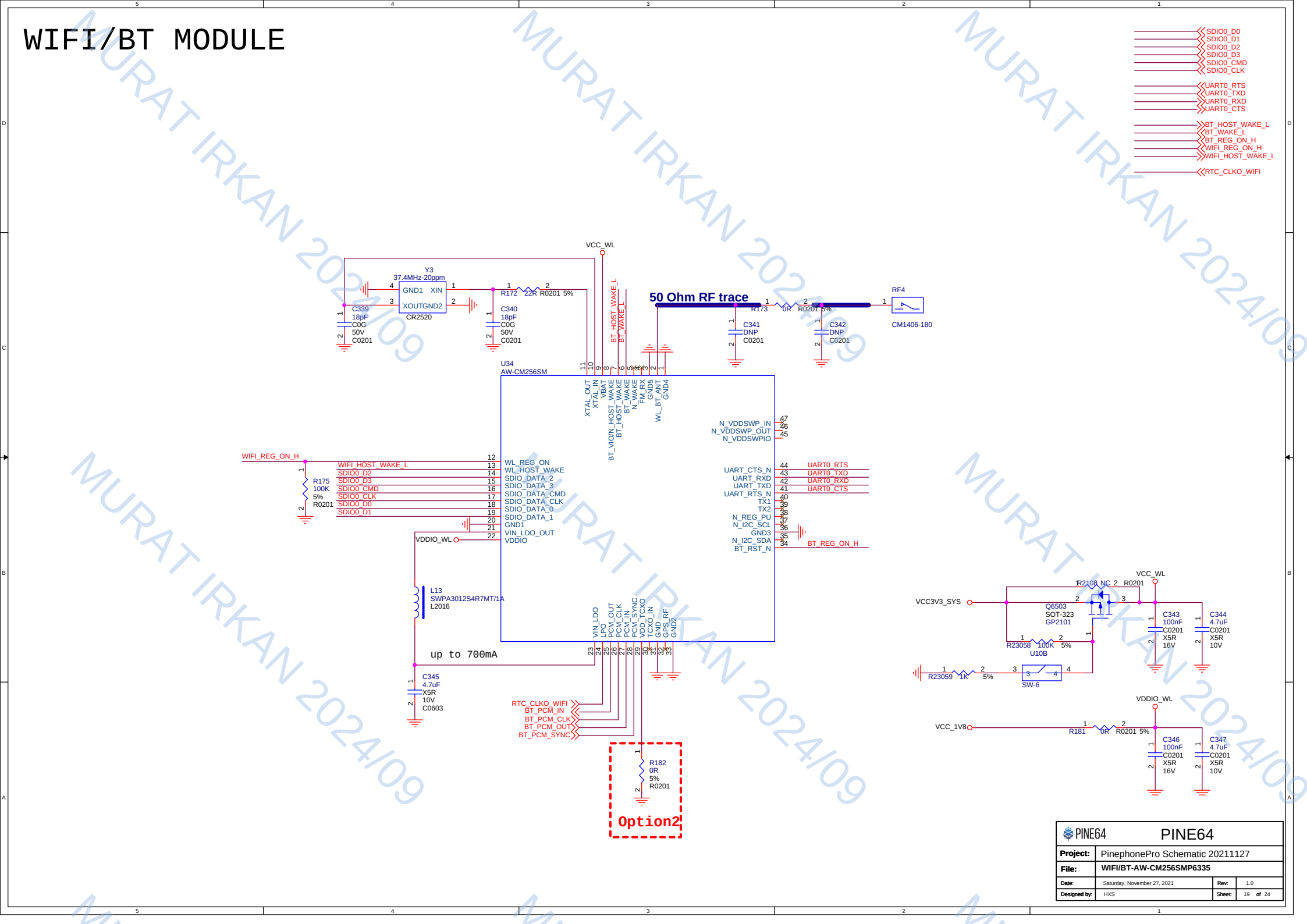
WIFI/BT MODULE



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Project:	PinephonePro Schematic 20211127
File:	**WIFI/BT-AW-CM256SMP6335**
Date:	Saturday, November 27, 2021
Rev:	1.0
Designed by:	HXS
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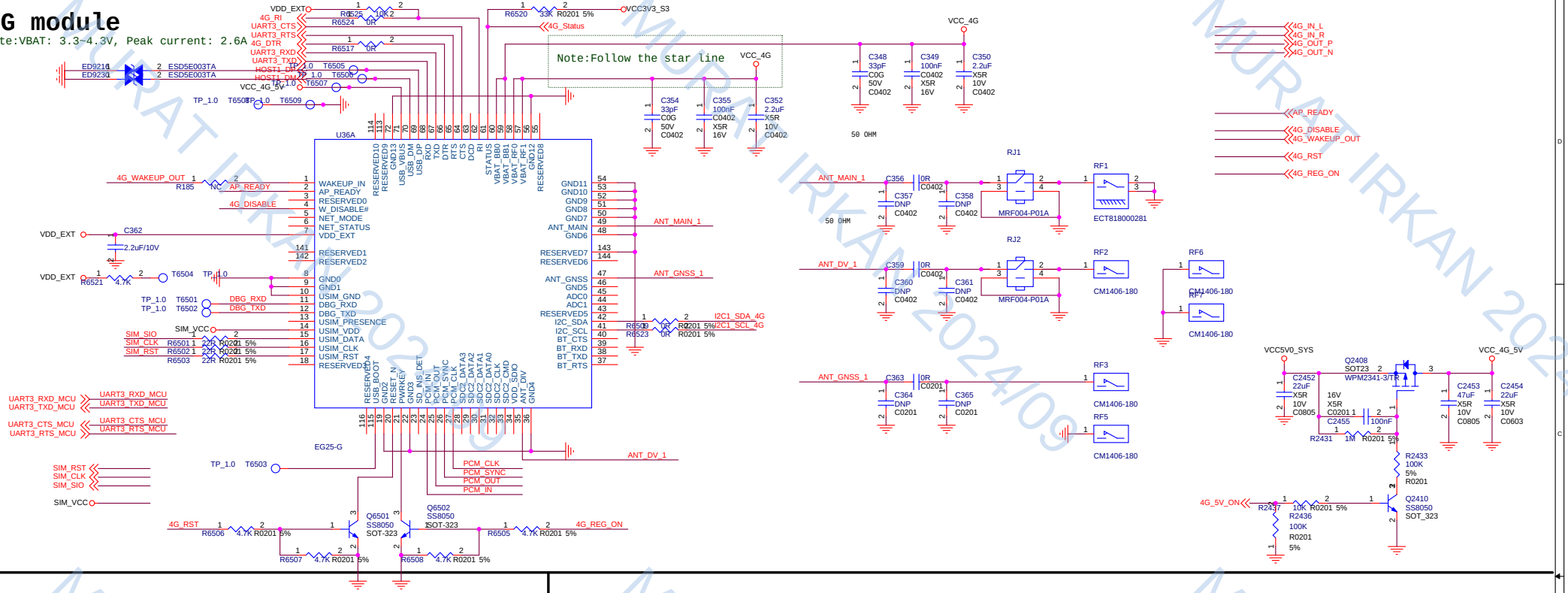
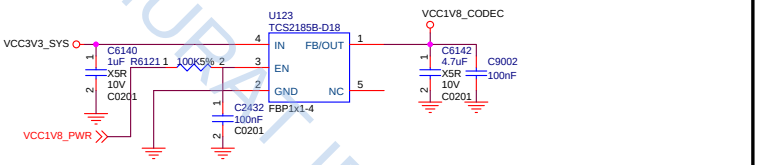
4G module

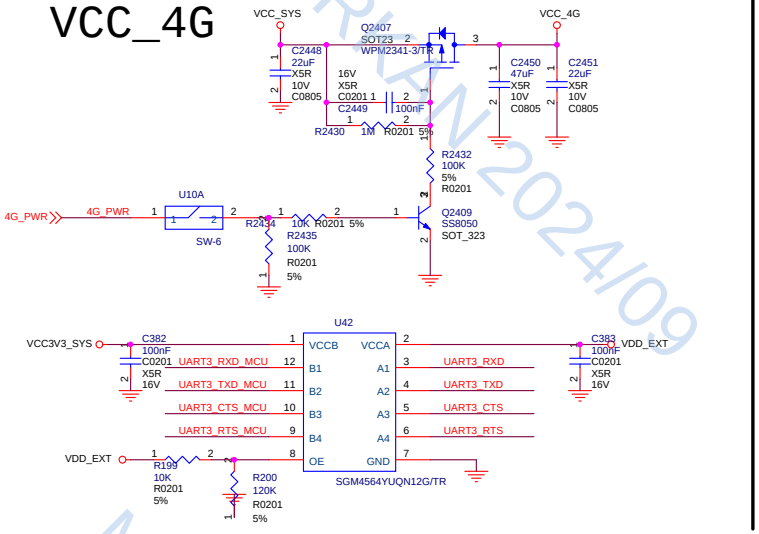
Note:VBAT: 3.3~4.3V, Peak current: 2.6A



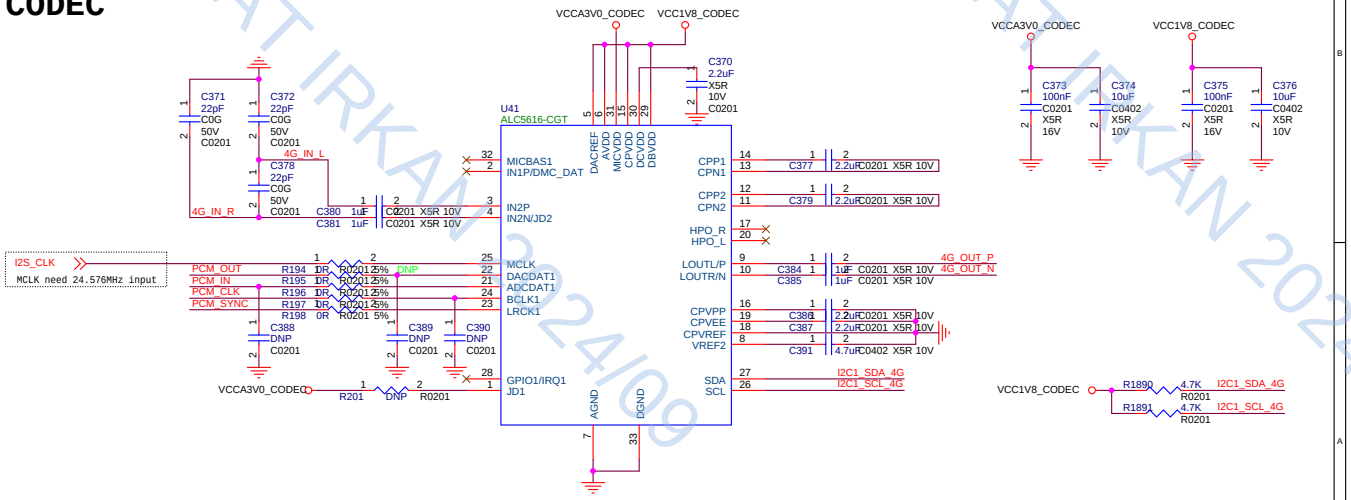
POWER



VCC_4G



CODEC



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Project:	PinephonePro Schematic 20211127		
File:	20.4G Module		
Date:	Saturday, November 27, 2021	Rev:	1.0
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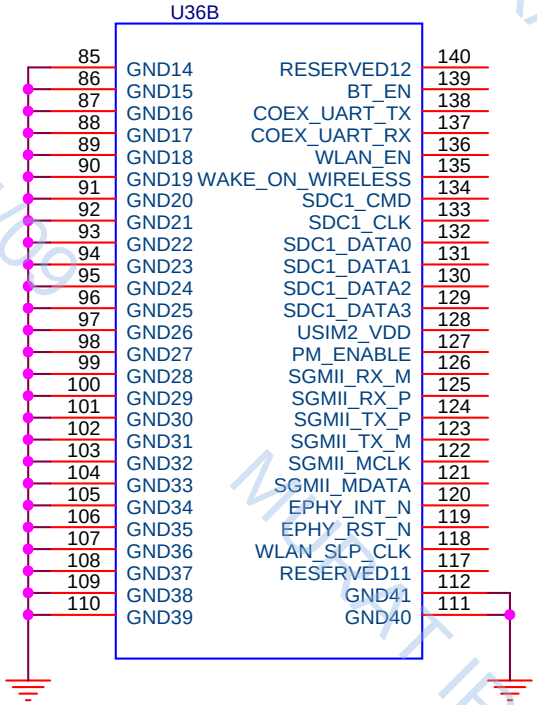

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PINE64

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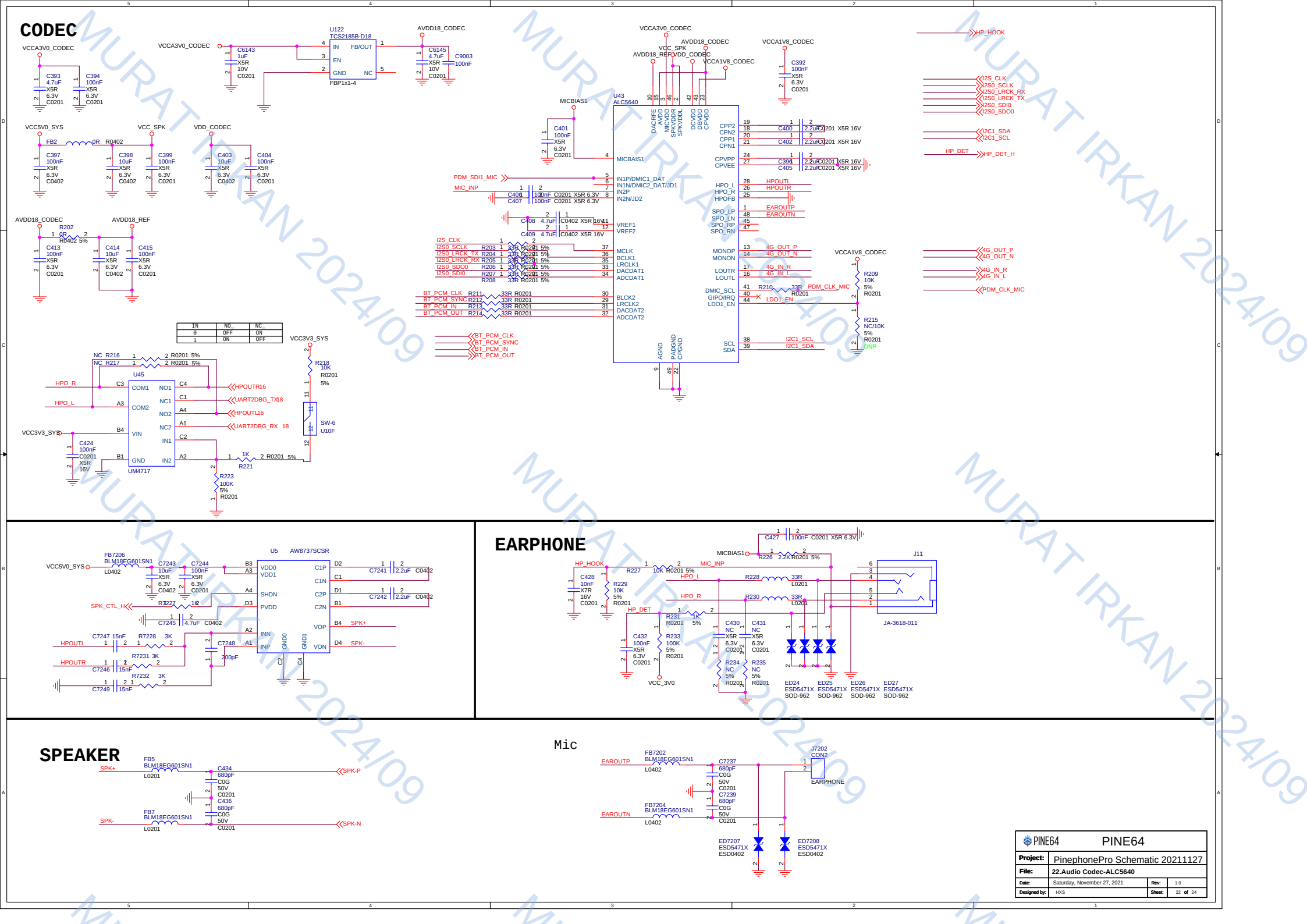

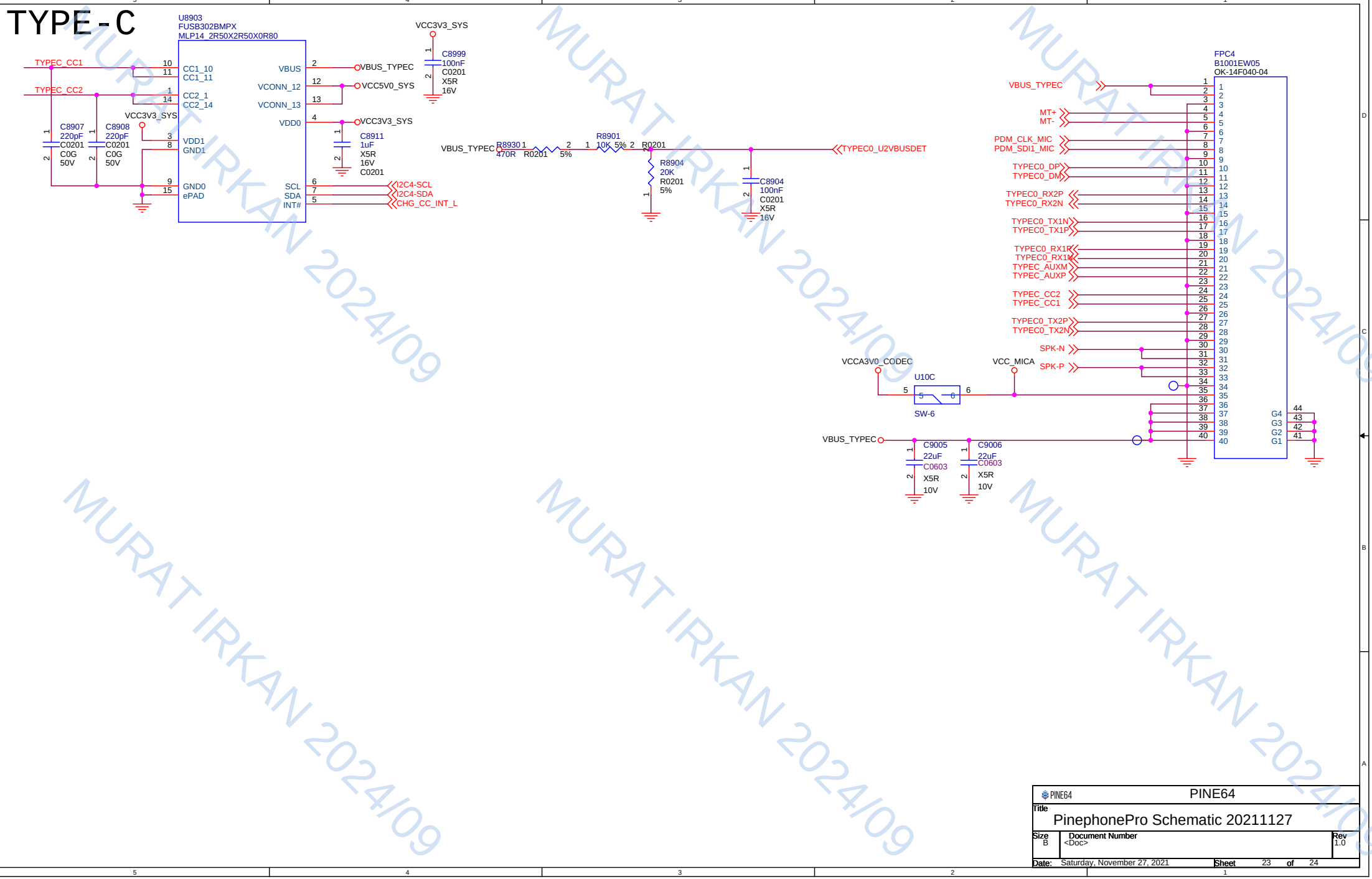
TYPE-C
U8903
FUSB302BMPX
MLP14_2R50X2R50X0R80
TYPEC_CC1
TYPEC_CC2
CC1_10
CC1_11
CC2_1
CC2_14
VDD1
GND1
GND0
ePAD
VBUS
VCONN_12
VCONN_13
VDD0
SCL
SDA
INT#
VBUS_TYPEC
VCC5V0_SYS
VCC3V3_SYS
C8907
220pF
C0201
C0G
50V
C8908
220pF
C0201
C0G
50V
C8911
1uF
X5R
16V
C0201
C8999
100nF
C0201
X5R
16V
I2C4-SCL
I2C4-SDA
CHG_CC_INT_L
R8930
470R
R0201
5%
R8901
10K 5%
R0201
R8904
20K
R0201
5%
C8904
100nF
C0201
X5R
16V
TYPEC0_U2VBUSDET
FPC4
B1001EW05
OK-14F040-04
MT+
MT-
PDM_CLK_MIC
PDM_SDI1_MIC
TYPEC0_DP
TYPEC0_DM
TYPEC0_RX2P
TYPEC0_RX2N
TYPEC0_TX1N
TYPEC0_TX1P
TYPEC0_RX1P
TYPEC0_RX1N
TYPEC_AUXM
TYPEC_AUXP
TYPEC_CC2
TYPEC_CC1
TYPEC0_TX2P
TYPEC0_TX2N
SPK-N
SPK-P
VCCA3V0_CODEC
VCC_MICA
U10C
SW-6
C9005
22uF
C0603
X5R
10V
C9006
22uF
C0603
X5R
10V
G4
G3
G2
G1
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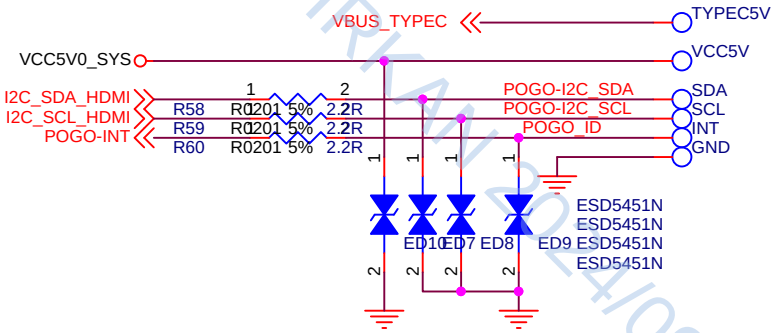
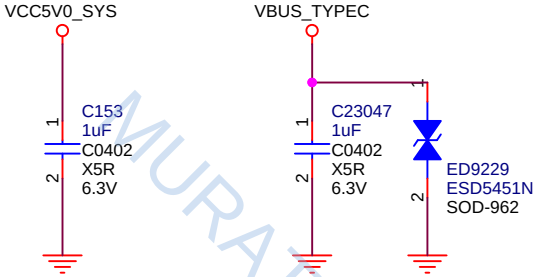
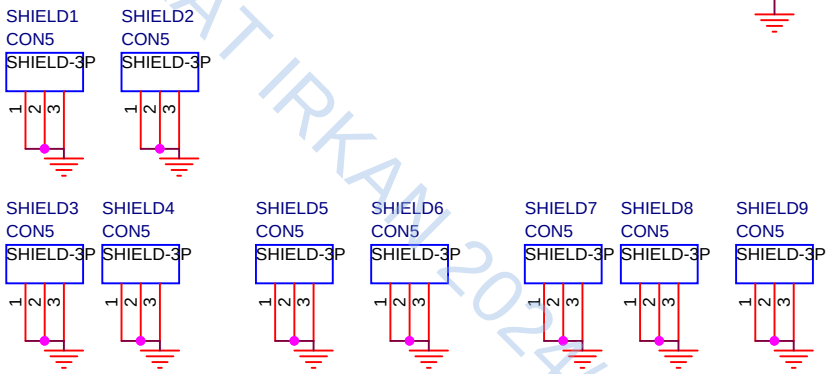
Pogo Pins





SHEILD&HOLE



PINE64	PINE64		
Project:	PinephonePro Schematic 20211127		
File:	**24.USB-POGO/SHILED**		
Date:	Saturday, November 27, 2021	**Rev:**	V1.0
Designed by:	Linus	**Sheet:**	24 **of** 24