Reference Schematics For RK3588S

RK3588S_Tablet_Demo_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x
4) ROM: eMMC5.1(Default)
5) Support: 1 x Type-C 3.0(with DP function)
6) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
7) Support: 1 x 2Lanes MIPI DPHY RX Camera
8) Support: 1 x 4Lanes MIPI D/CPHY TX
9) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
11) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
12) Support: 2 x PDM MIC Array
13) Support: Gyroscope+G-sensor+Ambient Light+Proximity

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	00.Cover Page				
Date:	Friday, January 07, 2022			Rev:	V10
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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

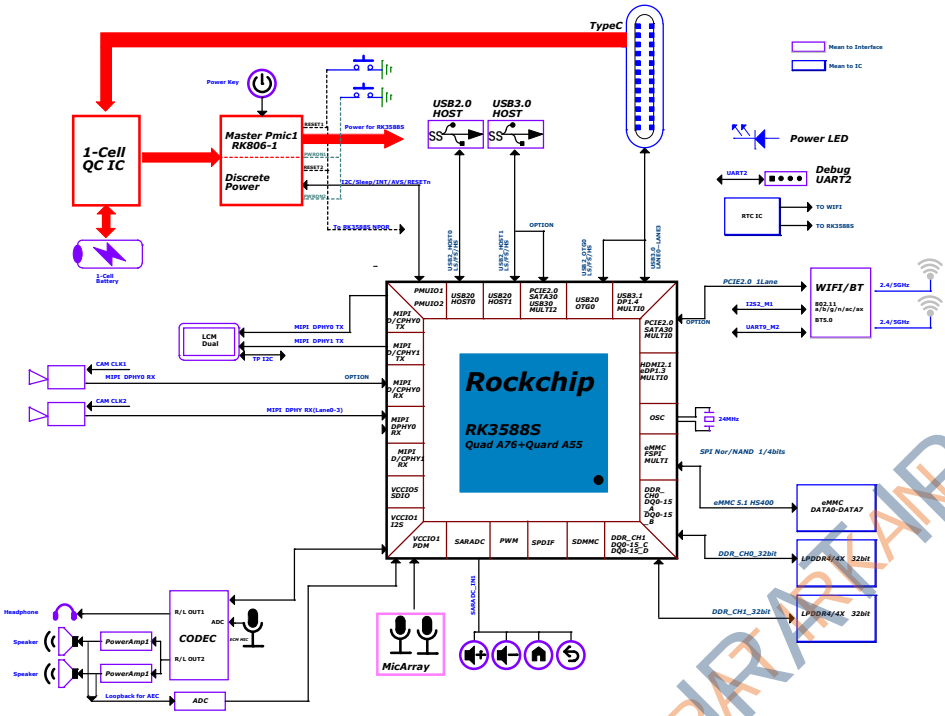
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	01.Index and Notes				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	2 of 32

Revision History

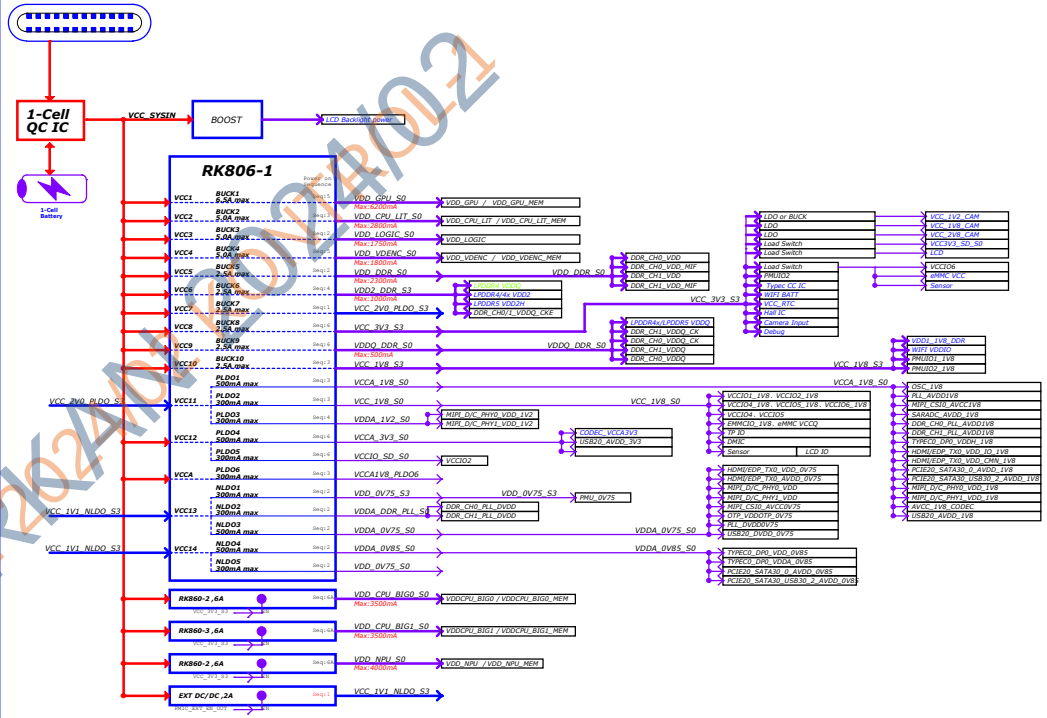
Version	Date	By	Change Dsecription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.Wei	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203，L2205，L2207，L2300，L2301，L2302电感由0.22uH(TDK)改为0.24uH(Sunlord); L2201的电感由0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。	

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	02.Revision History				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	3 of 32

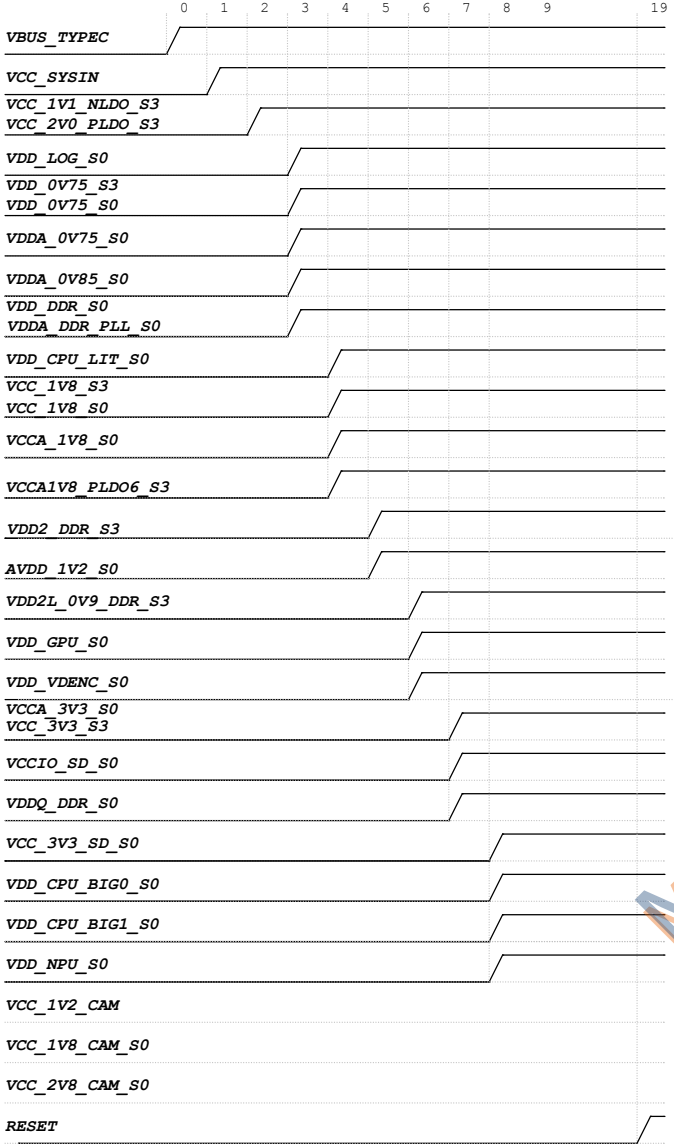
RK3588S Tablet Demo Block Diagram for 1-Cell Charger



Power tree for 1-Cell Charger



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	05.System Power Sequence				
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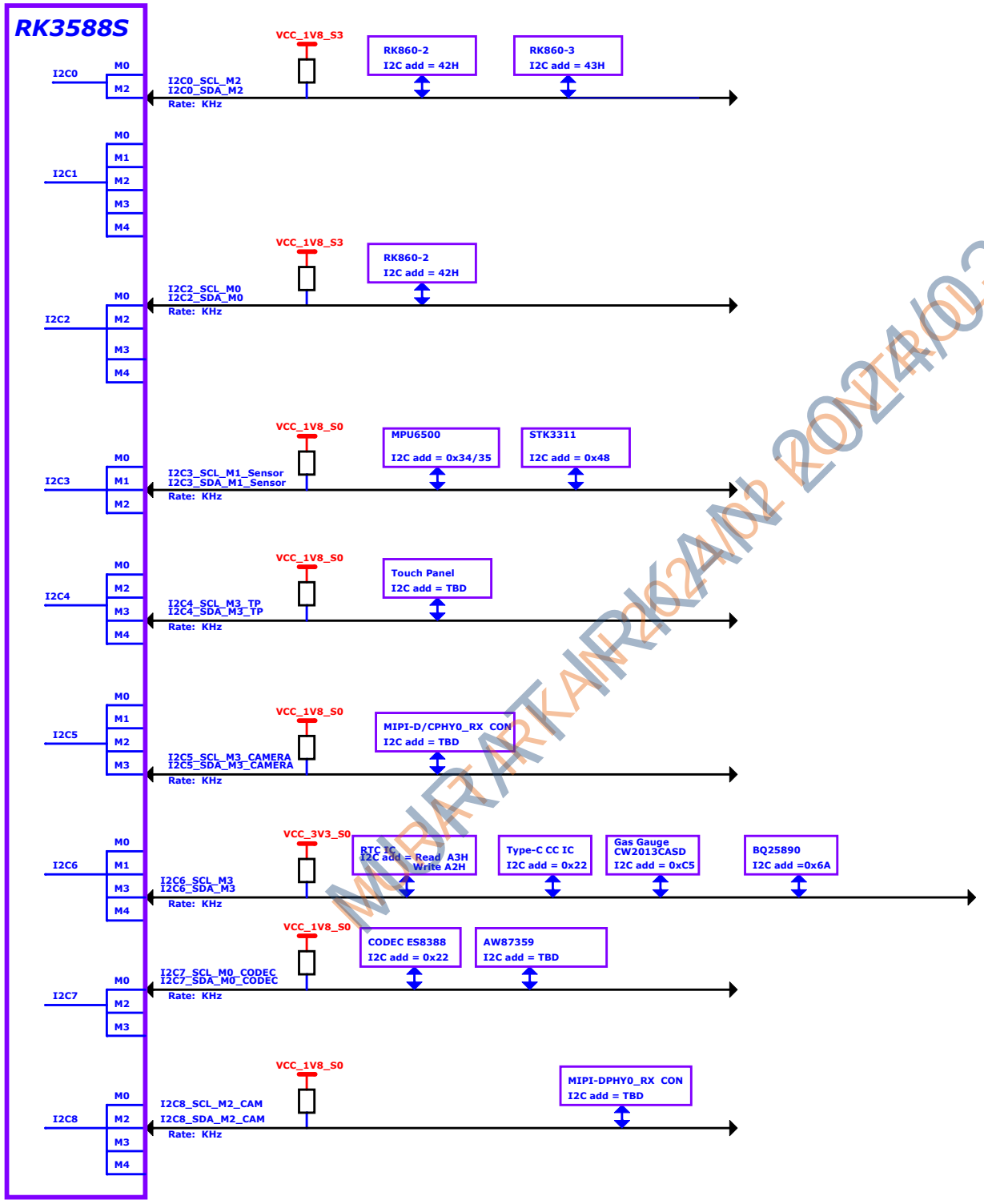
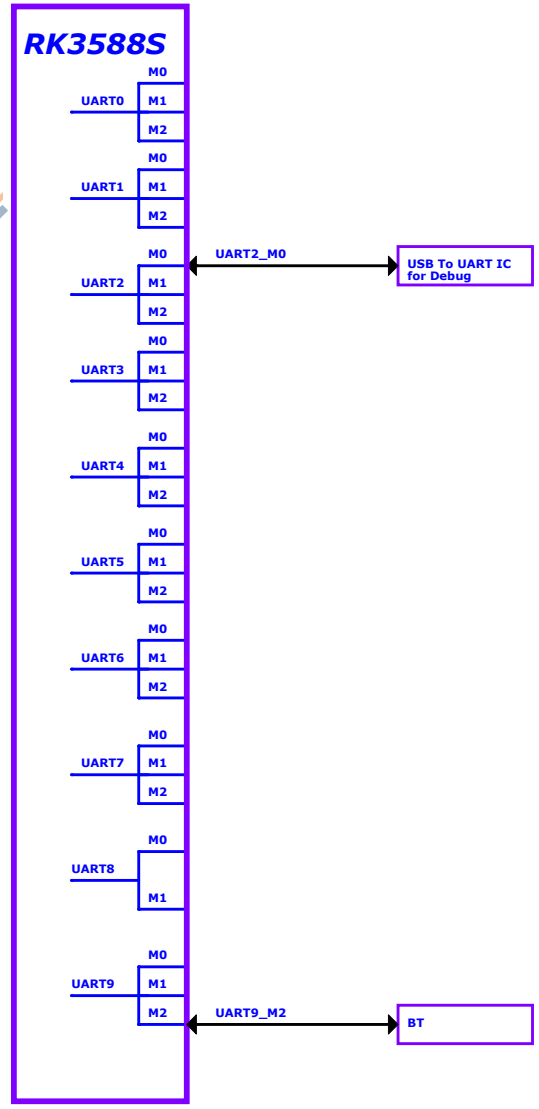
I2C MAP



UART MAP



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Demo
File:	06.Lower-Speed Bus Map
Date:	Monday, January 24, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
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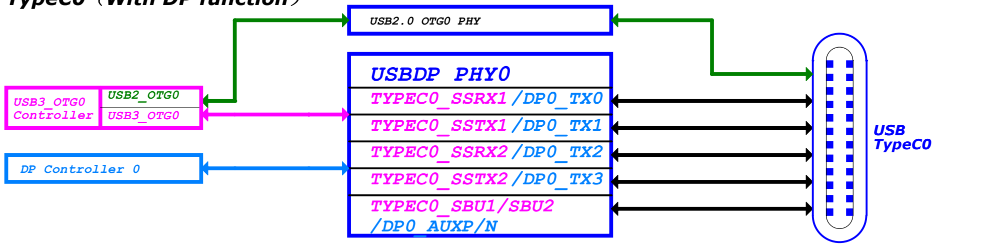
USB Controller Configure Table

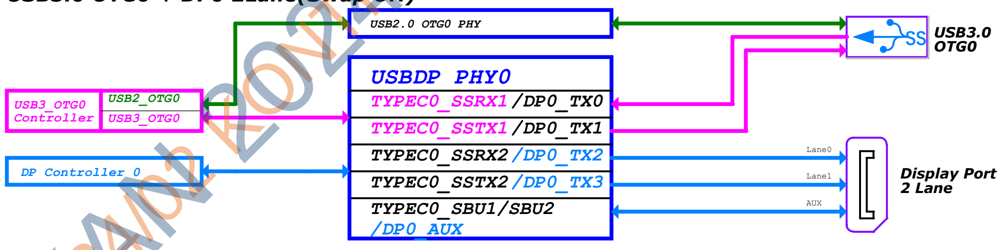
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG2 Device or Host			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

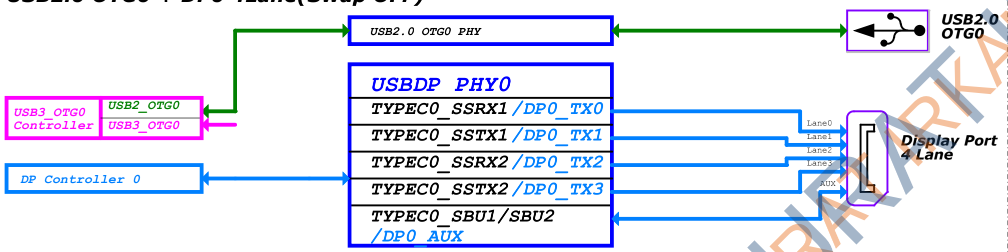
Config0:
TypeC0（With DP function）



Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)

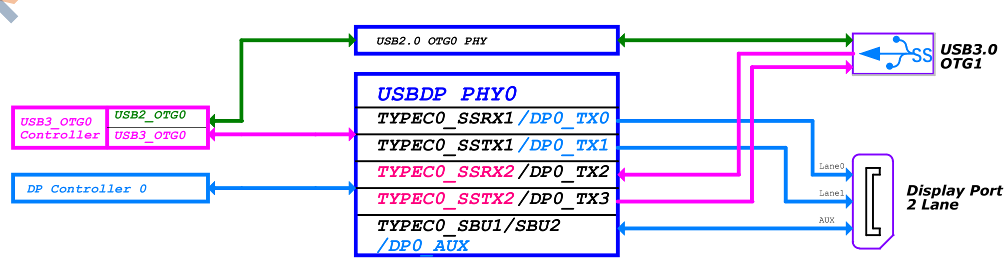


Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)

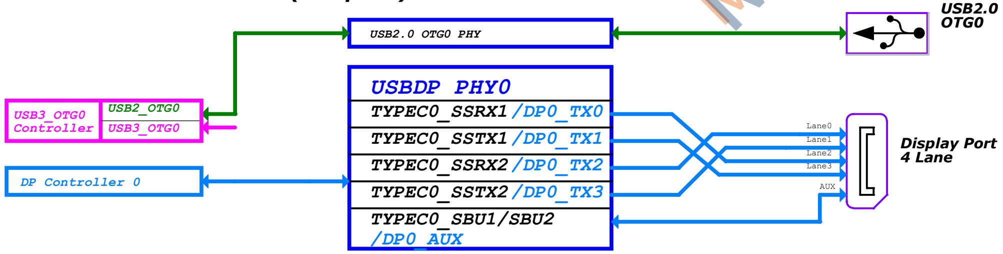


USB2.0 OTG0 PHY
USBDP PHY0
TYPEC0_SSRX1/DP0_TX0
TYPEC0_SSTX1/DP0_TX1
TYPEC0_SSRX2/DP0_TX2
TYPEC0_SSTX2/DP0_TX3
TYPEC0_SBU1/SBU2
/DP0_AUX
USB3_OTG0 Controller
USB2_OTG0
USB3_OTG0
DP Controller 0
USB2.0 OTG0
Lane0
Lane1
Lane2
Lane3
AUX
Display Port 4 Lane

Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)

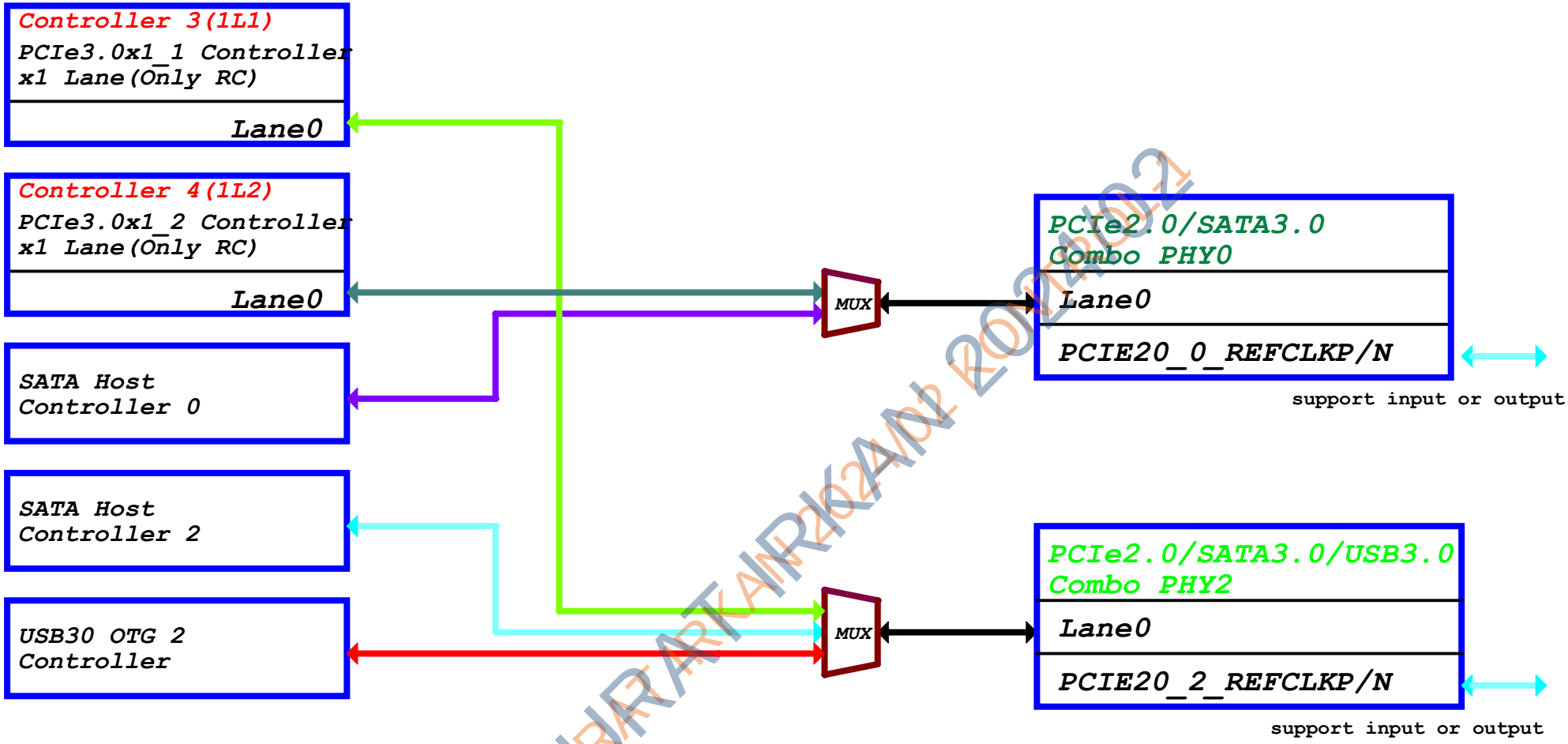


Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



USB2.0 OTG0 PHY
USBDP PHY0
TYPEC0_SSRX1/DP0_TX0
TYPEC0_SSTX1/DP0_TX1
TYPEC0_SSRX2/DP0_TX2
TYPEC0_SSTX2/DP0_TX3
TYPEC0_SBU1/SBU2
/DP0_AUX
USB3_OTG0 Controller
USB2_OTG0
USB3_OTG0
DP Controller 0
USB2.0 OTG0
Lane0
Lane1
Lane2
Lane3
AUX
Display Port 4 Lane

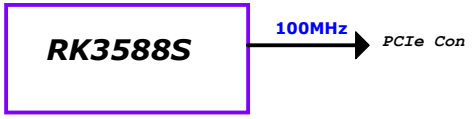
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

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RK3588S (Power&Gnd)

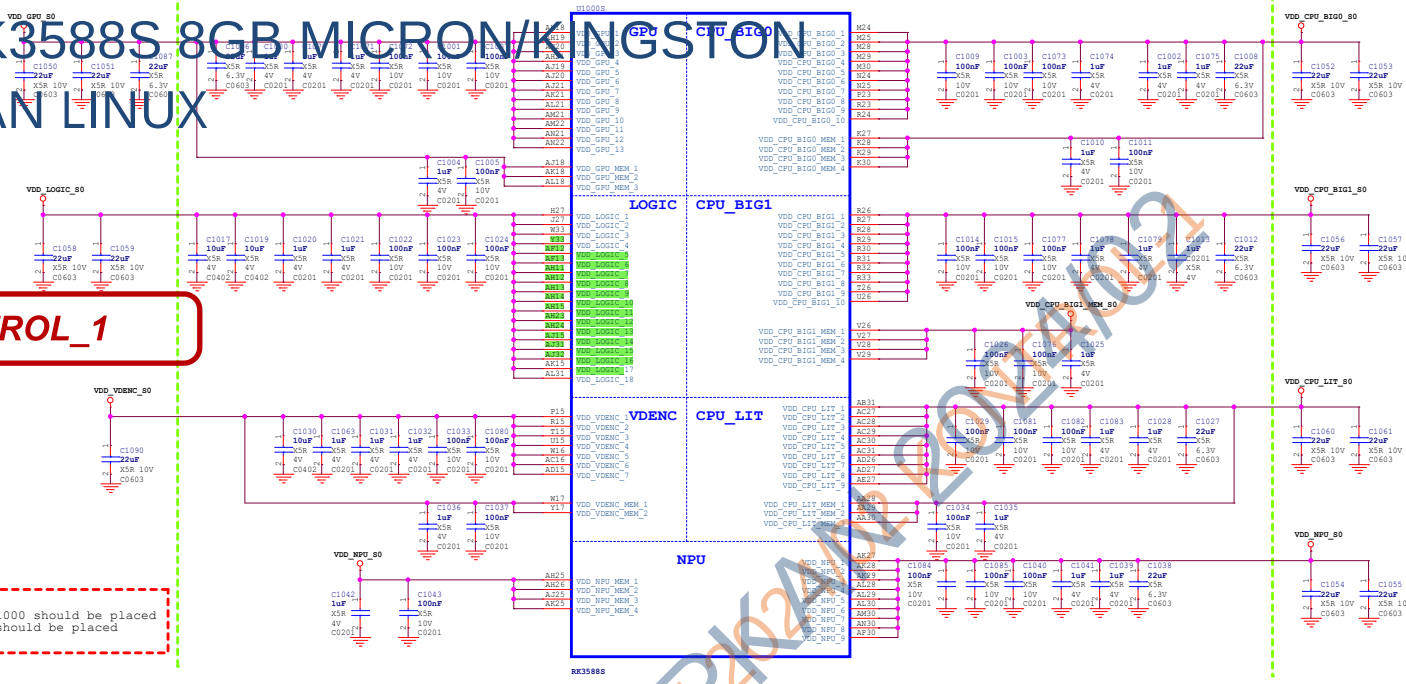
lokum notebook

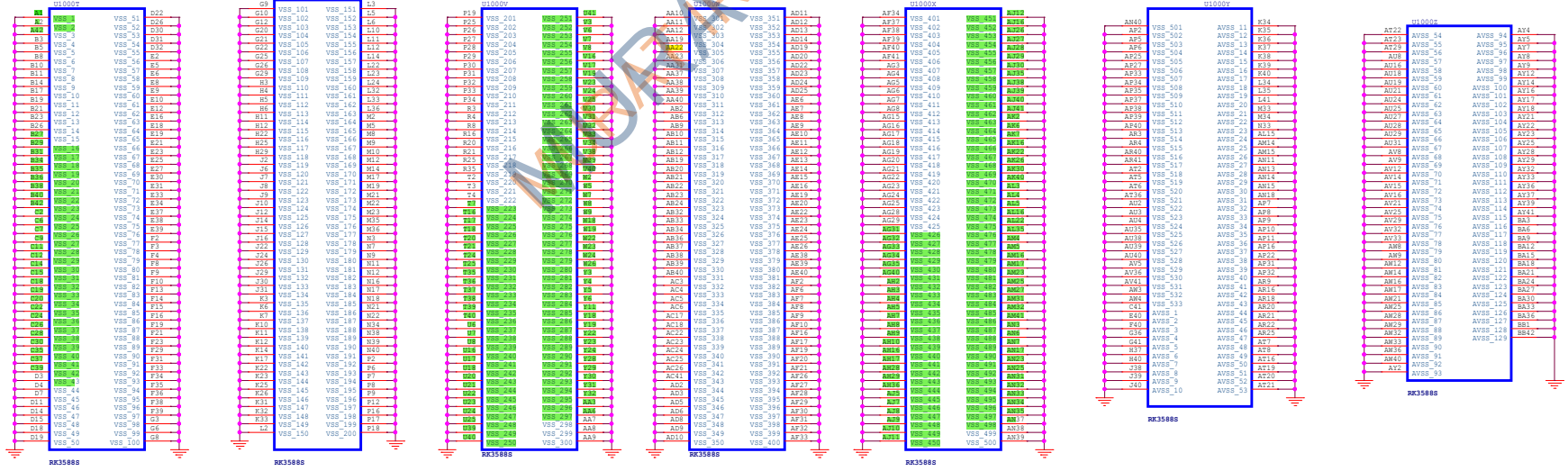
ROCKCHIP RK3588S 8GB MICRON/KINGSTON LPDDR4 DEBIAN LINUX ANDROID 12

SİSTEM_KONTROL_1

kapasitörler yeşil cizgi yi gecmeden yerleştirilmeli u1000 altına doğru.diger cap lar u1000 yakın olmalı.

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package





Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Demo
File:	10.RK3588S_Power/GND
Date:	Friday, January 07, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
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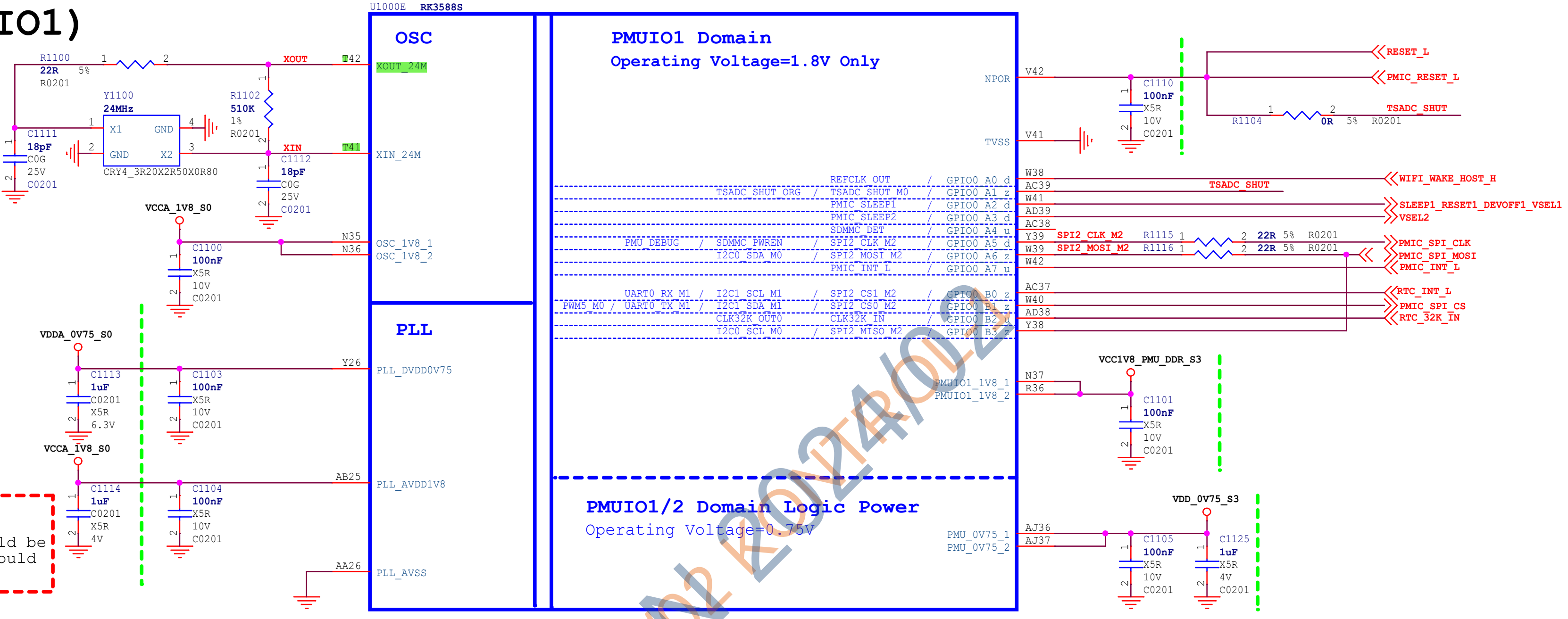
RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

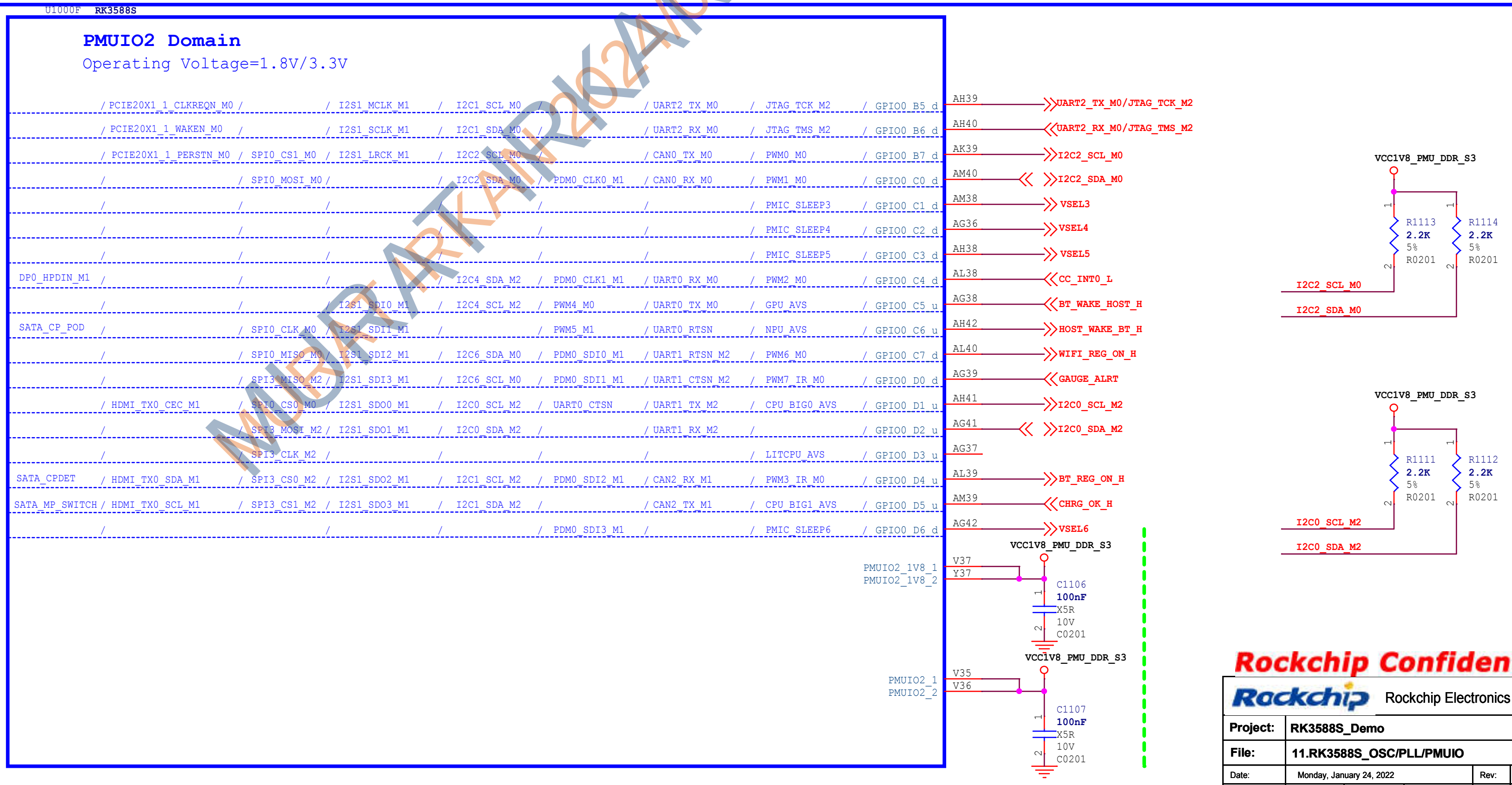
CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



U1000E RK3588S
OSC
XOUT_24M
XIN_24M
OSC_1V8_1
OSC_1V8_2
PLL
PLL_DVDD0V75
PLL_AVDD1V8
PLL_AVSS
PMUIO1 Domain
Operating Voltage=1.8V Only
NPOR
TVSS
PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V
R1100 22R 5% R0201
Y1100 24MHz
CRY4_3R20X2R50X0R80
R1102 510K 1% R0201
C1111 18pF C0G 25V C0201
C1112 18pF C0G 25V C0201
VCCA_1V8_S0
VDDA_0V75_S0
VCC1V8_PMU_DDR_S3
VDD_0V75_S3
RESET_L
PMIC_RESET_L
TSADC_SHUT
WIFI_WAKE_HOST_H
SLEEP1_RESET1_DEVOFF1_VSEL1
VSEL2
PMIC_SPI_CLK
PMIC_SPI_MOSI
PMIC_INT_L
RTC_INT_L
PMIC_SPI_CS
RTC_32K_IN

RK3588S(PMUIO2)



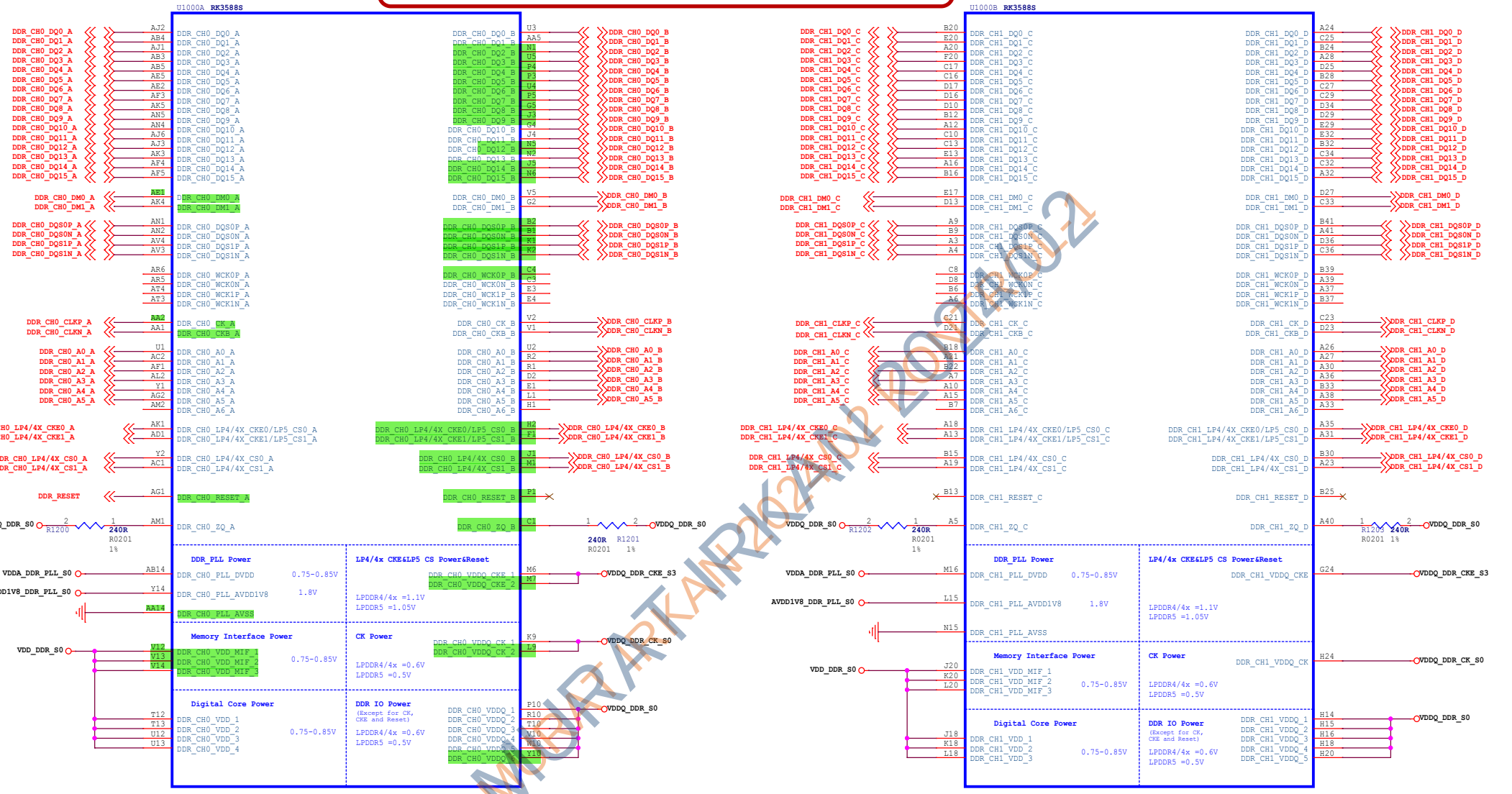
U1000F RK3588S
PMUIO2 Domain
Operating Voltage=1.8V/3.3V
UART2_TX_M0/JTAG_TCK_M2
UART2_RX_M0/JTAG_TMS_M2
I2C2_SCL_M0
I2C2_SDA_M0
VSEL3
VSEL4
VSEL5
CC_INT0_L
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_REG_ON_H
GAUGE_ALRT
I2C0_SCL_M2
I2C0_SDA_M2
BT_REG_ON_H
CHRG_OK_H
VSEL6
PMUIO2_1V8_1
PMUIO2_1V8_2
PMUIO2_1
PMUIO2_2
VCC1V8_PMU_DDR_S3
R1113 2.2K 5% R0201
R1114 2.2K 5% R0201
R1111 2.2K 5% R0201
R1112 2.2K 5% R0201

Rockchip Confidential

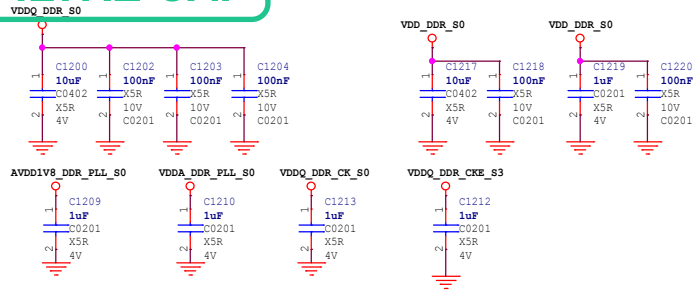
Rockchip Electronics Co., Ltd

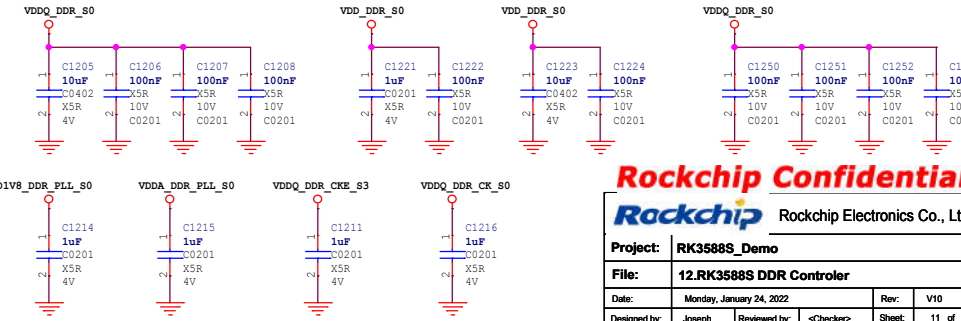
Project:	RK3588S_Demo		
File:	11.RK3588S_OSC/PLL/PMUIO		
Date:	Monday, January 24, 2022	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet:	10 of 32

RK3588S (DDR PHY) LPDDR4 MICRON-SAMSUNG VEYA KINGSTON



LPDDR4 FILTRE CAP

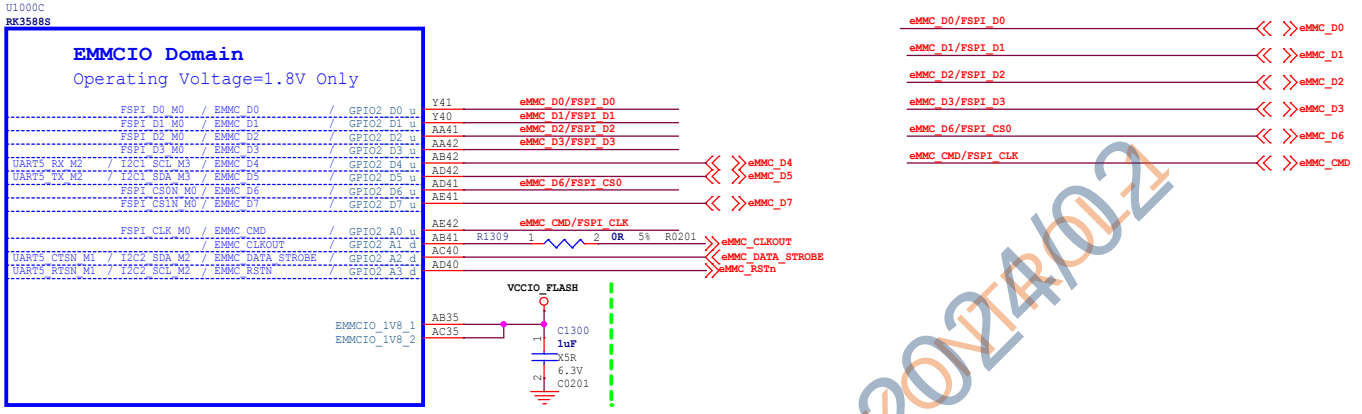




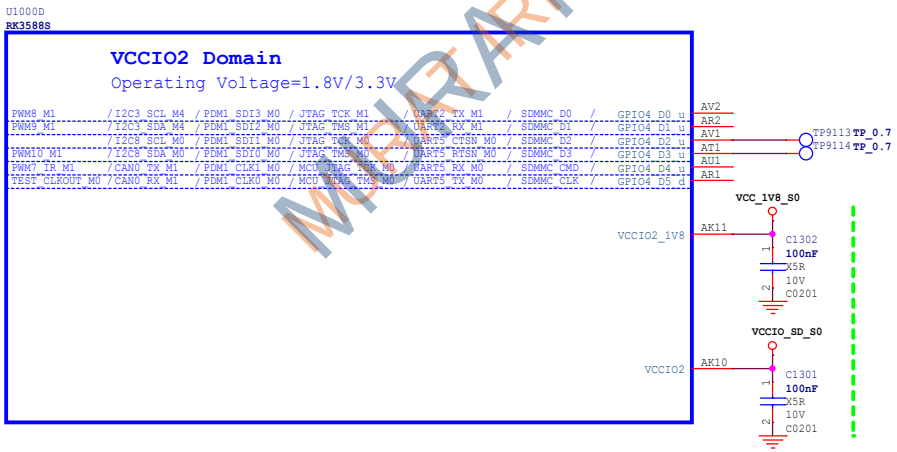
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	12.RK3588S DDR Controler				
Date:	Monday, January 24, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	11 of 32

RK3588S(EMMCIO Domain)



RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	13.RK3588S Flash/SD Controller				
Date:	Wednesday, January 12, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	12 of 32

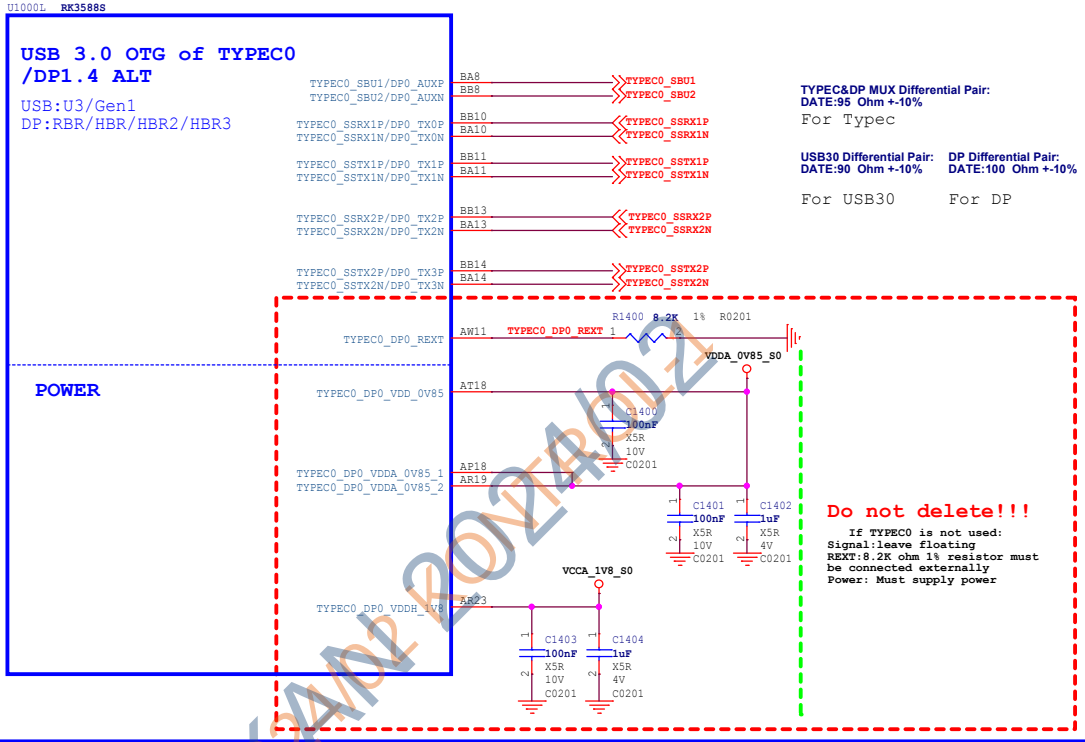
RK3588S(USB3.0/DP1.4)

USB_3.0 PORTLAR

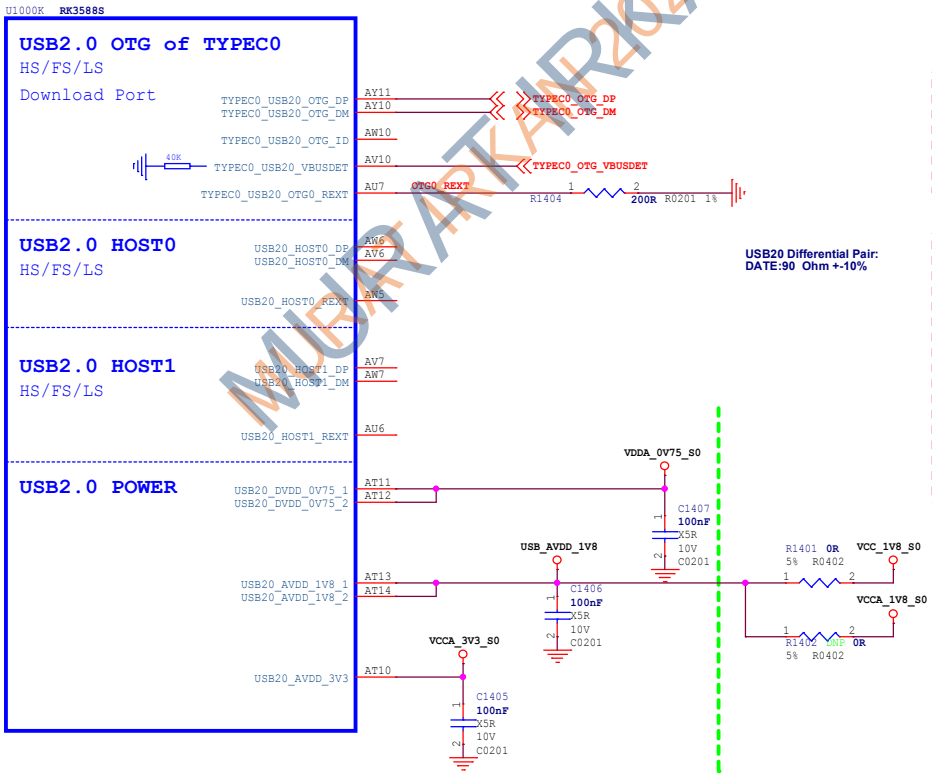
USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

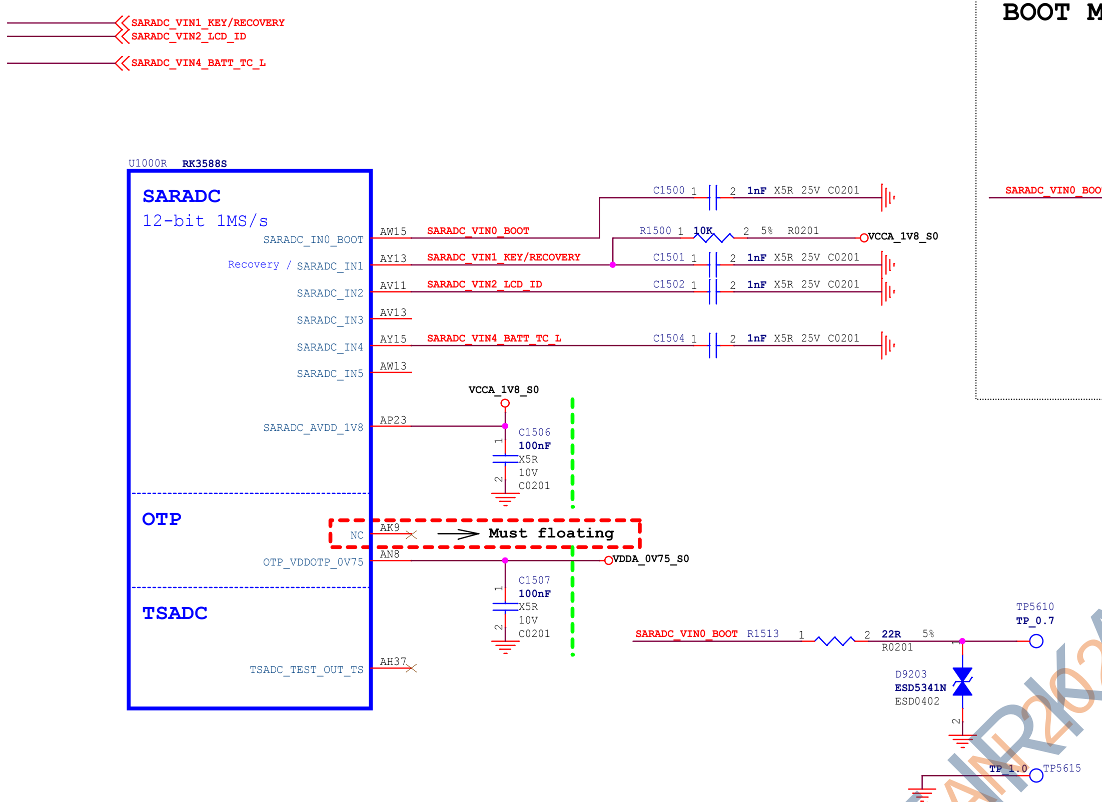
USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

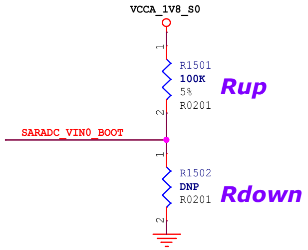
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	14.RK3588S_USB20/USB30/DP PHY				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 32

RK3588S(SARADC/OTP/TSADC)



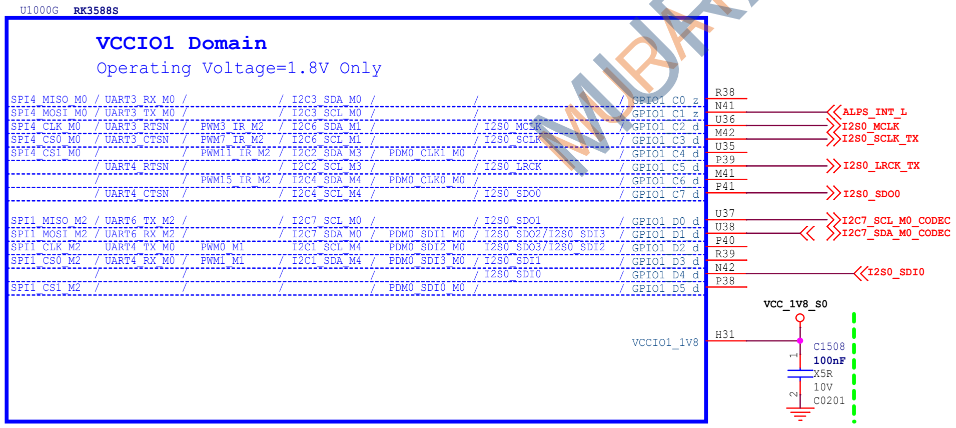
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_LCD_ID
SARADC_VIN4_BATT_TC_L
U1000R RK3588S
SARADC
12-bit 1MS/s
SARADC_IN0_BOOT
Recovery / SARADC_IN1
SARADC_IN2
SARADC_IN3
SARADC_IN4
SARADC_IN5
SARADC_AVDD_1V8
OTP
NC
OTP_VDDOTP_0V75
TSADC
TSADC_TEST_OUT_TS
Must floating
VCCA_1V8_S0
VDDA_0V75_S0
TP5610
TP_0.7
D9203
ESD5341N
ESD0402
TP5615

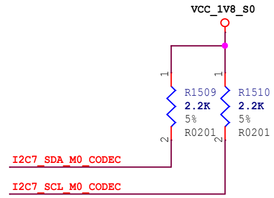
BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

RK3588S(VCCIO1 Domain)



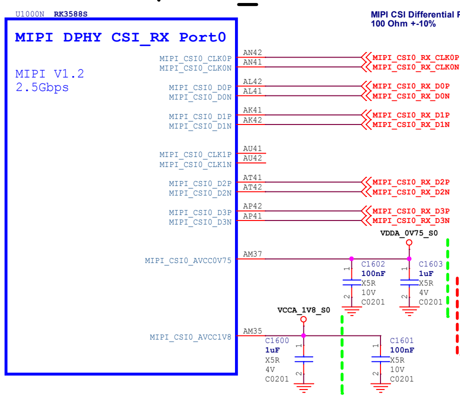


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd

Project:	RK3588S_Demo
File:	15.RK3588S_SARADC/1.8V GPIO
Date:	Friday, January 14, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	14 of 32

RK3588S(MIPI_DPHY CSI0 RX)



U1000N RK3588S
MIPI CSI Differential Pair:
100 Ohm +-10%
MIPI DPHY CSI_RX Port0
MIPI V1.2
2.5Gbps
MIPI_CSI0_CLK0P AN42 MIPI_CSI0_RX_CLK0P
MIPI_CSI0_CLK0N AN41 MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P AL42 MIPI_CSI0_RX_D0P
MIPI_CSI0_D0N AL41 MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P AK41 MIPI_CSI0_RX_D1P
MIPI_CSI0_D1N AK42 MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P AU41
MIPI_CSI0_CLK1N AU42
MIPI_CSI0_D2P AT41 MIPI_CSI0_RX_D2P
MIPI_CSI0_D2N AT42 MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P AP42 MIPI_CSI0_RX_D3P
MIPI_CSI0_D3N AP41 MIPI_CSI0_RX_D3N
VDDA_0V75_S0
MIPI_CSI0_AVCC0V75 AM37
C1602 100nF X5R 10V C0201
C1603 1uF X5R 4V C0201
VCCA_1V8_S0
MIPI_CSI0_AVCC1V8 AM35
C1600 1uF X5R 4V C0201
C1601 100nF X5R 10V C0201

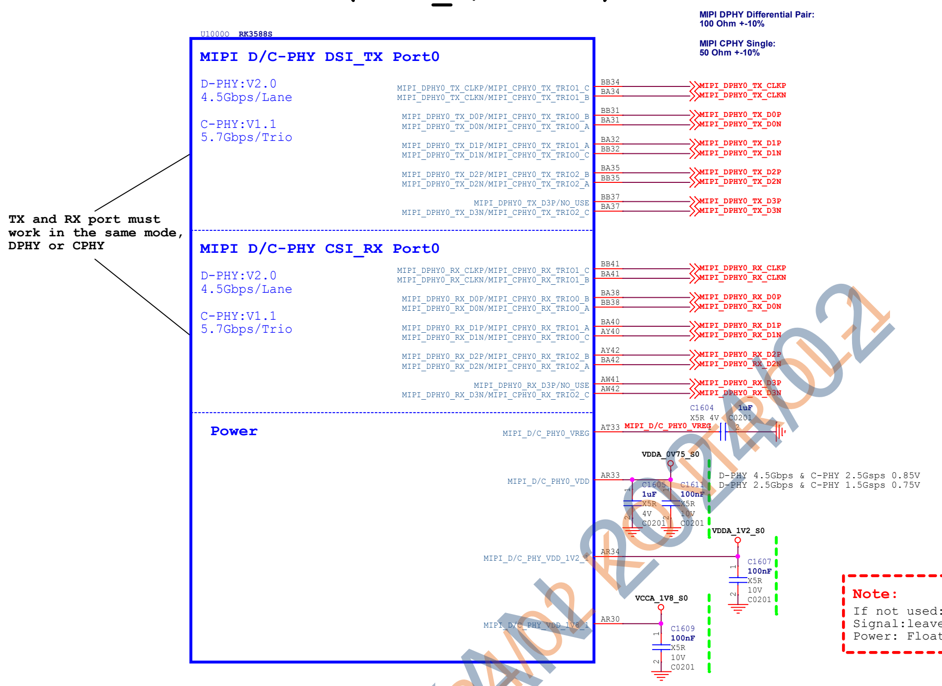
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
	+	
	Sensor2 x2Lane	*MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

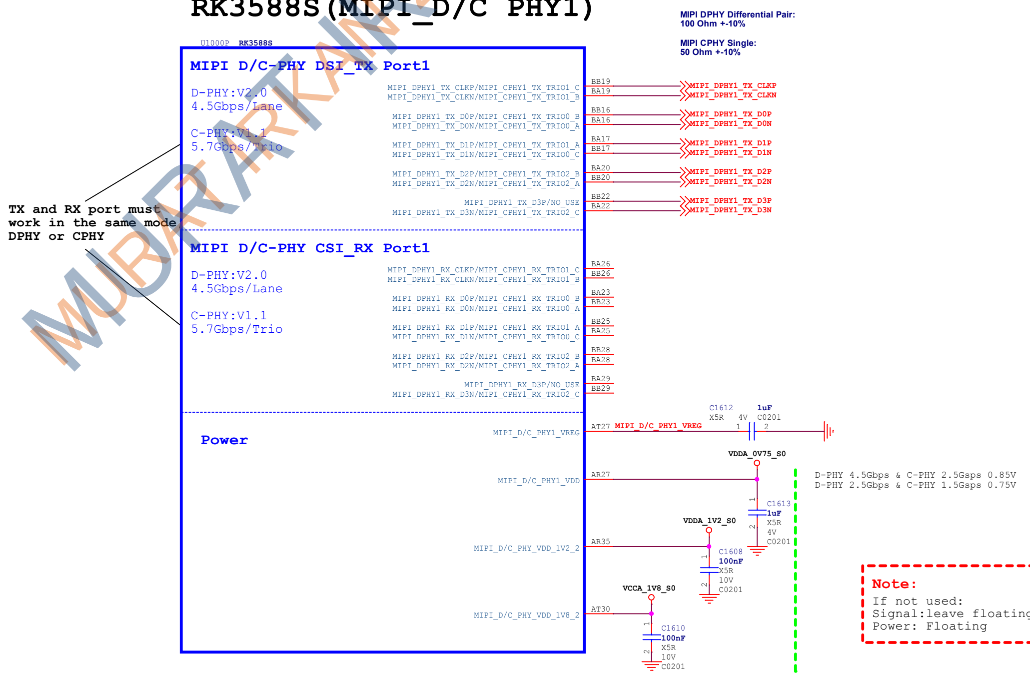
RK3588S(MIPI_D/C PHY0)



U1000O RK3588S
MIPI DPHY Differential Pair:
100 Ohm +-10%
MIPI CPHY Single:
50 Ohm +-10%
MIPI D/C-PHY DSI_TX Port0
D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio
MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C BB34 MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B BA34 MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B BB31 MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A BA31 MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A BA32 MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C BB32 MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B BA35 MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A BB35 MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE BB37 MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C BA37 MIPI_DPHY0_TX_D3N
TX and RX port must work in the same mode, DPHY or CPHY
MIPI D/C-PHY CSI_RX Port0
D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio
MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C BB41 MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B BA41 MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B BA38 MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A BB38 MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A BA40 MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C AY40 MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B AY42 MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A BA42 MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE AW41 MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C AW42 MIPI_DPHY0_RX_D3N
Power
MIPI_D/C_PHY0_VREG AT33 MIPI_D/C_PHY0_VREG
C1604 1uF X5R 4V C0201
VDDA_0V75_S0
MIPI_D/C_PHY0_VDD AR33
C1605 1uF X5R 4V C0201
C1611 100nF X5R 10V C0201
D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V
VDDA_1V2_S0
MIPI_D/C_PHY_VDD_1V2 AR34
C1607 100nF X5R 10V C0201
VCCA_1V8_S0
MIPI_D/C_PHY_VDD_1V8 AR30
C1609 100nF X5R 10V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)



U1000P RK3588S
MIPI DPHY Differential Pair:
100 Ohm +-10%
MIPI CPHY Single:
50 Ohm +-10%
MIPI D/C-PHY DSI_TX Port1
D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio
MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C BB19 MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B BA19 MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B BB16 MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A BA16 MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A BA17 MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C BB17 MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B BA20 MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A BB20 MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P/NO_USE BB22 MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C BA22 MIPI_DPHY1_TX_D3N
TX and RX port must work in the same mode DPHY or CPHY
MIPI D/C-PHY CSI_RX Port1
D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio
MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C BA26
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B BB26
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B BA23
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A BB23
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A BB25
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C BA25
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B BB28
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A BA28
MIPI_DPHY1_RX_D3P/NO_USE BA29
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C BB29
Power
MIPI_D/C_PHY1_VREG AT27 MIPI_D/C_PHY1_VREG
C1612 1uF X5R 4V C0201
VDDA_0V75_S0
MIPI_D/C_PHY1_VDD AR27
C1613 1uF X5R 4V C0201
D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V
VDDA_1V2_S0
MIPI_D/C_PHY_VDD_1V2_2 AR35
C1608 100nF X5R 10V C0201
VCCA_1V8_S0
MIPI_D/C_PHY_VDD_1V8_2 AT30
C1610 100nF X5R 10V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	16.RK3588S_MIPI Interface				
Date:	Monday, February 21, 2022		Rev:	V10	
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	15 of 32

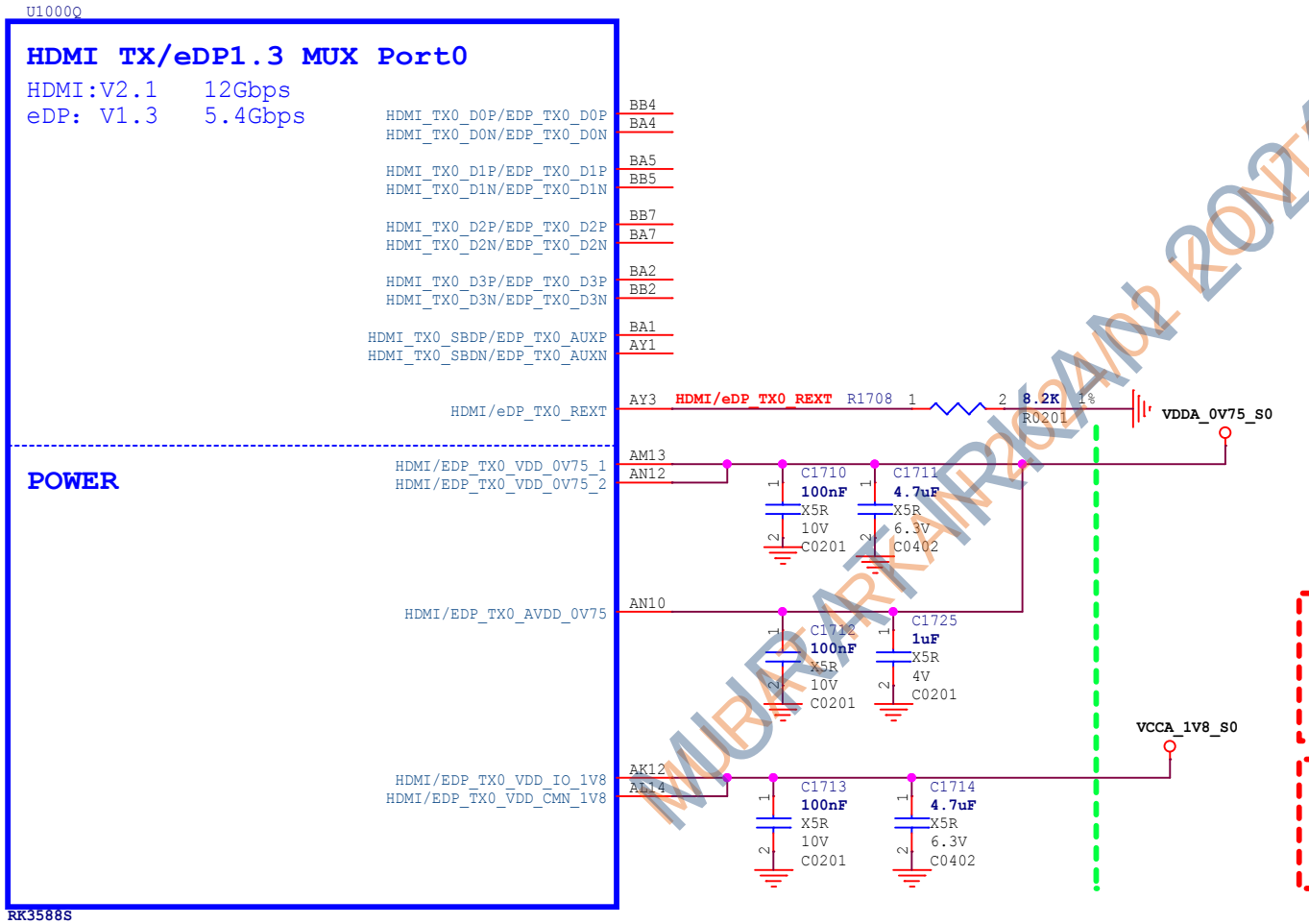
RK3588S(HDMI2.1 TX/eDP1.3 TX)

HDMİ VERSIYON 2.1

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm ±10%

HDMI TX
100 Ohm ±10%



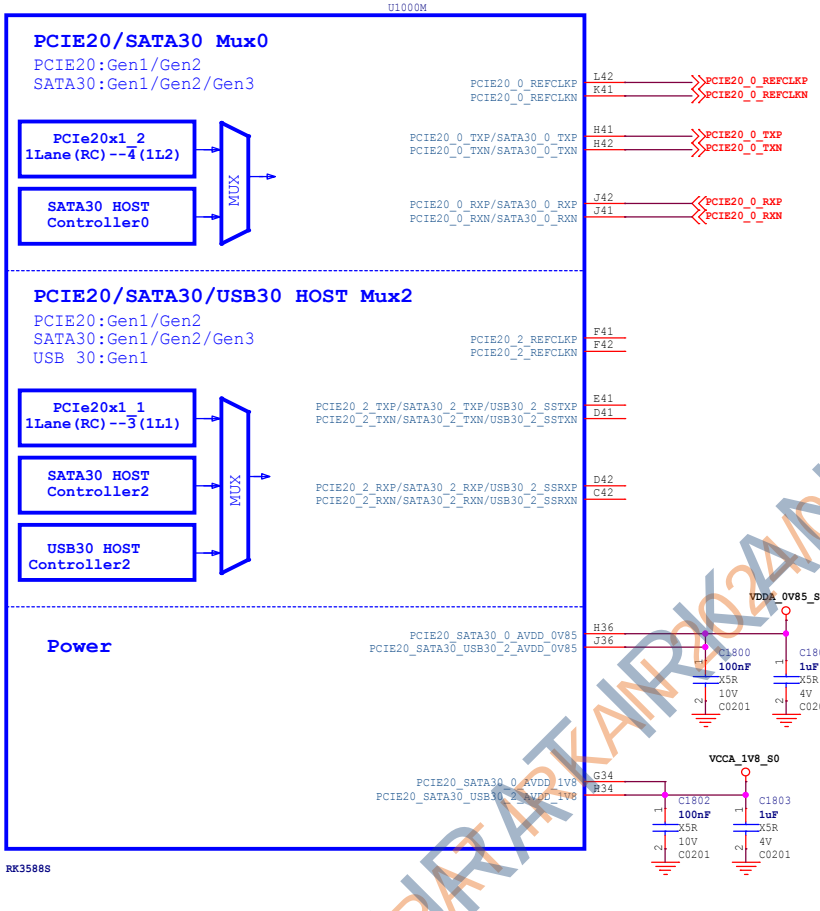
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	17.RK3588S_HDMI/eDP Interface				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	16 of 32

RK3588S(PCIE20/SATA30/USB30)

PCIE20 VE SATA PORT USB 3.0



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

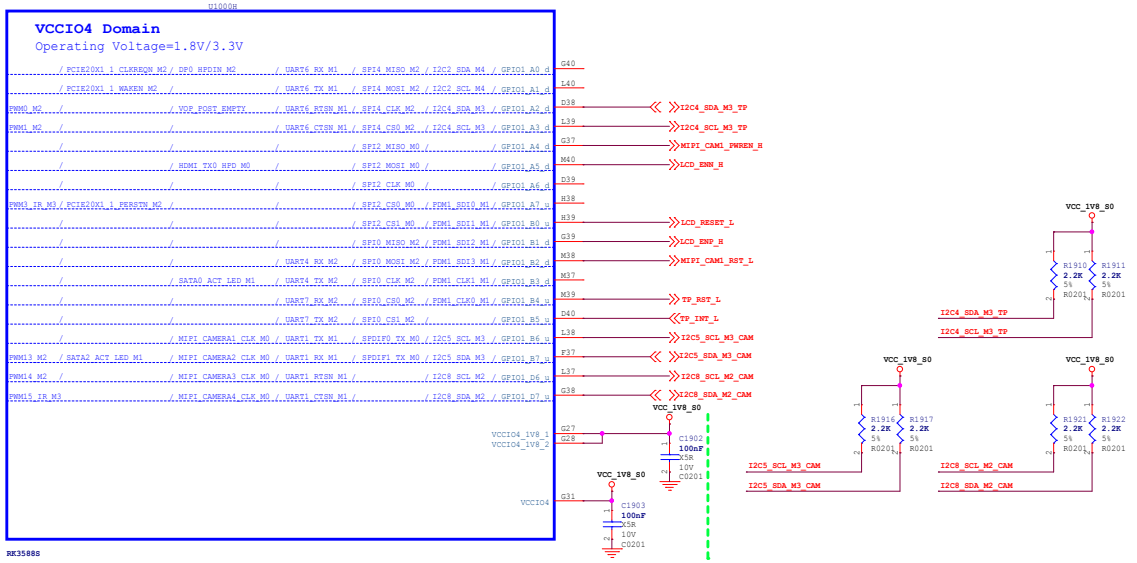
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

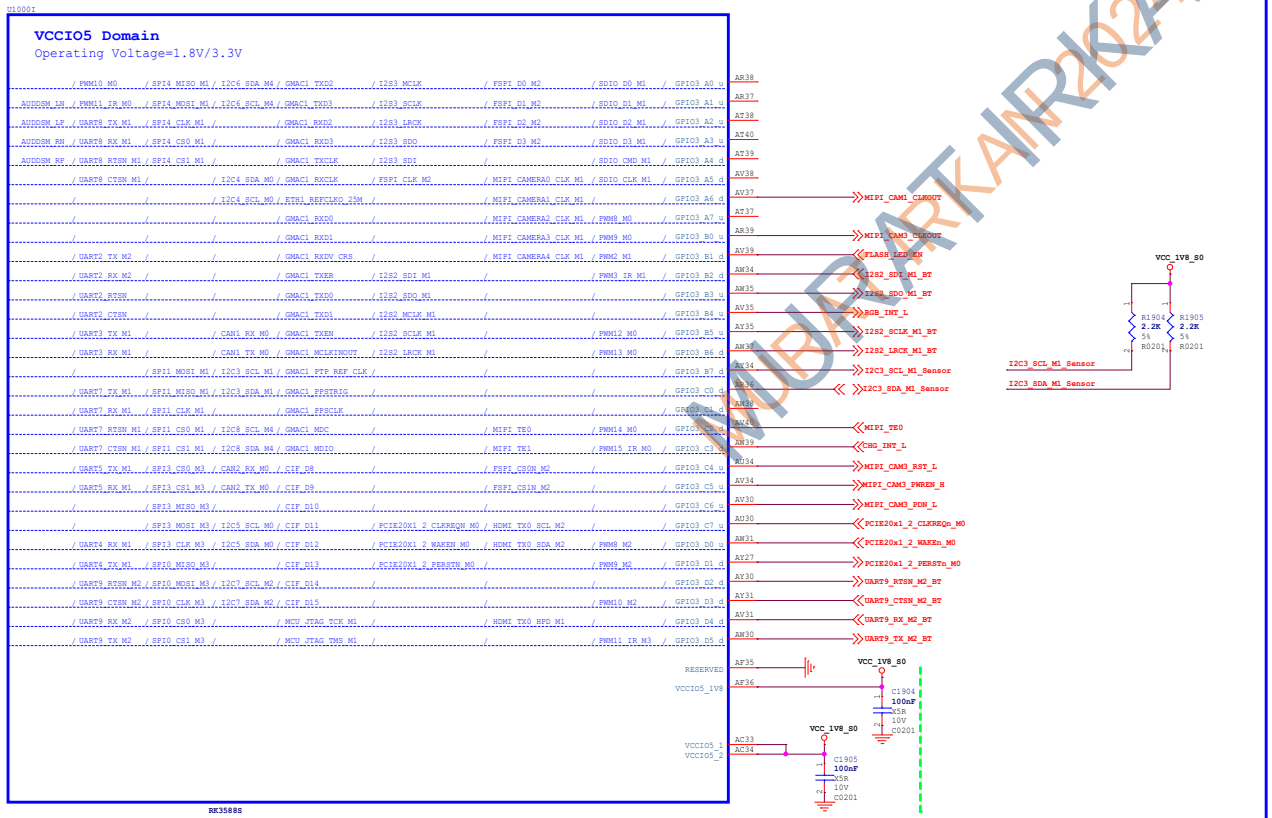
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	18.RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 32

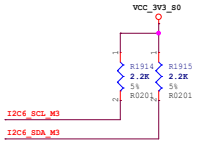
RK3588S(VCCIO4 Domain)



RK3588S(VCCIO6 Domain)

RK3588S(VCCIO5 Domain)

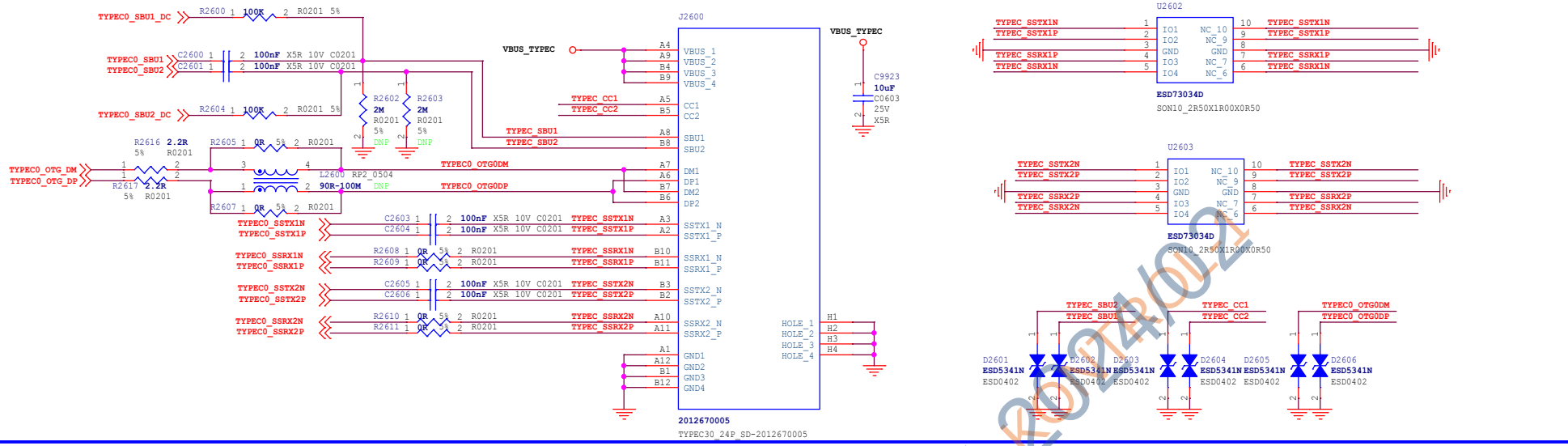




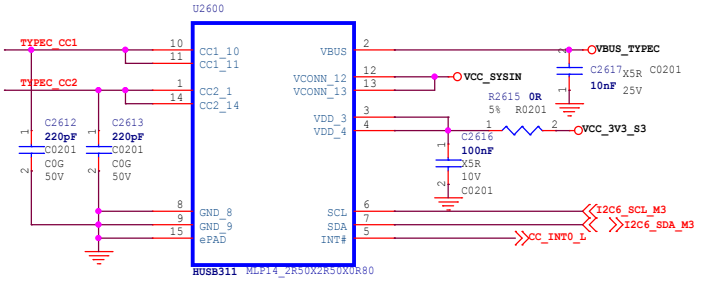
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Demo		
File:	19.RK3588S GPIO		
Date:	Friday, January 07, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet 18 of 32

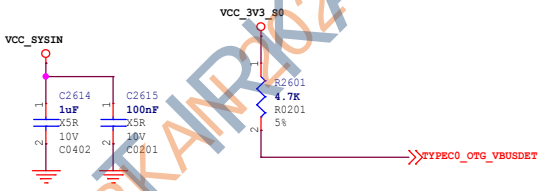
USB Type-C Port



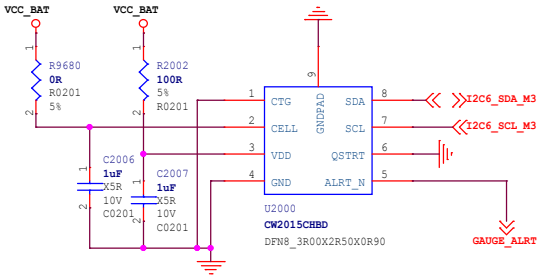
USB Type-C CC CTRL



USB Detection

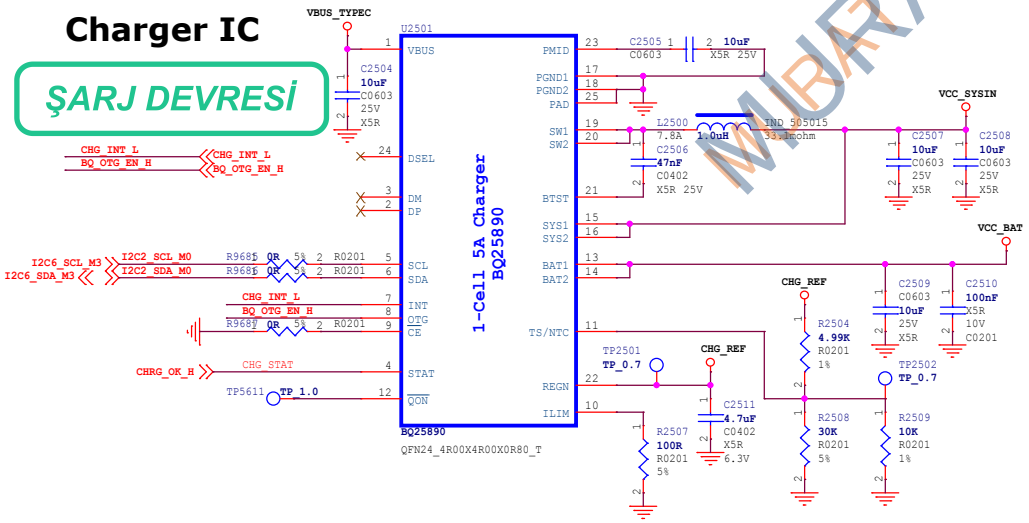


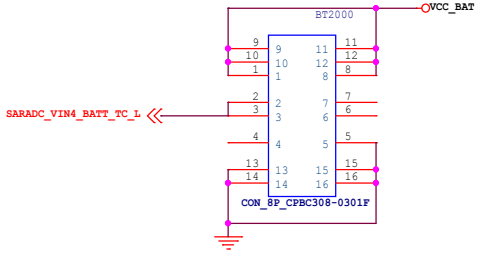
Gas Gauge



Charger IC

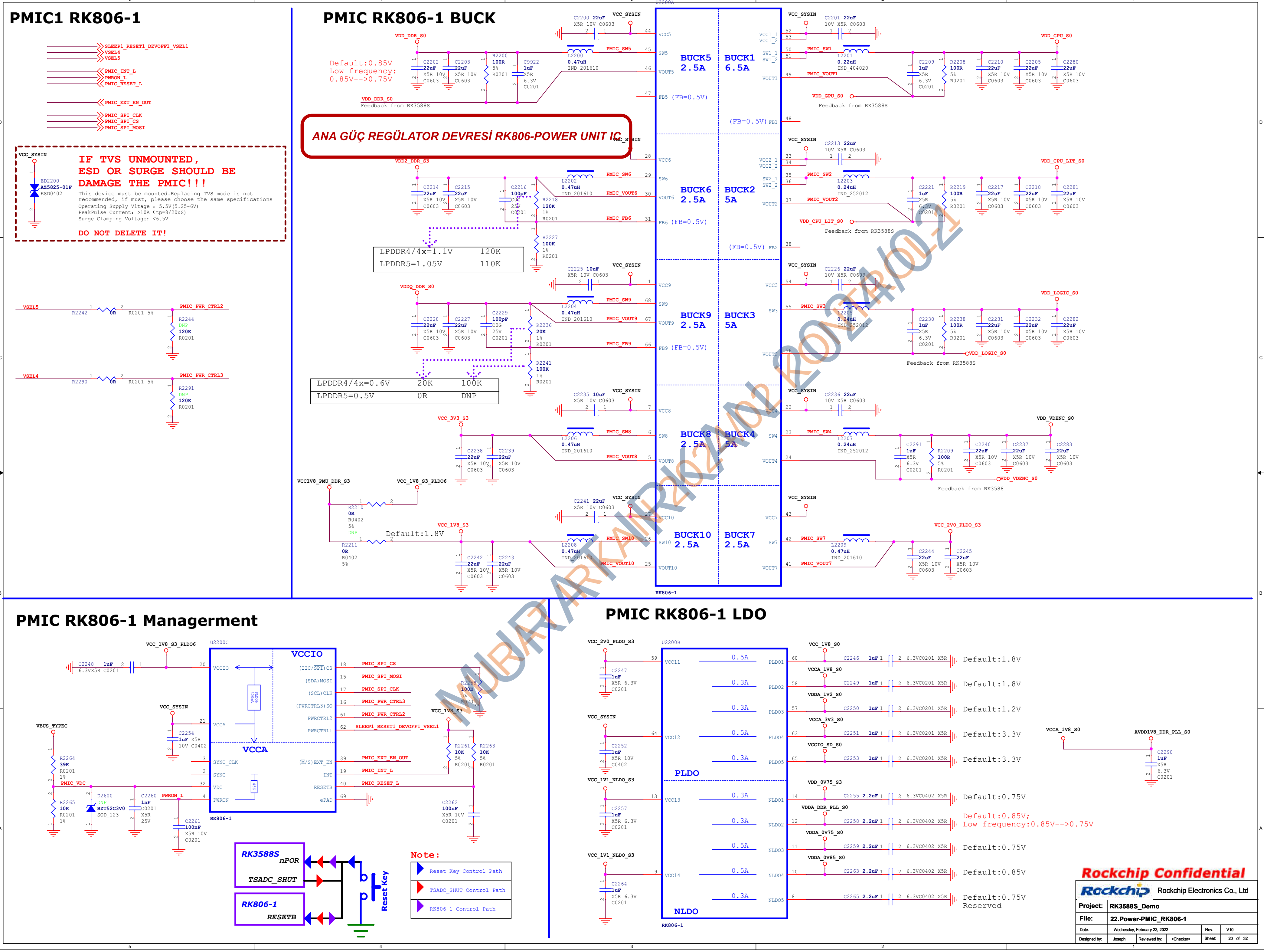
ŞARJ DEVRESİ





Rockchip Confidential

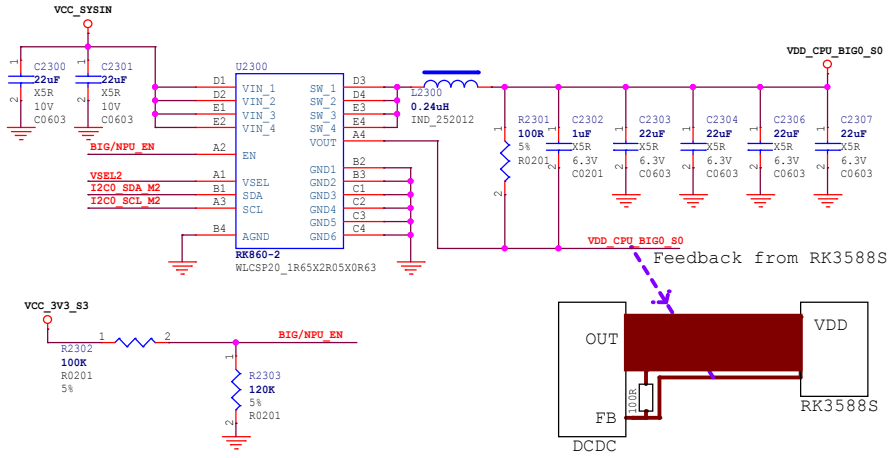
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	20.Power_1Cell_QC				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	19 of 32



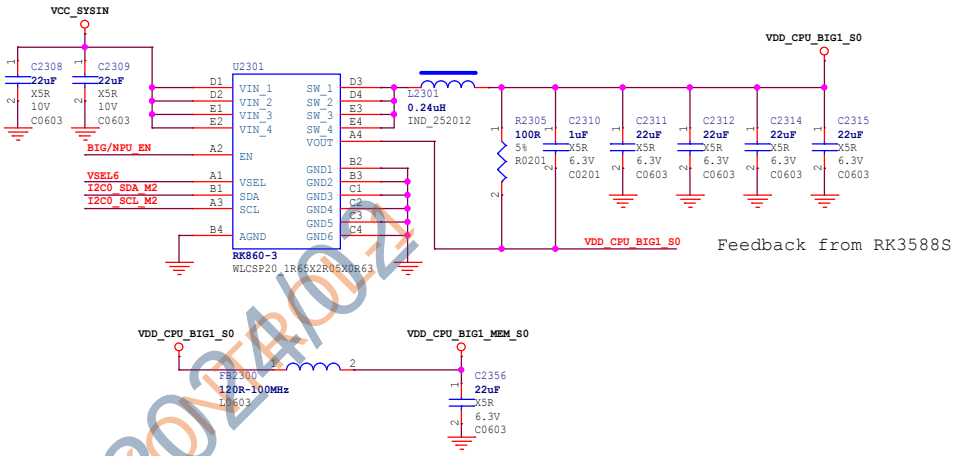
PMIC1 RK806-1
SLEEP1_RESET1_DEVOFF1_VSEL1
VSEL4
VSEL5
PMIC_INT_L
PWRON_L
PMIC_RESET_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI
IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!
This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V
DO NOT DELETE IT!
ED2200
AZ5825-01F
ESD0402
VCC_SYSIN
VSEL5
R2242 0R R0201 5%
PMIC_PWR_CTRL2
R2244 DNP 120K R0201
VSEL4
R2290 0R R0201 5%
PMIC_PWR_CTRL3
R2291 DNP 120K R0201
PMIC RK806-1 BUCK
ANA GÜÇ REGÜLATOR DEVRESİ RK806-POWER UNIT IC
Default:0.85V
Low frequency:
0.85V-->0.75V
VDD_DDR_S0
Feedback from RK3588S
VDD2_DDR_S3
LPDDR4/4x=1.1V 120K
LPDDR5=1.05V 110K
VDDQ_DDR_S0
LPDDR4/4x=0.6V 20K 100K
LPDDR5=0.5V 0R DNP
VCC_3V3_S3
VCC1V8_PMU_DDR_S3
VCC_1V8_S3_PLDO6
Default:1.8V
VCC_1V8_S3
BUCK5 2.5A
BUCK1 6.5A
BUCK6 2.5A
BUCK2 5A
BUCK9 2.5A
BUCK3 5A
BUCK8 2.5A
BUCK4 5A
BUCK10 2.5A
BUCK7 2.5A
FB5 (FB=0.5V)
(FB=0.5V) FB1
FB6 (FB=0.5V)
(FB=0.5V) FB2
FB9 (FB=0.5V)
RK806-1
VDD_GPU_S0
VDD_CPU_LIT_S0
VDD_LOGIC_S0
VDD_VDENC_S0
VCC_2V0_PLDO_S3
Feedback from RK3588S
Feedback from RK3588
PMIC RK806-1 Management
VCC_1V8_S3_PLDO6
VCCIO
VCCA
VBUS_TYPEC
PMIC_VDC
PWRON_L
RK3588S nPOR
TSADC_SHUT
RK806-1 RESETB
Reset Key
Note:
Reset Key Control Path
TSADC_SHUT Control Path
RK806-1 Control Path
PMIC RK806-1 LDO
VCC_2V0_PLDO_S3
VCC_SYSIN
VCC_1V1_NLDO_S3
PLDO
NLDO
VCC_1V8_S0 Default:1.8V
VCCA_1V8_S0 Default:1.8V
VDDA_1V2_S0 Default:1.2V
VCCA_3V3_S0 Default:3.3V
VCCIO_SD_S0 Default:3.3V
VDD_0V75_S3 Default:0.75V
VDDA_DDR_PLL_S0 Default:0.85V; Low frequency:0.85V-->0.75V
VDDA_0V75_S0 Default:0.75V
VDDA_0V85_S0 Default:0.85V
Default:0.75V Reserved
VCCA_1V8_S0
AVDD1V8_DDR_PLL_S0
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3588S_Demo
File: 22.Power-PMIC_RK806-1
Date: Wednesday, February 23, 2022
Rev: V10
Designed by: Joseph
Reviewed by: <Checker>
Sheet: 20 of 32

VDD_CPU_BIG0

ARM CPU BESLEME CPU-BIG

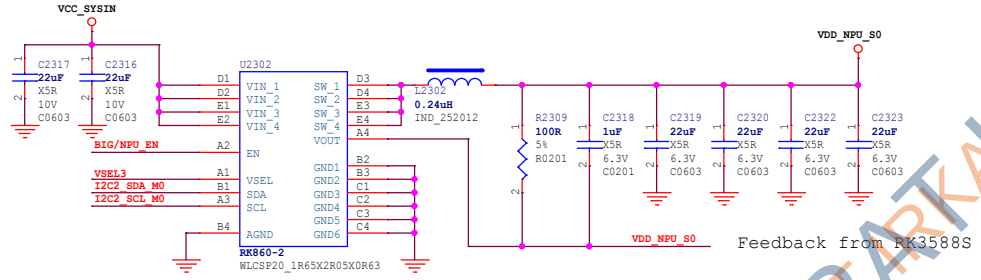


VDD_CPU_BIG1

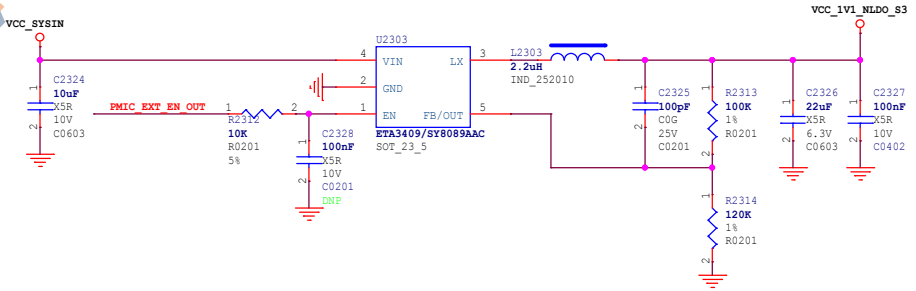


VDD_NPU

YAPAY ZEKA ÇEKİRDEK BESLEME

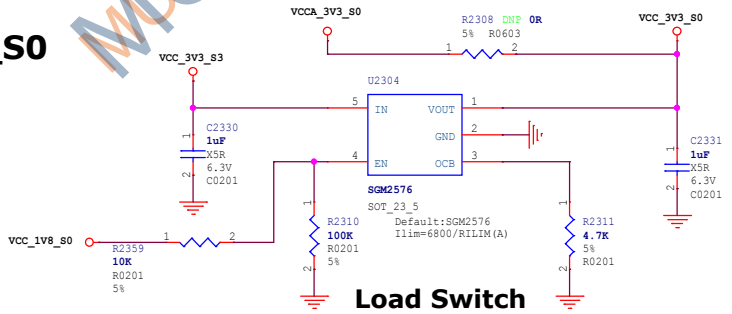


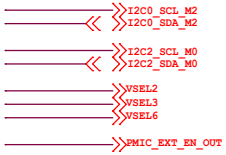
VCC_1V1_NLDO



3.3V REGÜLATOR

VCC_3V3_S0

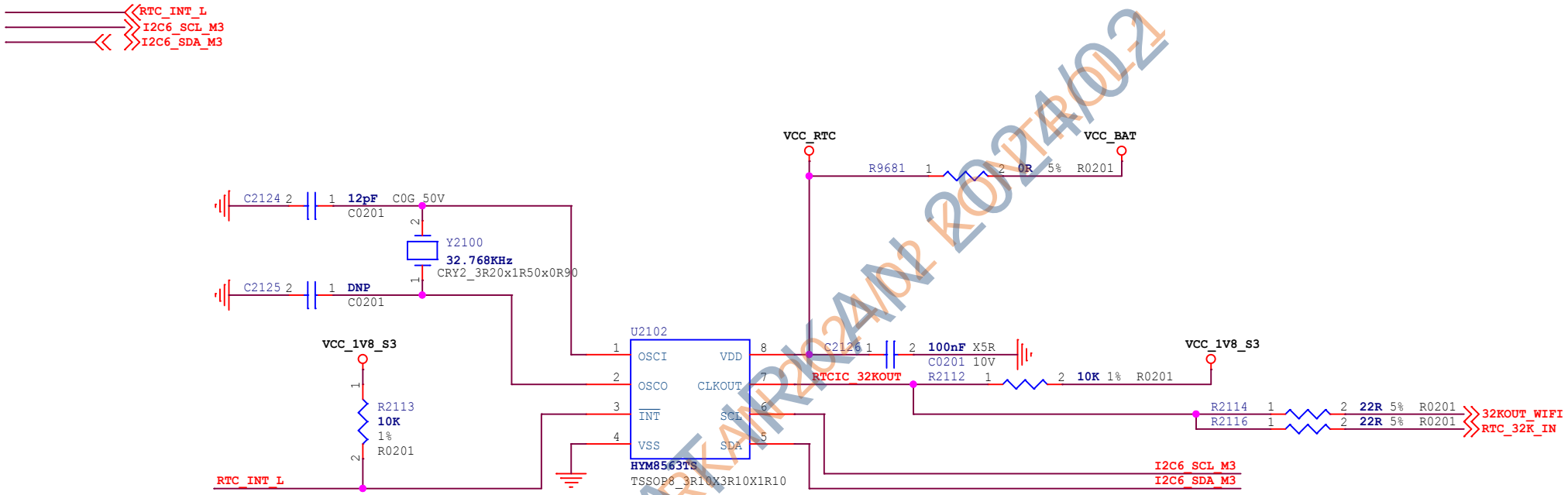




Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	23.Power_Ext Discrete				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	21 of 32

ZAMANLAMA ÜNİTESİ

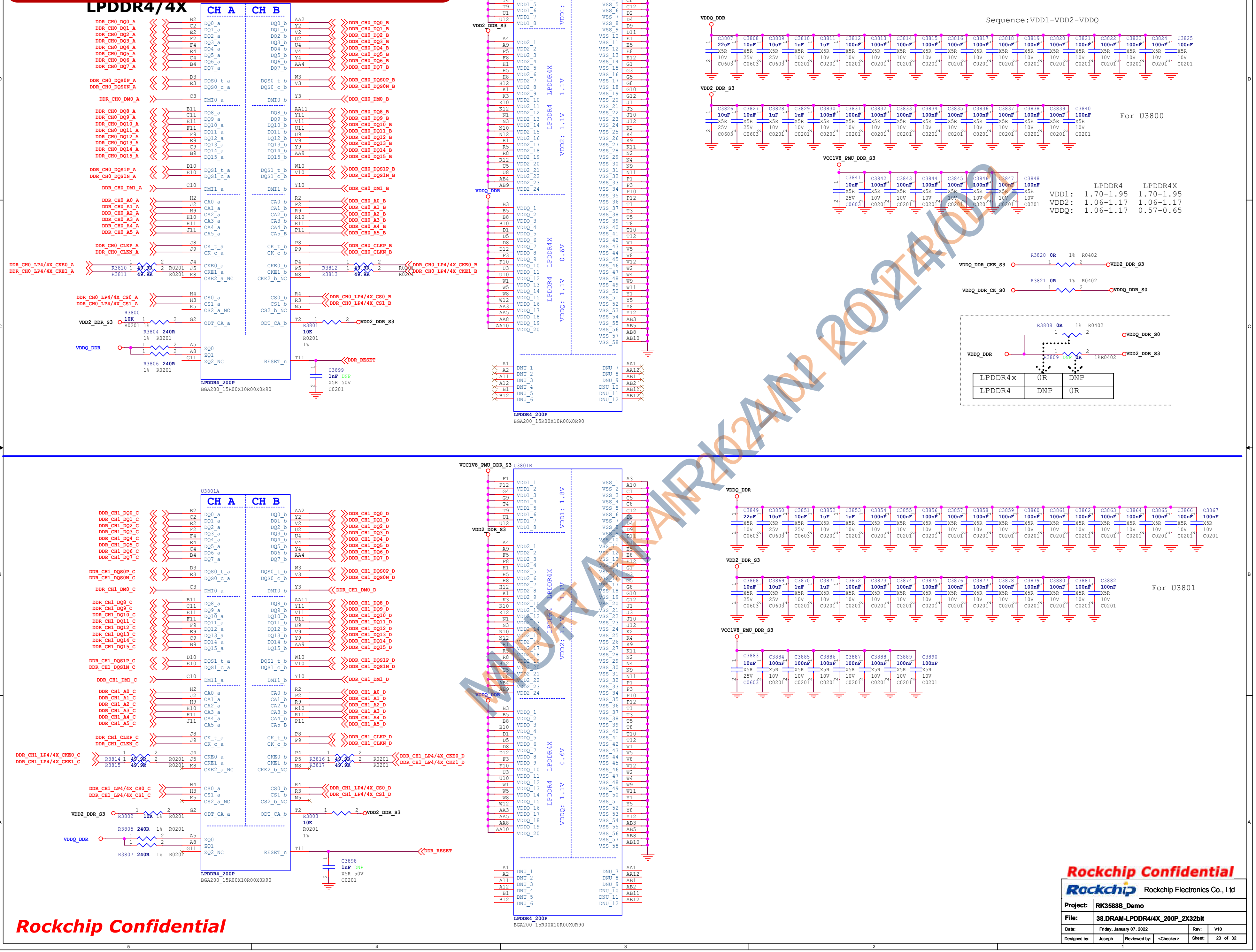
RTC IC



Address:Read A3H,Write A2H

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	24.RTC				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	22 of 32

LPDDR4 HAFIZA MODÜLLERİ A / B KANAL



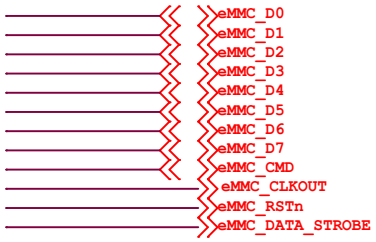
Rockchip Confidential

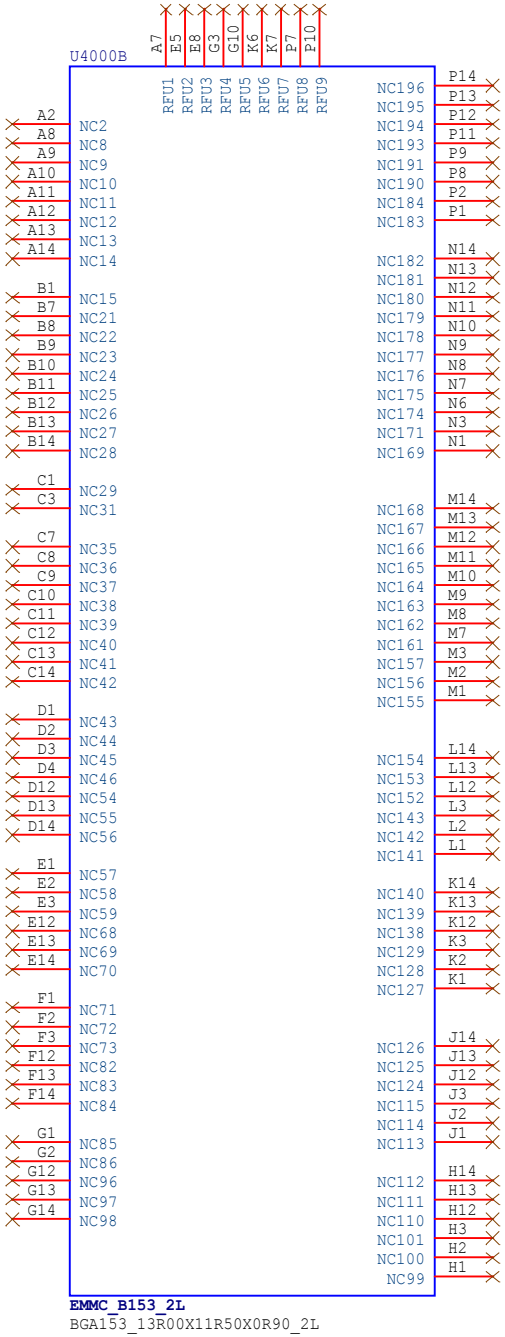
Rockchip Electronics Co., Ltd

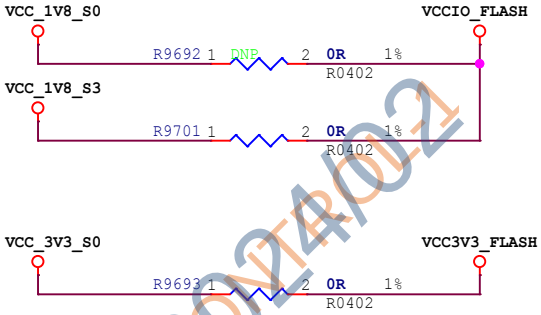
Project:	RK3588S_Demo
File:	38.DRAM-LPDDR4/4X_200P_2X32bit
Date:	Friday, January 07, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	23 of 32

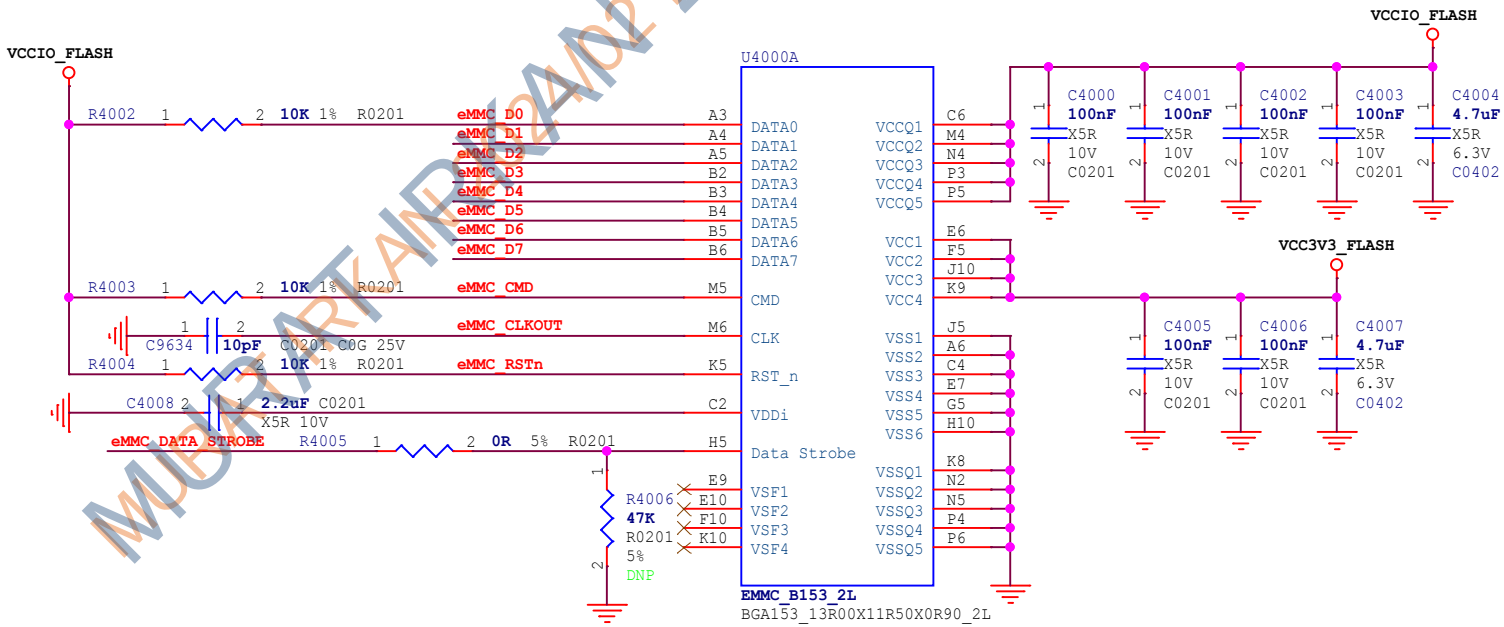
eMMC Flash

MULTI MEDYA KART GİRİŞLER









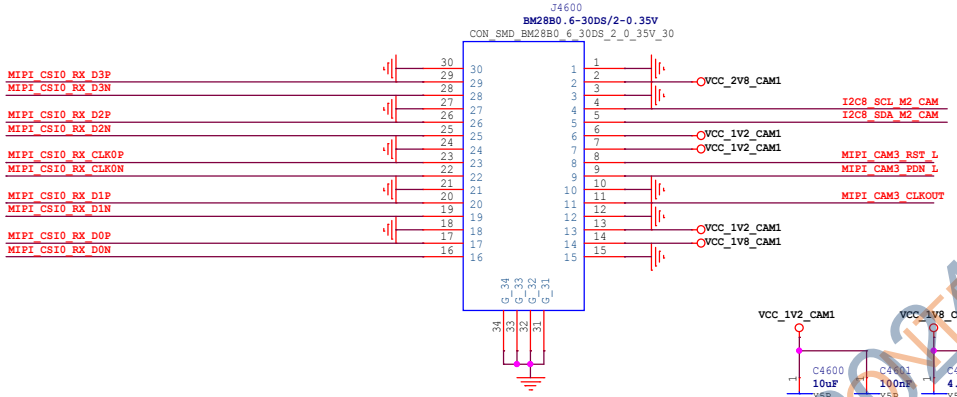
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	40.eMMC Flash				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	24 of 32

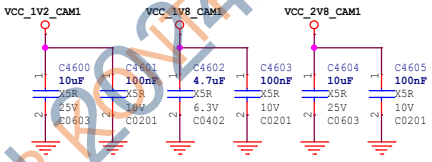
MIPI-CSI0_RX

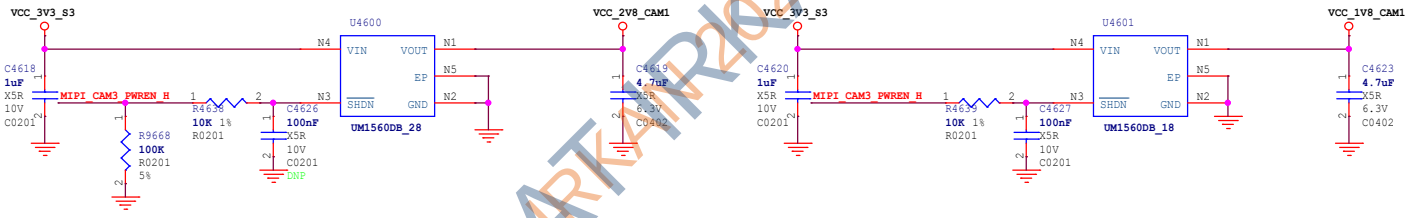
KAMERA

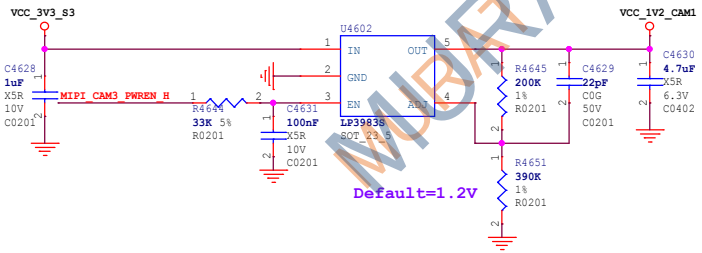
前摄：OV16A10-GA5A-Z

MIPI_CSI0_RX_D0P
MIPI_CSI0_RX_D0N
MIPI_CSI0_RX_D1P
MIPI_CSI0_RX_D1N
MIPI_CSI0_RX_D2P
MIPI_CSI0_RX_D2N
MIPI_CSI0_RX_D3P
MIPI_CSI0_RX_D3N
MIPI_CSI0_RX_CLK0P
MIPI_CSI0_RX_CLK0N
MIPI_CAM3_CLKOUT
MIPI_CAM3_RST_L
MIPI_CAM3_PWREN_H
MIPI_CAM3_PDN_L
I2C8_SCL_M2_CAM
I2C8_SDA_M2_CAM





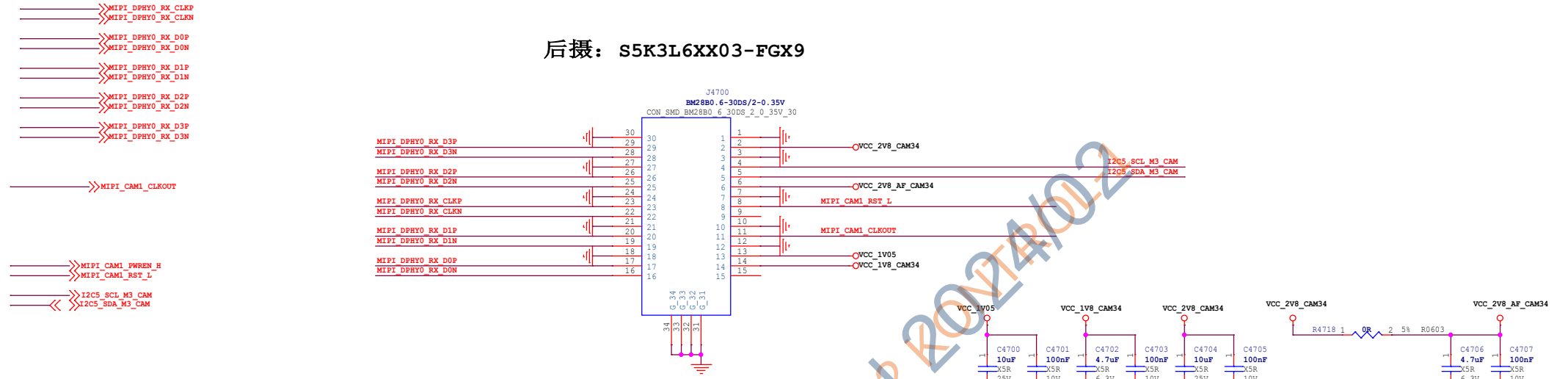


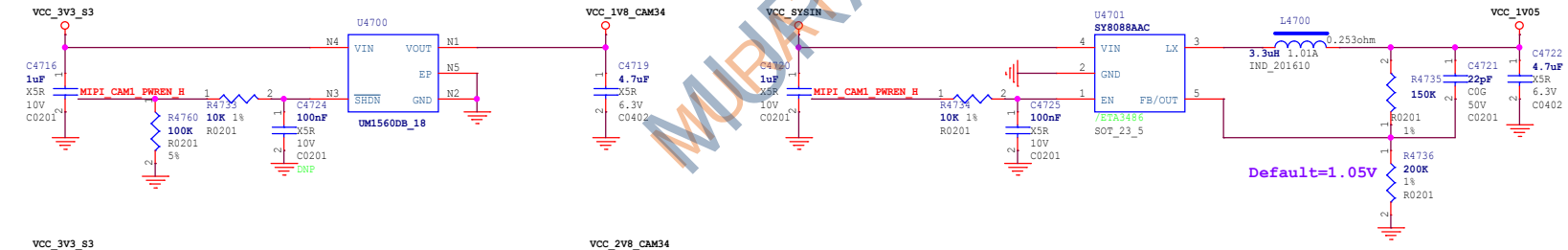


Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	46.VI-Camera MIPI CSI0-RX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	25 of 32

VI-Camera DPHY_RX

后摄： S5K3L6XX03-FGX9

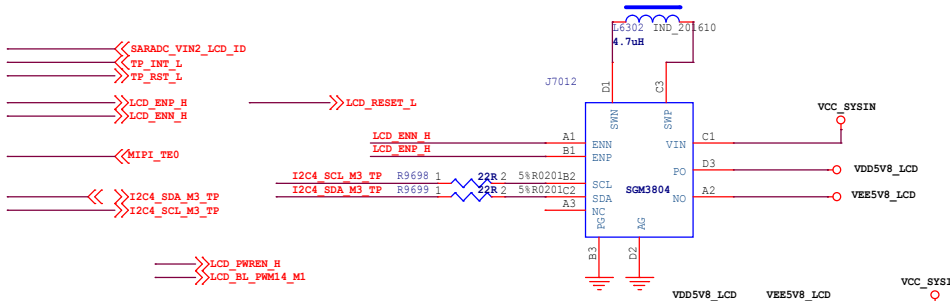


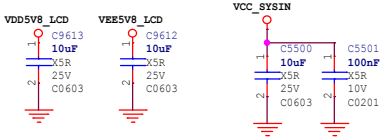


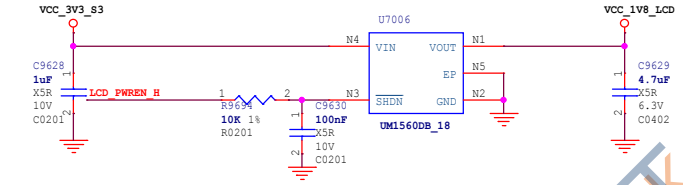
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	47.VI-Camera_MIPI-DPHY-RX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	26 of 32

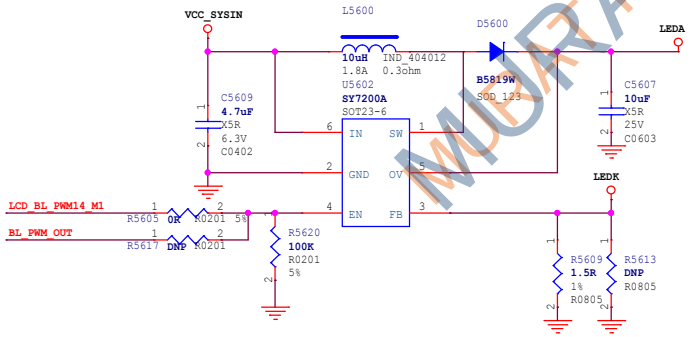
MIPI DPHY TX

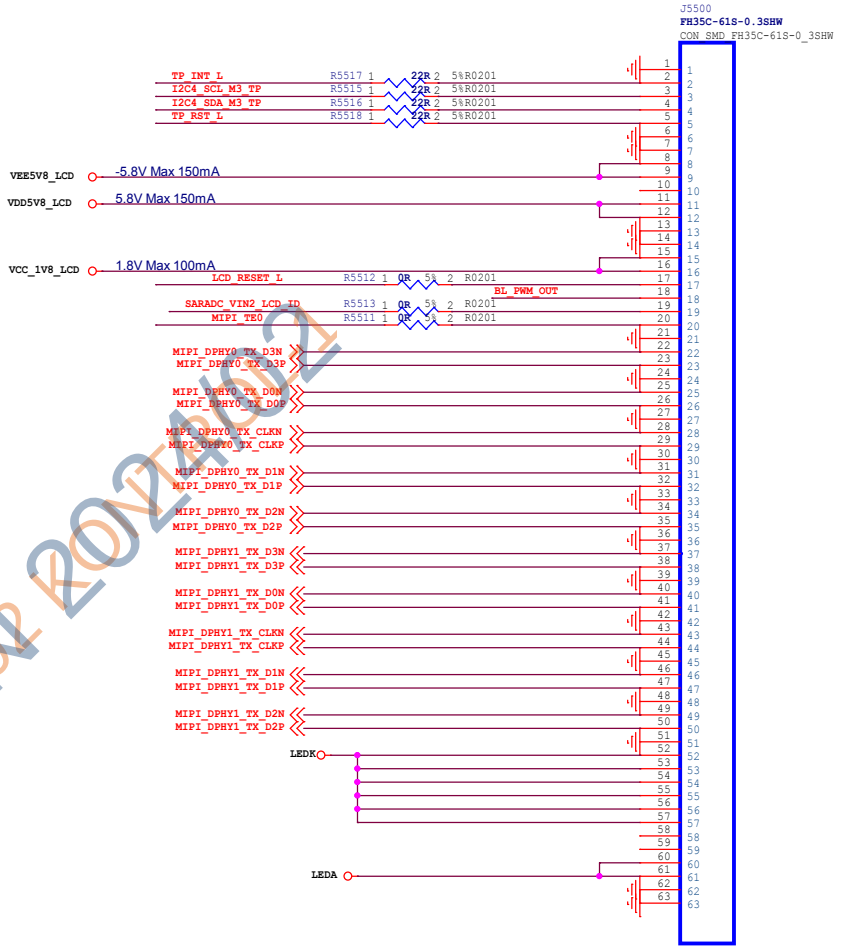
Power
REGÜLATÖR







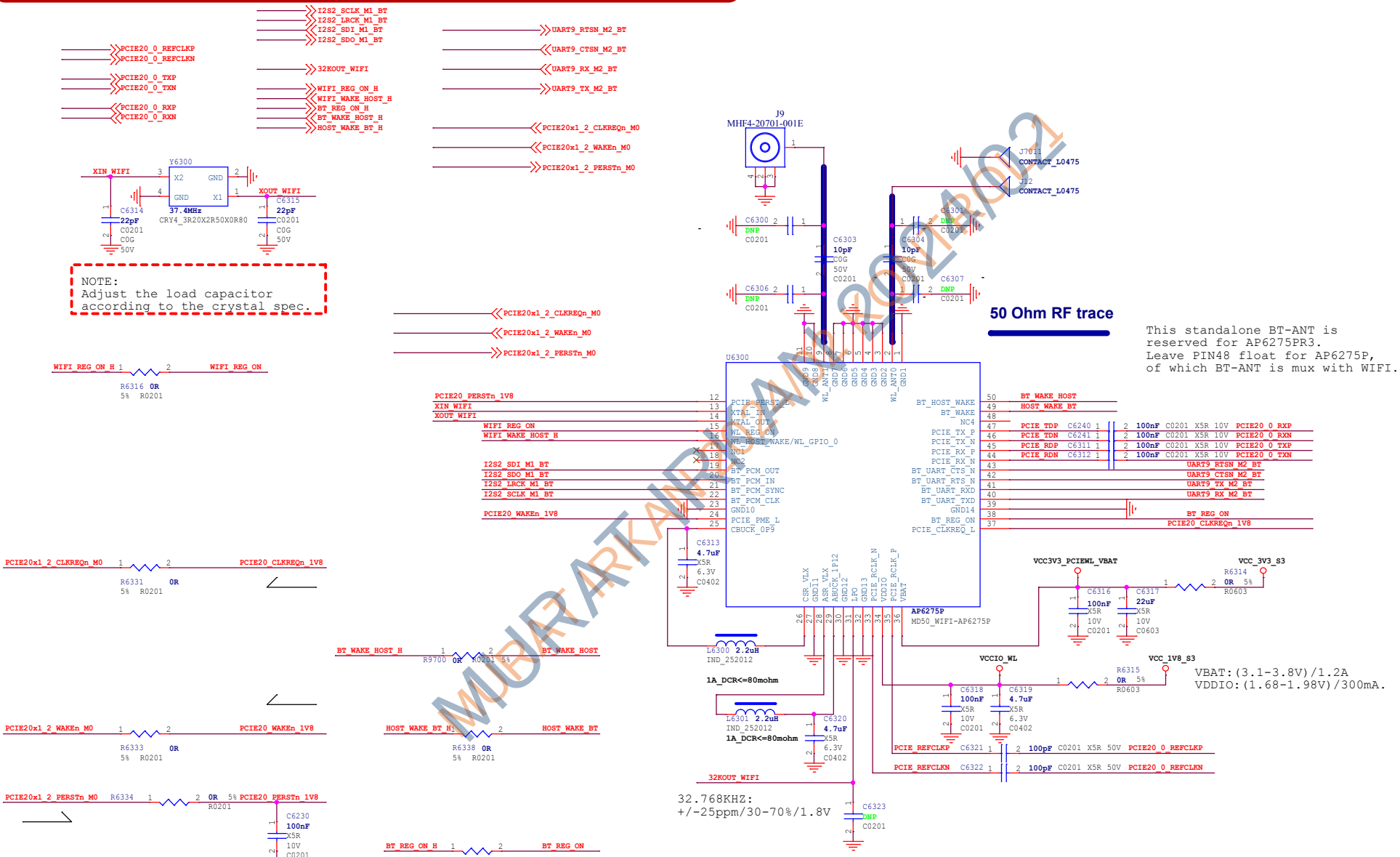




Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	55.VO-MIPI DPHY-TX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	27 of 32

PCIe WIFI6/BT Module-2T2R

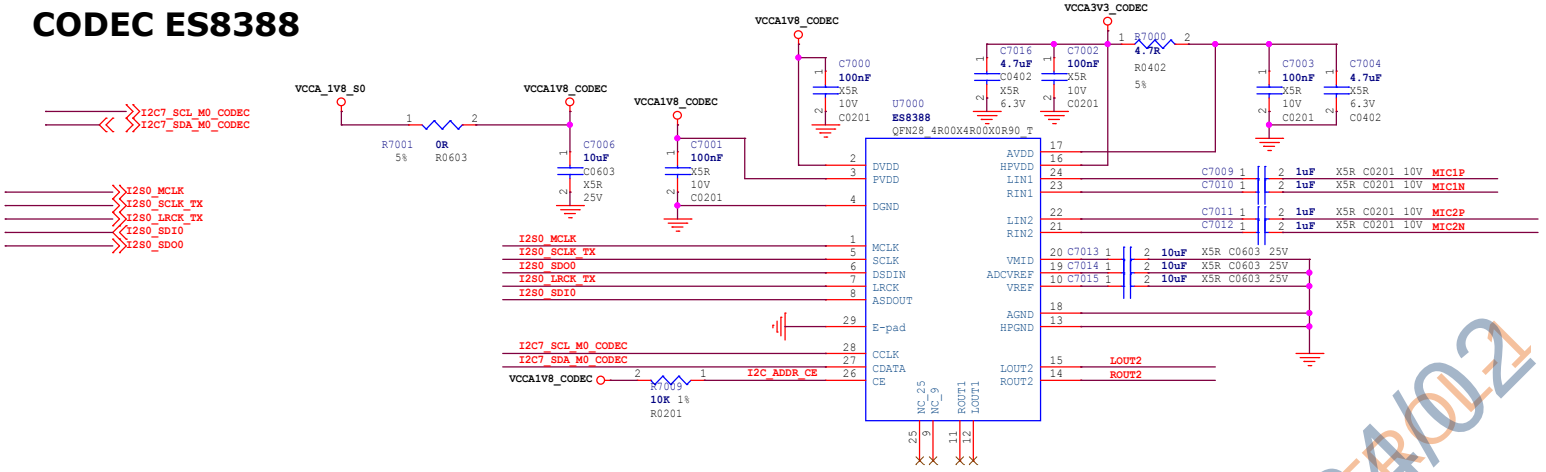
WIFI-6 VE BLUETOOTH MODÜLLERİ VE BAGLANTILAR



Rockchip Confidential

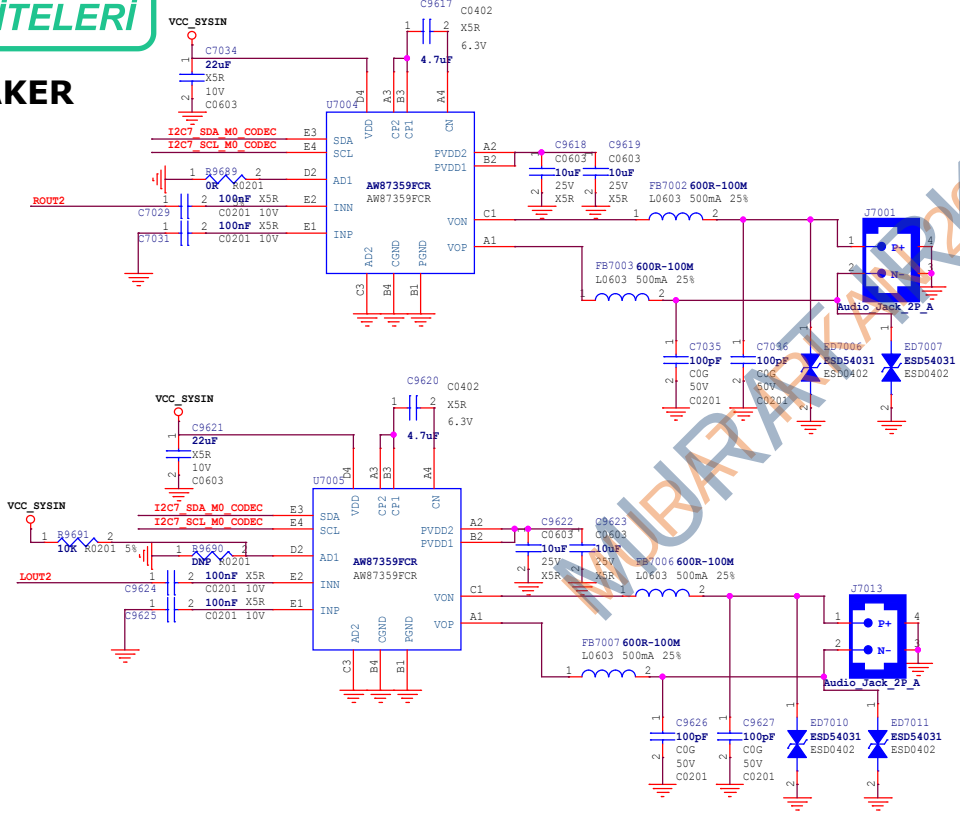
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	63.WIFI/BT-PCIe_2T2R(AP6275PR3)				
Date:	Monday, January 24, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	28 of 32

CODEC ES8388

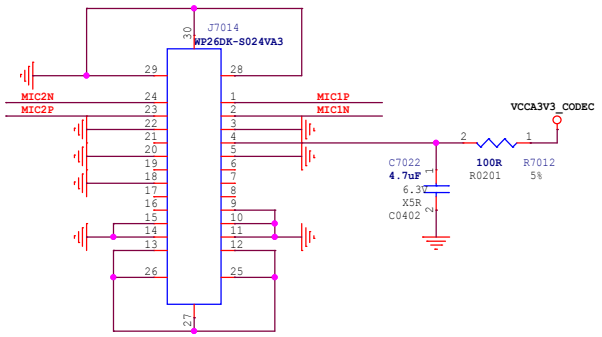


SES ÜNİTELERİ

SPEAKER



Analog MIC



Rockchip Confidential

Rockchip Electronics Co., Ltd

Project:	RK3588S_Demo				
File:	70.Audio Codec-ES8388				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	29 of 32

Sensor

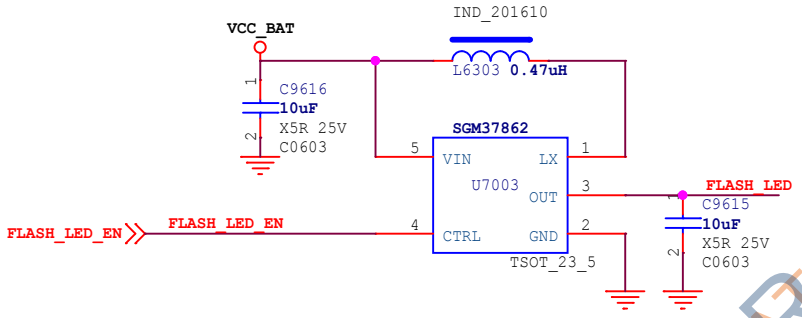
I2C3_SCL_M1_Sensor
I2C3_SDA_M1_Sensor
RGB_INT_L
ALPS_INT_L

I2C3_SCL_M1_Sensor — I2C_SCL_SENSOR

I2C3_SDA_M1_Sensor — I2C_SDA_SENSOR

VCC_1V8_S0
I2C_SCL_SENSOR
I2C_SDA_SENSOR
RGB_INT_L

J7006 CONTACT_L0475
J7007 CONTACT_L0475
J7008 CONTACT_L0475
J7009 CONTACT_L0475
J7010 CONTACT_L0475



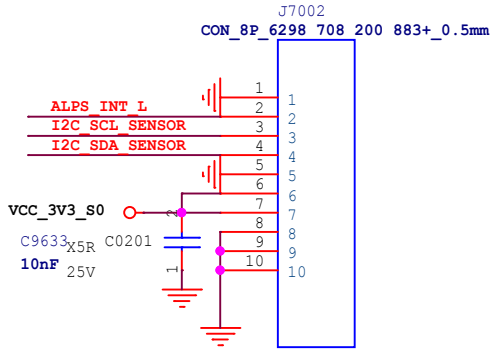
MAX:1.5A

FLASH_LED — J1 CONTACT_L0475

J3 CONTACT_L0475

Flashlight

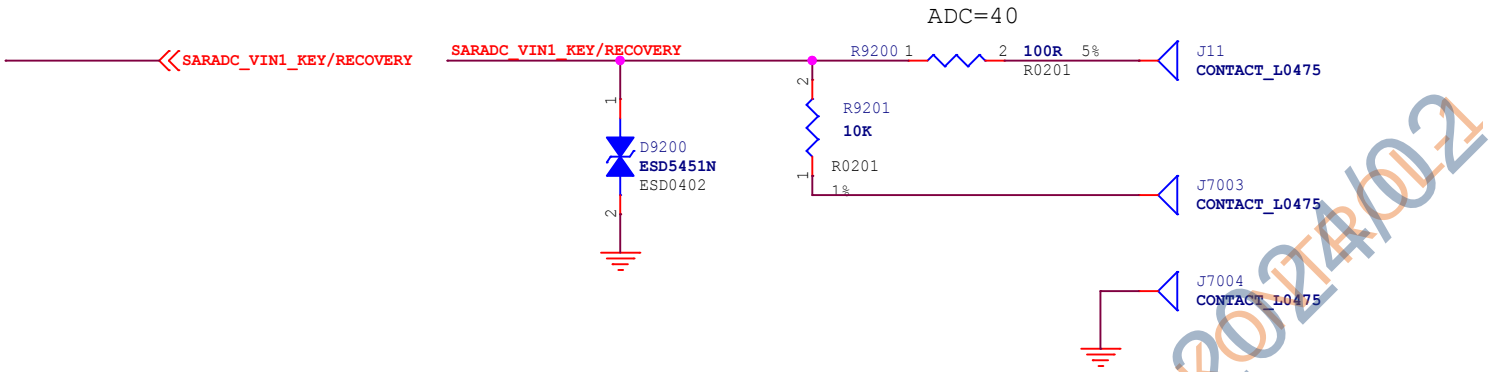
PLS+ALS



Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	90.Sensor				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	30 of 32

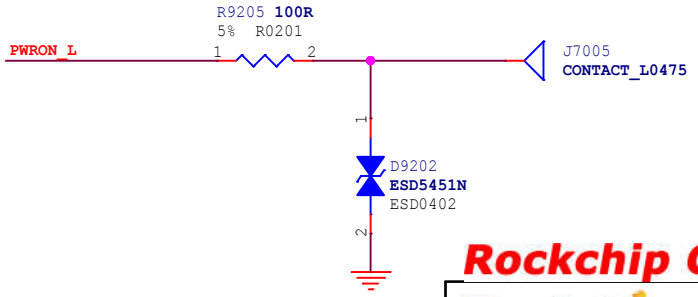
KLAVYE ADC GİRİŞLER

KEY Array



Reset_Key

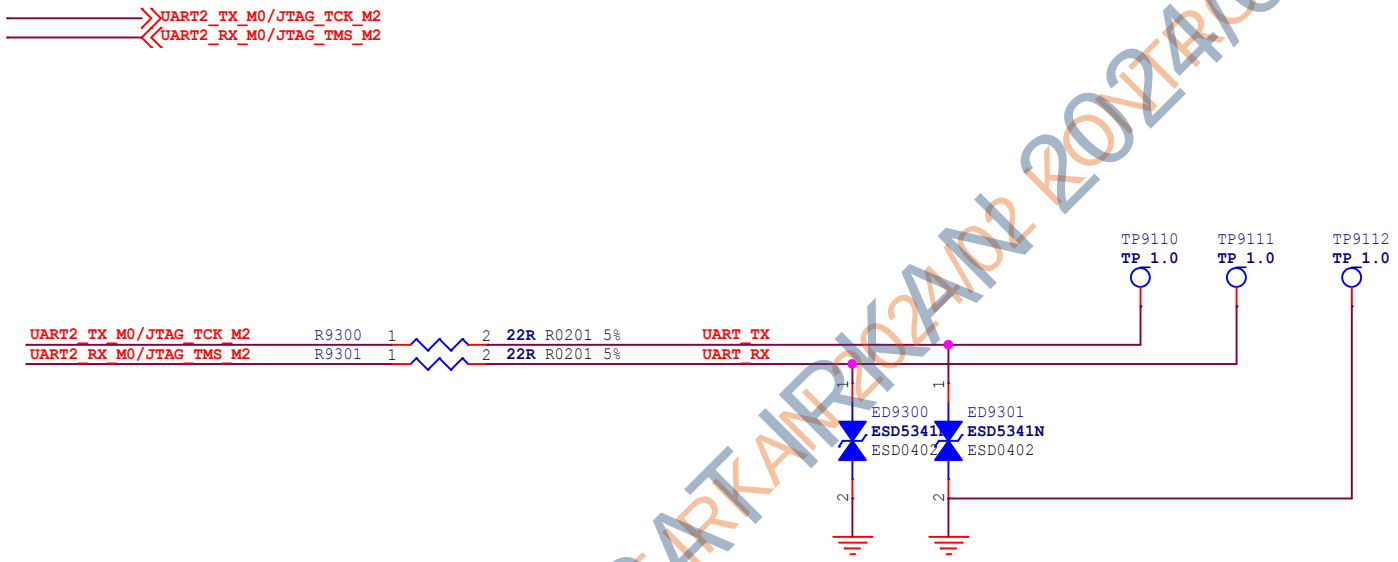
PWR_Key



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	92.KEY Array				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	31 of 32

UART Debug

JTAG Debug



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	93.Debug UART/JTAG Port				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	32 of 32