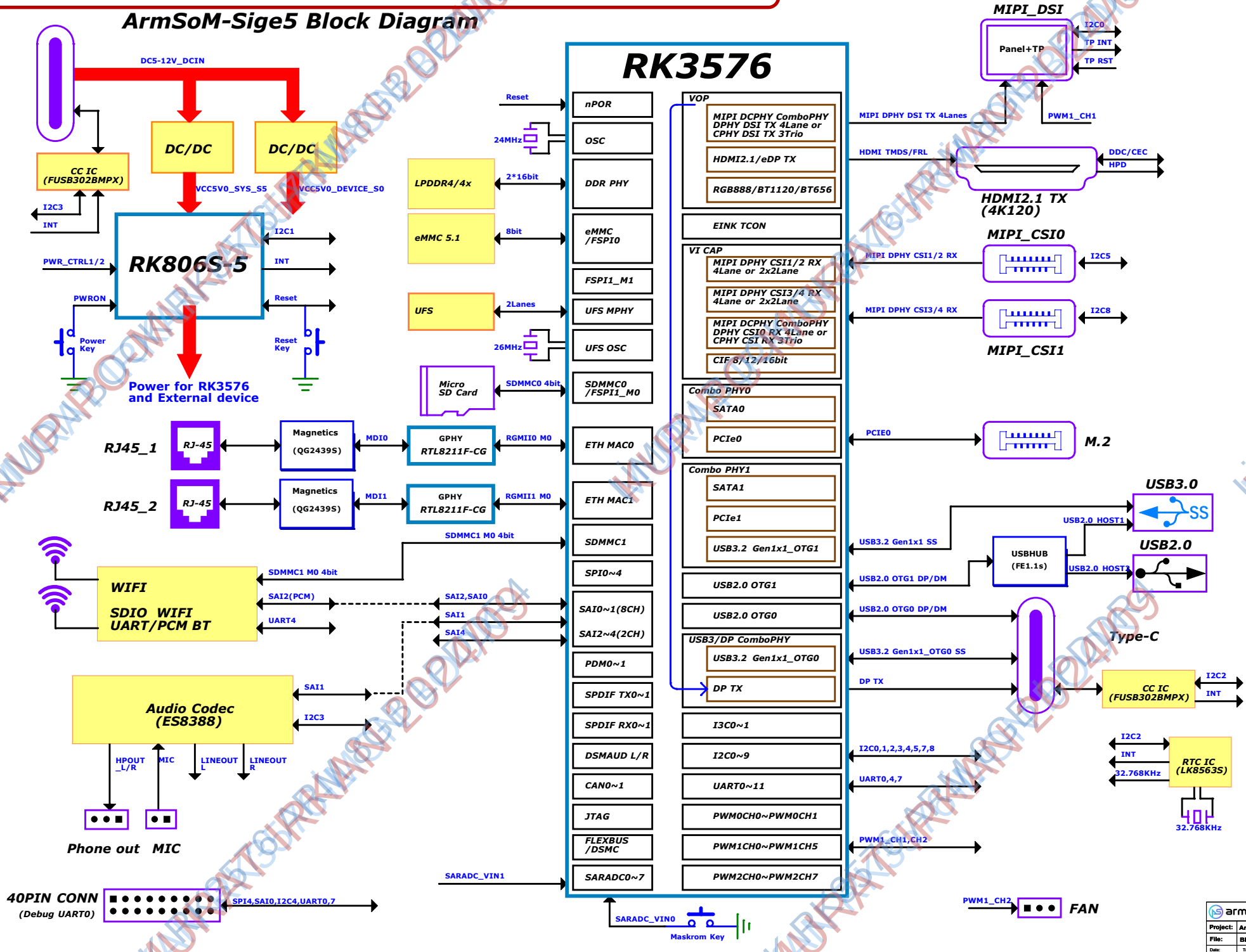
KUP BİLGİSAYAR RK3576 8-16GB LPDDR4

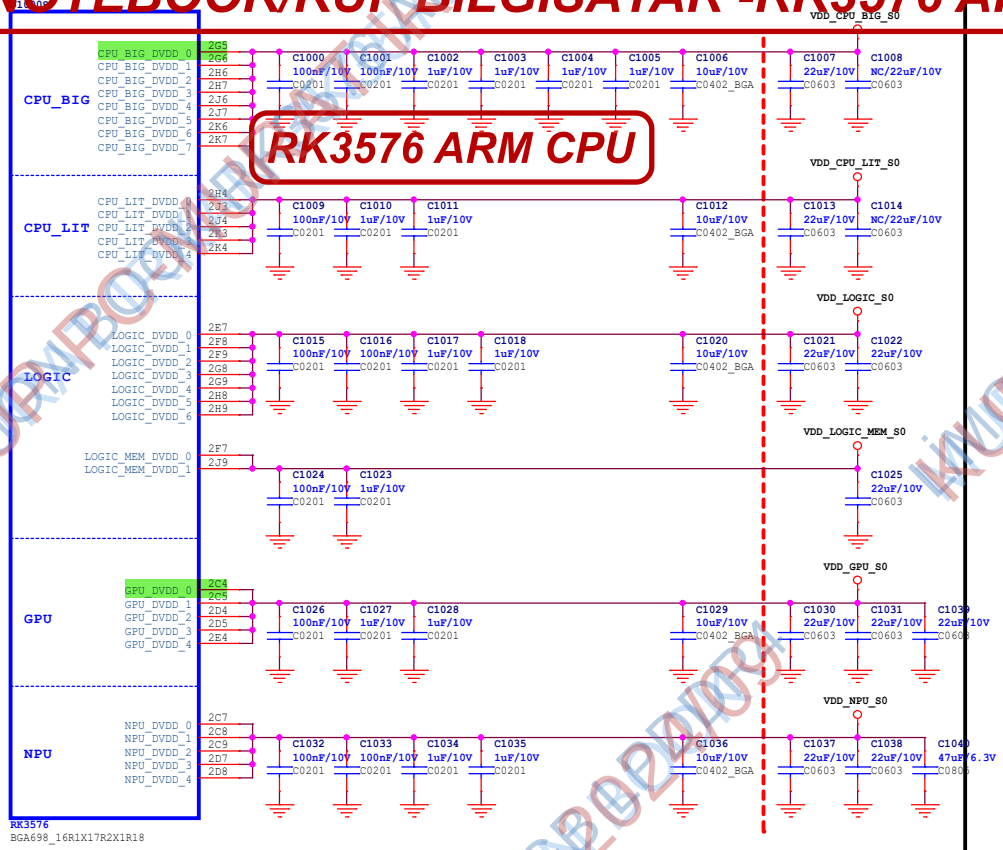
ArmSoM-Sige5 Block Diagram

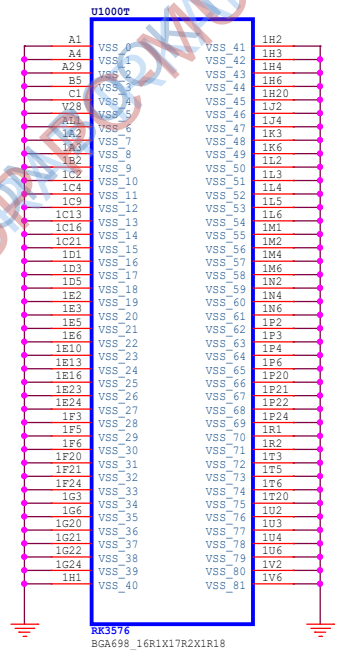


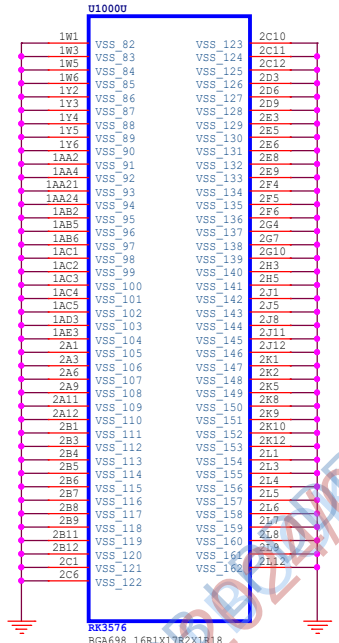
RK3576_S (Power)

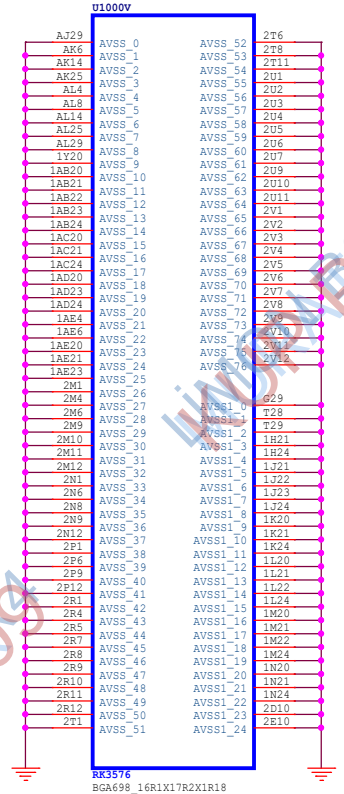
RK3576_T/U/V (GND)

NOTEBOOK/KÜP BİLGİSAYAR -RK3576 ARM LINUX





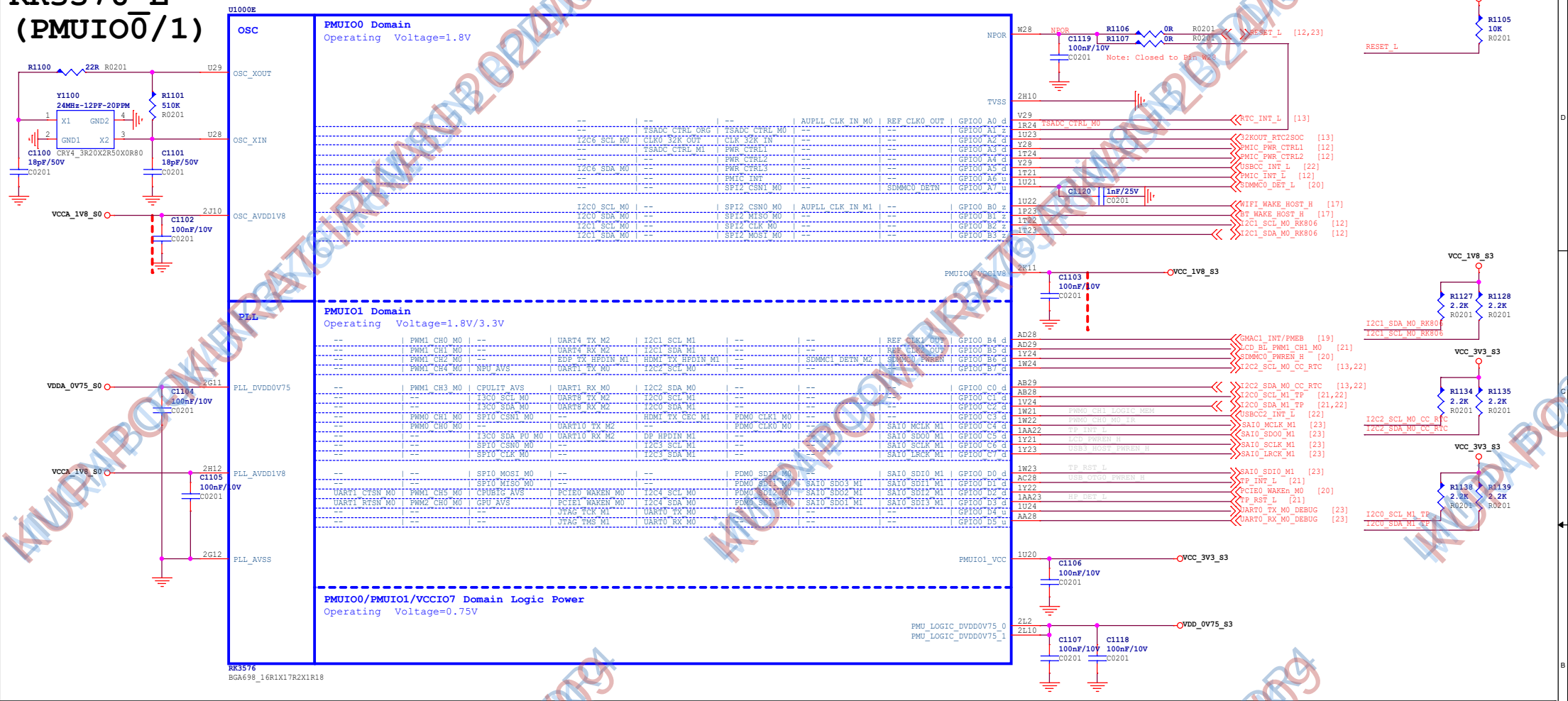




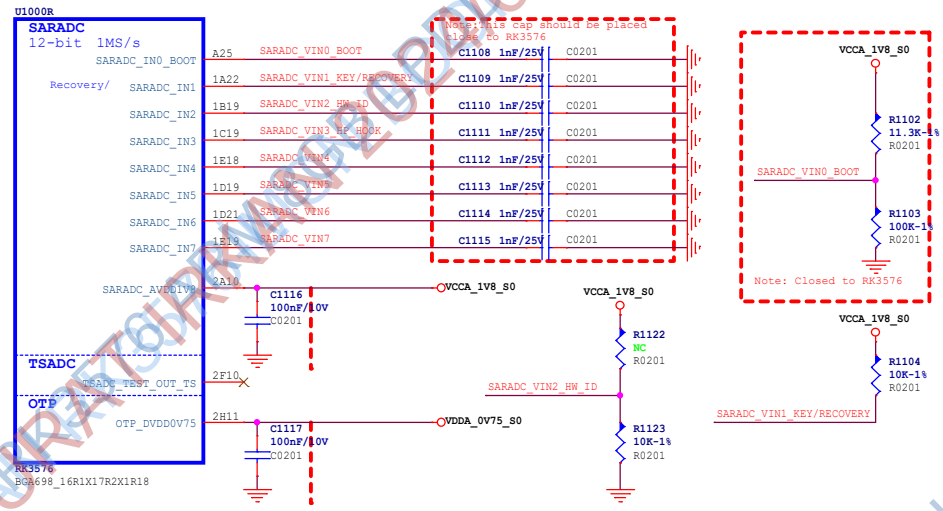
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	RK3576-Power/GND				
Date:	Tuesday, May 21, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 25

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package.

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

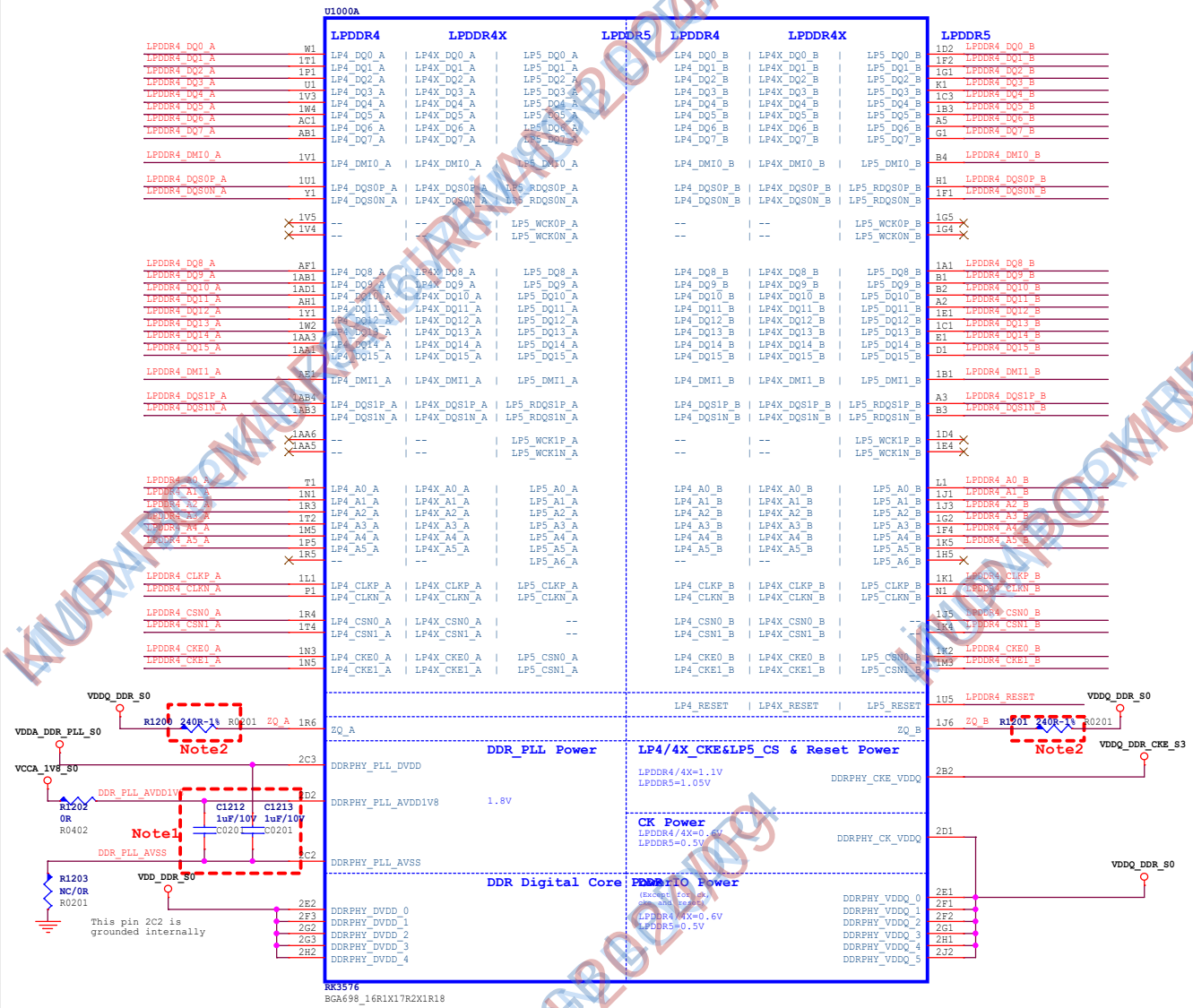
Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

SARADC_VIN0_BOOT [23]
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_HW_ID
SARADC_VIN3_HP_HOOK
SARADC_VIN4 [23]
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7 [22]

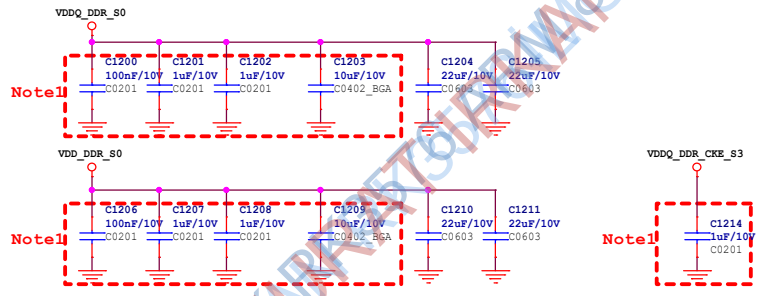
armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	RK3576-OSC/PLL/PMUIO/SARADC				
Date:	Tuesday, May 21, 2024			Rev.	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	3 of 25

RK3576_A(DDRPHY)



DDR FILTER

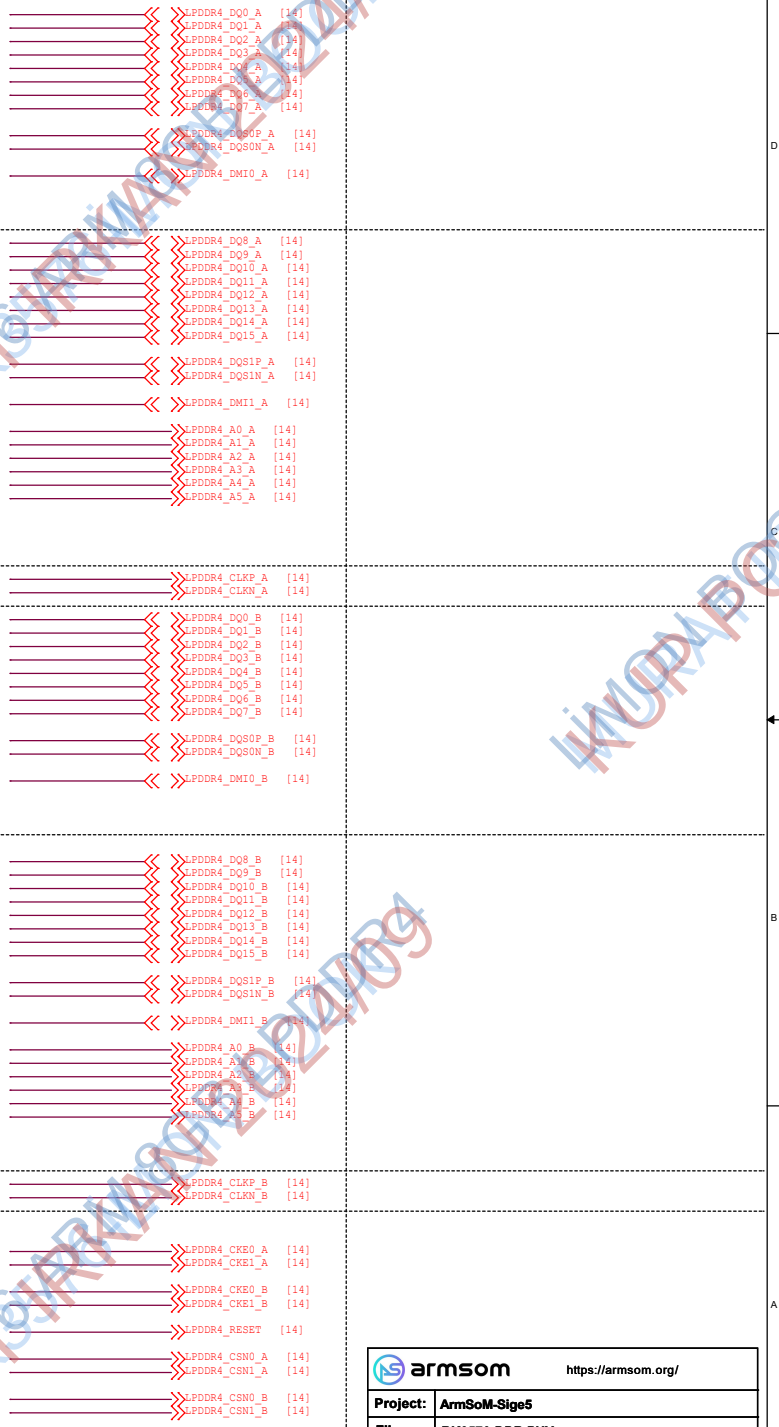


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

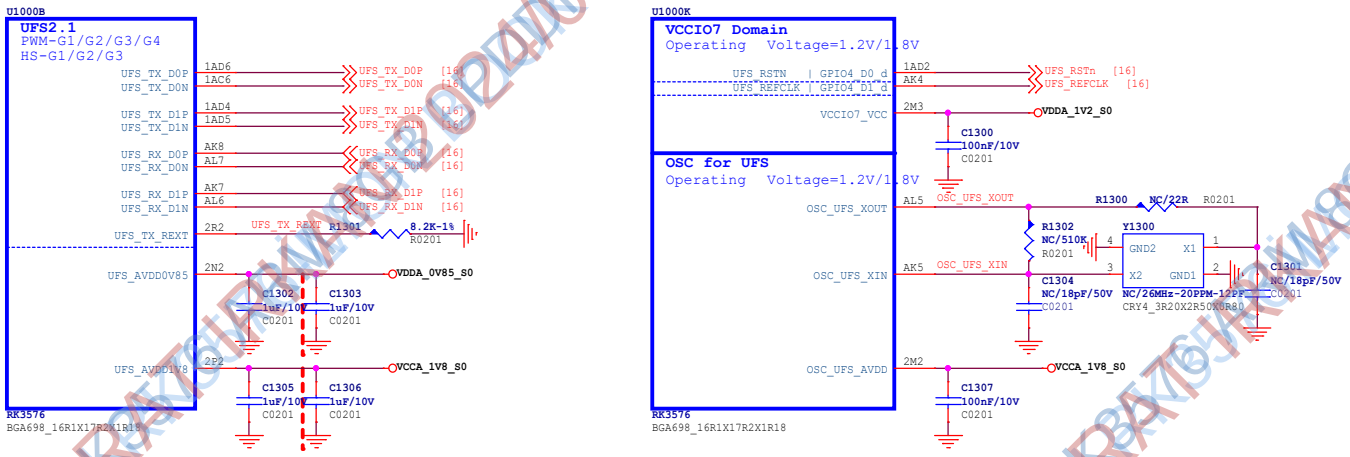
Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR4 Signal



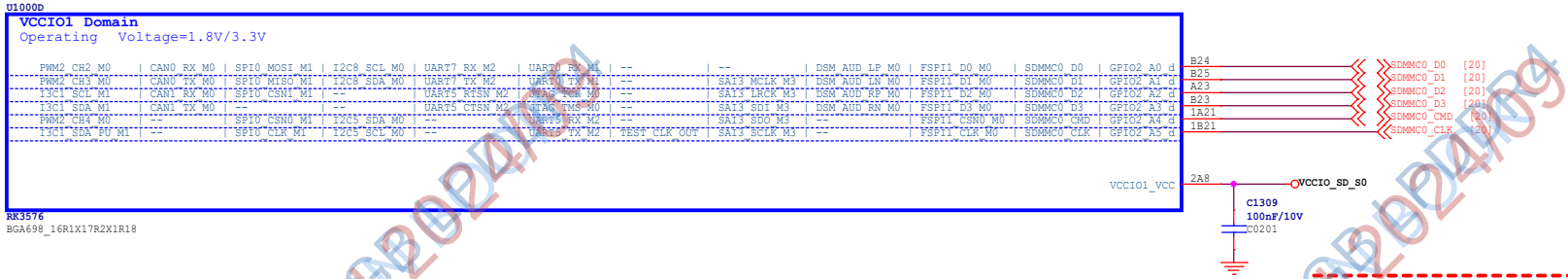
armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	RK3576-DDR PHY		
Date:	Tuesday, May 21, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 4 of 25

RK3576_B (UFS2.1)



RK3576_C (VCCIO0)

RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	RK3576-eMMC/UFS/SD				
Date:	Wednesday, May 22, 2024			Rev.	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	5 of 25

RK3576_L (USB3/DP)

USB-3 PORTU

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R18

Support:
Type-C With Displayport Alternate Mode

2T2 DP_TX_AUXP [22]
2T3 DP_TX_AUXN [22]
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P [22]
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N [22]
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P [22]
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N [22]
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P [22]
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N [22]
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P [22]
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N [22]
2T7 USB3_OTG0_DP_TX_REXT R1400 8.2K-1% R0201
2M5, 2N5 VDDA_0V85_S0
C1400 1uF/10V C0201
C1401 NC/1uF/10V C0201
2N4 VCCA_1V8_S0
C1402 1uF/10V C0201
C1403 NC/1uF/10V C0201

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

USB 2.0

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

RK3576
BGA698_16R1X17R2X1R18

AK9 USB2_OTG0_DP [22]
AL9 USB2_OTG0_DM [22]
2R6 USB2_OTG0_ID Note: There is an internal pull-up resistor connected to 1.8V TP18 TP_0R7
2P3 USB2_OTG0_VBUSDET [22]
2R3 USB2_OTG0_REXT R1401 200R-1% R0201
C1404 100nF/10V C0201
2T4 USB2_HOST1_DP [22]
2T5 USB2_HOST1_DM [22]
2T9 USB2_OTG1_ID TP19 TP_0R7
2T10 USB2_OTG1_VBUSDET
2U8 USB2_OTG1_REXT R1402 200R-1% R0201
VCC_3V3_S0
C1409 NC/100nF/10V C0201
R1406 NC/20K R0201
R1405 NC/4.7K R0201

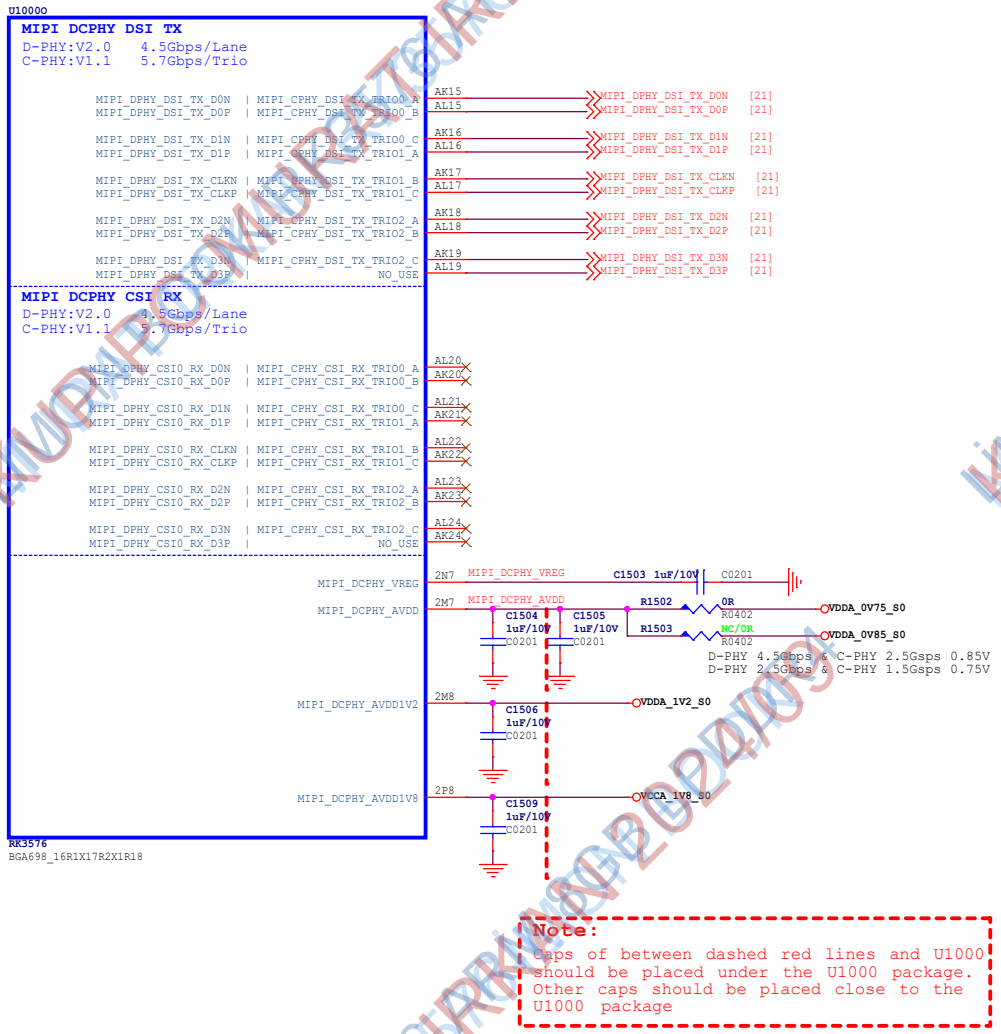
The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

2P5 VDDA_0V75_S0
C1405 100nF/10V C0201
2P4 VCCA_1V8_S0
C1406 100nF/10V C0201
C1407 NC/1uF/10V C0201
2P7 VCC_3V3_S0
C1408 100nF/10V C0201

armsom https://armsom.org/

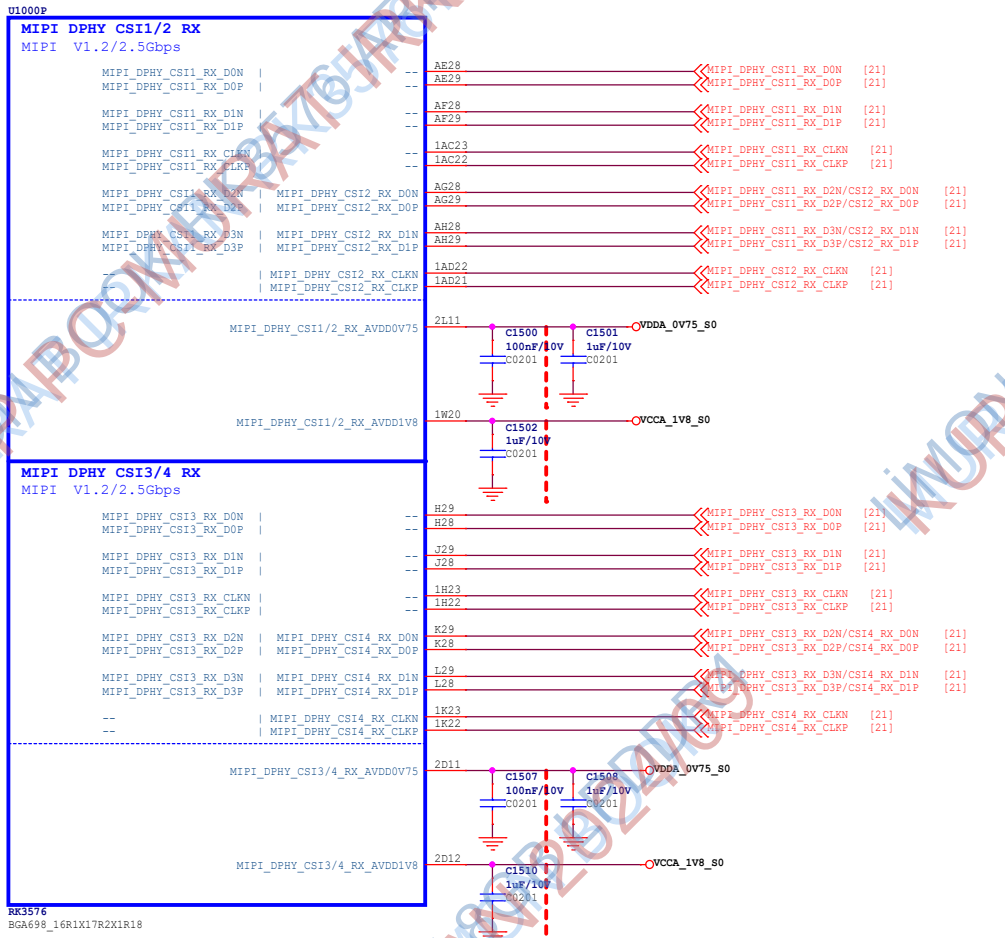
Project:	ArmSoM-Sige5				
File:	RK3576-TypeC/USB				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 25

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

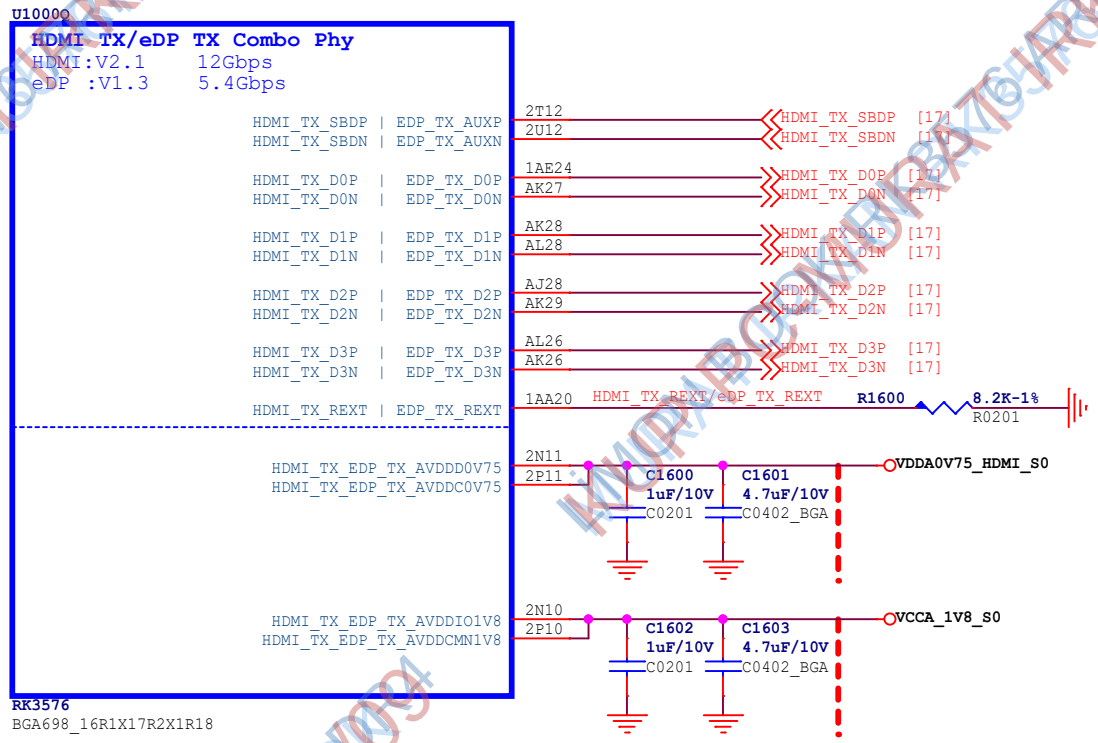


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	RK3576-MIPI DSI/CSI				
Date:	Tuesday, May 21, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 25

RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz

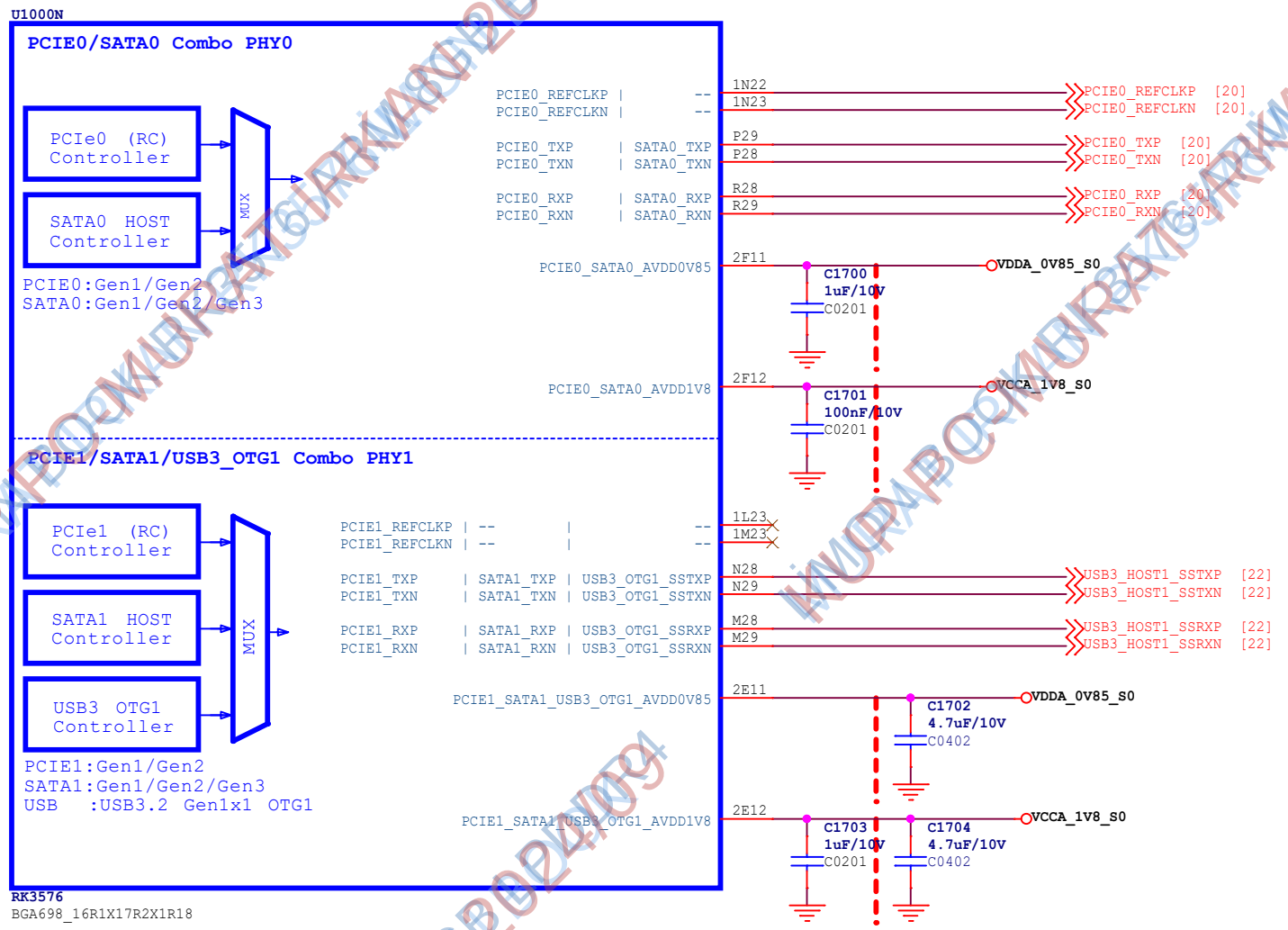


HDMI_TX_SBDP [17]
HDMI_TX_SBDN [17]
HDMI_TX_D0P [17]
HDMI_TX_D0N [17]
HDMI_TX_D1P [17]
HDMI_TX_D1N [17]
HDMI_TX_D2P [17]
HDMI_TX_D2N [17]
HDMI_TX_D3P [17]
HDMI_TX_D3N [17]

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ArmSoM-Sige5				
File:	RK3576-MIPI DSI/CSI				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 25

RK3576_N(PCIe/SATA/USB3)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ArmSoM-Sige5				
File:	RK3576-PCIe/SATA/USB3				
Date:	Tuesday, May 21, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 25

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain
Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	PCIE1_WAKEN_M2	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS1_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI3_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	PCIE0_WAKEN_M2	I2C3_SDA_M0	UART2_RX_M1	SPI4_CSN1_M2	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

RK3576
BGA698_16R1X17R2X1R18

1D6 SAI1_MCLK_M0 [23]
1C6 SAI1_SCLK_M0 [23]
1C5 USB3_HOST_PWREN_H [22]
1B6 SAI1_LRCK_M0 [23]
1B5 USB_OTG0_PWREN_H [22]
A7 SAI1_SDO0_M0 [23]

1A5 HP_DET_L [23]
B7 LED_RED_EN [23]
B6 LED_GREEN_EN [23]
1A6 SAI1_SDI0_M0 [23]
B8 I2C3_SDA_M0_Audio [23]
1A4 I2C3_SCL_M0_Audio [23]

VCCIO2_VCC 2A2 C1800 100nF/10V C0201 VCCIO_AUDIO

VCCIO_AUDIO
R1800 2.2K R0201
R1801 2.2K R0201
I2C3_SDA_M0_Audio
I2C3_SCL_M0_Audio

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	PCIE1_WAKEN_M1	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	PCIE0_WAKEN_M1	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
PWM0_CH1_M1	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d
PWM0_CH2_M1	--	SPI2_CSN1_M1	I2C8_SCL_M1	UART4_RTSN_M1	--	--	SPDIF_CSN1_M1	SPDIF_RSTN_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C8_SDA_M1	UART4_CTSN_M1	--	--	--	SPDIF_CSN0_M1	SDMMC1_PWRCTRL_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	SPDIF_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	SPDIF_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	SPDIF_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	SPDIF_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	FSPI1_D4_M1	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	FSPI1_D5_M1	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	FSPI1_D6_M1	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	FSPI1_D7_M1	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	FSPI1_DQS_M1	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWITCH	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

RK3576
BGA698_16R1X17R2X1R18

A28 SDMMC1_D0_M0 [17]
B27 SDMMC1_D1_M0 [17]
1A23 SDMMC1_D2_M0 [17]
A27 SDMMC1_D3_M0 [17]

B26 SDMMC1_CMD_M0 [17]
1B22 SDMMC1_CLK_M0 [17]
B29 UART4_RTSN_M1 [17]
1C23 UART4_CTSN_M1 [17]
1B23 UART4_TX_M1 [17]
B28 UART4_RX_M1 [17]
A26 WIFI_REG_ON_H [17]
1C22 BT_REG_ON_H [17]

For BT

C29 SAI2_SDO_M0 [17]
1D22 SAI2_SCLK_M0 [17]
1A24 SAI2_LRCK_M0 [17]
C28 SAI2_SDI_M0 [17]
1E21 HOST_WAKE_BT_H [17]
1E22 LCD_PWREN_H [21]

For BT

VCCIO3_VCC 2B10 C1801 100nF/10V C0201 VCCIO_WL

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	PCIE1_WAKEN_M3	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RP_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACT_LED_M1	PCIE0_WAKEN_M3	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACT_LED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

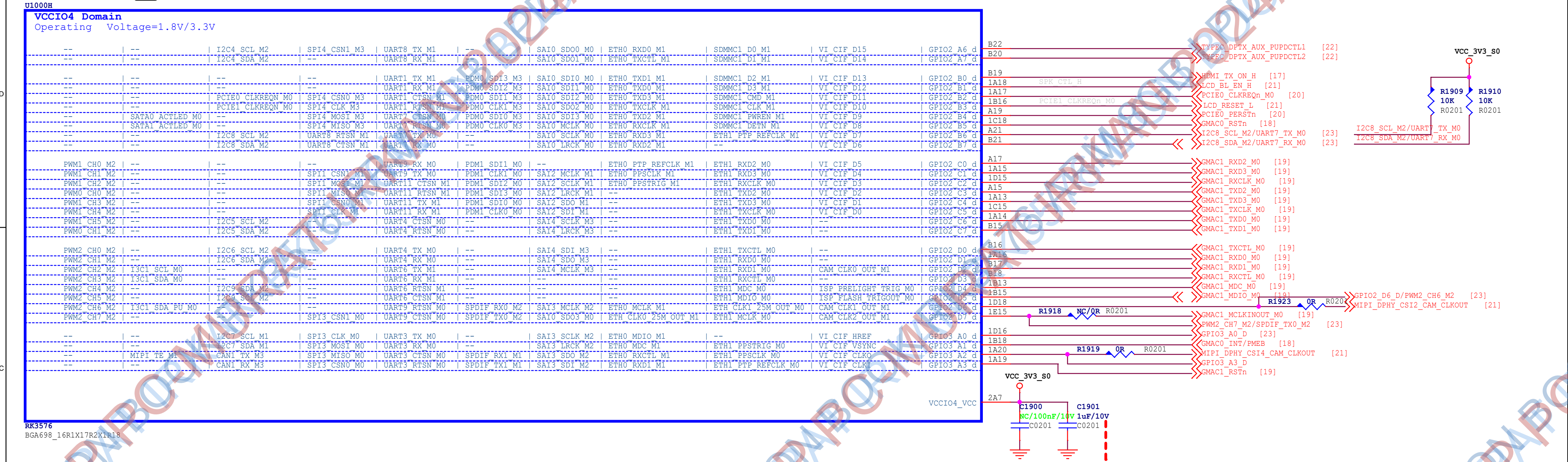
RK3576
BGA698_16R1X17R2X1R18

AK3 HDMI_TX_CEC_M0 [17]
AK2 HDMI_TX_HPDIN_M0 [17]
AL2 HDMI_TX_SCL [17]
1AE2 HDMI_TX_SDA [17]
AL3 SPI4_CSN0_M0 [23]
AK1 SPI4_MOSI_M0 [23]
1AE1 SPI4_MISO_M0 [23]
AJ1 SPI4_CLK_M0 [23]

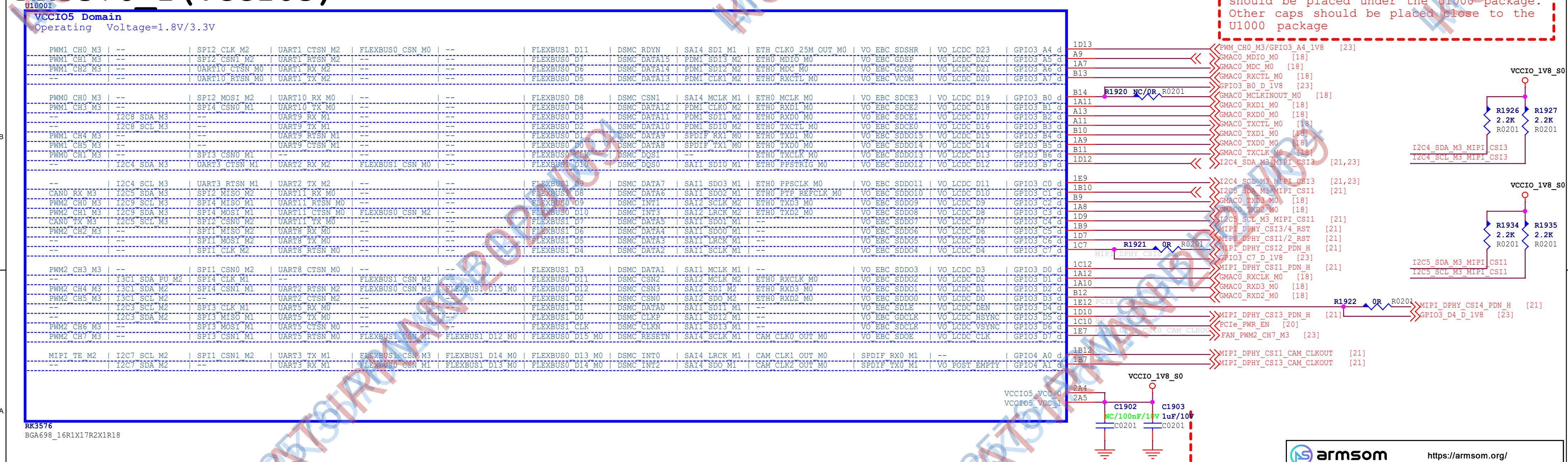
VCCIO6_VCC 2N3 C1802 100nF/10V C0201 VCC_3V3_S0

armsom	https://armsom.org/			
Project:	ArmSoM-Sige5			
File:	RK3576-GPIO VCCIO2/3/6			
Date:	Tuesday, May 21, 2024		Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	10 of 25

RK3576_H(VCCIO4)



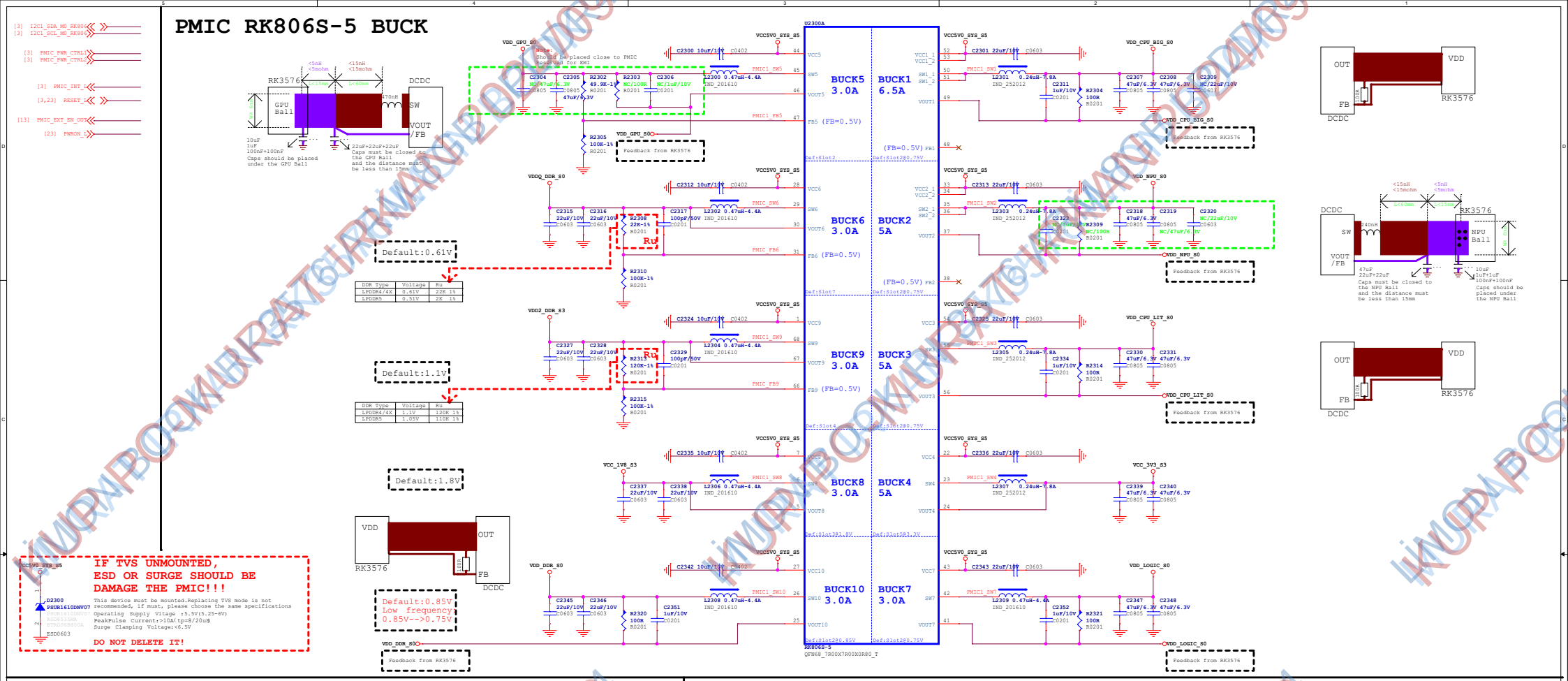
RK3576_I(VCCIO5)



armsom https://armsom.org/

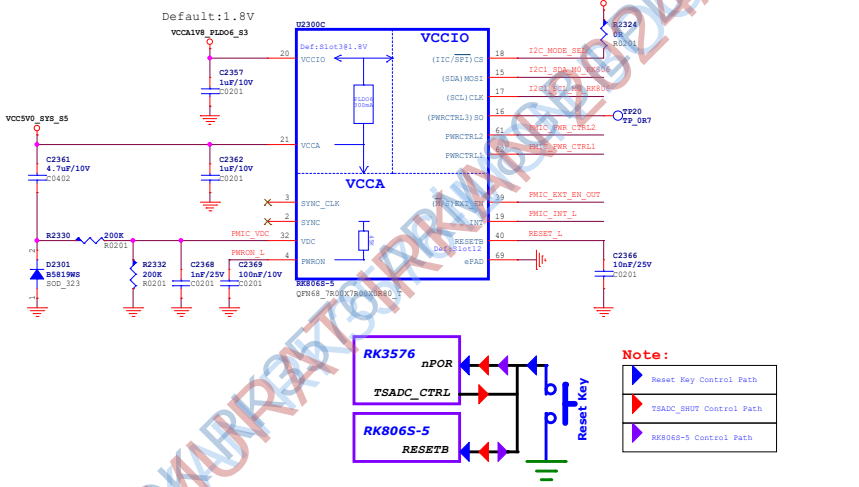
Project:	ArmSoM-Sige5
File:	RK3576-GPIO VCCIO4/5
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	11 of 25

PMIC RK806S-5 BUCK

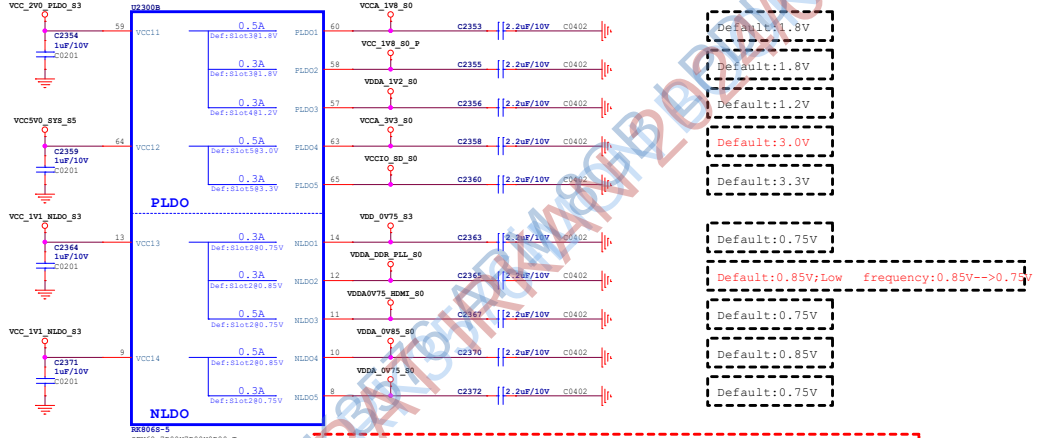


PMIC RK806S-5 Managerment

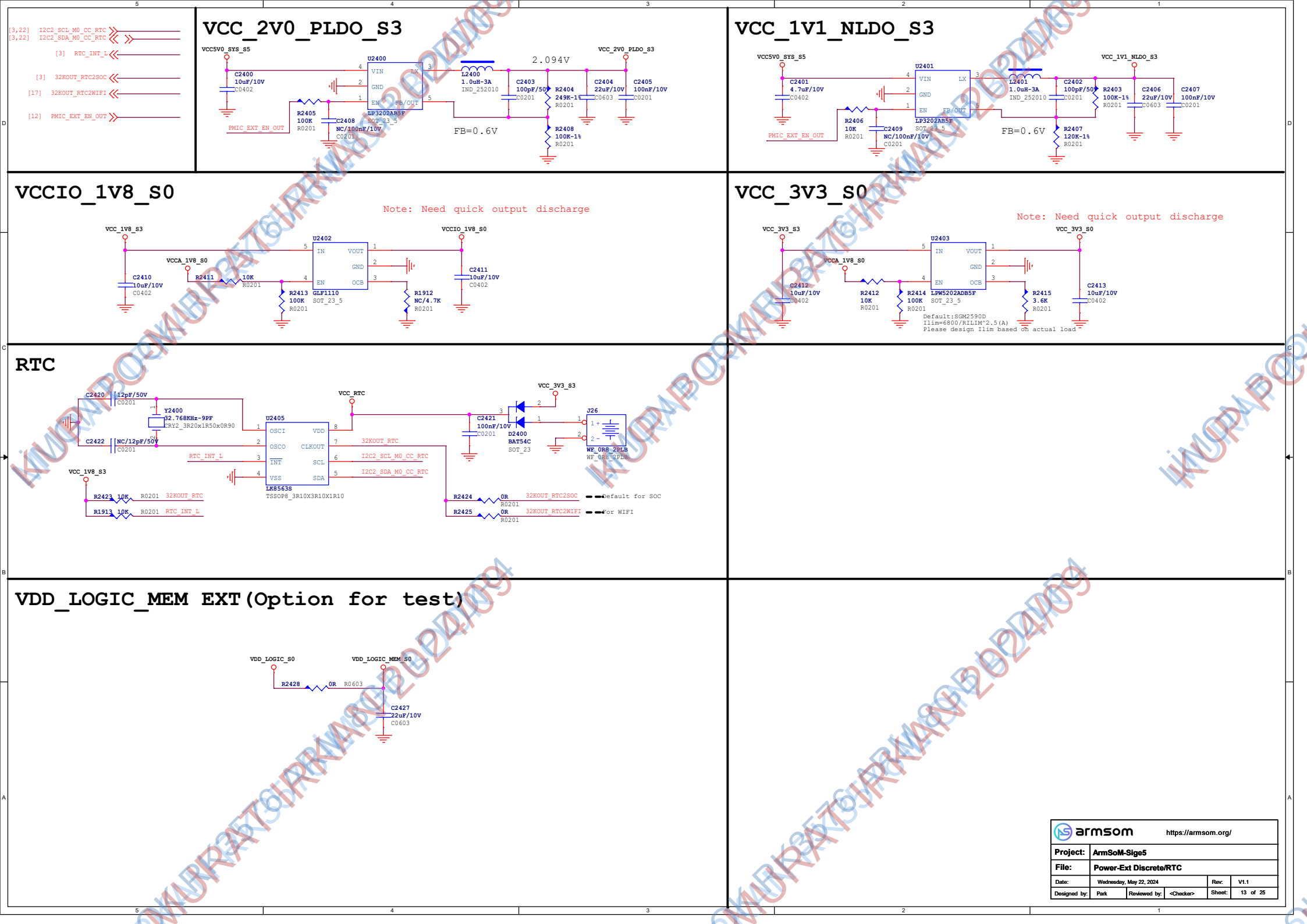
Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



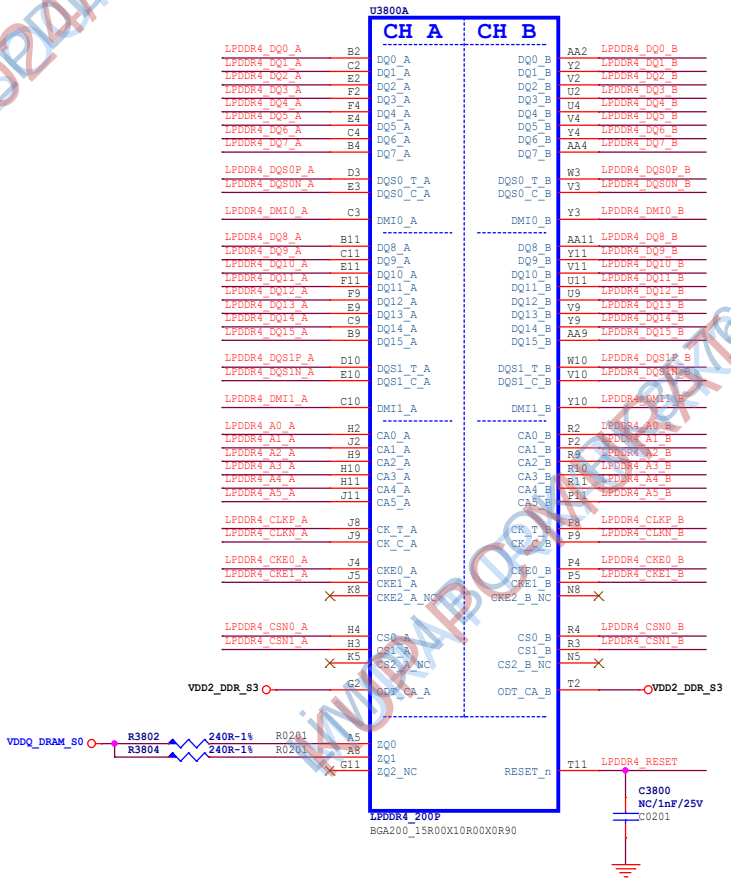
PMIC RK806S-5 LDO

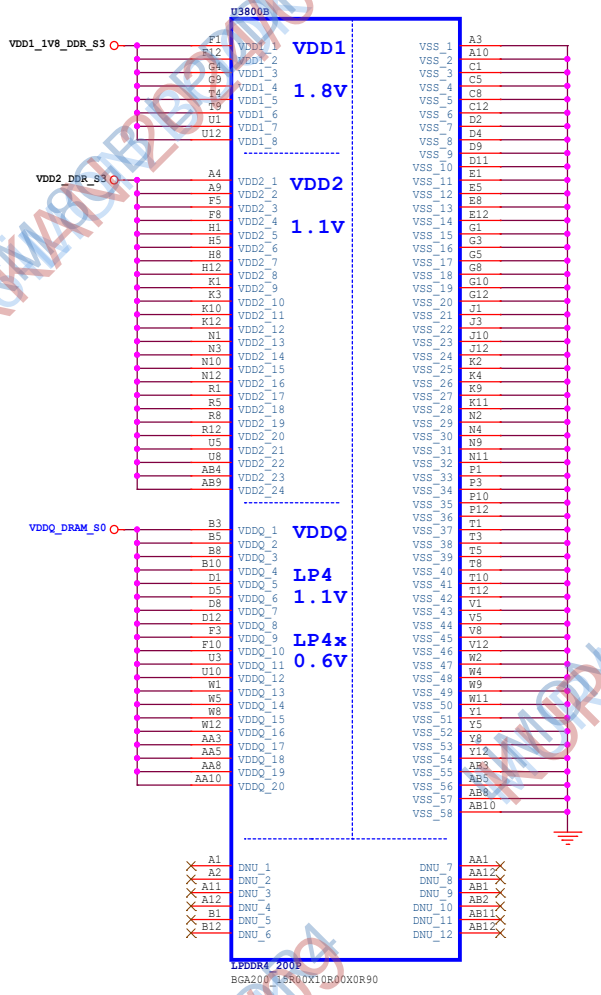


armsom	https://armsom.org/		
Project:	ArmSoM-Sige5		
File:	Power-PMIC RK806S-5		
Date:	Wednesday, May 22, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 12 of 25


[3,22] I2C2_SCL_M0_CC_RTC
[3,22] I2C2_SDA_M0_CC_RTC
[3] RTC_INT_L
[3] 32KOUT_RTC2SOC
[17] 32KOUT_RTC2WIFI
[12] PMIC_EXT_EN_OUT
VCC_2V0_PLDO_S3
VCC5V0_SYS_S5
U2400
LP3202AB5F
L2400 1.0uH-3A IND_252010
2.094V
FB=0.6V
VCC_1V1_NLDO_S3
U2401
LP3202AB5F
FB=0.6V
VCCIO_1V8_S0
Note: Need quick output discharge
U2402
GLF1110
VCC_3V3_S0
U2403
LPW5202ADB5F
Default:SGM2590D
Ilim=6800/RILIM^2.5(A)
Please design Ilim based on actual load
RTC
U2405
LK8563S
TSSOP8_3R10X3R10X1R10
Y2400 32.768KHz-9PF
D2400 BAT54C
J26
WF_0R8_2PLB
Default for SOC
For WIFI
VDD_LOGIC_MEM EXT(Option for test)
VDD_LOGIC_S0
VDD_LOGIC_MEM_S0
armsom https://armsom.org/
Project: ArmSoM-Sige5
File: Power-Ext Discrete/RTC
Date: Wednesday, May 22, 2024
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 13 of 25

LPDDR4/4X

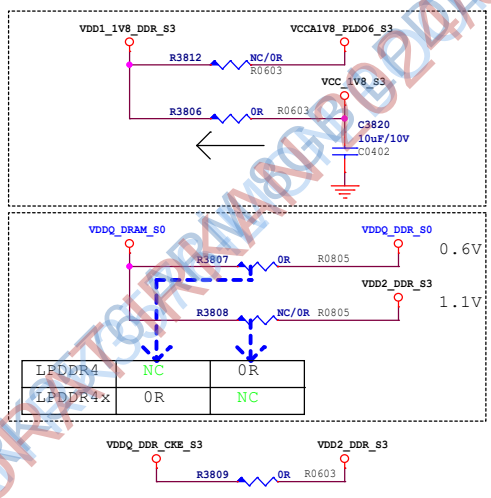


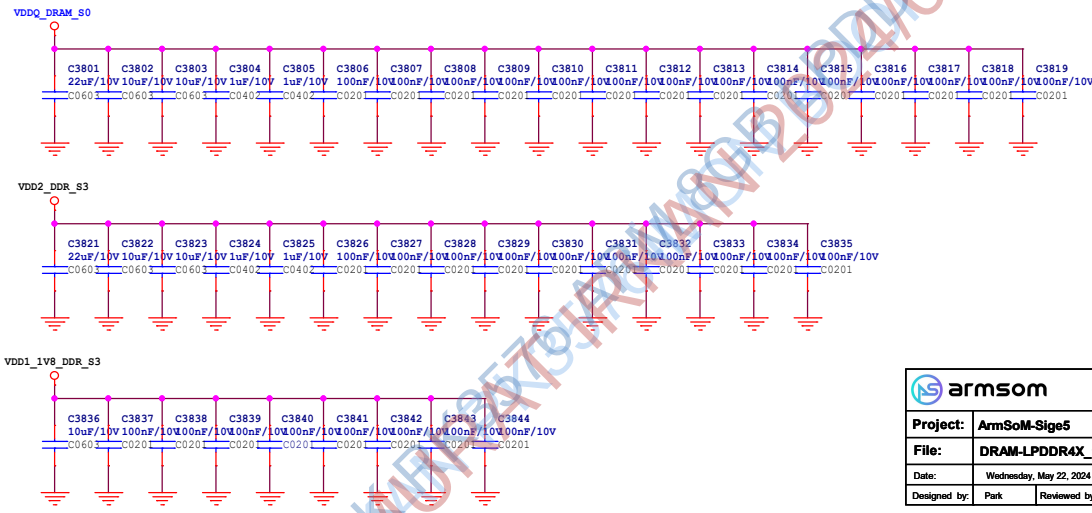


Note:

Sequence:VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

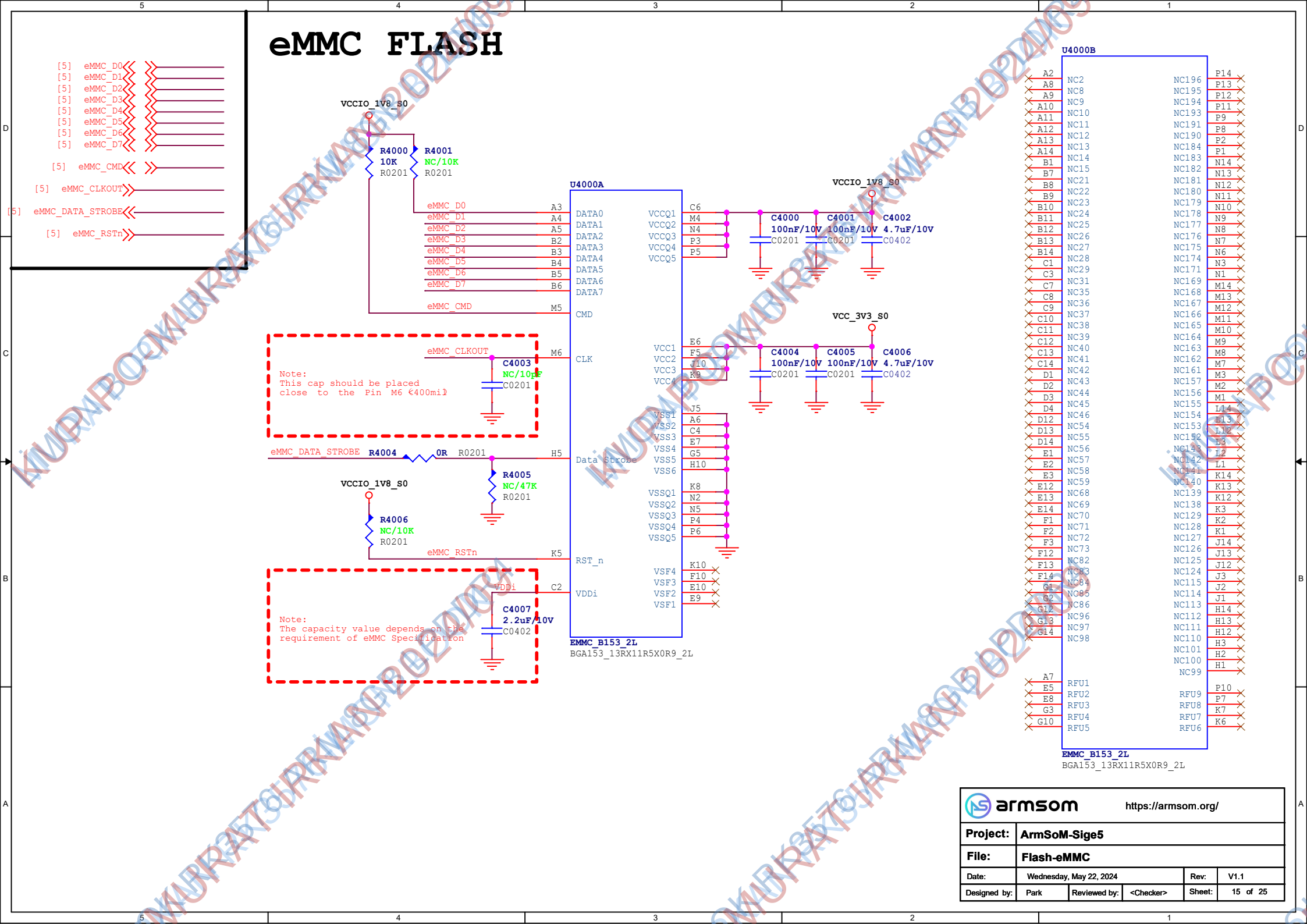




armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	DRAM-LPDDR4X_1X32bit_200P				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 25

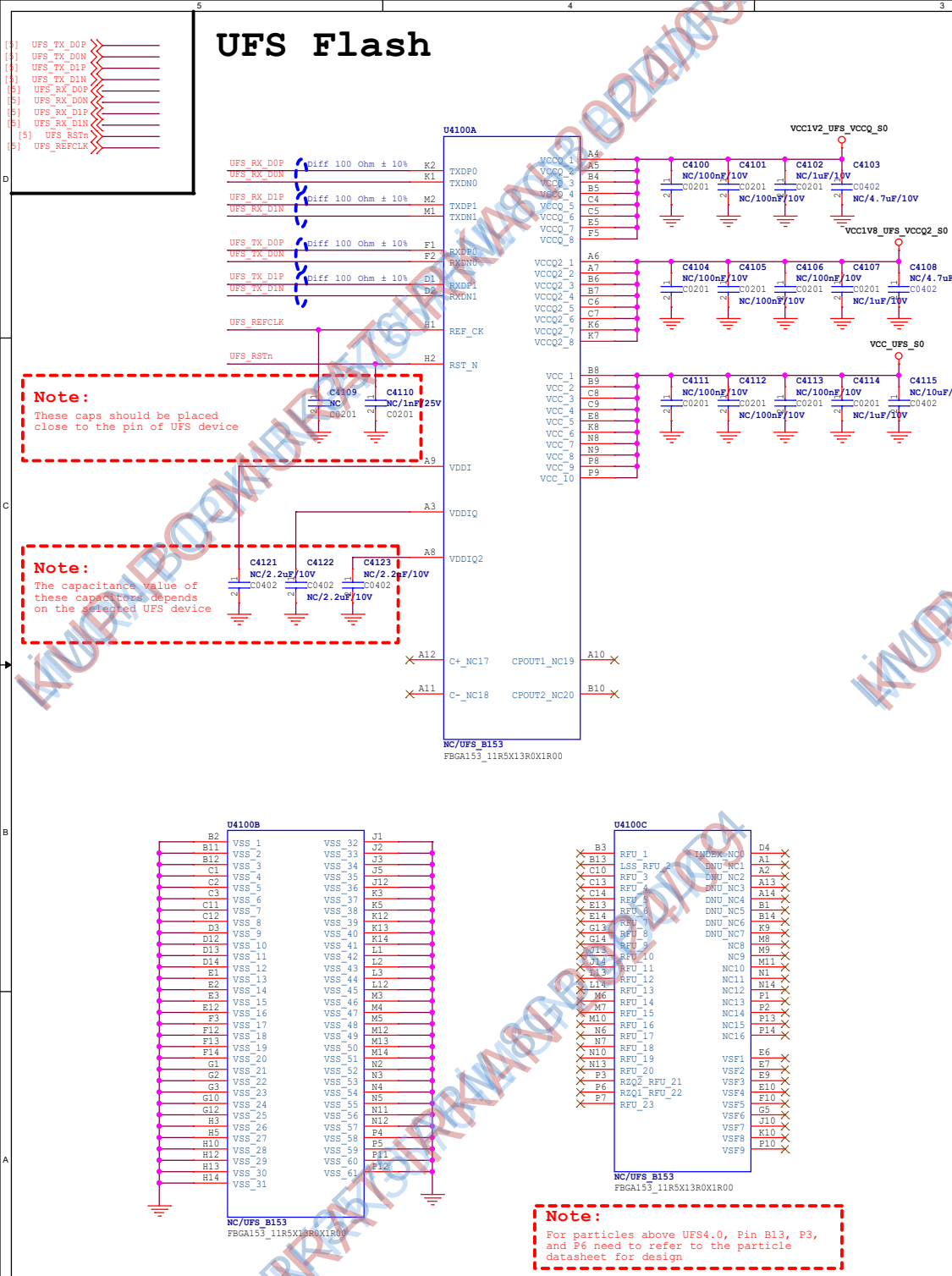
eMMC FLASH



armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	Flash-eMMC				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 25

UFS Flash



Note:
These caps should be placed close to the pin of UFS device

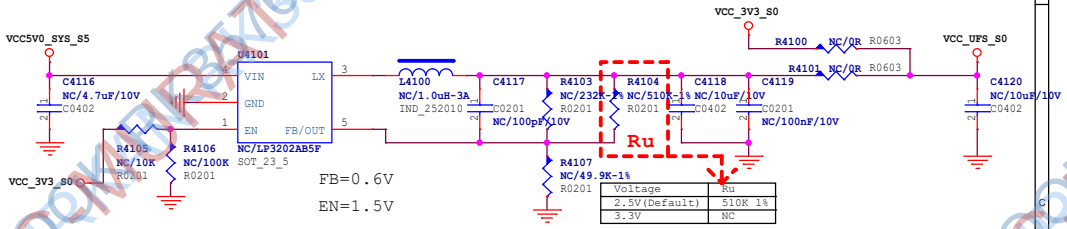
Note:
The capacitance value of these capacitors depends on the selected UFS device

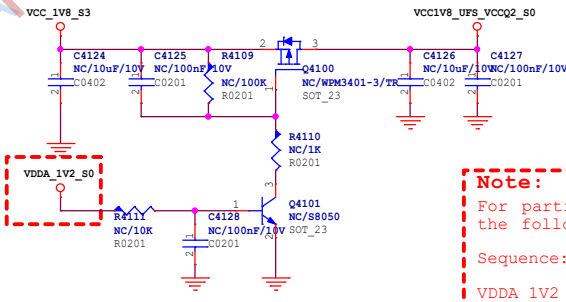
Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

UFS POWER

	VCCQ	VCCQ2	VCC	
UFS2.0	1.2V	1.8V	3.3V	Default UFS device: UFS2.2
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	
UFS4.0	1.2V	No Connect	2.5V	
Sequence:VCCQ2->VCCQ, VCC is independent				

Note: Do not support UFS4.0 Device!
The power ball that is not used at the particle must be kept floating.

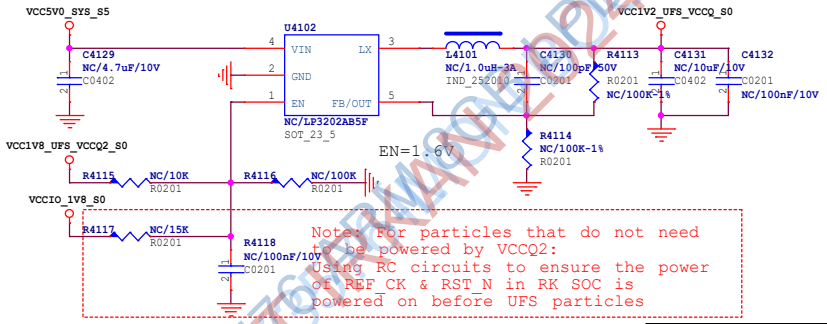




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

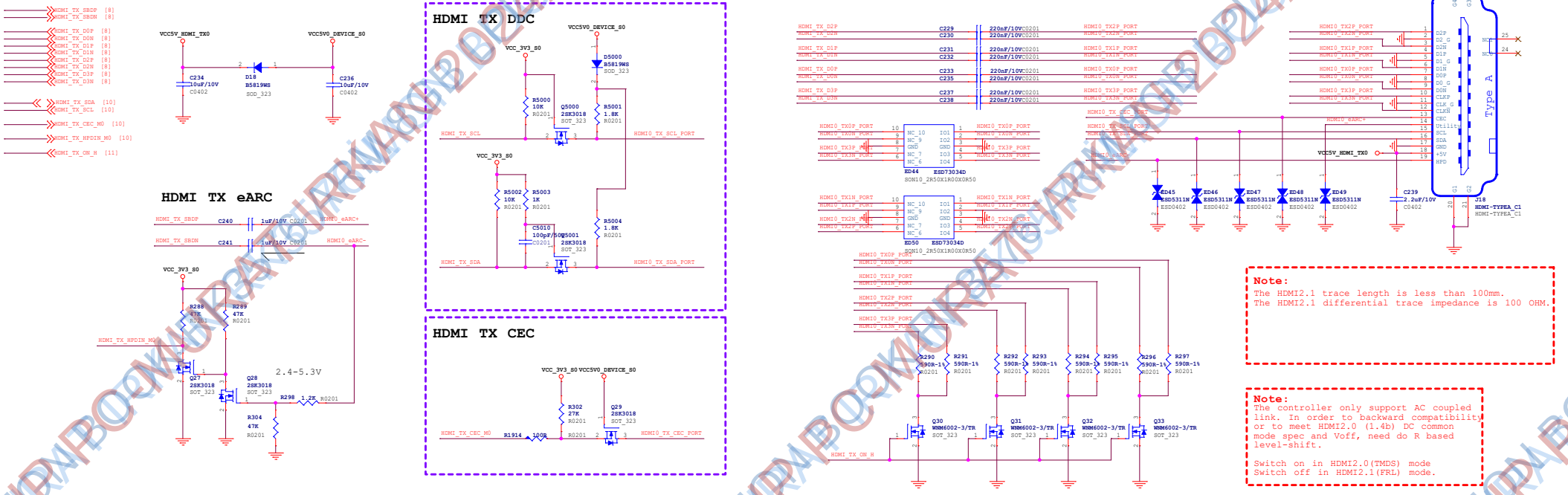
VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles



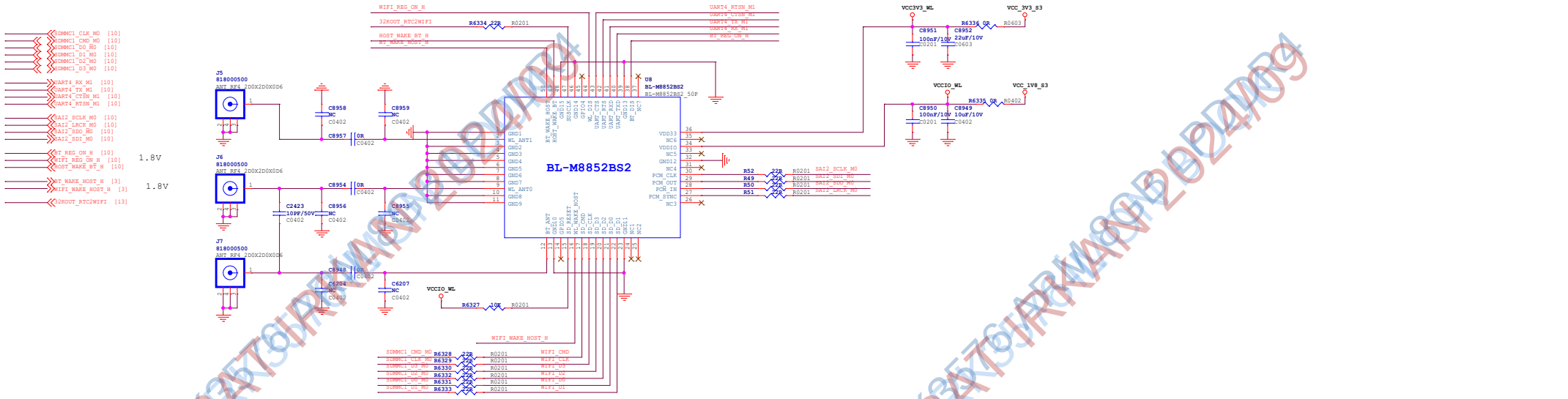
Note: For particles that do not need to be powered by VCCQ2:
Using RC circuits to ensure the power of REF_CK & RST_N in RK SOC is powered on before UFS particles

armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	Flash-UFS				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 25

HDMI TX0

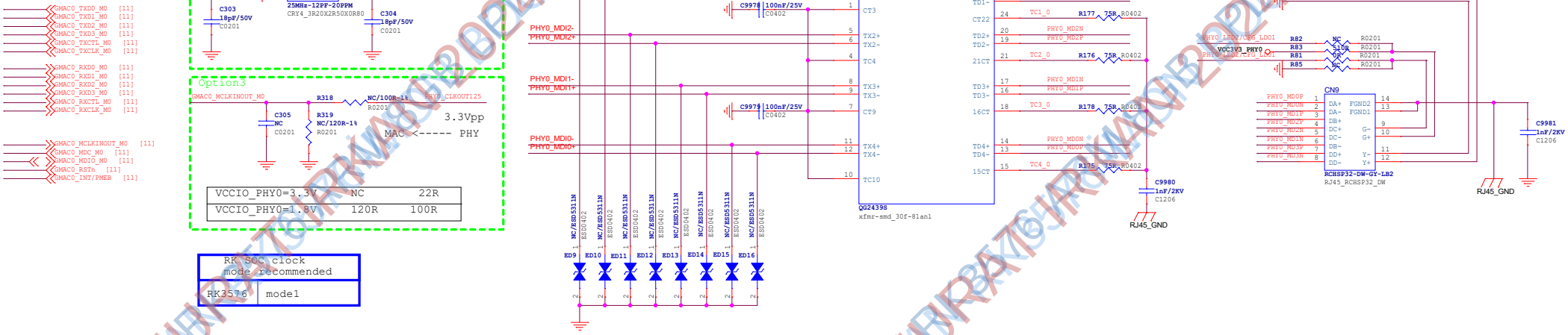


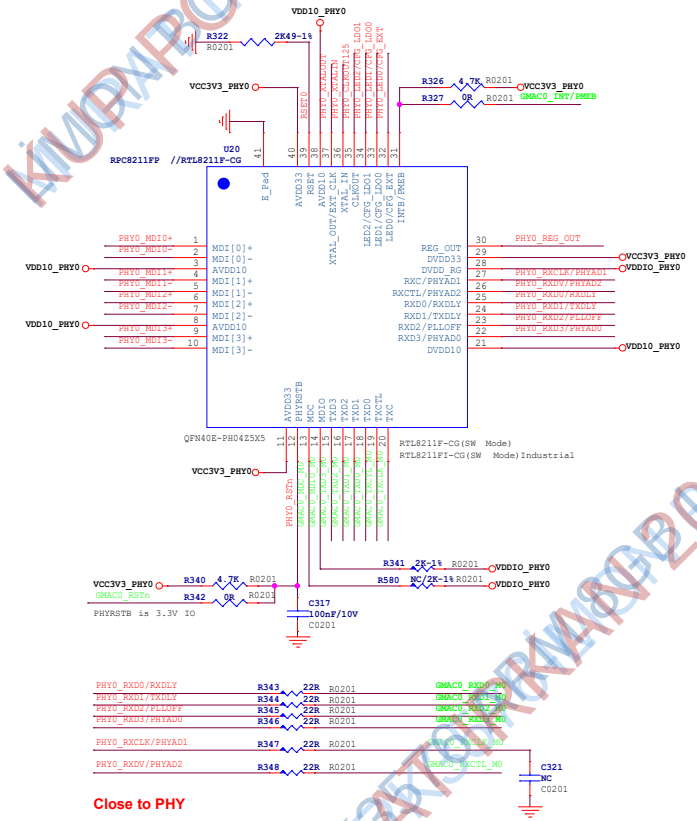
SDIO WIFI6/BT Module-2T2R

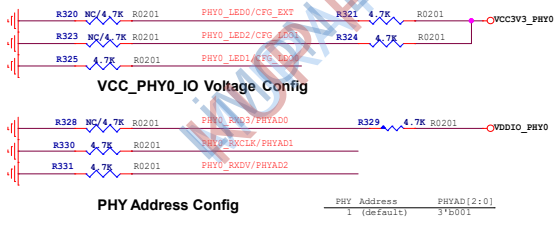


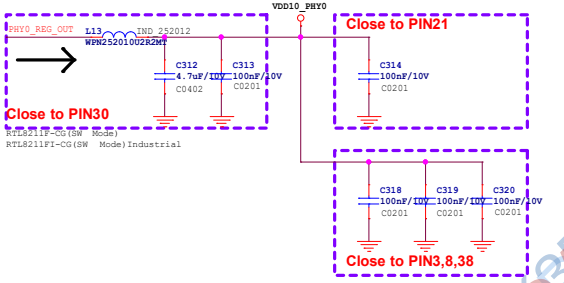
armsom	https://armsom.org/
Project:	ArmSoM-Sige5
File:	HDMI_TX0_WIFI
Date:	Wednesday, May 22, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	17 of 25

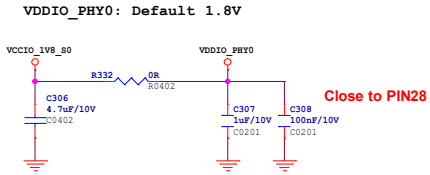
GPHY To JR45

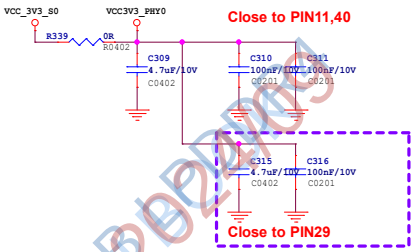








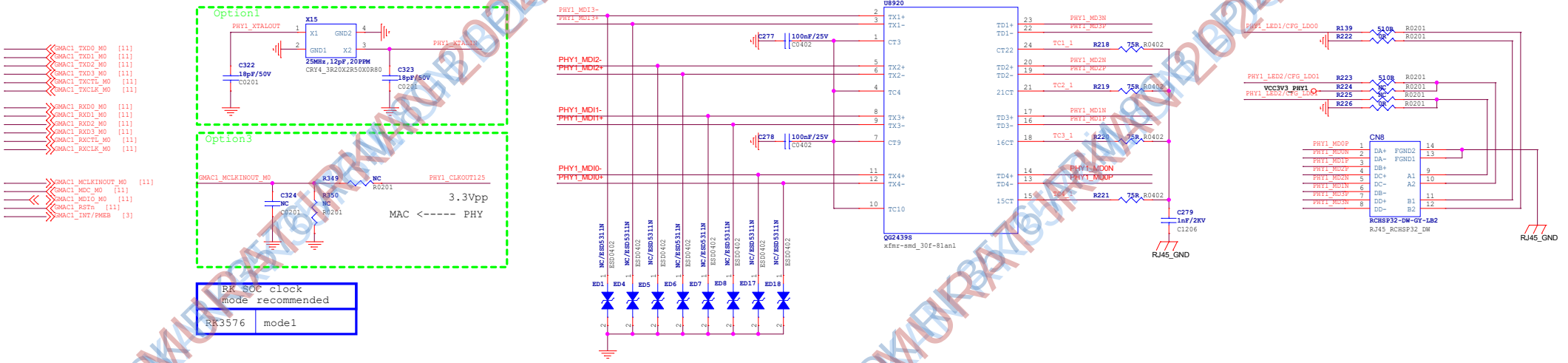




armsom https://armsom.org/

Project:	ArmSoM-Sige5		
File:	Ethernet-GPHY		
Date:	Wednesday, May 22, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 18 of 25

Giga PHY1_WAN



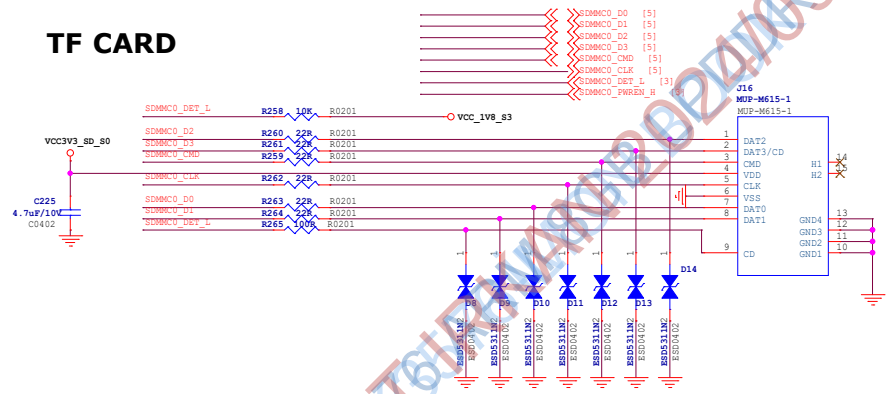
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO Pad. 0:Integrated LDO for IO Pad. CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

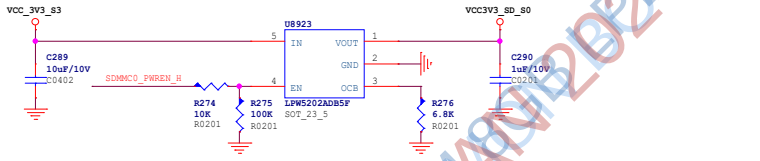
PHY Address	PHYAD[2:0]
1 (default)	3'b001

armsom https://armsom.org/

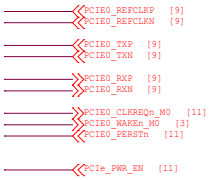
Project:	ArmSoM-Sige5				
File:	Ethernet-GMAC1				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	19 of 25

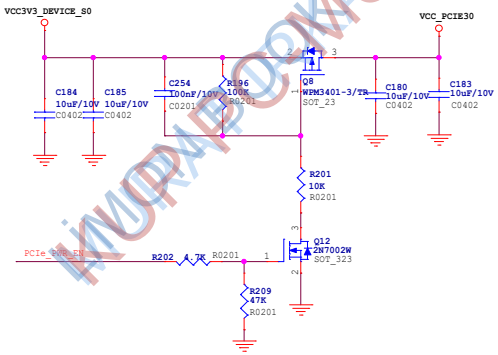
TF CARD

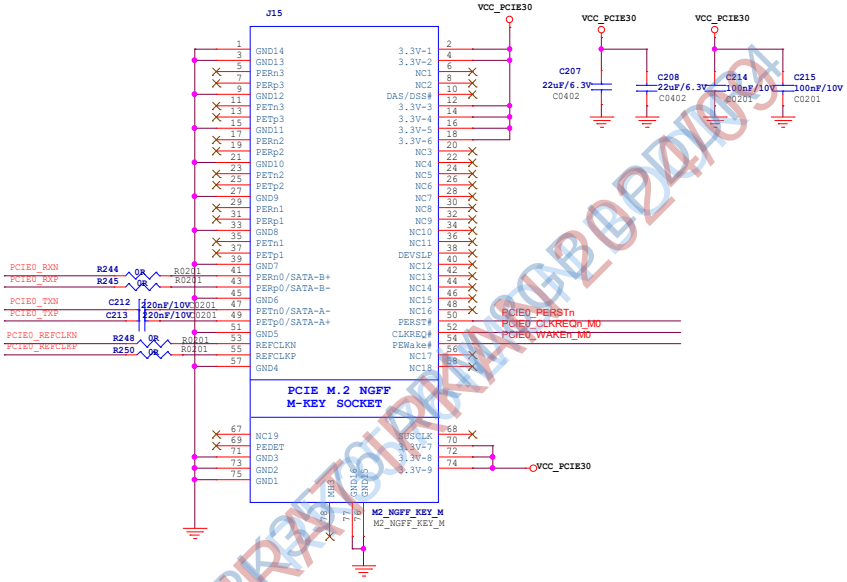




M.2_PCIE

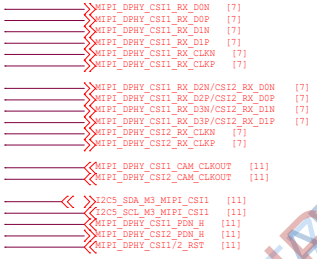


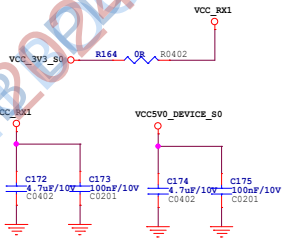


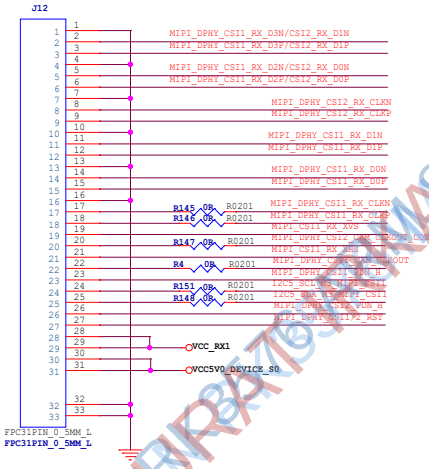


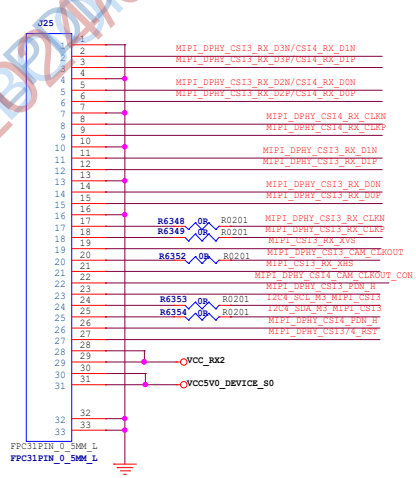
armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	M2_TF				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	20 of 25

CSI0_MIPI

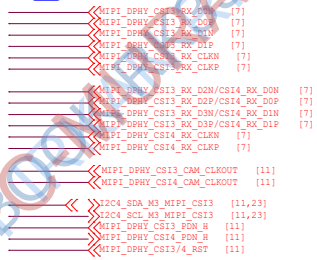


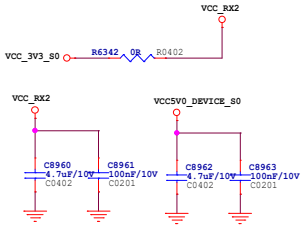


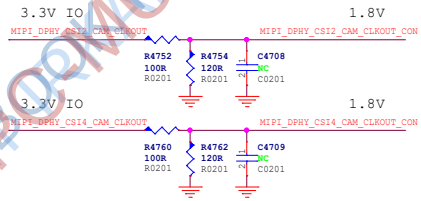




CS1_MIPI







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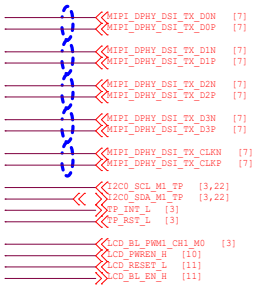
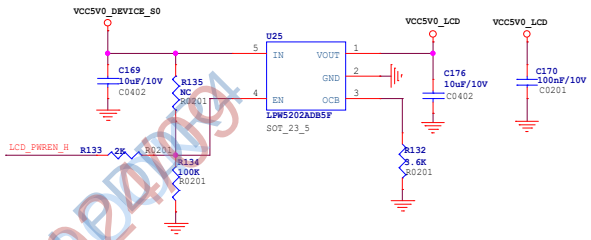
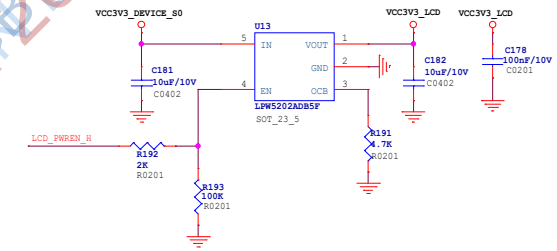
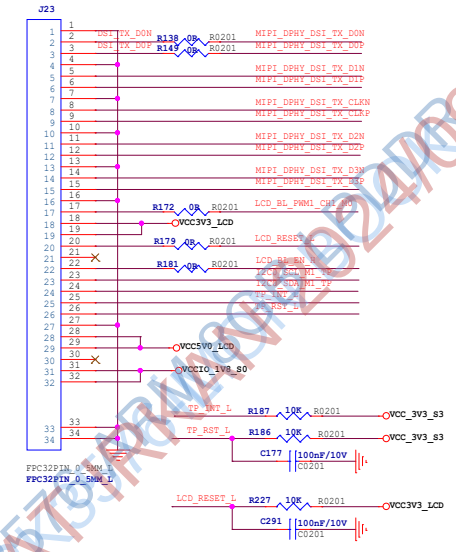


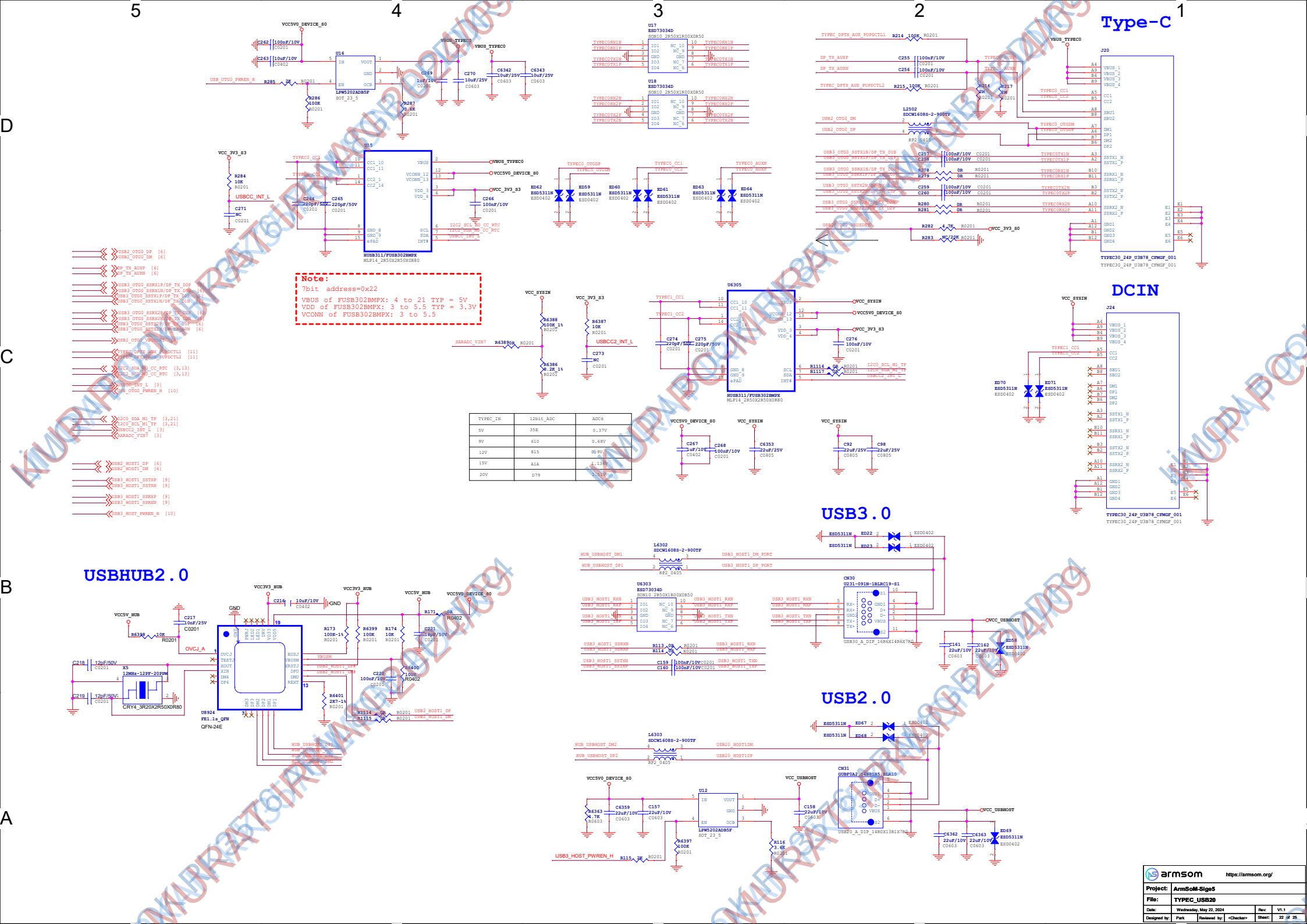


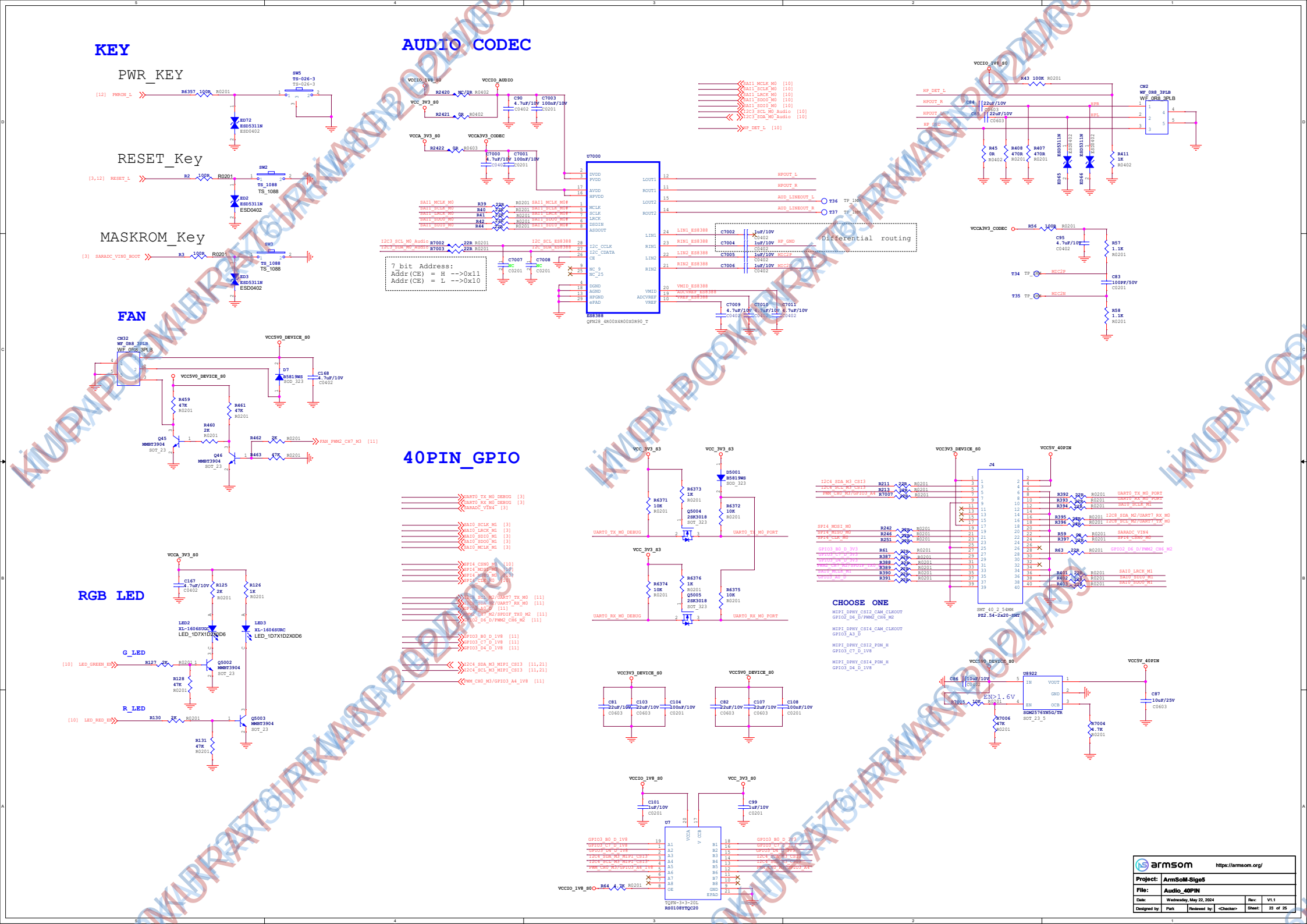


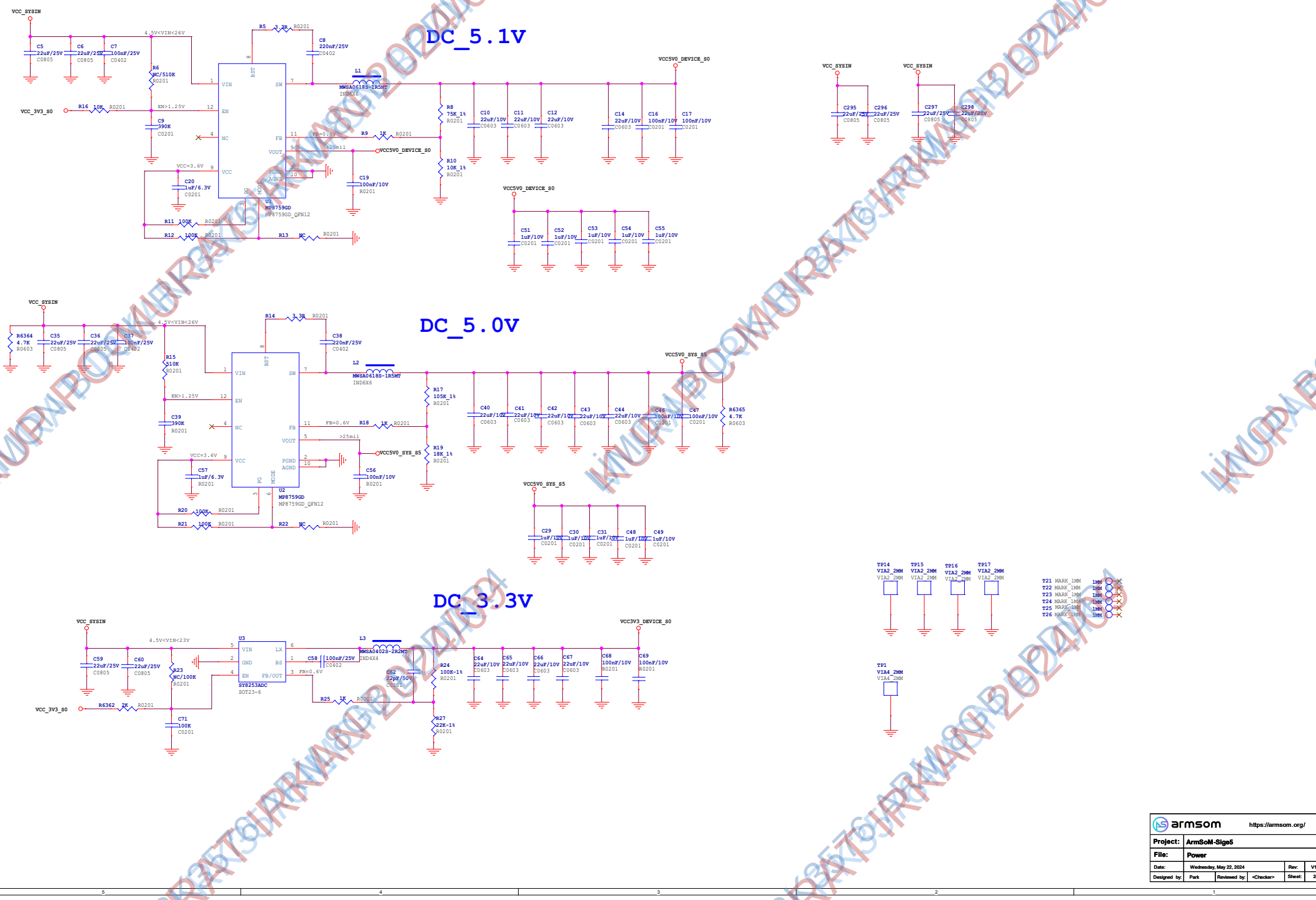


armsom https://armsom.org/

Project:	ArmSoM-Sige5				
File:	MIPI_RX_CSI/MIPI_DSI				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	21 of 25


Type-C
DCIN
USB3.0
USB2.0
USBHUB2.0
Note:
7bit address=0x22
VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5
TYPEC_IN | 12bit_ADC | ADC6
5V | 35E | 0.37V
9V | 610 | 0.68V
12V | 815 | 0.99V
15V | A1A | 1.13V
20V | D79 | 1.61V
armsom https://armsom.org/
Project: ArmSoM-Sige5
File: TYPEC_USB20
Date: Wednesday, May 22, 2024 Rev: V1.1
Designed by: Park Reviewed by: <Checker> Sheet: 22 of 25


KEY
PWR_KEY
RESET_Key
MASKROM_Key
AUDIO CODEC
7_bit Address:
Addr(CE) = H -->0x11
Addr(CE) = L -->0x10
differential routing
FAN
40PIN_GPIO
RGB LED
G_LED
R_LED
CHOOSE ONE
armsom
https://armsom.org/
Project: ArmSoM-Sige5
File: Audio_40PIN
Date: Wednesday, May 22, 2024
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 23 of 25



armsom	https://armsom.org/				
Project:	ArmSoM-Sige5				
File:	Power				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	24 of 25

Revision History

Version	Date	By	Change Dscription	Approved
V1.0	2024-03-27	SL Chen	First release;	
V1.1	2024-05-15	SL Chen	1.U1/U2 Pin5 connect to output; TF_DET_L connect to VCC_1V8_S3; J23 Pin2&Pin3 change position; 2.J25 MIPI_DPHY_CSI3_CAM_CLKOUT&MIPI_DPHY_CSI4_CAM_CLKOUT_CON change position;	