H11H4-AM V:1.1

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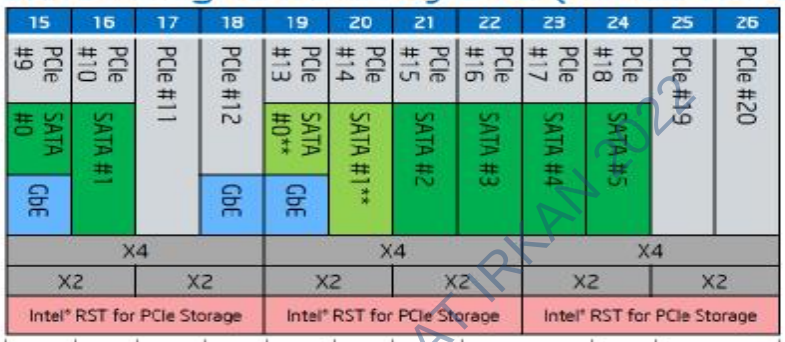
HSIO Lane Assignements by SKU (Lanes 1-14)

Sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB3/ GTS	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ VLAN	PCIe	PCIe	PCIe

HSIO Lane Assignements by SKU (Lanes 15-26)



Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

Elitegroup Computer Systems

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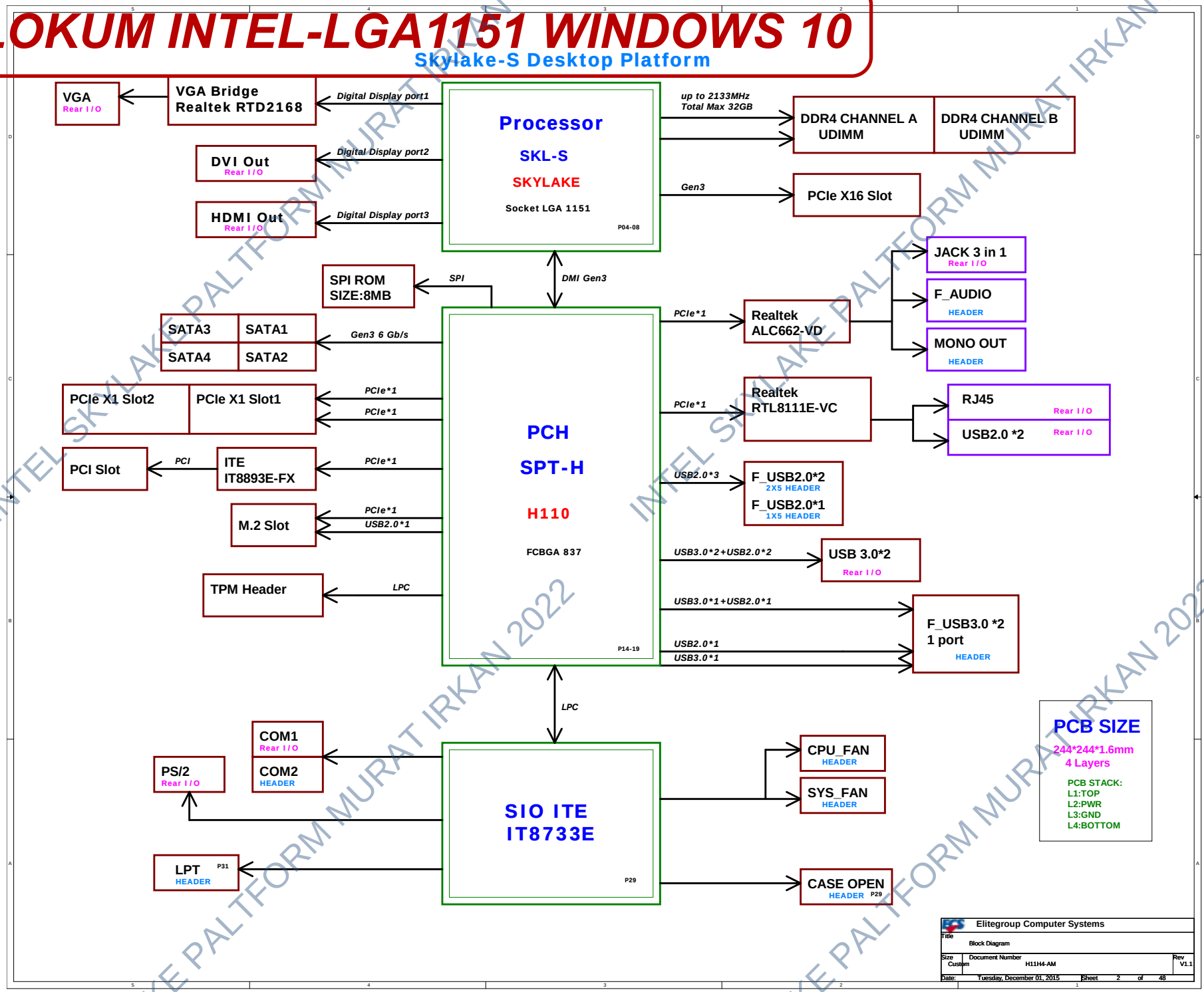
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

LOKUM INTEL-LGA1151 WINDOWS 10

Skylake-S Desktop Platform



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

PCH-GPIO function

Data:2014/10/02

Pin Name	Power Well	Usage	Default Status	Boot Set(BIOS Check)
GPP_A11	3VSB	PME_L	PME#	PME#
GPP_G13	VCC3	HDPANEL_DETECT	GPI	GPI
GPP_G14	VCC3	on-board TPM detect	GPI	GPI
GPP_E7	VCC3	THERMAL_SD	GPI	GPI
GPP_B3	3VSB	BT_DIS_L	GPI	GPO-->Hi
GPP_H15	3VSB	for ACER reserve	GPI	GPI
GPP_H14	3VSB	for ACER reserve	GPI	GPI
GPP_E9	3VSB	BIOS WP Jumper	GPI	GPI
GPP_F16	3VSB	USB_EN	GPI	GPO-->Hi
GPP_F17	3VSB	LPC_PME_L	GPI	GPI
GPP_E0	VCC3	OBR	GPI	GPI
GPD11	DSW	LAN_DIS_L	LANPHYPC	LANPHYPC
GPD9	DSW	PCH_RI_L	SLP_WLAN#	GPI
GPD10	DSW	ME Disable	SLP_S5#	GPO-->Low
GPD0	DSW	RLAN_PWR_EN	BATLOW#	GPO-->Hi
GPP_F22	VCC3	PCH_GPP_F22	GPI	PCH_GPP_F22
GPP_G22	VCC3	TP_VGA	GPI	TP_VGA
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPI	CLK_REQ1_M.2_WLAN_L
GPP_B17	3VSB	M.2_DIS_L_R	GPI	M.2_DIS_L_R

SIO-GPIO function

Data:2013/10/01

Pin Name	Power Well	Usage	Default SET

Interrupt mapping

Data:2014/11/10

Function	INT# port	PCIe*1 port	Device

INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

Elitegroup Computer Systems	
Title	GPIO Function/INT# Mapping
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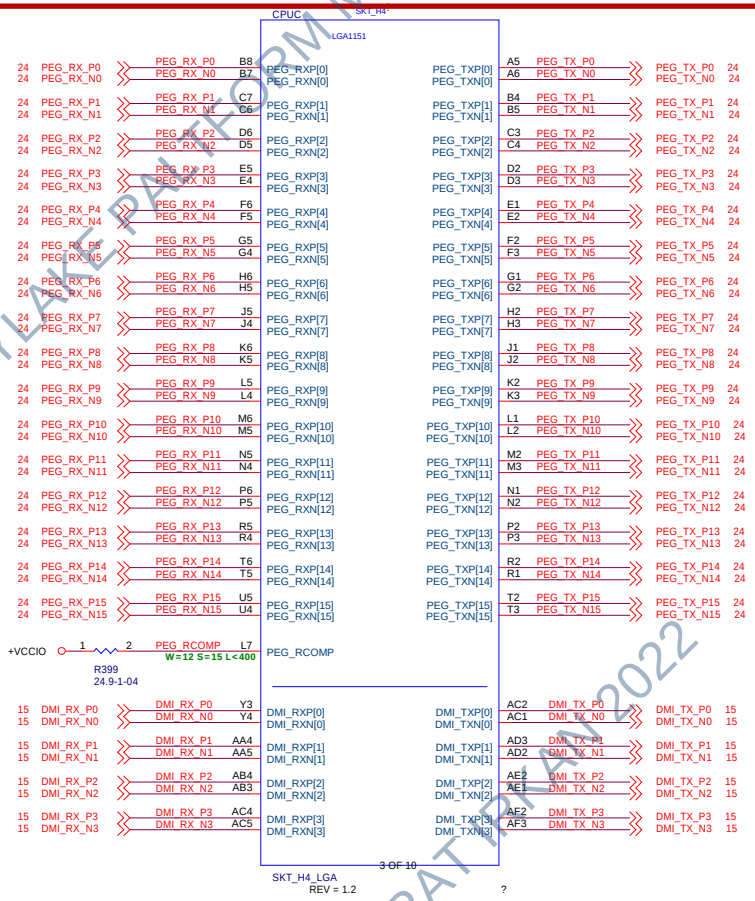
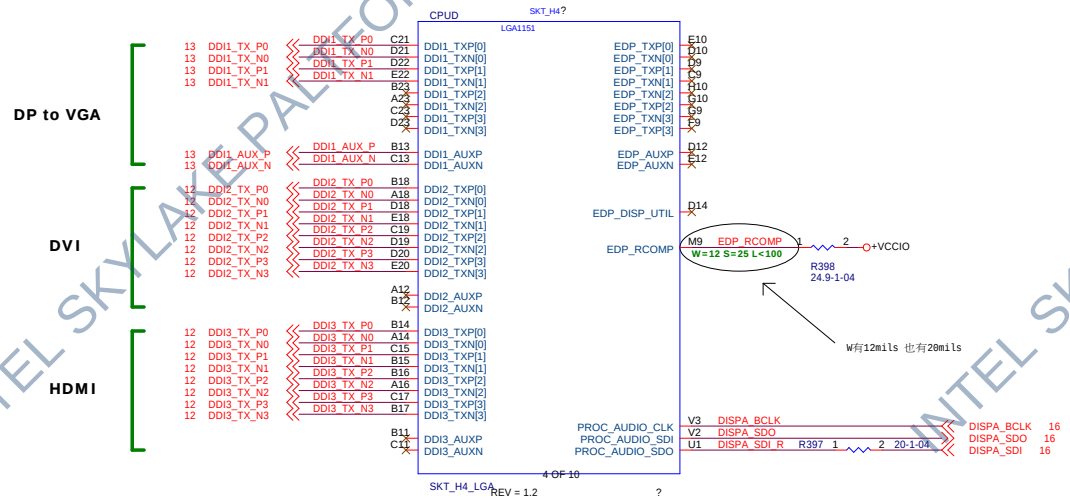
INTEL LGA1151 SOKET PLATFORM





Elitegroup Computer Systems	
Title	CPU-PEG/DMI/DDI/EDP
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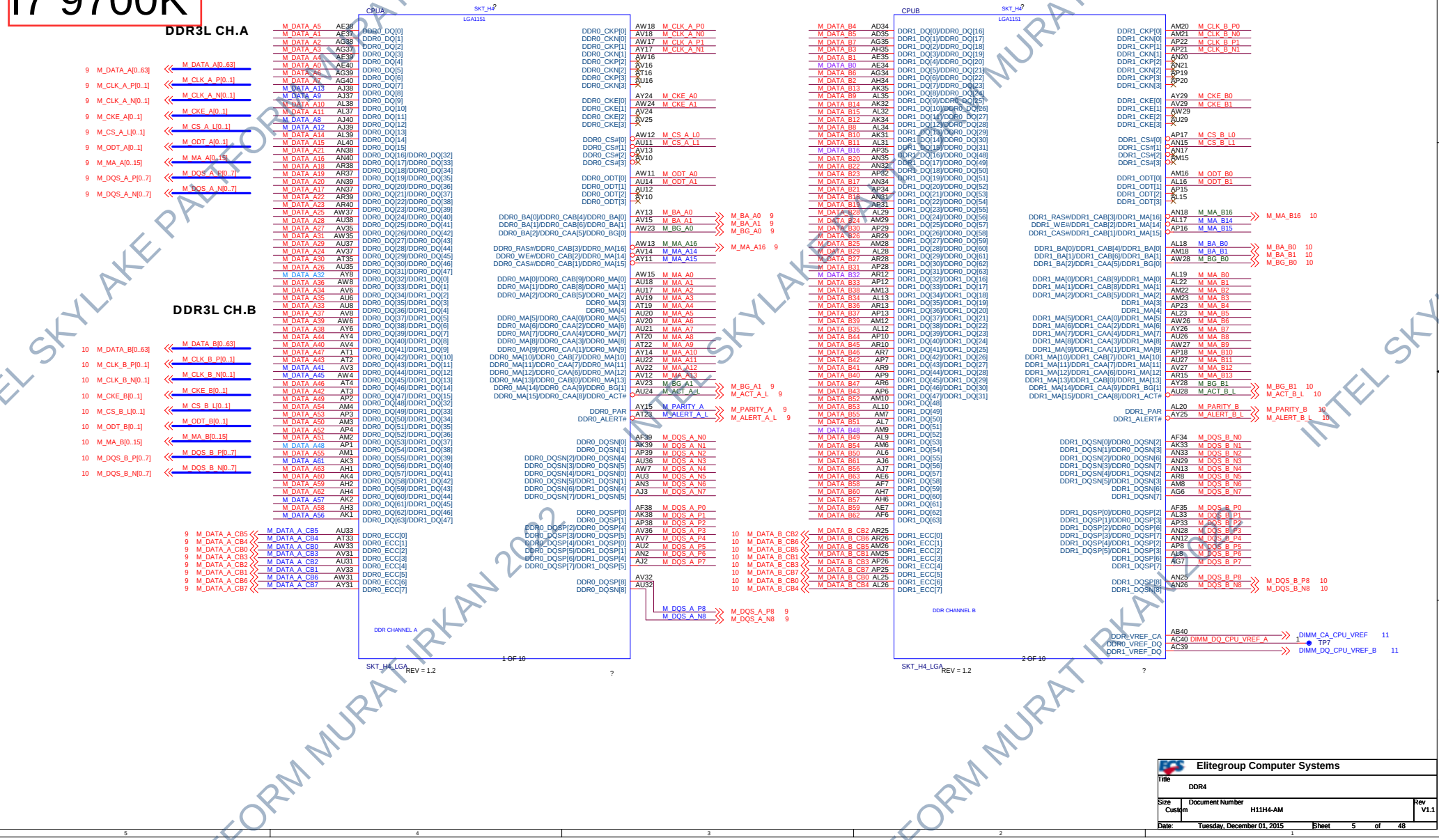
INTEL LGA1151 SOKET PLATFORM

I7 9700K



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Elitegroup Computer Systems	
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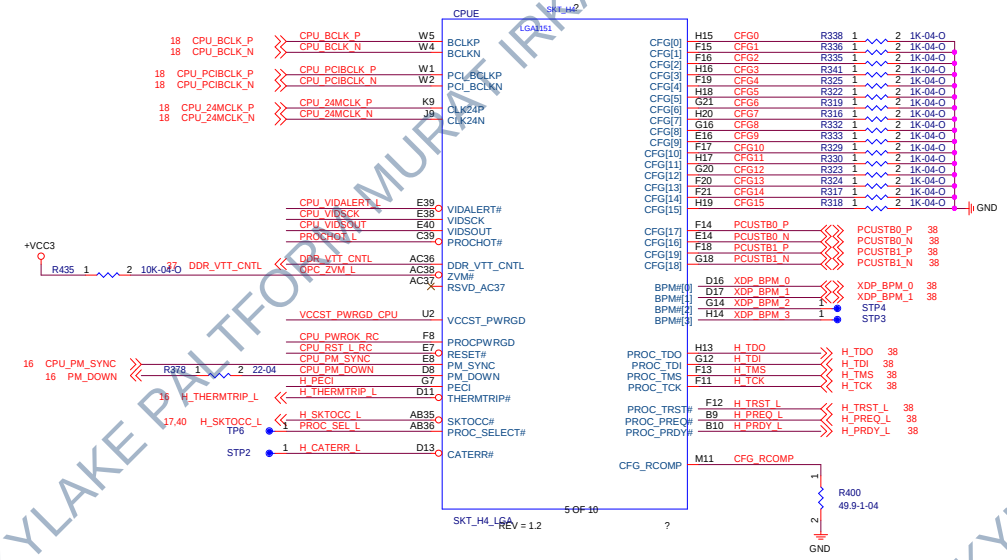
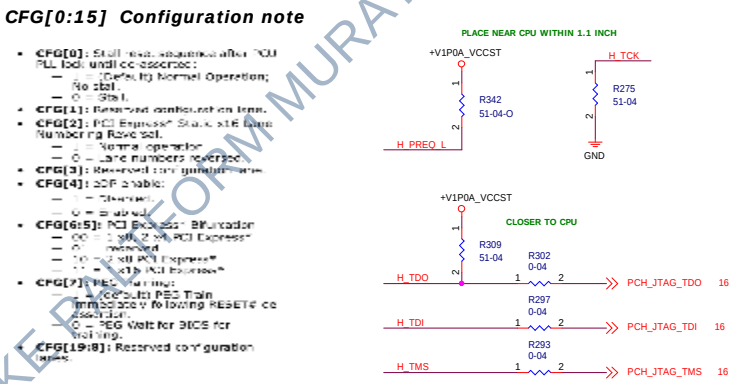
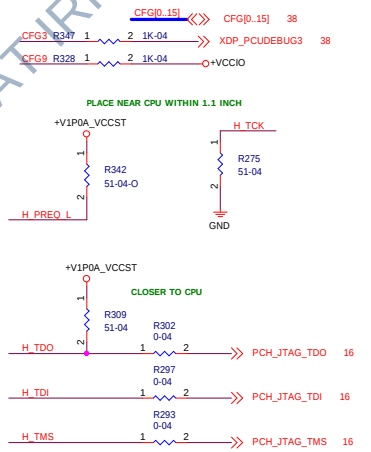
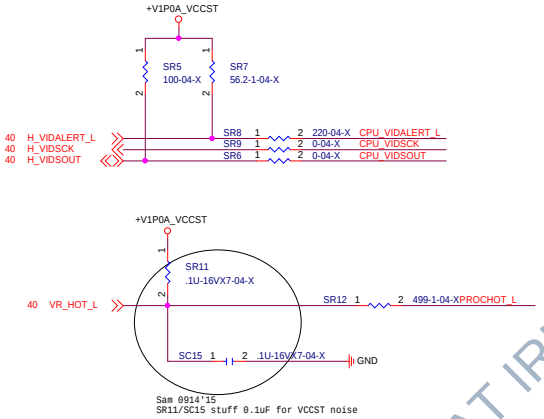


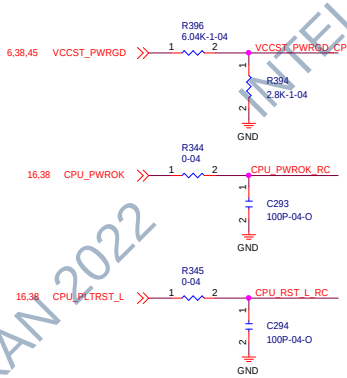




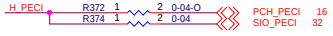
Asynchronous & Sideband Signal



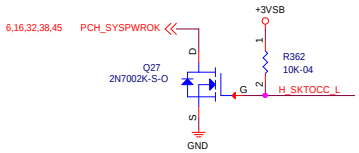
Processor Power Good



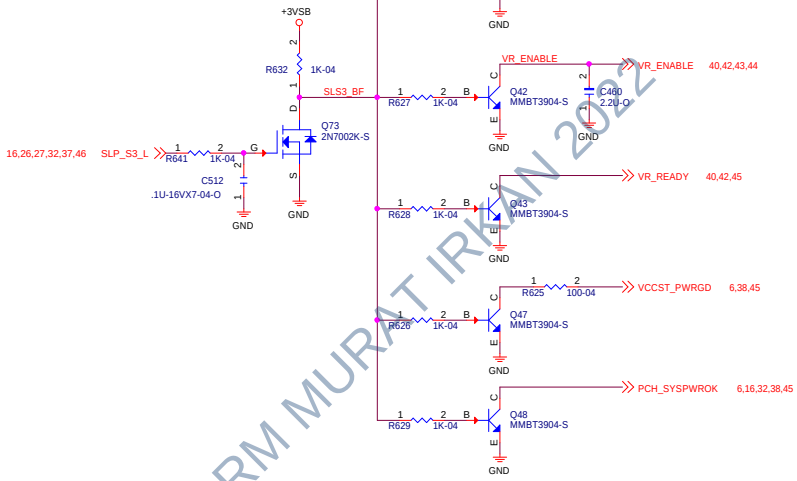
PECI



SKTOCC#



Sequencing Circuit



Elitegroup Computer Systems		
Title: CPU-MISC		
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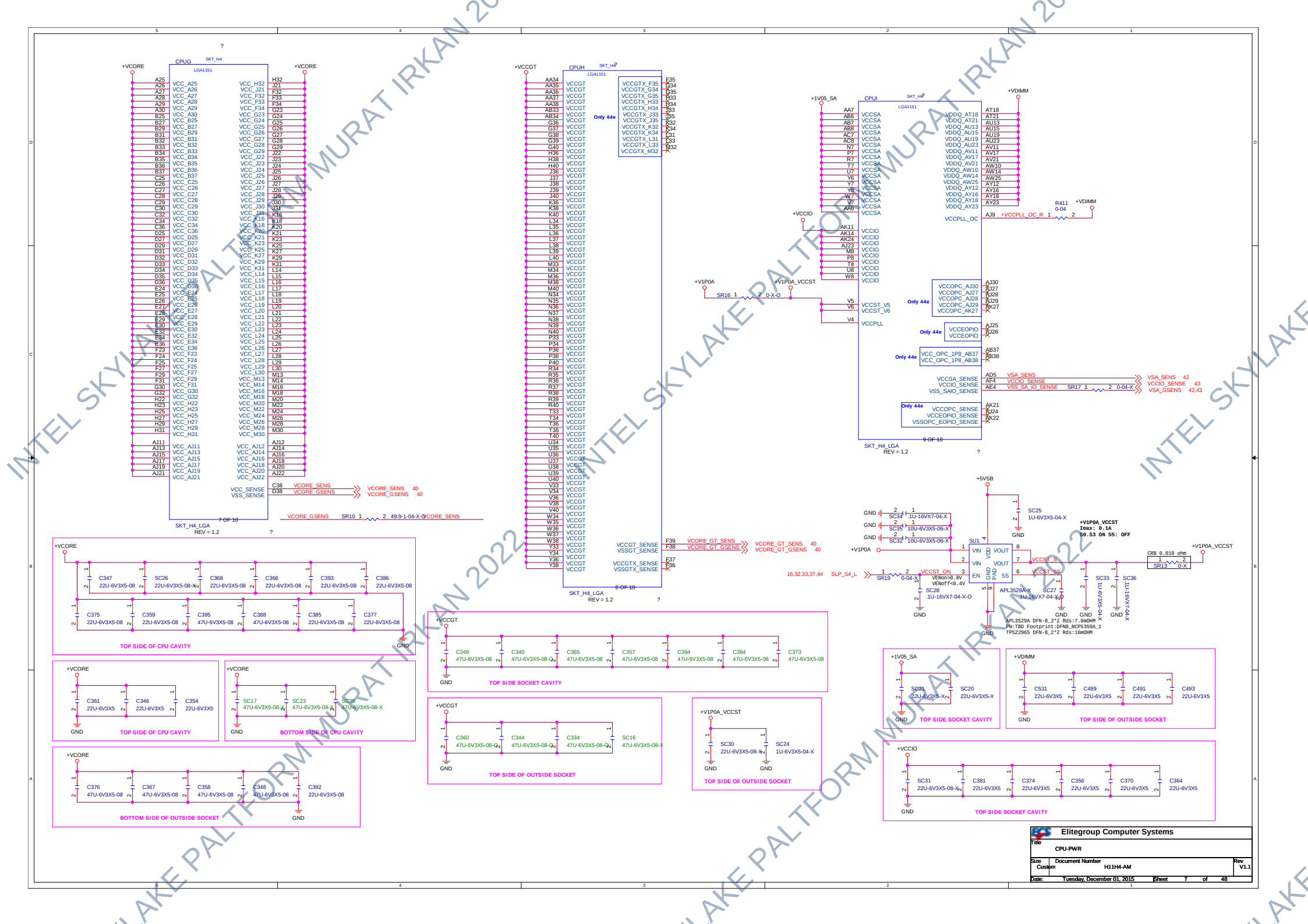

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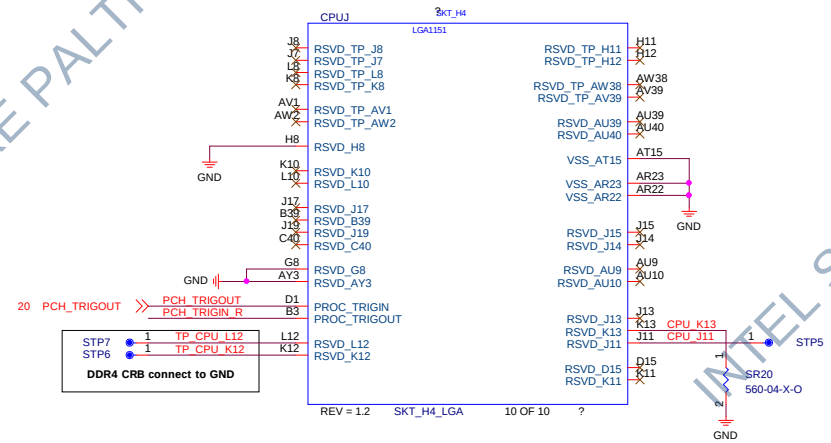

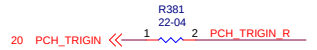

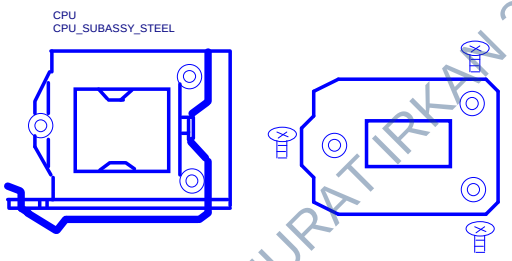

CPU steel (T/U pahse)
PN:20-800-005911
SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES
(替)20-800-007611

Elitegroup Computer Systems			
Title: CPU-GND			
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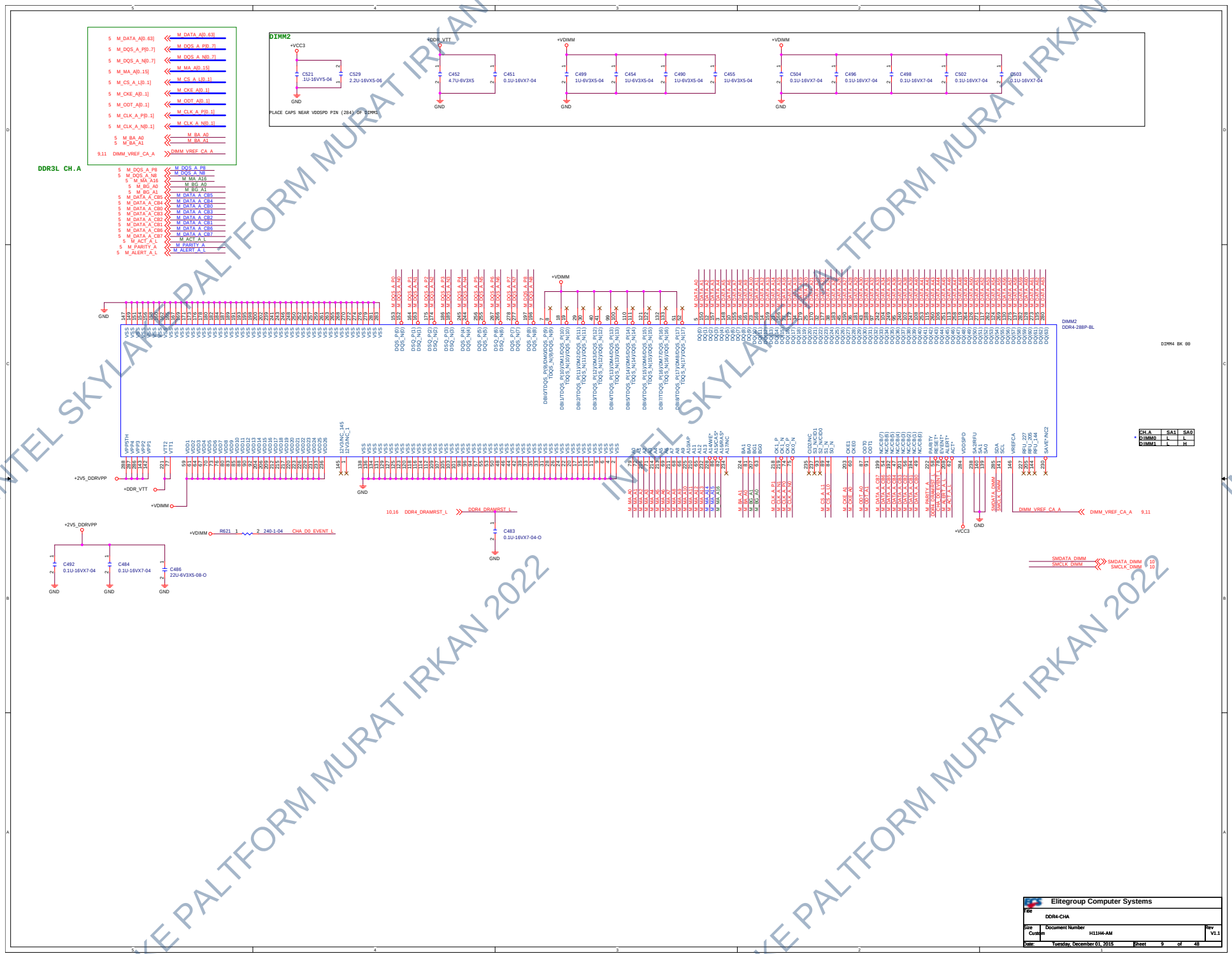

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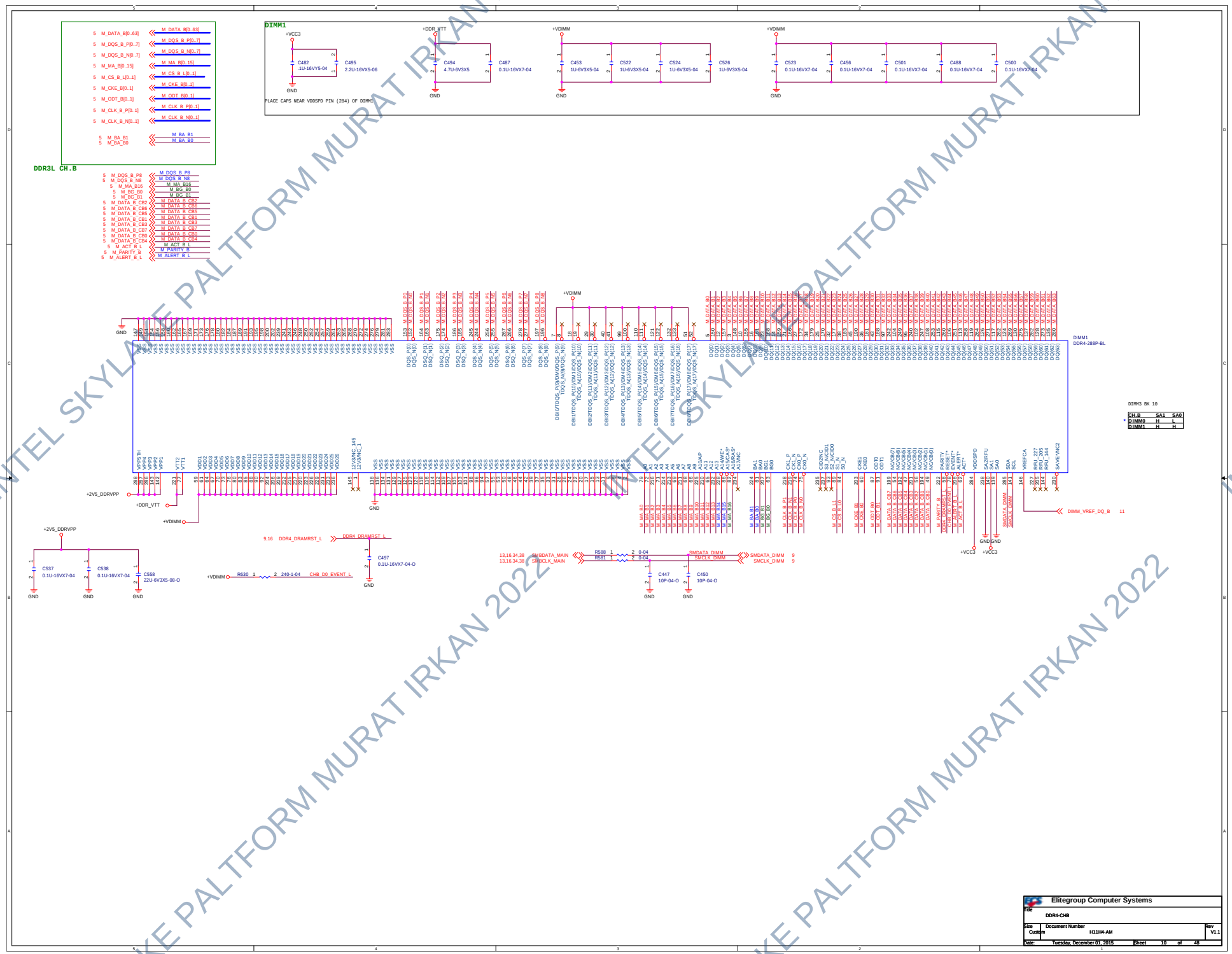

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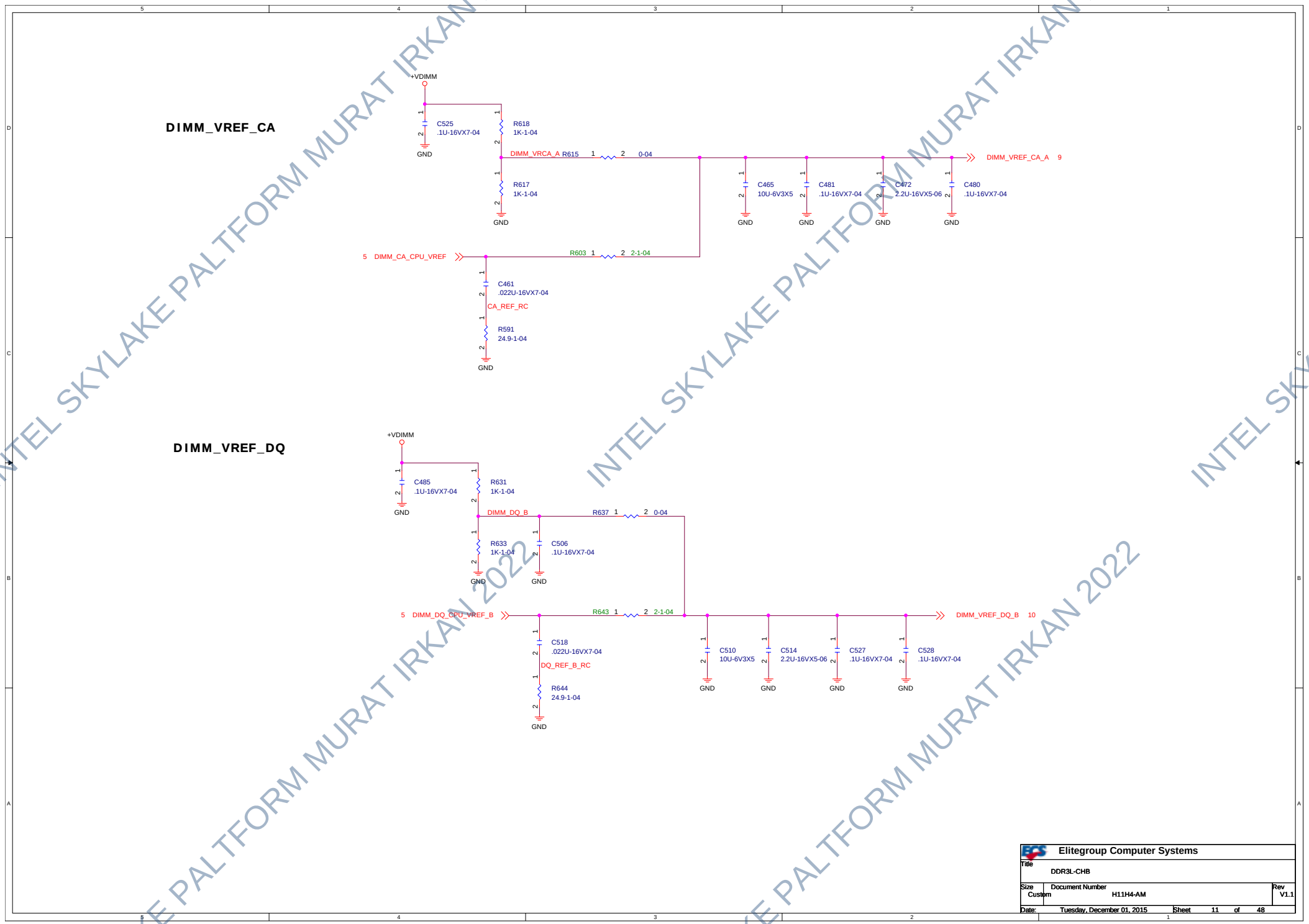

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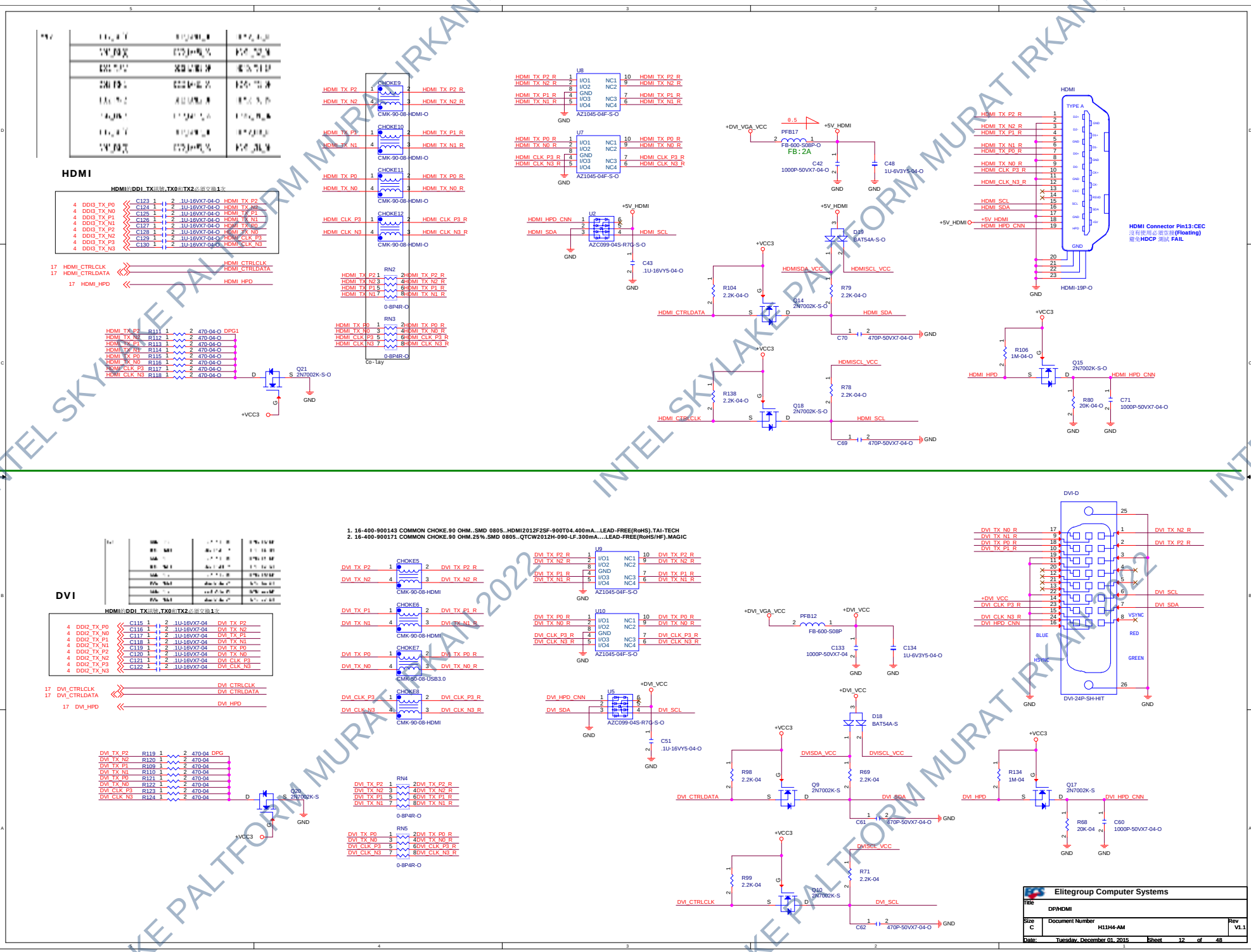

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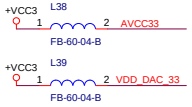
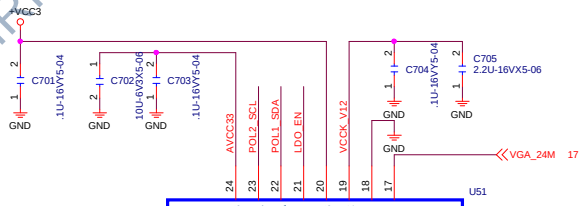
Power



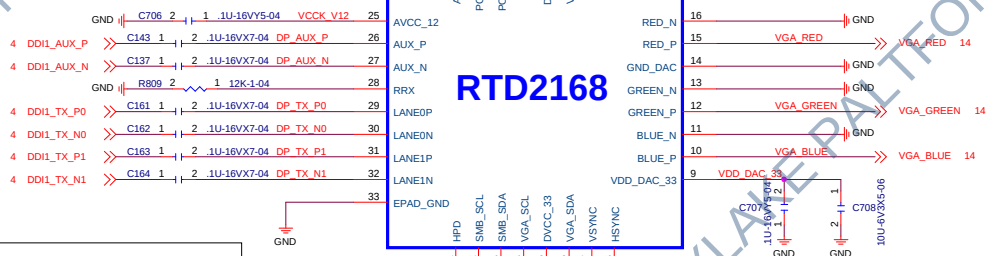


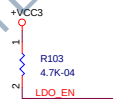
Note: When connected to non-EDID monitor,
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.
XO Pin Pull High : Enable RTD2168 embedded EDID.

10,16,34,38 SMBDATA_MAIN
10,16,34,38 SMBCLK_MAIN
SMBDATA_MAIN
SMBCLK_MAIN

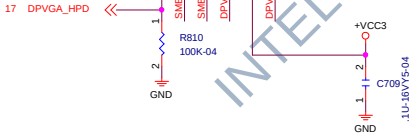
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



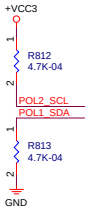


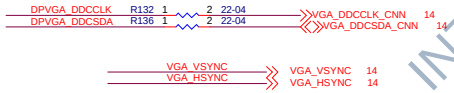
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.





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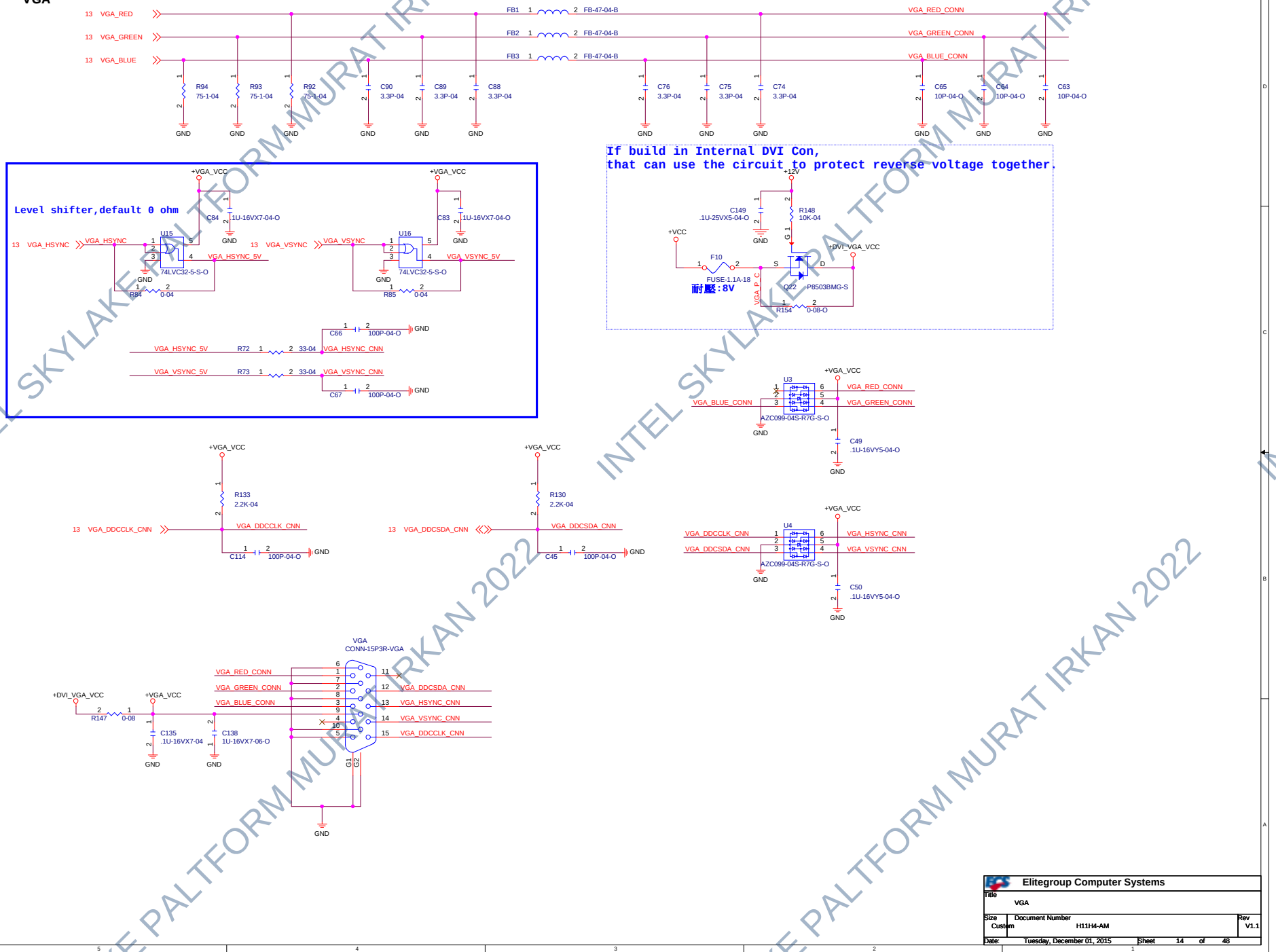
VGA



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

Elitegroup Computer Systems		
Title: VGA		
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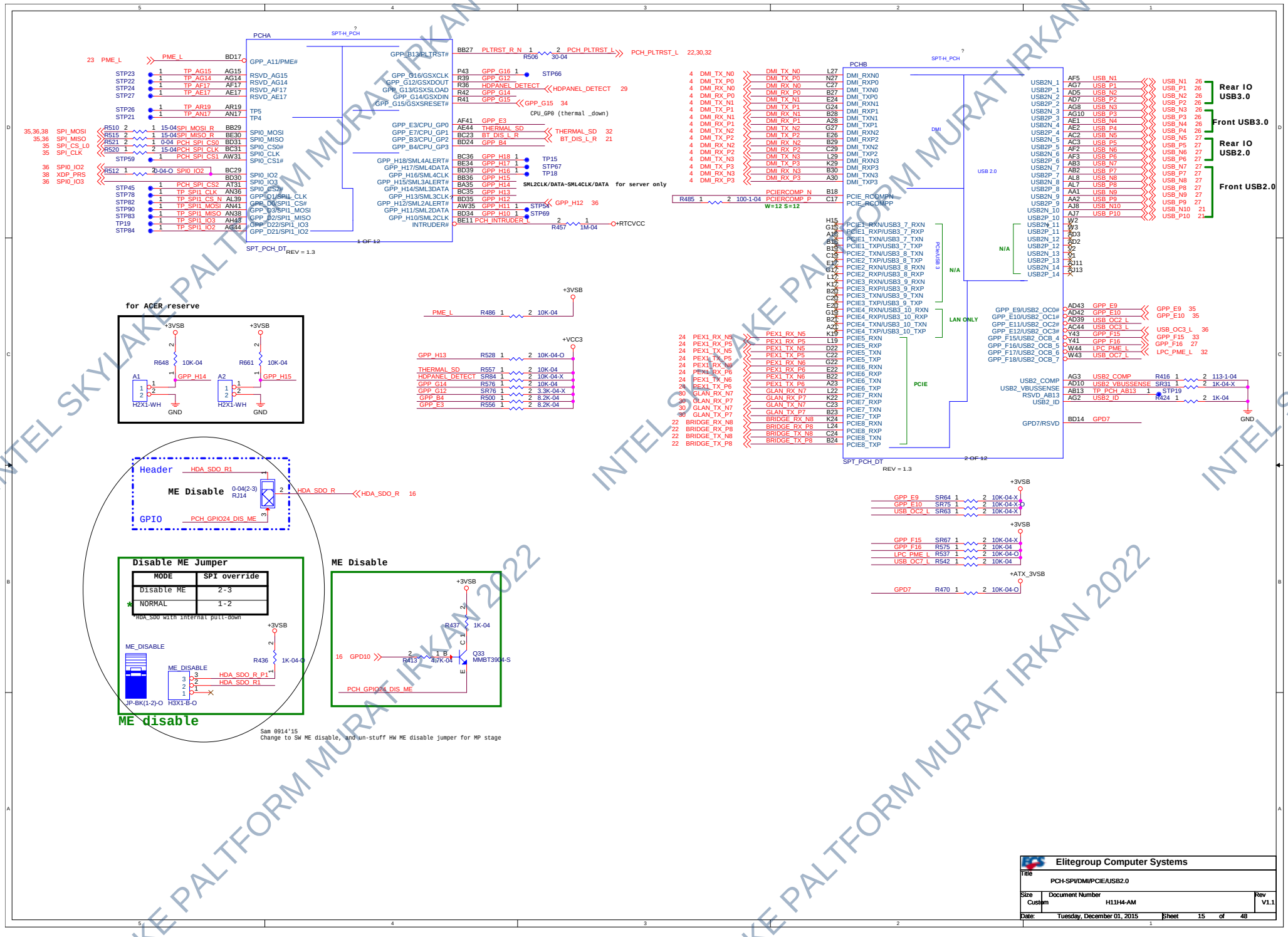
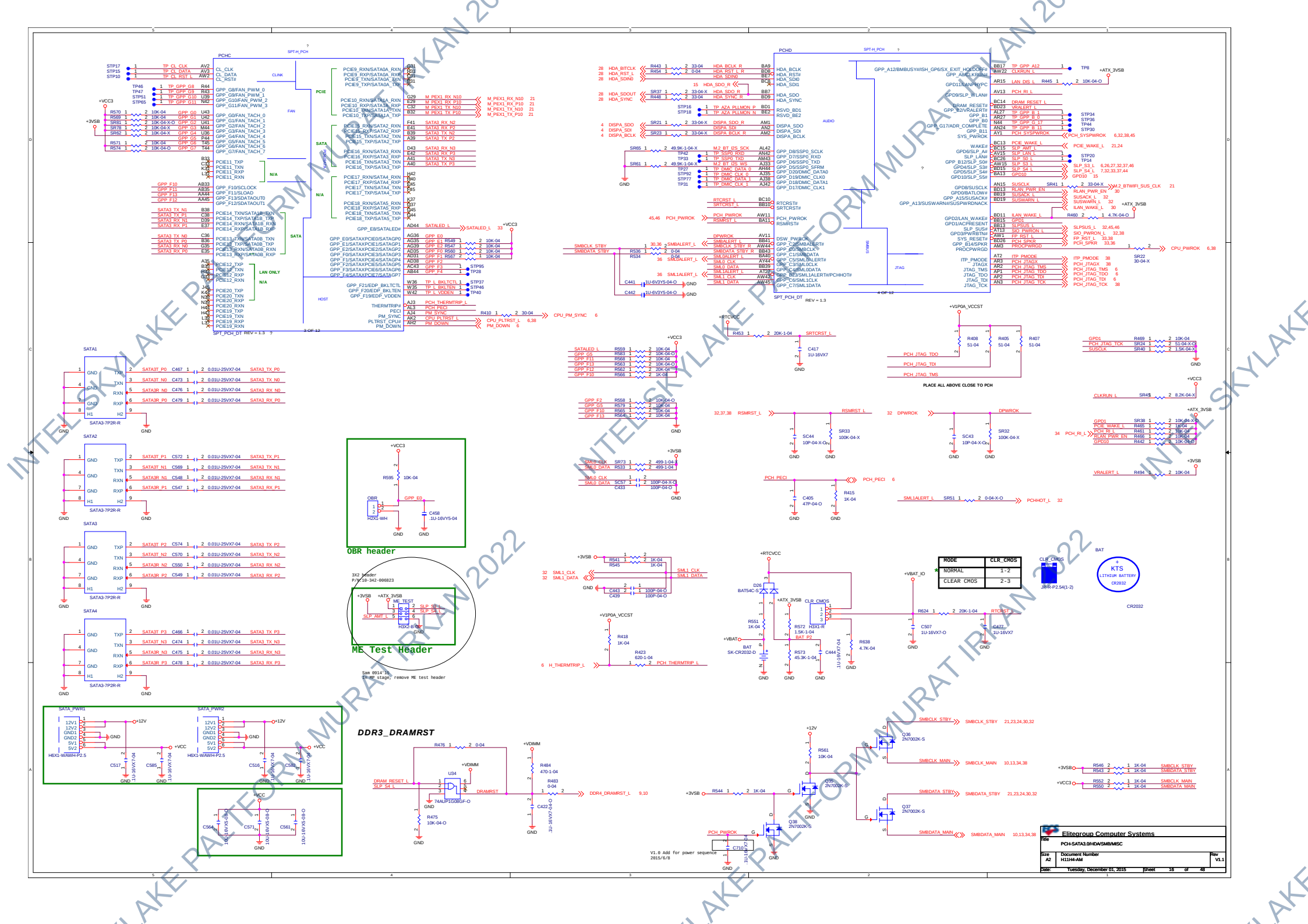
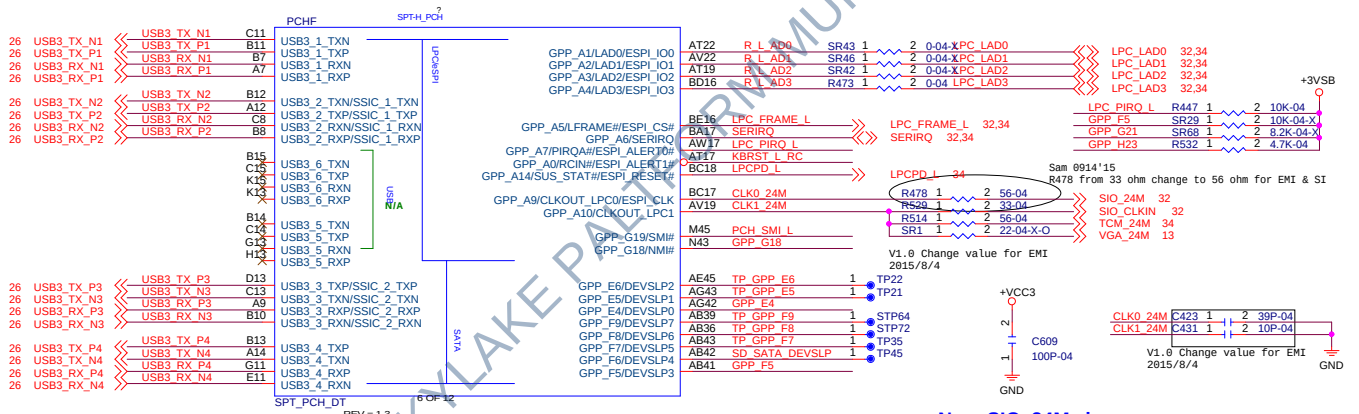
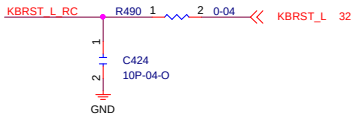


INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

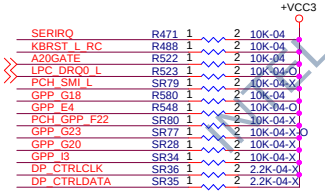

PCHC
PCHD
SATA1
SATA2
SATA3
SATA4
OBR header
ME Test Header
DDR3_DRAMRST
Elitegroup Computer Systems
PCH-SATA3.0/HDA/SMB/MISC
Document Number H11H4-AM
Tuesday, December 01, 2015

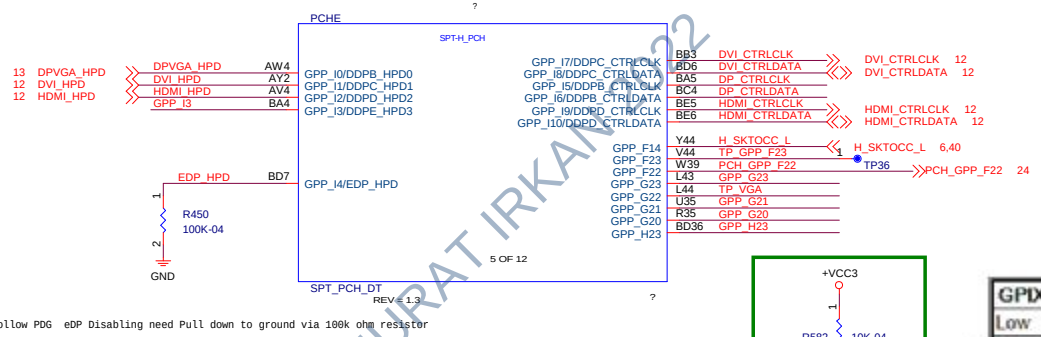
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022



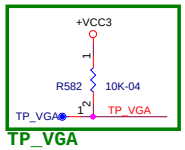


Near SIO_24M via





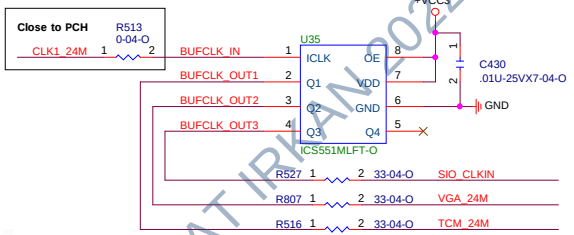
follow PDG eDP Disabling need Pull down to ground via 100k ohm resistor



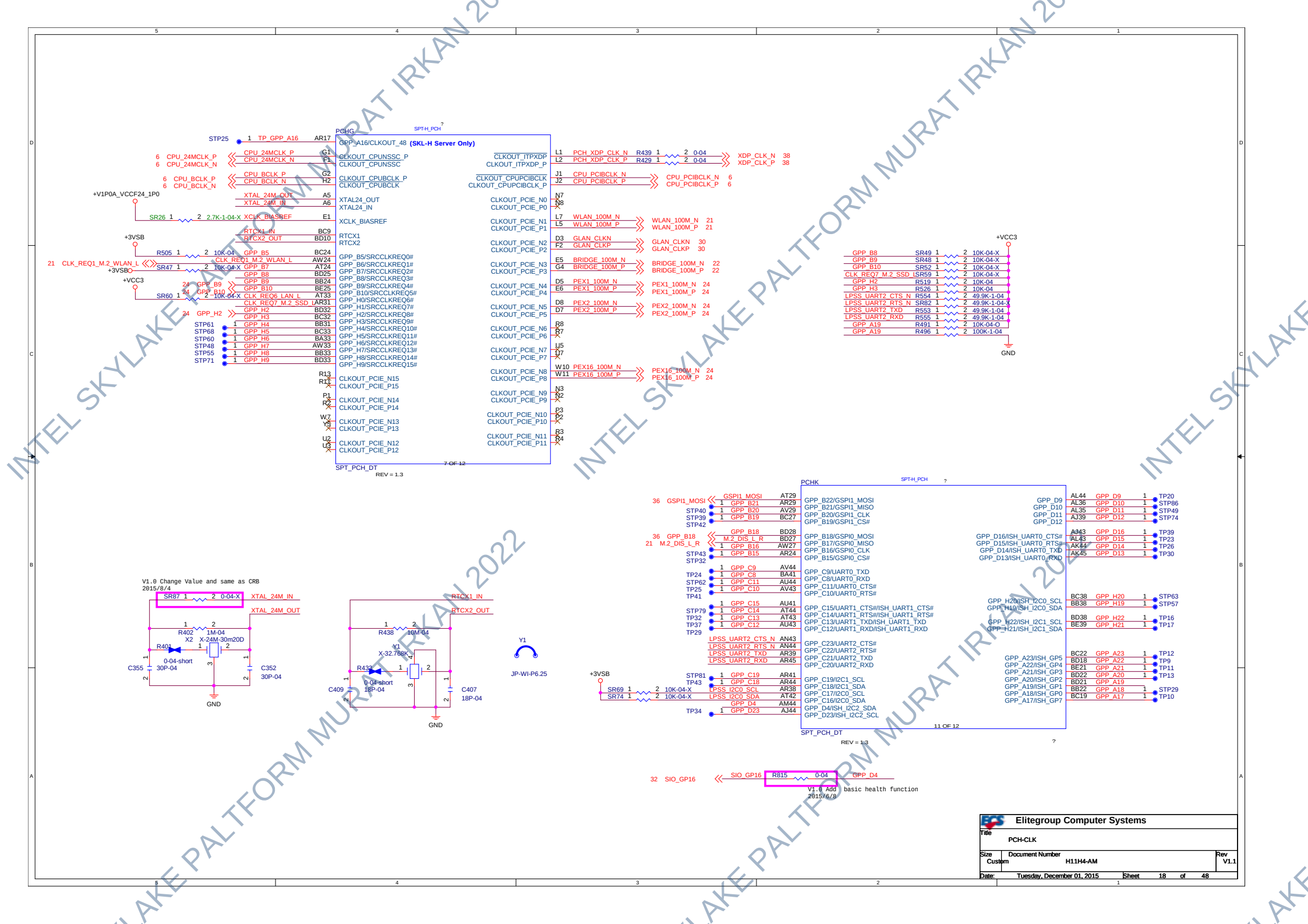
TP_VGA

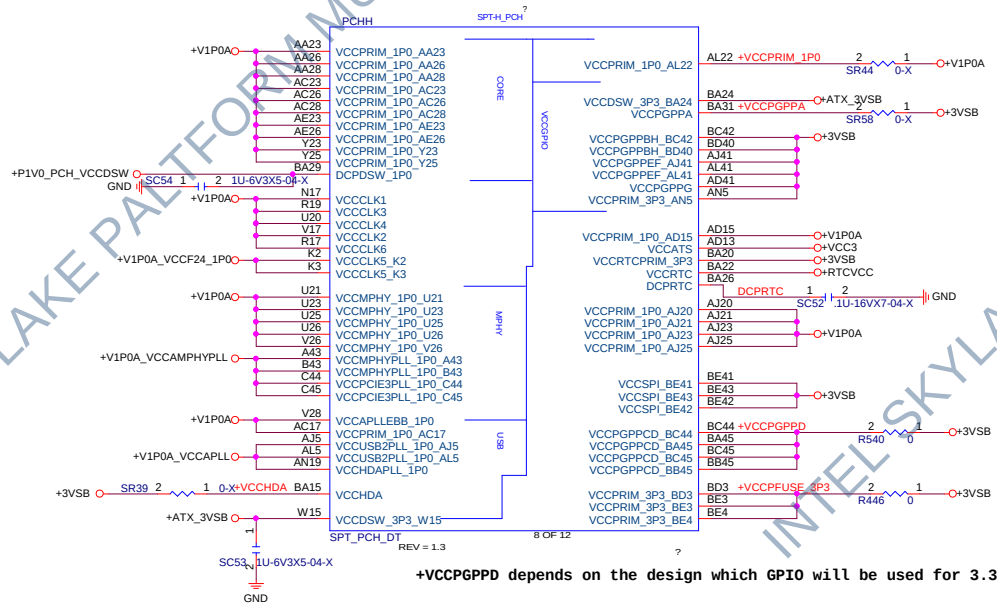
GPIXX	Display Type
Low	onboard VGA
* High	default BIOS

CLOCK BUFFER

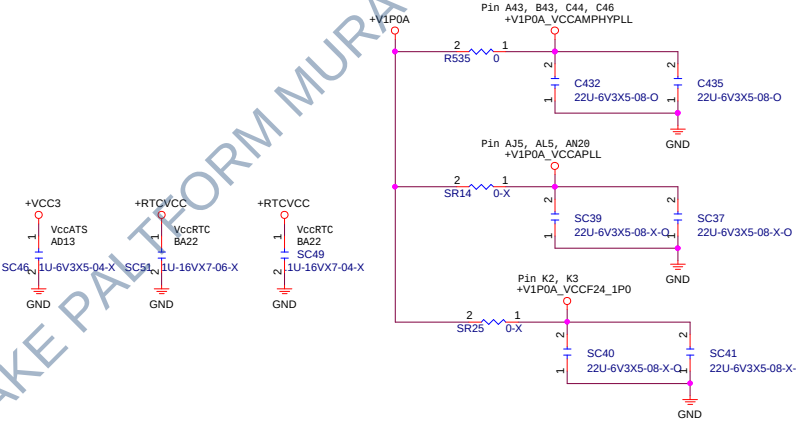


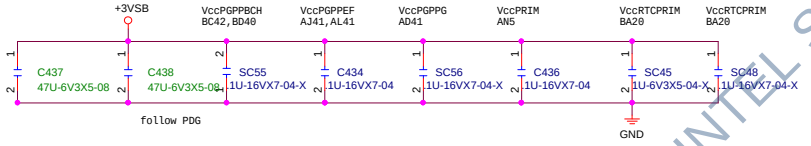
Elitegroup Computer Systems	
Title	PCH-USB3.0/LPC
Size: Custom	Document Number: H11H4-AM
Rev	V1.1
Date: Tuesday, December 01, 2015	Sheet 17 of 48

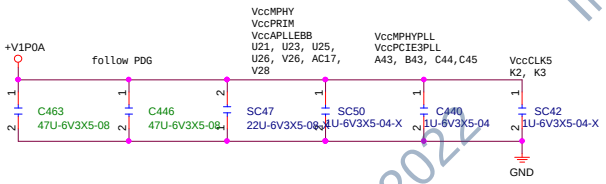

PCHG
SPT-H_PCH
GPP_A16/CLKOUT_48 (SKL-H Server Only)
SPT_PCH_DT
REV = 1.3
7 OF 12
PCHK
SPT_PCH_DT
REV = 1.3
11 OF 12
V1.0 Change Value and same as CRB
2015/8/4
V1.0 Add basic health function
2015/6/8
Elitegroup Computer Systems
PCH-CLK
H11H4-AM
V1.1
Tuesday, December 01, 2015
Sheet 18 of 48

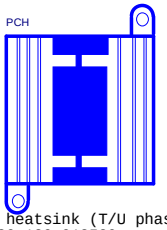


+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.





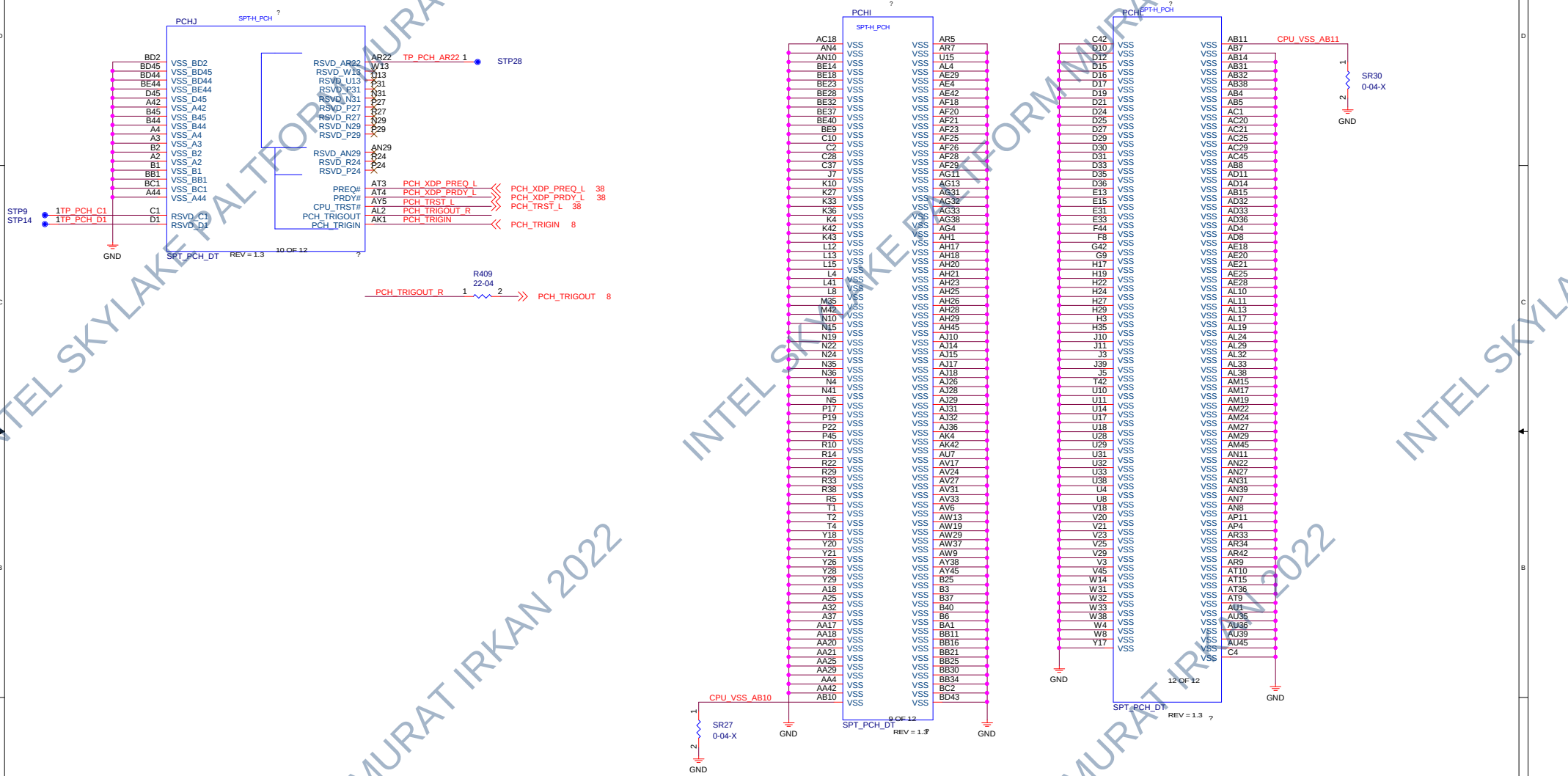




PCH heatsink (T/U phase)
P/N20-120-013580
20-120-013581
V1.0 Change
2015/6/8

Elitegroup Computer Systems			
Title: PCH-PWR			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 19 of 48		

INTEL SKYLAKE PALTFORM MURAT IRKAN 2022



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

Elitegroup Computer Systems		
Title: PCH-GND		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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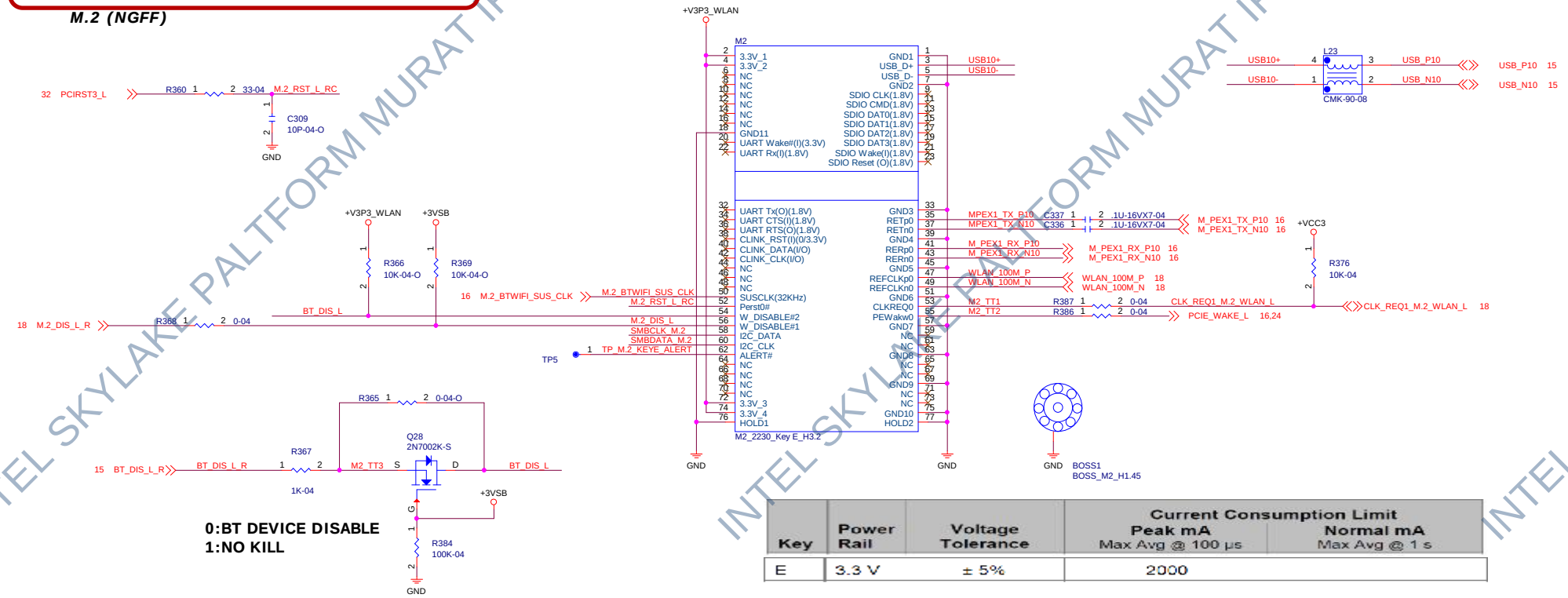
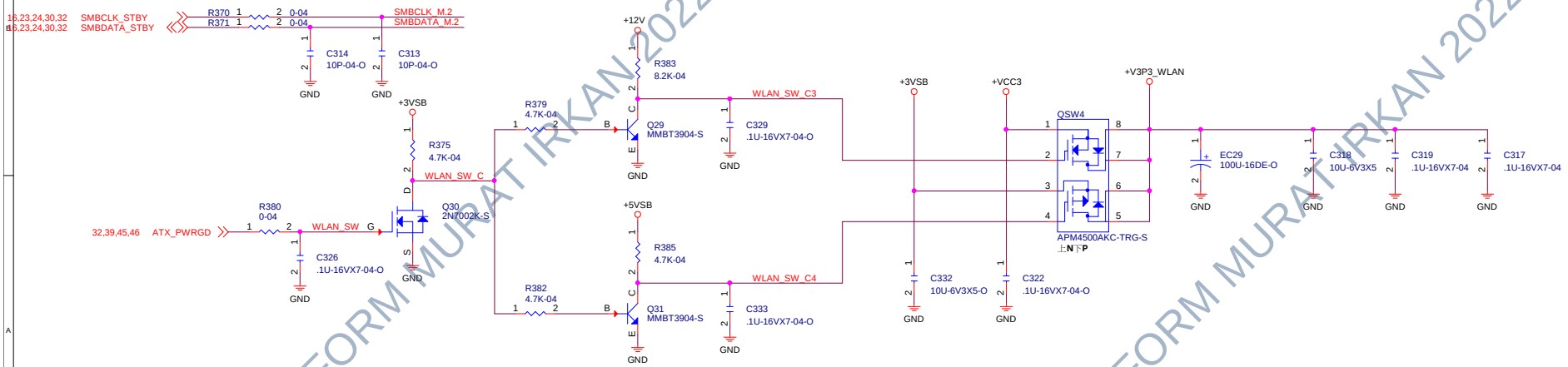
INTEL LGA1151 SOKET M.2 SSD DISK

M.2 (NGFF)



0:BT DEVICE DISABLE
1:NO KILL

Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak mA Max Avg @ 100 µs	Current Consumption Limit Normal mA Max Avg @ 1 s
E	3.3 V	± 5%	2000	



	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB

Elitegroup Computer Systems	
Title	M.2 Slot
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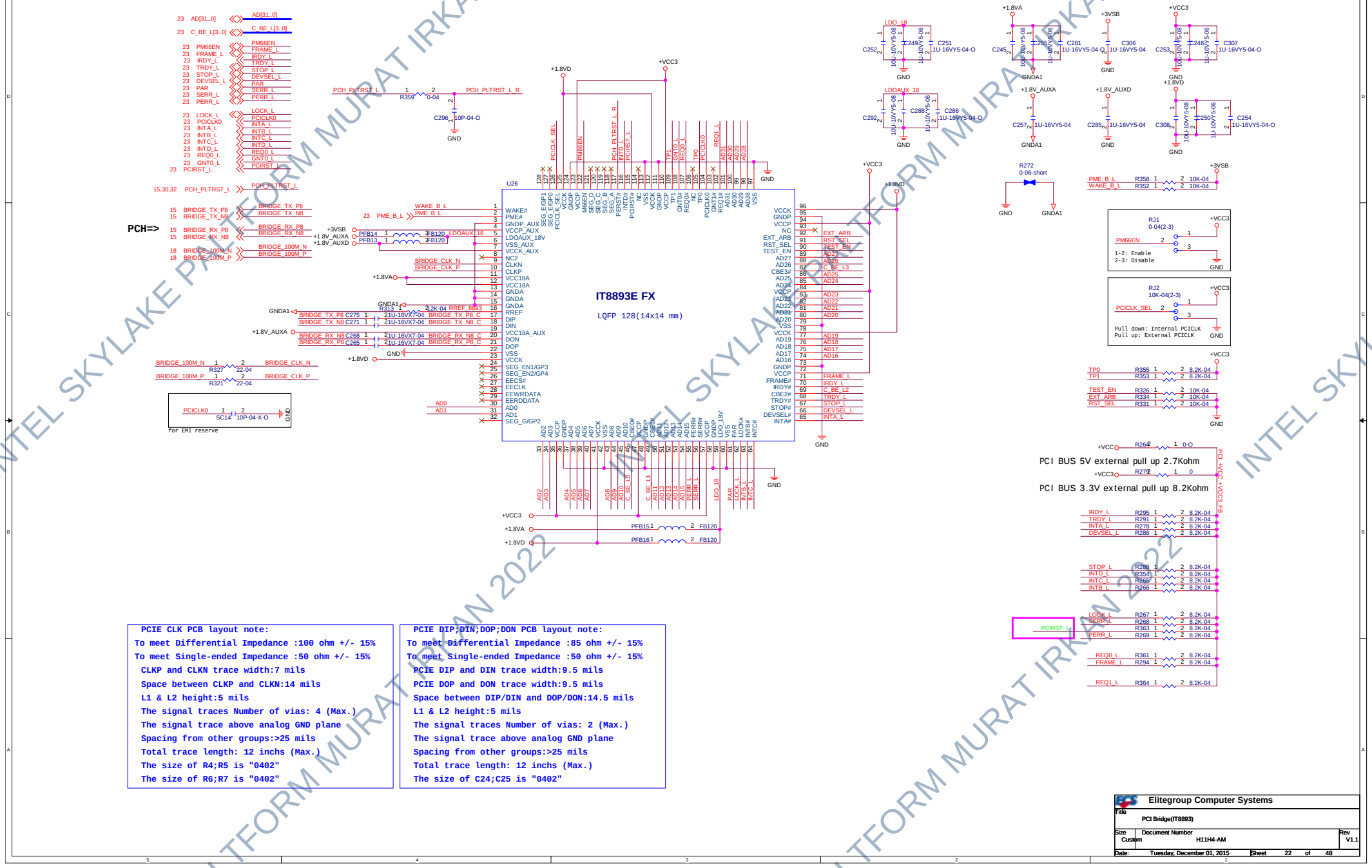
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022


PCH=>
IT8893E FX
LQFP 128(14x14 mm)
U26
PCH_PLTRST_L
PCH_PLTRST_L_R
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C24;C25 is "0402"
PCI BUS 5V external pull up 2.7Kohm
PCI BUS 3.3V external pull up 8.2Kohm
Elitegroup Computer Systems
PCI Bridge(IT8893)
H11H4-AM
Tuesday, December 01, 2015
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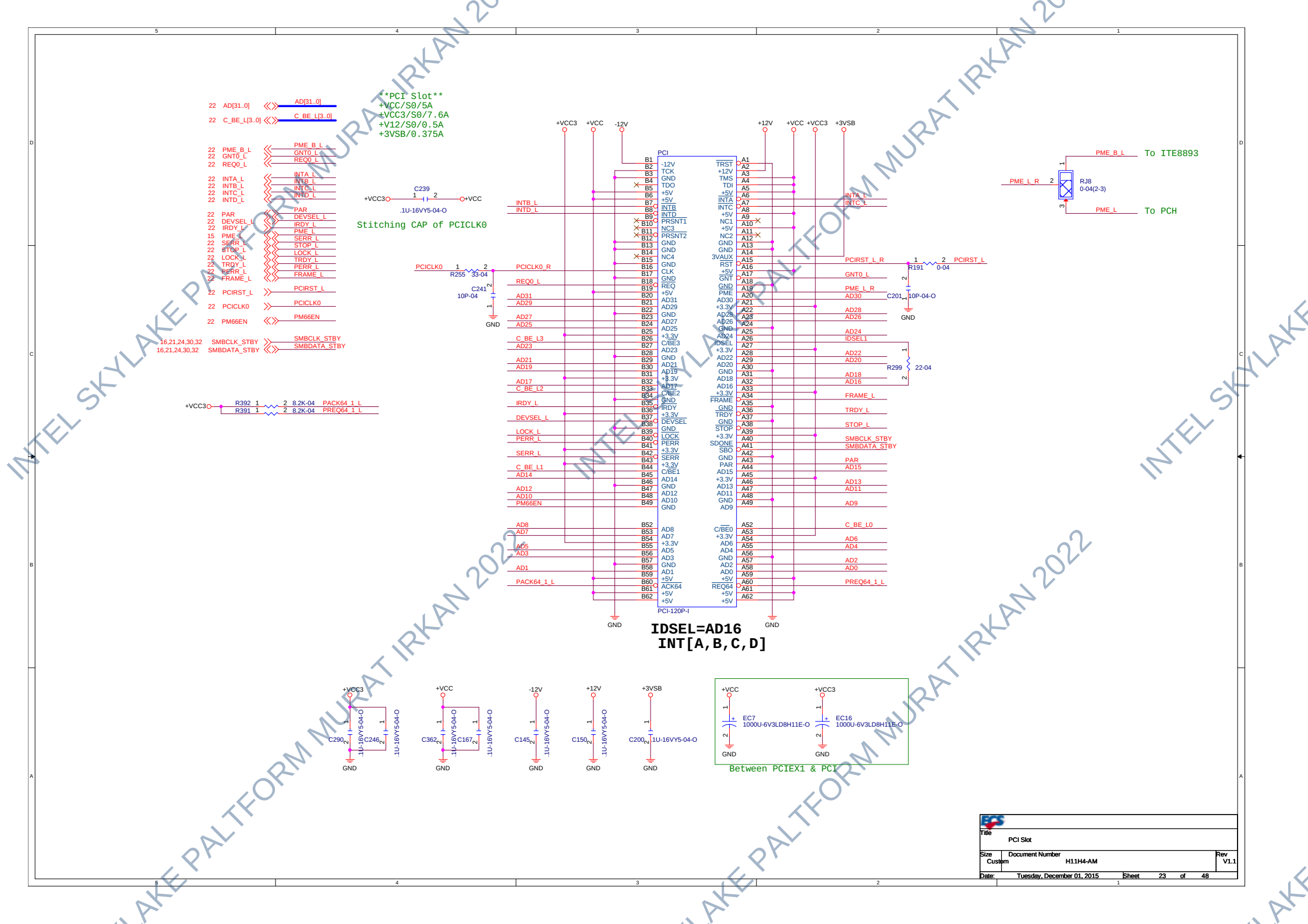
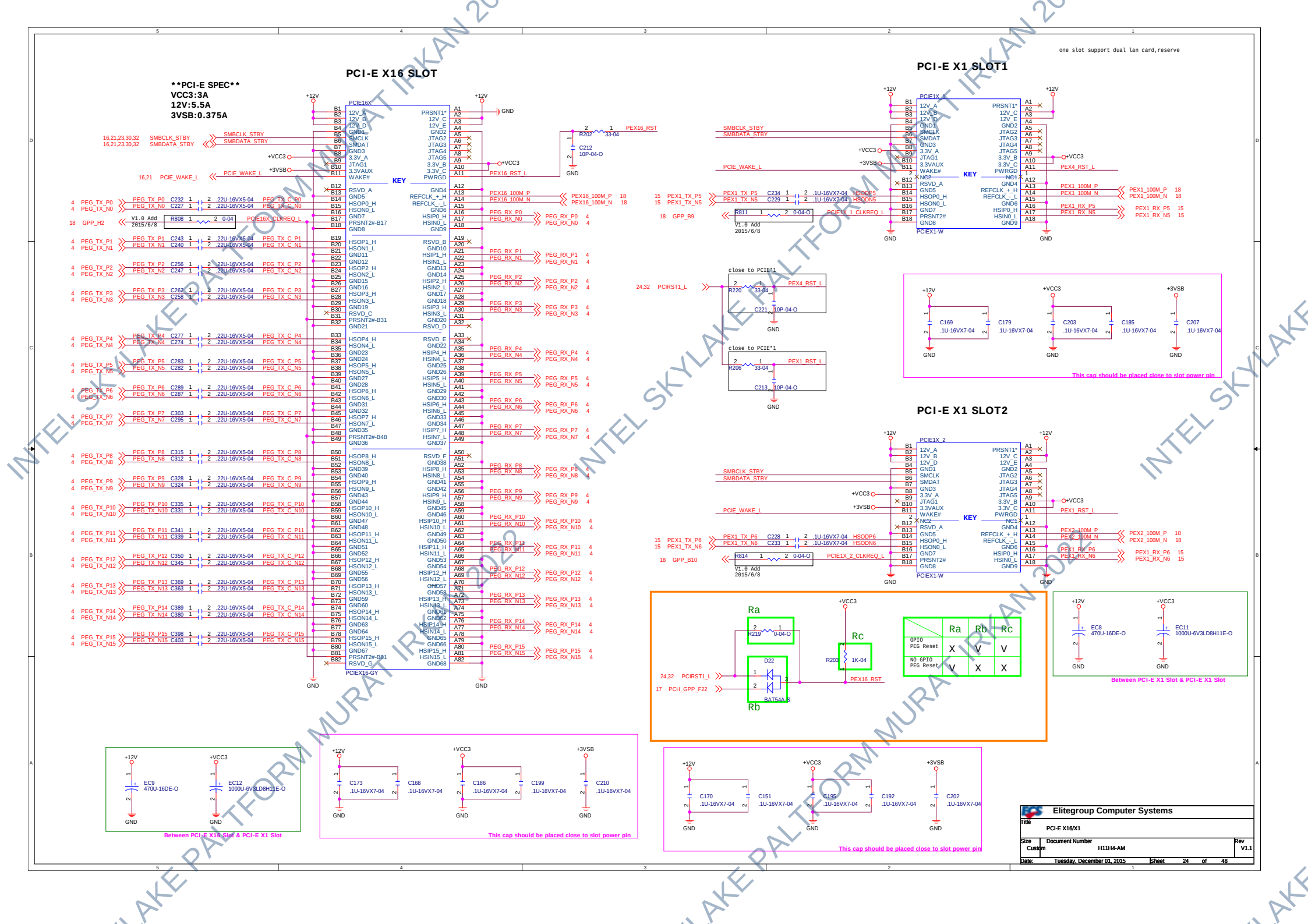
48



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022


PCI-E X16 SLOT
PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A
PCIE16X
PCIEX16-GY
KEY
PCI-E X1 SLOT1
PCIE1X_1
PCIEX1-W
PCI-E X1 SLOT2
PCIE1X_2
one slot support dual lan card,reserve
close to PCIE*1
Ra
Rb
Rc
GPIO PEG Reset
NO GPIO PEG Reset
Between PCI-E X16 Slot & PCI-E X1 Slot
Between PCI-E X1 Slot & PCI-E X1 Slot
This cap should be placed close to slot power pin
Elitegroup Computer Systems
PCI-E X16/X1
H11H4-AM
V1.1
Tuesday, December 01, 2015
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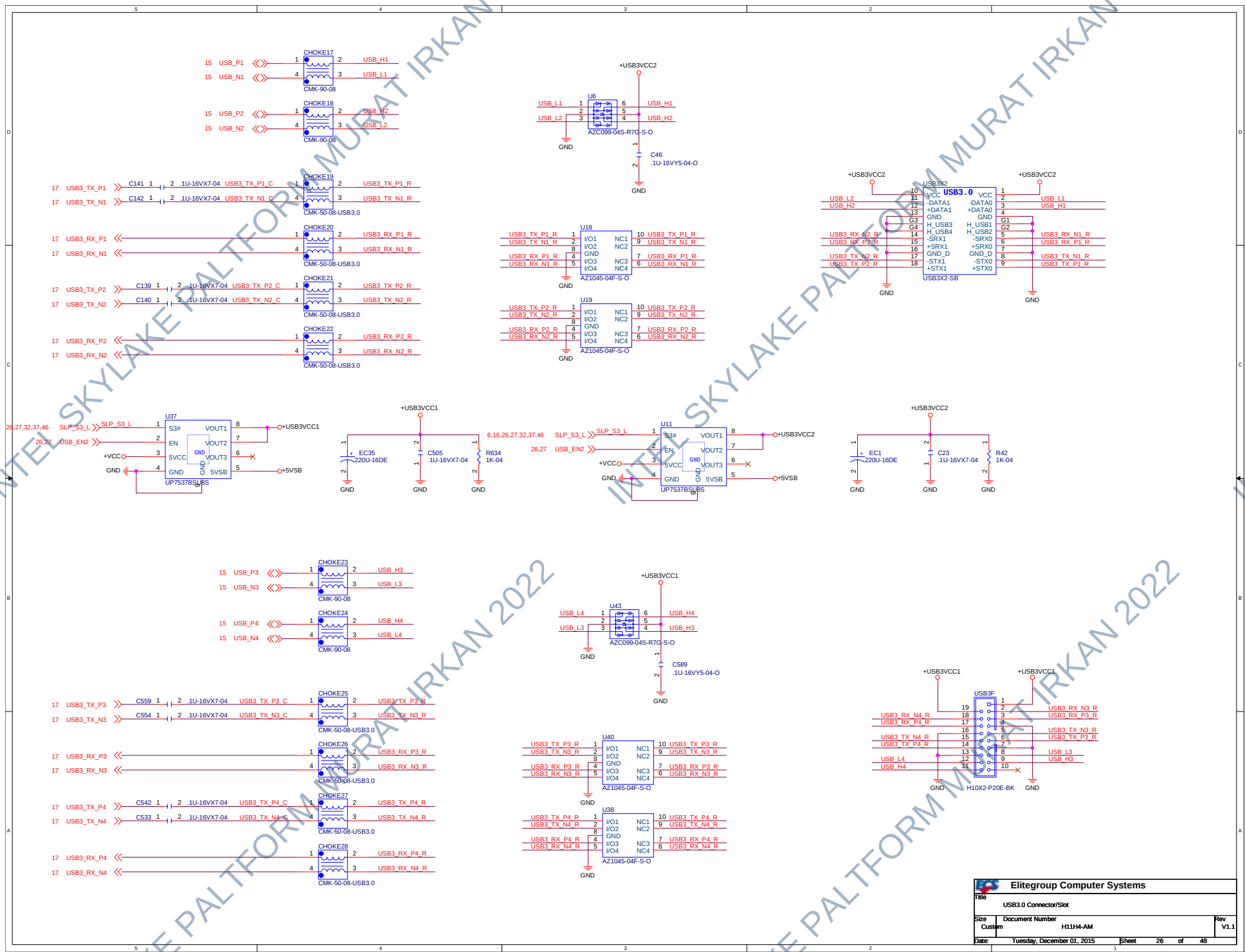
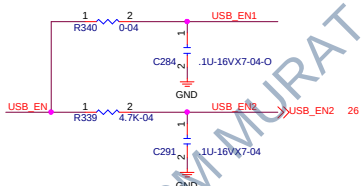
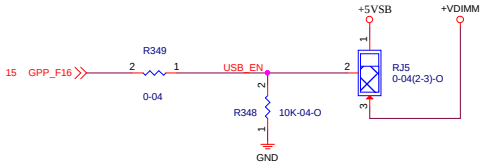
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

Title	Reserved		
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 25 of 48		

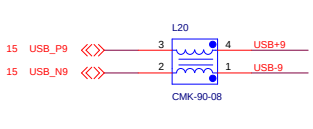


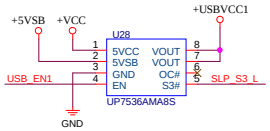
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

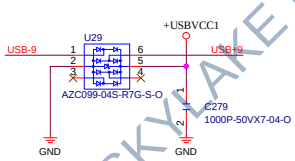


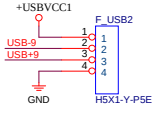


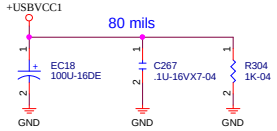
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

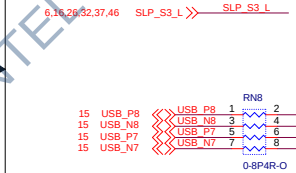


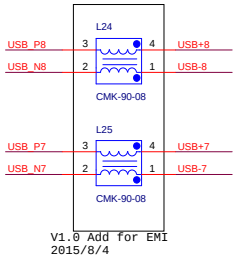


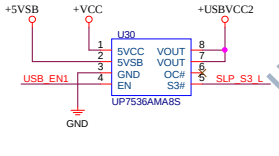


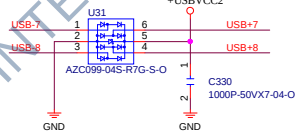


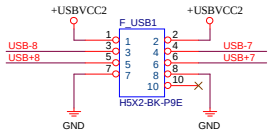


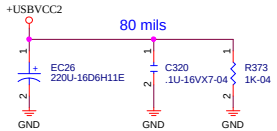






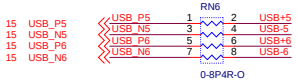


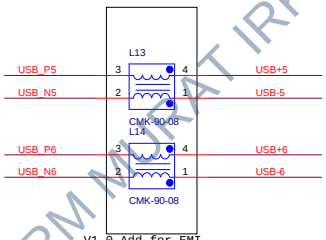


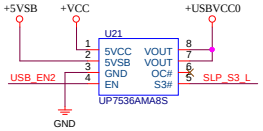


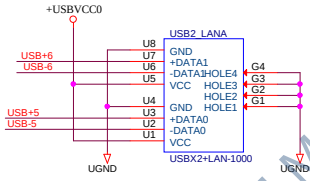
USB2.0 header

USB2.0 connecter

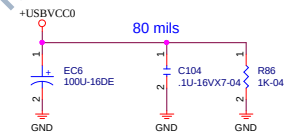


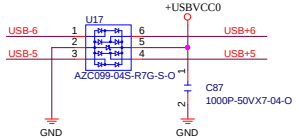






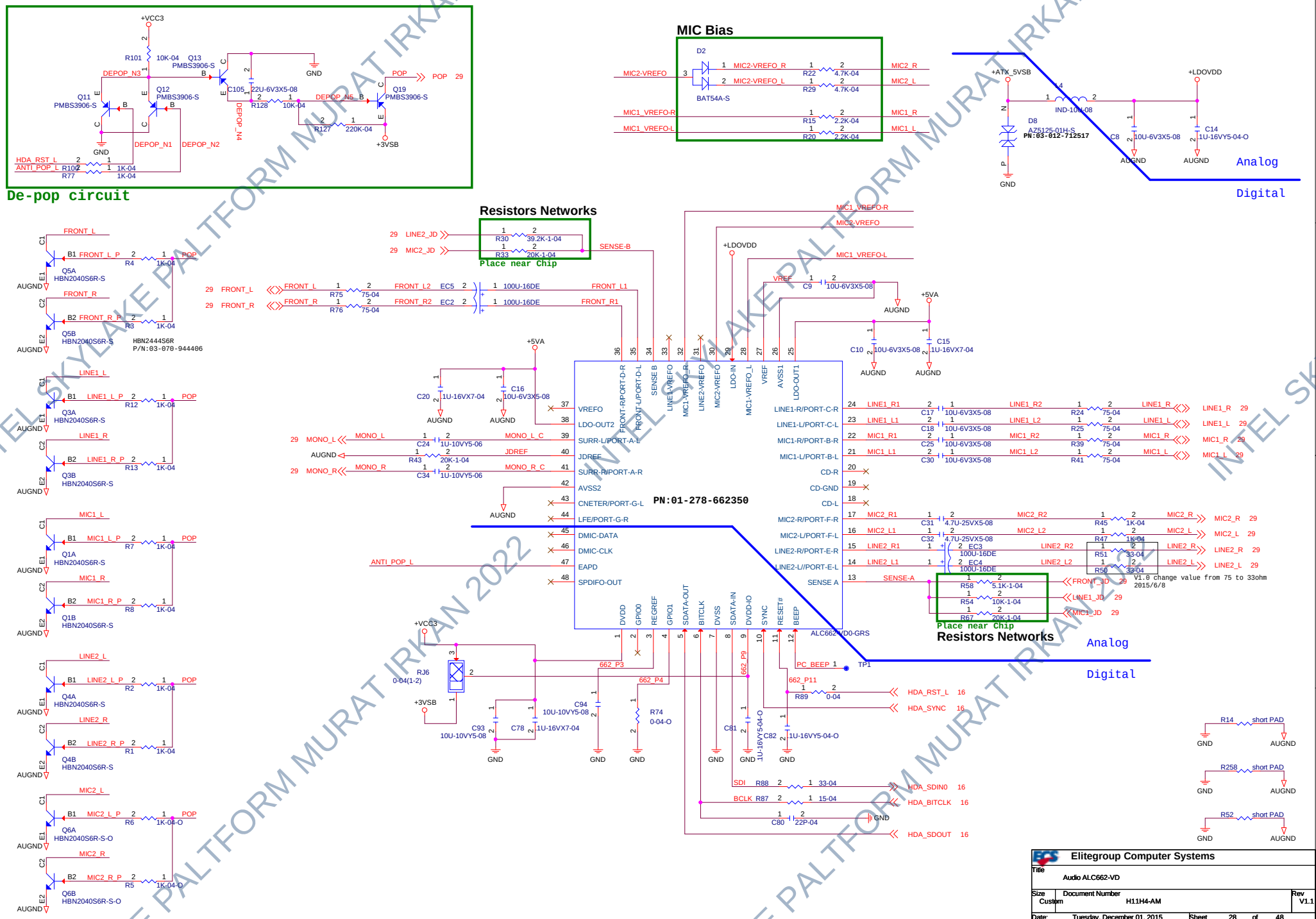
Lan + USB2.0



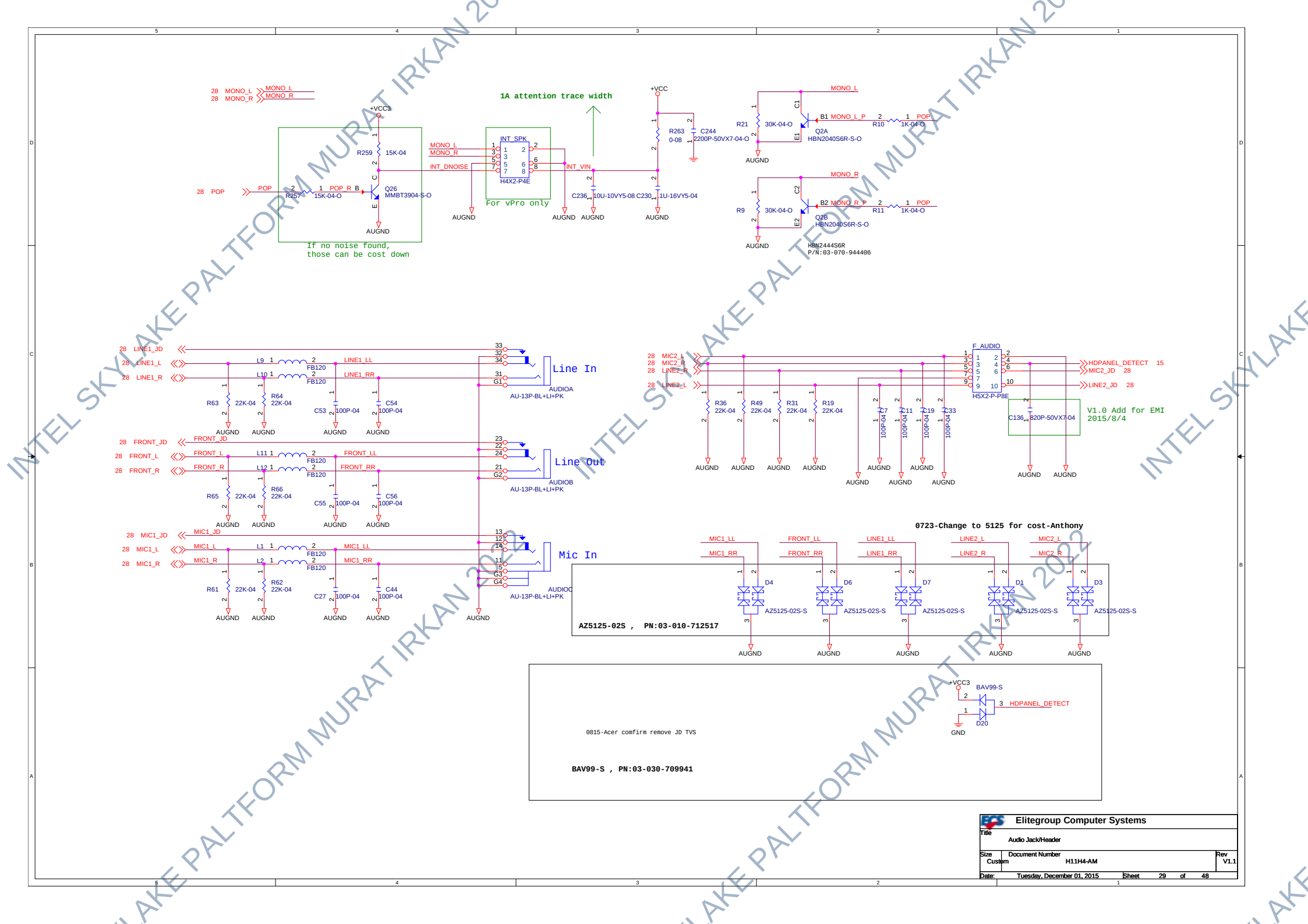


Elitegroup Computer Systems	
Title	USB2.0 Connector/Header
Size: Custom	Document Number: H11H4-AM
Rev	V1.1
Date: Tuesday, December 01, 2015	Sheet 27 of 48

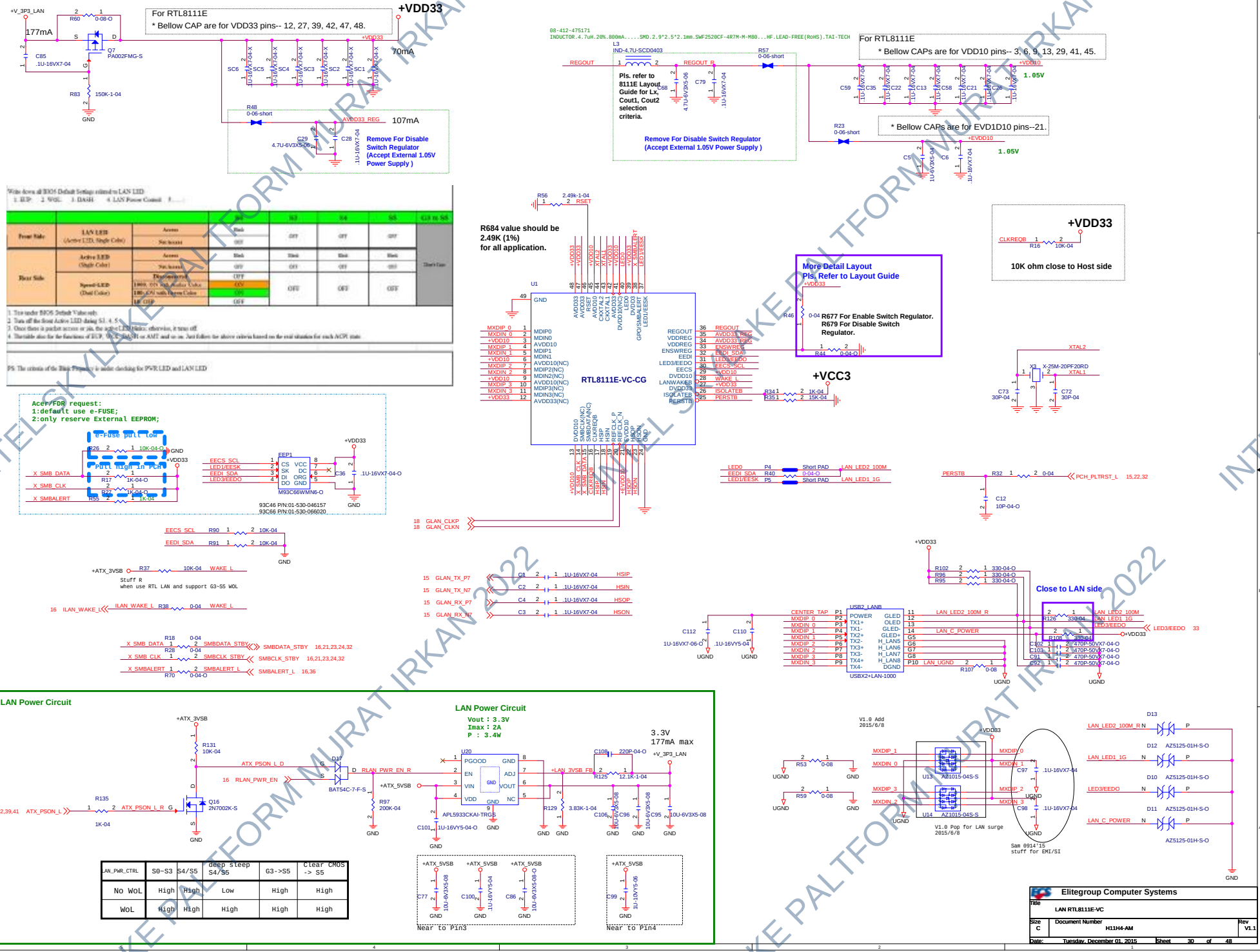
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

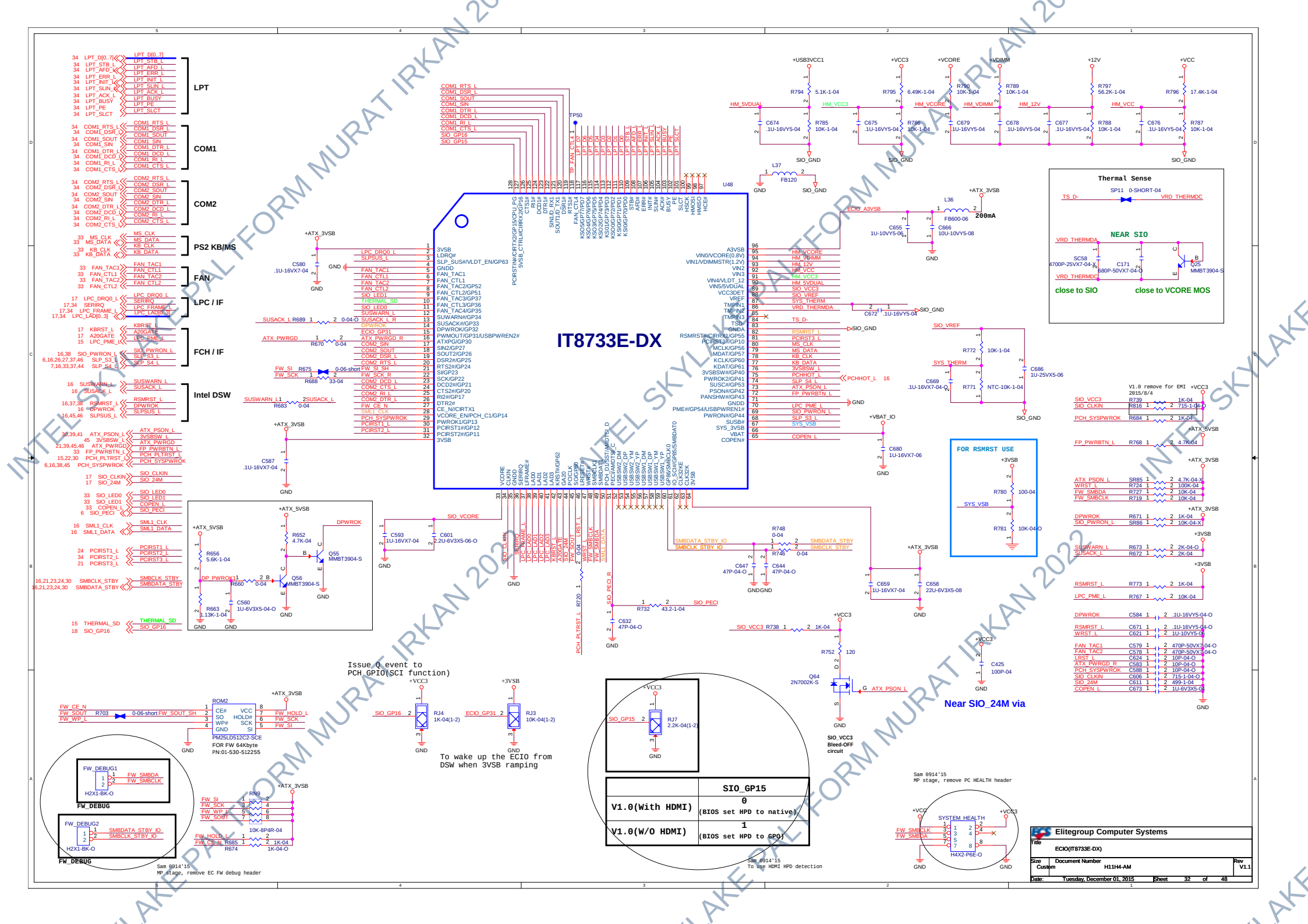


LAN_PWR_CTRL	S0~S3	S4/S5	deep sleep S4/S5	G3->S5	Clear CMOS -> S5
No WoL	High	High	Low	High	High
WoL	High	High	High	High	High

INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

Elitegroup Computer Systems		
Title: Reserved		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 31 of 48	


IT8733E-DX
LPT
COM1
COM2
PS2 KB/MS
FAN
LPC / IF
FCH / IF
Intel DSW
Thermal Sense
NEAR SIO
close to SIO
close to VCORE MOS
FOR RSMRST USE
Near SIO_24M via
Issue Q event to
PCH_GPIO(SCI function)
To wake up the ECIO from
DSW when 3VSB ramping
FW_DEBUG
FW_DEBUG
SIO_VCC3
Bleed-OFF
circuit
SIO_GP15
V1.0(With HDMI)
0
(BIOS set HPD to native)
V1.0(W/O HDMI)
1
(BIOS set HPD to GPO)
Elitegroup Computer Systems
ECIO(IT8733E-DX)
H11H4-AM
V1.1
Tuesday, December 01, 2015
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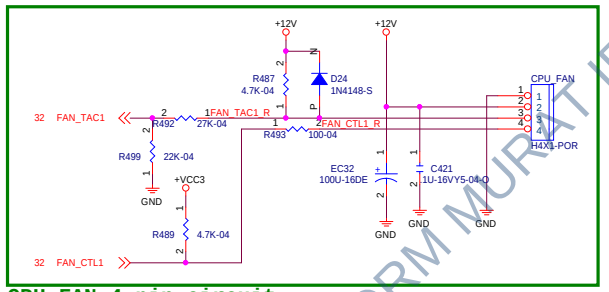
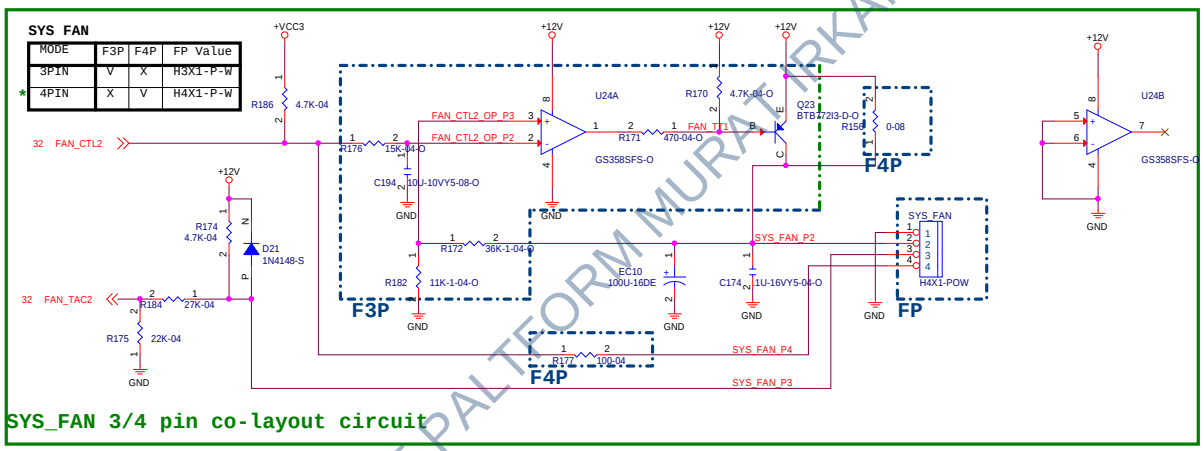
48



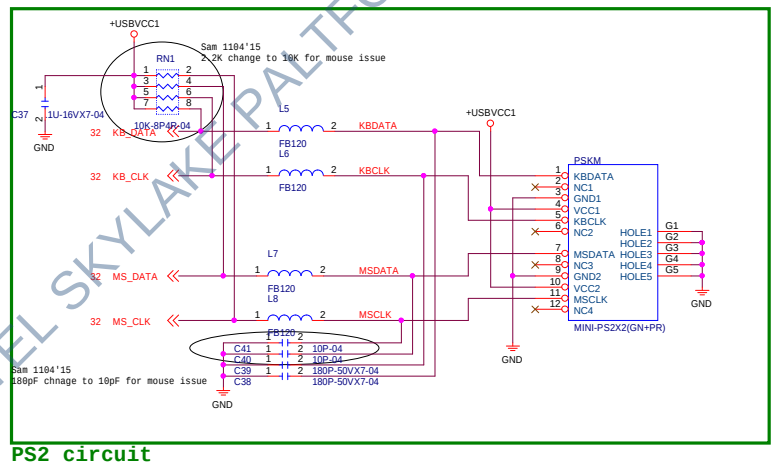
CPU_FAN 4 pin circuit

SYS FAN

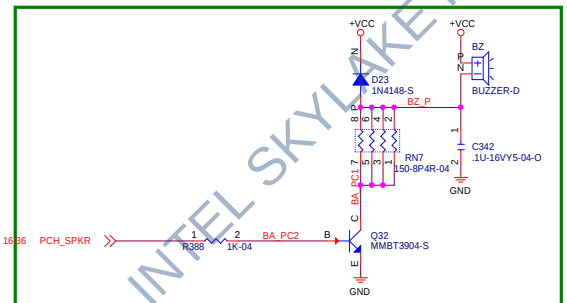
MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
* 4PIN	X	V	H4X1-P-W



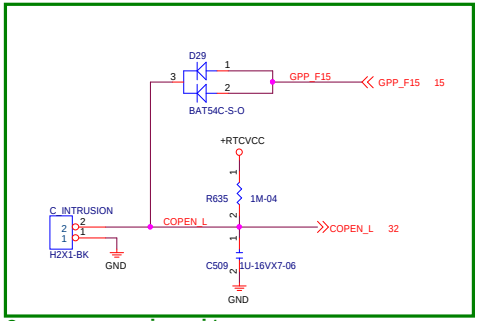
SYS_FAN 3/4 pin co-layout circuit



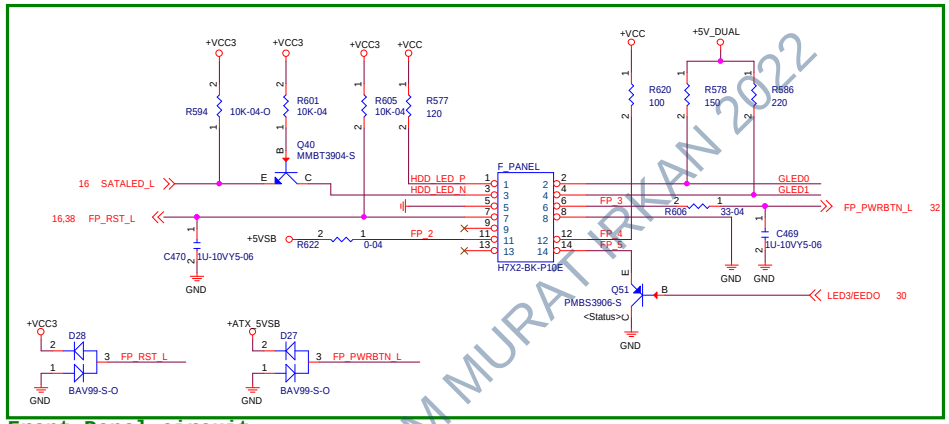
PS2 circuit



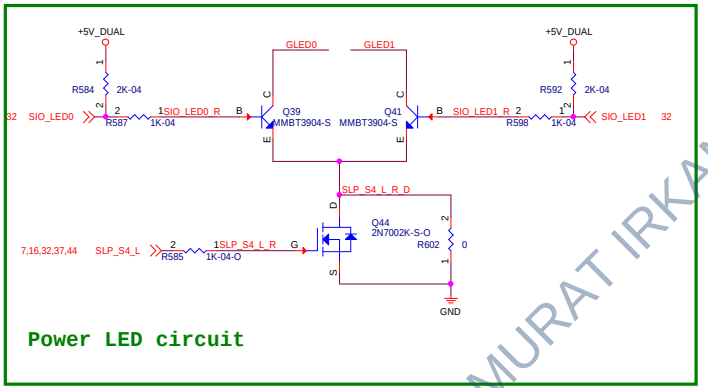
Buzzer circuit



Case open circuit



Front Panel circuit



Power LED circuit

Elitegroup Computer Systems			
Title: FAN/Buzzer/PS2/Front Panel			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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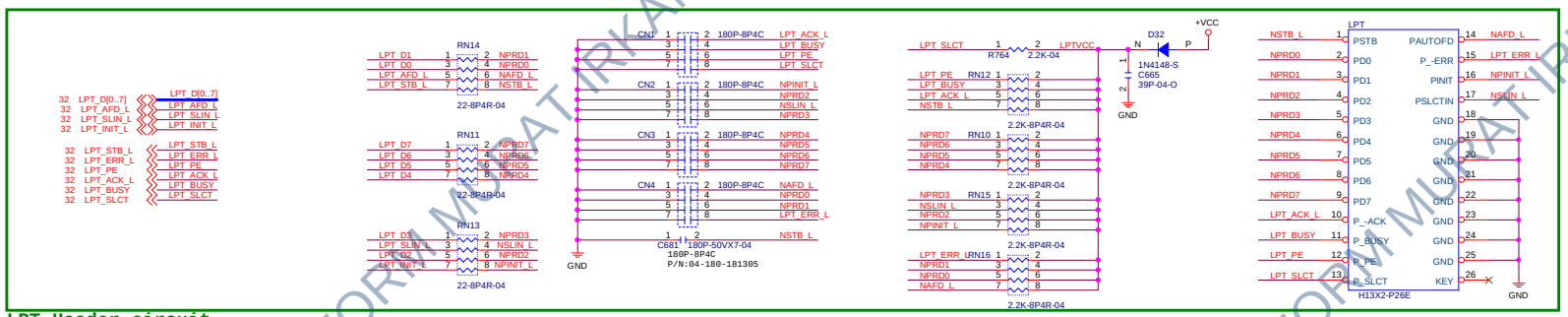

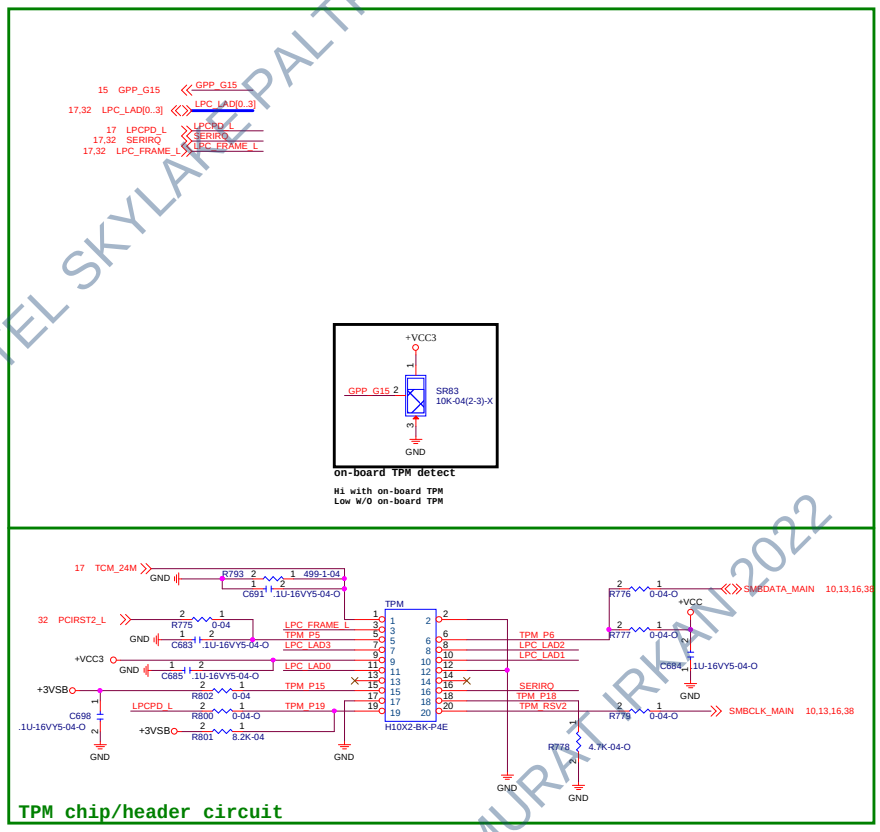

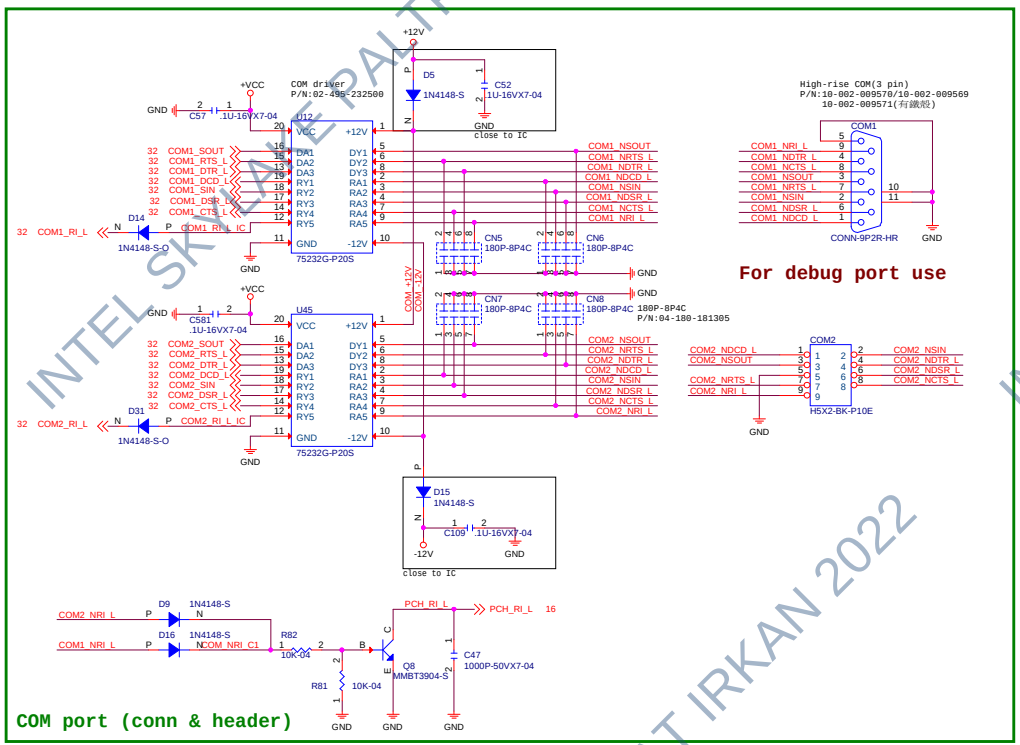

Elitegroup Computer Systems		
Title: TPM/TCM/LPT/COM/Asset ID		
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15,36,38 SPI_MOSI
15,36 SPI_MISO
SPI_MOSI R474 2 1 0-04 SPI_MOSI0
SPI_MISO R451 2 1 0-04 SPI_MISO0

15 SPI_CLK
SPI_CLK R455 2 1 0-04 SPI_CLK0

15 SPI_CS_L0
SPI_CS_L0 1 R463 2 0-04 ROM_CS_L0
Re

Sam 0914'15
In MP stage, remove SPI debug header

SPI_MOSI0 C419 1 2 12P-04-O GND
SPI_MISO0 C418 1 2 12P-04-O
ROM_CS_L0 C414 1 2 12P-04-O
C420 12P-04-O

SPIROM1
ROM_CS_L0 1 CS# VCC 8
SPI_MISO0 2 SO HOLD# 7
SPI_IO2_0 3 WP# SCK 6
4 GND SI 5
SPI-64M-WINBOND
GND
+SPI_3P3V
SPI_IO3_0
SPI_CLK0
SPI_MOSI0
C426 2 10U-10VY5-08 C427 2 1U-16VX7-04
GND GND
close
ROM1

SPI_IO3_0 R462 2 1 1K-04 +SPI_3P3V
SPI_IO2_0 R472 2 1 0-04 SPI_WP

+3VSB +SPI_3P3V
R501 short PAD
D25 1 2 3
BAT54C-S-O

A3 stuff BAT54C for debug and reserve 0 ohm
A4 0 ohm change to SH

SPI ROM

BIOS_WP JP-R(2-3)
BIOS_WP 1 2 3 H3X1-R
GPP_E9 15
GND

BIOS WP Jumper:

MODE	WP
BIOS WP	1-2
* NORMAL	2-3

+SPI_3P3V
R495 2 1 10K-04
SPI_WP
R504 2 1 0-04
Q34 E B C PMBS3906-S-O
<Status>
GPP_E10 15
GND

BIOS WP

Sam 0914'15
In MP stage, remove SPI debug header

Ra
Rc
Rb
Rd
Re

SPI_MISO0 R456 2 1 0-04-O
SPI_DEBUG
ROM_CS_L0
SPI_CS_L0
SPI_MISO0_R
SPI_WP
+SPI_3P3V
SPI_IO3_0_R
SPI_CLK0
SPI_MOSI0_R
H6X2-BK-P2E-P1.27-O
GND
6*2 SMD header
PN:10-382-012820

Rb
R458 2 1 0-04-O SPI_IO3_0
R449 2 1 0-04-O SPI_MOSI0

Rd
SPI_DEBUG
JP-P1.27(1-3)-O
1.27mm jumper
PN:10-611-002144

	Ra	Rb	Rc	Rd	Re
A3~A5	0	0	0	0	X
MP	X	X	X	X	0

Title	SPI ROM		
Size B	Document Number H11H4-AM		Rev V1.1
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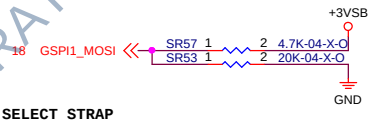
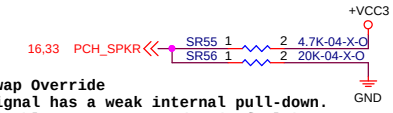
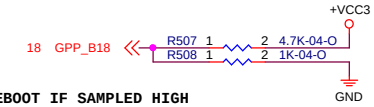


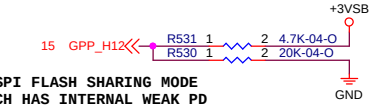
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



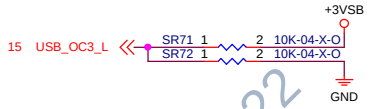
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



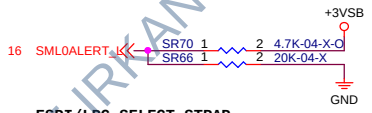
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING



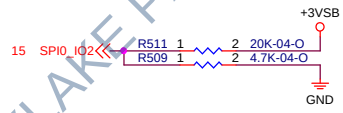
DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



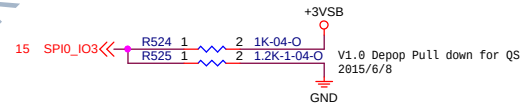
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

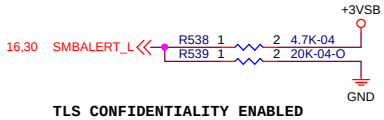
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



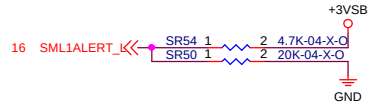
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1/ES2 only)



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD



EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

Title: Strap Pin		
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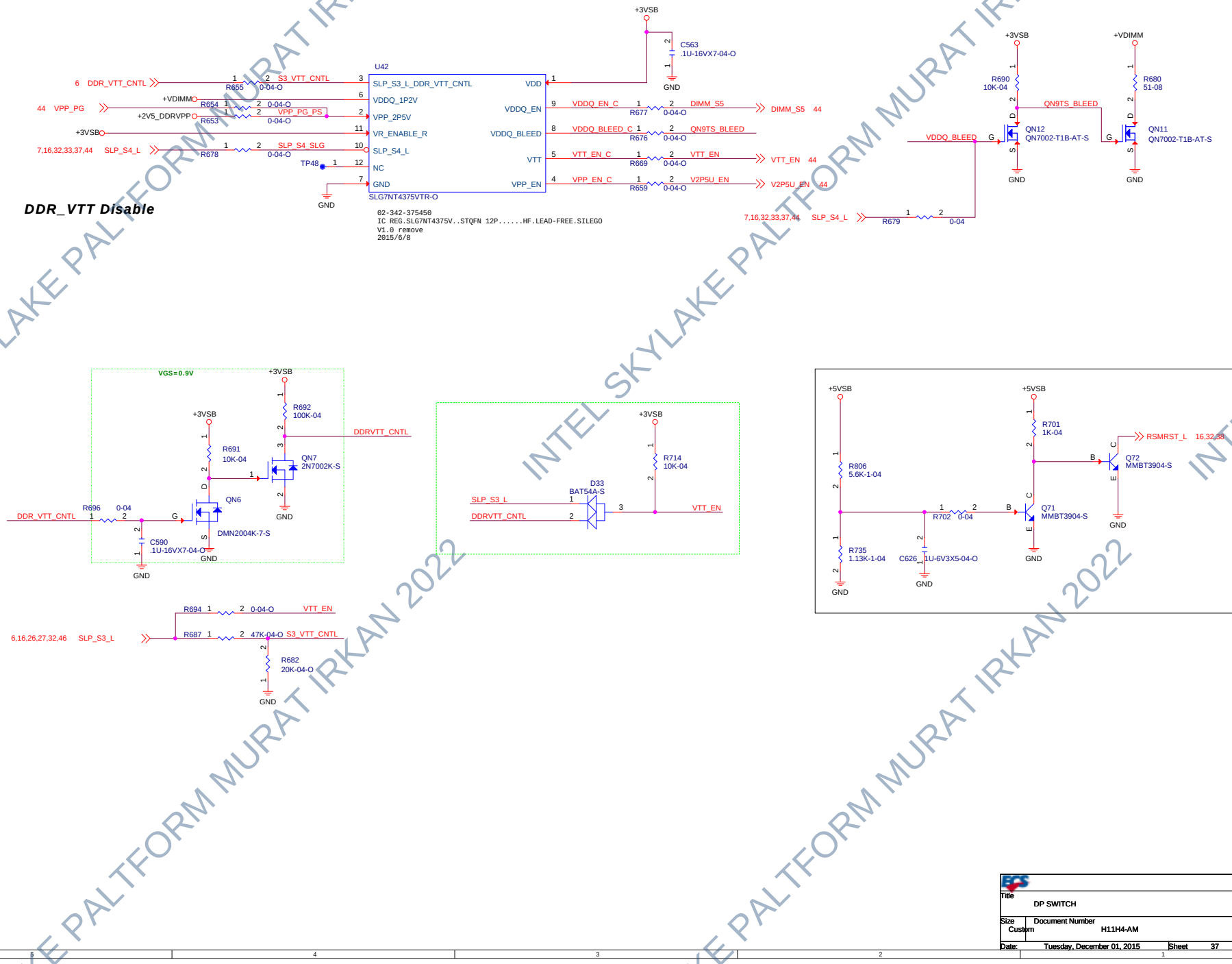
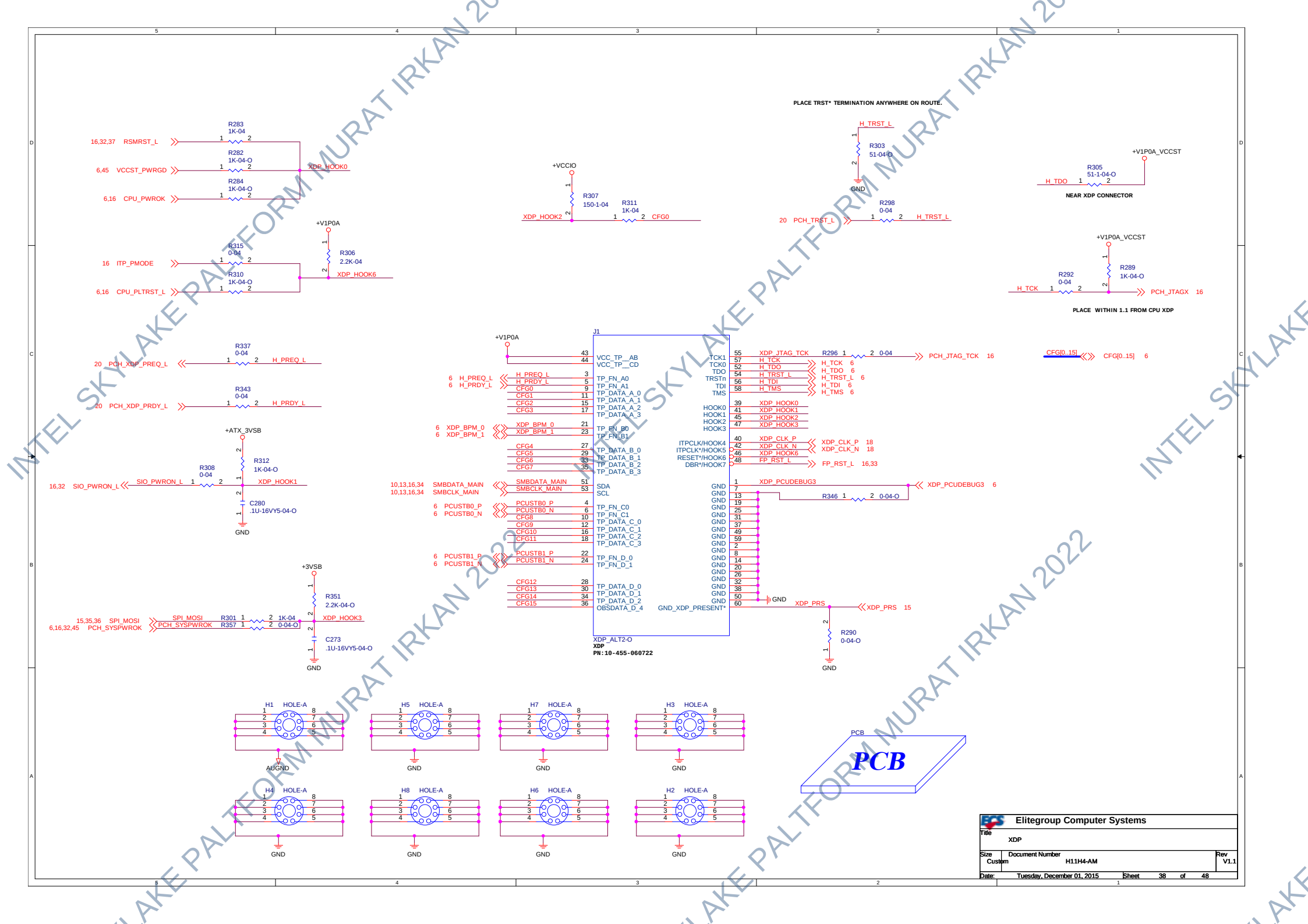


Title	DP SWITCH	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
Date: Tuesday, December 01, 2015	Sheet 37 of 48	

INTEL SKYLAKE PALTFORM MURAT IRKAN 2022


PLACE TRST* TERMINATION ANYWHERE ON ROUTE.
NEAR XDP CONNECTOR
PLACE WITHIN 1.1 FROM CPU XDP
J1
XDP_ALT2-O
XDP
PN:10-455-060722
PCB
PCB
Elitegroup Computer Systems
Title
XDP
Size
Custom
Document Number
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V1.1
Date:
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38
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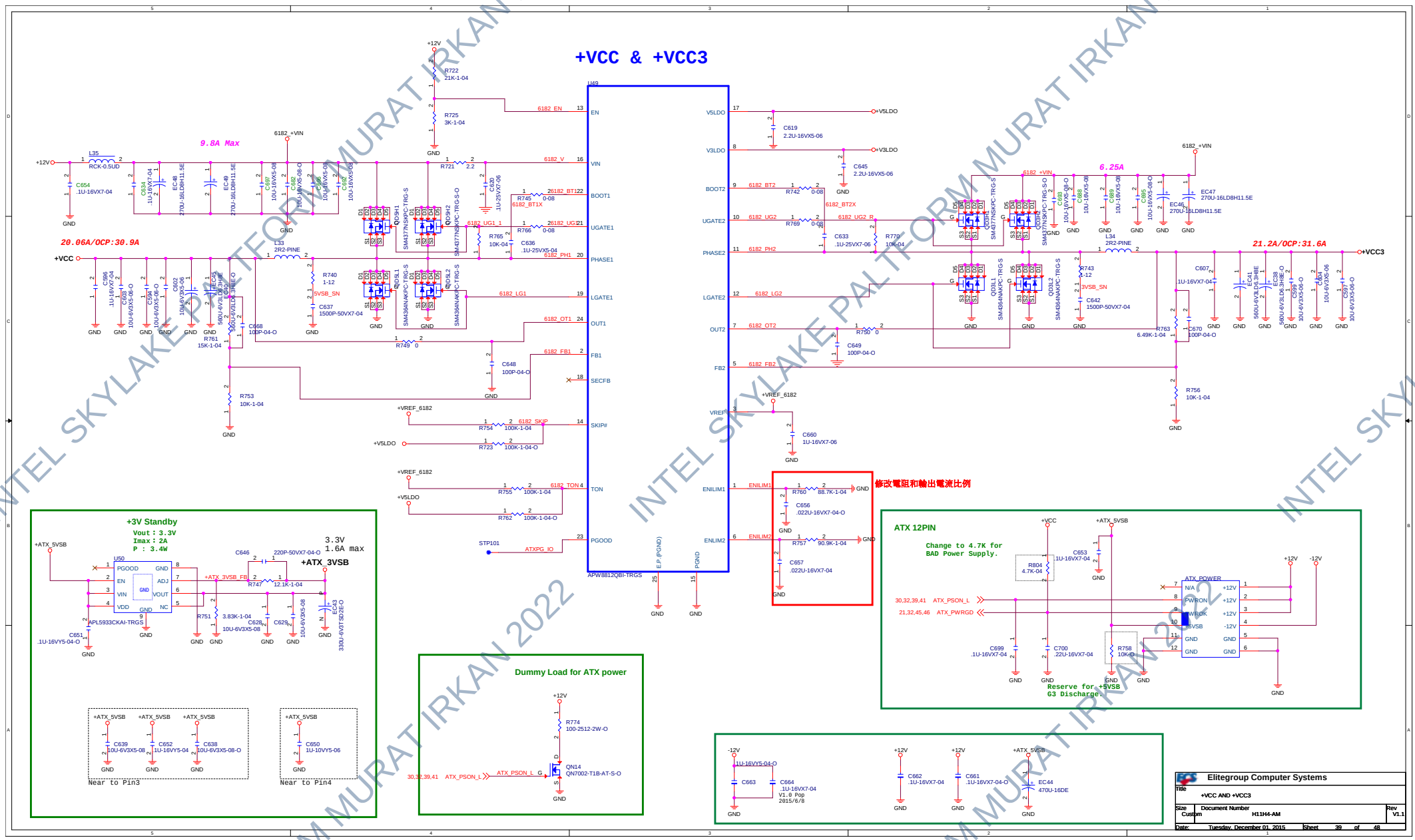
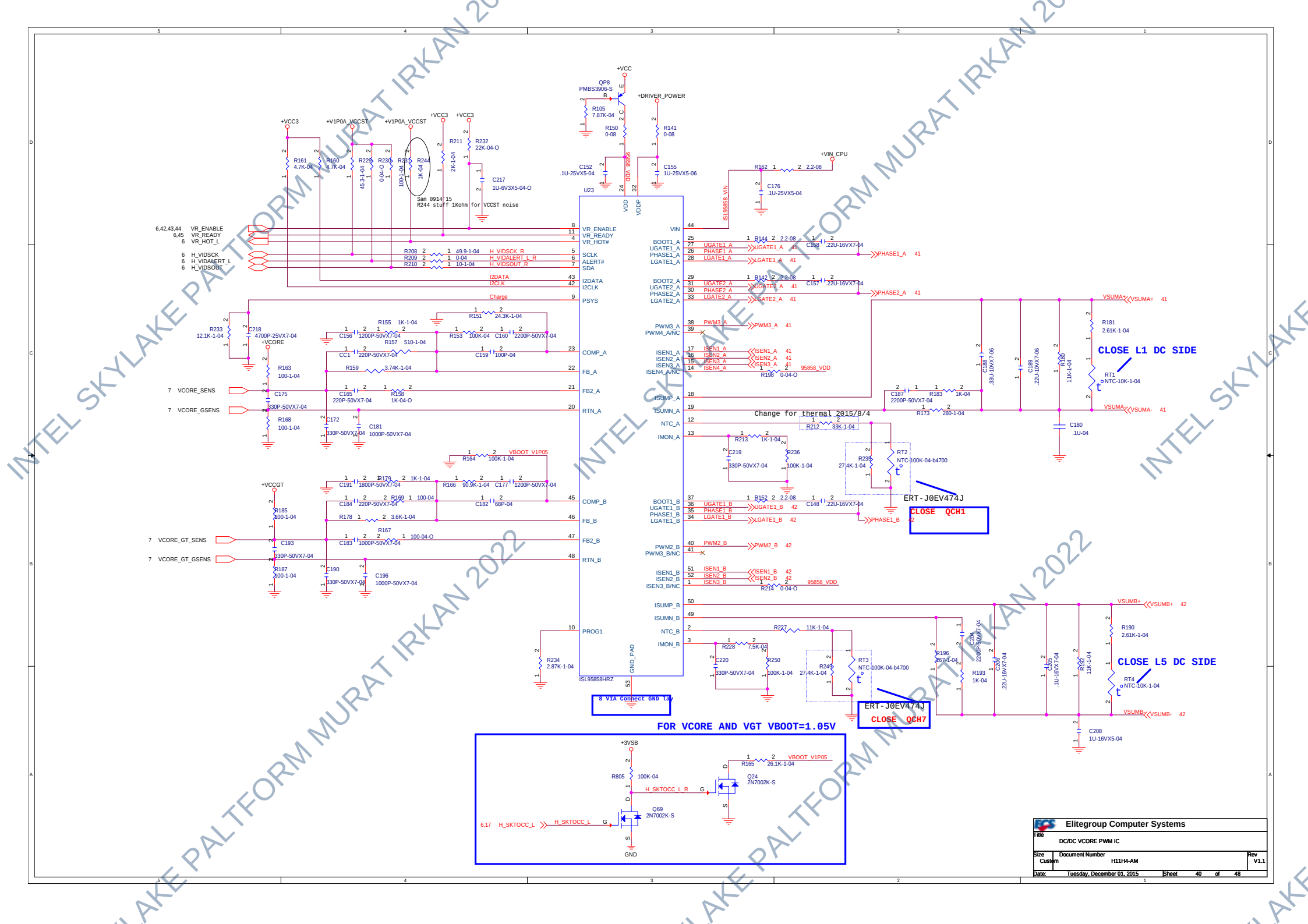
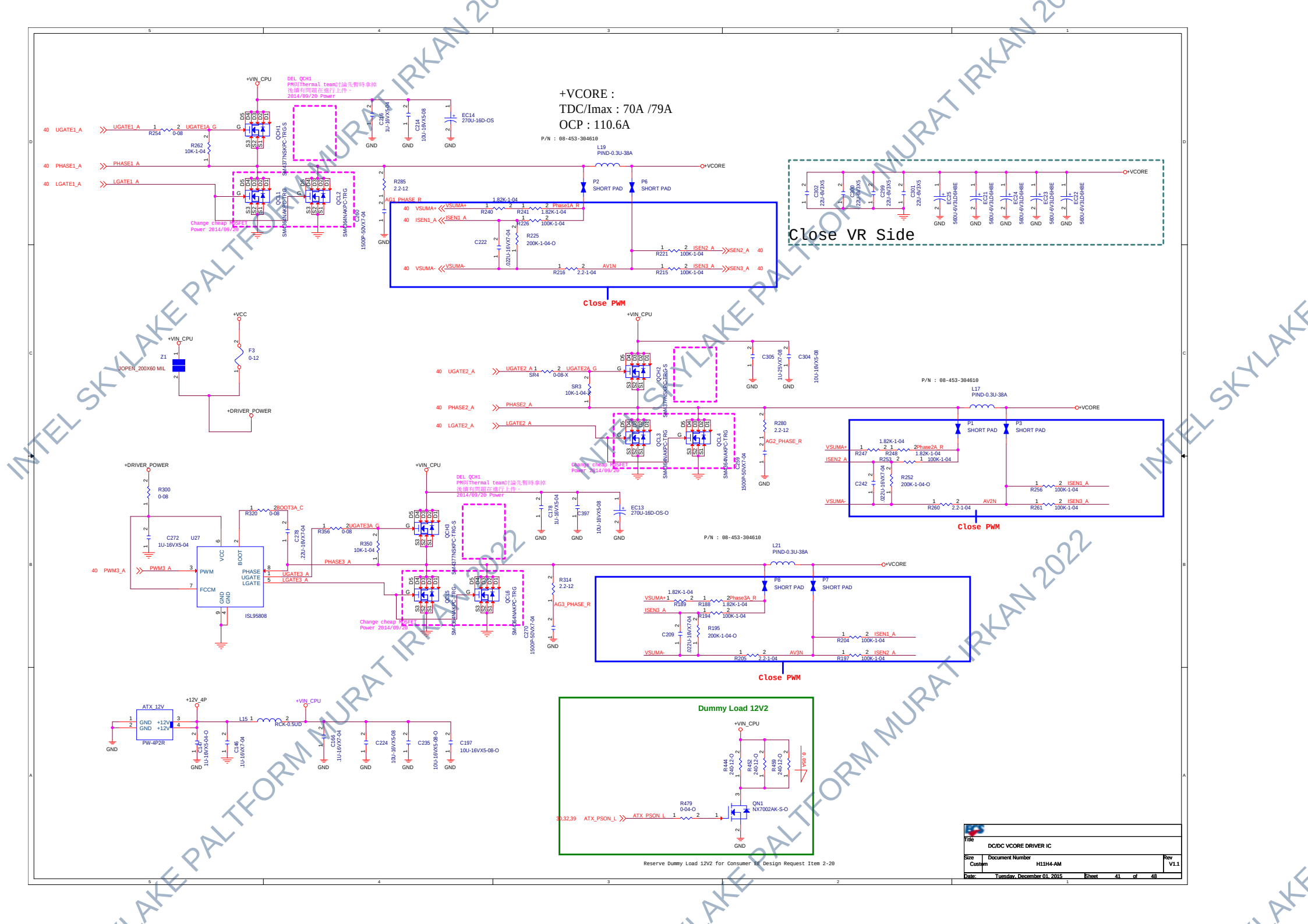
48

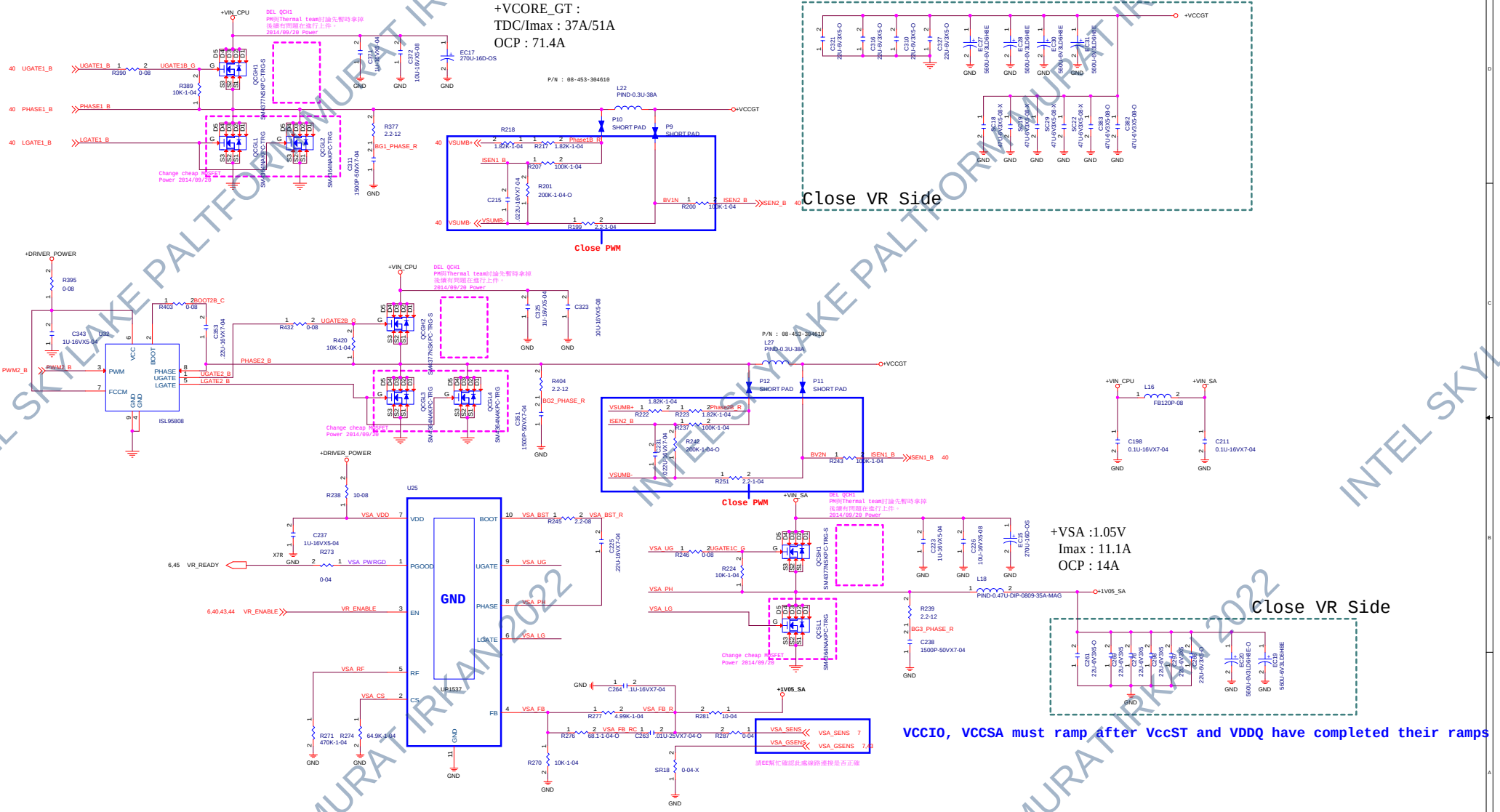


INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

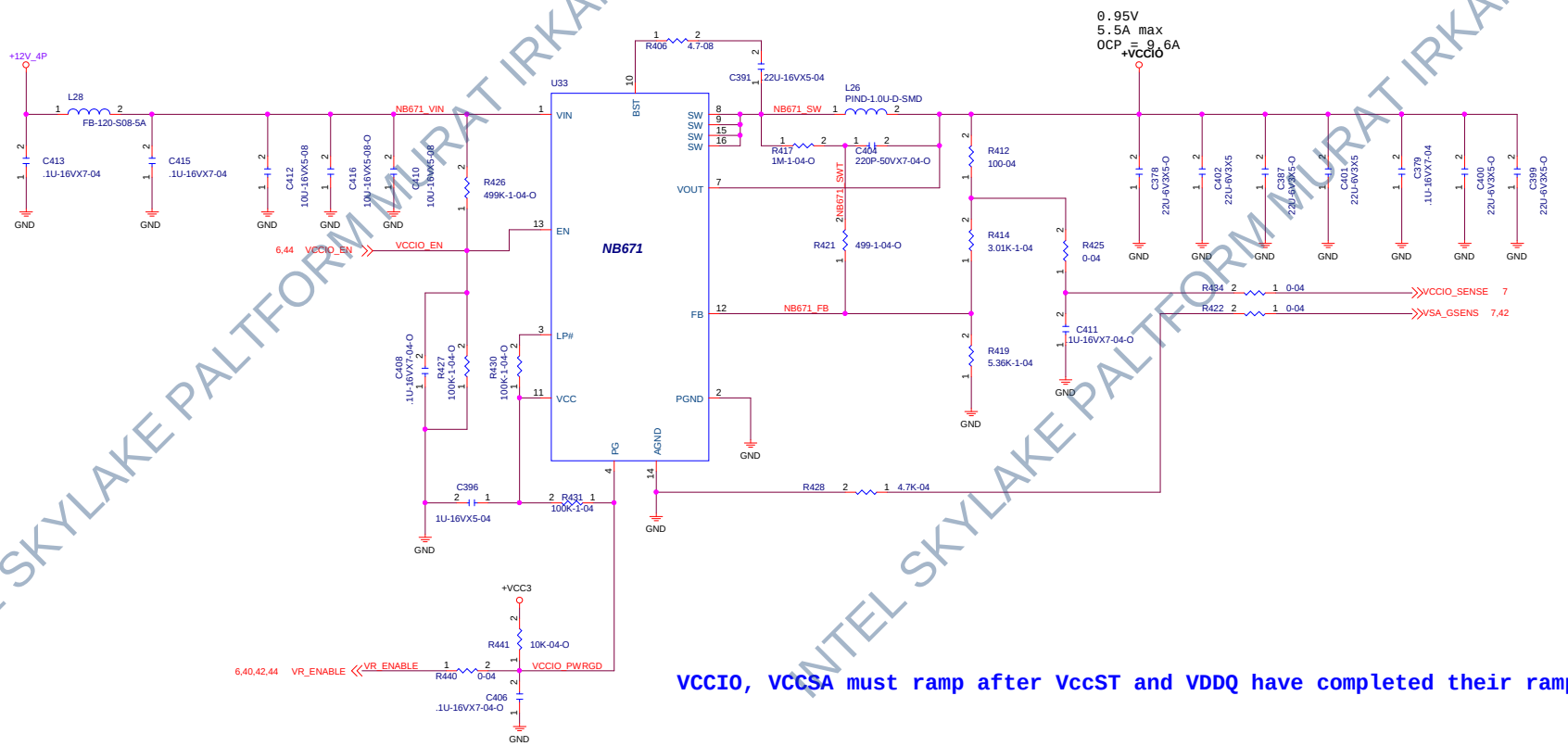

+VCC
+DRIVER_POWER
+VIN_CPU
+VCC3
+V1P0A_VCCST
+3VSB
+VCCGT
QP8
PMBS3906-S
U23
ISL95858HRZ
VR_ENABLE
VR_READY
VR_HOT#
H_VIDSCK
H_VIDALERT_L
H_VIDSOUT
I2DATA
I2CLK
PSYS
COMP_A
FB_A
FB2_A
RTN_A
COMP_B
FB_B
FB2_B
RTN_B
PROG1
VCORE_SENS
VCORE_GSENS
VCORE_GT_SENS
VCORE_GT_SENS
H_SKTOCC_L
H_SKTOCC_L_R
VBOOT_V1P05
Change for thermal 2015/8/4
ERT-J0EV474J
CLOSE QCH1
ERT-J0EV474J
CLOSE QCH7
CLOSE L1 DC SIDE
CLOSE L5 DC SIDE
8 VIA Connect GND tab
FOR VCORE AND VGT VBOOT=1.05V
Sam 0914'15
R244 stuff 1Kohm for VCCST noise
Elitegroup Computer Systems
DC/DC VCORE PWM IC
H11H4-AM
Tuesday, December 01, 2015



INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

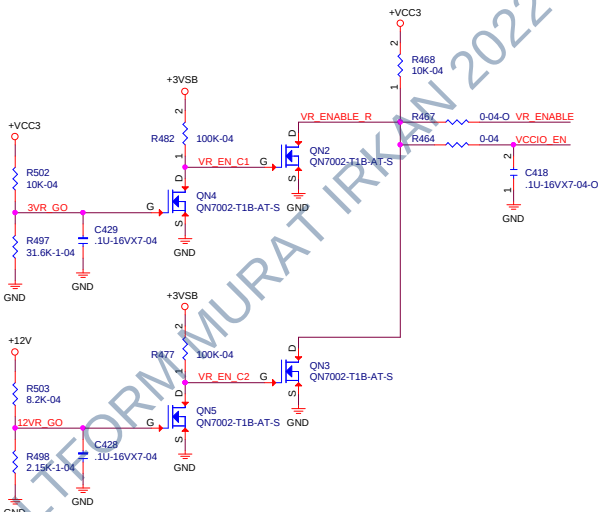


INTEL SKYLAKE PALTFORM MURAT IRKAN 2022



VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

VCCIO & VR ENABLE



Title	DC/DC VCCIO	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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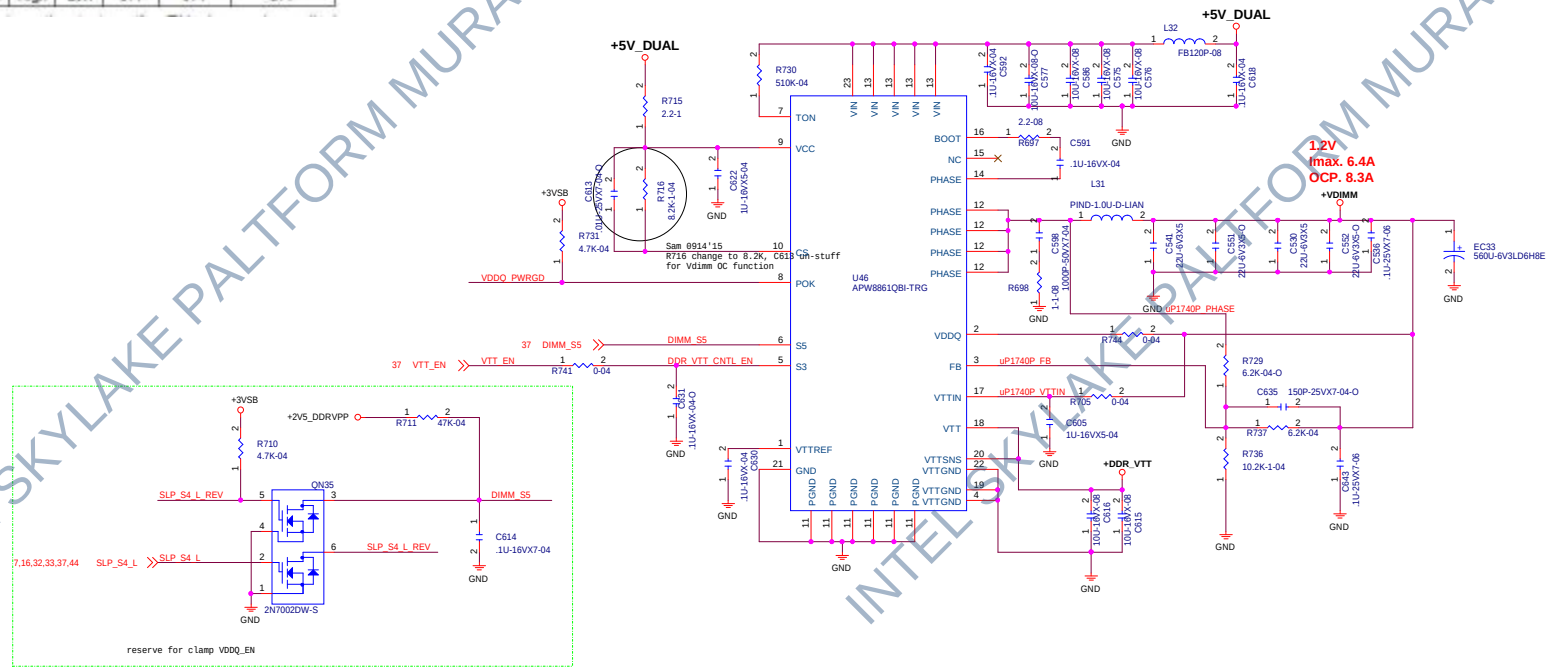
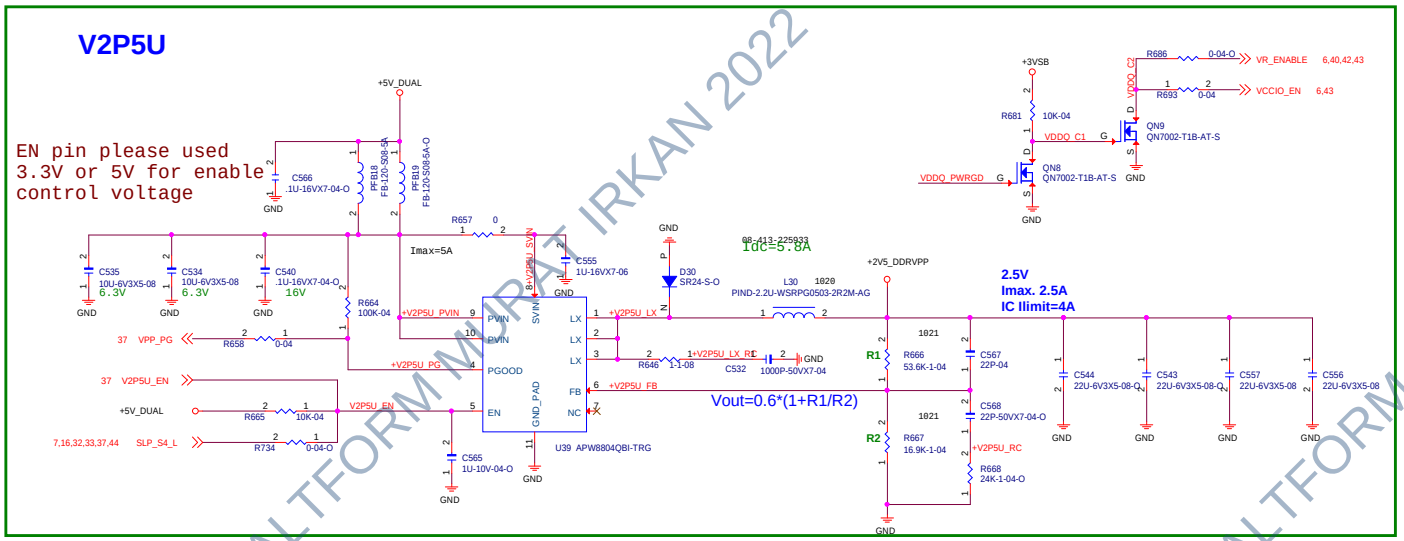
VDIMM Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF





Title	DC/DC VDIMM & DDRVTT	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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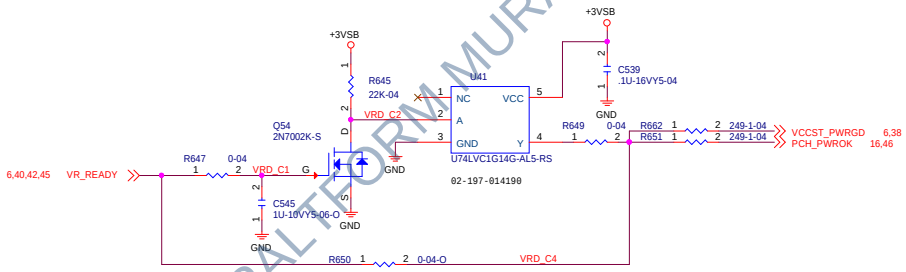
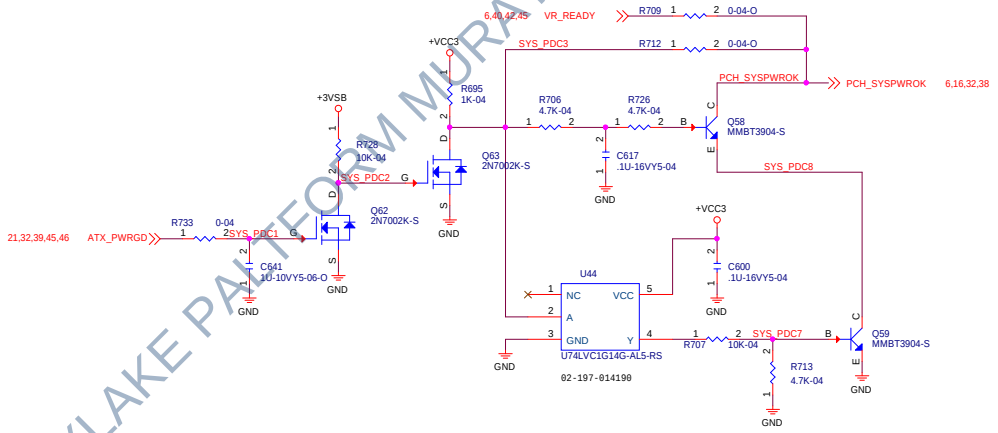
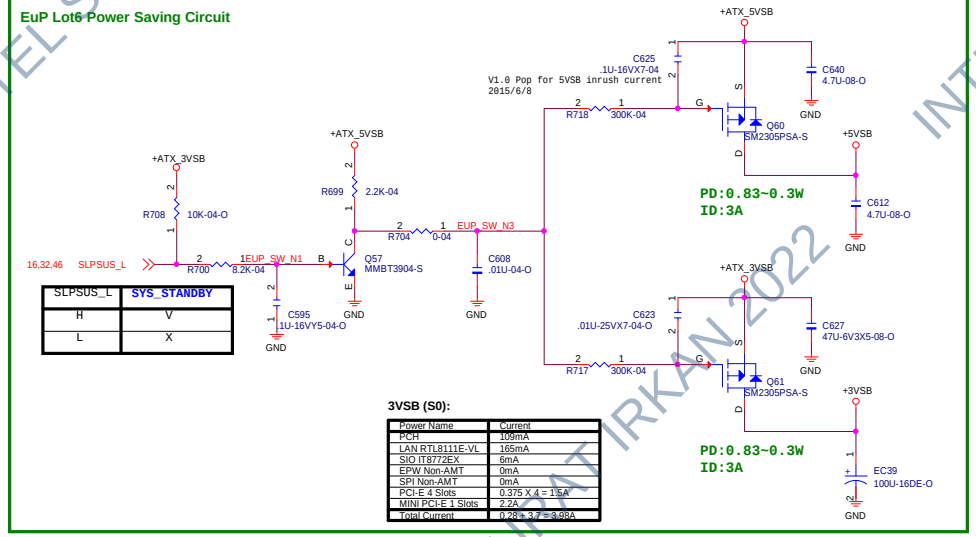
PCH & VCCST PWROK



SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit

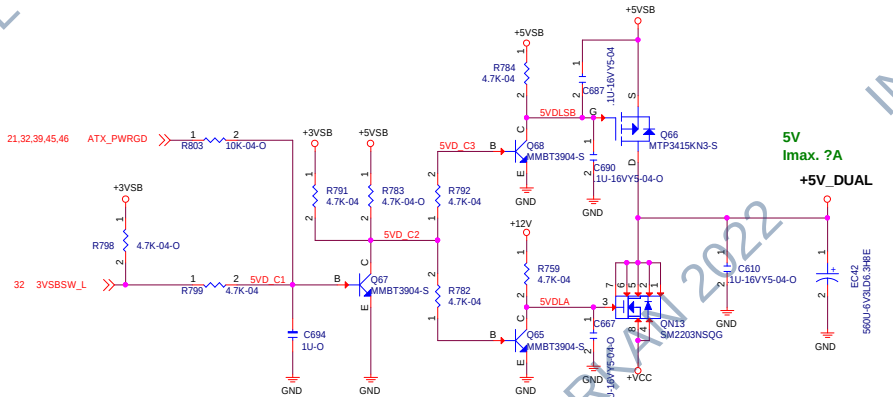


SLPSUS_L	SYS_STANDBY
H	V
L	X

3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A

5VDUAL



Title	DC/DC DDRVPP & 5VDUAL		
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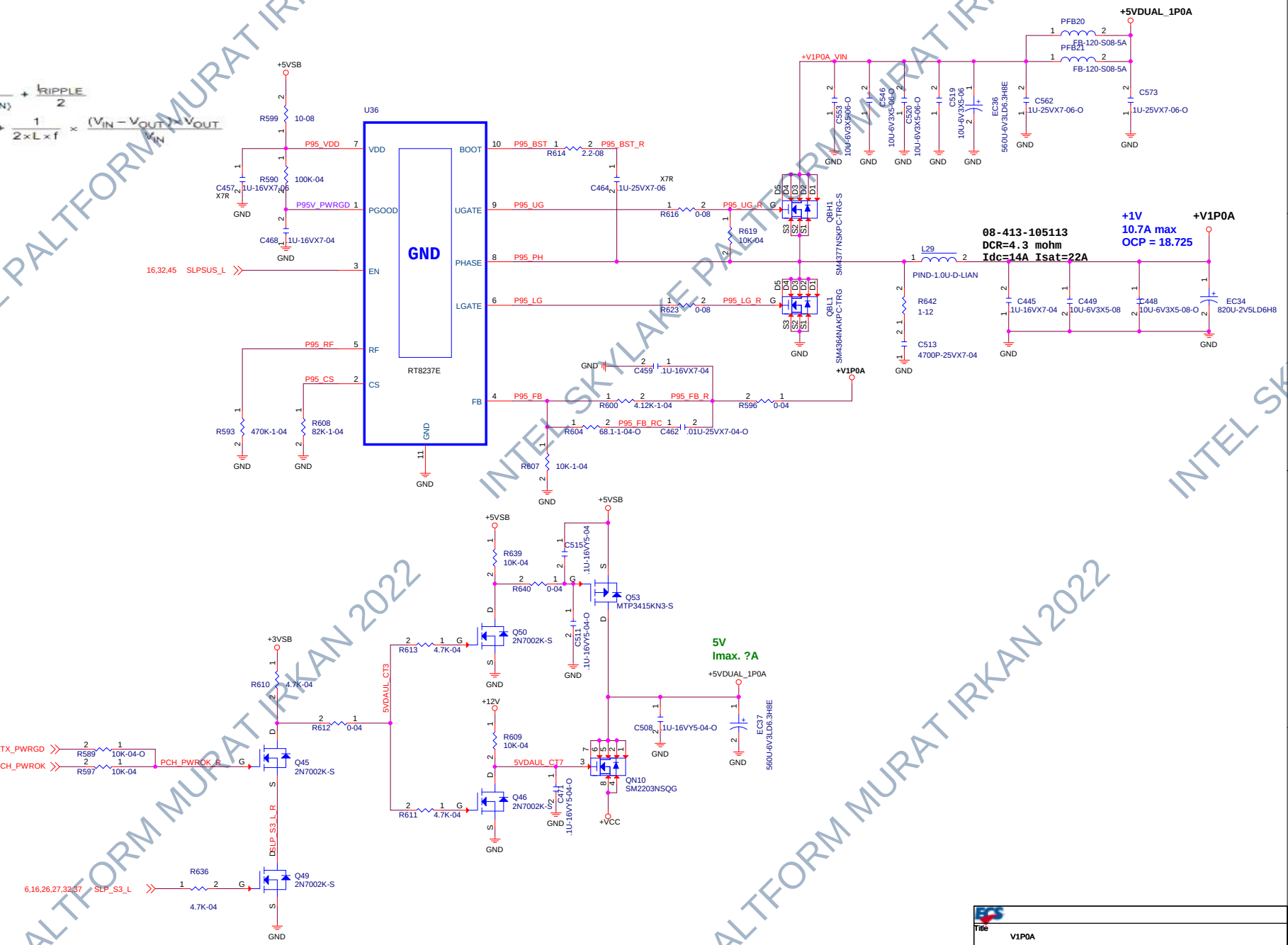
INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



Title	V1P0A		
Size	Custom	Document Number H11H4-AM	Rev V1.1
Date:	Tuesday, December 01, 2015	Sheet 46 of 48	

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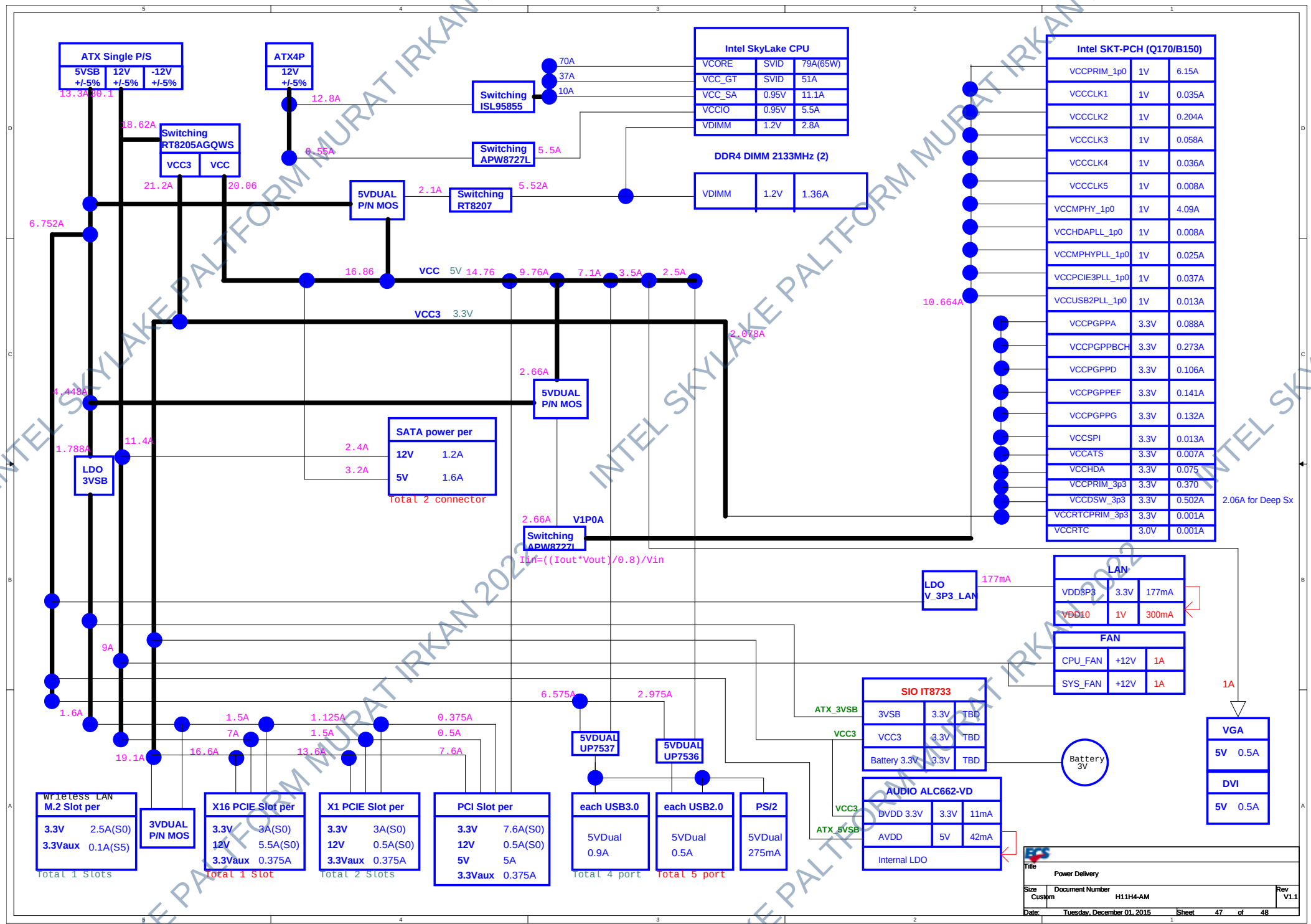


INTEL SKYLAKE PALTFORM MURAT IRKAN 2022

5 SLP4_L → +V1P0A_VCCST

+VDIMM

8.2 +VCC3 → +VCCIO

PGOOD[10]

9 → +1V05_SA

ISL95855HRTZ

VRDY[6]

10

PCIe X1 Slot_2

PCIe X16 Slot

PCIe X1 Slot_1

NGFF (For SSD)

NGFF (For WLAN & BT module)

TCM HEADER TPM module

13 SIO_PCIRST1_L

13 SIO_PCIRST2_L

13 SIO_PCIRST2_L

3 FP_PWRBTN_L

POWER BUTTON

1 +3VSB

9 ATX_PWRGD

30 PCIRST1# 31 PCIRST3# 81 PCIRST2#

PANSHW#[72] LRESET#[34]

Super I/O IT8733E-DX

RSMRST#[82] SUSB#[68] PWRON#[69] PWROK1[29] PSON#[73]

3VSB[32] ATXPG[16] VIN[2:3] [92],[93]

13 PCH_PLTRST_L

RSMRST# de-actives delay 75ms from SYS_3VSB

2 RSMRST_L

5 SLP3_L

4 SIO_PWRBTN_L

11 PWROK1

Delay Logic 150ms

PCH_PWROK[AW11]

PLTRST#[BB27]

RSMRST#[BA11] PLTRST_CPU#[AK2]

SLP_S3#[AW15] PCH-H

PWRBTN#[AT13] PROCPWRGD[AM3]

SYS_PWROK[AY1]

CPU_PLTRST_L

12 PROCPWRGD

RESET#[E7]

S-processor

PROCPWRGD

7.1 +12V

8.1 +VCC

7.2 +12V

MOS SWITCH

ATX Power 12V

6 PSON_L

8.2 +VCC3

5VSB to +3VSB LDO

Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

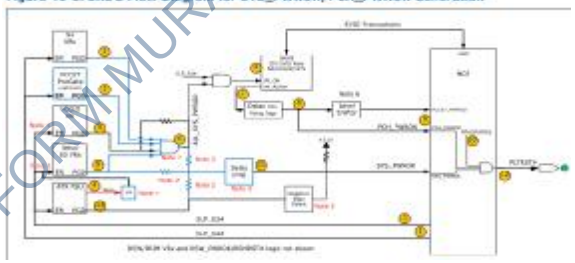
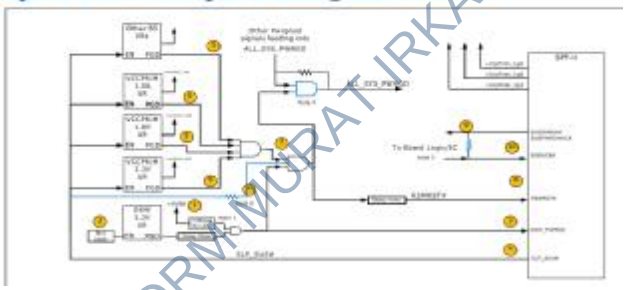


Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



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