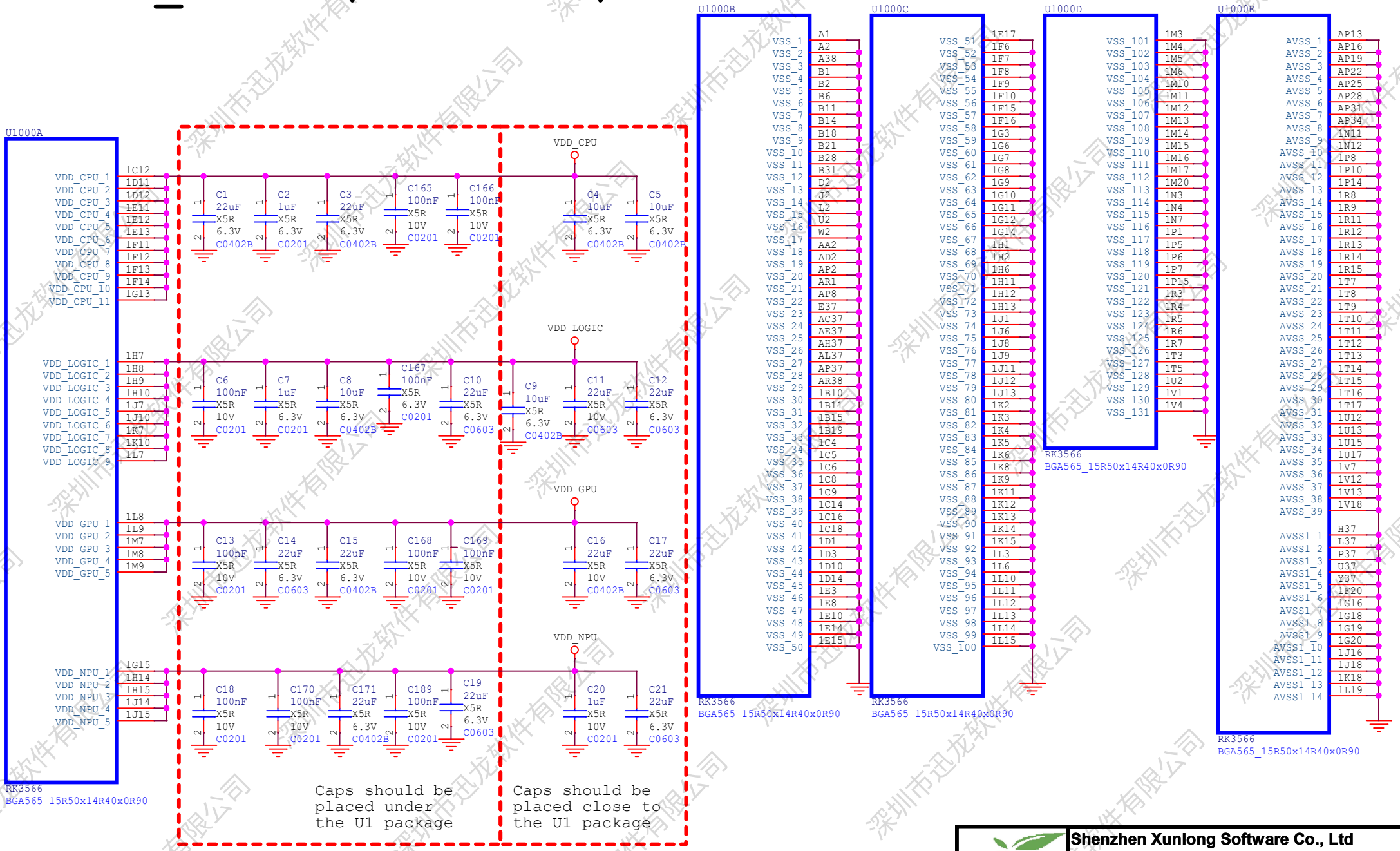
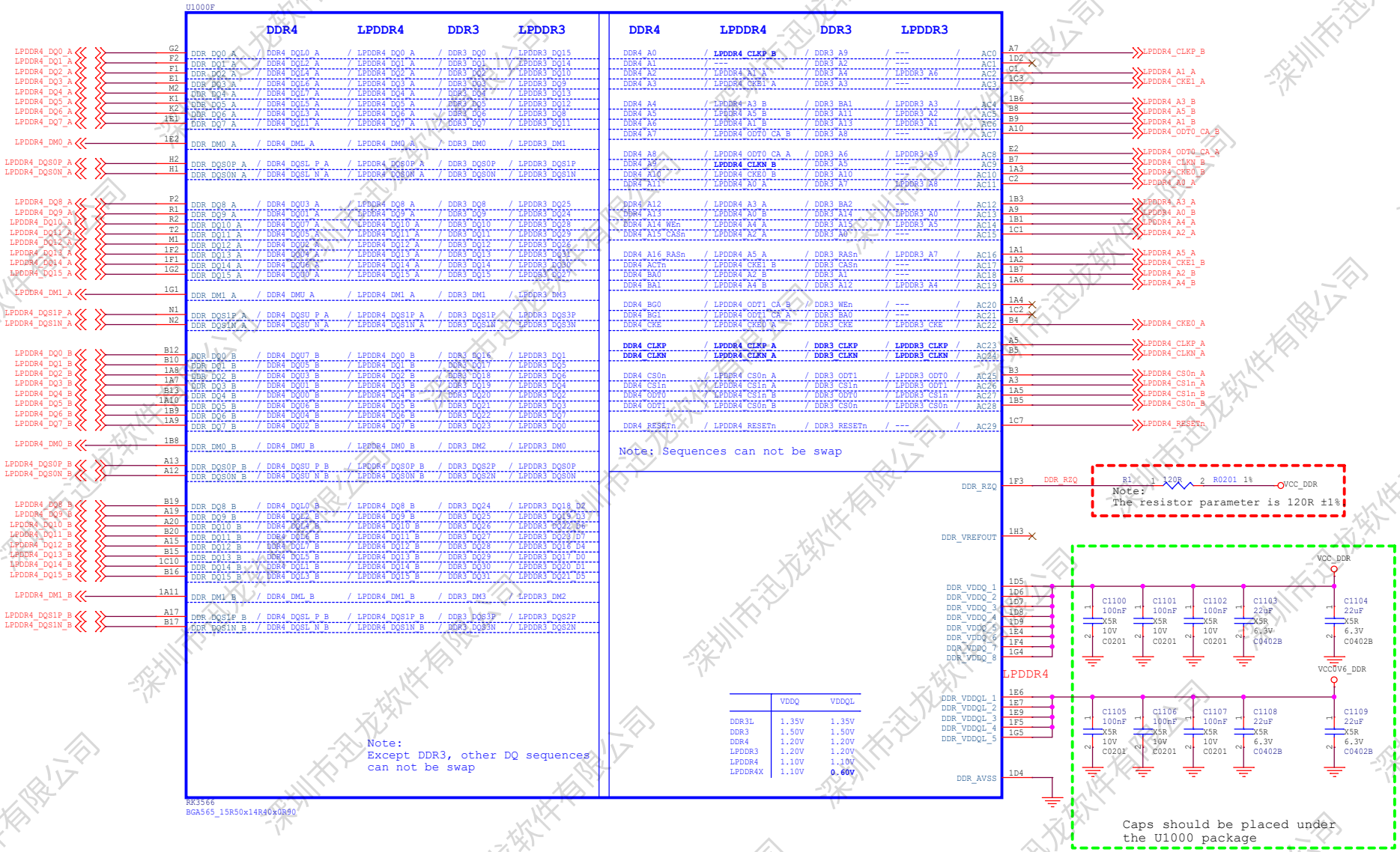
RK3566_ABCDE (Power&GND)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	01.RK3566_Power/GND				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

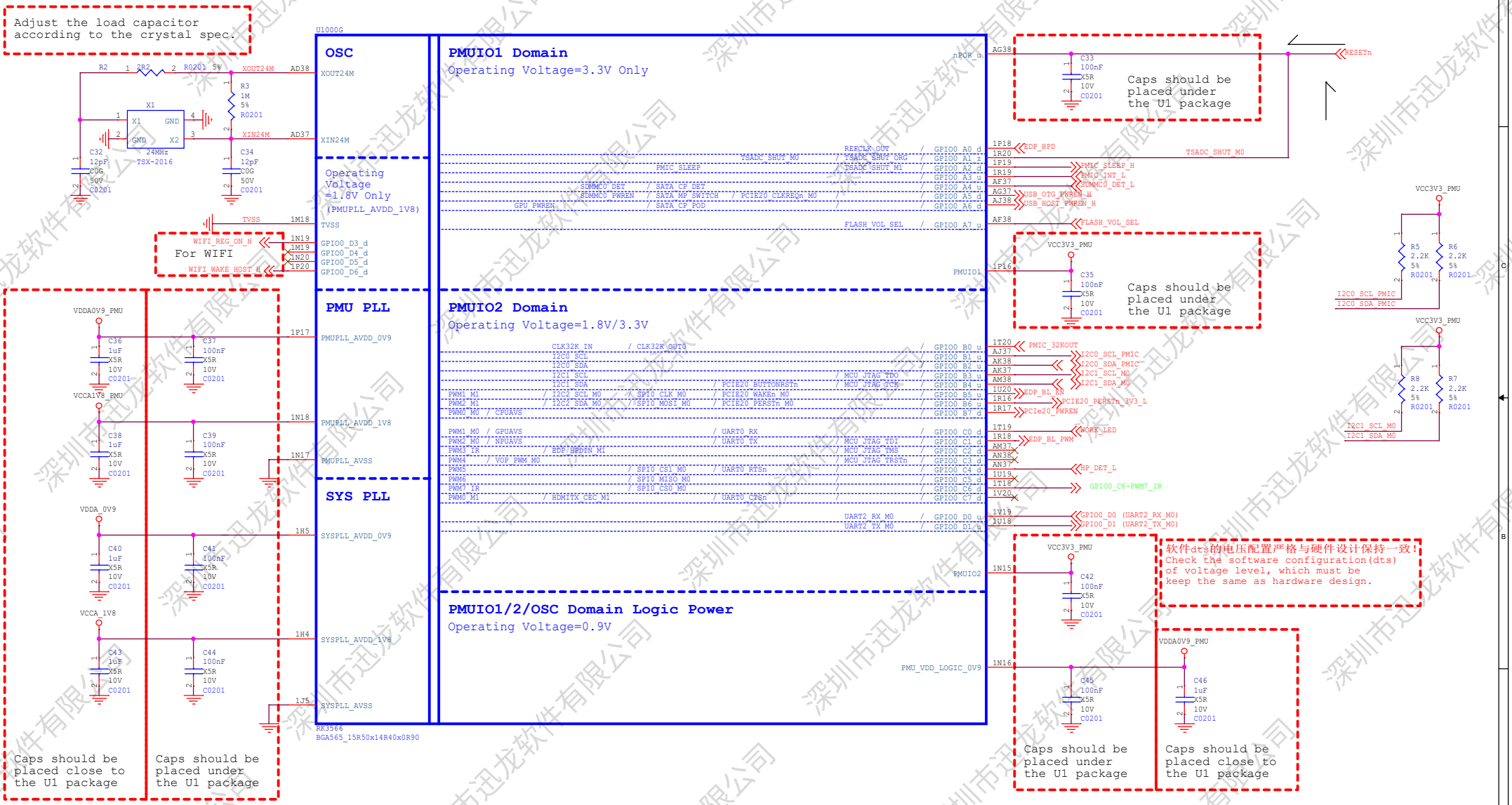
RK3566_F(DDR PHY)



	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	**0.60V**

Shenzhen Xunlong Software Co., Ltd				
Project:	OPi 3B			
File:	02.RK3566_DDR_PHY			
Date:	Monday, May 27, 2024		Rev:	V2.1
Size:	A3	Sheet: 0	Of:	0

RK3566_G(OSC/PLL/PMUIO1/2)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	03.RK3566_OSC/PLL/PMUIO				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0/FLASH_D0
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1/FLASH_D1
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2/FLASH_D2
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3/FLASH_D3
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4/FLASH_D4
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5/FLASH_D5
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6/FLASH_D6
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7/FLASH_D7
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD/FLASH_WRn
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	eMMC_CLKOUT/FLASH_DQS
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE/FLASH_CLE
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_CLK	/ FLASH_ALE	/ GPIO1_D0_d	1A15	FSPI_CLK/FLASH_ALE
FSPI_D0	/ FLASH_RDY	/ GPIO1_D1_u	1A17	FSPI_D0/FLASH_RDY
FSPI_D1	/ FLASH_RDn	/ GPIO1_D2_u	1A18	FSPI_D1/FLASH_RDn
FSPI_CS0n	/ FLASH_CS0n	/ GPIO1_D3_u	1B17	FSPI_CS0n/FLASH_CS0n
FSPI_D3	/ FLASH_CS1n	/ GPIO1_D4_u	1C15	FSPI_D3/FLASH_CS1n

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2

RK3566
BGA565_15R50x14R40x0R90

C209 C0201 2 1 12pF 25V C0G

VCCIO_FLASH

1C13 — C47 100nF X5R 10V C0201 — 1.8V

Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

TP5 eMMC_D0/FLASH_D0 TP100

TP7 FSPI_CLK/FLASH_ALE TP100

D2 B5819WS SOD_323 — eMMC_D0/FLASH_D0

D4 B5819WS SOD_323 — FSPI_CLK/FLASH_ALE

BOOT BOOT-SW T2Key

C196 100nF X5R 50V C0201

1. eMMC or Nand Flash:
   Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

2. SPI Flash:
   Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

RK3566_J(VCCIO3 Domain)

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1 / SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	SDMMC0_D0
PWM9_M1 / SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	SDMMC0_D1
SDMMC0_D2	/ ARM_JTAG_TCK/ UART5_CTSn_M0	/ GPIO1_D7_u	1D20	SDMMC0_D2
SDMMC0_D3	/ ARM_JTAG_TMS/ UART5_RTSn_M0	/ GPIO2_A0_u	1F18	SDMMC0_D3
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	1E19	SDMMC0_CMD
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ GPIO2_A2_d	G38 R23 0R R0201	SDMMC0_CLK

VCCIO3

RK3566
BGA565_15R50x14R40x0R90

C227 NC X5R 16V C0201

VCCIO_SD

1F17 — C50 100nF X5R 10V C0201

Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

default VCC = VCCIO_FLASH 1.8V

U2
XM25QU128CWIQT08Q
wson-6x5-mm

FSPI_CS0n/FLASH_CS0n — CS
FSPI_D1/FLASH_RDn — DO(D1)
eMMC_RSTn/FSPI_D2/FLASH_WPn — WP(D2)
VSS
HOLD(D3) — FSPI_D3/FLASH_CS1n
CLK — FSPI_CLK/FLASH_ALE
DI(D0) — FSPI_D0/FLASH_RDY
VCC
EPAD

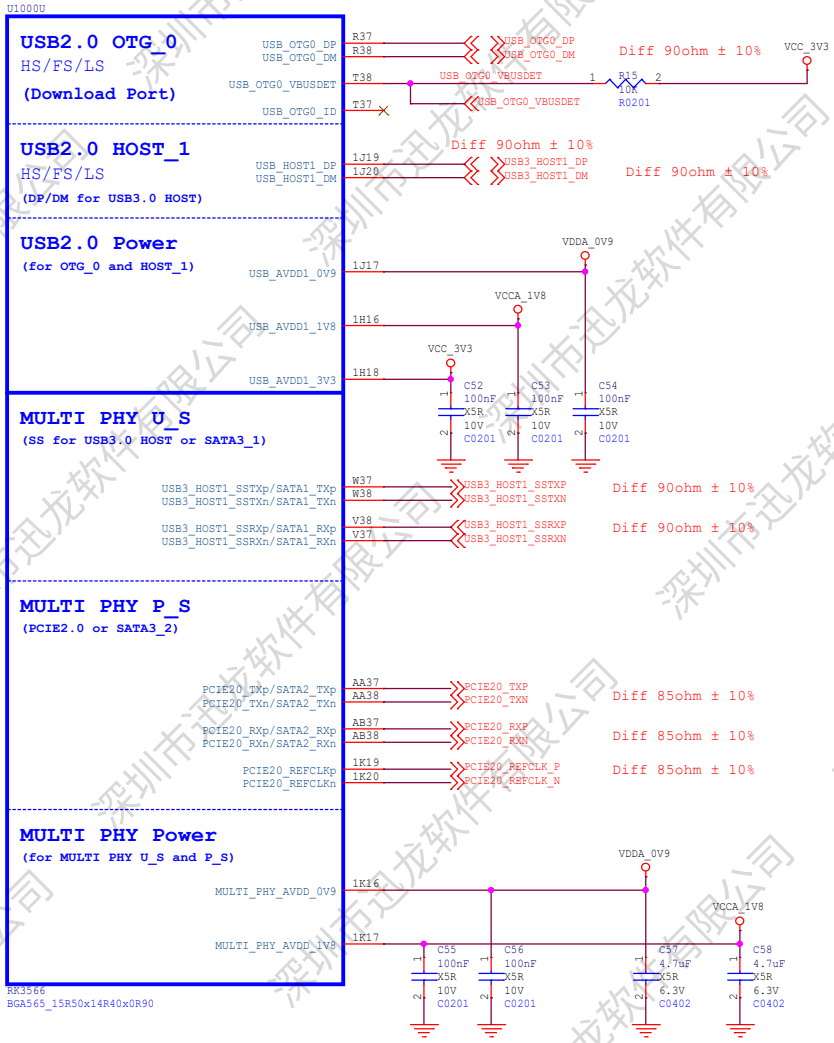
R12 10K R0201
R13 10K R0201

VCCIO_FLASH

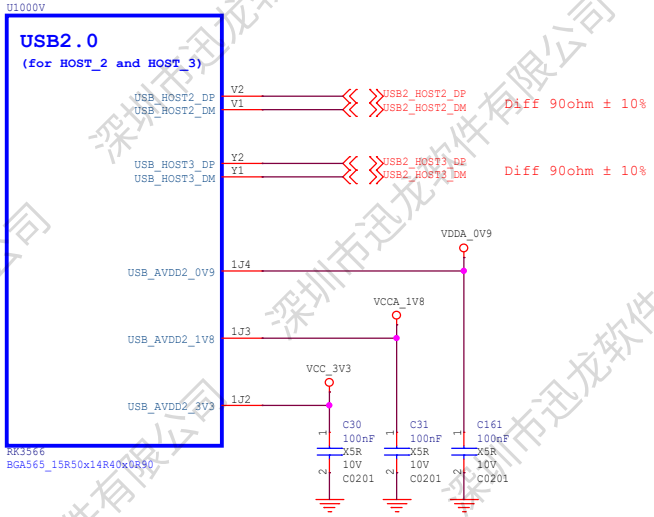
C48 100nF X5R 10V C0201
C49 1uF X5R 6.3V C0201

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	04.RK3566_Flash/SD_Contr				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_U(USB3.0/PCIe2.0x1/SATA)

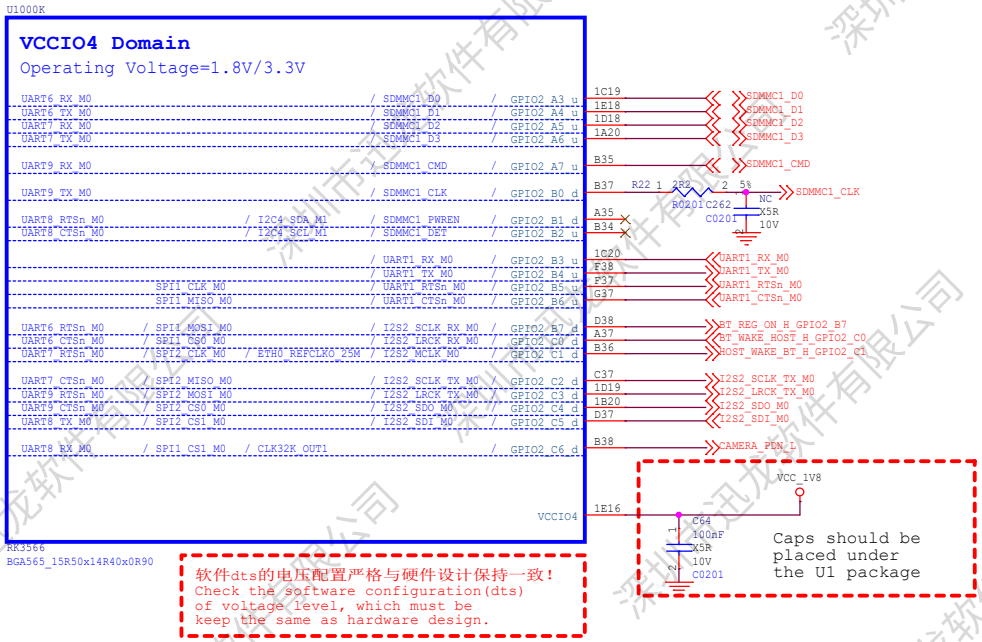


RK3566_V(USB2.0 HOST)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	05.RK3566_USB/PCIe/SATA_PHY				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

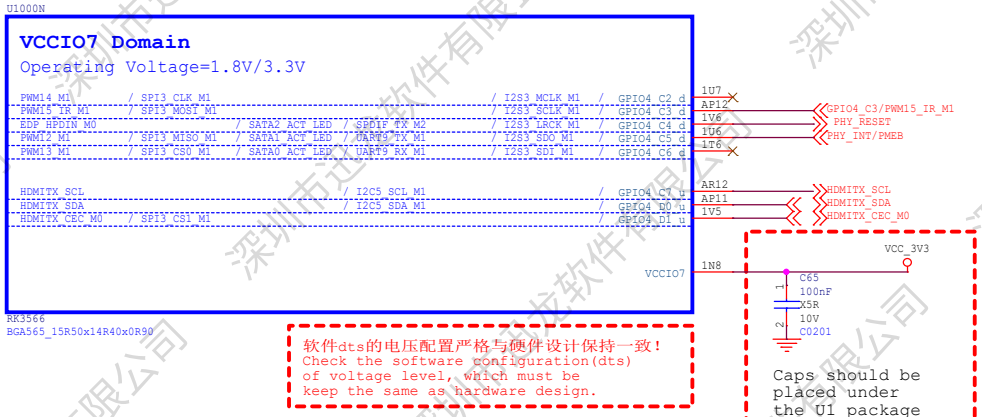
RK3566_K(VCCIO4 Domain)



Caps should be placed under the U1 package

软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

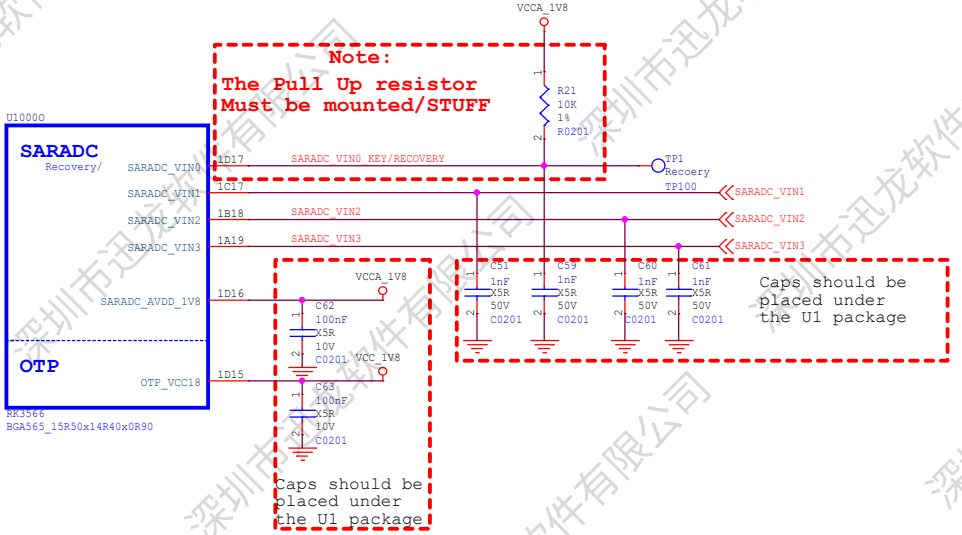
RK3566_N(VCCIO7 Domain)



Caps should be placed under the U1 package

软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

RK3566_O(SARADC/OTP)

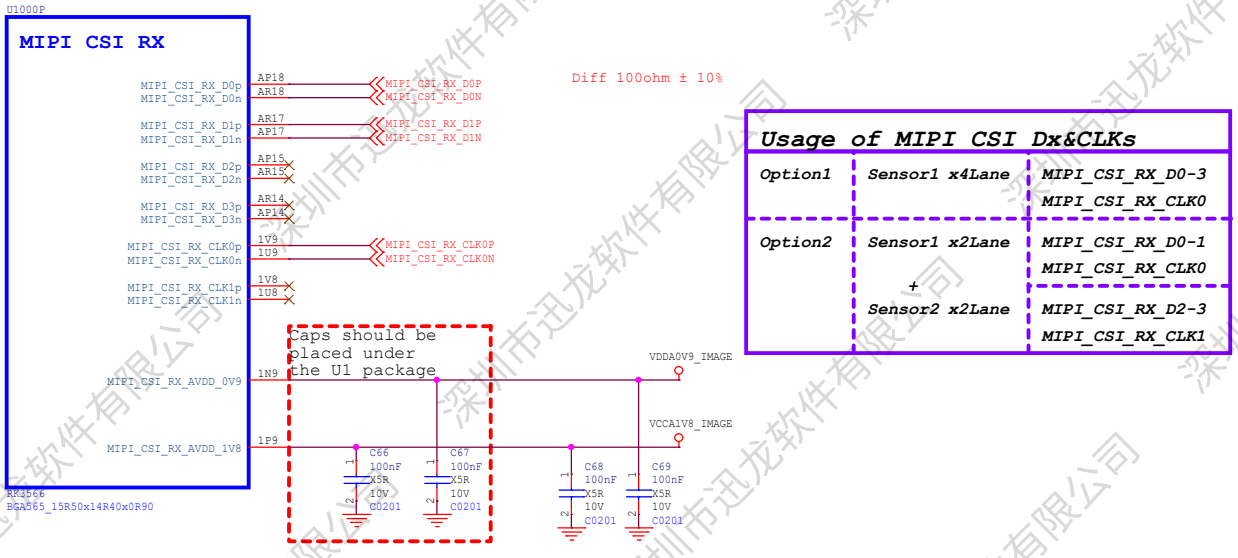


Caps should be placed under the U1 package

Caps should be placed under the U1 package

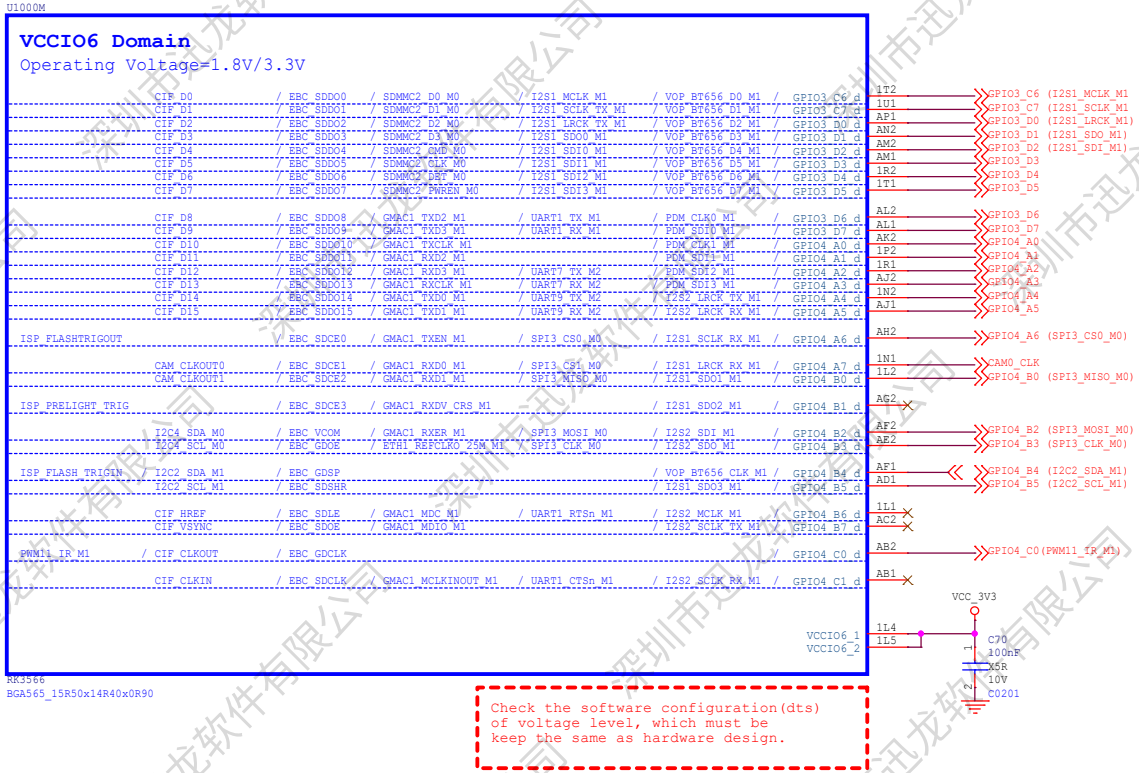
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	06.RK3566_SARADC/GPIO				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_P(MIPI_CSI_RX)

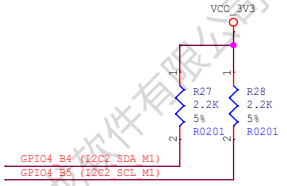


Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566_M(VCCIO6 Domain)

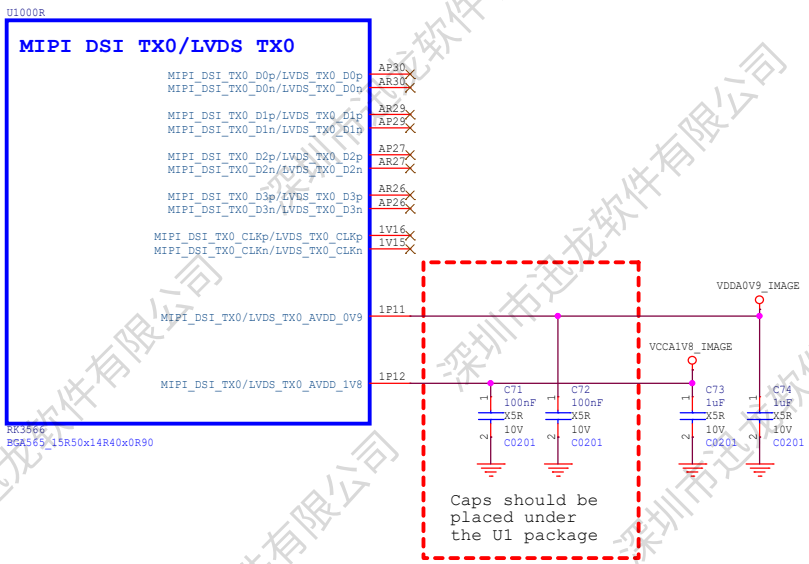


Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

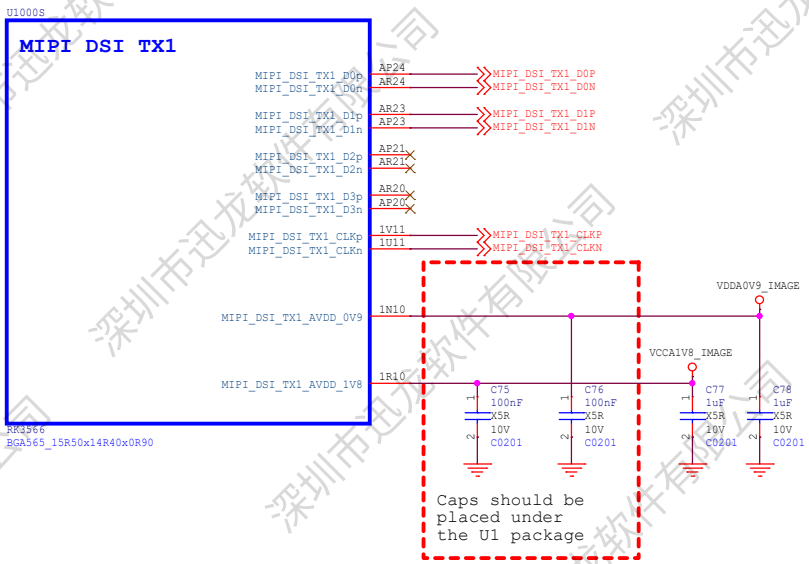


Shenzhen Xunlong Software Co., Ltd				
Project:	OPi 3B			
File:	07.RK3566_CSI/GPIO			
Date:	Monday, May 27, 2024		Rev:	V2.1
Size:	A3	Sheet: 0	Of:	0

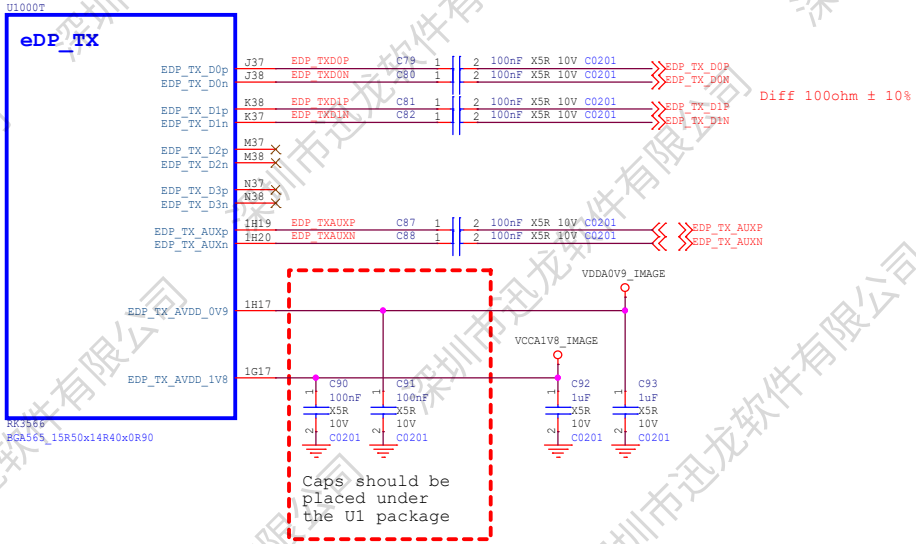
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



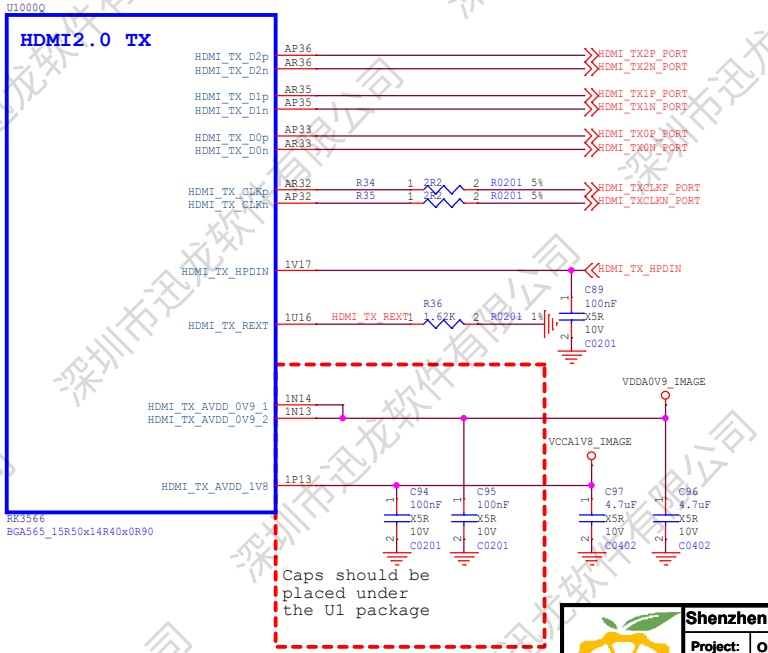
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



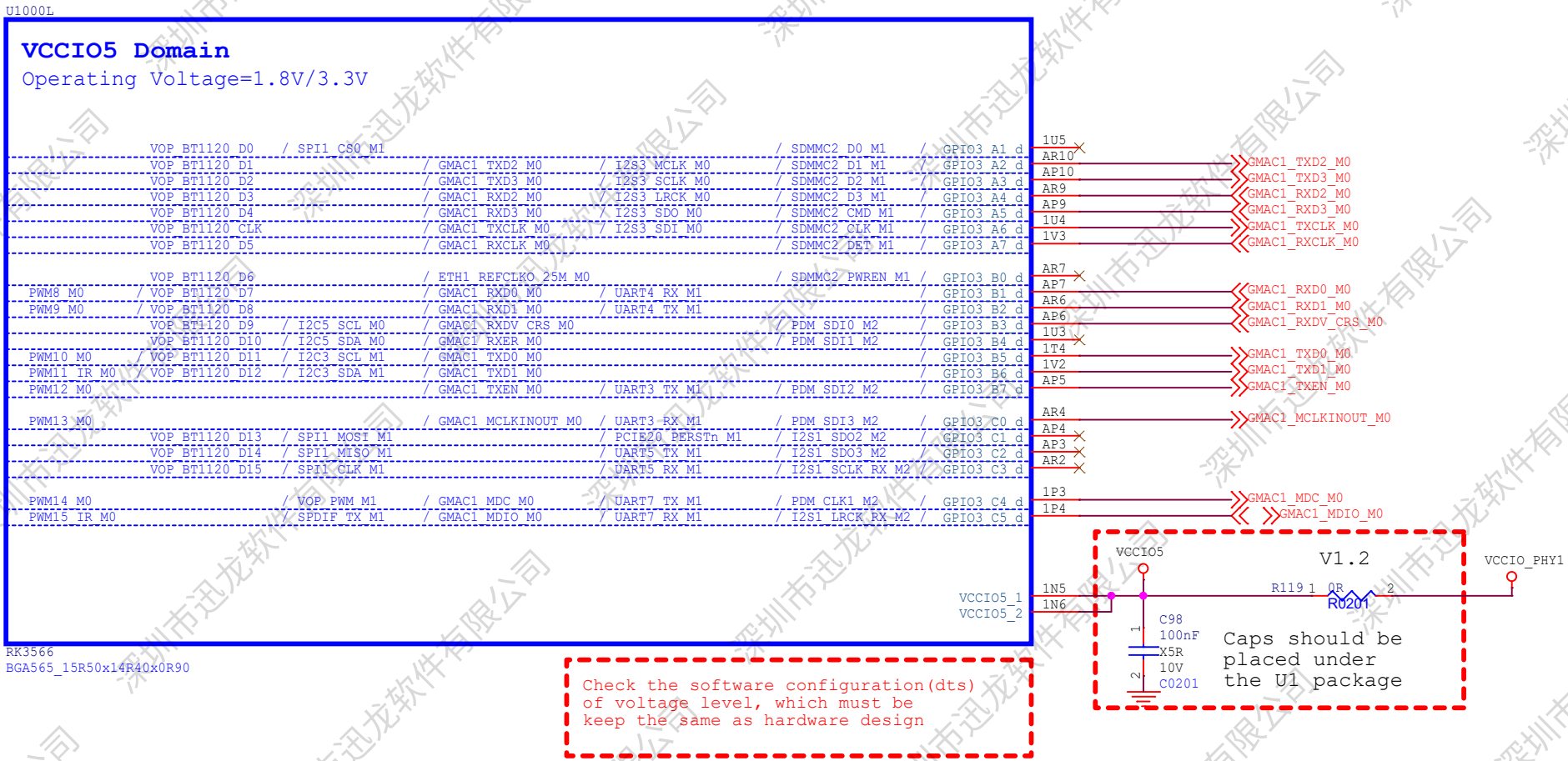
RK3566_Q(HDMI2.0 TX)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	08.RK3566_LVDS_MIPI				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

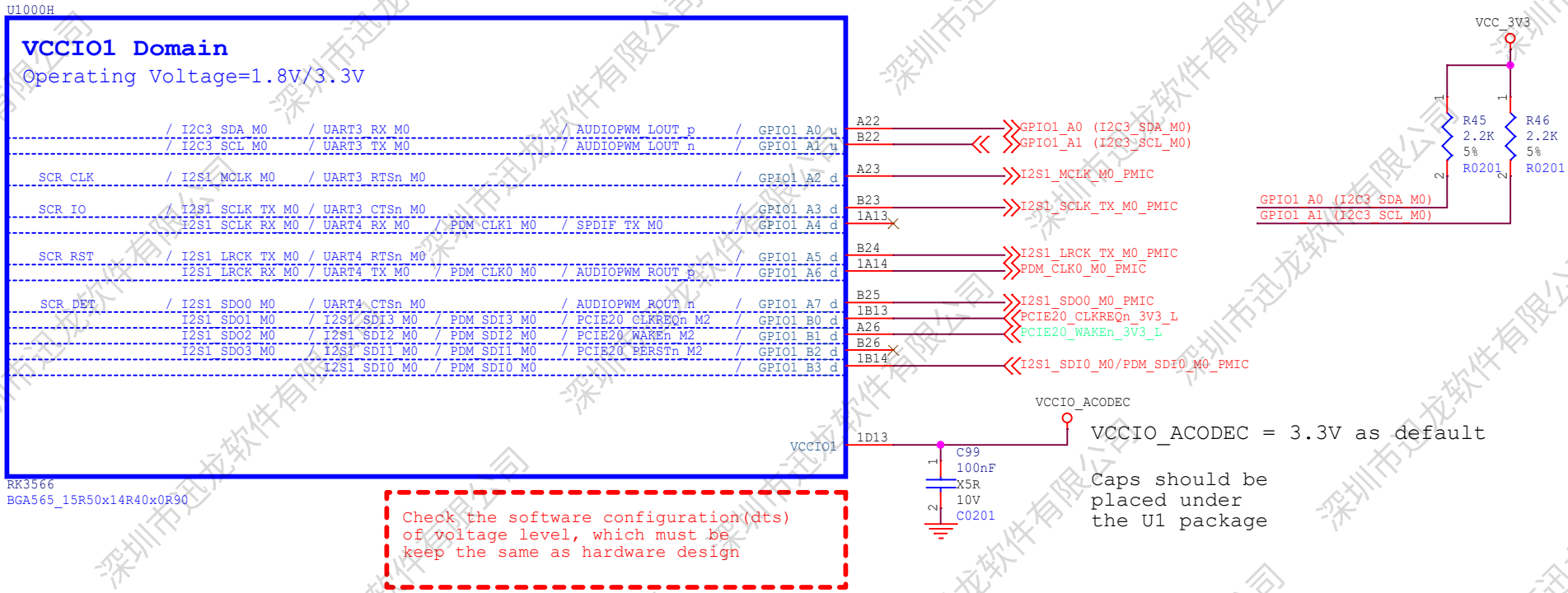
深圳市迅龙软件有限公司

RK3566_L(VCCIO5 Domain)

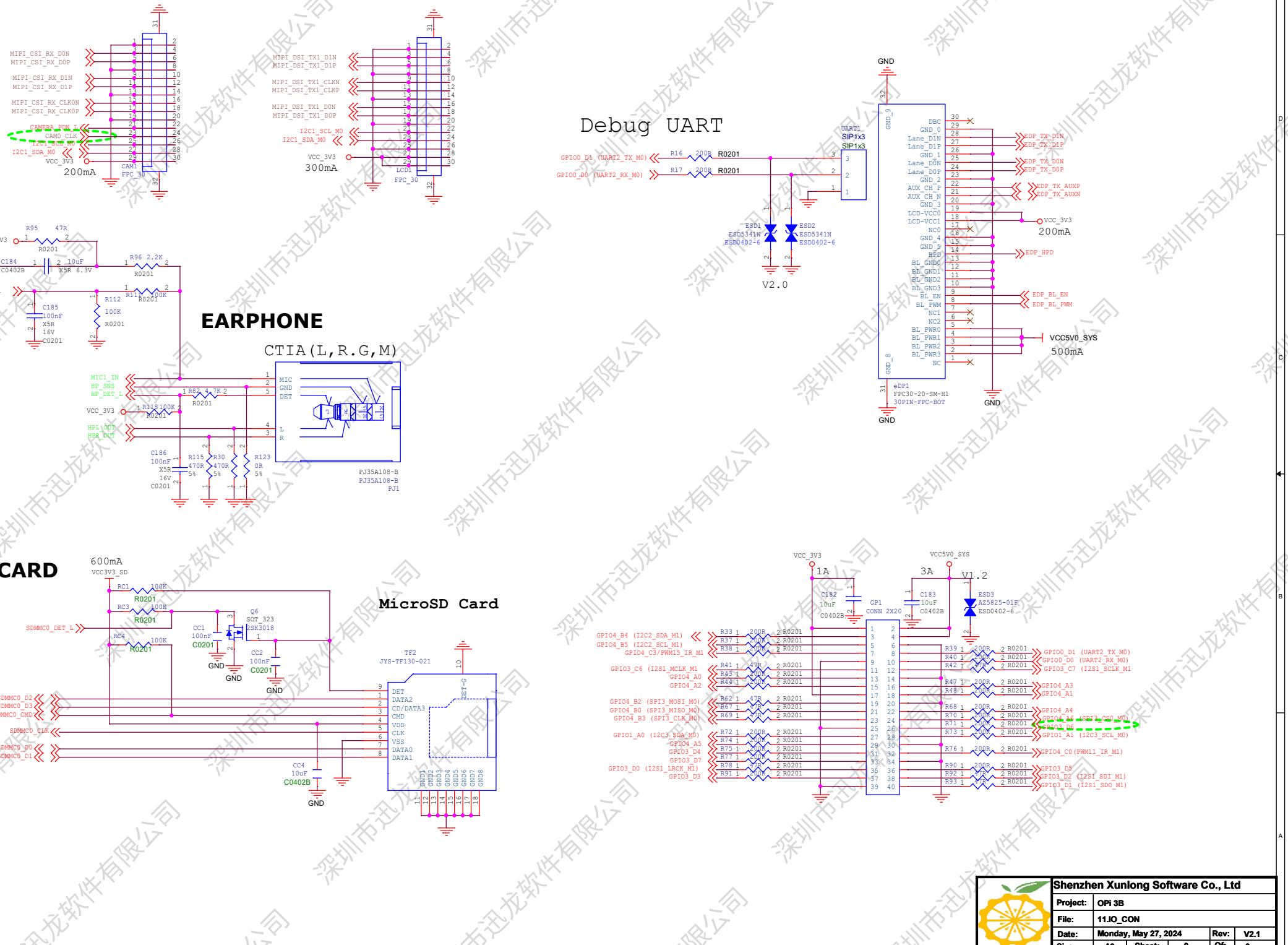


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	09.RK3566_GMAC				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

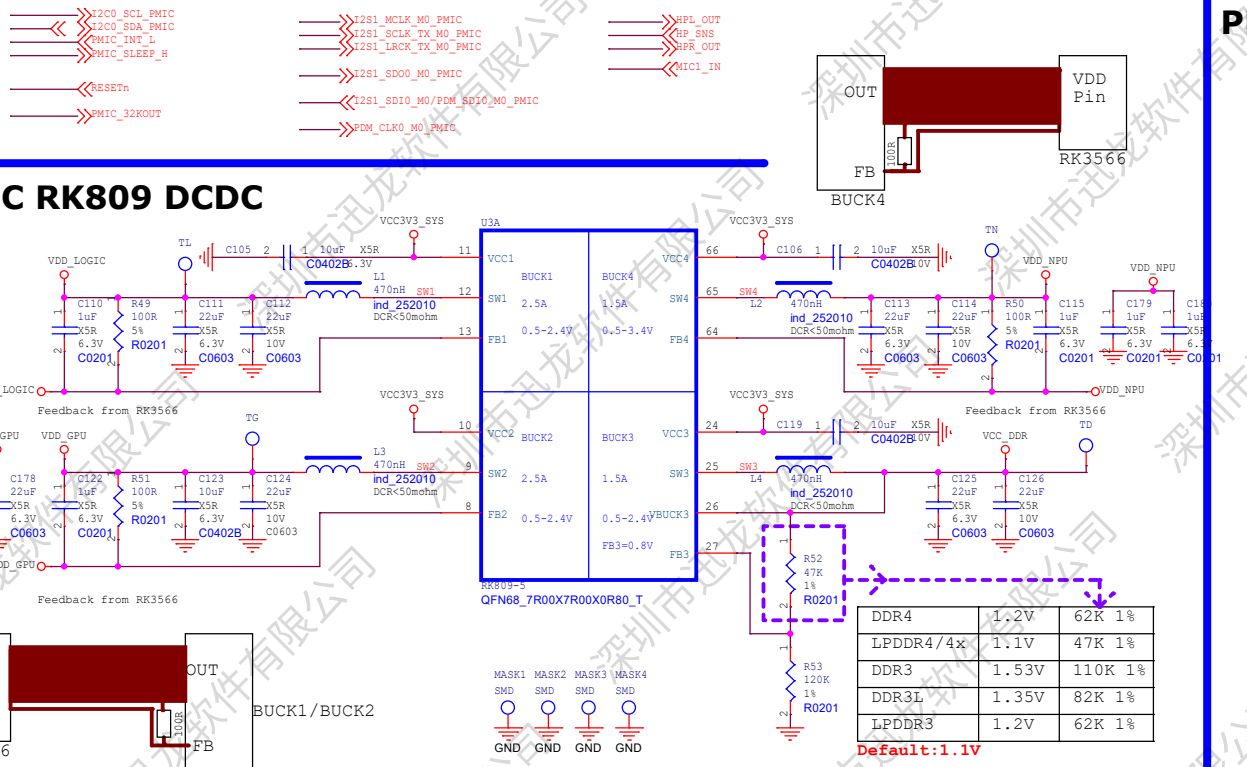
RK3566_H(VCCIO1 Domain)

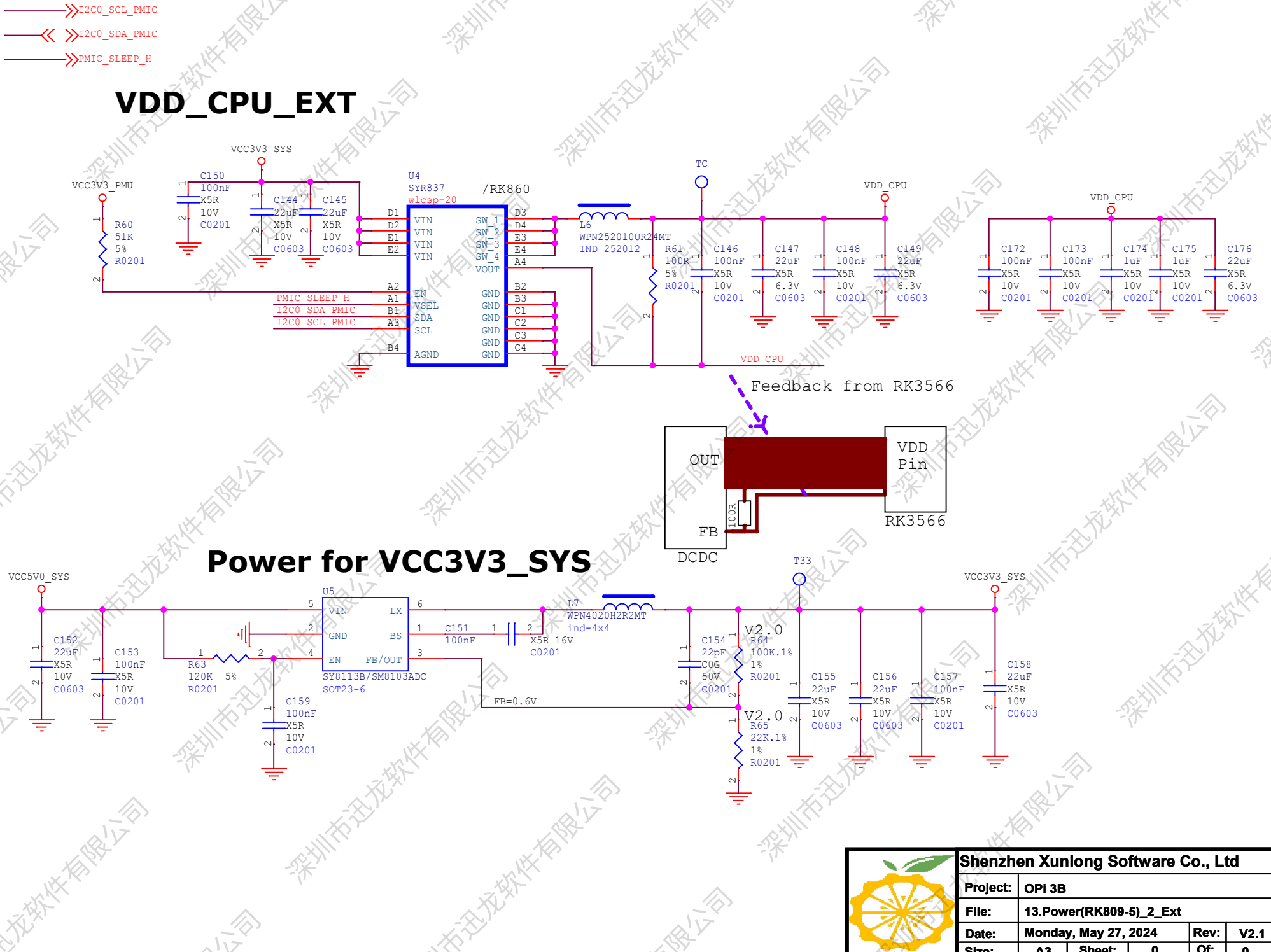


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	10.RK3566_Audio_Interface				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	11.IO_CON				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

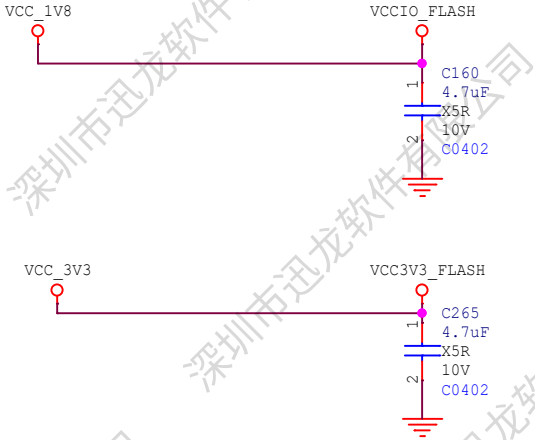

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RESETn
PMIC_32KOUT
I2S1_MCLK_M0_PMIC
I2S1_SCLK_TX_M0_PMIC
I2S1_LRCK_TX_M0_PMIC
I2S1_SDO0_M0_PMIC
I2S1_SDI0_M0/PDM_SDI0_M0_PMIC
PDM_CLK0_M0_PMIC
HPL_OUT
HP_SNS
HPR_OUT
MIC1_IN
PMIC RK809 DCDC
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
VCC3V3_SYS
U3A
RK809-5
QFN68_7R00X7R00X0R80_T
Feedback from RK3566
BUCK1/BUCK2
BUCK4
RK3566
VDD Pin
OUT
FB
100R
MASK1 MASK2 MASK3 MASK4
SMD
GND
DDR4 1.2V 62K 1%
LPDDR4/4x 1.1V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.2V 62K 1%
Default:1.1V
PMIC RK809 LDO
U3B
400mA LDO: 400mA@Vin>3V
200mA@Vin>2V
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V~3.6V 2.5A
VCC8\9: 2.7V~5.5V
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_1V8
PMIC RK809 Managerment
VCC5V0_SYS
VCC_RTC
RTC
D5
SOT_323
2PIN_1R25
A1251WF-2P-125
U3C
Gas Gauge
VREF
GNDREF
ePAD
XIN
XOUT
SDA
SCL
INT
SLEEP
CLK32K
RESETB
BATDIV
SNSP
SNSN
EXT_EN
VDC
PWRON
32.768HKz
SX-3215
RESET
RESET-SW
T2Key
PMIC_PWRON
TS-026-3
PWR_ON
1.2V
V2.0
PMIC RK809 CODEC
U3D
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p
MIC1n
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 12.Power(RK809-5)_1_PMIC
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
Of: 0

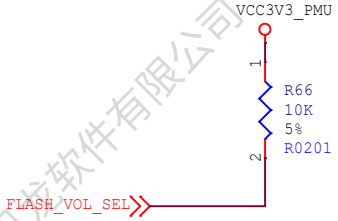


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	13.Power(RK809-5)_2_Ext				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

Flash Power Manage

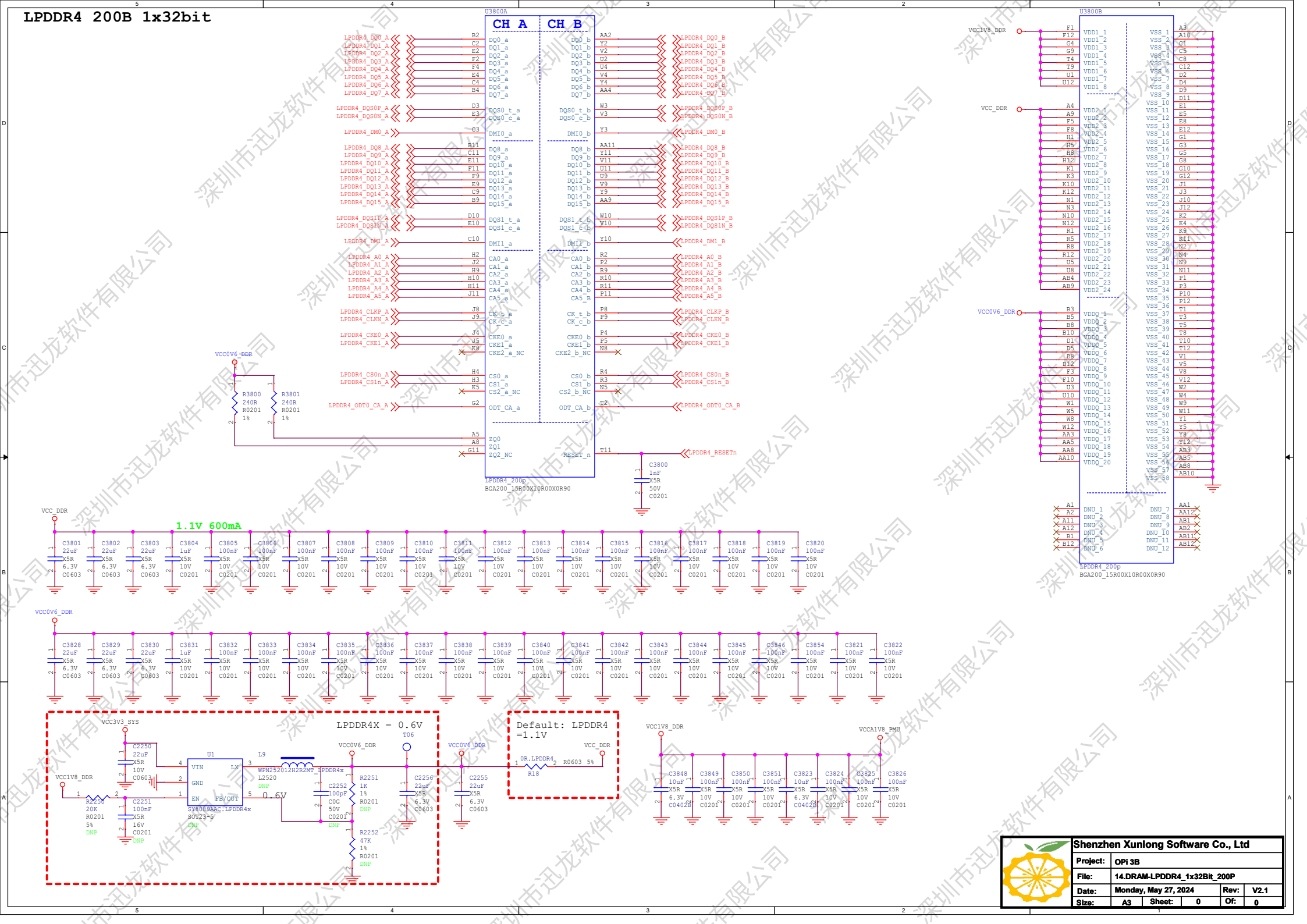
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=L(Default)

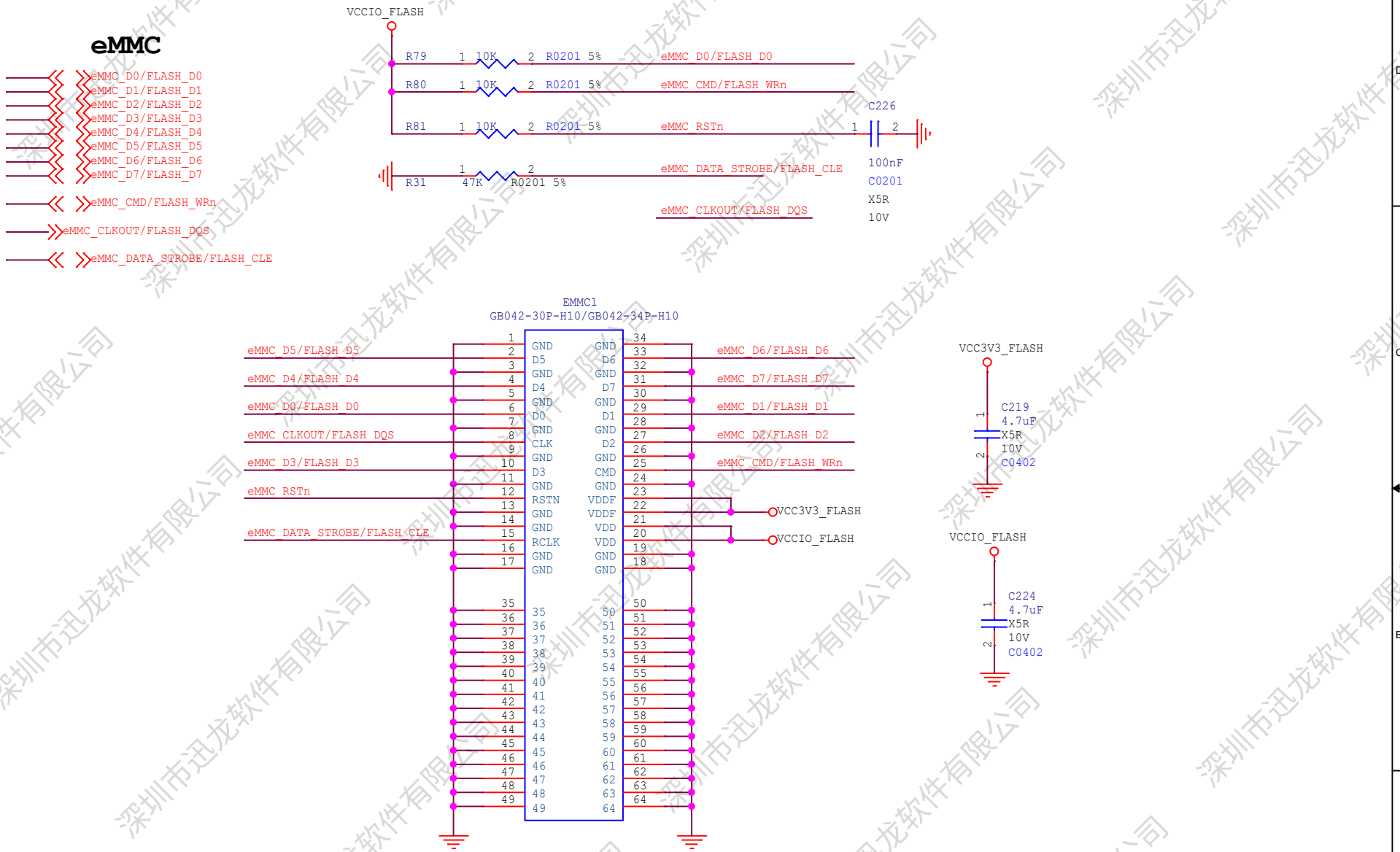




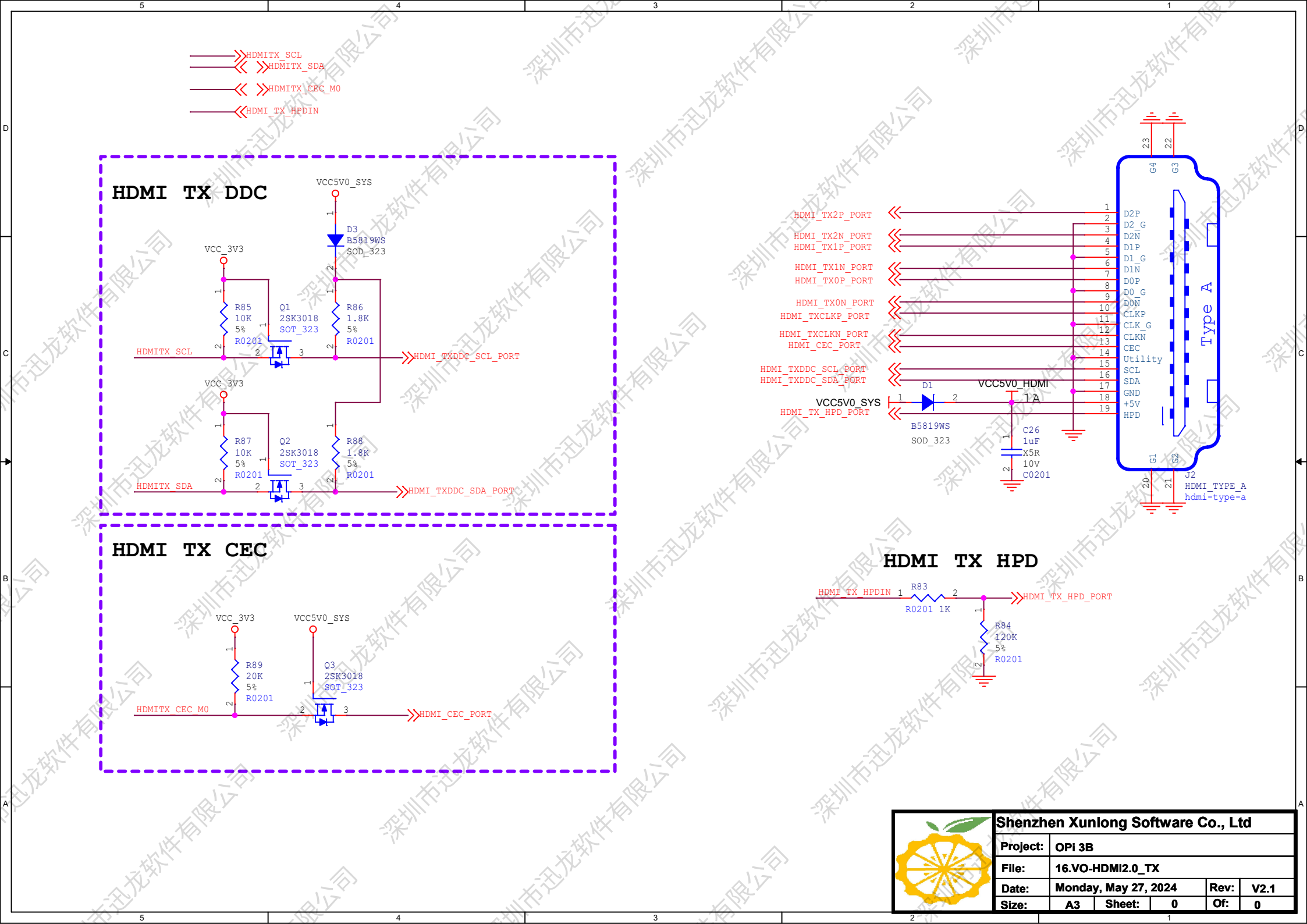
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	13.Power_Flash_Power_Manage				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

LPDDR4 200B 1x32bit





Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	15.Flash-eMMC_Flash				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	16.VO-HDMI2.0_TX				
Date:	Monday, May 27, 2024			Rev:	V2.1
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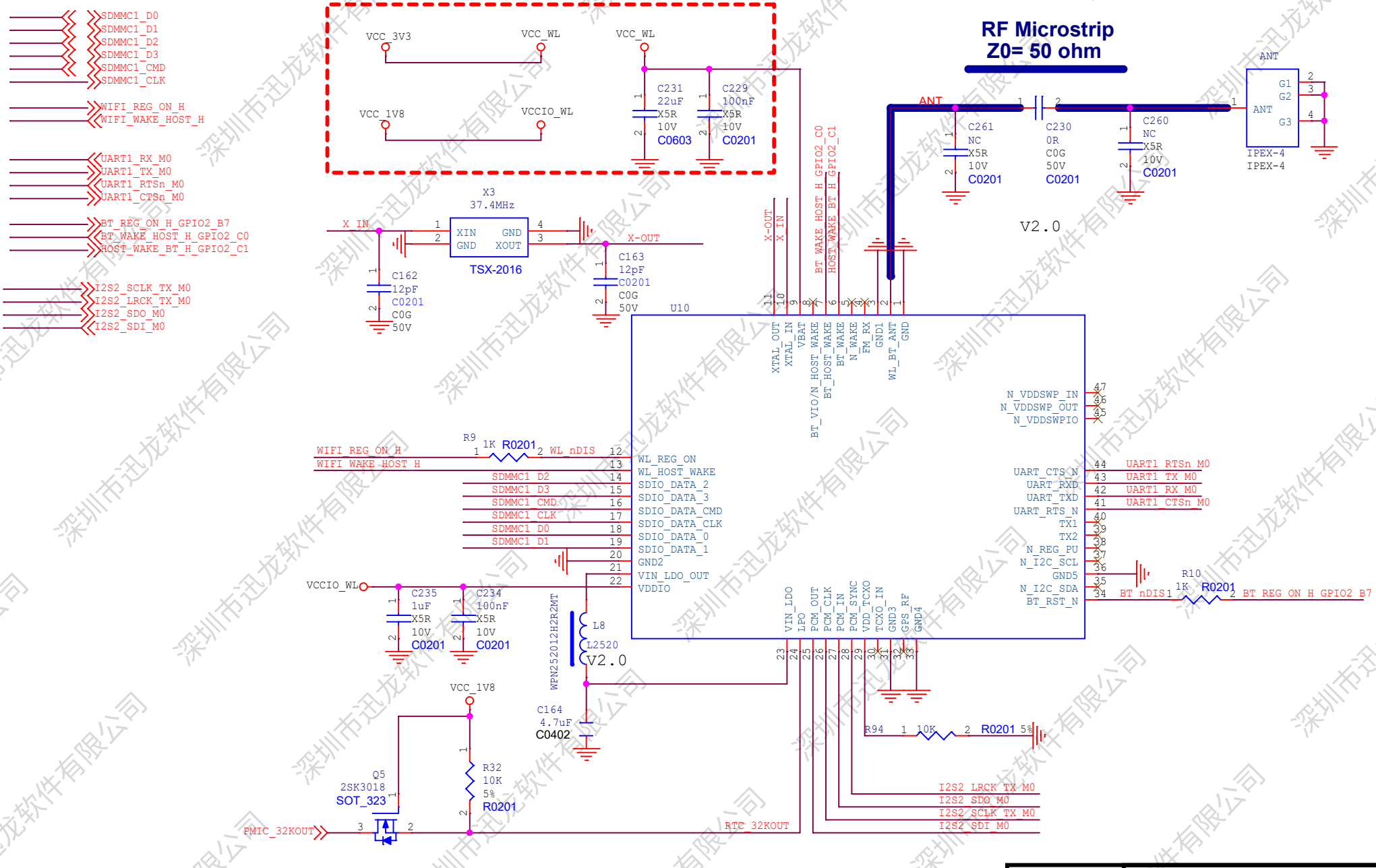
SDIO WIFI/BT Module-1T1R



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	17.WIFI/BT-SDIO_1T1R+UART				
Date:	Monday, May 27, 2024			Rev:	V2.1
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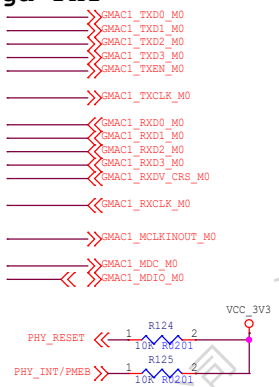
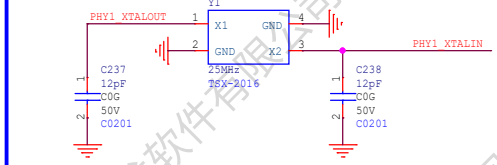
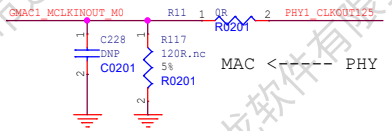
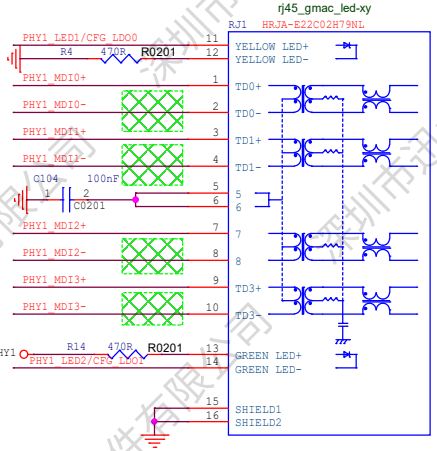
Giga PHY

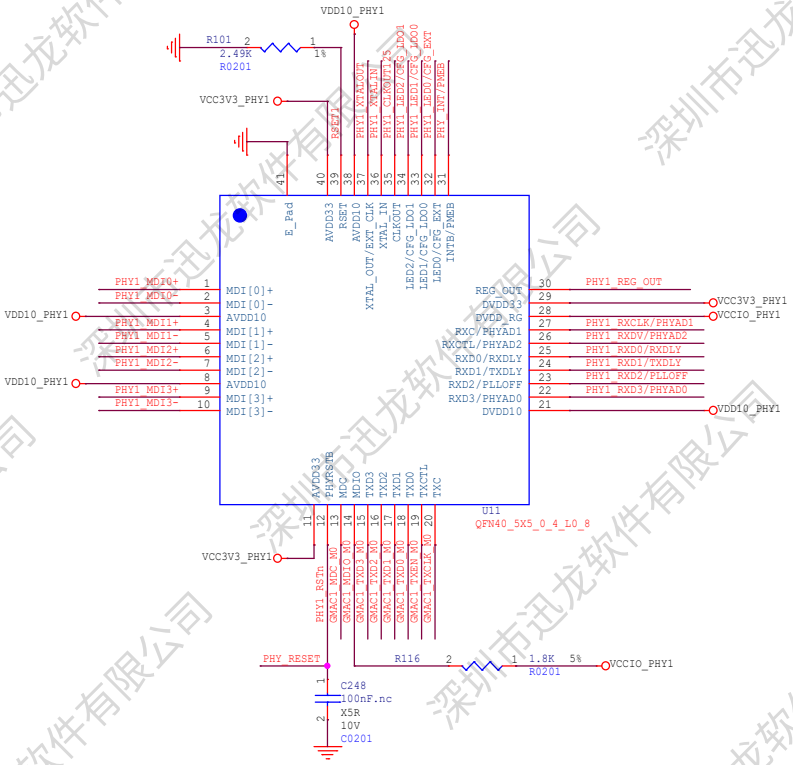


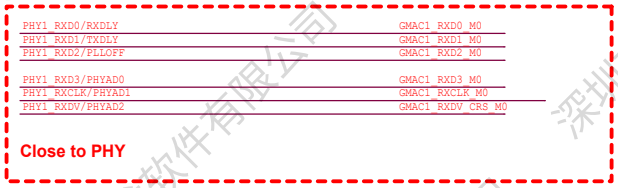


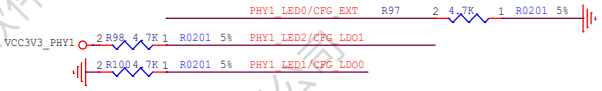


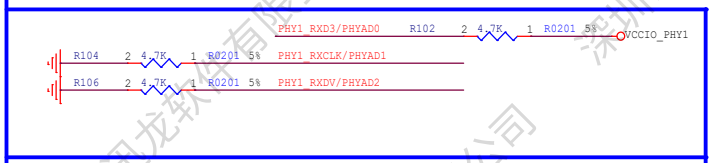
Differential pairs
Z0= 100 ohm

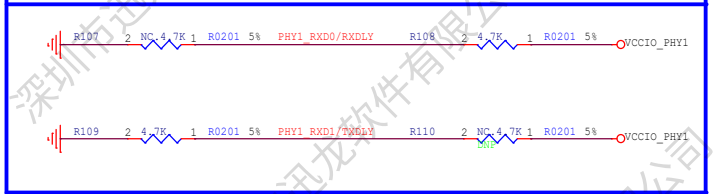


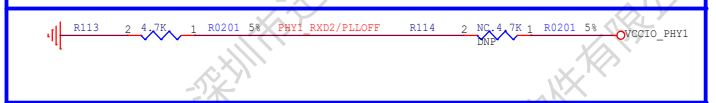




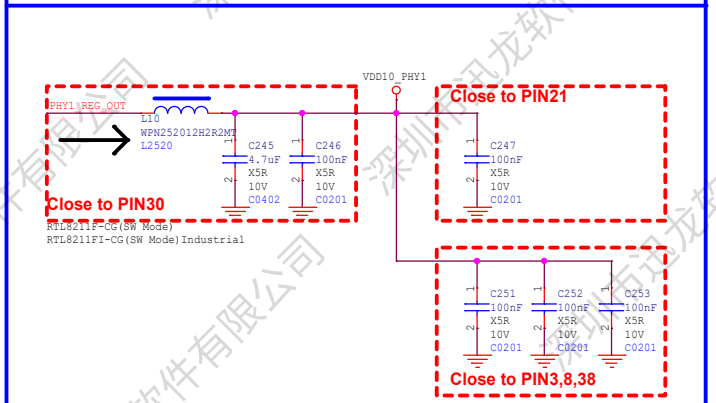


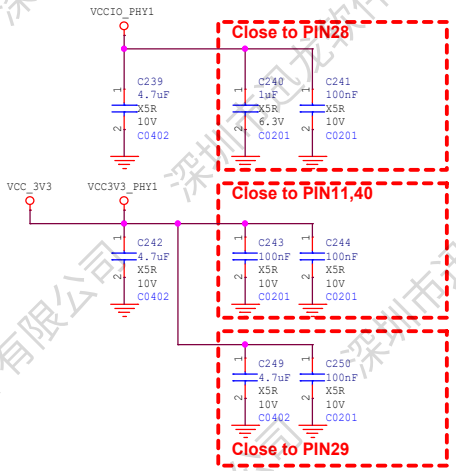






RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V(default)	1'b0	2'b10





Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	18.Ethernet-GEPHY_RGMII				
Date:	Monday, May 27, 2024			Rev:	V2.1
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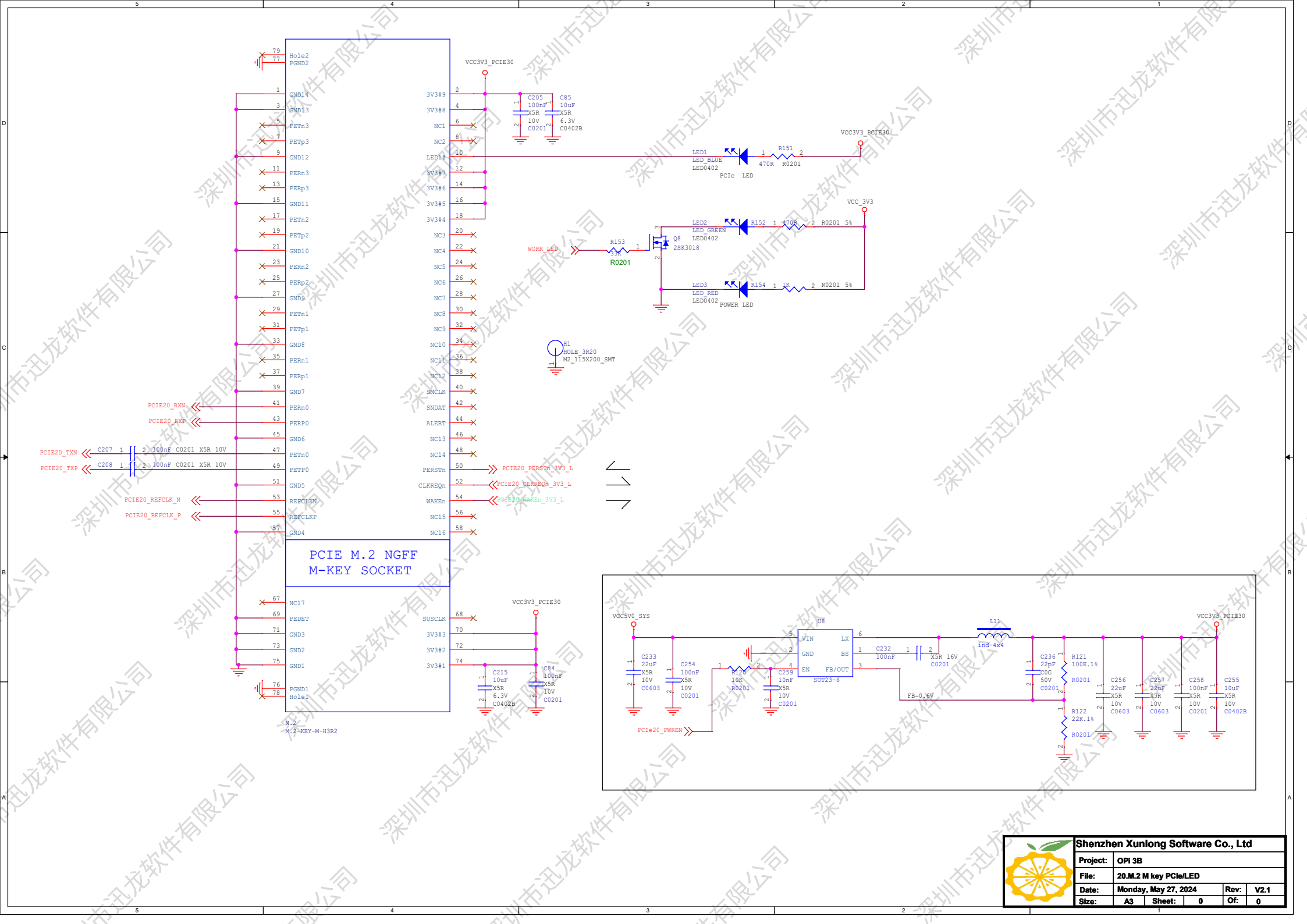
PCIE M.2 NGFF
M-KEY SOCKET
M.2
M.2-KEY-M-H3R2
VCC3V3_PCIE30
VCC_3V3
VCC5V0_SYS
PCIE20_RXN
PCIE20_RXP
PCIE20_TXN
PCIE20_TXP
PCIE20_REFCLK_N
PCIE20_REFCLK_P
PCIE20_PERSTn_3V3_L
PCIE20_CLKREQn_3V3_L
PCIE20_WAKEn_3V3_L
WORK_LED
PCIe LED
POWER LED
PCIe20_PWREN
FB=0.6V
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 20.M.2 M key PCIe/LED
Date: Monday, May 27, 2024
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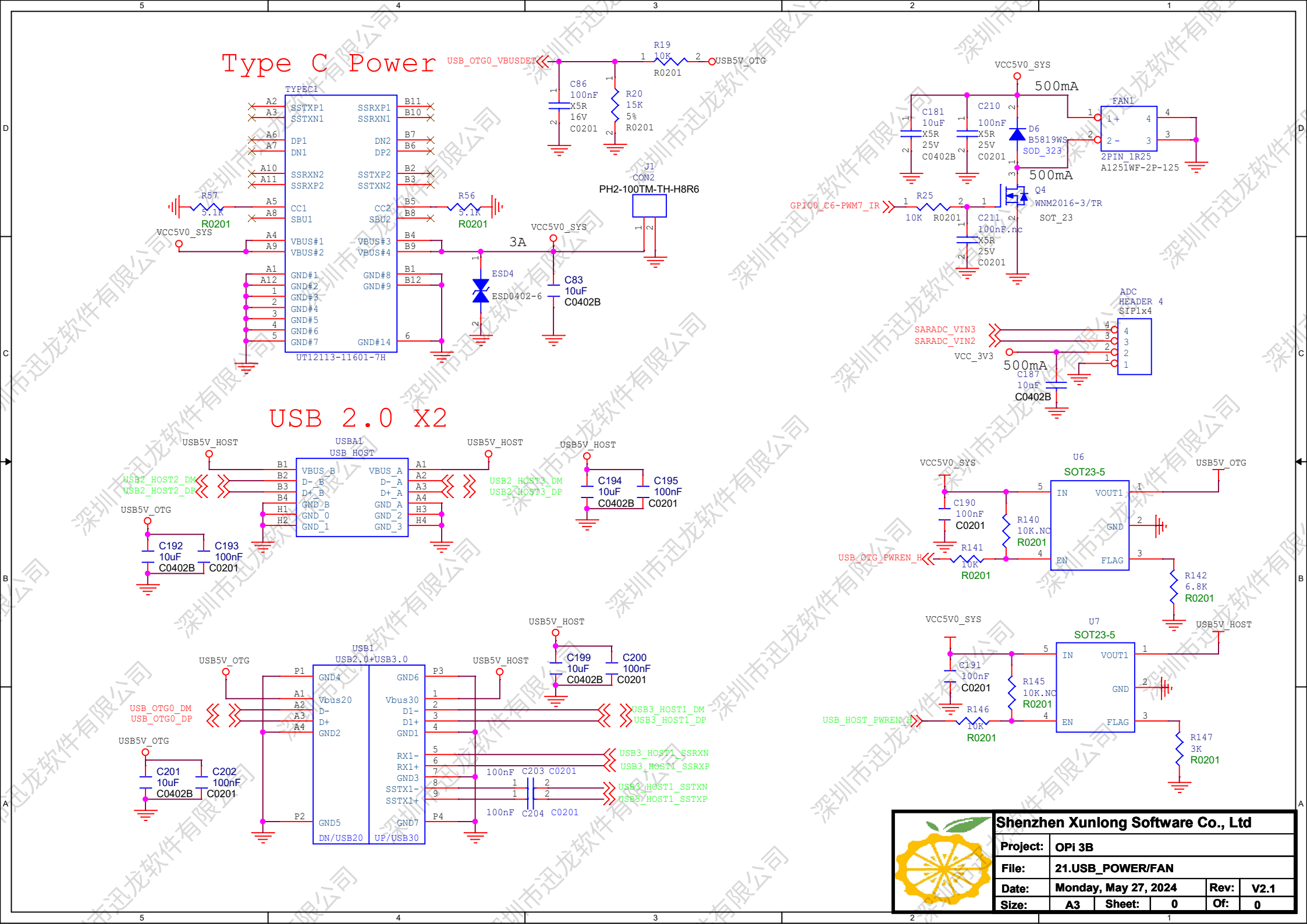
Type C Power
TYPEC1
UT12113-11601-7H
USB_OTG0_VBUSDET
R19
10K
R0201
USB5V_OTG
C86
100nF
X5R
16V
C0201
R20
15K
5%
R0201
J1
CON2
PH2-100TM-TH-H8R6
R57
5.1K
R0201
R56
5.1K
R0201
VCC5V0_SYS
3A
ESD4
ESD0402-6
C83
10uF
C0402B
VCC5V0_SYS
500mA
C181
10uF
X5R
25V
C0402B
C210
100nF
X5R
25V
C0201
D6
B5819WS
SOD_323
FAN1
2PIN_1R25
A1251WF-2P-125
500mA
Q4
WNM2016-3/TR
SOT_23
GPIO0_C6-PWM7_IR
R25
10K
R0201
C211
100nF.nc
X5R
25V
C0201
ADC
HEADER 4
SIP1x4
SARADC_VIN3
SARADC_VIN2
VCC_3V3
500mA
C187
10uF
C0402B
USB 2.0 X2
USBA1
USB_HOST
USB5V_HOST
USB2_HOST2_DM
USB2_HOST2_DP
USB2_HOST3_DM
USB2_HOST3_DP
C192
10uF
C0402B
C193
100nF
C0201
C194
10uF
C0402B
C195
100nF
C0201
USB1
USB2.0+USB3.0
USB_OTG0_DM
USB_OTG0_DP
C201
10uF
C0402B
C202
100nF
C0201
C199
10uF
C0402B
C200
100nF
C0201
USB3_HOST1_DM
USB3_HOST1_DP
USB3_HOST1_SSRXN
USB3_HOST1_SSRXP
USB3_HOST1_SSTXN
USB3_HOST1_SSTXP
100nF C203 C0201
100nF C204 C0201
U6
SOT23-5
C190
100nF
C0201
R140
10K.NC
R0201
R141
10K
R0201
USB_OTG_PWREN_H
R142
6.8K
R0201
U7
SOT23-5
C191
100nF
C0201
R145
10K.NC
R0201
R146
10K
R0201
USB_HOST_PWREN_H
R147
3K
R0201
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 21.USB_POWER/FAN
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