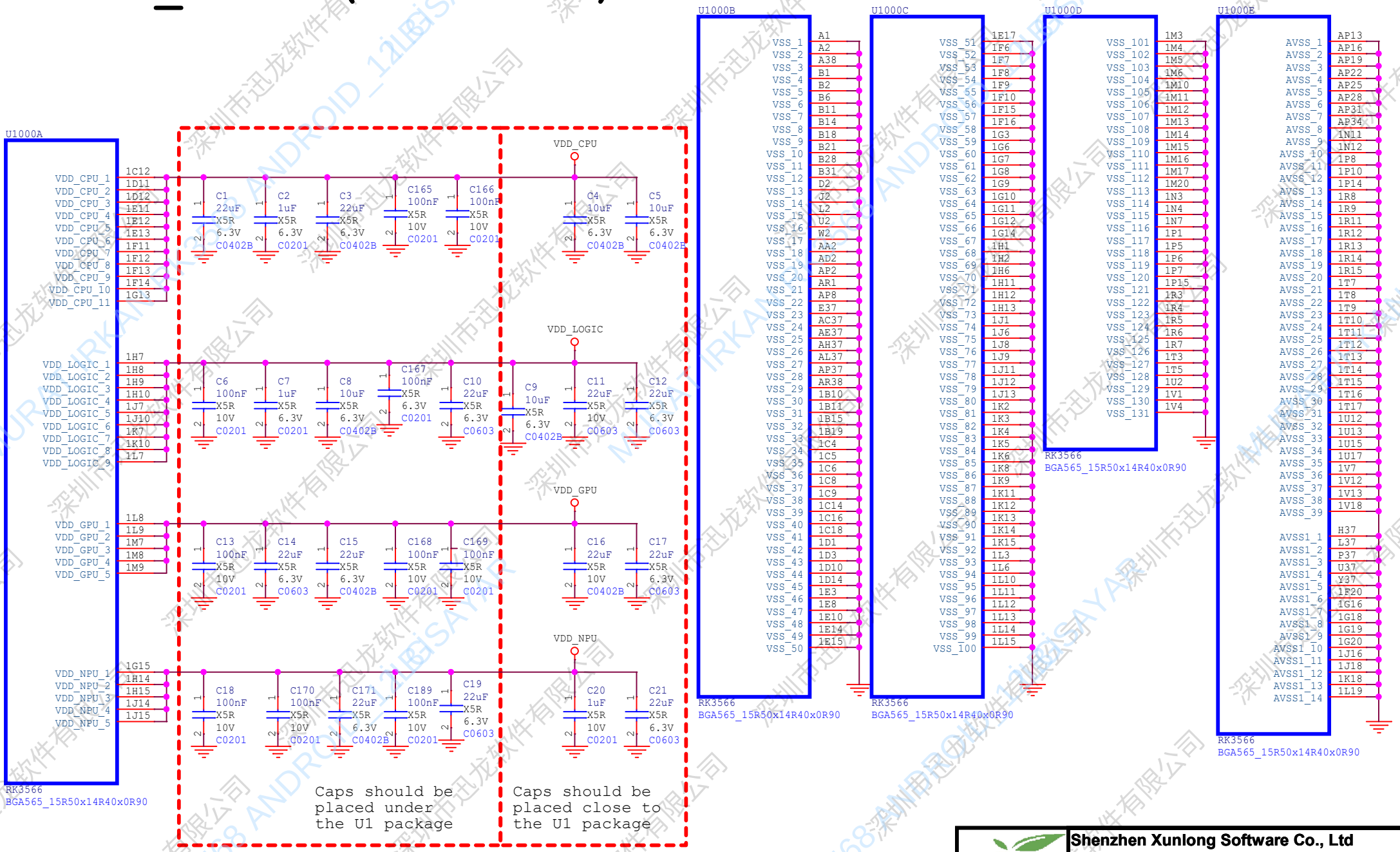
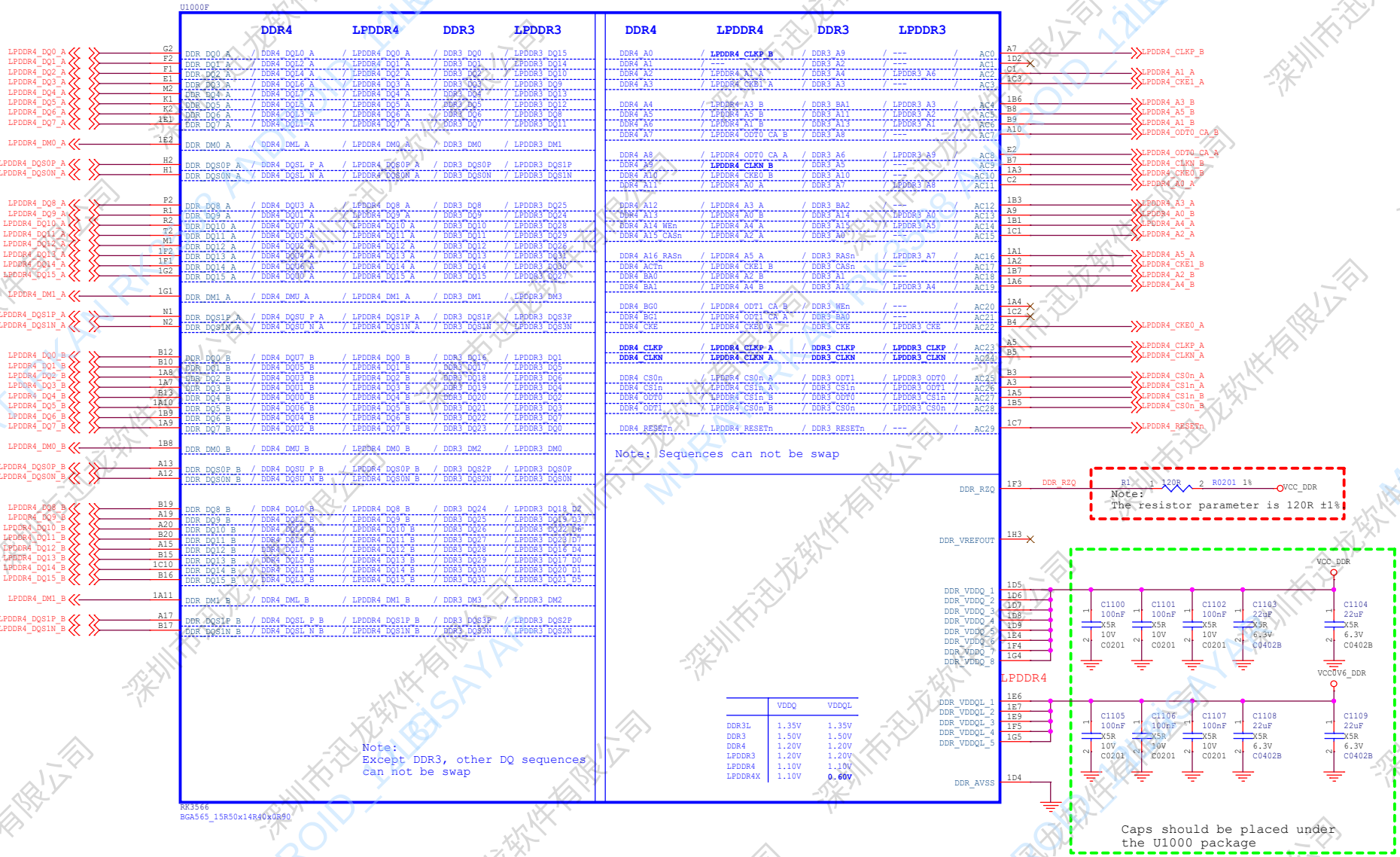
RK3566_ABCDE (Power&GND)



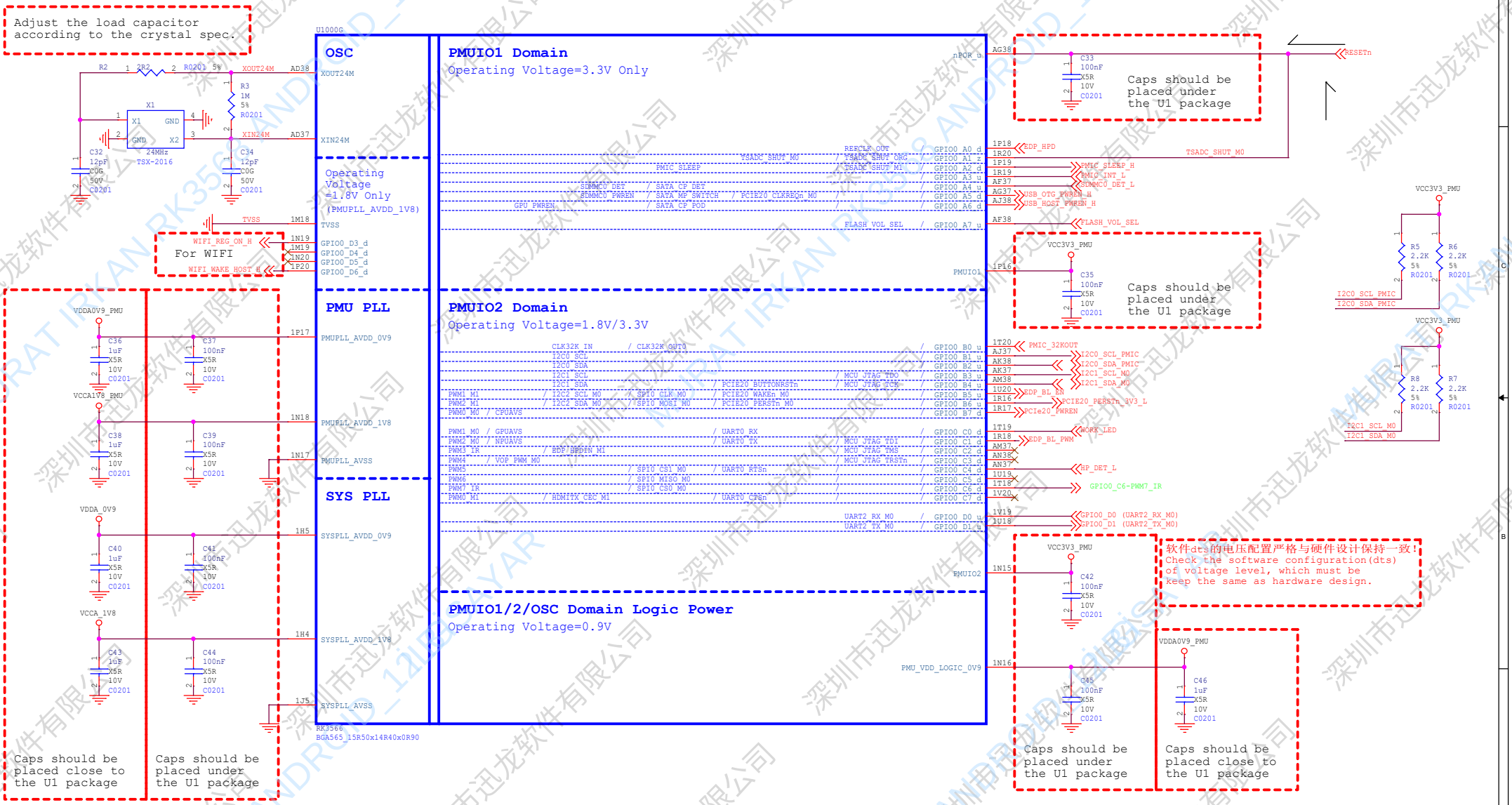
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	01.RK3566_Power/GND				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_F(DDR PHY)



Shenzhen Xunlong Software Co., Ltd	
Project:	OPi 3B
File:	02.RK3566_DDR_PHY
Date:	Monday, May 27, 2024
Rev:	V2.1
Size:	A3
Sheet:	0
Of:	0

RK3566_G(OSC/PLL/PMUIO1/2)



Shenzhen Xunlong Software Co., Ltd	
Project:	OPi 3B
File:	03.RK3566_OSC/PLL/PMUIO
Date:	Monday, May 27, 2024
Rev:	V2.1
Size:	A3
Sheet:	0
Of:	0

RK3566_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0/FLASH_D0
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1/FLASH_D1
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2/FLASH_D2
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3/FLASH_D3
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4/FLASH_D4
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5/FLASH_D5
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6/FLASH_D6
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7/FLASH_D7
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD/FLASH_WRn
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	eMMC_CLKOUT/FLASH_DQS
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE/FLASH_CLE
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	eMMC_RSTn/FSPI_D2/FLASH_WPn
	FSPI_CLK / FLASH_ALE	/ GPIO1_D0_d	1A15	FSPI_CLK/FLASH_ALE
	FSPI_D0 / FLASH_RDY	/ GPIO1_D1_u	1A17	FSPI_D0/FLASH_RDY
	FSPI_D1 / FLASH_RDn	/ GPIO1_D2_u	1A18	FSPI_D1/FLASH_RDn
	FSPI_CS0n / FLASH_CS0n	/ GPIO1_D3_u	1B17	FSPI_CS0n/FLASH_CS0n
	FSPI_D3 / FLASH_CS1n	/ GPIO1_D4_u	1C15	FSPI_D3/FLASH_CS1n

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2

RK3566
BGA565_15R50x14R40x0R90

1C13

VCCIO_FLASH

C47 100nF X5R 10V C0201

1.8V

Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

TP5 eMMC_D0/FLASH_D0 TP100

TP7 FSPI_CLK/FLASH_ALE TP100

D2 B5819WS SOD_323

D4 B5819WS SOD_323

eMMC_D0/FLASH_D0

FSPI_CLK/FLASH_ALE

BOOT BOOT-SW T2Key

C196 100nF X5R 50V C0201

1. eMMC or Nand Flash:
   Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

2. SPI Flash:
   Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

RK3566_J(VCCIO3 Domain)

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1 / SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	SDMMC0_D0
PWM9_M1 / SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	SDMMC0_D1
SDMMC0_D2	/ ARM_JTAG_TCK/ UART5_CTSn_M0	/ GPIO1_D7_u	1D20	SDMMC0_D2
SDMMC0_D3	/ ARM_JTAG_TMS/ UART5_RTSn_M0	/ GPIO2_A0_u	1F18	SDMMC0_D3
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	1E19	SDMMC0_CMD
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ GPIO2_A2_d	G38	SDMMC0_CLK

VCCIO3

RK3566
BGA565_15R50x14R40x0R90

R23 0R R0201

C227 NC X5R 16V C0201

VCCIO_SD

1F17

C50 100nF X5R 10V C0201

Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

default VCC = VCCIO_FLASH 1.8V

U2
XM25QU128CWIQT08Q
wson-6x5-mm

FSPI_CS0n/FLASH_CS0n
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn

CS DO(D1) WP(D2) VSS VCC HOLD(D3) CLK DI(D0) EPAD

R12 10K R0201

R13 10K R0201

VCCIO_FLASH

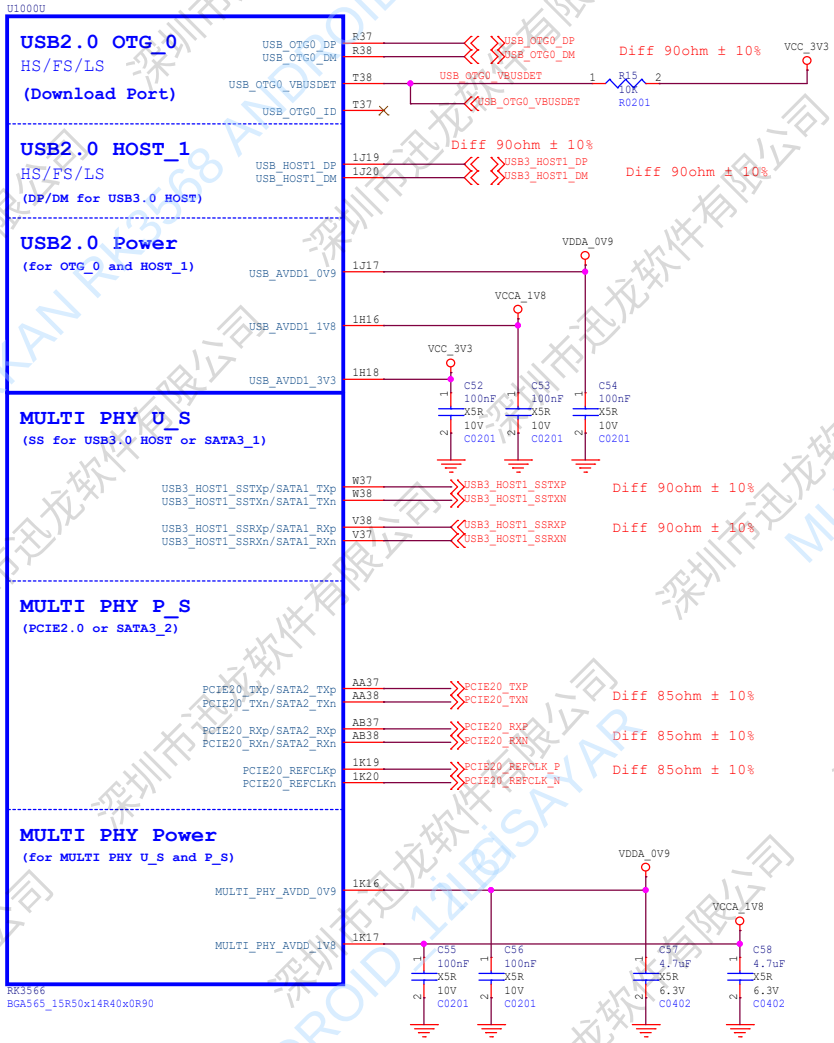
FSPI_D3/FLASH_CS1n
FSPI_CLK/FLASH_ALE
FSPI_D0/FLASH_RDY

C48 100nF X5R 10V C0201

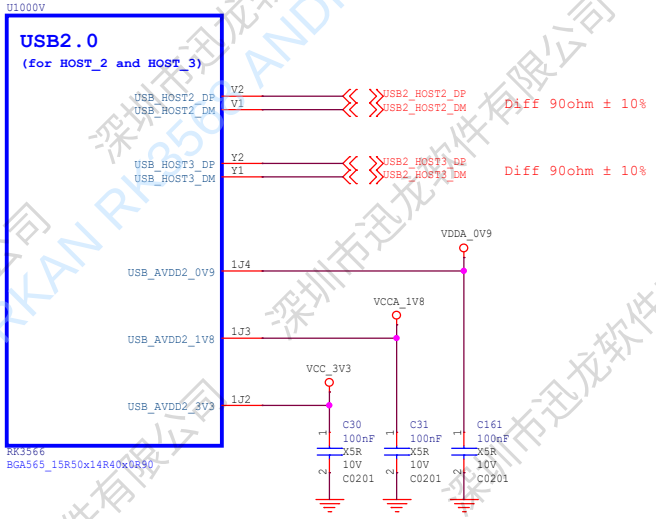
C49 1uF X5R 6.3V C0201

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	04.RK3566_Flash/SD_Contr				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_U(USB3.0/PCIe2.0x1/SATA)

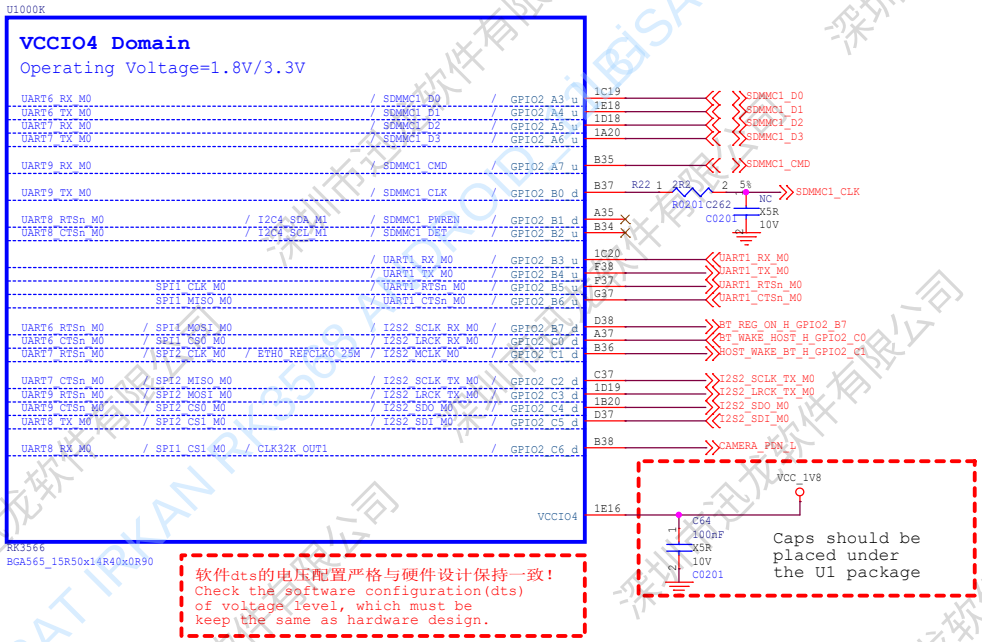


RK3566_V(USB2.0 HOST)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	05.RK3566_USB/PCIe/SATA_PHY				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_K(VCCIO4 Domain)

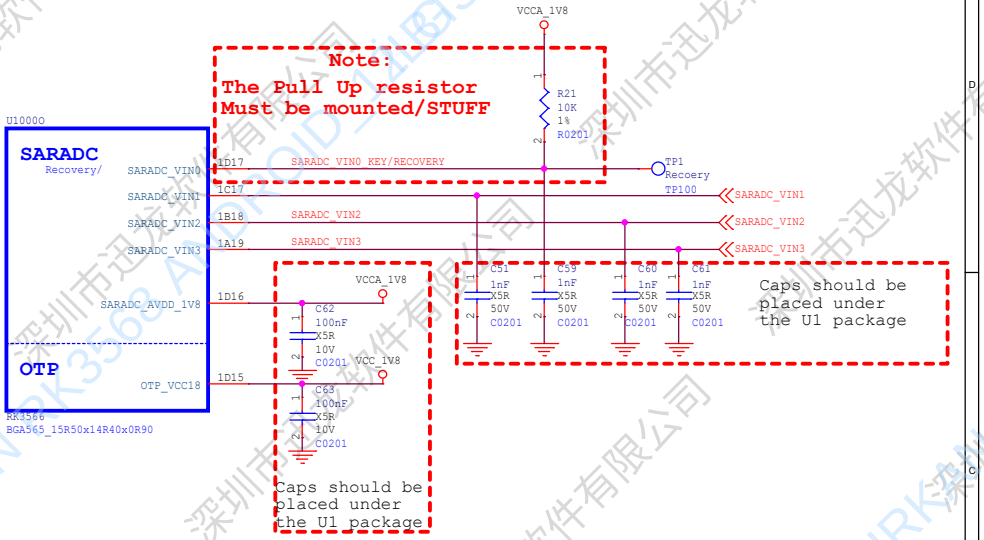


软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

RK3566_N(VCCIO7 Domain)

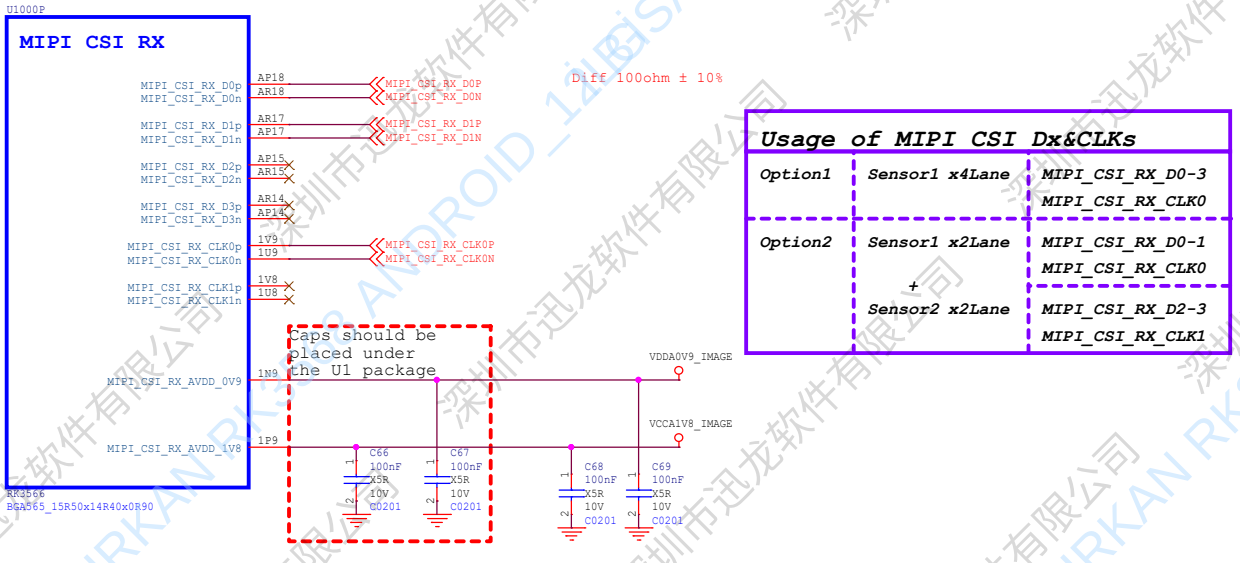
软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

RK3566_O(SARADC/OTP)



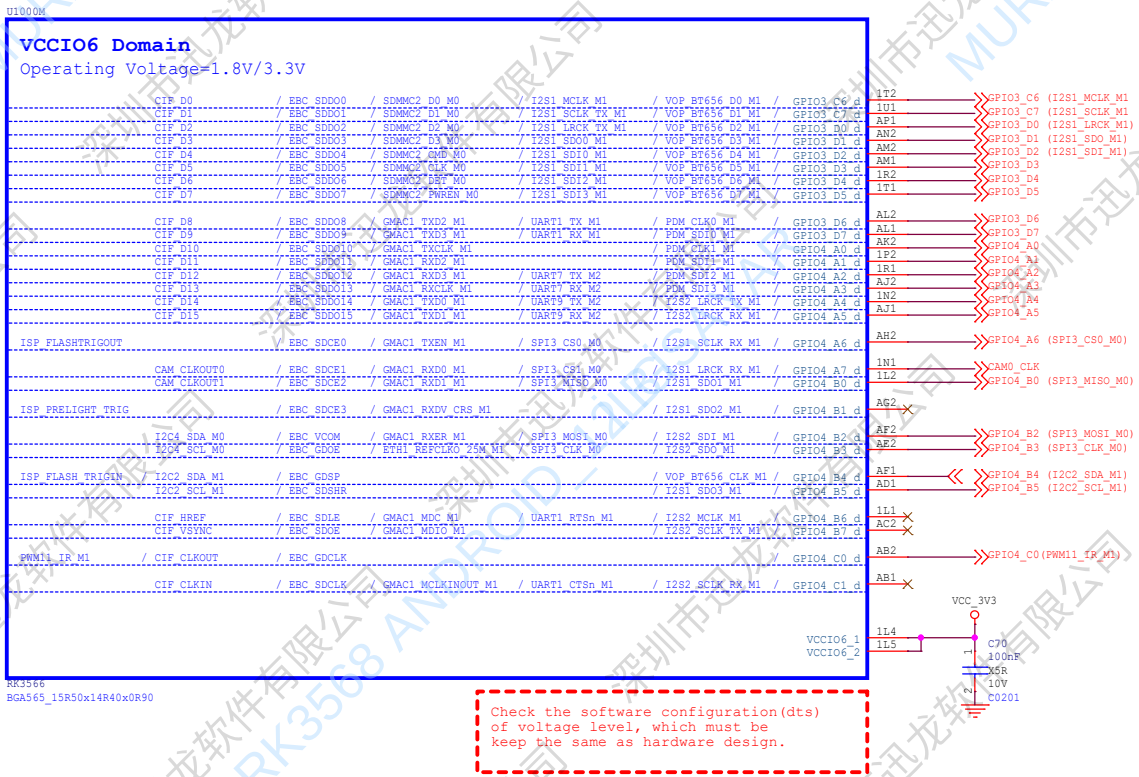
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	06.RK3566_SARADC/GPIO				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_P(MIPI_CSI_RX)

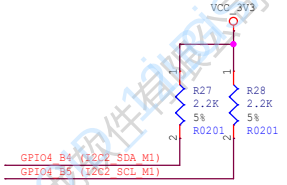


Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566_M(VCCIO6 Domain)

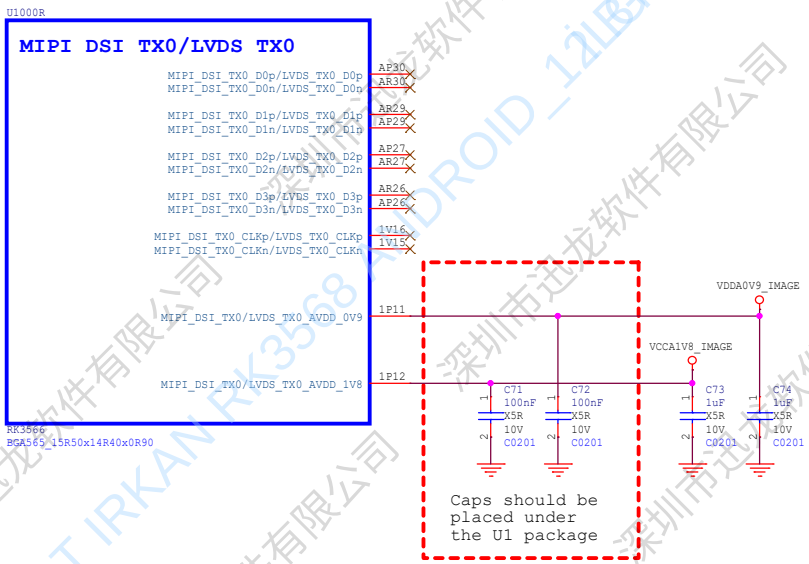


Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

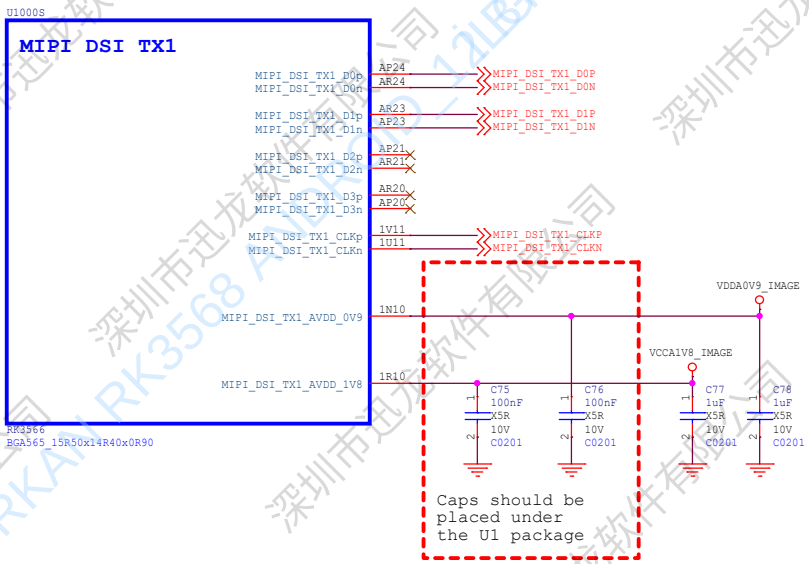


Shenzhen Xunlong Software Co., Ltd				
Project:	OPi 3B			
File:	07.RK3566_CSI/GPIO			
Date:	Monday, May 27, 2024		Rev:	V2.1
Size:	A3	Sheet: 0	Of:	0

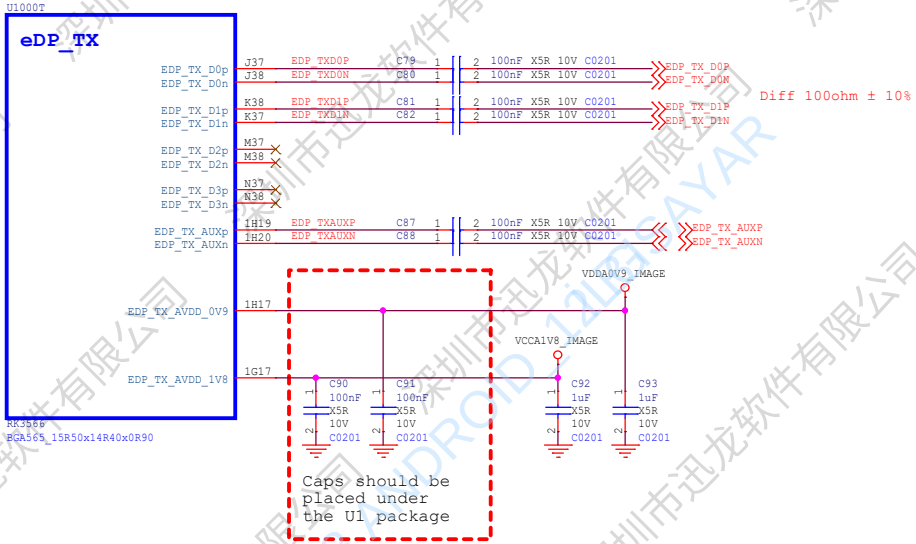
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



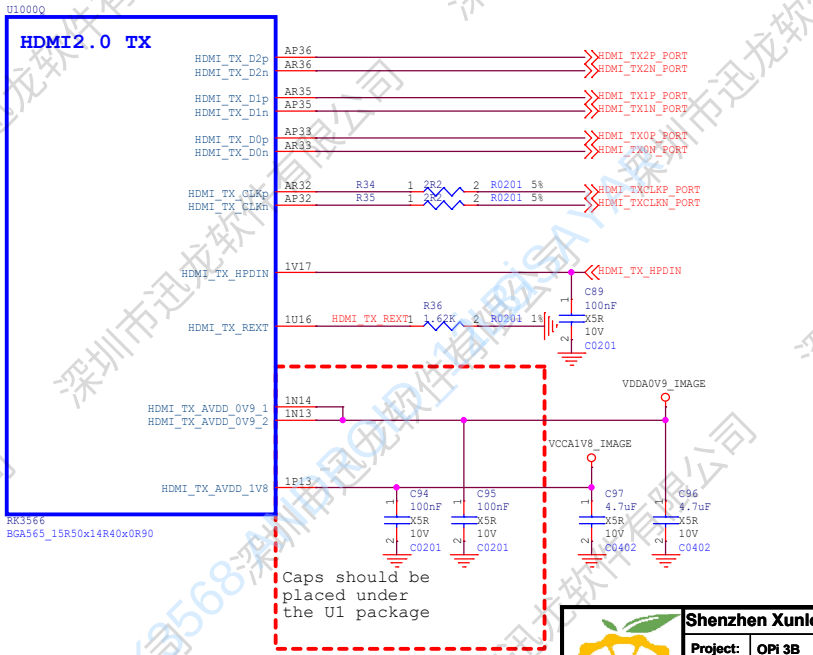
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	08.RK3566_LVDS_MIPI				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1			/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0			/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0			/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1		/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3566
BGA565_15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

1U5 AR10 GMAC1_TXD2_M0
AP10 GMAC1_TXD3_M0
AR9 GMAC1_RXD2_M0
AP9 GMAC1_RXD3_M0
1U4 GMAC1_TXCLK_M0
1V3 GMAC1_RXCLK_M0

AR7
AP7 GMAC1_RXD0_M0
AR6 GMAC1_RXD1_M0
AP6 GMAC1_RXDV_CRS_M0
1U3
1T4 GMAC1_TXD0_M0
1V2 GMAC1_TXD1_M0
AP5 GMAC1_TXEN_M0

AR4 GMAC1_MCLKINOUT_M0
AP4
AP3
AR2

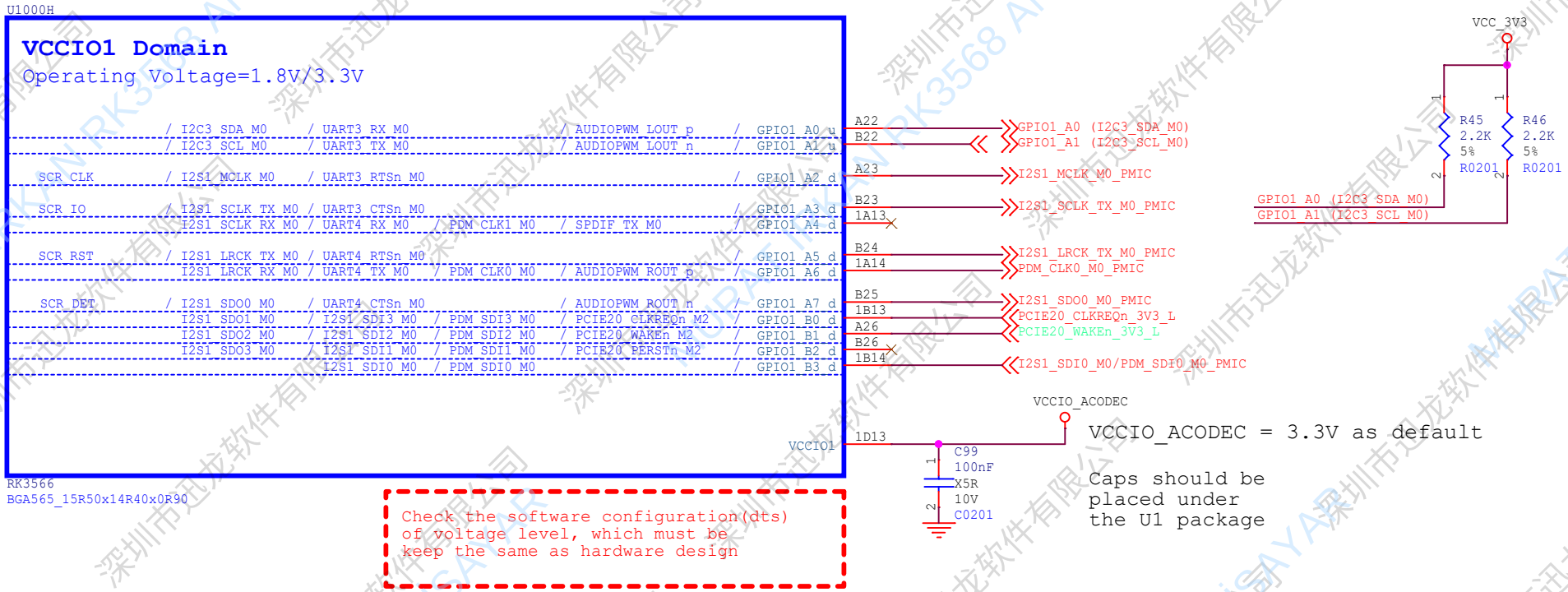
1P3 GMAC1_MDC_M0
1P4 GMAC1_MDIO_M0

1N5
1N6

VCCIO5 V1.2 VCCIO_PHY1
R119 1 0R 2
R0201
C98 100nF X5R 10V C0201
Caps should be placed under the U1 package

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	09.RK3566_GMAC				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

RK3566_H(VCCIO1 Domain)

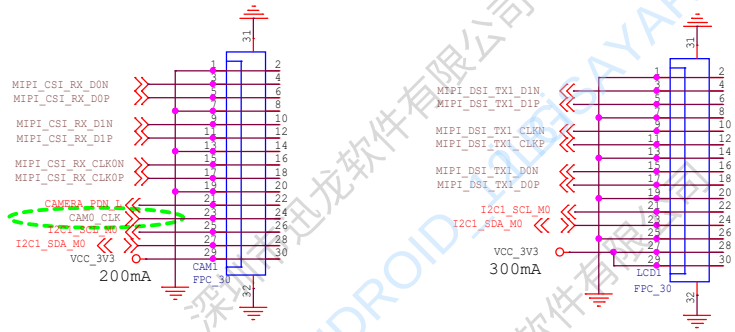


VCCIO_ACODEC = 3.3V as default

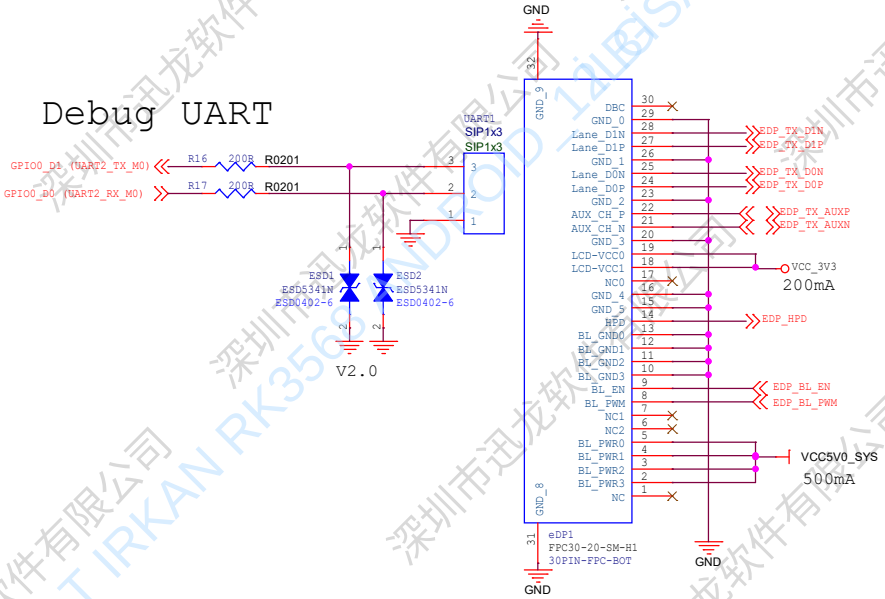
Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	10.RK3566_Audio_Interface				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

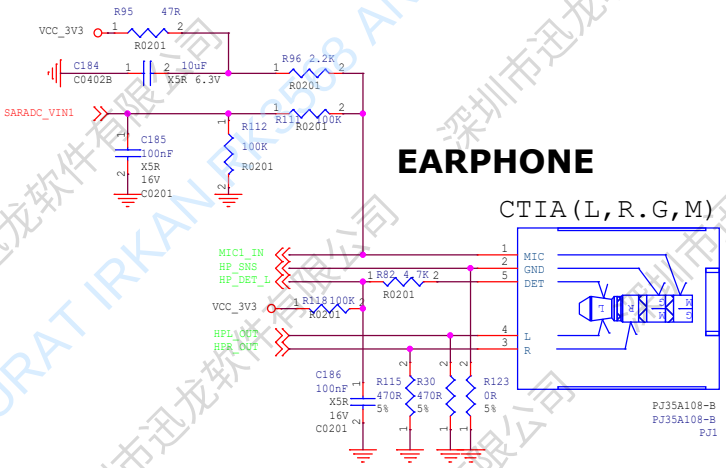


Debug UART



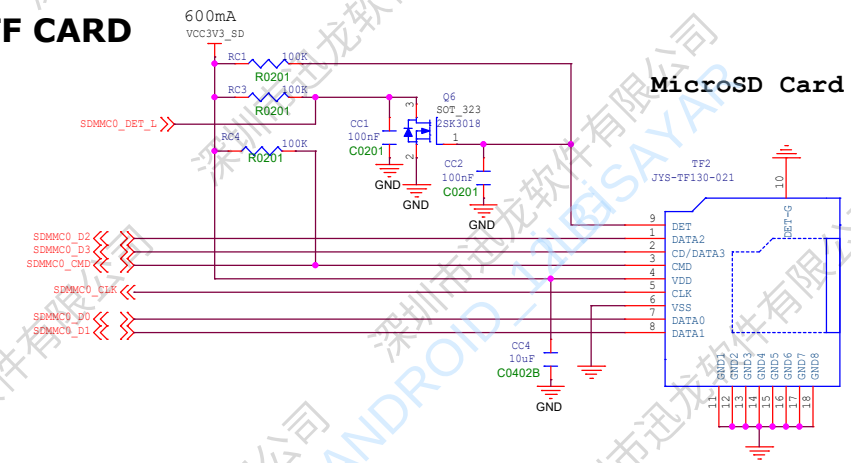
EARPHONE

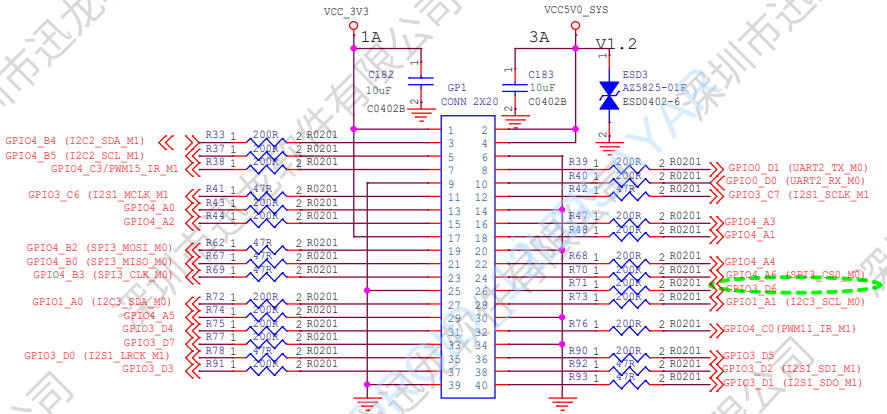
CTIA(L,R.G,M)



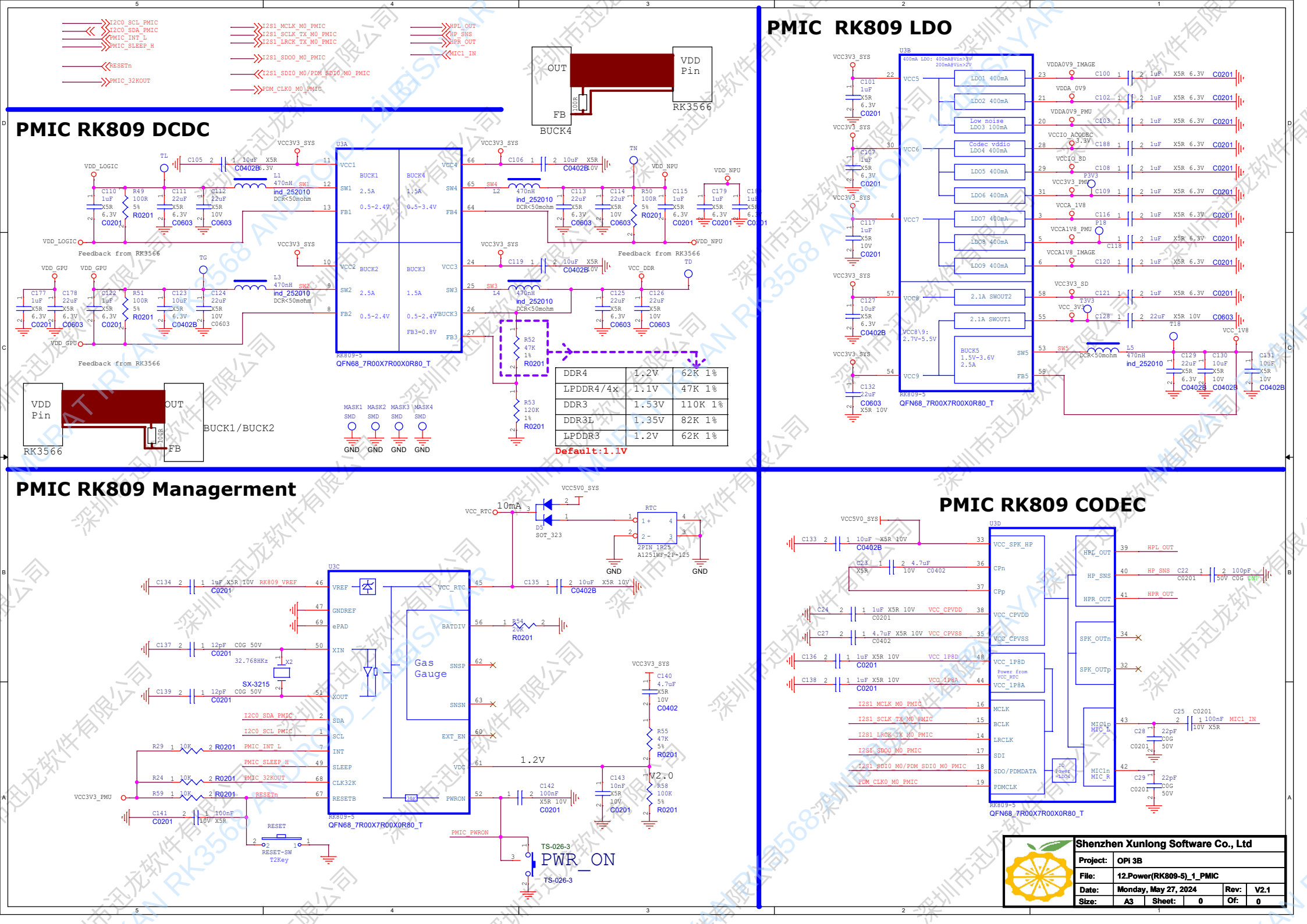
TF CARD

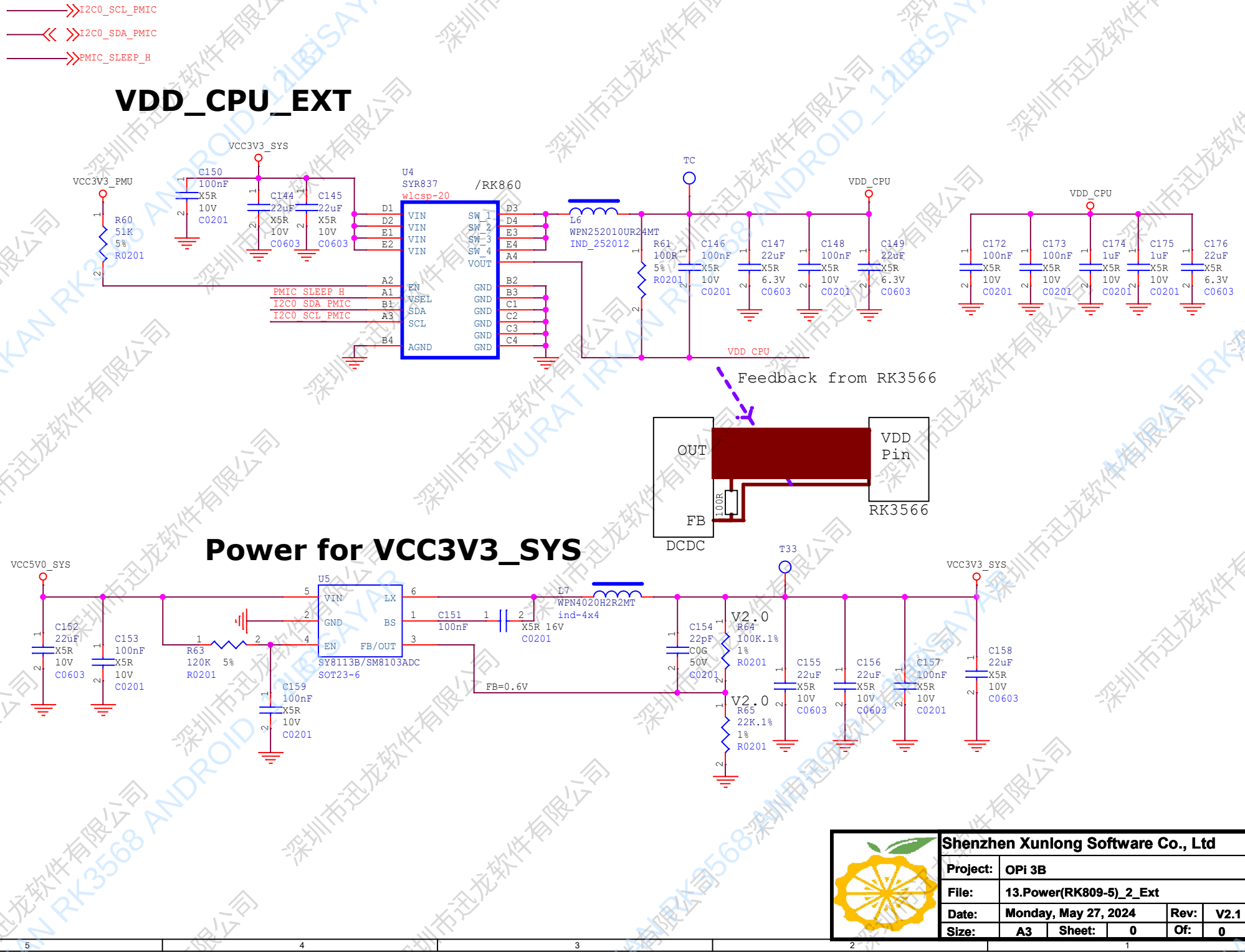
MicroSD Card





Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	11.IO_CON				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0


I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RESETn
PMIC_32KOUT
I2S1_MCLK_M0_PMIC
I2S1_SCLK_TX_M0_PMIC
I2S1_LRCK_TX_M0_PMIC
I2S1_SDO0_M0_PMIC
I2S1_SDI0_M0/PDM_SDI0_M0_PMIC
PDM_CLK0_M0_PMIC
HPL_OUT
HP_SNS
HPR_OUT
MIC1_IN
OUT
VDD Pin
FB
100R
RK3566
BUCK4
PMIC RK809 DCDC
VCC3V3_SYS
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
Feedback from RK3566
U3A
RK809-5
QFN68_7R00X7R00X0R80_T
BUCK1/BUCK2
MASK1 MASK2 MASK3 MASK4
SMD
GND
DDR4 1.2V 62K 1%
LPDDR4/4x 1.1V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.2V 62K 1%
Default:1.1V
PMIC RK809 LDO
U3B
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V~3.6V 2.5A
VCC8\9: 2.7V~5.5V
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_1V8
PMIC RK809 Managerment
VCC5V0_SYS
VCC_RTC
10mA
D5
SOT_323
RTC
2PIN_1R25
A1251WF-2P-125
U3C
VREF
GNDREF
ePAD
XIN
XOUT
SX-3215
32.768HKz
X2
Gas Gauge
SDA
SCL
INT
SLEEP
CLK32K
RESETB
BATDIV
SNSP
SNSN
EXT_EN
VDD
PWRON
I2C0_SDA_PMIC
I2C0_SCL_PMIC
PMIC_INT_L
PMIC_SLEEP_H
PMIC_32KOUT
RESETn
VCC3V3_PMU
RESET
RESET-SW
T2Key
1.2V
V2.0
PMIC_PWRON
TS-026-3
PWR_ON
PMIC RK809 CODEC
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p
MIC1n
MIC_L
MIC_R
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 12.Power(RK809-5)_1_PMIC
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
Of: 0


I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_EXT
VCC3V3_SYS
VCC3V3_PMU
C150
100nF
X5R
10V
C0201
C144
22uF
X5R
10V
C0603
C145
22uF
X5R
10V
C0603
R60
51K
5%
R0201
U4
SYR837
wlcsp-20
/RK860
D1
D2
E1
E2
VIN
VIN
VIN
VIN
A2
A1
B1
A3
B4
EN
VSEL
SDA
SCL
AGND
SW_1
SW_2
SW_3
SW_4
VOUT
GND
D3
D4
E3
E4
A4
B2
B3
C1
C2
C3
C4
PMIC_SLEEP_H
I2C0_SDA_PMIC
I2C0_SCL_PMIC
L6
WPN252010UR24MT
IND_252012
TC
R61
100R
5%
R0201
C146
100nF
X5R
10V
C0201
C147
22uF
X5R
6.3V
C0603
C148
100nF
X5R
10V
C0201
C149
22uF
X5R
6.3V
C0603
VDD_CPU
VDD_CPU
C172
100nF
X5R
10V
C0201
C173
100nF
X5R
10V
C0201
C174
1uF
X5R
10V
C0201
C175
1uF
X5R
10V
C0201
C176
22uF
X5R
6.3V
C0603
VDD_CPU
Feedback from RK3566
OUT
FB
100R
VDD
Pin
RK3566
DCDC
Power for VCC3V3_SYS
VCC5V0_SYS
C152
22uF
X5R
10V
C0603
C153
100nF
X5R
10V
C0201
R63
120K
5%
R0201
C159
100nF
X5R
10V
C0201
U5
VIN
GND
EN
LX
BS
FB/OUT
SY8113B/SM8103ADC
SOT23-6
C151
100nF
X5R 16V
C0201
L7
WPN4020H2R2MT
ind-4x4
T33
FB=0.6V
C154
22pF
C0G
50V
C0201
V2.0
R64
100K.1%
1%
R0201
V2.0
R65
22K.1%
1%
R0201
C155
22uF
X5R
10V
C0603
C156
22uF
X5R
10V
C0603
C157
100nF
X5R
10V
C0201
C158
22uF
X5R
10V
C0603
VCC3V3_SYS
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 13.Power(RK809-5)_2_Ext
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
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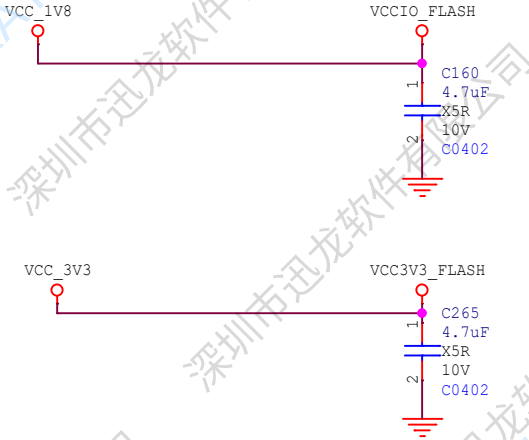
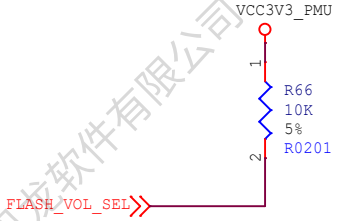
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=L(Default)





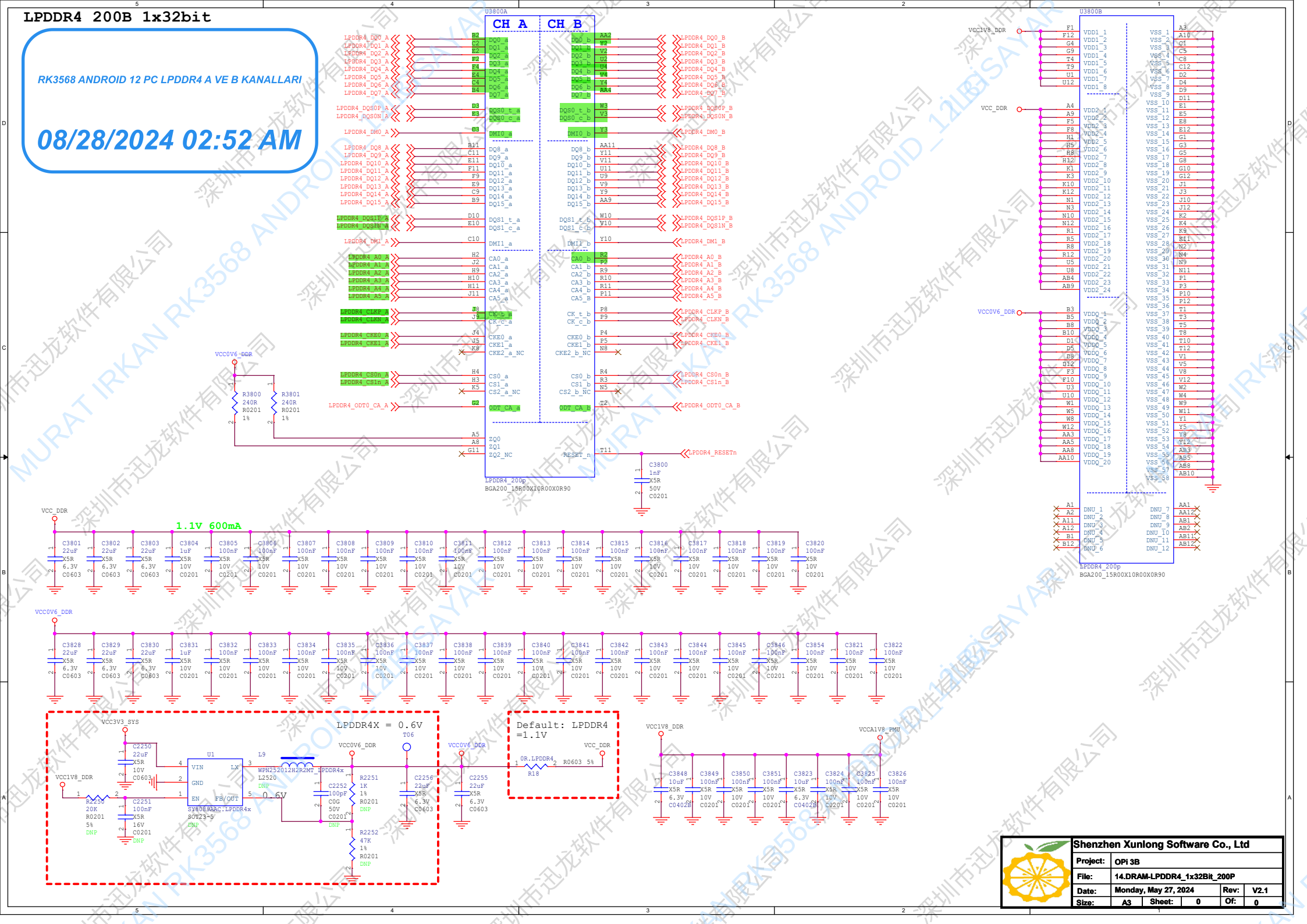
RK3568
UBUNTU LINUX
8GB LPDDR4
PC

unlong Software Co., Ltd			
3B			
ower_Flash_Power_Manage			
day, May 27, 2024		Rev:	V2.1
	Sheet: 0	Of:	0

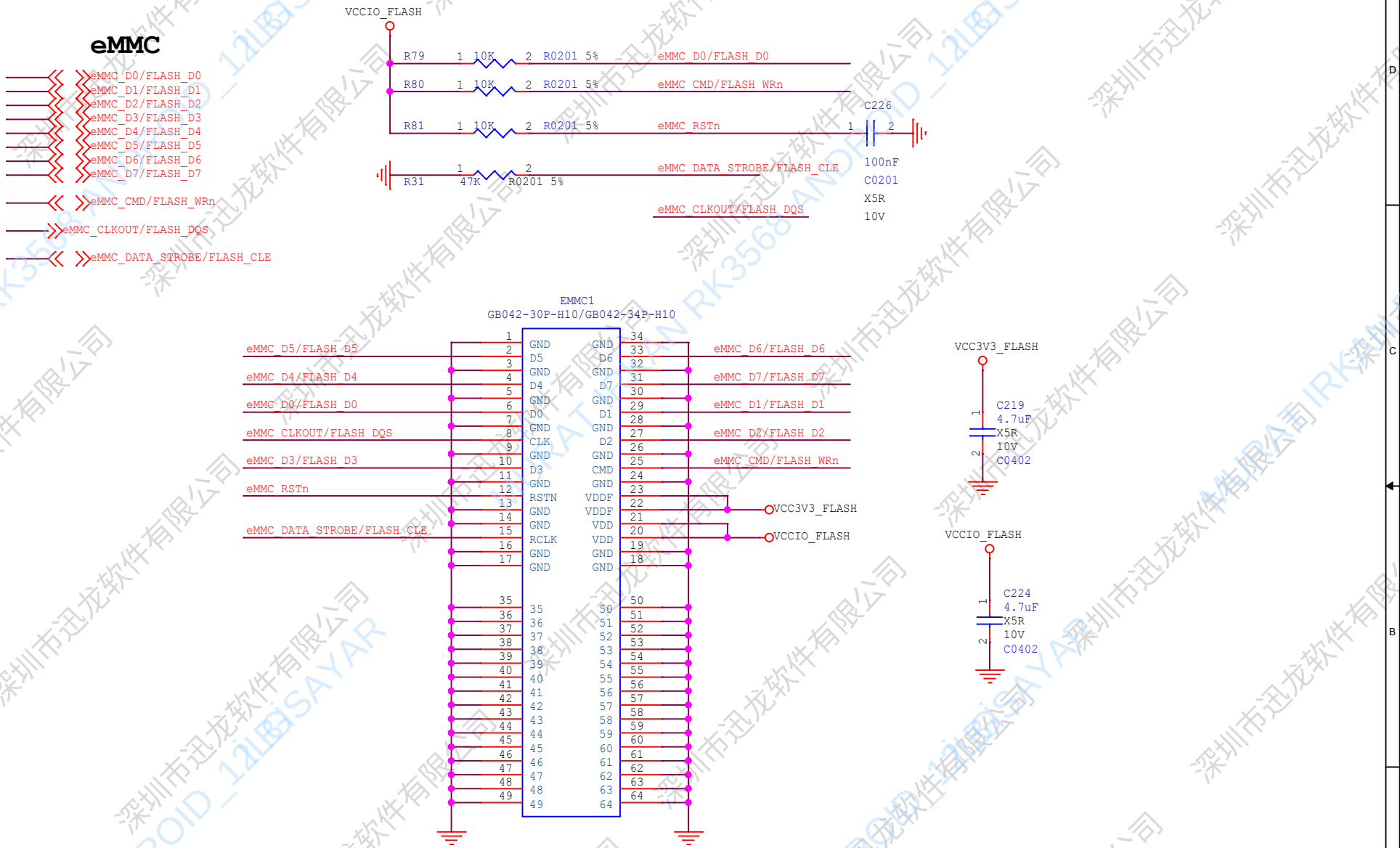
LPDDR4 200B 1x32bit

RK3568 ANDROID 12 PC LPDDR4 A VE B KANALLARI

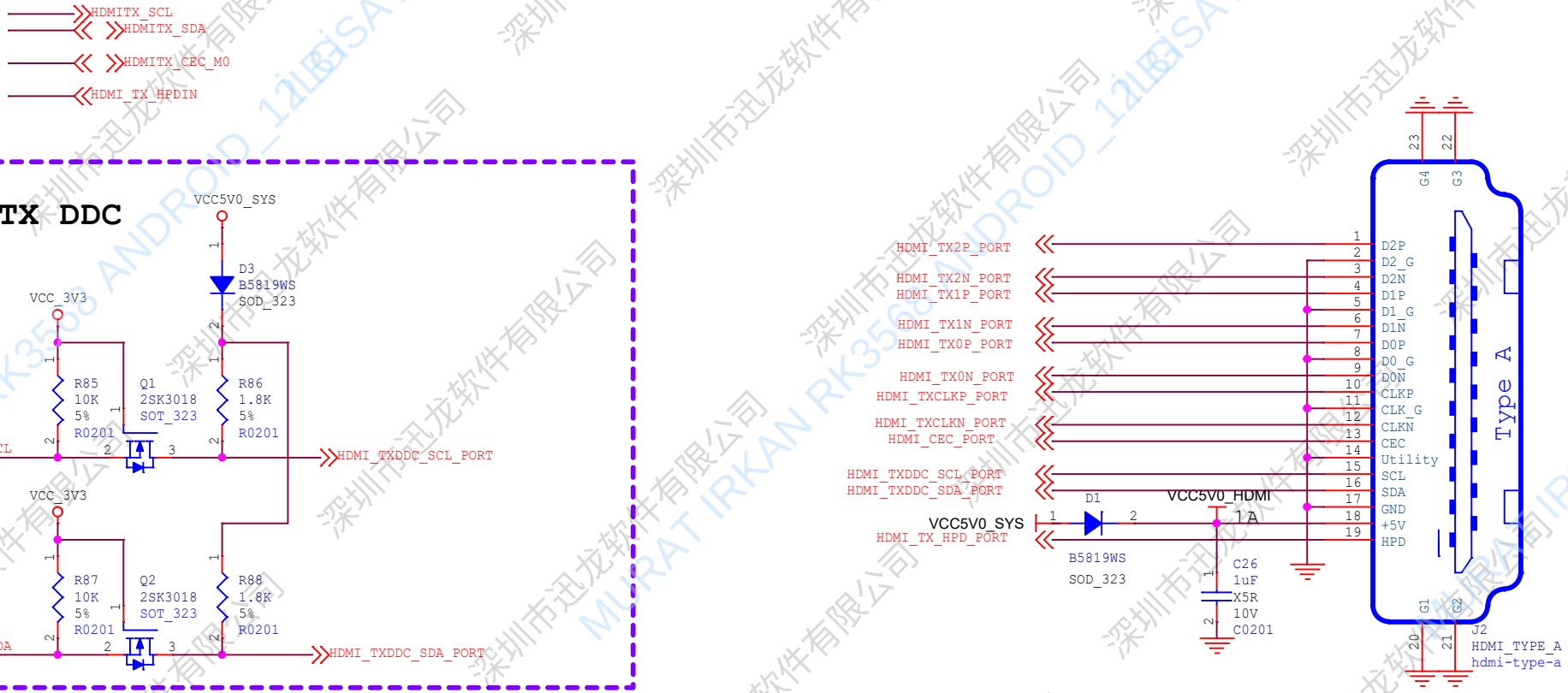
08/28/2024 02:52 AM



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	14.DRAM-LPDDR4_1x32Bit_200P				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

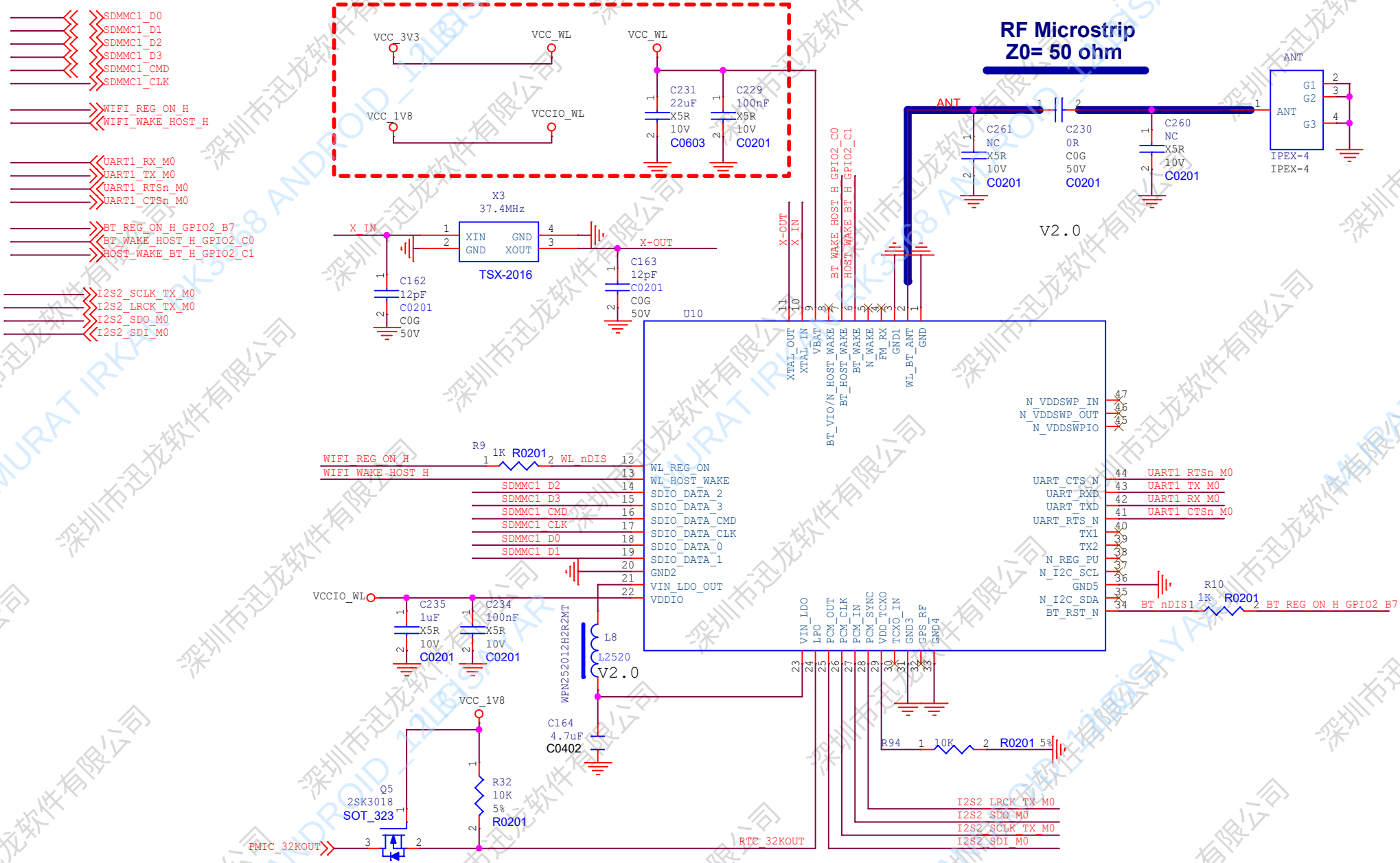


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	15.Flash-eMMC_Flash				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

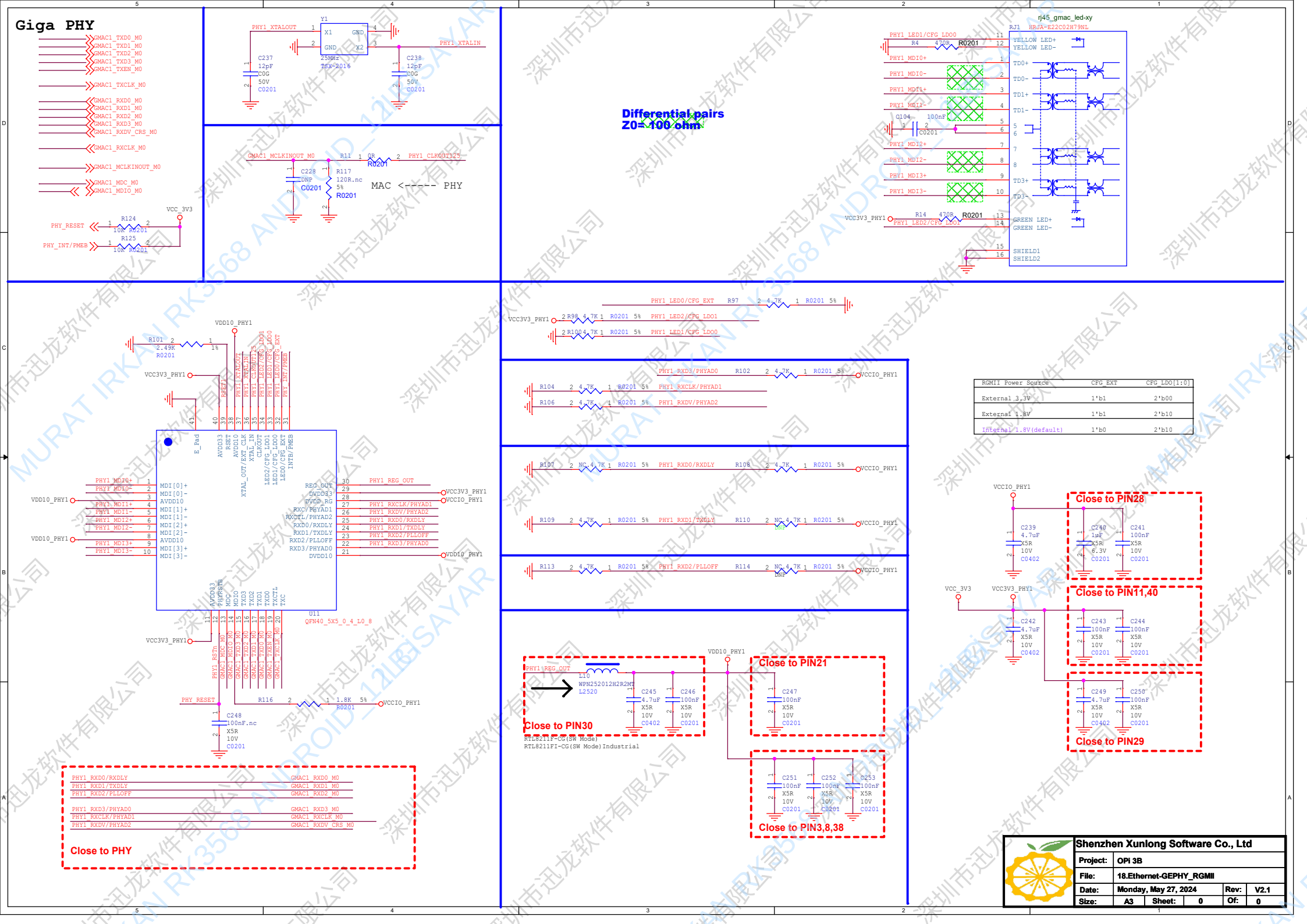


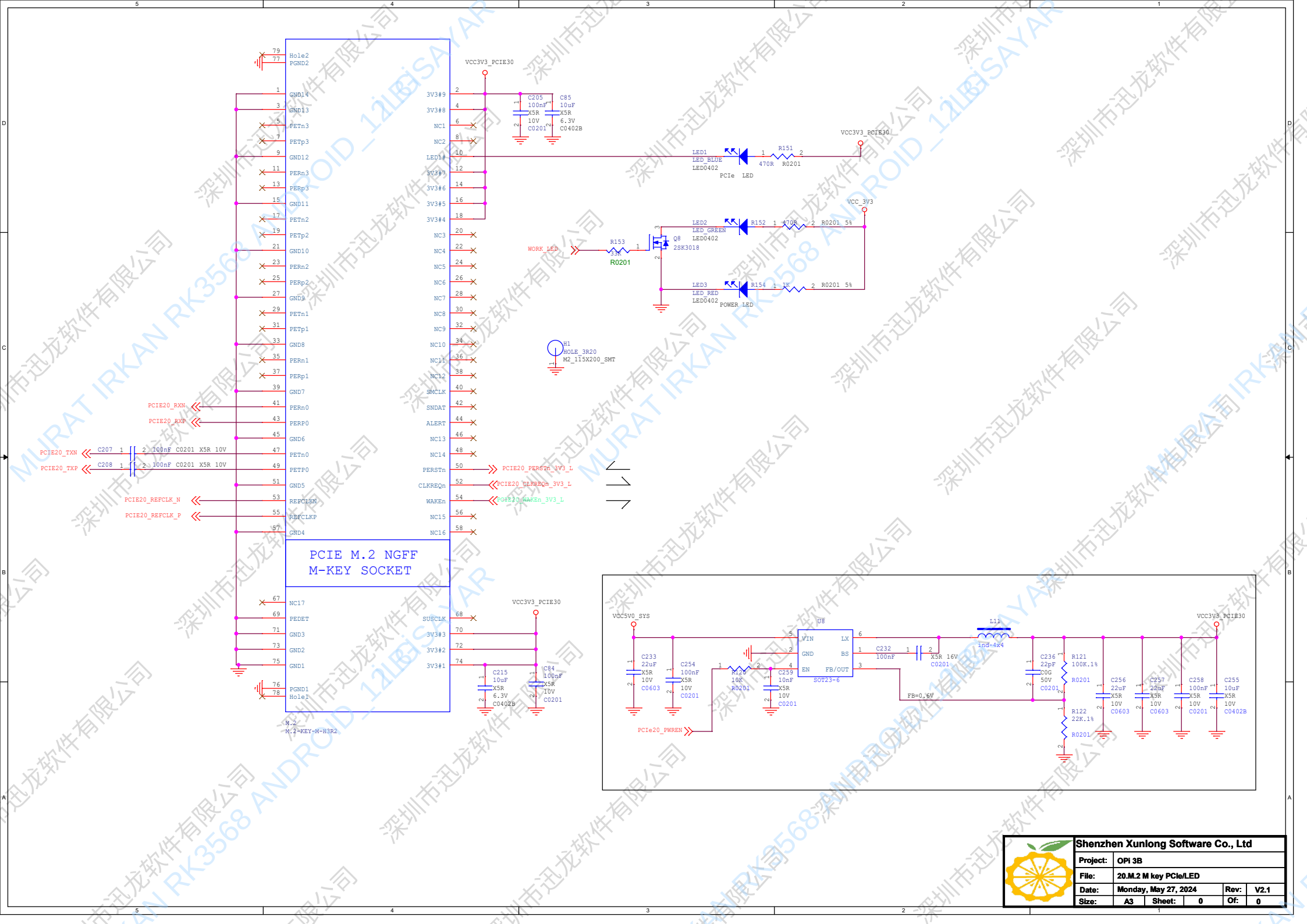
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	16.VO-HDMI2.0_TX				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0

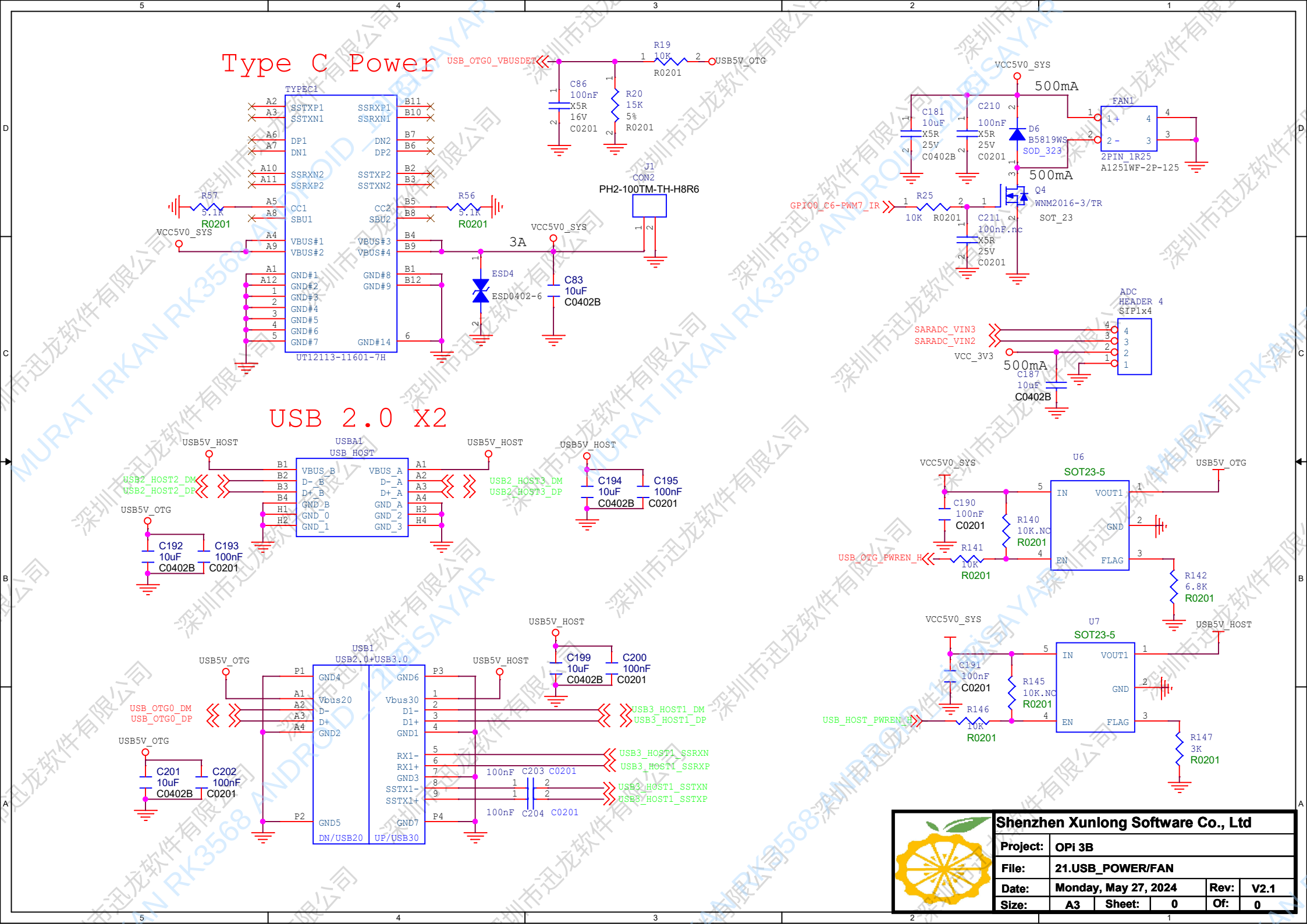
SDIO WIFI/BT Module-1T1R



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 3B				
File:	17.WIFI/BT-SDIO_1T1R+UART				
Date:	Monday, May 27, 2024			Rev:	V2.1
Size:	A3	Sheet:	0	Of:	0


Giga PHY
GMAC1_TXD0_M0
GMAC1_TXD1_M0
GMAC1_TXD2_M0
GMAC1_TXD3_M0
GMAC1_TXEN_M0
GMAC1_TXCLK_M0
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXD2_M0
GMAC1_RXD3_M0
GMAC1_RXDV_CRS_M0
GMAC1_RXCLK_M0
GMAC1_MCLKINOUT_M0
GMAC1_MDC_M0
GMAC1_MDIO_M0
VCC_3V3
PHY_RESET
R124
10M R0201
PHY_INT/PMEB
R125
10M R0201
PHY1_XTALOUT
Y1
X1
GND
X2
25MHz
TSX-2016
PHY1_XTALIN
C237
12pF
C0G
50V
C0201
C238
12pF
C0G
50V
C0201
GMAC1_MCLKINOUT_M0
R11
0R
R0201
PHY1_CLKOUT125
C228
DNP
C0201
R117
120R.nc
5%
R0201
MAC <----- PHY
Differential pairs
Z0= 100 ohm
rj45_gmac_led-xy
RJ1 HRJA-E22C02H79NL
PHY1_LED1/CFG_LDO0
R4 470R R0201
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
C104 100nF
C0201
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
VCC3V3_PHY1
R14 470R R0201
PHY1_LED2/CFG_LDO1
YELLOW LED+
YELLOW LED-
TD0+
TD0-
TD1+
TD1-
TD3+
TD3-
GREEN LED+
GREEN LED-
SHIELD1
SHIELD2
VDD10_PHY1
R101 2.49K R0201
VCC3V3_PHY1
RSET
PHY1_XTALOUT
PHY1_XTALIN
PHY1_CLKOUT125
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
PHY1_LED0/CFG_EXT
PHY1_INT/PMEB
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INT#/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY1_REG_OUT
VCC3V3_PHY1
VCCIO_PHY1
VDD10_PHY1
U11
QFN40_5X5_0_4_L0_8
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
PHY1_RSTn
GMAC1_MDC_M0
GMAC1_MDIO_M0
GMAC1_TXD3_M0
GMAC1_TXD2_M0
GMAC1_TXD1_M0
GMAC1_TXD0_M0
GMAC1_TXEN_M0
GMAC1_TXCLK_M0
PHY_RESET
R116 1.8K 5% R0201
VCCIO_PHY1
C248
100nF.nc
X5R
10V
C0201
Close to PHY
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXD2_M0
GMAC1_RXD3_M0
GMAC1_RXCLK_M0
GMAC1_RXDV_CRS_M0
PHY1_LED0/CFG_EXT R97 4.7K R0201 5%
VCC3V3_PHY1
R98 4.7K R0201 5% PHY1_LED2/CFG_LDO1
R100 4.7K R0201 5% PHY1_LED1/CFG_LDO0
R104 4.7K R0201 5% PHY1_RXCLK/PHYAD1
R106 4.7K R0201 5% PHY1_RXDV/PHYAD2
R102 4.7K R0201 5% VCCIO_PHY1
R107 NC_4.7K R0201 5% PHY1_RXD0/RXDLY
R105 4.7K R0201 5% VCCIO_PHY1
R109 4.7K R0201 5% PHY1_RXD1/TXDLY
R110 NC_4.7K R0201 5% VCCIO_PHY1
R113 4.7K R0201 5% PHY1_RXD2/PLLOFF
R114 NC_4.7K R0201 5% VCCIO_PHY1
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
PHY1_REG_OUT
L10
WPN252012H2R2MT
L2520
C245 4.7uF X5R 10V C0402
C246 100nF X5R 10V C0201
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
VDD10_PHY1
C247 100nF X5R 10V C0201
Close to PIN21
C251 100nF X5R 10V C0201
C252 100nF X5R 10V C0201
C253 100nF X5R 10V C0201
Close to PIN3,8,38
VCCIO_PHY1
C239 4.7uF X5R 10V C0402
C240 1uF X5R 6.3V C0201
C241 100nF X5R 10V C0201
Close to PIN28
VCC_3V3
VCC3V3_PHY1
C242 4.7uF X5R 10V C0402
C243 100nF X5R 10V C0201
C244 100nF X5R 10V C0201
Close to PIN11,40
C249 4.7uF X5R 10V C0402
C250 100nF X5R 10V C0201
Close to PIN29
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 18.Ethernet-GEPHY_RGMII
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
Of: 0


PCIE M.2 NGFF
M-KEY SOCKET
Hole2
PGND2
GND14
GND13
PETn3
PETp3
GND12
PERn3
PERp3
GND11
PETn2
PETp2
GND10
PERn2
PERp2
GND9
PETn1
PETp1
GND8
PERn1
PERp1
GND7
PERn0
PERP0
GND6
PETn0
PETP0
GND5
REFCLKN
REFCLKP
GND4
NC17
PEDET
GND3
GND2
GND1
PGND1
Hole1
M.2
M.2-KEY-M-H3R2
3V3#9
3V3#8
NC1
NC2
LED1#
3V3#7
3V3#6
3V3#5
3V3#4
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
SMCLK
SNDAT
ALERT
NC13
NC14
PERSTn
CLKREQn
WAKEn
NC15
NC16
SUSCLK
3V3#3
3V3#2
3V3#1
VCC3V3_PCIE30
C205 100nF X5R 10V C0201
C85 10uF X5R 6.3V C0402B
LED1 LED_BLUE LED0402
PCIe LED
R151 470R R0201
VCC_3V3
LED2 LED_GREEN LED0402
R152 470R R0201 5%
WORK_LED
R153 33K R0201
Q8 2SK3018
LED3 LED_RED LED0402
POWER_LED
R154 1K R0201 5%
H1 HOLE_3R20 M2_115X200_SMT
PCIE20_RXN
PCIE20_RXP
PCIE20_TXN
PCIE20_TXP
C207 100nF C0201 X5R 10V
C208 100nF C0201 X5R 10V
PCIE20_REFCLK_N
PCIE20_REFCLK_P
PCIE20_PERSTn_3V3_L
PCIE20_CLKREQn_3V3_L
PCIE20_WAKEn_3V3_L
VCC5V0_SYS
U8
VIN
GND
EN
LX
BS
FB/OUT
SOT23-6
C233 22uF X5R 10V C0603
C254 100nF X5R 10V C0201
R129 10K R0201
C259 10nF X5R 10V C0201
C232 100nF
X5R 16V C0201
L11 ind-4x4
FB=0.6V
C236 22pF C0G 50V C0201
R121 100K.1% R0201
R122 22K.1% R0201
C256 22uF X5R 10V C0603
C257 22uF X5R 10V C0603
C258 100nF X5R 10V C0201
C255 10uF X5R 10V C0402B
PCIe20_PWREN
C215 10uF X5R 6.3V C0402B
C84 100nF X5R 10V C0201
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 20.M.2 M key PCIe/LED
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
Of: 0


Type C Power
TYPEC1
UT12113-11601-7H
USB_OTG0_VBUSDET
R19
10K
R0201
USB5V_OTG
C86
100nF
X5R
16V
C0201
R20
15K
5%
R0201
J1
CON2
PH2-100TM-TH-H8R6
R57
5.1K
R0201
R56
5.1K
R0201
VCC5V0_SYS
3A
ESD4
ESD0402-6
C83
10uF
C0402B
VCC5V0_SYS
500mA
C181
10uF
X5R
25V
C0402B
C210
100nF
X5R
25V
C0201
D6
B5819WS
SOD_323
500mA
FAN1
2PIN_1R25
A1251WF-2P-125
GPIO0_C6-PWM7_IR
R25
10K
R0201
Q4
WNM2016-3/TR
SOT_23
C211
100nF.nc
X5R
25V
C0201
ADC
HEADER 4
SIP1x4
SARADC_VIN3
SARADC_VIN2
VCC_3V3
500mA
C187
10uF
C0402B
USB 2.0 X2
USBA1
USB_HOST
USB5V_HOST
USB2_HOST2_DM
USB2_HOST2_DP
USB2_HOST3_DM
USB2_HOST3_DP
C194
10uF
C0402B
C195
100nF
C0201
C192
10uF
C0402B
C193
100nF
C0201
USB1
USB2.0+USB3.0
USB_OTG0_DM
USB_OTG0_DP
C199
10uF
C0402B
C200
100nF
C0201
USB3_HOST1_DM
USB3_HOST1_DP
USB3_HOST1_SSRXN
USB3_HOST1_SSRXP
USB3_HOST1_SSTXN
USB3_HOST1_SSTXP
100nF C203 C0201
100nF C204 C0201
C201
10uF
C0402B
C202
100nF
C0201
U6
SOT23-5
C190
100nF
C0201
R140
10K.NC
R0201
R141
10K
R0201
USB_OTG_PWREN_H
R142
6.8K
R0201
U7
SOT23-5
C191
100nF
C0201
R145
10K.NC
R0201
R146
10K
R0201
USB_HOST_PWREN_H
R147
3K
R0201
Shenzhen Xunlong Software Co., Ltd
Project: OPi 3B
File: 21.USB_POWER/FAN
Date: Monday, May 27, 2024
Rev: V2.1
Size: A3
Sheet: 0
Of: 0