DATASHEET

Low Power DRAM (LPDDR4 FBGA)

D0811PM2FDGUK-U (512Mx16bitsx1channel)
D0811PM2FDGUKW-U (512Mx16bitsx1channel)
B1621PM2FDGUK-U (512Mx16bitsx2channels)
B1621PM2FDGUKW-U (512Mx16bitsx2channels)

Specifications

- Die Density: 8Gbits
- Organization
  - x 16 bits: 64M words x 16 bits x 8 banks
  - 2 pieces of 8Gb (x16) in one package (For 16Gb)
  - Row Address: R0 ~ R15
  - Column Address: C0 ~ C9
- Package
  - 200-ball FBGA
- Power supply
  - VDD1 = 1.8V (1.70V to 1.95V) ,
  - VDD2, VDDCA and VDDQ = 1.1V (1.06V to 1.17V)
- Data rate:
  - 3733Mbps max. Backward compatible
- Eight internal banks per channel for concurrent operation
- Burst lengths (BL): 16, 32 and on-the-fly
  - On the fly mode is enabled by MRS
- Programmable RL (Read Latency) and WL (Write Latency)
- Precharge: auto precharge option for each burst access
- Programmable driver strength
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/32ms
  - Average refresh period: 3.9μs
- Operating temperature range
  - TC = -25°C to +85°C (Standard)
  - TC = -40°C to +95°C (Industrial Temperature)

Features

- Low power consumption
- Per Bank Refresh
- Partial Array Self-Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self-Refresh
  - (ATCSR) by built-in temperature sensor
- All bank auto refresh and directed per bank auto refresh supported
- Double-data-rate architecture; two data transfers per one clock cycle
- Differential clock inputs (CK_t and CK_c)
- Bi-directional differential data strobe (DQS_tandDQS_c)
- Commands entered on both rising and falling CK_t edge; data and data mask referenced to both edges of DQS_t
- DMI pin support for write data masking and DBIdc functionality

Lower Clock Frequency Limit (MHz)	Upper Clock Frequency Limit (Mb/s/pin)	WRITE Latency		READ Latency	
		Set A	Set B	DBI Disabled	DBI Enabled
1600	1866	16	30	32	36

Device Addressing

<table>
<tr><th colspan="2">Device density</th><th>8Gb (512M x 16 I/O x 1 channel)</th><th>16Gb (512M x 16 I/O x 2 channels)</th></tr>
<tr><td colspan="2">Number of die per device</td><td>1</td><td>2</td></tr>
<tr><td colspan="2">Device density (per rank)</td><td>8Gb</td><td>16Gb</td></tr>
<tr><td colspan="2">Die density</td><td>8Gb</td><td>8Gb</td></tr>
<tr><td colspan="2">Device configuration</td><td>64Mb x 1 rank(s) x 8 banks x 16 DQ x 1 channel</td><td>64Mb x 1 rank(s) x 8 banks x 16 DQ x 2 channels</td></tr>
<tr><td colspan="2">Number of channels</td><td>1</td><td>2</td></tr>
<tr><td colspan="2">Number of ranks</td><td>1</td><td>1</td></tr>
<tr><td colspan="2">Number of banks (per channel)</td><td>8</td><td>8</td></tr>
<tr><td colspan="2">Number of rows (per channel)</td><td>65,536</td><td>65,536</td></tr>
<tr><td colspan="2">Bank address</td><td>BA0-BA2</td><td>BA0-BA2</td></tr>
<tr><td rowspan="2">x16</td><td>Row addresses</td><td>R0-R15</td><td>R0-R15</td></tr>
<tr><td>Column addresses</td><td>C0-C9</td><td>C0-C9</td></tr>
<tr><td colspan="2">Burst starting address boundary</td><td>64-bit</td><td>64-bit</td></tr>
</table>

Notes: 1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.

2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."

Revision History

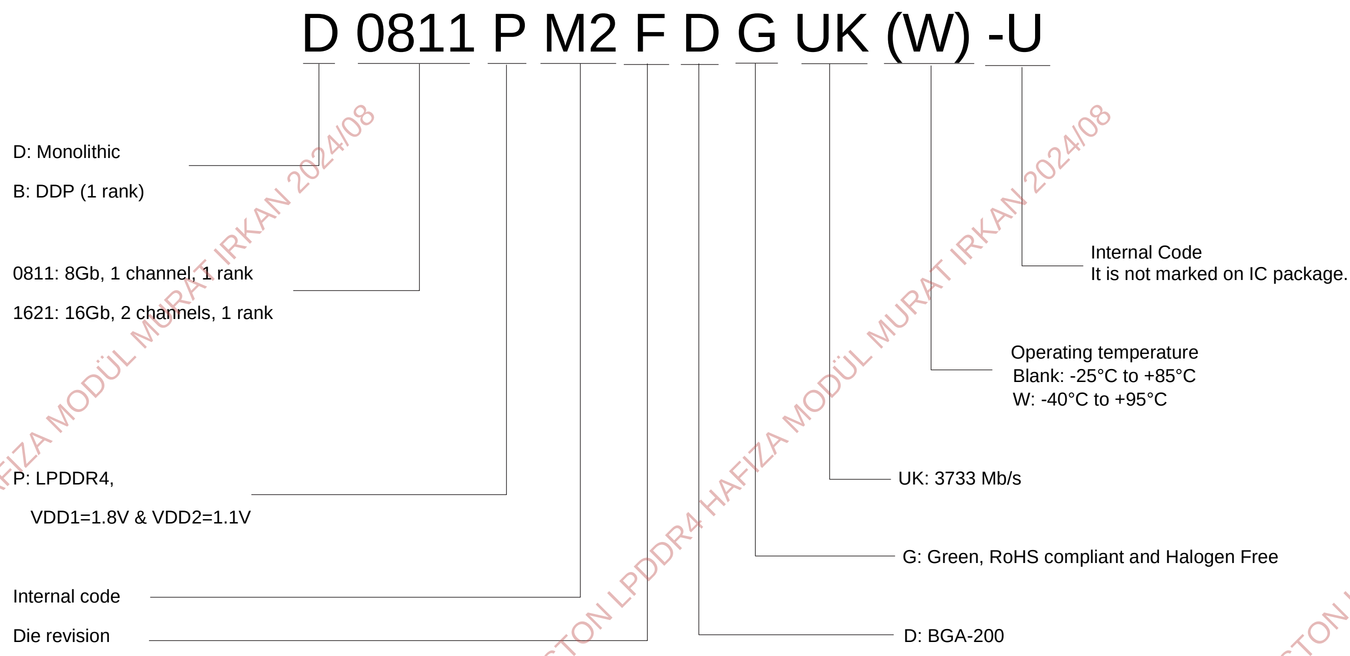
Revision No.	History	Release date	Editor	Approved by
A00	Initial release	August 2023	Annie Hsu	Sander Huang / CK Wang
B00	Add industrial temperature & remove “preliminary” mark	October 2023	Jona Lee	Sander Huang / CK Wang

**Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by without notice.*
All information discussed herein is provided on an “as is” basis, without warranties of any kind.

Ordering Information

Part number	Die revision	Organization (words x bits x channels)	Internal banks	JEDEC speed	Package
D0811PM2FDGUK-U	F Die	512M x 16bits x 1 channel	8 banks	3733 Mb/s	200 ball FBGA
D0811PM2FDGUKW-U	F Die	512M x 16bits x 1 channel	8 banks	3733 Mb/s	200 ball FBGA
B1621PM2FDGUK-U	F Die	512M x 16bits x 2 channels	8 banks	3733 Mb/s	200 ball FBGA
B1621PM2FDGUKW-U	F Die	512M x 16bits x 2 channels	8 banks	3733 Mb/s	200 ball FBGA

Part Number



1. LPDDR4 Interface

1.1 Pin Function and Descriptions

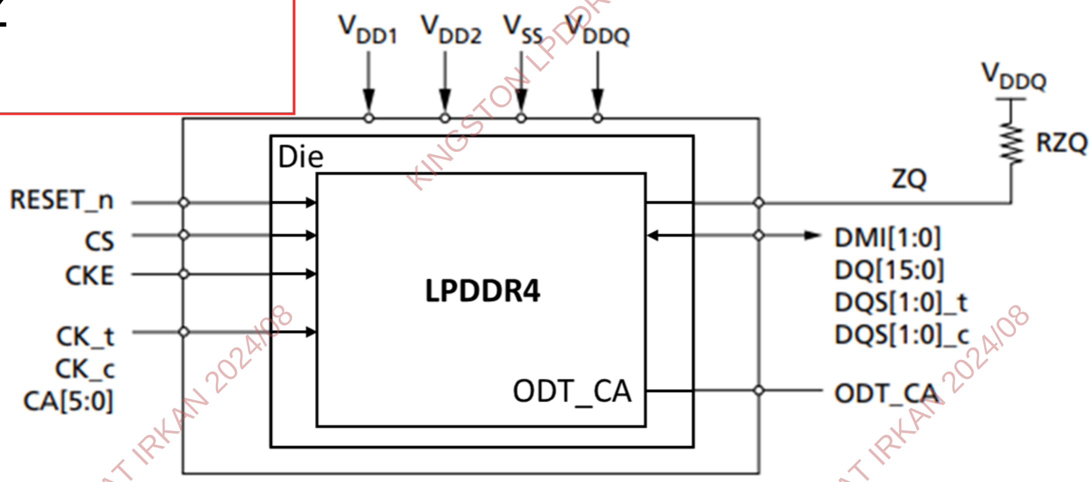
Table — Pin Function and Descriptions

Name	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE0_A CKE0_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS0_A CS0_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

NOTE 1 "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.

Functional Block Diagram

KÜP PC LPDD4
4133 MHz

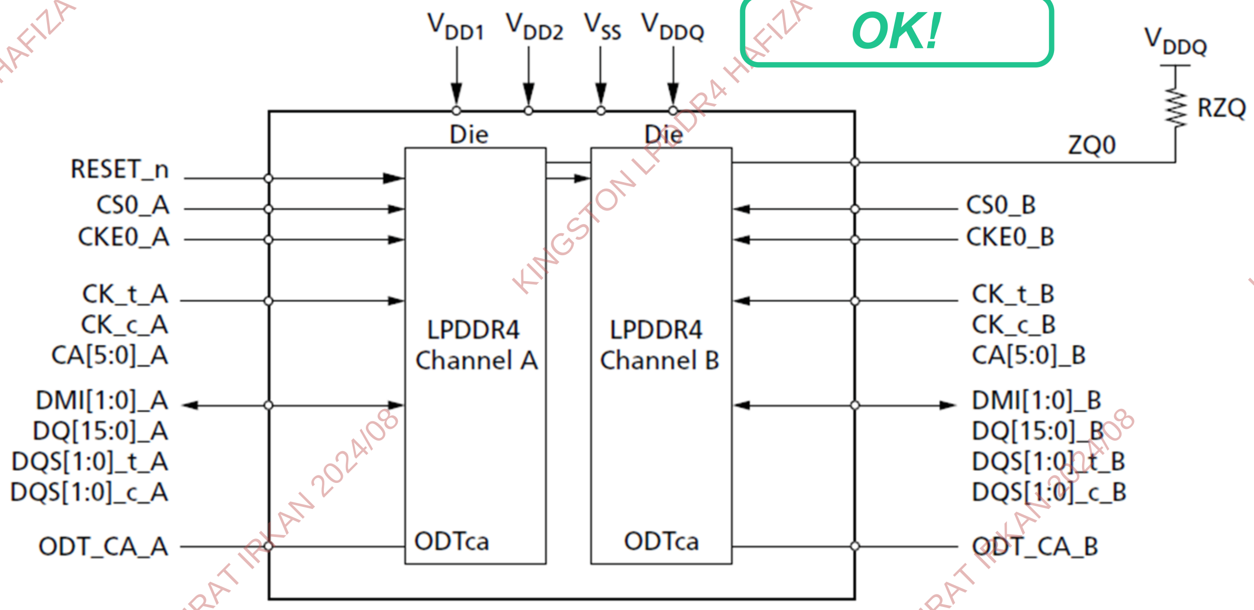


Single-Die, Single-Channel, Single-Rank Package Block Diagram (x16 I/O)

DDP

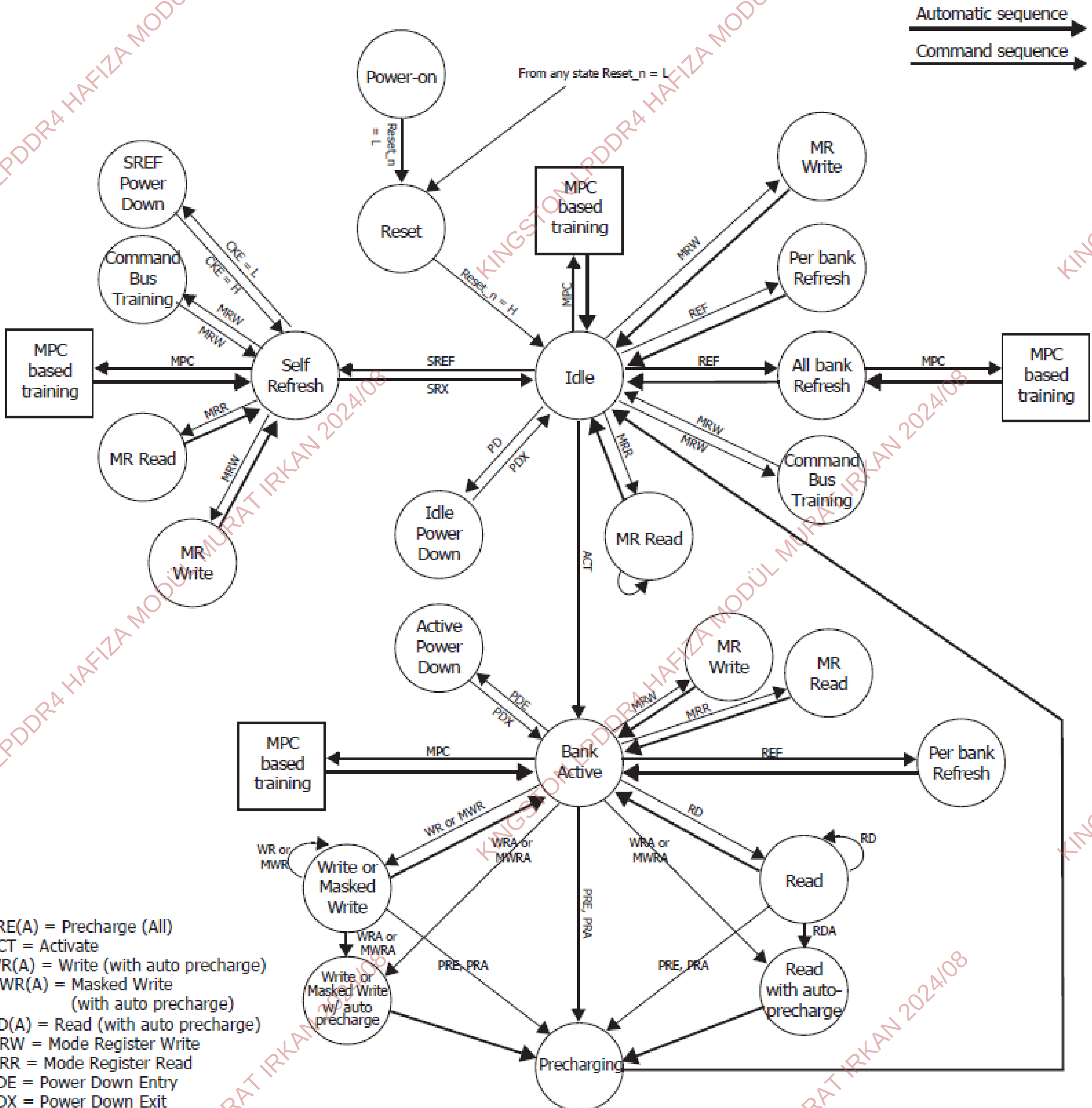
KÜP VE NOTEBOOK LINUX PC 8GB LPDDR4

OK!



Dual-Die, Dual-Channel, Single-Rank Package Block Diagram (x16 I/O)

Simplified State Diagram



PRE(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with auto precharge)
MWR(A) = Masked Write (with auto precharge)
RD(A) = Read (with auto precharge)
MRW = Mode Register Write
MRR = Mode Register Read
PDE = Power Down Entry
PDX = Power Down Exit
SREF = Self Refresh Entry
SRX = Self Refresh Exit
REF = Refresh
MPC = Multi Purpose Command

Figure — Simplified Bus Interface State Diagram

Note 1: For DDR4 Mobile RAM in the Idle state, all banks are precharged.

1.2 Electrical Conditions

All voltages are referenced to VSS (GND)

— Execute power-up and Initialization sequence before proper device operation is achieved.

— Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR4 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

1.2.1 Absolute maximum Ratings

Table — Absolute maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.5	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.5	V	2
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	3

Notes:

1. Stresses greater than those listed under “Absolute maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See Power-Ramp section “Power-up, initialization and Power-Off” on section1.4 for relationship between power supplies
3. Storage Temperature is the case surface temperature on the center/top side of the DDR3 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution

Exposing the device to stress above those listed in Absolute maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute maximum Rating conditions for extended periods may affect device reliability.

1.2.2 Recommended DC Operating Conditions

Table — Recommended DC Operating Conditions

Parameter	Symbol	min.	Typ	max.	Unit	Note
Core Power1	VDD1	1.70	1.80	1.95	V	1,2
Core Power2, Input buffer power	VDD2	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	VDDQ	1.06	1.10	1.17	V	2,3

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mV at the DRAM ball is not included in the TdIVW.

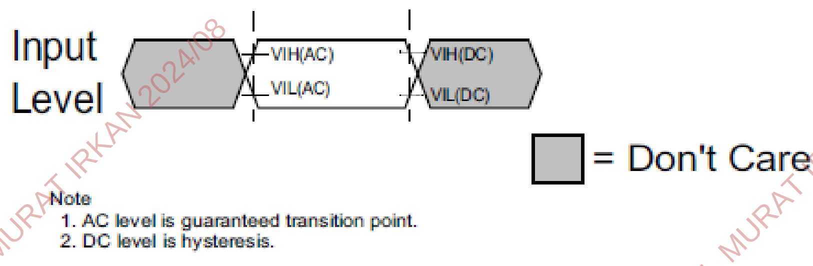
1.2.3 AC and DC Input Measurement Levels

1.2.3.1 V High speed LVCMOS (HS_LLVCMOS)

Table — LPDDR4 Input level for CKE

Parameter	Symbol	min.	max.	Unit	Note
AC input logic high	VIH(AC)	0.75*VDD2	VDD2+0.2	V	1
AC input logic low	VIL(AC)	-0.2	0.25*VDD2	V	1
DC input logic high	VIH(DC)	0.65*VDD2	VDD2+0.2	V	
DC input logic low	VIL(DC)	-0.2	0.35*VDD2	V	

Note: 1. See “Overshoot and Undershoot Specifications” on section 1.2.4.

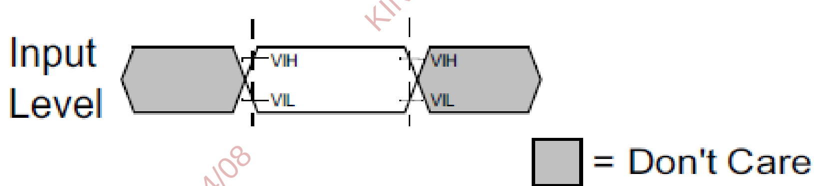


1.2.3.2 LPDDR4 Input Level for Reset_n and ODT_CA

Table — LPDDR4 Input level for Reset_n and ODT_CA

Parameter	Symbol	min.	max.	Unit	Note
Input high level	VIH	0.8*VDD2	VDD2+0.2	V	1
Input low level	VIL	-0.2	0.20*VDD2	V	1

Note: 1. See “Overshoot and Undershoot Specifications” on section 1.2.4.



1.2.4 AC Overshoot and Undershoot Specifications

Table — LPDDR4 Overshoot/Undershoot Specification

Parameter		Specification	Unit
maximum peak amplitude allowed for overshoot area.	Max.	0.3	V
maximum peak amplitude allowed for undershoot area.	Max.	0.3	V
maximum overshoot area above VDD/VDDQ	Max.	0.8	V-ns
maximum undershoot area below VSS/VSSQ	Max.	0.8	V-ns

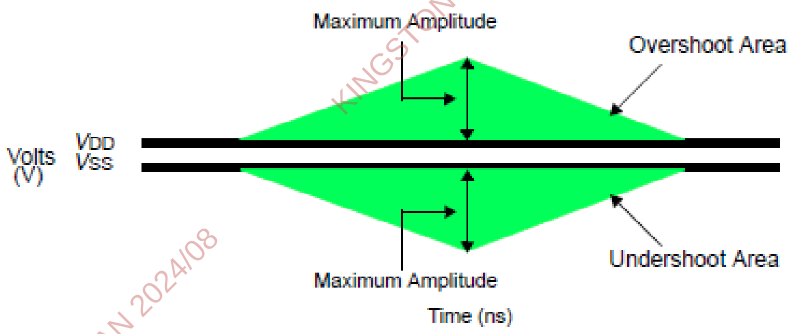


Figure — AC Overshoot and Undershoot Definition

1.2.5 Differential Input Voltage

1.2.5.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

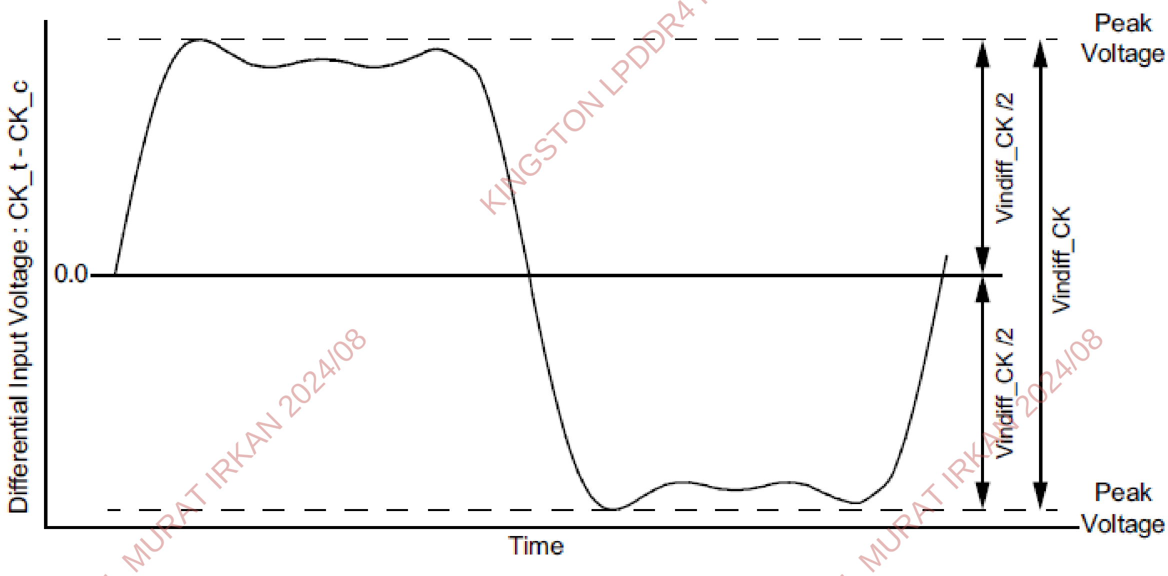


Figure — CK Differential input voltage

Table — CK Differential input voltage

Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867		2133/2400/3200		3733/4267			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV	1

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VCK_t - VCK_c

1.2.5.2 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V

Figure - DQS Differential Input Voltage

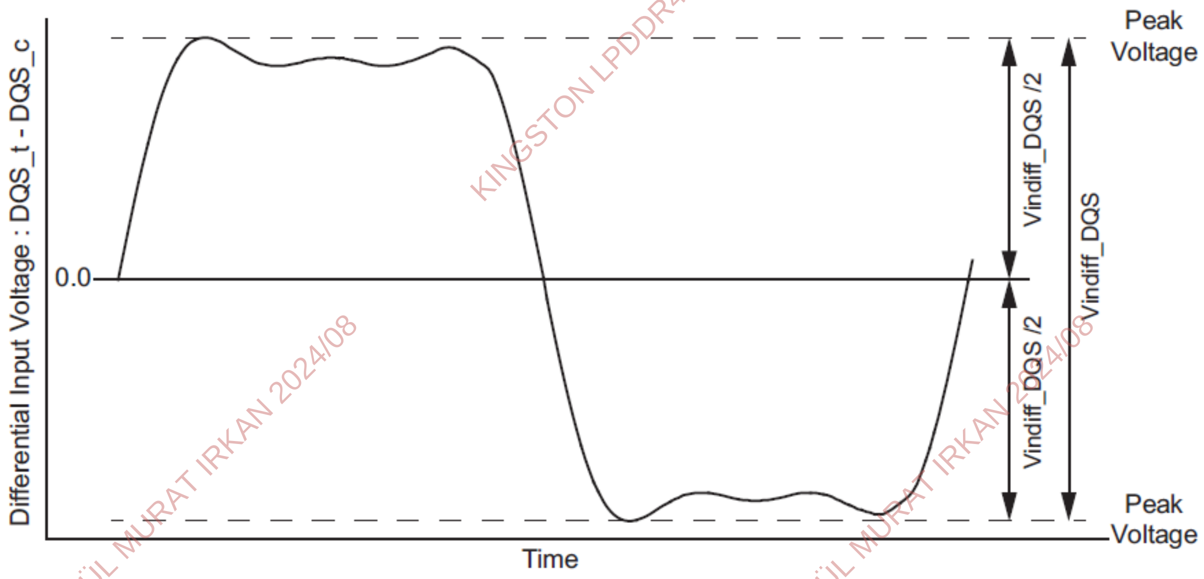


Table — Differential AC and DC Input Levels

Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867		2133/2400/3200		3733/4267			
		Min	Max	Min	Max	Min	Max		
DQS differential input	Vindiff_DQS	360	-	360	-	340	-	mV	1

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VDQS_t - VDQS_c

1.2.6 Differential Input Cross Point Voltage

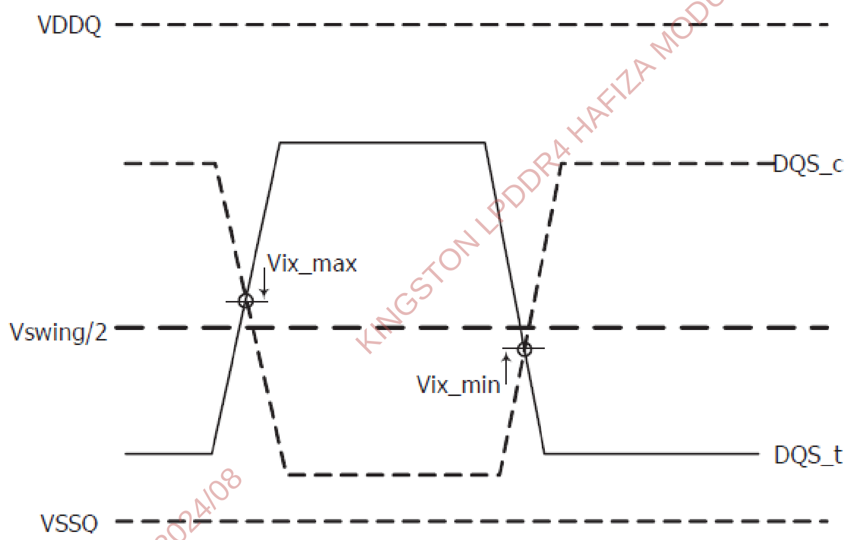


Figure — DQS input cross-point voltage (V)VIX Definition

Table — DQS input voltage cross-point (Vix) ratio

Parameter	Symbol	Min / Max	Data rate			Unit	Note
			1600/1867	2133/2400/3200	3733/4267		
DQS Differential input cross-point voltage ratio	Vix_DQS_ratio	Max	20	20	20	%	1,2

Notes:
1. The Vix voltage is referenced to Vswing/2(avg)= 0.5(VDQS_t + VDQS_c) where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (Vix_DQS/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|.

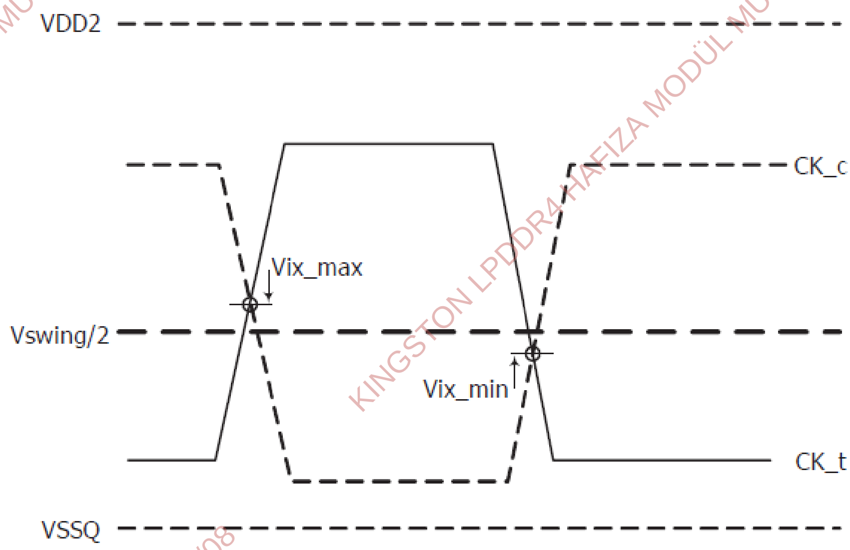


Figure — CK input cross-point voltage (Vix)

Parameter	Symbol	Min / Max	Data rate			Unit	Note
			1600/1867	2133/2400/3200	3733/4267		
CK Differential input cross-point voltage ratio	Vix_CK_ratio	Max	25	25	25	%	1,2

Notes:
1. The Vix voltage is referenced to Vswing/2(avg)= 0.5(VCK_t + VCK_c) where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by Vdiff_CK : Vix_CK_Ratio = 100* (Vix_CK/Vdiff CK pk-pk) where VdiffCK pk-pk = 2*|VCK_t - VCK_c|

1.2.6.1 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table 14 and Figure 8.

Table — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) – VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) – VOL(AC)] / DeltaTFse

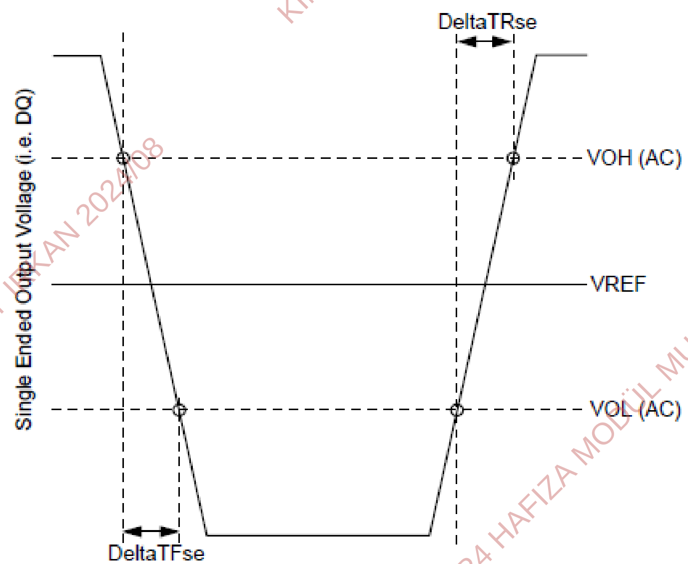


Figure — Single Ended Output Slew Rate Definition

Table — Output Slew Rate (single-ended)

Parameter	Symbol	min.	max.	Unit
Single-ended Output Slew Rate (VOH = VDDQ/3)	SRQse	3.0	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)		0.8	1.2	

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Notes:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

1.2.7 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 16 and Figure 9.

Table — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

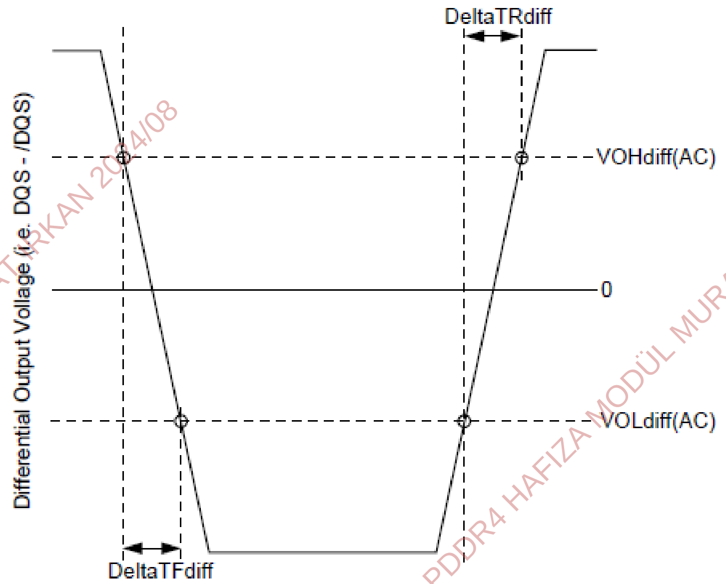


Figure — Differential Output Slew Rate Definition

Table — Differential Output Slew Rate

Parameter	Symbol	min.	max.	Unit
Differential Output Slew Rate (VOH=VDDQ x 0.5)	SRQdiff	6	18	V/ns

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals

Notes:

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

1.3 Electrical Specifications

1.3.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: VIN ≤ VIL(DC) max.
HIGH: VIN ≥ VIH(DC) min.
STABLE: Inputs are stable at a HIGH or LOW level

Table — Definition of Switching for CA Input Signals

	Switching for CA							
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:
1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table — CA pattern for IDD4R for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L
N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, CA[9:4] = 000000 or 111111, Burst Order CA[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

Table — CA pattern for IDD4W for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L
N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W Spec.)
2. Difference from LPDDR3 Spec:
   1-No burst ordering
   2-CA pins are kept low with DES CMD to reduce ODT current.

Table — Data pattern for IDD4W (DBI off) for BL = 16

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4

BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:
1. Simplified pattern compared with last showing.
2. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table — Data pattern for IDD4R (DBI off) for BL =16

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:
1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table — Data pattern for IDD4W (DBI on) for BL = 16

	DBI ON case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Notes:
1. Green colored cells are DBI enabled burst.

Table — Data pattern for IDD4R (DBI on) for BL = 16

	DBI ON case									No. of 1’s
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1’s	8	8	8	8	8	8	16	16	8	

Notes:
1. Green colored cells are DBI enabled burst.

1.3.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

Table — IDD Specification Parameters and Operating Conditions-Single Die

Parameter/Condition	Symbol	Power Supply	LPDDR4-3733		Units	Notes
			85 °C	95 °C		
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD01	VDD1	4.00	5.56	mA	
	IDD02	VDD2	29.00	39.06	mA	
	IDD0Q	VDDQ	0.75	0.82	mA	3
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD2P1	VDD1	1.10	1.13	mA	
	IDD2P2	VDD2	1.80	2.97	mA	
	IDD2PQ	VDDQ	0.75	0.82	mA	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT is disabled.	IDD2PS1	VDD1	1.10	1.13	mA	
	IDD2PS2	VDD2	1.80	2.97	mA	
	IDD2PSQ	VDDQ	0.75	0.82	mA	3
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT is disabled.	IDD2N1	VDD1	1.20	1.24	mA	
	IDD2N2	VDD2	16.00	23.19	mA	
	IDD2NQ	VDDQ	0.75	0.82	mA	3

Parameter/Condition	Symbol	Power Supply	LPDDR4-3733		Units	Notes
			85 ºC	95 ºC		
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD2NS1	VDD1	1.20	1.24	mA	
	IDD2NS2	VDD2	10.00	15.70	mA	
	IDD2NSQ	VDDQ	0.75	0.82	mA	3
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3P1	VDD1	1.10	1.13	mA	
	IDD3P2	VDD2	4.80	7.42	mA	
	IDD3PQ	VDDQ	0.75	0.82	mA	3
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3PS1	VDD1	1.10	1.13	mA	
	IDD3PS2	VDD2	4.80	7.51	mA	
	IDD3PSQ	VDDQ	0.75	0.82	mA	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3N1	VDD1	1.50	1.55	mA	
	IDD3N2	VDD2	21.00	30.00	mA	
	IDD3NQ	VDDQ	0.75	0.82	mA	4

Parameter/Condition	Symbol	Power Supply	LPDDR4-3733		Units	Notes
			85 ºC	95 ºC		
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3NS$_1$	VDD1	1.50	1.55	mA	
	IDD3NS$_2$	VDD2	15.00	22.87	mA	
	IDD3NS$_Q$	VDDQ	0.75	0.82	mA	4
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled.	IDD4R$_1$	VDD1	2.50	3.13	mA	
	IDD4R$_2$	VDD2	263.00	288.95	mA	
	IDD4R$_Q$	VDDQ	61.57	81.07	mA	5
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W$_1$	VDD1	1.50	1.73	mA	
	IDD4W$_2$	VDD2	195.00	222.68	mA	
	IDD4W$_Q$	VDDQ	0.75	0.82	mA	4

All-bank REFRESH Burst current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5$_1$	VDD1	9.00	11.59	mA	

	IDD5$_2$	VDD2	90.00	110.08	mA	
	IDD5$_Q$	VDDQ	0.75	0.82	mA	4

Parameter/Condition	Symbol	Power Supply	LPDDR4-3733		Units	Notes
			85 °C	95 °C		

All-bank REFRESH Average current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5AB1	VDD1	1.70	1.85	mA	

	IDD5AB2	VDD2	22.00	30.21	mA	
	IDD5ABQ	VDDQ	0.75	0.82	mA	4

Per-bank REFRESH Average current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5PB1	VDD1	1.70	1.85	mA	

	IDD5PB2	VDD2	22.00	30.21	mA	
	IDD5PBQ	VDDQ	0.75	0.82	mA	4
Self refresh current (85 °C / 95 °C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	IDD61	VDD1	1.50	1.55	mA	6,7,9
	IDD62	VDD2	6.00	14.42	mA	6,7,9
	IDD6Q	VDDQ	0.75	0.82	mA	4,6,7,9
Self refresh current (25 °C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	IDD61	VDD1	0.19	0.19	mA	6,7,9
	IDD62	VDD2	0.46	0.46	mA	6,7,9
	IDD6Q	VDDQ	0.01	0.01	mA	4,6,7,9

Notes:
1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. This is the general definition that applies to full array Self Refresh.
7. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
8. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9. IDD6 95˚C is guaranteed, IDD6 25/105˚C is typical of the distribution of the arithmetic mean.
10. IDD6ET is a typical value, is sampled only, and is not tested.

1.3.3 AC Timing Parameters

Table — Core Parameters

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
ACTIVE to ACTIVE command period	tRC	min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)								ns	
Self Refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)								ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 5nCK)								ns	
CAS to CAS delay	tCCD	min	8								tCK(avg)	
CAS to CAS delay (Masked Write w/ECC)	tCCDMW	min	32								tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 8nCK)								ns	
RAS to CAS Delay	tRCD	min	max(18ns, 4nCK)								ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns, 3nCK)								ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 3nCK)								ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)								ns	
		max	min(9 * tREFI * Refresh Rate, 70.2)								us	
Write Recovery Time	tWR	min	max(18ns, 4nCK)								ns	
Write to Read Command Delay	tWTR	min	max(10ns, 8nCK)								ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 4ncK)							max(7.5ns,4nCK)	ns	1
Precharge to Precharge Delay	tPPD	min	4								tCK	2
Four Bank Activate Window	tFAW	min	40							30	ns	1
Delay from SRE command to CKE input LOW	tESCKE	min	max(1.75ns, 3nCK)								-	3

Notes:
1. 4267 Mbps timing value is supported at lower data rates if the device is supporting 4266 Mbps speed grade.
2. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
3. Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycle (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

Table — Clock timings

Parameter	Symbol	min/max	LPDDR4 1600	LPDDR4 3200	LPDDR4 3733	LPDDR4 4267	Unit	Note
Average Clock Period	tCK(avg)	min	1.25	0.625	0.535	0.468	ns	
		max	100	100	100	100		
Average high pulse width	tCH(avg)	min	0.46				tCK(avg)	
		max	0.54					
Average low pulse width	tCL(avg)	min	0.46				tCK(avg)	
		max	0.54					
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min				ps	
Absolute clock HIGH pulse width	tCH(abs)	min	0.43				tCK(avg)	
		max	0.57					
Absolute clock LOW pulse width	tCL(abs)	min	0.43				tCK(avg)	
		max	0.57					
Clock Period Jitter	tJIT(per)	min	-70	-40	-34	-30	ps	
		max	70	40	34	30		
Maximum Clock Jitter between two consecutive clock cycles	tJIT(cc)	min	-				ps	
		max	140	80	68	60		

Table — ZQ Calibration timings

Parameter	Symbol	min/max	LPDDR4 Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
ZQ Calibration Time	tZQCAL	min	1								us	
ZQ Calibration Latch Quiet Time	tZQLAT	min	max(30ns, 8nCK)								ns	
Calibration Reset Time	tZQRESET	min	max(50ns, 3nCK)								ns	

Table —DQ Tx Voltage and Timings (Read Timing parameters)

Parameter	Symbol	min/ max	533/ 1066/ 1600	2133/ 2667	3200/ 3733/ 4267	Unit	Note
Data Timing							
DQS_t,DQS_c to DQ Skew	tDQSQ	max	0.18			UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min	min(tQSH, tQSL)			ps	6
DQ output window time total, per pin (DBI-Disabled)	tQW_total	min	0.75	0.73	0.70	UI	6,11
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	max	0.18			UI	6
DQ output hold time total from DQS_t, DQS_c (DBIenabled)	tQH_DBI	min	min(tQSH_DBI, tQSL_DBI)			ps	6
DQ output window time total, per pin (DBI-enabled)	tQW_total_DBI	min	0.75	0.73	0.70	UI	6,11
Read preamble	tRPRE	min	1.8			tCK(avg)	
Read postamble	tRPST	min	0.4			tCK(avg)	
Extended Read postamble	tRPSTE	min	1.4			tCK(avg)	
DQS Low-impedance time from CK_t, CK_c	tLZ(DQS)	min	(RL x tCK) + tDQSCK(Min) - (tPRE(Max) x tCK) - 200ps			ps	
DQS High-impedance time from CK_t, CK_c	tHZ(DQS)	max	(RL x tCK) + tDQSCK(Max) + (BL/2 x tCK) + (tRPST(Max) x tCK) - 100ps			ps	
DQ Low-impedance time from CK_t, CK_c	tLZ(DQ)	min	(RL x tCK) + tDQSCK(Min) - 200ps			ps	
DQ High-impedance time from CK_t, CK_c	tHZ(DQ)	max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max)+ (BL/2 x tCK) - 100ps			ps	
Data Strobe Timing							
DQS output access time from CK/CK#	tDQSCK	min	1.5			ns	1
		max	3.5				
DQSCK Temperature Drift	tDQSCK_temp	max	4			ps/℃	3
DQSCK Volgate Drift	tDQSCK_volt	max	7			ps/mV	2
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	max	1			ns	4,5
DQS Output Low Pulse Width (DBI Disabled)	tQSL	min	tCL(abs)-0.05			tCK(avg)	9,11
DQS Output High Pulse Width (DBI Disabled)	tQSH	min	tCH(abs)-0.05			tCK(avg)	10.,11
DQS Output Low Pulse Width (DBI Enabled)	tQSL_DBI	min	tCL(abs)-0.045			tCK(avg)	9,11
DQS Output High Pulse Width (DBI Enabled)	tQSH_DBI	min	tCH(abs)-0.045			tCK(avg)	10,11

Notes:
1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The volage supply noise must comply to the component Min-Max DC Operating conditions.
2. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}] / abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.
3. tDQSCK_temp max delay variation as a function of Temperature.
4. The same voltage and temperature are applied to tDQS2CK_rank2rank.
5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
6. DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to thenext consecutive rising edge.
11. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater than tCK(avg), the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.
12. UI=tCK(avg)min/2

Table — DQ Tx Voltage and Timings (Write Timing parameters)

Parameter	Symbol	min/max	1600/ 1867	2133/ 2400	3200/ 3733	4267	Unit	Note
Rx Mask voltage p-p total	VdIVW_total	max	140	140	140	120	mV	1,2,3,5
Rx Mask voltage - deterministic	VdIVW_dV	max	TBD	TBD	TBD	TBD	mV	1,5
Rx timing window total (At VdIVW voltage levels)	TdIVW_total	max	0.22	0.22	0.25	0.25	UI	1,2,4,5
Rx deterministic timing	TdIVW_dj	max	TBD	TBD	TBD	TBD	UI	1,5
Rx timing window 1bit toggle (At VdIVW voltage levels)	TdIVW_1bit	max	TBD	TBD	TBD	TBD	UI	1,2,4,5,14
DQ AC input pulse amplitude p-p	VIHIL_AC	min	180	180	180	170	mV	7,15
DQ input pulse width (At Vcent_DQ)	TdIPW	min	0.45	0.45	0.45	0.45	UI	10
DQ to DQS offset	TDQS2DQ	min	200	200	200	200	ps	9
		max	800	800	800	800		
DQ to DQ offset	TDQDQ	max	30	30	30	30	ps	10
DQ to DQS offset temperature variation	TDQS2DQ_temp	max	0.6	0.6	0.6	0.6	ps/°C	11
DQ to DQS offset voltage variation	TDQS2DQ_volt	max	33	33	33	33	ps/50mV	12
DQ to DQS offset rank to rank	TDQS2DQ_rank2rank	max	200	200	200	200	ps	17,18
Write command to 1st DQS latching transition	tDQSS	min	0.75				tCK(avg)	
		max	1.25					
DQS input high-level width	tDQSH	min	0.4				tCK(avg)	
DQS input low-level width	tDQSL	min	0.4				tCK(avg)	
DQS falling edge to CK setup time	tDSS	min	0.2				tCK(avg)	
DQS falling edge hold time from CK	tDSH	min	0.2				tCK(avg)	
Write preamble	tWPRE	min	1.8				tCK(avg)	
0.5 tCK Write postamble	tWPST	min	0.4				tCK(avg)	
1.5 tCK Write postamble	tWPSTE	min	1.4				tCK(avg)	
Input slew rate over VdIVW_total	SRIN_dIVW	min	1	1	1	1	V/ns	13
		max	7	7	7	7		

Notes:
1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >250KHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.
5. Defined over the DQ internal Vref range. The Rx mask at the pin must be within the internal Vref DQ range irrespective of the input signal common mode.
6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method TBD

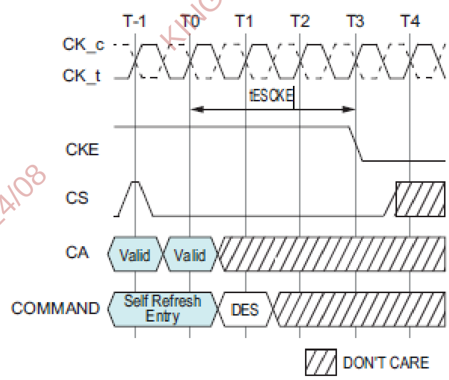
7. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that IHL_AC/2 min must be met both above and below Vcent_DQ.
8. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
9. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
10. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
11. TDQS2DQ max delay variation as a function of temperature.
12. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2.
13. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
14. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
15. VIHL_AC does not have to be met when no transitions are occurring.
16. UI=tCK(avg)min/2
17. The same voltage and temperature are applied to tDQS2DQ_rank2rank
18. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

A. The following Rx voltage and timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min/2= 625ps for DQ=1600. For example the TdIVW_total(ps) =0.22*625ps= 137.5ps.

Table — Self-Refresh Timing Parameters

Parameter	Symbol	min/max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Delay from Self Refresh Entry to CKE Input Low	tESCKE	min	max(1.75ns,3tCK)								nCK	1
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)								ns	1
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)								ns	1,2

Note
1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.



2. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

Table — Command Address Input Parameters

Parameter	Symbol	min/ max	DQ-1333[A)]	DQ-1600/ 1867	DQ-3200	DQ-4266	Unit	Note
Rx Mask voltage p-p	VcIVW	max	175	175	155	145	mV	1,2,4
Rx timing window	tcIVW	max	0.3	0.3	0.3	0.3	UI	1,2,3,4
CA AC input pulse amplitude pk-pk	VIHL_AC	min	210	210	190	180	mV	5,8
CA input pulse width	TcIPW	min	0.55	0.55	0.6	0.6	UI	6
Input slew rate over VcIVW	SRIN_cIVW	min	1	1	1	1	V/ns	7
		max	7	7	7	7		

Notes:
1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal Vref range. The Rx mask at the pin must be within the internal Vref CA range irrespective of the input signal common mode.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
8. VIHL_AC does not have to be met when no transitions are occurring.
9. UI=tCK(avg)min

A. The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min= 1.5ns for DQ=1333. For example the TcIVW(ps) = 0.3*1.5ns=450ps.

Table — Boot Parameters

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Clock Cycle Time	tCKb	min	18								ns	
		max	100									
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	1								ns	
		max	10									
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2								ns	

Table — Mode Register Parameters

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Additional time after tXP has expired until the MRR command may be issued	tMRRI	min	tRCD + 3nCK								ns	
MODE REGISTER Write command period	tMRW	min	max(10ns, 10nCK)								ns	
MODE REGISTER Read command period	tMRR	min	8								nCK	
Mode Register Write Set Command Delay	tMRD	min	max(14ns, 10nCK)								ns	

Table — VRCG Enable/Disable Timing

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
VREF high current mode enable time	tVRCG_Enable	max	200								ns	
VREF high current mode disable time	tVRCG_Disable	max	100								ns	

Table — Command Bus Training Parameters

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Valid Clock Requirement after CKE Input Low	tCKELCK	min	max(5ns, 5nCK)								-	
Data Setup for Vref Training Mode	tDStrain	min	2								ns	
Data Hold for Vref Training Mode	tDHtrain	min	2								ns	
Asynchronous Data Read	tADR	max	20								ns	
CA Bus Training Command to CA Bus Training command Delay	tCACD	min	RU(tADR/tCK)								tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	min	10								ns	1
First CA Bus Training Command Following CKE Low	tCAENT	min	250								ns	
Vref Step Time – multiple steps	tVref_long	max	250								ns	
Vref Step Time – one step	tVref_short	max	80								ns	
Valid Clock Requirement before CS High	tCKPRECS	min	2*tCK + tXP								-	
Valid Clock Requirement after CS High	tCKPSTCS	min	max(7.5ns, 5nCK)								-	
Minimum delay from CS to DQS toggle in command bus training	tCS_Vref	min	2								tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	min	10								ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	min	max(1.75ns, 3nCK)								-	
CA Bus Training CKE High to DQ Tri-state	tMRZ	min	1.5								ns	
ODT turn-on latency from CKE	tCKELODTon	min	20								ns	
ODT turn-off latency from CKE	tCKELODToff	min	20								ns	

Notes:
1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

Table — Write Leveling Parameters

Parameter	Symbol	min/ max	Data Rate						Unit	Note
			1600	2133	2400	3200	3733	4267		
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	min	20						tCK	
Write preamble for Write Leveling	tWLWPRE	min	20						tCK	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40						tCK	
Write leveling output delay	tWLO	min	0						ns	
		max	20							
Valid Clock Requirement before DQS Toggle	tCKPRDQS	min	max(7.5ns, 4nCK)							
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	min	max(7.5ns, 4nCK)							
Write leveling hold time	tWLH	min	150	100	100	75	62.5	50	ps	1,2
Write leveling setup time	tWLS	min	150	100	100	75	62.5	50	ps	1,2
Write leveling invalid window	tWLIVW_Total	min	240	160	160	120	105	90	ps	1,2

Notes:
1. In addition to the traditional setup and hold time specifications above, there is value in a invalid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW_Total is defined in a similar manner to tdIVW_Total, except that here it is a DQS invalid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

The DQS input mask for timing with respect to CK is shown in the following figure. The “total” mask (TdiVW_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

Figure — DQS_t/DQS_c and CK_t/CK_c at DRAM Latch

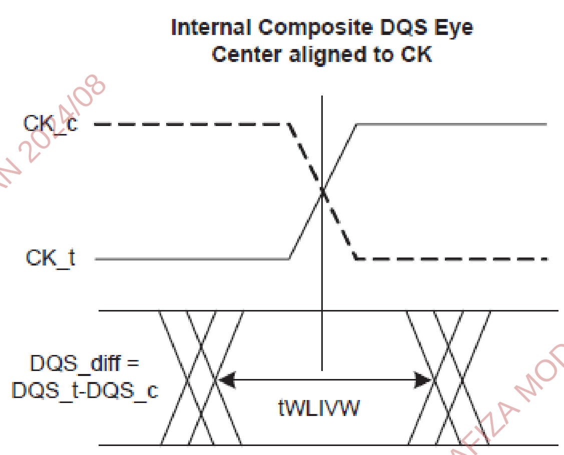


Table — Read Preamble Training Timings

Parameter	Symbol	min/max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Delay from MRW command to DQS Driven out	tSDO	max	max(12nCK, 20ns)								ns	1

Table — MPC [Write FIFO] AC Timing

Parameter	Symbol	min/max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	min	tRCD + 3nCK									

Table — DQS Interval Oscillator AC Timing

Parameter	Symbol	min/max	Value	Unit	Note
Delay time from OSC stop to Mode Register Readout	tOSCO	min	max(40ns,8nCK)	ns	

Table — Frequency Set Point Timing

Parameter	Symbol	min/max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
Frequency Set Point Switching Time	tFC_Short	min	200								ns	1
	tFC_Middle	min	200								ns	1
	tFC_Long	min	250								ns	1
Valid Clock Requirement after entering FSP change	tCKFSPE	min	max(7.5ns, 4nCK)									
Valid Clock Requirement before 1st valid ommand after FSP change	tCKFSPX	min	max(7.5ns, 4nCK)									

Notes:
1. Frequency Set Point Switching Time depends on value of Vref(ca) setting: MR12 OP[5:0] and Vref(ca) Range: MR12 OP[6] of FSPOP
0 and 1. The details are shown in Table “tFC value maping”.
Additionally change of Frequency Set Point may affect Vref(dq) setting. Setting time of Vref(dq) level is same as Vref(ca) level.

Table — CA ODT setting timing

Parameter	Symbol	min/max	LPDDR4-1600/1866/2133/2400/3200/4267	Unit	Note
ODT CA Value Update Time	tODTUP	min	RU(20ns/tCK,avg)		

Table — Power Down timing

Parameter	Symbol	min/ max	Data Rate								Unit	Not e
			533	1066	1600	2133	2667	3200	3733	4267		
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	min	Max(7.5ns,4nCK)								-	
Delay from valid command to CKE input LOW	tCMDCKE	min	Max(1.75ns,3nCK)								ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	min	Max(5ns,5nCK)								ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	min	1.75								ns	
Valid CS Requirement after CKE Input low	tCKELCS	min	Max(5ns, 5nCK)								ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	min	Max(1.75ns, 3nCK)								ns	1
Exit power- down to next valid command delay	tXP	min	Max(7.5ns, 5nCK)								ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	min	1.75								ns	
Valid CS Requirement after CKE Input High	tCKEHCS	min	Max(7.5ns, 5nCK)								ns	1
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	min	Max(14ns, 10nCK)								ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	min	Max(1.75ns, 3nCK)								ns	1

Notes:
1. Delay time has to satisfy both analog time(ns) and clock count(nCK).
   For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 3.75ns has transpired. The case which 3nCK is applied to is shown below.

Figure — tCMDCKE Timing

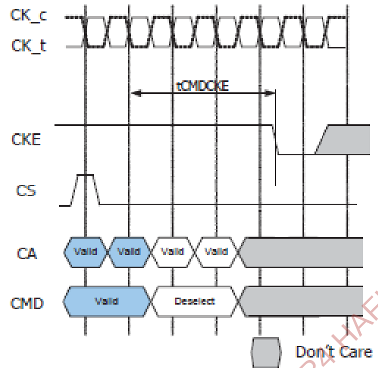


Table — PPR Timing Parameters

Parameter	Symbol	LPDDR4		Unit	Note
		Min	Max		
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting Time	tPGMPST	50	-	us	

Table — Temperature Derating for AC timing

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4267		
DQS Output access time from CK_t/CK_c (derated)	tDQSCKd	max	3600								ps	1
RAS-to-CAS delay (derated)	tRCDd	min	tRCD + 1.875								ns	1
Activate-to-Activate command period (derated)	tRCd	min	tRC + 3.75								ns	1
Row active time (derated)	tRASd	min	tRAS + 1.875								ns	1
Row precharge time (derated)	tRPd	min	tRP + 1.875								ns	1
Active bank A to Active bank B (derated)	tRRDd	min	tRRD + 1.875								ns	1

Notes:
1. Timing derating applies for operation at 85°C to 95°C

1.3.4 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table — Command Truth Table

Command	SDR Command Pins	DDR CA Pins (10)						CK_tedge	Notes
	CS_n	CA0	CA1	CA2	CA3	CA4	CA5		
Deselect (DES)	L	X						R1	1,2
Multi Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,2,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write-1	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write-1	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read-1	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2 or Mask Write-2 or Read-2 or MRR-2)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
MRW-1	H	L	H	H	L	L	OP7	R1	1,2,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
MRW-2	H	L	H	H	L	H	OP6	R1	1,2,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
MRR-1	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

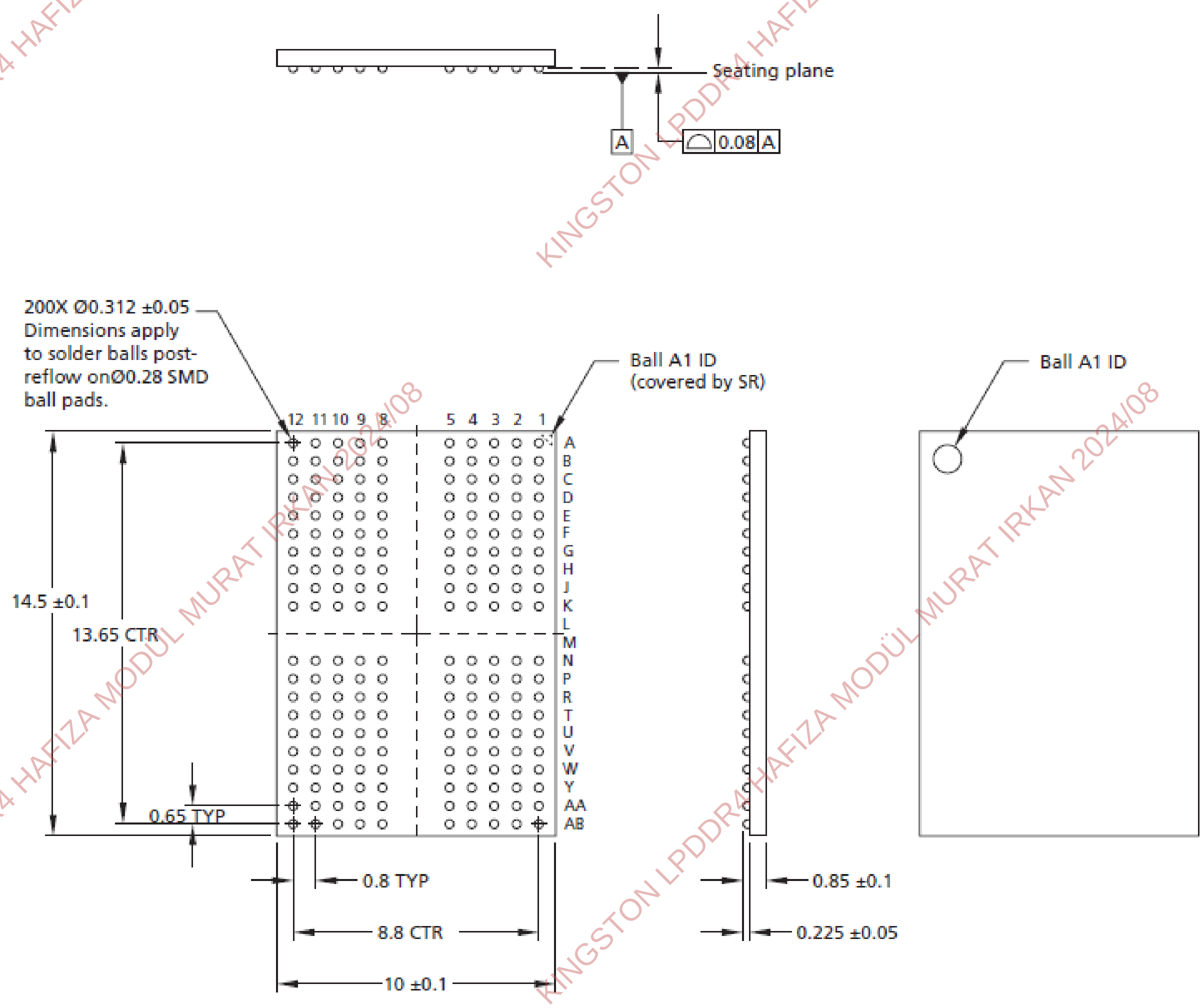
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate-1	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	V	R10	R11	R2	
Activate-2	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Notes

1. All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don’t care in which case CS, CK_t, CK_c and CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don’t care.
5. Mask Write-1 command supports only BL 16. For Mark Write-1 comamnd, CA5 must be driven LOW on first rising clock cycle (R1).
6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

2. Package Mechanical

2.1. 200 ball FBGA (10 x 14.5 x 1.0mm max)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with NiAu pads (Sn3Ag0.2Cu).

3. Ball Assignment

3.1. 200 balls assignment

0.80 mm Pitch

0.65 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT(ca)_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT(ca)_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.
NOTE 5 Die pad VSS and VSSQ signals are combined to VSS package balls.
NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_x.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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