


BPI_F3_LP4XP200_32X1

Revision	Date	Change Description
V1.0	20231207	Initial version
V2.0	20240131	Update based on test results
V3.0	20240401	Update based on test results

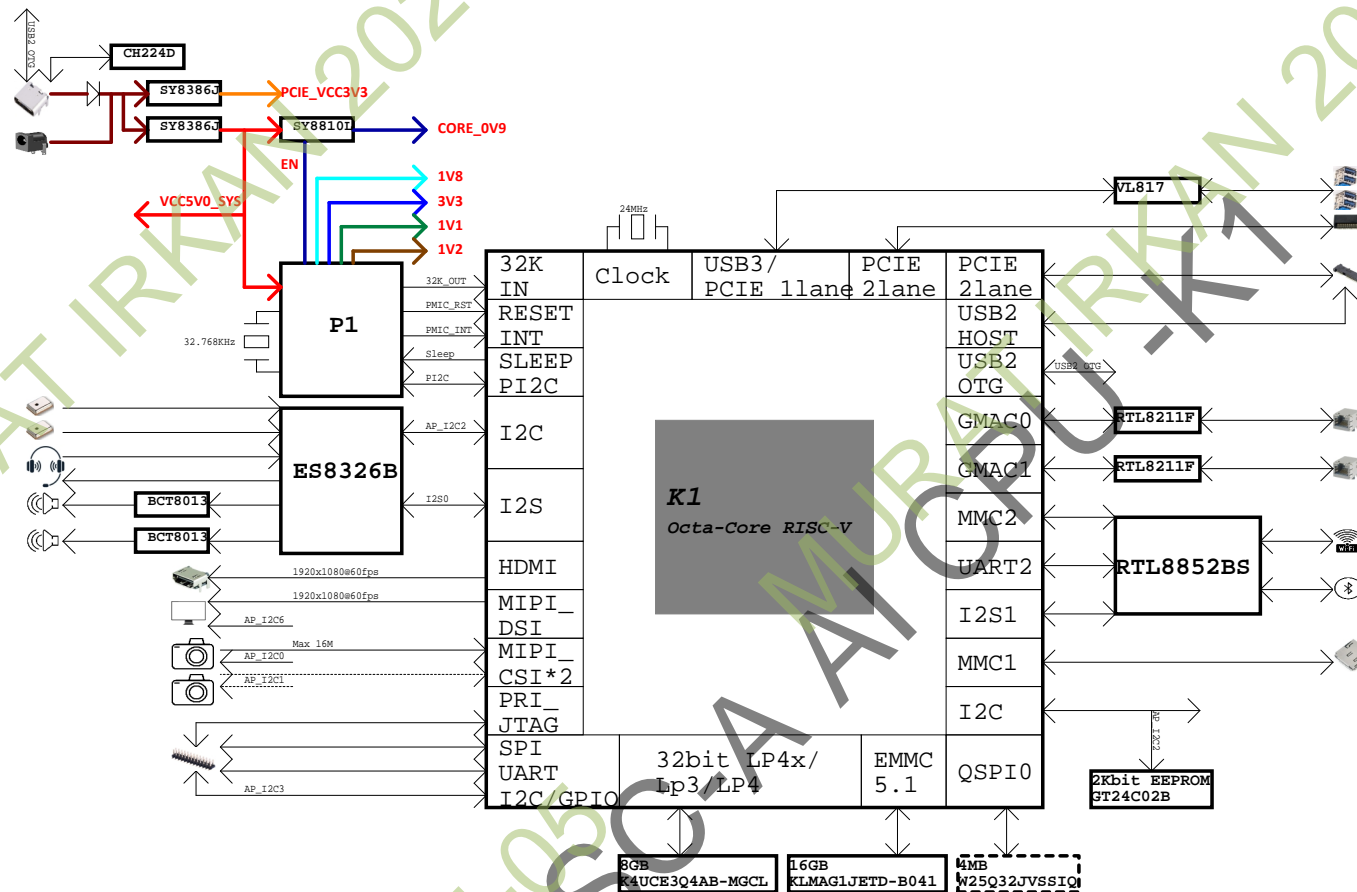
			
GUANGDONG BIPAI KEJI CPA.LTD			
Design Name			
BPI-F3_LP4XP200_32X1			
Size	Page Name		Rev
A3	01 REVISION HISTORY		<RevCode>
Date:	Wednesday, May 08, 2024		Sheet 1 of 28

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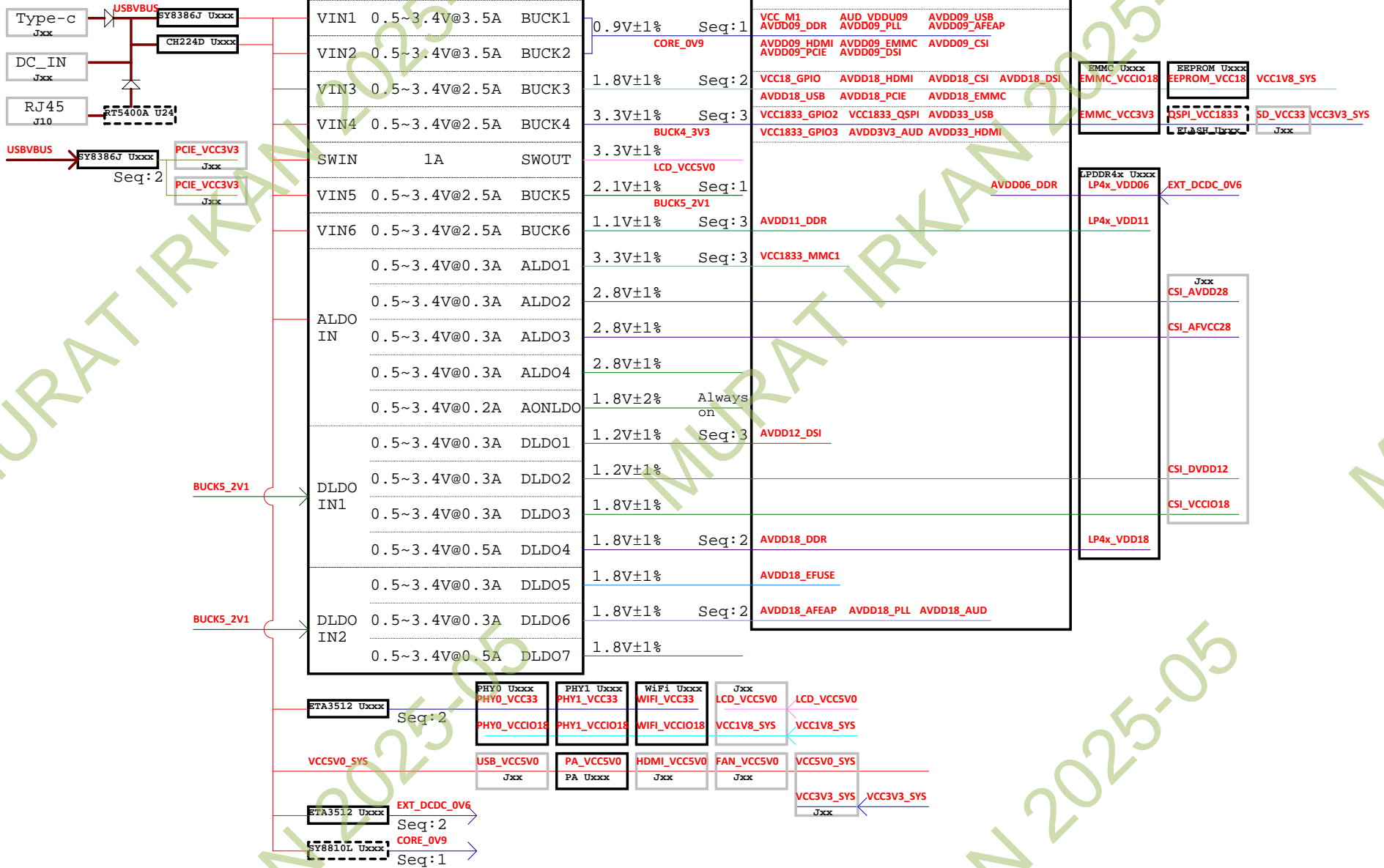
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BLOCK

RISC-V 64-BIT K1 CPU : YAPAY ZEKA BİLGİSAYAR-K1

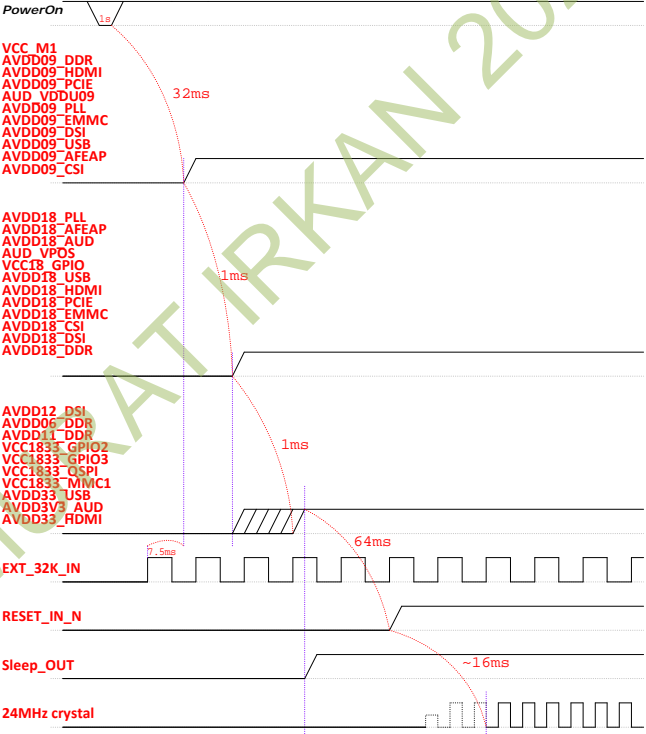


POWER TREE



POWER SEQUENCE

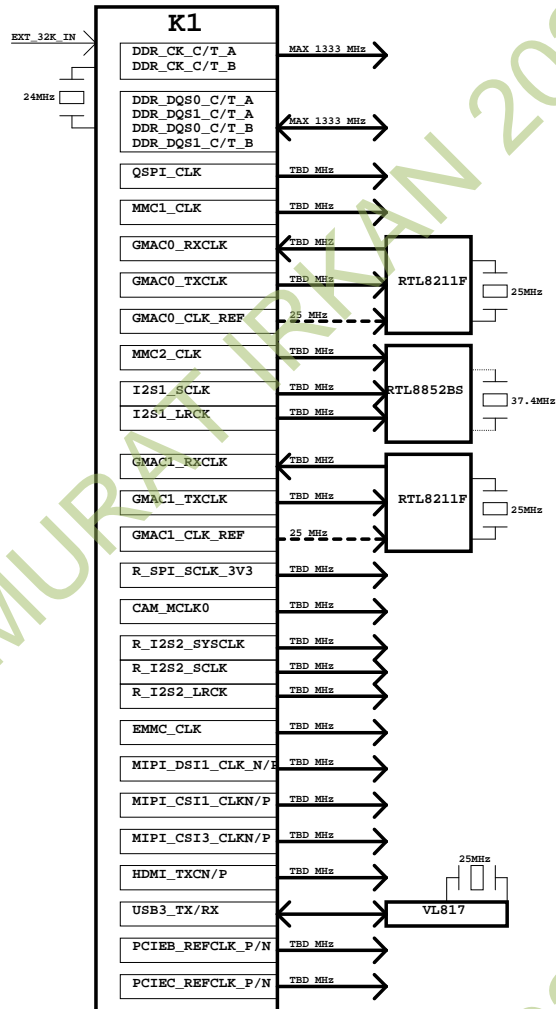
Control by PMIC
冷起自动上电，后续长按关机，短按开机



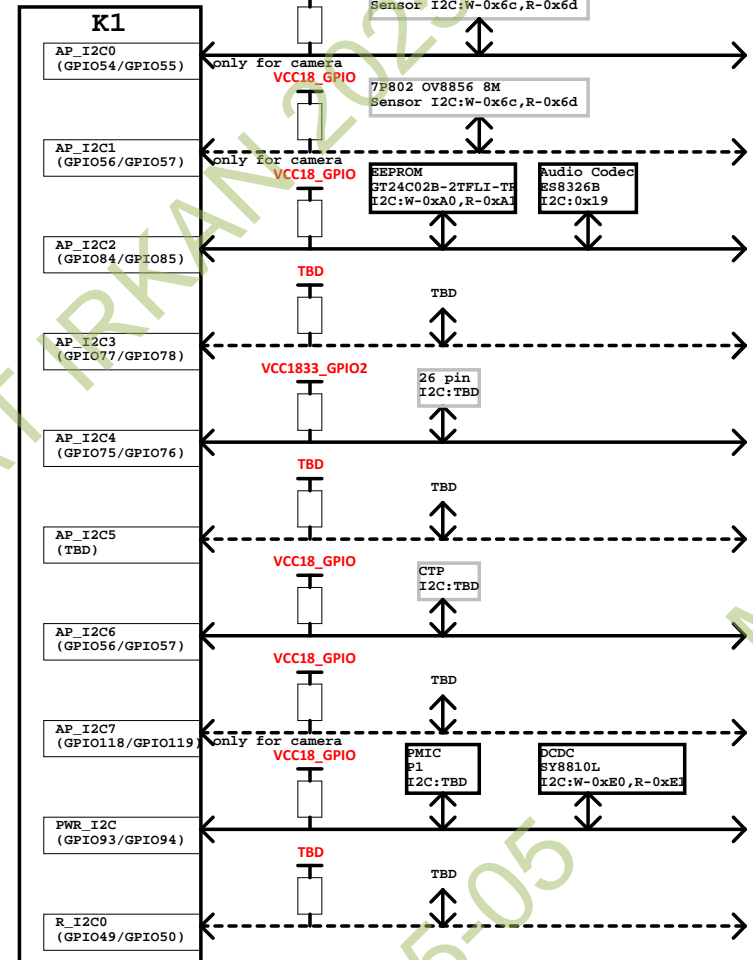
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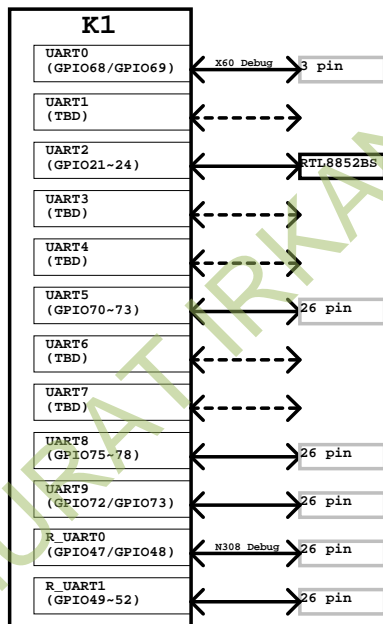
CLOCK MAP



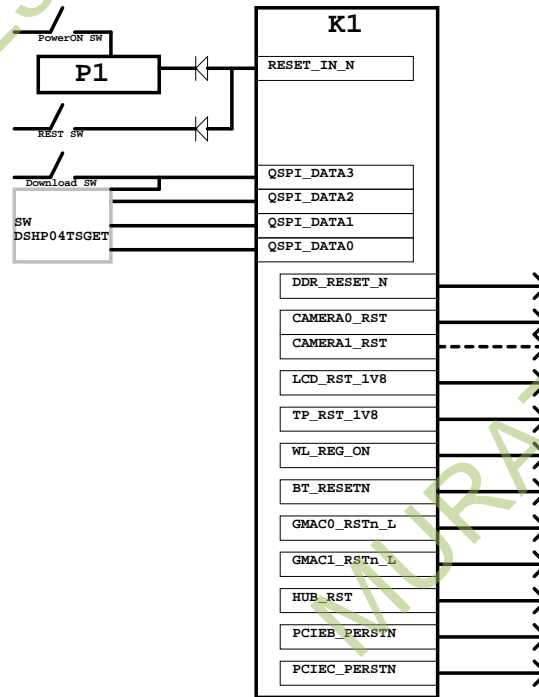
I2C MAP



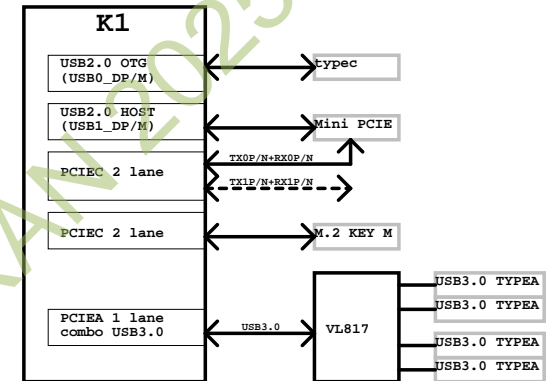
UART MAP



SW&RESET MAP



PCIE/USB MAP



GPIO ASSIGNMENT

PIN	Define	CFG	Function
GPIO0	GMAC0_RXDV	1	Ethernet -GMAC0
GPIO1	GMAC0_RXD0	1	
GPIO2	GMAC0_RXD1	1	
GPIO3	GMAC0_RXCLK	1	
GPIO4	GMAC0_RXD2	1	
GPIO5	GMAC0_RXD3	1	
GPIO6	GMAC0_TXD0	1	
GPIO7	GMAC0_TXD1	1	
GPIO8	GMAC0_TXCLK	1	
GPIO9	GMAC0_TXD2	1	
GPIO10	GMAC0_TXD3	1	
GPIO11	GMAC0_TXEN	1	
GPIO12	GMAC0_MDC	1	
GPIO13	GMAC0_MDIO	1	
GPIO14	GMAC0_INT_N	1	WiFi/BT
GPIO15	MMC2_DATA3	1	
GPIO16	MMC2_DATA2	1	
GPIO17	MMC2_DATA1	1	
GPIO18	MMC2_DATA0	1	
GPIO19	MMC2_CMD	1	
GPIO20	MMC2_CLK	1	
GPIO21	UART2_TXD	1	
GPIO22	UART2_RXD	1	
GPIO23	UART2_CTS_N	1	
GPIO24	UART2_RTS_N	1	
GPIO25	I2S1_SCLK	1	
GPIO26	I2S1_LRCK	1	
GPIO27	I2S1_TXD	1	Ethernet -GMAC1
GPIO28	I2S1_RXD	1	
GPIO29	GMAC1_RXDV	1	
GPIO30	GMAC1_RXD0	1	
GPIO31	GMAC1_RXD1	1	
GPIO32	GMAC1_RXCLK	1	
GPIO33	GMAC1_RXD2	1	
GPIO34	GMAC1_RXD3	1	
GPIO35	GMAC1_TXD0	1	
GPIO36	GMAC1_TXD1	1	
GPIO37	GMAC1_TXCLK	1	
GPIO38	GMAC1_TXD2	1	
GPIO39	GMAC1_TXD3	1	
GPIO40	GMAC1_TXEN	1	LCD/CTP
GPIO41	GMAC1_MDC	1	
GPIO42	GMAC1_MDIO	1	
GPIO43	GMAC1_INT_N	1	
GPIO44	LCD_BL_PWM_1V8	4	
GPIO45	GMAC0_CLK_REF	1	GMAC0
GPIO46	GMAC1_CLK_REF	1	GMAC1

PIN	Define	CFG	Function
GPIO110	GMAC0_RSTn_L	0	GMAC0
GPIO115	GMAC1_RSTn_L	0	GMAC1
GPIO116	WL_DIS_N	0	WiFi/BT
GPIO117	PCIEC_CLKREQN	4	PCIEC
GPIO118	I2S0_SCLK	3	Audio Codec
GPIO119	I2S0_LRCK	3	
GPIO120	I2S0_OUT	3	
GPIO121	I2S0_IN	3	USB3_HUB
GPIO122	I2S0_SYSCLK	3	
GPIO123	HUB_PWREN	0	USB2
GPIO124	HUB_RST	0	
GPIO125	VBUS_ON0	1	Audio Codec
GPIO126	CODEC_IRQ	0	
GPIO127	PA_SHUTDOWN	0	

PIN	Define	CFG	Function
GPIO53	CAM_MCLK0	1	CAMERA0
GPIO54	CAM_I2C0_SCL	1	
GPIO55	CAM_I2C0_SDA	1	
GPIO56	AP_I2C6_SCL	5	LCD/CTP
GPIO57	AP_I2C6_SDA	5	
GPIO58	TP_INT_1V8	0	CAMERA0
GPIO111	CAMERA0_RST	1	
GPIO112	PCIEC_WAKEN	3	PCIEC
GPIO113	CAMERA0_PDN	1	CAMERA0
GPIO114	TP_RST_1V8	0	LCD/CTP
GPIO63	BT_RESETN	0	WiFi/BT
GPIO64	AP_WAKE_BT	0	
GPIO65	BT_WAKE_AP	0	
GPIO66	WL_WAKE_AP	0	
GPIO67	WL_REG_ON	0	X60 Debug
GPIO68	UART0_TXD	2	
GPIO69	UART0_RXD	2	

PIN	Define	CFG	Function
GPIO59	PCIEB_PERSTN	4	PCIEB
GPIO60	PCIEB_WAKEN	4	
GPIO61	PCIEB_CLKREQN	4	
GPIO62	PCIEC_PERSTN	4	PCIEC
GPIO70	GPIO70	1	26 pin
GPIO71	GPIO71	1	
GPIO72	GPIO72	1	
GPIO73	GPIO73	1	
GPIO74	GPIO74	0	

红色字体GPIO表示默认、持续上拉，等效上拉电阻约60K。需要软件修改才能解除默认上拉状态

PIN	Define	CFG	Function
GPIO93	PI2C_SCL	0	PMIC
GPIO94	PI2C_SDA	0	
GPIO95	SLEEP_OUT	0	LED
GPIO96	GPIO96	1	
GPIO97	USB3_PWREN	1	USB3_HUB
GPIO81	LCD_RST_1V8	0	LCD/CTP
GPIO82	LCD_BL_EN_1V8	0	
GPIO83	LCD_PWR_EN_1V8	0	EEPROM Audio
GPIO84	AP_I2C2_SCL	4	
GPIO85	AP_I2C2_SDA	4	HDMI_OUT
GPIO86	HDMI_SCL	1	
GPIO87	HDMI_SDA	1	
GPIO88	HDMI_CEC	1	26 pin
GPIO89	HDMI_HPD	1	
GPIO90	GPIO90	0	
GPIO91	GPIO91	0	
GPIO92	GPIO92	0	

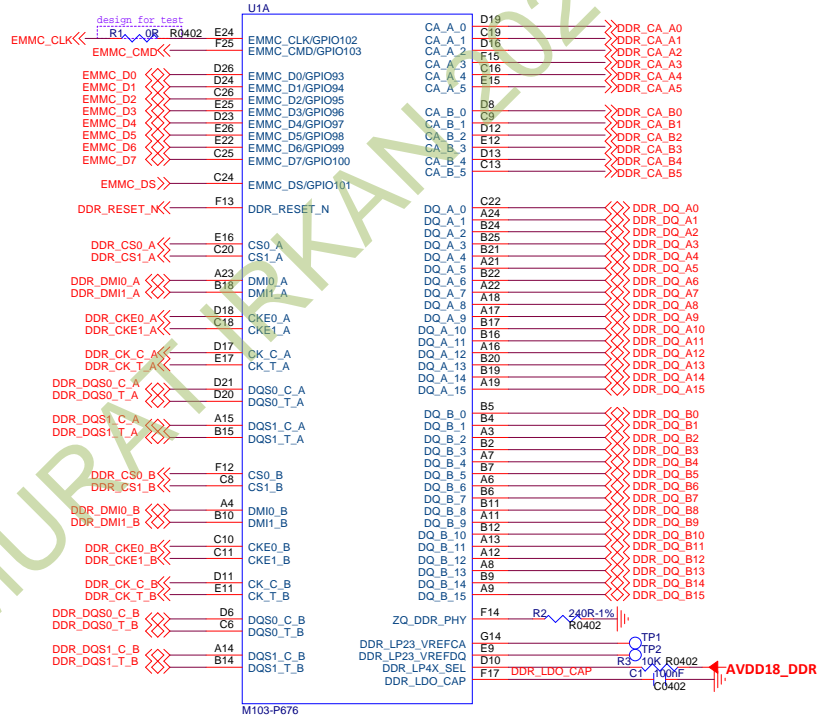
PIN	Define	CFG	Function
GPIO98	QSPI_DATA3	0	SPI FLASH
GPIO99	QSPI_DATA2	0	
GPIO100	QSPI_DATA1	0	
GPIO101	QSPI_DATA0	0	
GPIO102	QSPI_CLK	0	
GPIO103	QSPI_CS1	0	

PIN	Define	CFG	Function
GPIO104	MMC1_DATA3	0	TF CARD
GPIO105	MMC1_DATA2	0	
GPIO106	MMC1_DATA1	0	
GPIO107	MMC1_DATA0	0	
GPIO108	MMC1_CMD	0	
GPIO109	MMC1_CLK	0	

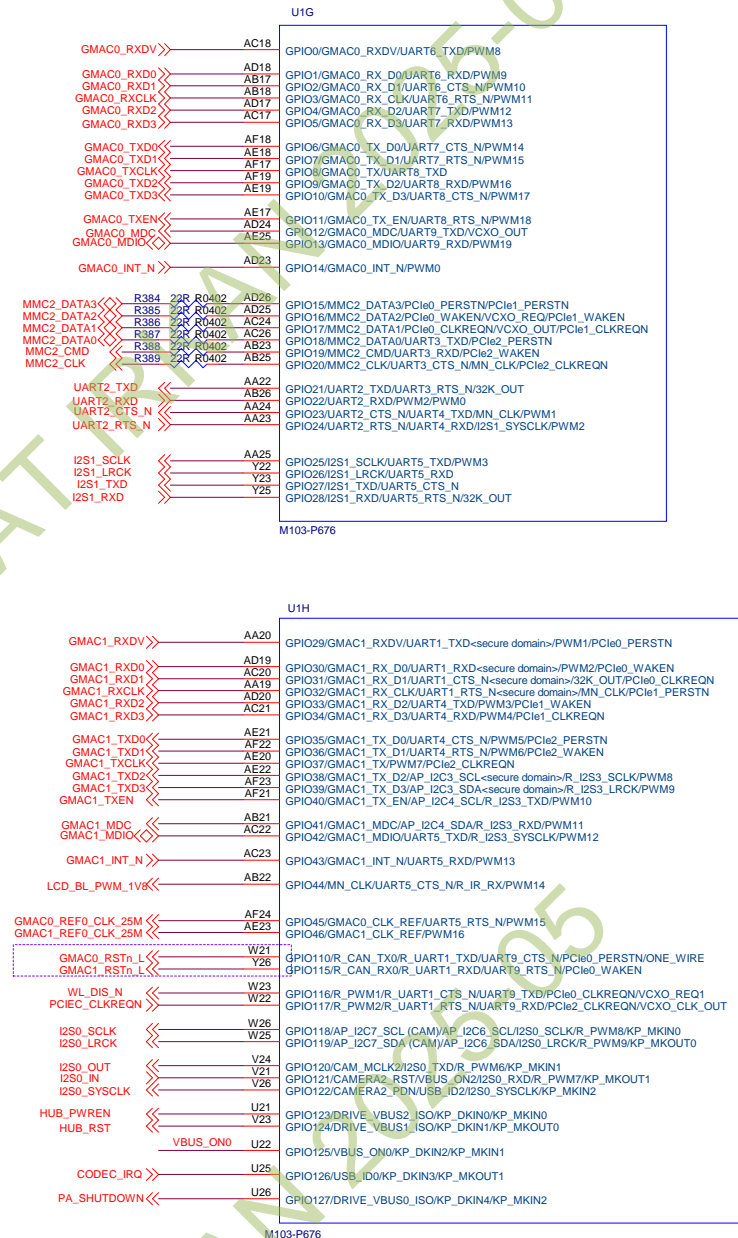
PIN	Define	CFG	Function
GPIO75	SPI3_SCLK_3V3	2	26 pin
GPIO76	SPI3_CS_3V3	2	
GPIO77	SPI3_MOSI_3V3	2	
GPIO78	SPI3_MISO_3V3	2	
GPIO79	FAN_PWM	2	FAN
GPIO80	SD_CD_3V3	1	TF CARD

PIN	Define	CFG	Function
GPIO47	R_UART0_TXD_3V3	1	26 pin
GPIO48	R_UART0_RXD_3V3	1	
GPIO49	GPIO_49_3V3	0	
GPIO50	GPIO_50_3V3	0	
GPIO51	AP_I2C4_SCL_3V3	4	
GPIO52	AP_I2C4_SDA_3V3	4	

eMMC+DDR

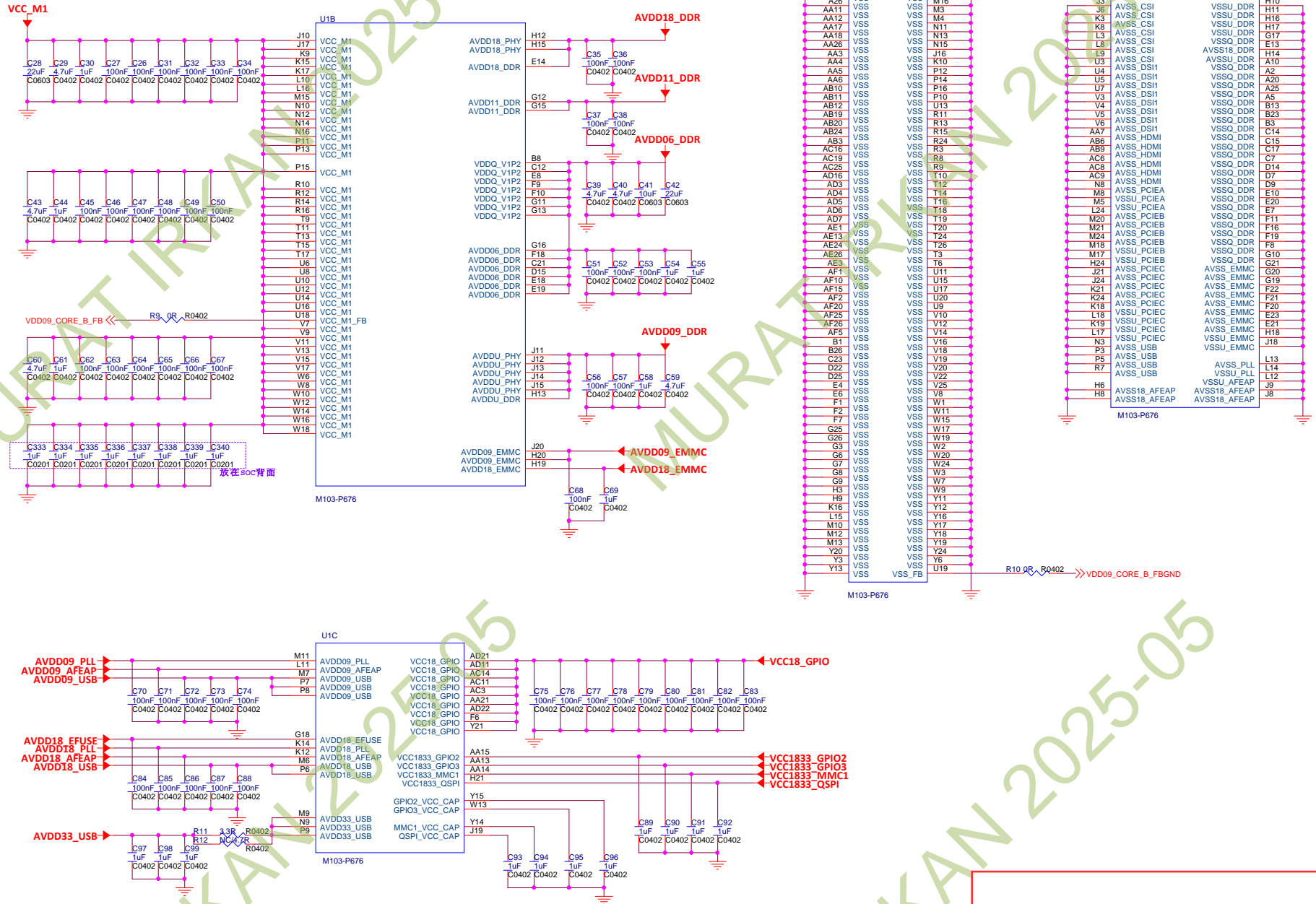


GPIO

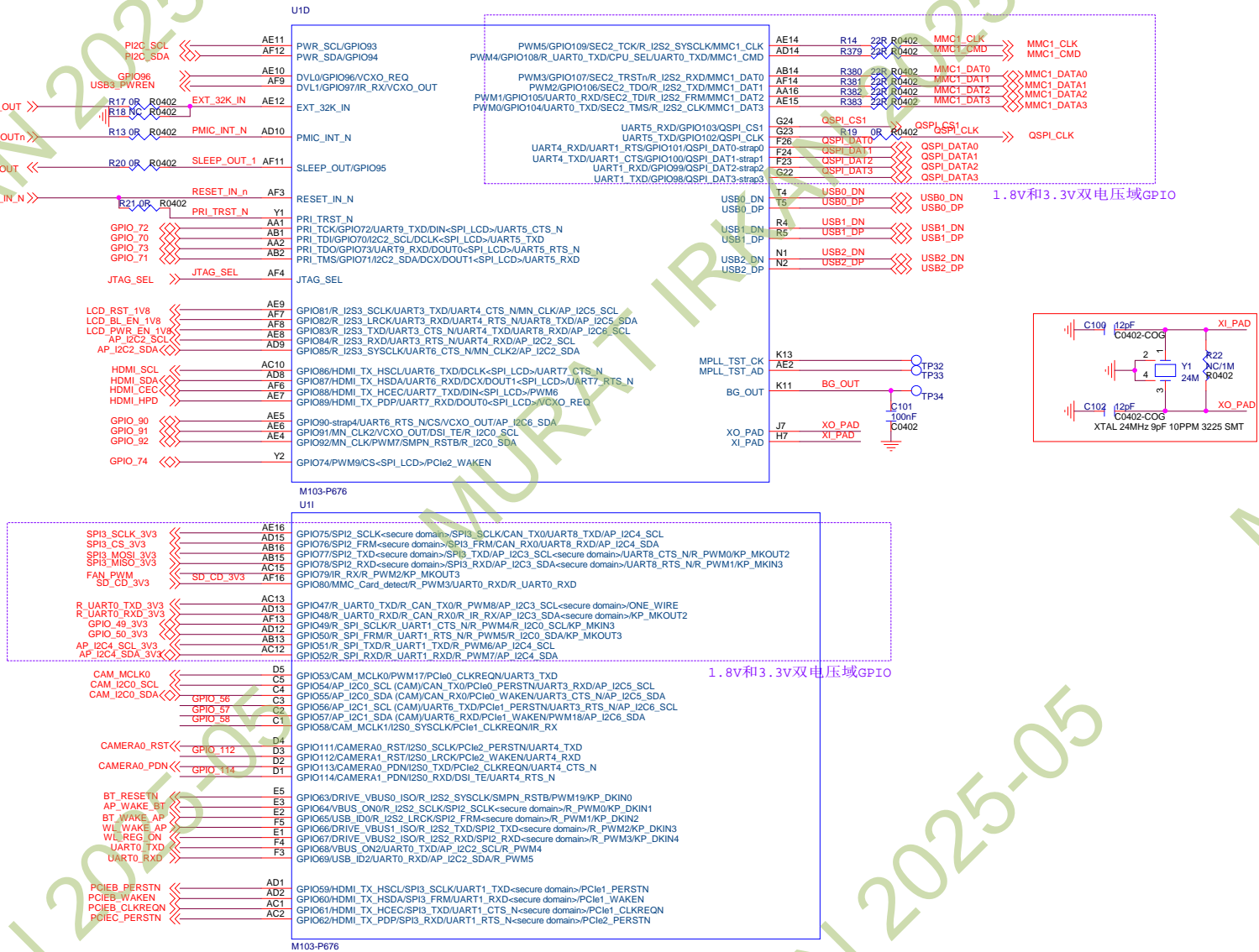
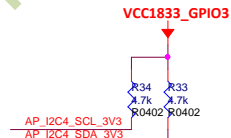
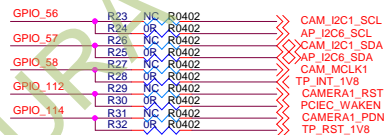
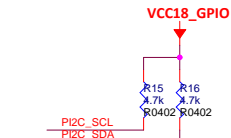


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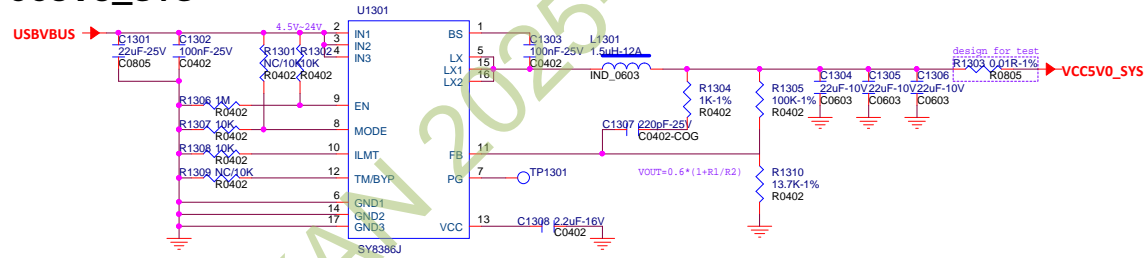
CPU-PWR



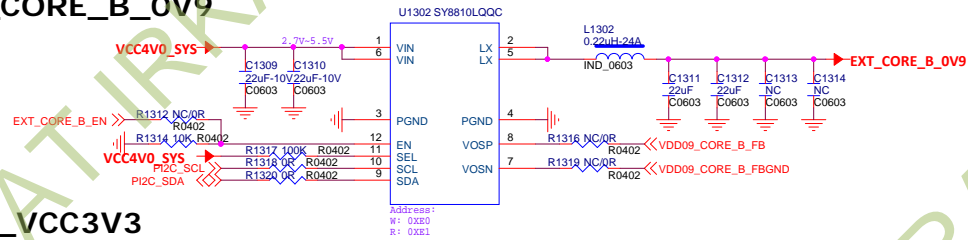
SYS-GPIO



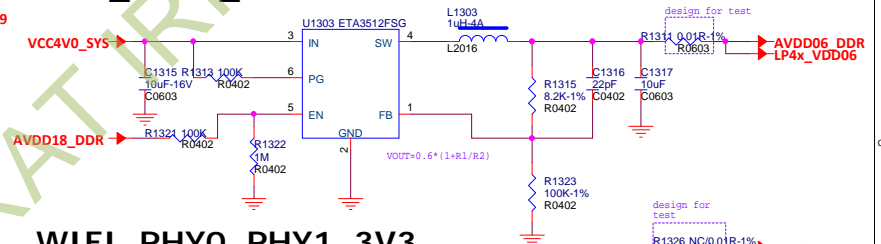
VCC5V0_SYS



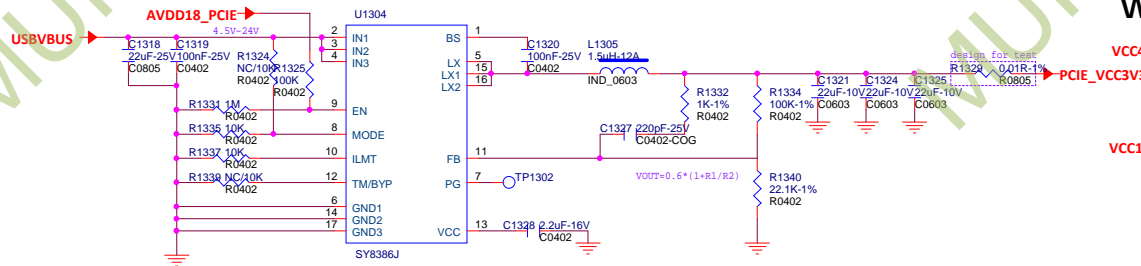
EXT_CORE_B_0V9



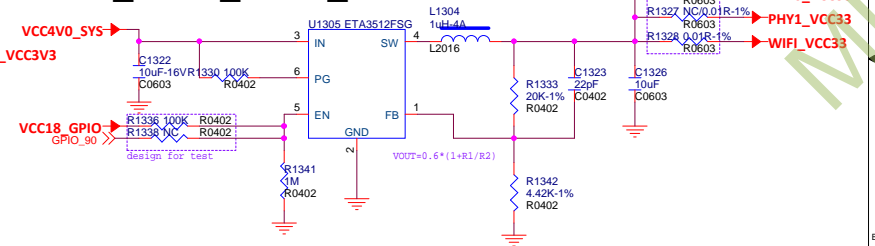
EXT_DCDC_0V6



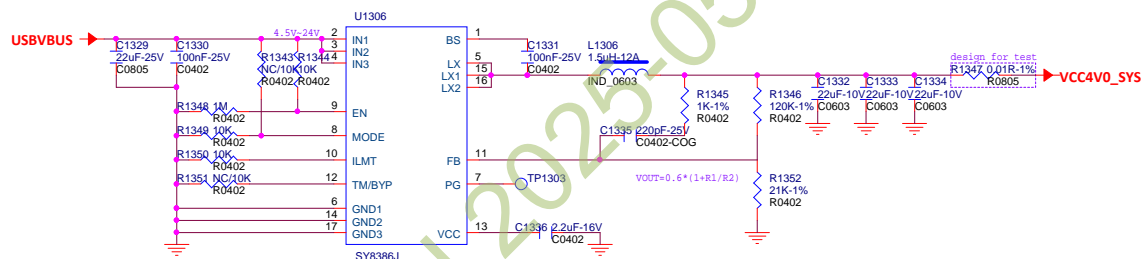
PCIE_VCC3V3



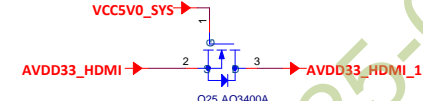
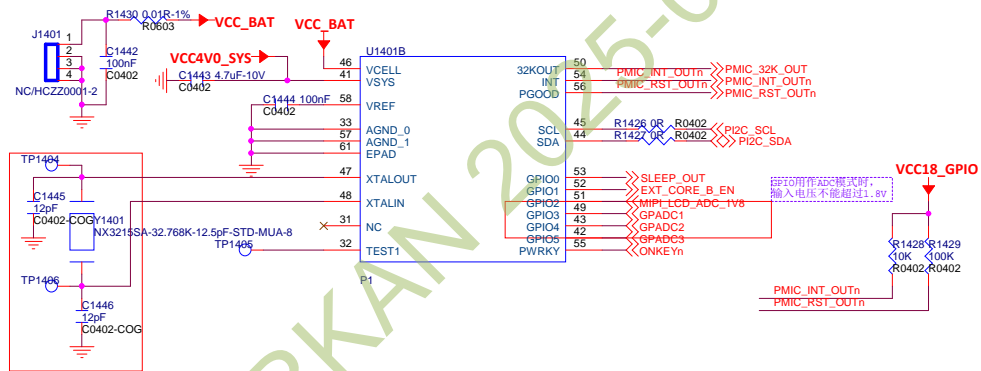
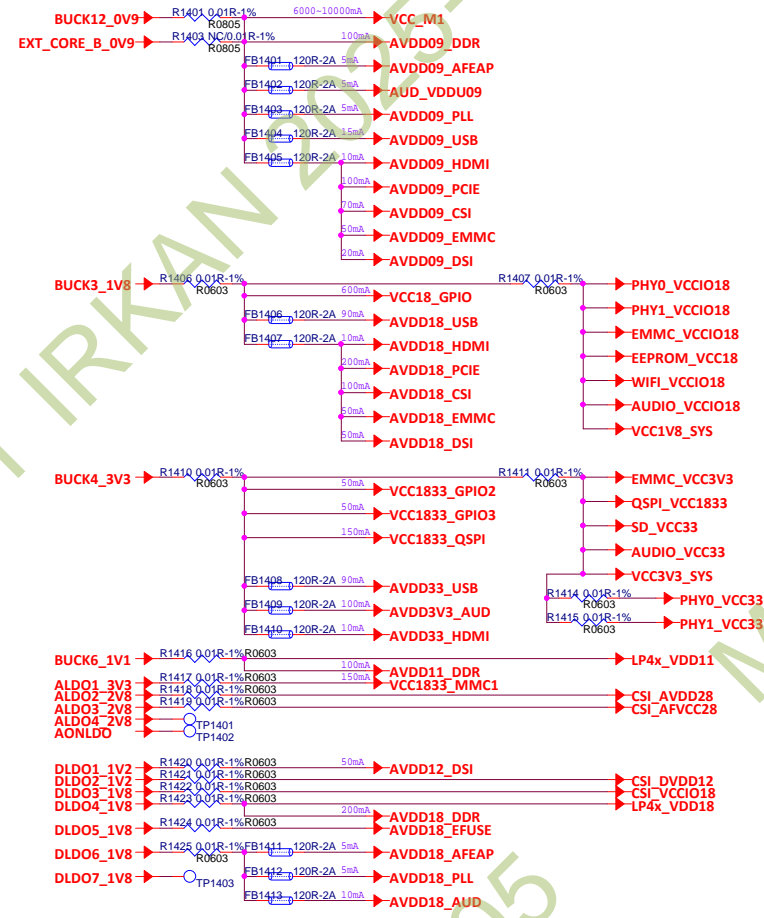
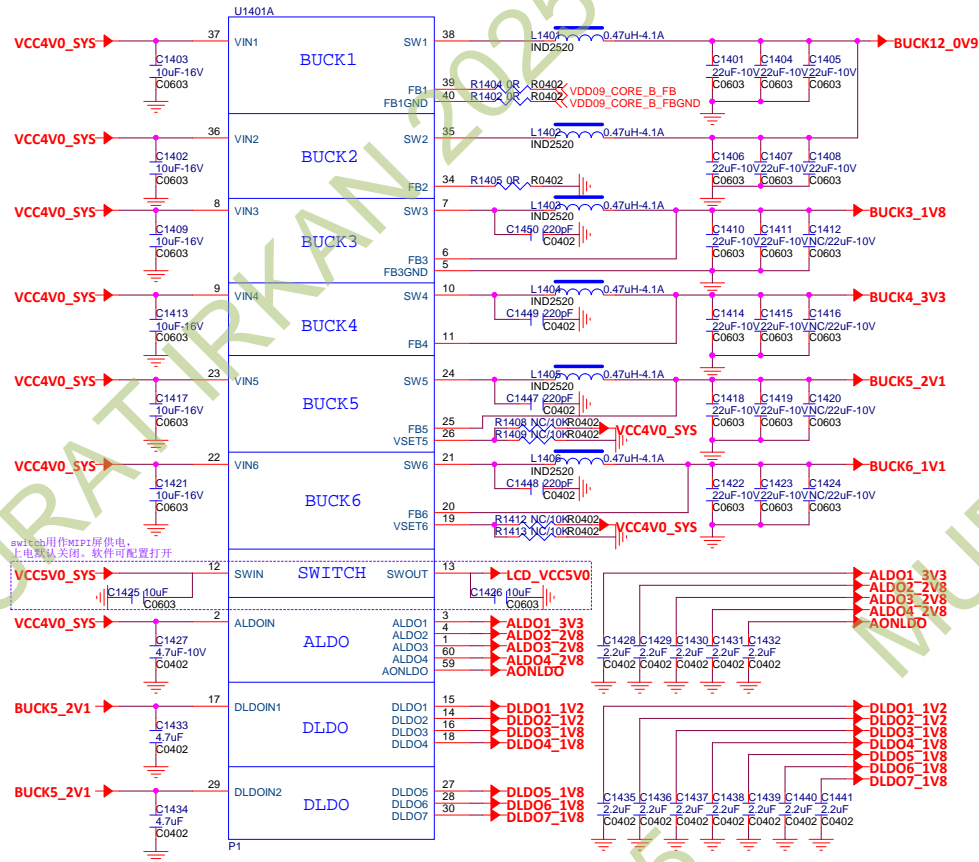
WIFI_PHY0_PHY1_3V3



VCC4V0_SYS

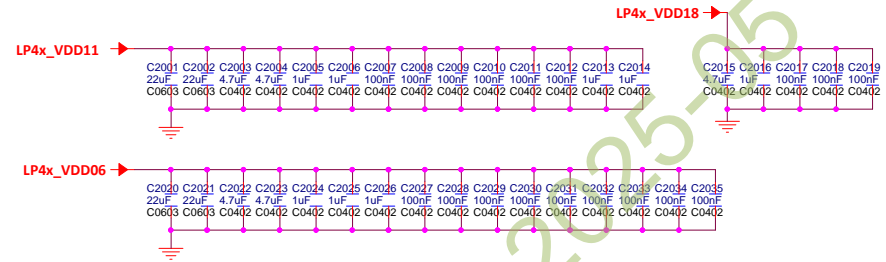
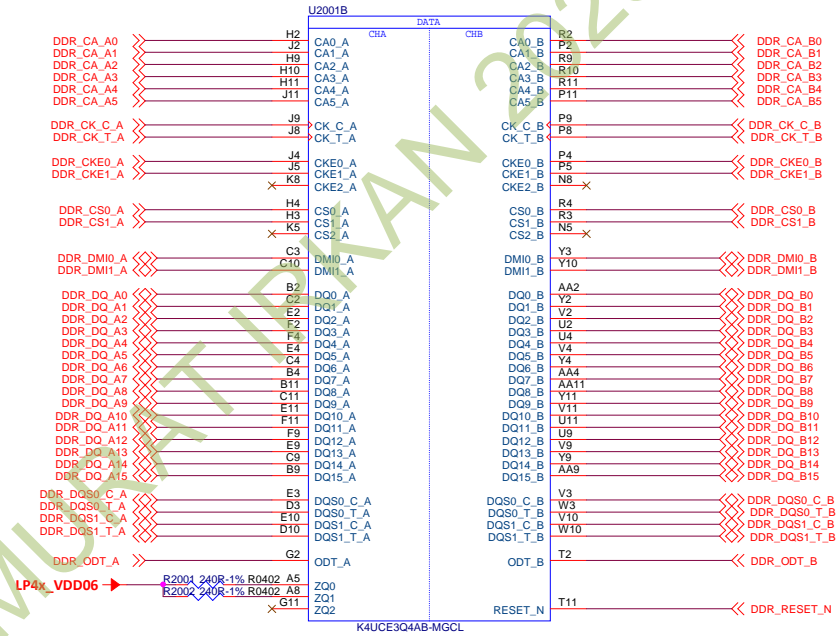
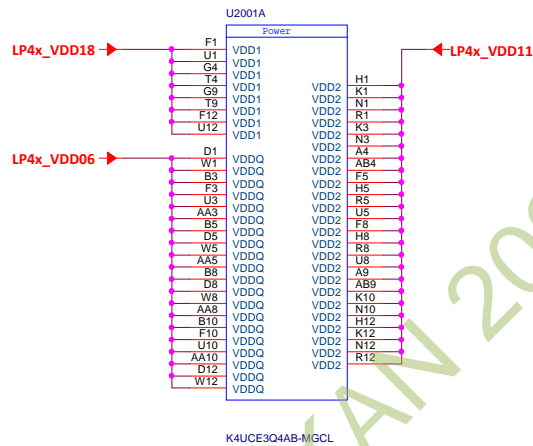
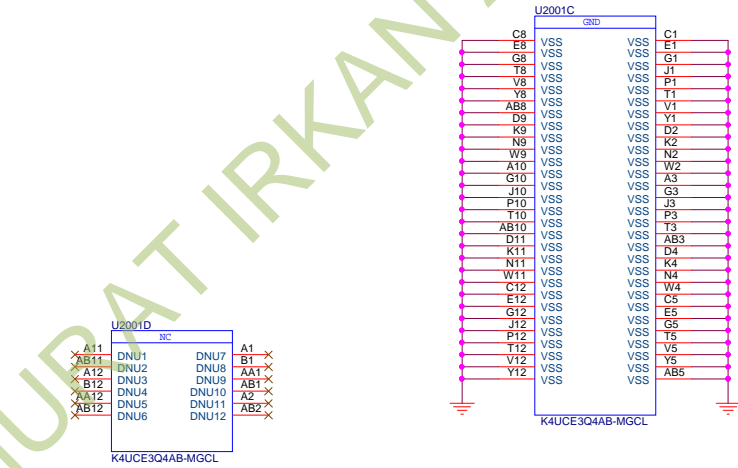


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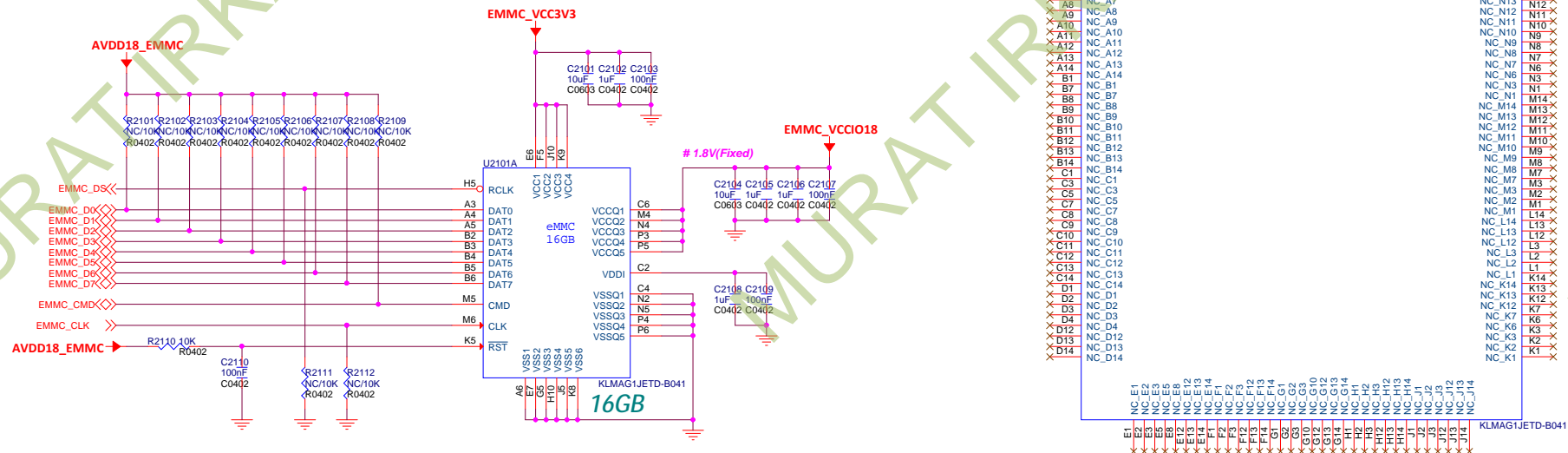


LPDDR4X

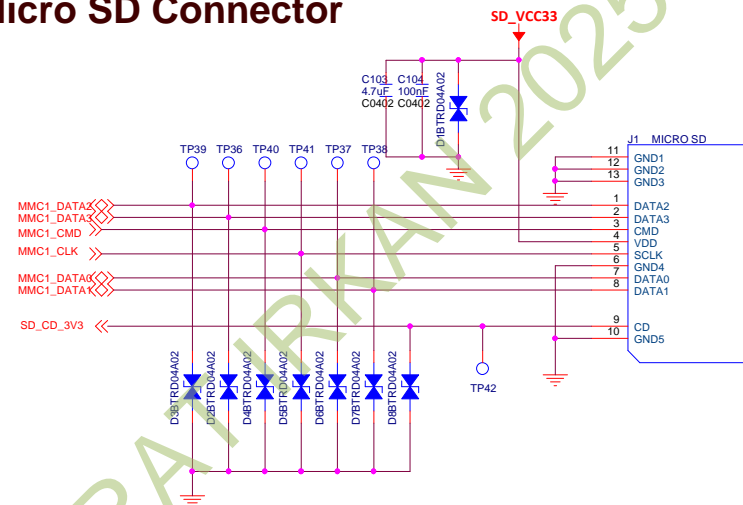
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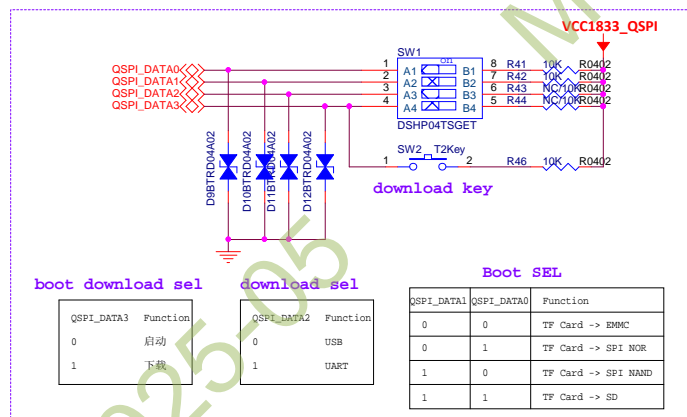
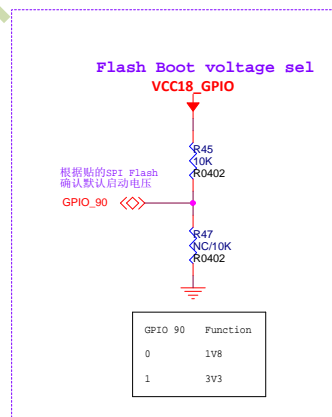
EMMC



Micro SD Connector



The schematic diagram illustrates the VCC1833_QSPI interface. It features a 1.8V QSPI flash (U3, NCW25Q32JVSSIQ) connected to a 3.3V VCC1833_QSPI supply. The QSPI signals (CS, SCLK, D0-D3) are connected to the flash's CS, SCLK, and data pins. The flash's VCC and GND pins are connected to the 3.3V supply and ground, respectively. The flash's I/O pins are connected to the 3.3V supply through 100nF capacitors (C106, C107, C402, C0402).



QSPI_DATA1	QSPI_DATA0	Function
0	0	TF Card -> EMMC
0	1	TF Card -> SPI NOR
1	0	TF Card -> SPI NAND
1	1	TF Card -> SD

CAMERA

VCC18_GPIO

Differential pairs
Z0= 100 ohm
Design for ESD test,
Option for cost down

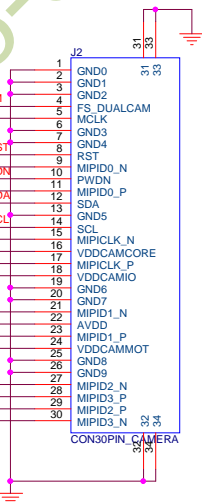
VCC18_GPIO

R48 NC 100K R0402
R49 100K R0402
R50 4.7K R0402
R51 100K R0402

CSI_AFVCC28 CSI_AVDD28 CSI_VCCIO18 CSI_DVDD12

C109 1uF C0402
C110 4.7uF C0402
C111 1uF C0402
C112 1uF C0402
C113 NC C0402

TP45 FS_DUALCAM
CAM_MCLK0
CAMERA0_RST
MIPI_CSH1_DN0
CAMERA0_PDN
MIPI_CSH1_DP0
CAM_I2C0_SDA
CAM_I2C0_SCL
MIPI_CSH1_CLKP
CSI_DVDD12
CSI_VCCIO18
MIPI_CSH1_DN1
CSI_AVDD28
MIPI_CSH1_DP1
CSI_AFVCC28
MIPI_CSH1_DN2
MIPI_CSH1_DP3
MIPI_CSH1_DP2
MIPI_CSH1_DN3



VCC18_GPIO

Differential pairs
Z0= 100 ohm
Design for ESD test,
Option for cost down

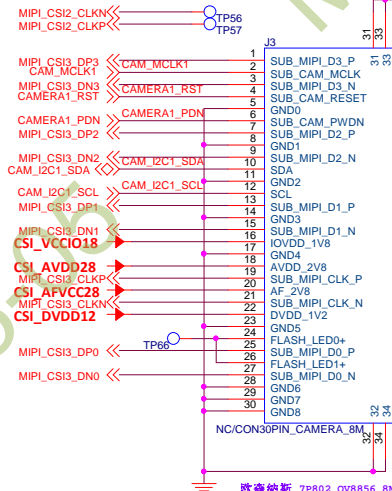
VCC18_GPIO

R52 NC 100K R0402
R53 100K R0402
R54 4.7K R0402
R55 100K R0402

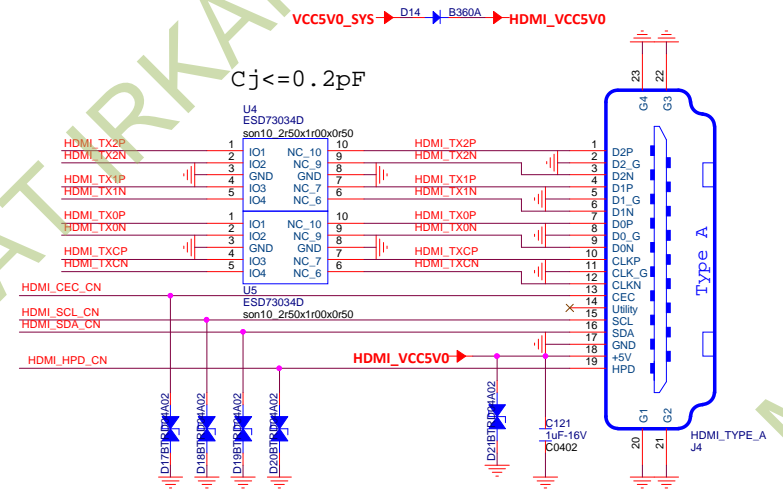
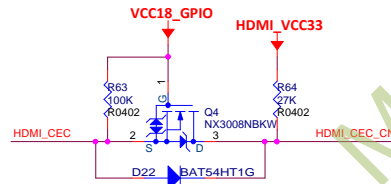
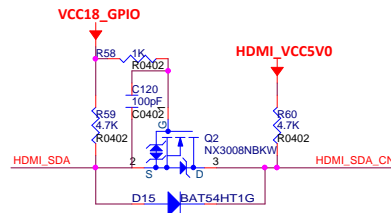
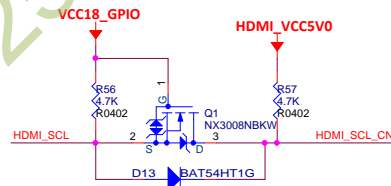
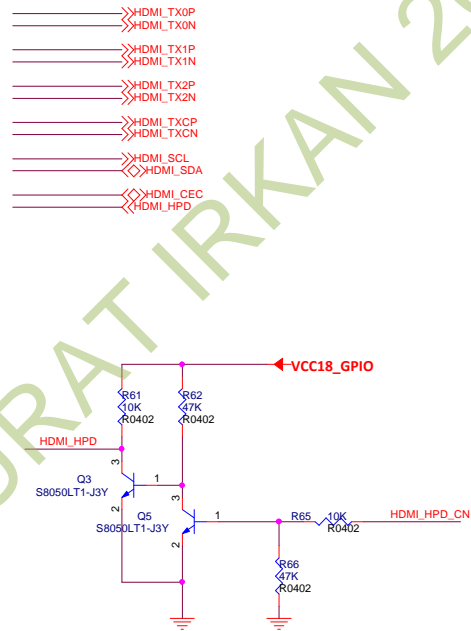
CSI_AFVCC28 CSI_AVDD28 CSI_VCCIO18 CSI_DVDD12

C115 1uF C0402
C116 4.7uF C0402
C117 1uF C0402
C118 1uF C0402
C119 NC C0402

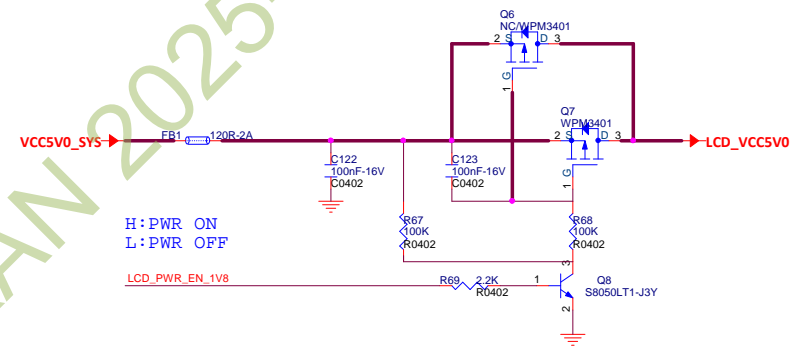
MIPI_CSI2_CLKP
MIPI_CSI2_CLKP
MIPI_CSI3_DP3
CAM_MCLK1
MIPI_CSI3_DN3
CAMERA1_RST
CAMERA1_PDN
MIPI_CSI3_DP2
CAM_I2C1_SDA
CAM_I2C1_SCL
MIPI_CSI3_DP1
MIPI_CSI3_DN1
CSI_VCCIO18
CSI_AVDD28
MIPI_CSI3_CLKP
CSI_AFVCC28
MIPI_CSI3_CLKP
CSI_DVDD12
MIPI_CSI3_DP0
MIPI_CSI3_DN0



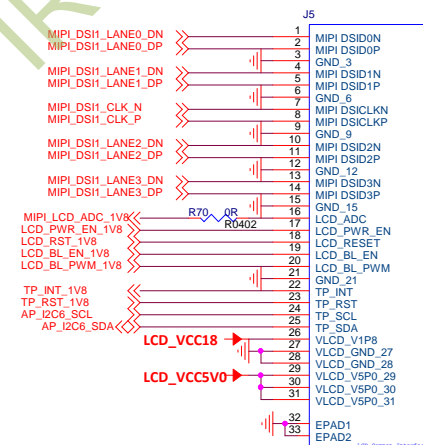
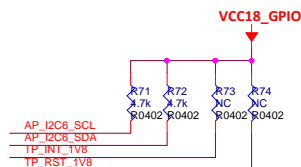
HDMI



MIPI-DSI



VCC1V8_SYS → FB2 120R-2A → LCD_VCC18



FH35C-31S-0.3SHW

RTL8852BS

XTAL_XON R89 NC/0R

Y2

XIN GND1 XOUT GND2

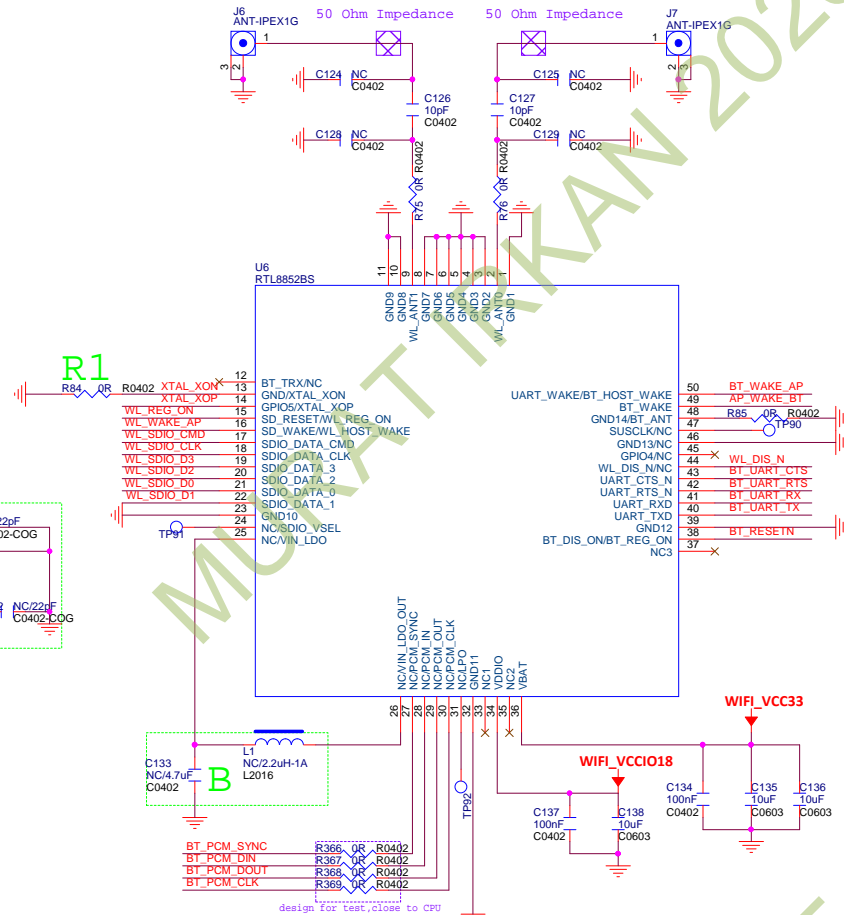
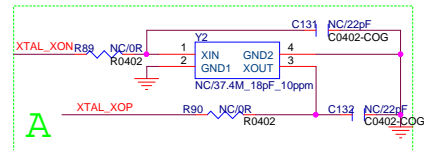
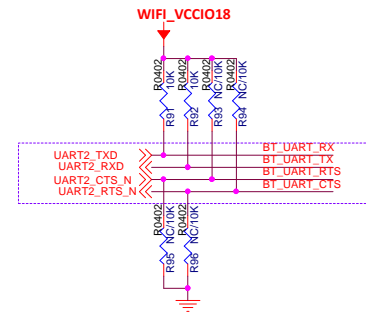
NC/37.4M_18pF_10ppm

XTAL_XOP R90 NC/0R

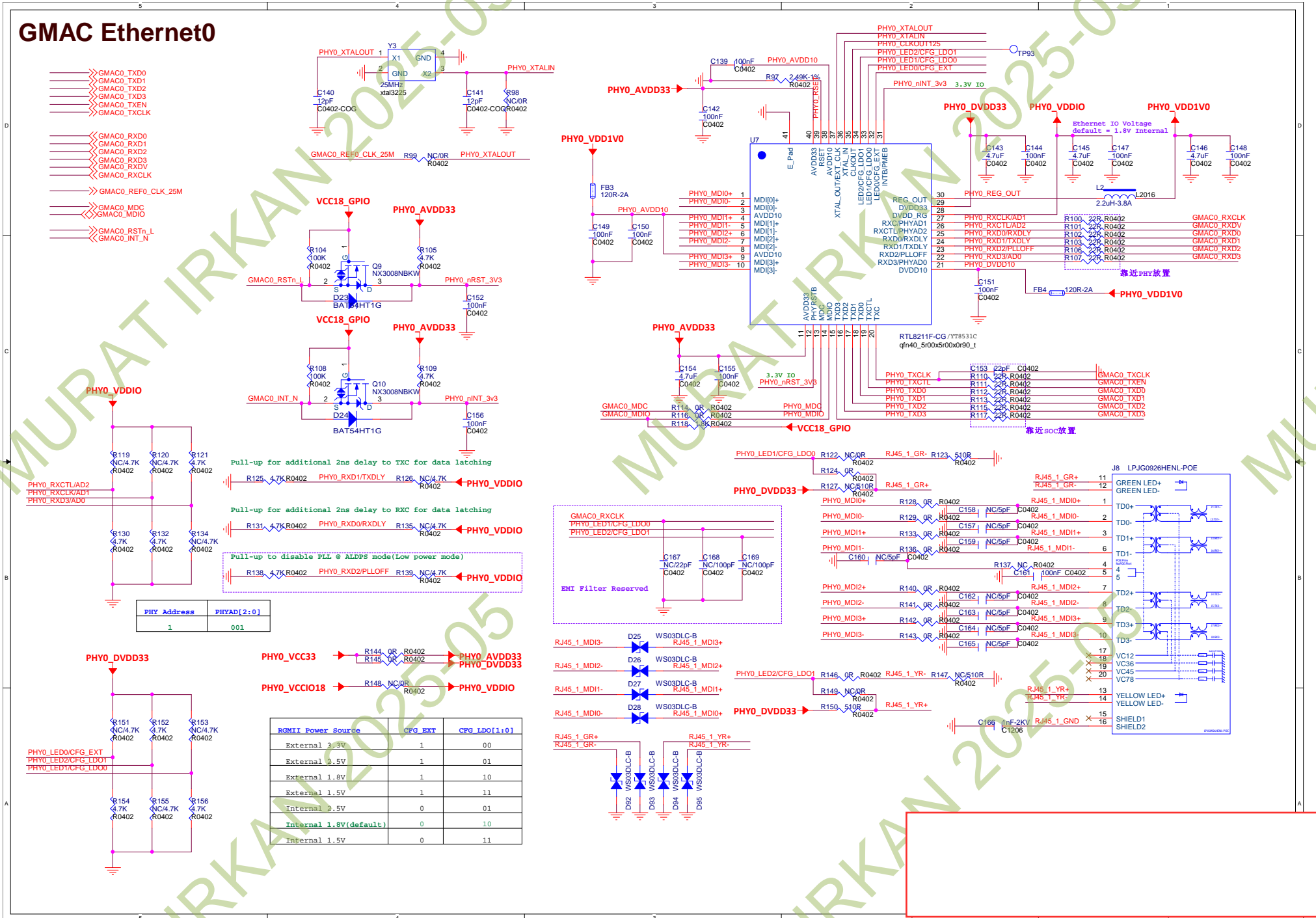
C131 NC/2 C040

C132

A



GMAC Ethernet0



GMAC Ethernet1

The schematic diagram illustrates the GMAC Ethernet1 interface, showing the connection between the PHY1 and GMAC1 blocks. The PHY1 block is connected to the GMAC1 block via various signal lines, including TX, RX, and control signals. The PHY1 block is also connected to power supplies (PHY1_VDDIO, PHY1_VDD33, PHY1_AVDD33) and ground. The GMAC1 block is connected to the PHY1 block via various signal lines, including TX, RX, and control signals. The GMAC1 block is also connected to power supplies (GMAC1_VDDIO, GMAC1_VDD33, GMAC1_AVDD33) and ground. The diagram includes a table for PHY Address and PHYAD[2:0], and a table for RGMII Power Source, CFG_EXT, and CFG_LDO[1:0].

PHY Address	PHYAD[2:0]
1	001

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(default)	0	10
Internal 1.5V	0	11

GMAC Ethernet1

The schematic diagram illustrates the GMAC Ethernet1 interface, showing the connection between the PHY1 and GMAC1 blocks. The PHY1 block is connected to the GMAC1 block via various signal lines, including TX, RX, and control signals. The PHY1 block is also connected to power supplies (PHY1_VDDIO, PHY1_VDD33, PHY1_AVDD33) and ground. The GMAC1 block is connected to the PHY1 block via various signal lines, including TX, RX, and control signals. The GMAC1 block is also connected to power supplies (GMAC1_VDDIO, GMAC1_VDD33, GMAC1_AVDD33) and ground. The diagram includes a table for PHY Address and PHYAD[2:0], and a table for RGMII Power Source, CFG_EXT, and CFG_LDO[1:0].

PHY Address	PHYAD[2:0]
1	001

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(default)	0	10
Internal 1.5V	0	11

GMAC Ethernet1

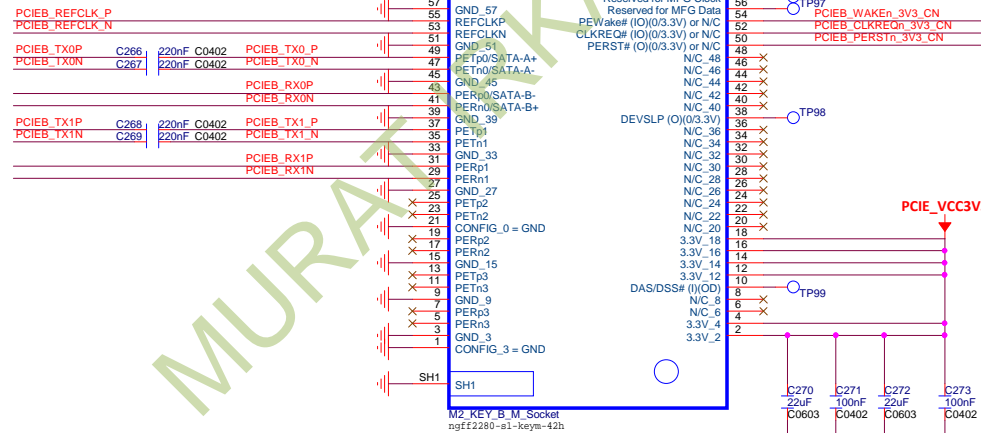
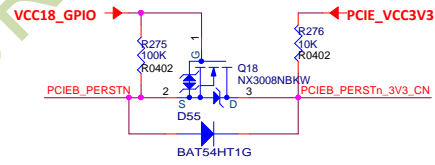
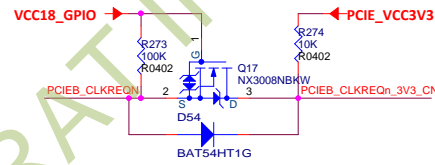
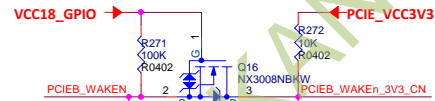
The schematic diagram illustrates the GMAC Ethernet1 interface, showing the connection between the PHY1 and GMAC1 blocks. The PHY1 block is connected to the GMAC1 block via various signal lines, including TX, RX, and control signals. The PHY1 block is also connected to power supplies (PHY1_VDDIO, PHY1_VDD33, PHY1_AVDD33) and ground. The GMAC1 block is connected to the PHY1 block via various signal lines, including TX, RX, and control signals. The GMAC1 block is also connected to power supplies (GMAC1_VDDIO, GMAC1_VDD33, GMAC1_AVDD33) and ground. The diagram includes a table for PHY Address and PHYAD[2:0], and a table for RGMII Power Source, CFG_EXT, and CFG_LDO[1:0].

PHY Address	PHYAD[2:0]
1	001

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(default)	0	10
Internal 1.5V	0	11

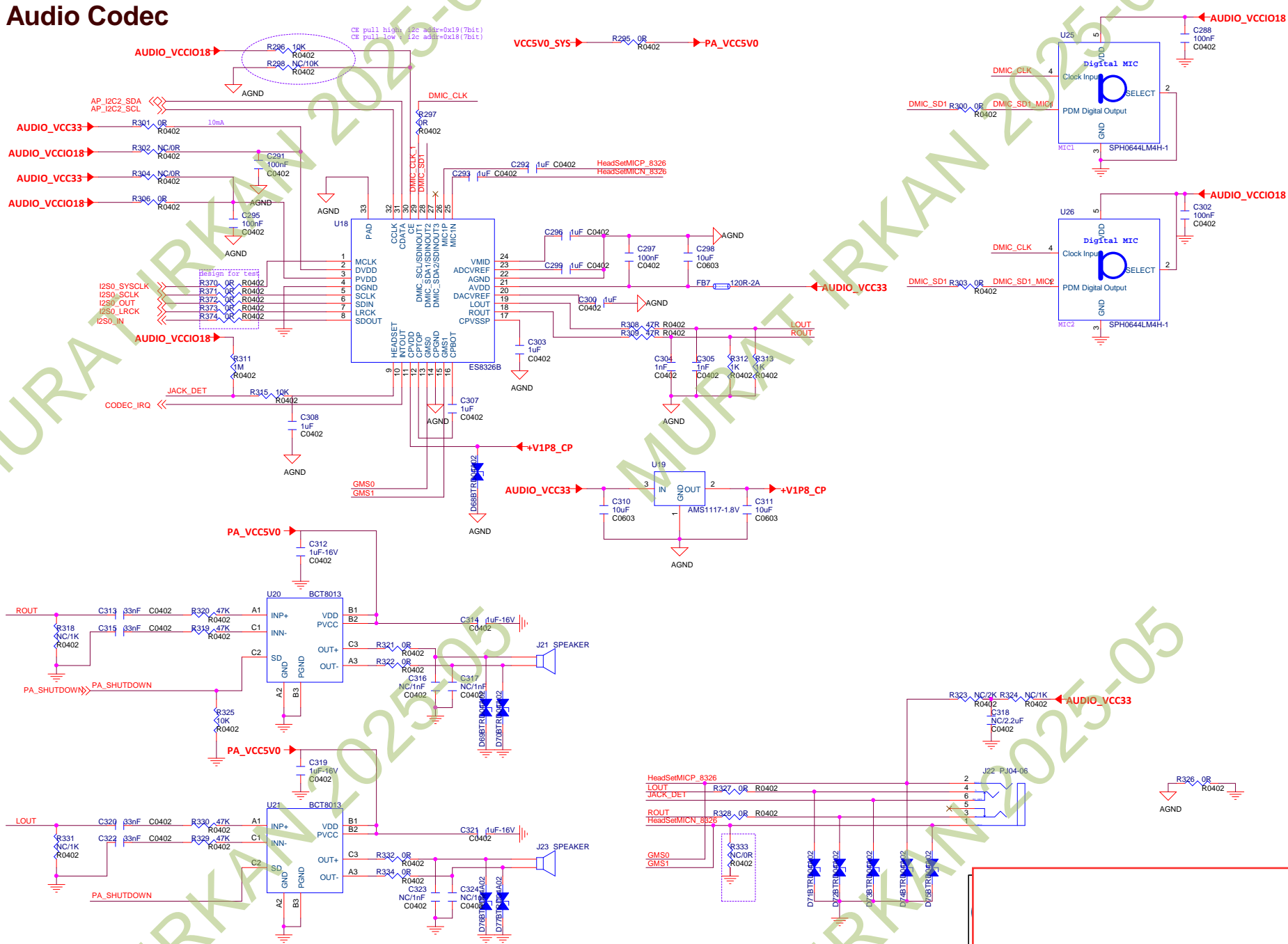
PCIEB

<<PCIEB_REFCLK_P
 <<PCIEB_REFCLK_N
 <<PCIEB_TX0P
 <<PCIEB_TX0N
 <<PCIEB_RX0P
 <<PCIEB_RX0N
 <<PCIEB_TX1P
 <<PCIEB_TX1N
 <<PCIEB_RX1P
 <<PCIEB_RX1N
 <<PCIEB_PERSTN
 <<PCIEB_WAKEN
 <<PCIEB_CLKREQN



[illegible]

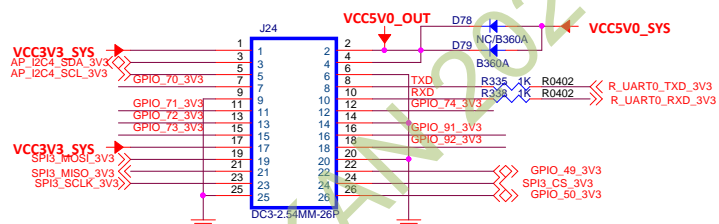
Audio Codec



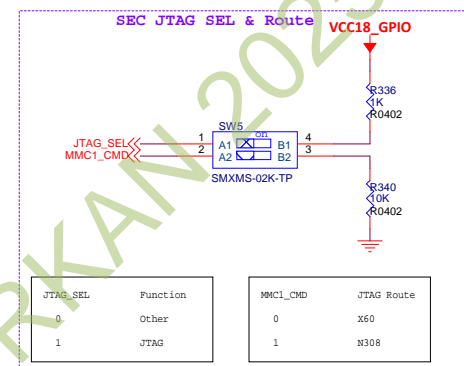
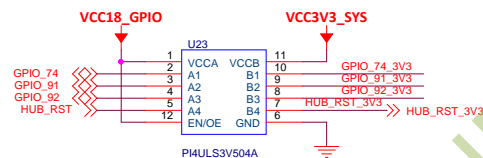
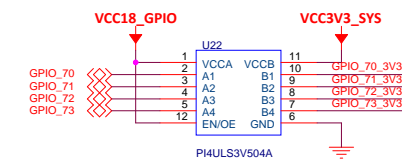
Rev	
<RevCode>	

26 pin GPIO

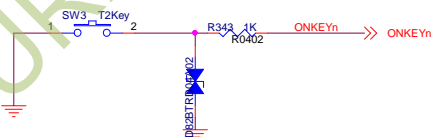
```
1.SPI_LCD:GPIO_70~74+GPIO_91+GPIO_92
2.PRI_JTAG:GPIO_70~73
3.N308 Debug:R UART0_TXD_3V3/R UART0_RXD_3V3
```



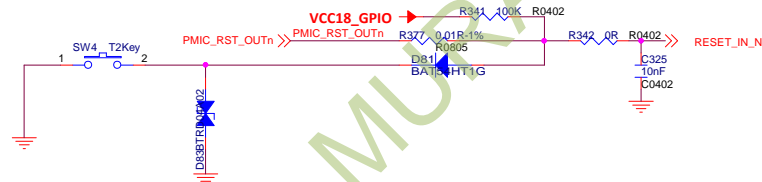
JTAG SEL



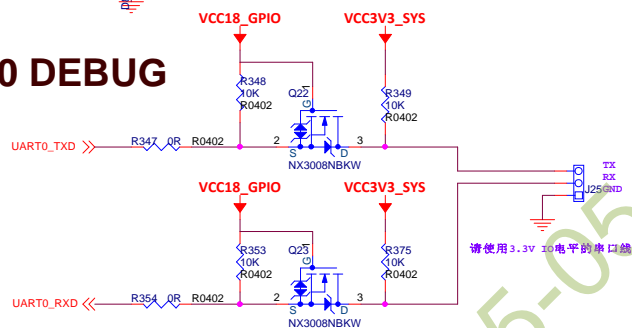
PowerON



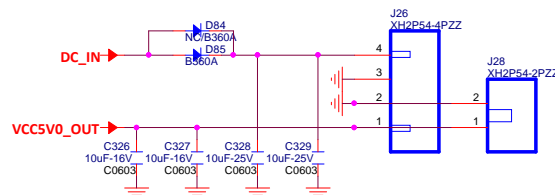
REST



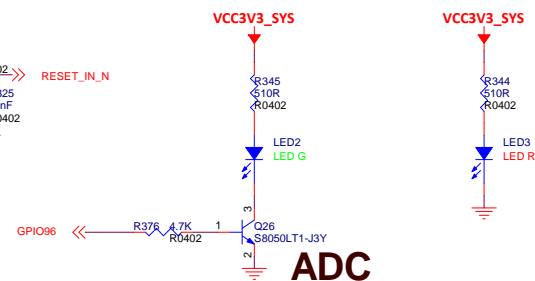
X60 DEBUG



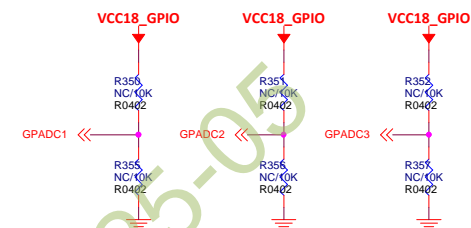
SATA HDD



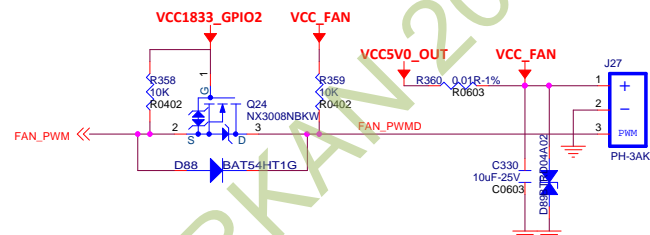
LED



ADC



FAN



Mark Port

