Reference Schematic For RK3399

RK3399_BOX_REF_V1.3

20180821

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	00.Cover Page		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
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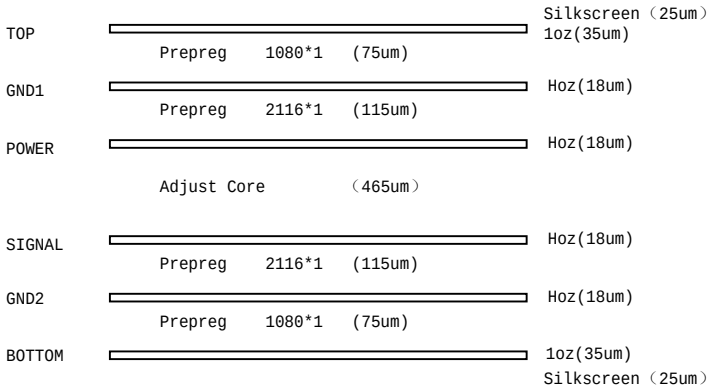
CONTENT INDEXING

6 LAYERS PCB STACK（e.g. PCB=1.0mm）



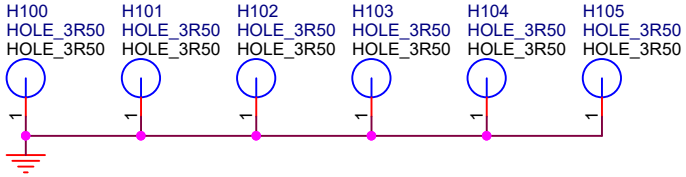
Note：

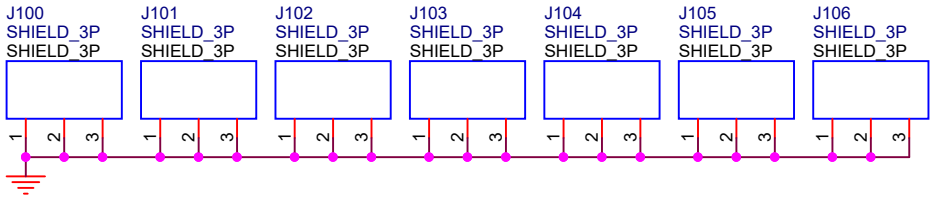
1：If the Value or option of the component properties is DNP，indicating do not mounted

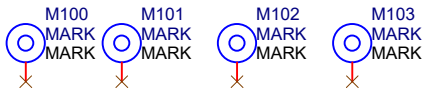
Note

Option

Description







Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	01.Index		
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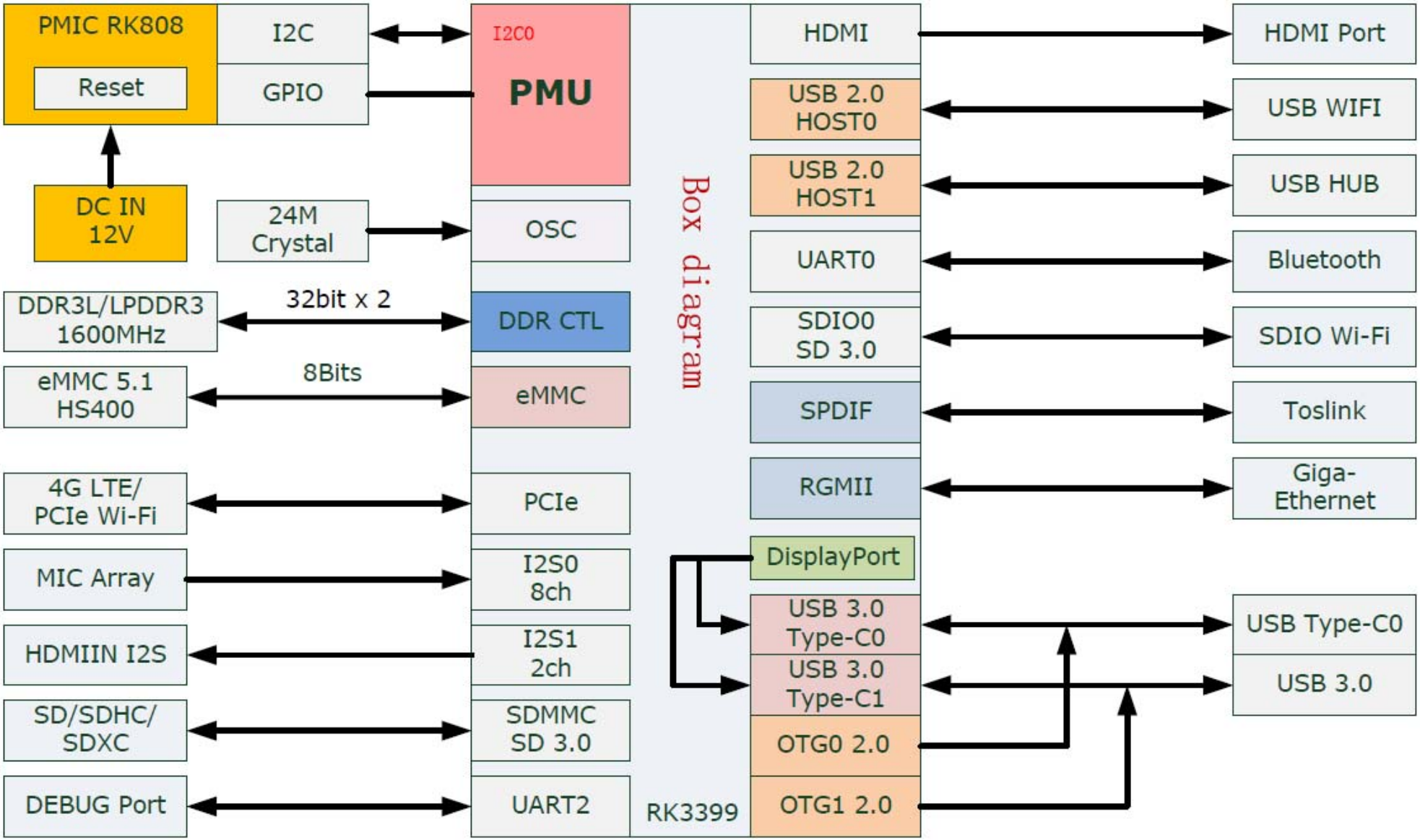
Revision History

Version	Date	Author	Change Note	Approved
V1.0	2017.01.12	Linus.Lin	First edition	
V1.1	2017.05.12	Linus.Lin	Please refer to the document of 《RK3399_BOX_REF_V11_20170512 Modify Notes》	
V1.2	2017.12.18	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_V12_20171218.xlsx》	
V1.3	2018.08.21	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_V13_20180821.xlsx》	

Block Diagram



Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808-D	0x1b	PMIC	100kHz,400KHz
					Silergy SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					Silergy SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8	Toshiba TC358749XBG		HDMI Transmit	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	RESERVE					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_TYPEC I2C_SCL_TYPEC	VCC_1V8	Fairchild FUSB302B ETEK ET302Y	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					

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Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCCIO_SD	RK808-D VLDO4

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RK808-D Power Diagram and Sequence

PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF
VCC3V3_SYS	EX_DCDC	Slot:1	3.3V	2.0A	ON	ON
VCC_1V8	DCDC4	Slot:1	1.8V	3.0A	ON	ON
VCCA_1V8	VLDO3	Slot:1	1.8V	100mA	ON	ON
VCC_1V5	VLDO6	Slot:1	1.5V	150mA	ON	ON
VDD_LOG	EX_DCDC	Slot:1A	0.9V	1.0A	ON	ON
VCCA_0V9	EX_LDO	Slot:1A	0.9V	300mA	ON	ON
VDD_CPU_B	EX_DCDC	Slot:1A	0.9V	6.0A	ON	OFF
VDD_GPU	EX_DCDC	Slot:1A	0.9V	6.0A	ON	OFF
VCC_DDR	DCDC3	Slot:2	FB=1.0V	2.5A	ON	ON
VCC3V0_SD	EX_LDO	Slot:2	3.0V	500mA	ON	ON
VDD_CPU_L	DCDC2	Slot:3	0.9V	5.0A	ON	OFF
VDD_CENTER	DCDC1	Slot:4	0.9V	5.0A	ON	OFF
VCC_3V0	VLDO8	Slot:5	3.0V	300mA	ON	ON
VCCIO_SD	VLDO4	Slot:7	3.0V	150mA	ON	ON
VCCA1V8_HDMI	VLDO2		1.8V	150mA	OFF	ON
VCCA0V9_HDMI	VLDO7		0.9V	300mA	OFF	ON
Reserve	VSWOUT1	Slot:6		5.0A	ON	OFF
Reserve	VSWOUT2			5.0A	OFF	OFF
Reserve	VLDO1			150mA	OFF	OFF
Reserve	VLDO5			300mA	OFF	OFF
RESET		Slot:7	OD		ON	

DC Adapter 12V

VCC12V_DCIN

1110mA/23mA/TBD

SY8113B BUCK,PWM 3A,<5uA shutdown — EN always ON

SY8113B BUCK,PWM 3A,<5uA shutdown — EN always ON

VCC5V0_USB 5.1V

2440mA/48mA/TBD

VCC5V0_SYS 5.0V

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VBUS5V0_TYPEC (VCC5V0_TYPEC0_EN) → VBUS USB 3.0 Type-C0 port

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST0 (VCC5V0_HOST_EN) → VBUS USB 2.0 A port

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST1 (VCC5V0_HOST_EN) → VBUS USB 2.0 A port

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST2 (VCC5V0_HOST_EN) → VBUS USB 3.0 A port

FUSB302 Type-C VCONN CC 300mA/1uA

VCC_RTC — VCC of PMIC RTC — S0/S3/S5 7.6mA/TBD/30uA

VCC_BAT 3.3V

WPM2015 P-MOSFET 1.8A,110mR@4.5V — VCC5V0_FAN (FAN_CTL_H) → VCC of Speaker AMP — S0/OFF/OFF

B5819WS — VCC5V0_HDMI → VCC of HDMI Device

SY8089AAAC BUCK,PWM 2A,<1uA shutdown (PMIC_EXT_EN)

VCC3V3_SYS

PT5108E23E-30 LDO 3.0V/500mA <1uA shutdown — VCC3V0_SD (SDMMC0_PWR_H) → SD/TF Card — S0/OFF/OFF TBD/TBD/TBD

TT2102 ADJ LDO 0.9V/300mA <1uA shutdown — VCCA_0V9 (VCC3V3_SYS)

VCC0V9_PLL			
VCC0V9_PMUPLL	AVDD of PLL	S0/S3/OFF	13.4mA/108uA/TBD
VCC0V9_DDRPLL	VDD of PMU PLL	S0/S3/OFF	12.3mA/160uA/TBD
VCC0V9_EMMC	AVDD of DDR CTRL	S0/S3/OFF	13.4mA/18uA/TBD
VCC0V9_USB	VDD of EMMC CTRL CORE DLL	S0/S3/OFF	3.4mA/<3mA/TBD
VCC0V9_PCIE	AVDD of USB phy	S0/S3/OFF	20.6mA/2.54mA/TBD
	AVDD of PCIE phy	S0/S3/OFF	6.3mA/TBD/TBD

PT5108E23E-18 LDO 1.8V/500mA <1uA shutdown — VCC_EFUSE (EFUSE_VQPS_EN_H) → VCC of EFUSE — User/OFF/OFF 1.7mA/TBD/TBD

VCC3V3_CC			
VCC3V3_USB	VCC of FUSB302	S0/S3/OFF	8.6mA/<0.3mA/TBD
VCC3V3_EMMC	AVDD of USB phy	S0/S3/OFF	17.7mA/0.25mA/TBD
VCC3V3_WL	CORE VCC of EMMC FLASH	S0/S3/OFF	200mA/0.24mA/TBD
VCC3V3_WLIN	VCC of WIFI module	S0/OFF/OFF	
VCC3V3_LAN	VBAT of WIFI+BT module	S0/S3/OFF	864mA/12.1mA/TBD
VCC3V3_MIC	AVCC/DVCC of ethernet phy	S0/S3/OFF	103.5mA/26.3mA/TBD
VCC3V3_SPDIF	VDD of MIC Array	S0/S3/OFF	
VCC3V3_PCIE	VCC of SPDIF Driver IC	S0/S3/OFF	TBD/TBD/TBD
VCC3V3_IR	VCC of PCIE Device	S0/OFF/OFF	
VCC3V3_HDMIIN	VCC of IR Receiver	S0/S3/OFF	5.3mA/1.1mA/TBD
VCC3V3_LED	VCC of PCIE Device	S0/OFF/OFF	
VCC3V3_HUB	Work LED	S0/S3/OFF	1.2mA/1.2mA/TBD
	AVDD of USB HUB	S0/S3/OFF	TBD/0.56mA/TBD

PMIC RK808 BUCK1 5A,0.7-1.5V TBD uA shutdown — VDD_CENTER → VDD of SOC center — S0/OFF/OFF 1050mA/TBD/TBD

PMIC RK808 BUCK2 5A,0.7-1.5V TBD uA shutdown — VDD_CPU_L → VDD of Quard-A53 — S0/OFF/OFF 1480mA/TBD/TBD

PMIC RK808 BUCK3 2.5A,1.0-1.8V TBD uA shutdown — VCC_DDR

VDD of DDR CTRL	S0/S3/OFF	
VDDCA/VDD2 of DDR	S0/S3/OFF	1240mA/3.5mA/TBD
VDDQ of DDR	S0/S3/OFF	

PMIC RK808 BUCK4 3A,1.8-3.3V TBD uA shutdown — VCC_1V8

VCC1V8_EMMC			
VCC1V8_WIFI	VDD of EMMC CRTL,VDDQ of EMMC FLASH IO	S0/S3/OFF	234mA/<4mA/TBD
VCC1V8_IO	VDDIO of WIFI+BT module	S0/S3/OFF	10.6mA/4.25mA/TBD
VCC1V8_DDR	VDDIO/VDDPST of GPIO	S0/S3/OFF	20mA/0.3mA/TBD
	VDD1 of LPDDR3	S0/S3/OFF	49.7mA/940uA/TBD uA

PMIC RK808 LDO1 150mA,1.8-3.4V TBD uA shutdown

PMIC RK808 LDO2 150mA,1.8-3.4V TBD uA shutdown — VCCA1V8_HDMI → AVDD of HDMI/MIPI TX phy — S0/OFF/OFF 11.7mA/TBD/TBD

PMIC RK808 LDO3 100mA,0.8-2.5V TBD uA shutdown — VCCA_1V8

VCC1V8_PMUIO1			
VCC1V8_PMUPLL	VDDIO/VDDPST of PMUIO1	S0/S3/OFF	5mA/133uA/TBD
VCC1V8_PLL	VDD of PMU PLL	S0/S3/OFF	9.6mA/1.01mA/TBD
VCC1V8_USB	AVDD of PLL	S0/S3/OFF	18mA/0.3uA/TBD
VCC1V8_ADC	AVDD of USB phy	S0/S3/OFF	10.1mA/1.79mA/TBD
VCC1V8_PCIE	AVDD of SARADC	S0/S3/OFF	3.3mA/<1mA/TBD
	AVDD of PCIE phy	S0/S3/OFF	5mA/<1mA/TBD

PMIC RK808 LDO4 150mA,1.8-3.4V TBD uA shutdown — VCCIO_SD → VDDIO of SDMMC0 — S0/OFF/OFF 3.4mA/TBD/TBD

PMIC RK808 LDO5 300mA,1.8-3.4V TBD uA shutdown

PMIC RK808 LDO6 150mA,0.8-2.5V TBD uA shutdown — VCC_1V5 → VDDPST of APIO2/APIO4 — S0/OFF/OFF 17.4mA/TBD/TBD

PMIC RK808 LDO7 300mA,0.8-2.5V TBD uA shutdown — VCCA0V9_HDMI → AVDD of HDMI/MIPI TX phy — S0/OFF/OFF 20.5mA/TBD/TBD

PMIC RK808 LDO8 300mA,1.8-3.4V TBD uA shutdown — VCC_3V0 → VDD of APIO2/APIO4/PMUIO2 — S0/OFF/OFF 13.5mA/TBD/TBD

PMIC RK808 VSW1 5A,200mohm TBD uA shutdown

PMIC RK808 VSW2 5A,200mohm TBD uA shutdown

SYR837PKC Switch 6A,1uA shutdown (VCC_1V8) — VDD_CPU_B → VDD of Dual-A72 — S0/OFF/OFF 4140mA/TBD/TBD

SYR838PKC Switch 6A,1uA shutdown (VCC_1V8) — VDD_GPU → VDD of Mali-T864 — S0/OFF/OFF 3880mA/TBD/TBD

SY8088AAC BUCK,PWM 1A,<1uA shutdown (VCC_1V8) — VDD_LOG → VDD of SOC Logic — S0/S3/OFF 390mA/7.5mA/TBD

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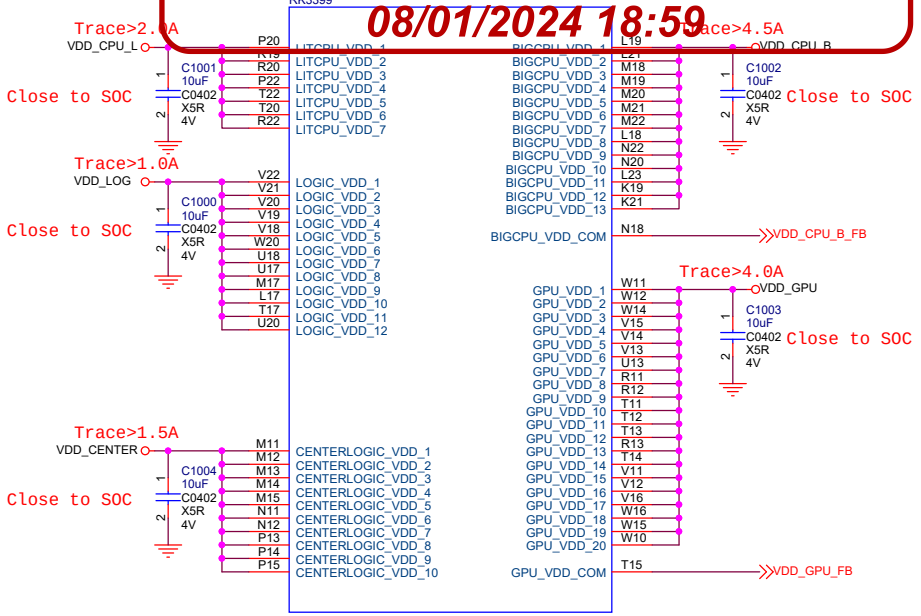
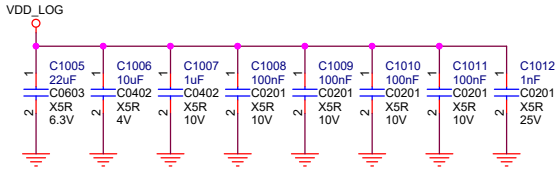
RK3399_W

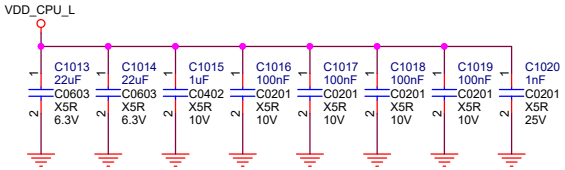
MURAT IRKAN YAPAY ZEKA PC

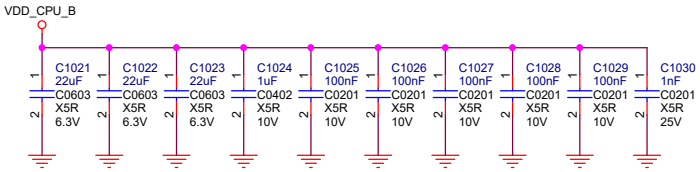
08/01/2024 18:59

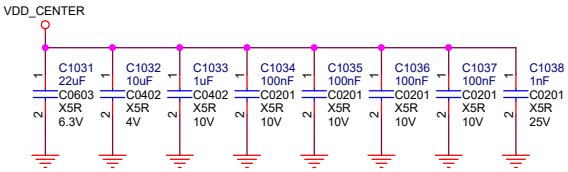


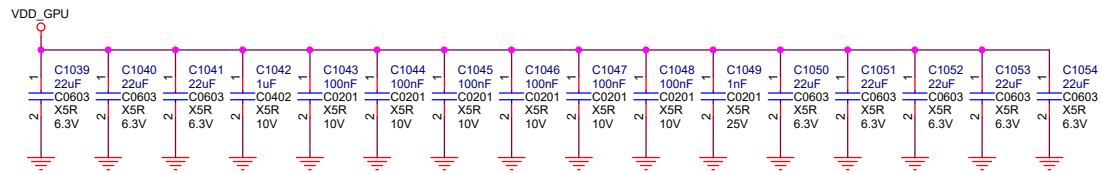
Note:All the Power filter capacitors should be placed close to the power pins of RK3399











RK3399_X

YAPAY ZEKA PC RK3399 ARM A72+A53 CPU

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	10.RK3399 Power		
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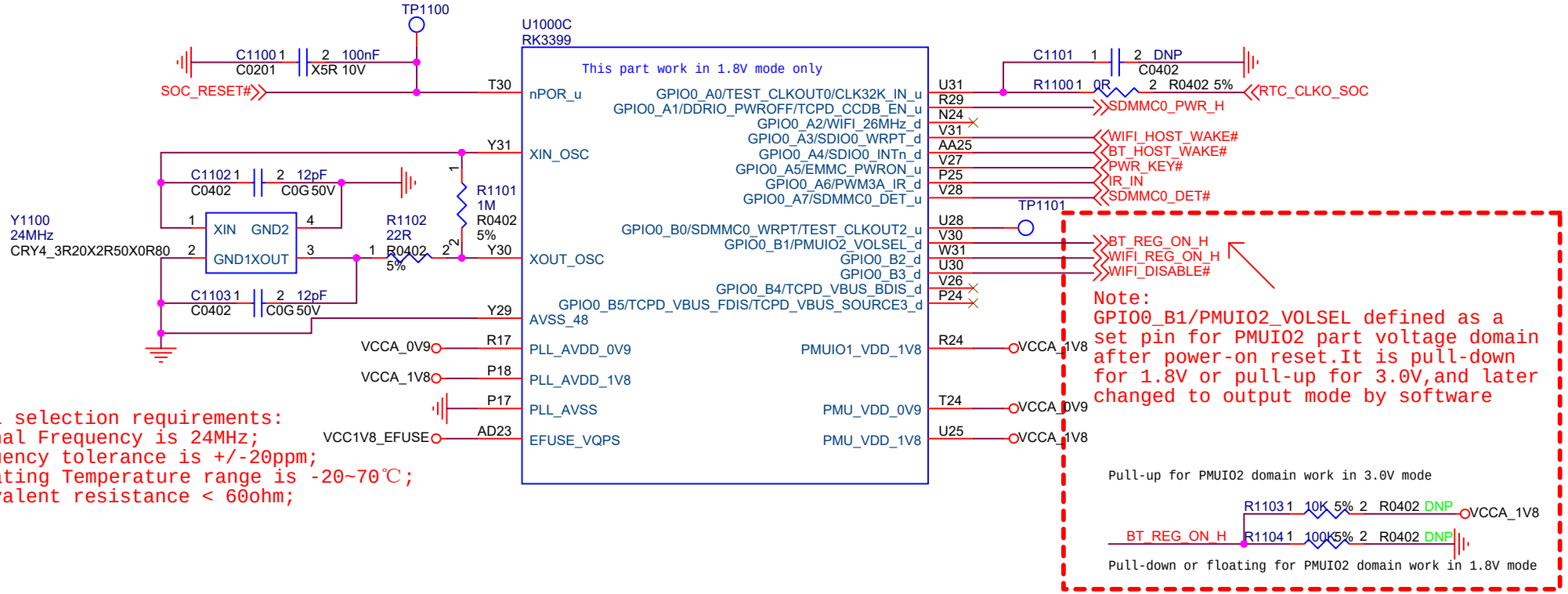
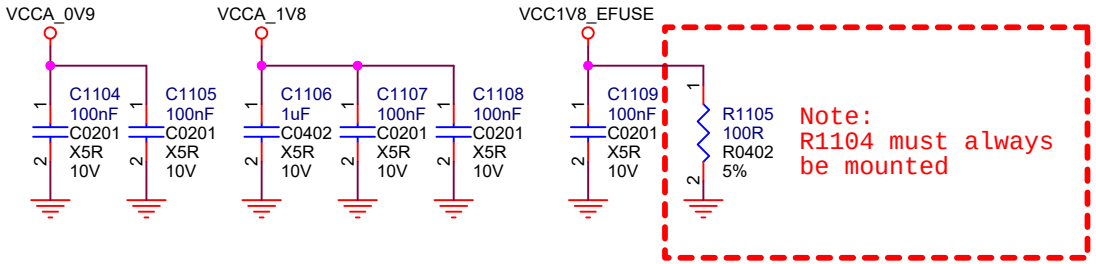
RK3399_C



Cristal selection requirements:
1.Nominal Frequency is 24MHz;
2.Frequency tolerance is +/-20ppm;
3.Operating Temperature range is -20~70℃;
4.Equivalent resistance < 60ohm;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
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File:	11.RK3399 PMU Controller		
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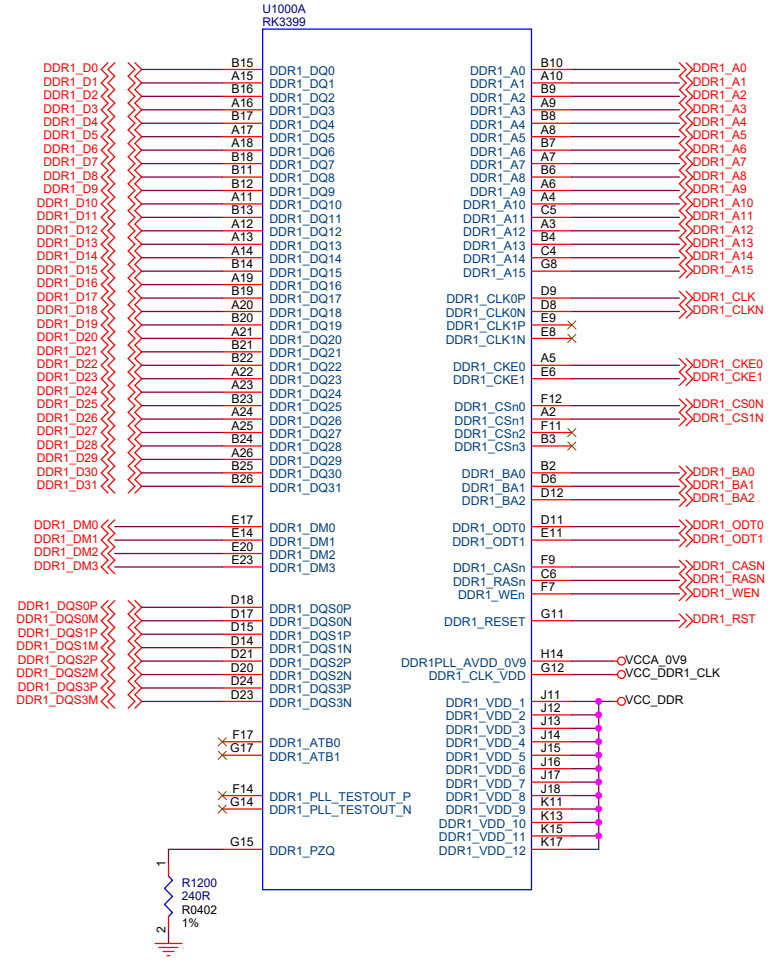
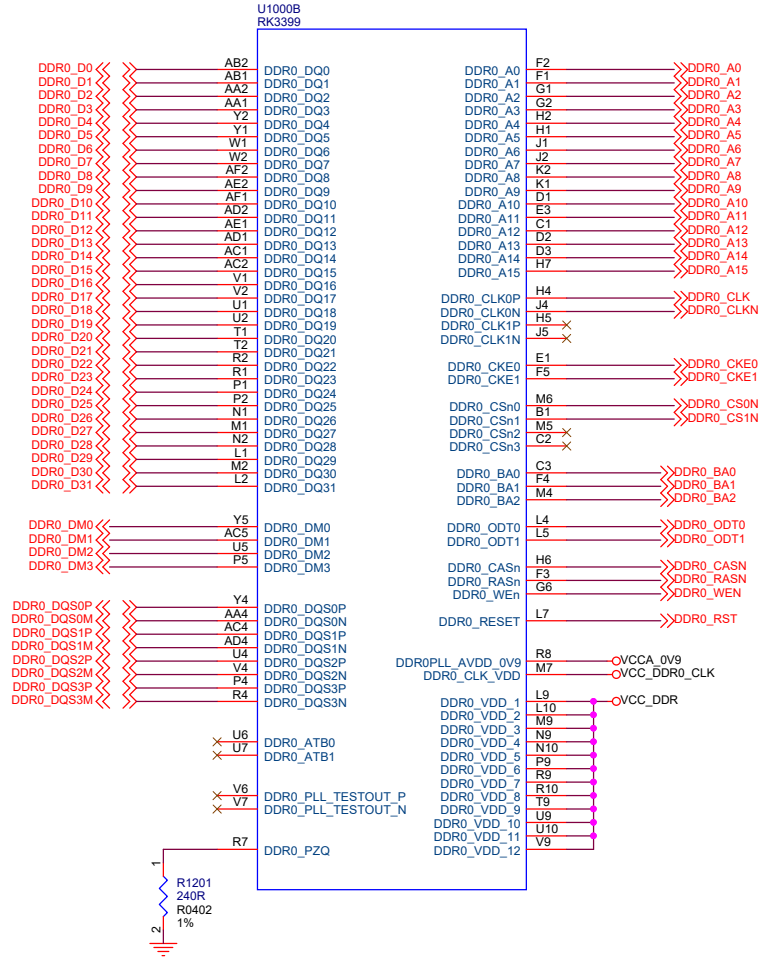
RK3399_A

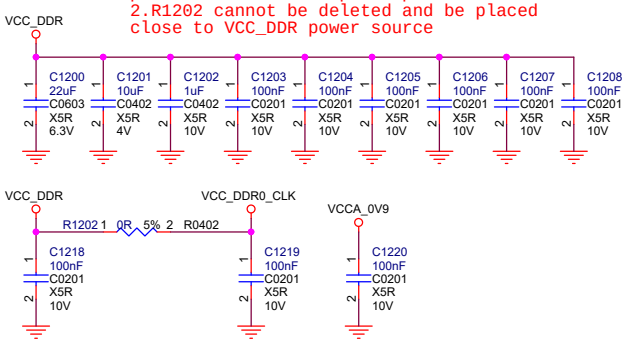


RK3399_B



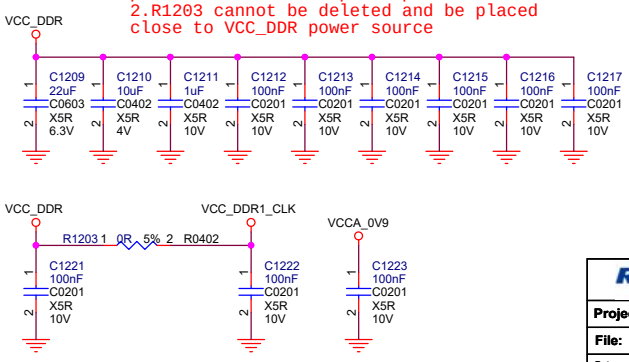
DDR FILTER

Note:
1.All the Power filter capacitors should be placed close to the power pins of RK3399
2.R1202 cannot be deleted and be placed close to VCC_DDR power source



DDR FILTER

Note:
1.All the Power filter capacitors should be placed close to the power pins of RK3399
2.R1203 cannot be deleted and be placed close to VCC_DDR power source



Fuzhou Rockchip Electronics			
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File:	12.RK3399 DDR Controller		
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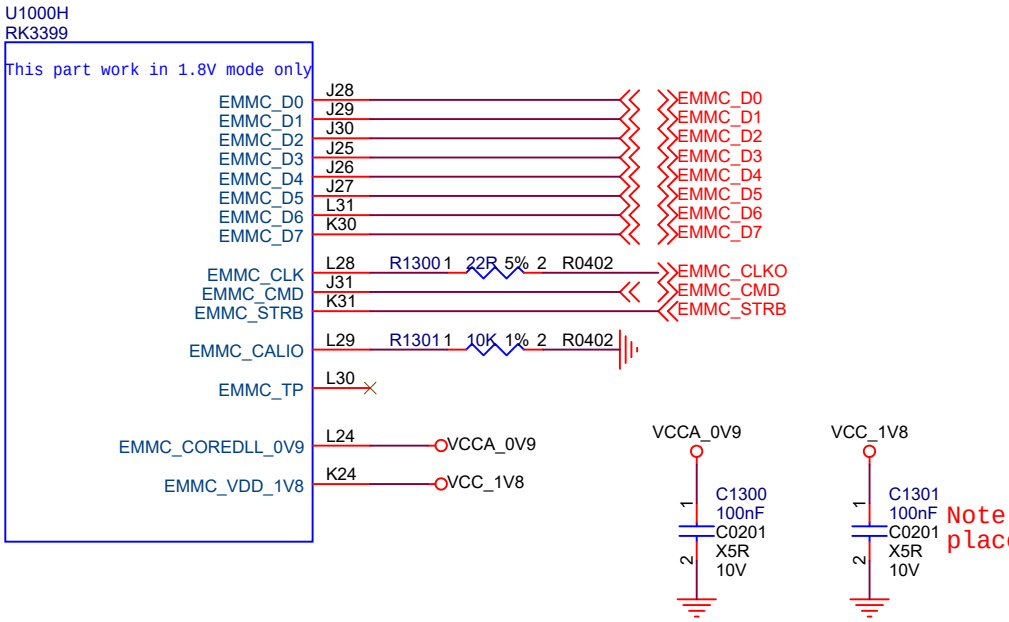
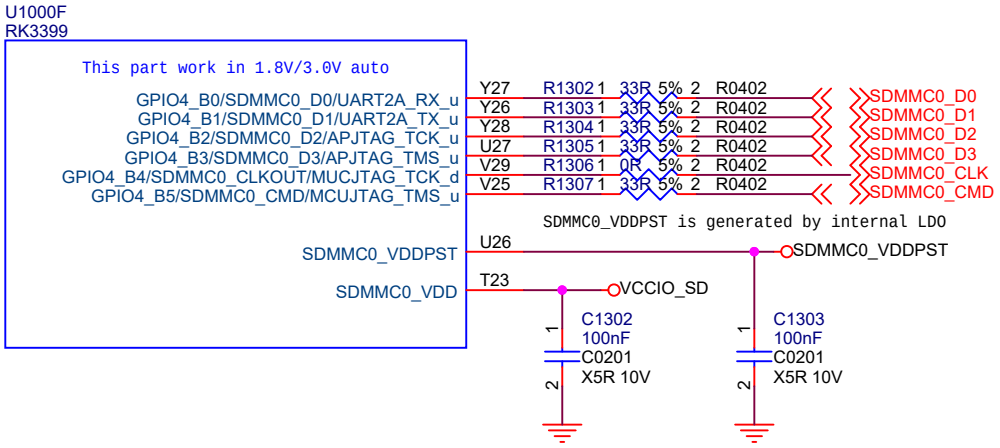
RK3399_H



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

EMMC design rules:
1.Data[0:3],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
6.R1300 should be place close to RK3399;

RK3399_F

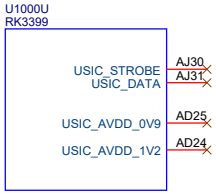


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

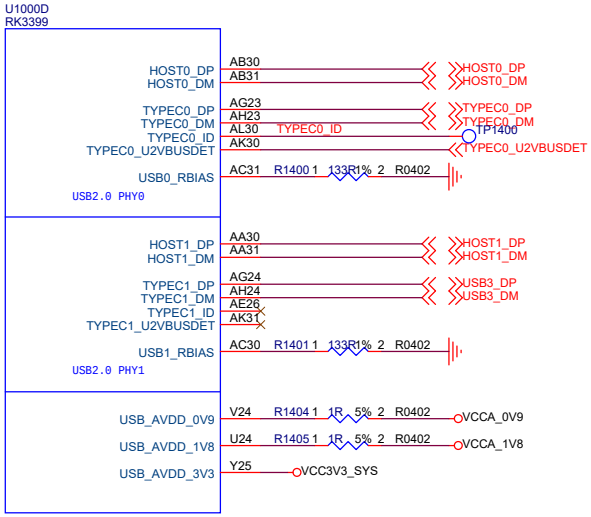
SDMMC design rules:
1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

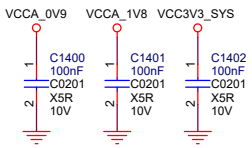
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	13.RK3399 FLASH/SDMMC Controlle		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	11 of 45

RK3399_U



RK3399_D

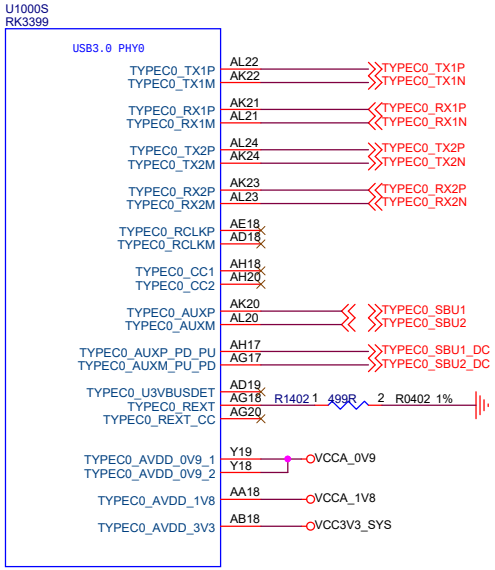


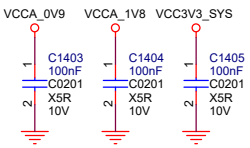


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

RK3399_S

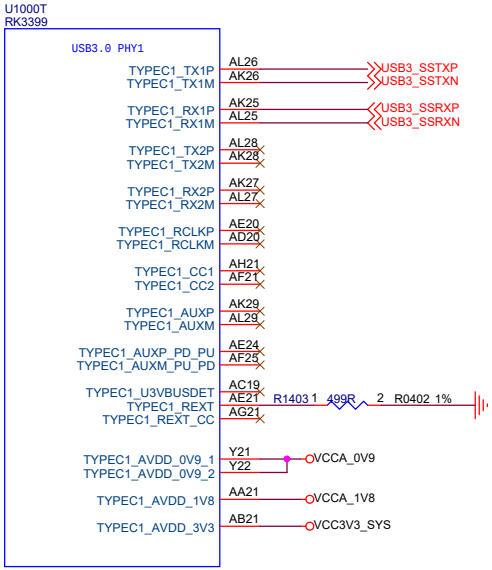




Note:All the Power filter capacitors should be placed close to the power pins of RK3399

USB3.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between TX and RX < 1.6ns;
3.Max trace length < 6inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals follows the 3W rule;

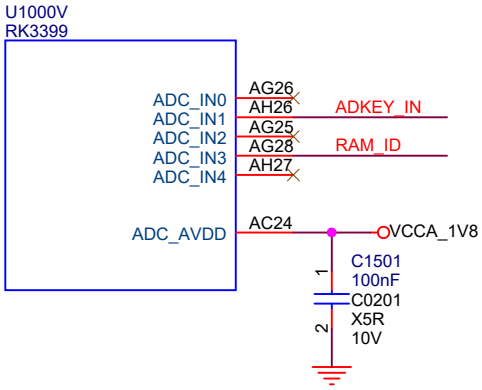
RK3399_T

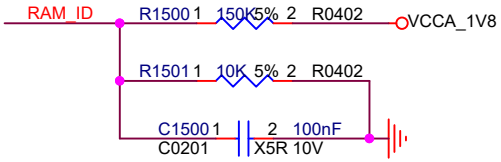


DP design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	14.RK3399 USB/USIC Controller		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	12 of 45

RK3399_V

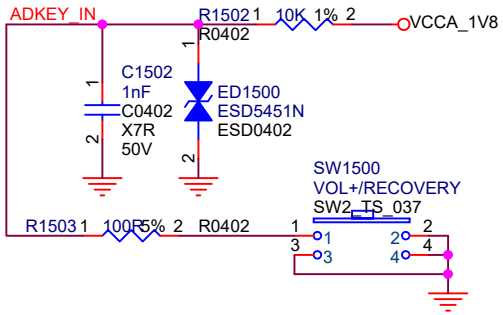




Note:All the Power filter capacitors should be placed close to the power pins of RK3399

	RAM ID	R1500 PU	R1501 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K

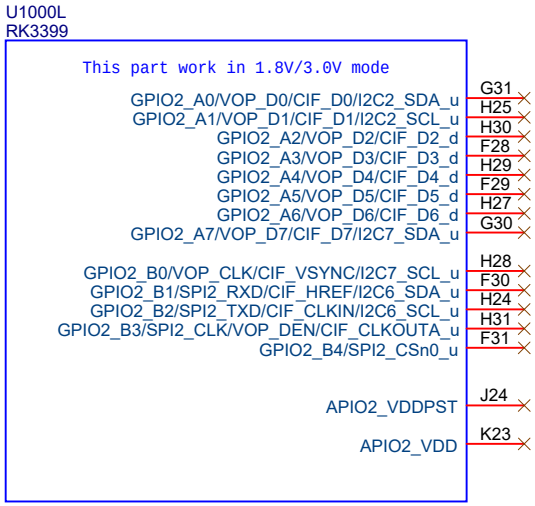
KEY



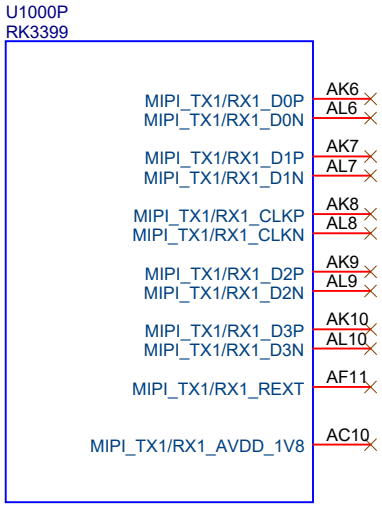
Note:
1.If ADKEY_IN=0V at power-on reset,
then system will enter into Recovery mode.
2.R1503,SW1500,ED1500 can be deleted if no need at Mass Production

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	15.RK3399 SAR-ADC/Key		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	13 of 45

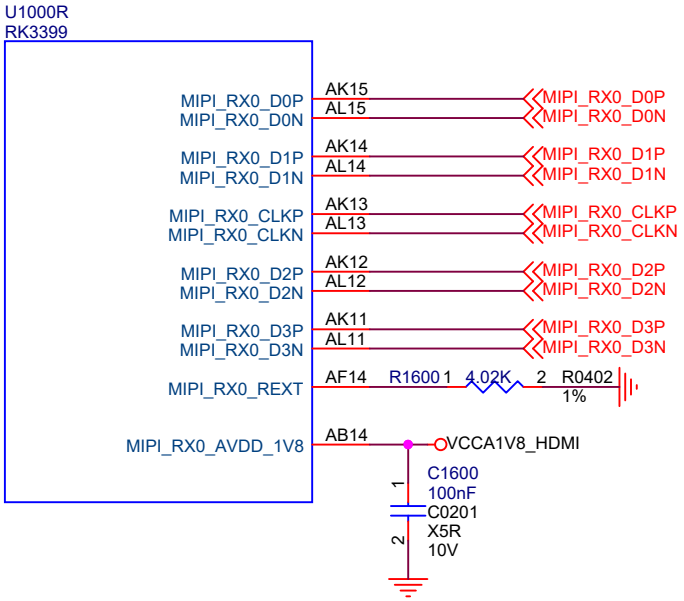
RK3399_L



RK3399_P



RK3399_R



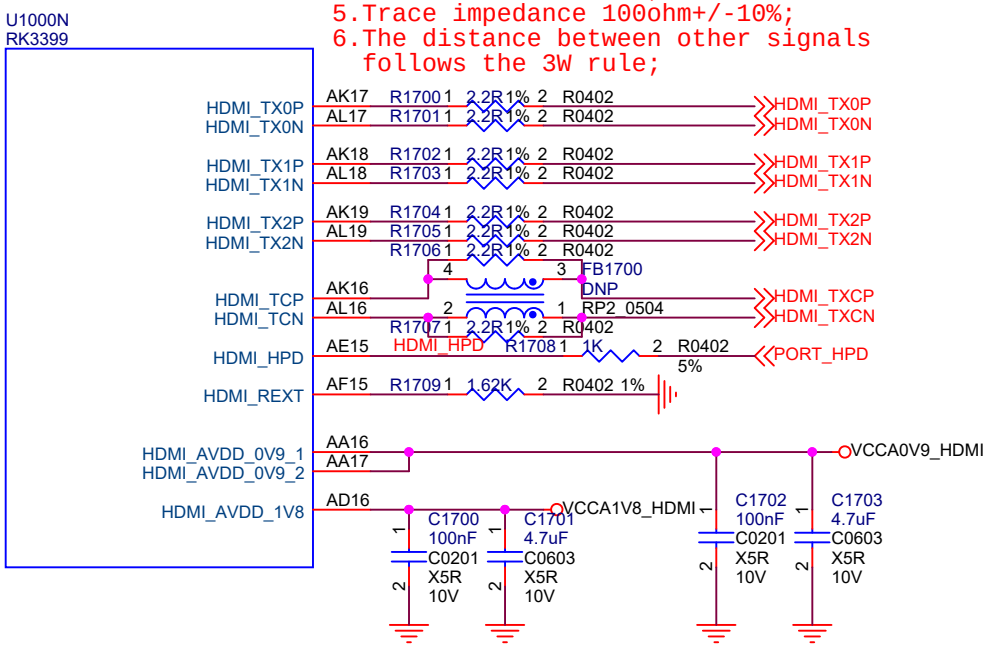
MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	16.RK3399 DVP Interface		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	14 of 45

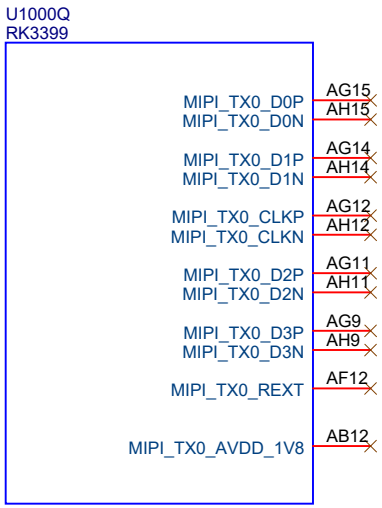
RK3399_N

HDMI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 80ps;
3.Max trace length < 9.8inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

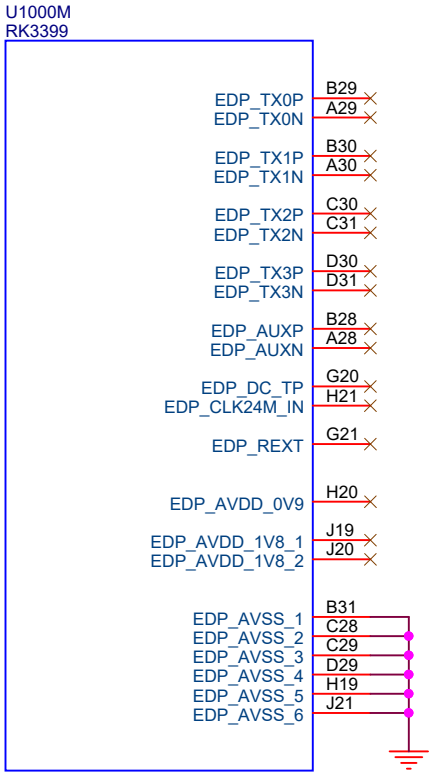


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_Q



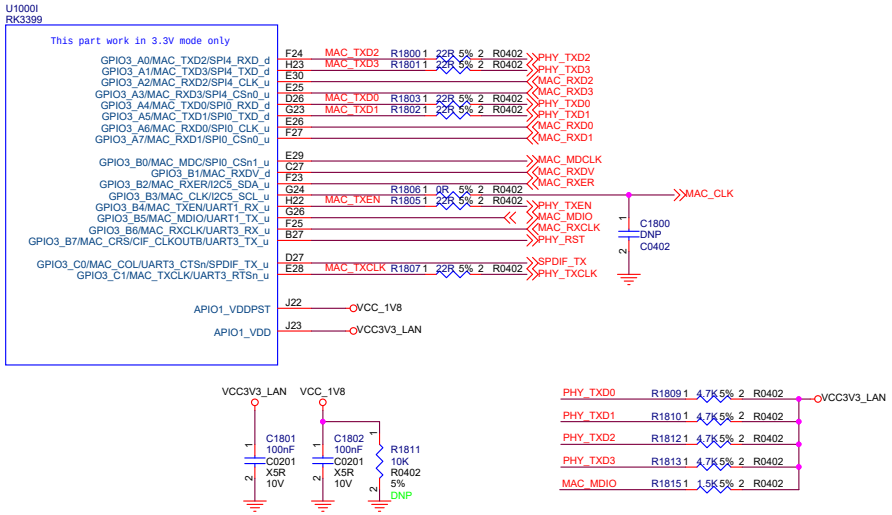
RK3399_M



eDP design rules:
1.Max intra-pair skew <4 ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

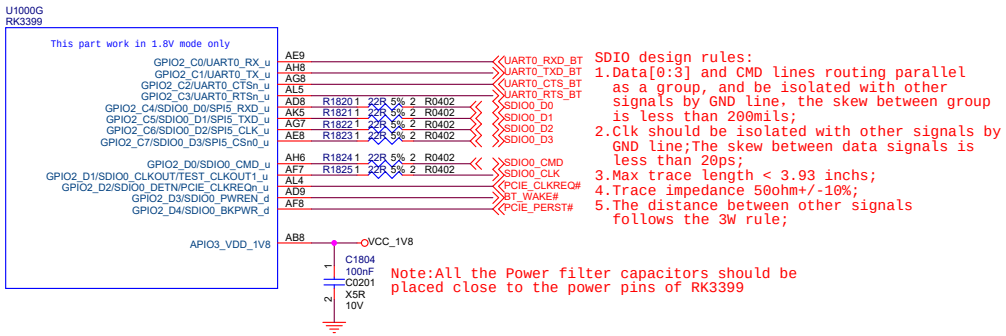
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	17.RK3399 Display Interface		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	15 of 45

RK3399_I



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

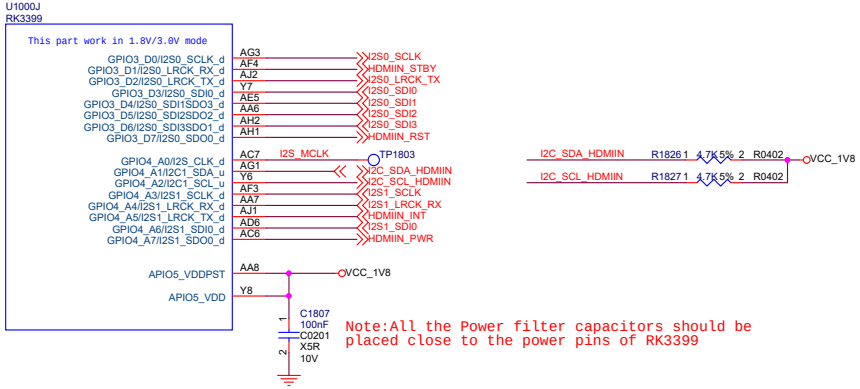
RK3399_G



SDIO design rules:
1.Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signals by GND line. the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

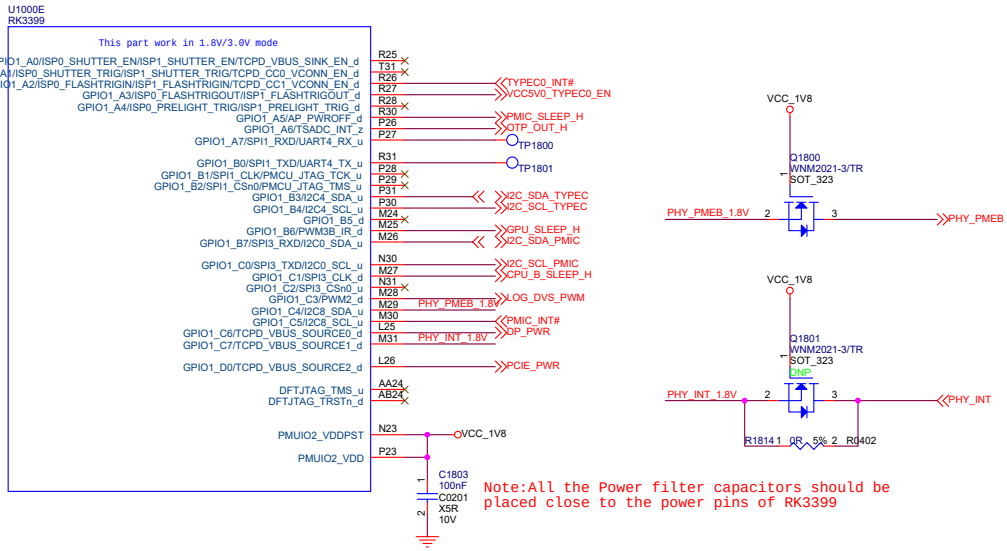
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_J

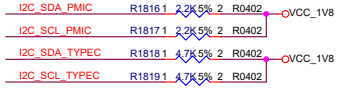


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_E



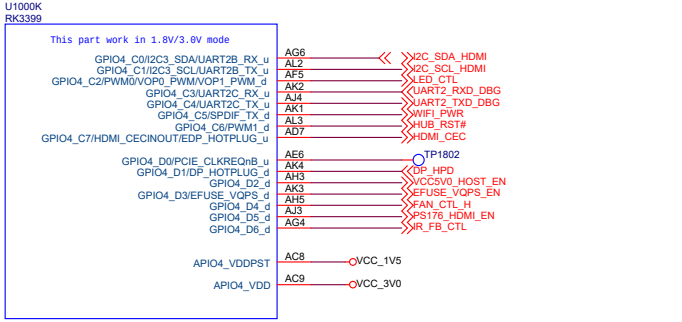
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

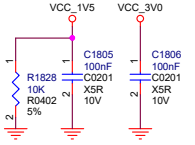


1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
1.8V/3.0V mode	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V

Note:All the part which support 1.8V and 3.0V mode, software config should match with hardware design.

RK3399_K

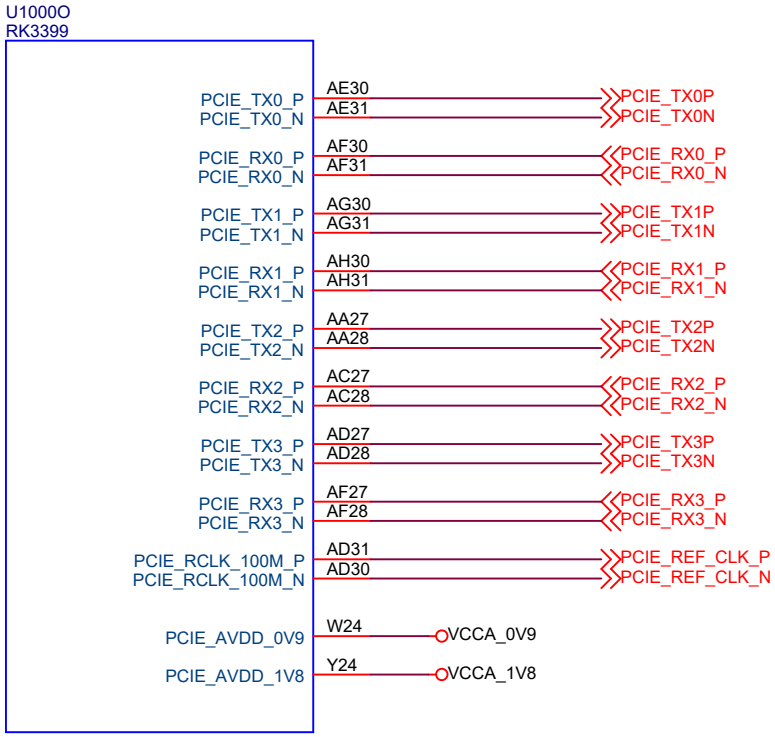




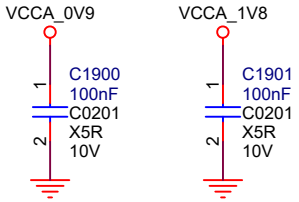
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	18.RK3399 GPIO		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	16 of 45

RK3399_0



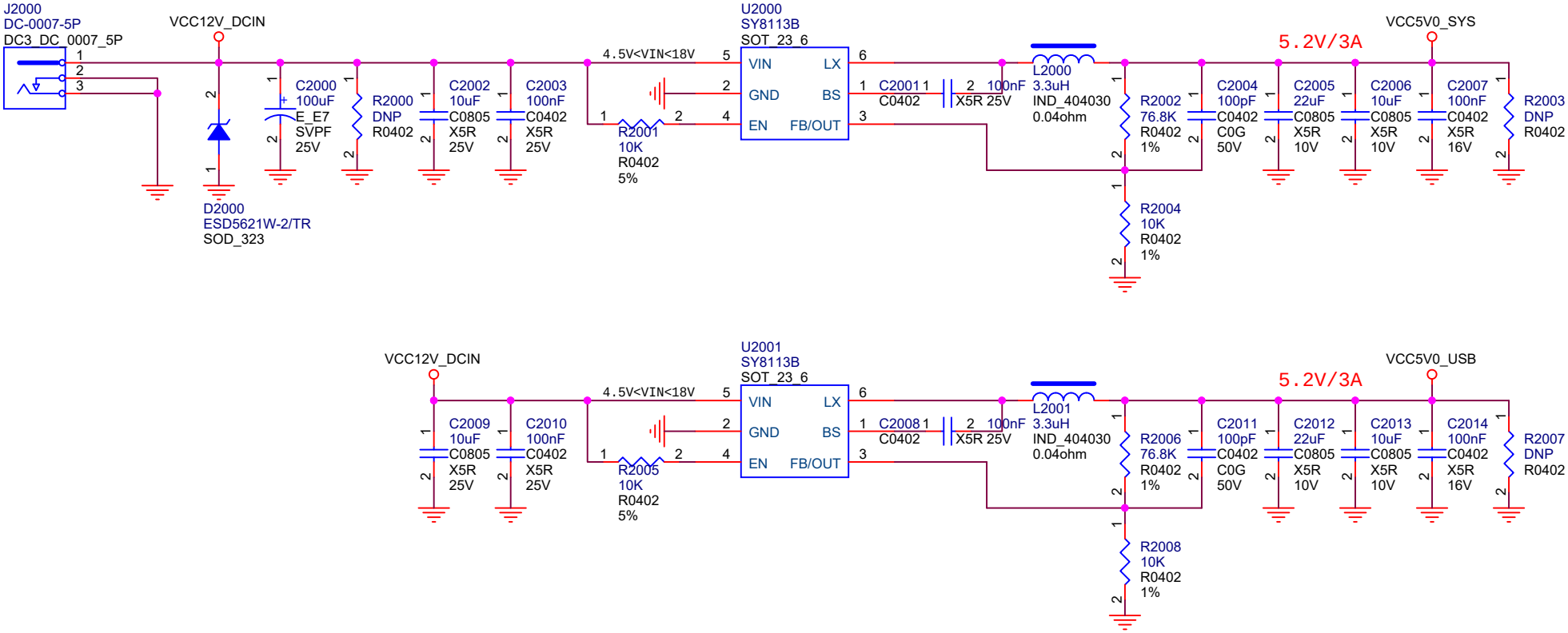
PCIE design rules:
1.Max intra-pair skew < 4ps;
2.Max inter-pair skew < 1.6ns;
3.Max trace length < 14inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

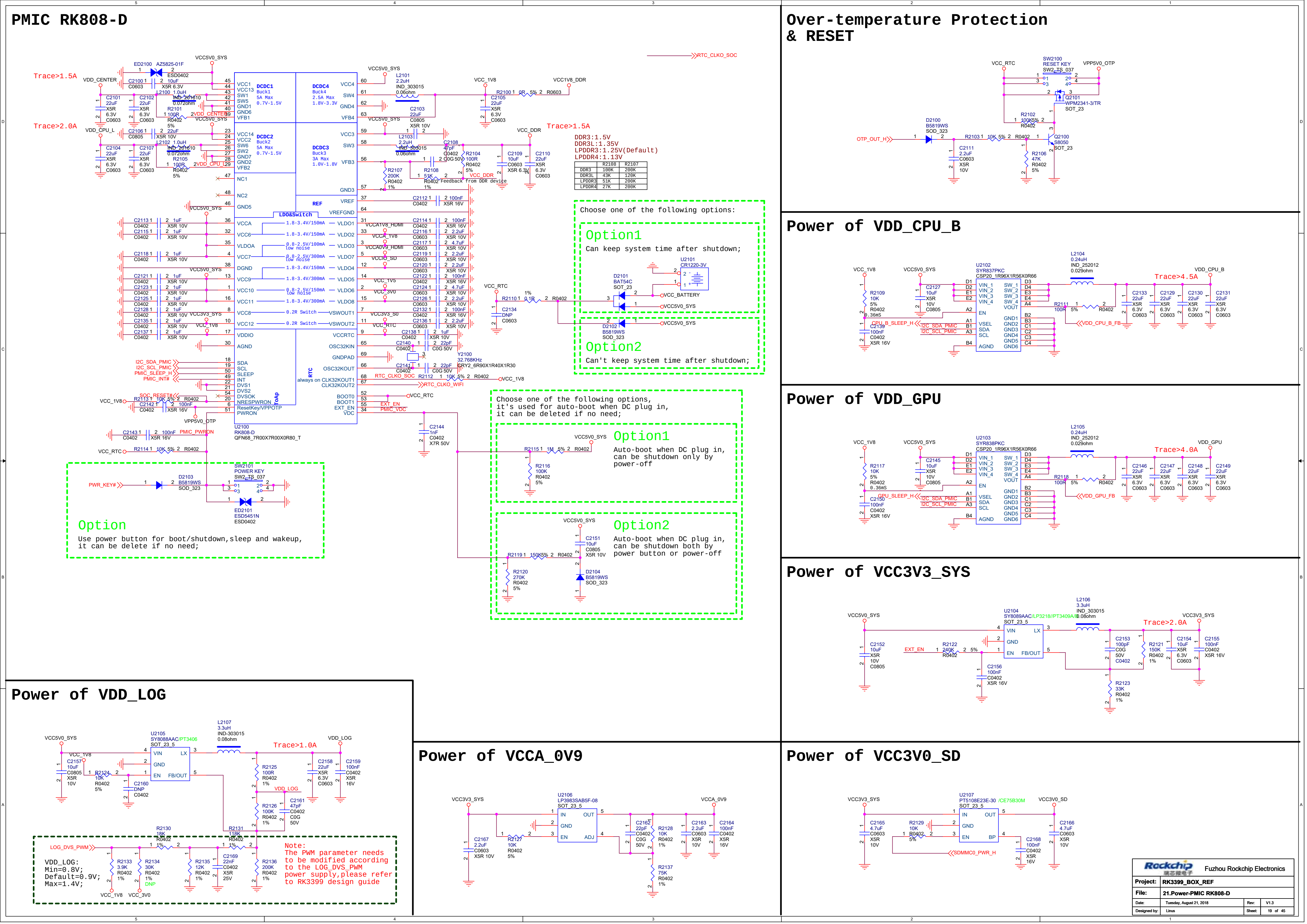
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	19.RK3399 PCIE		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	17 of 45

DC IN & SYSTEM Power



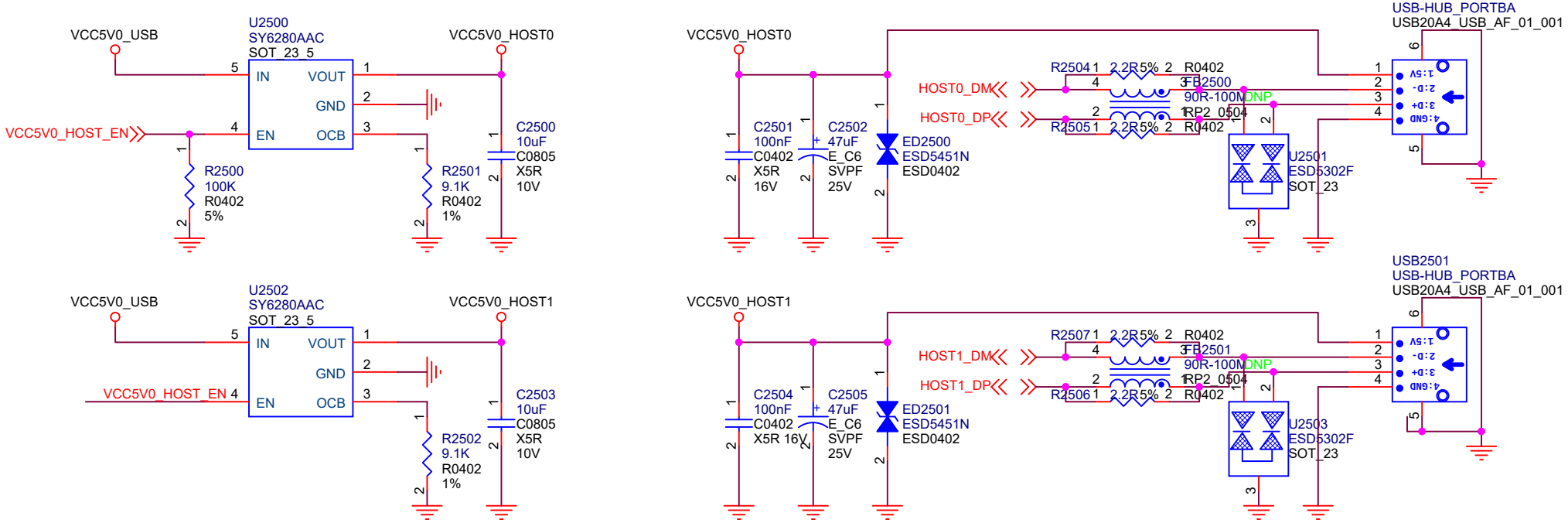
Note:If use USB3.0 HUB, U2001 must support over 3A current

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	20.Power-DC IN		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	18 of 45

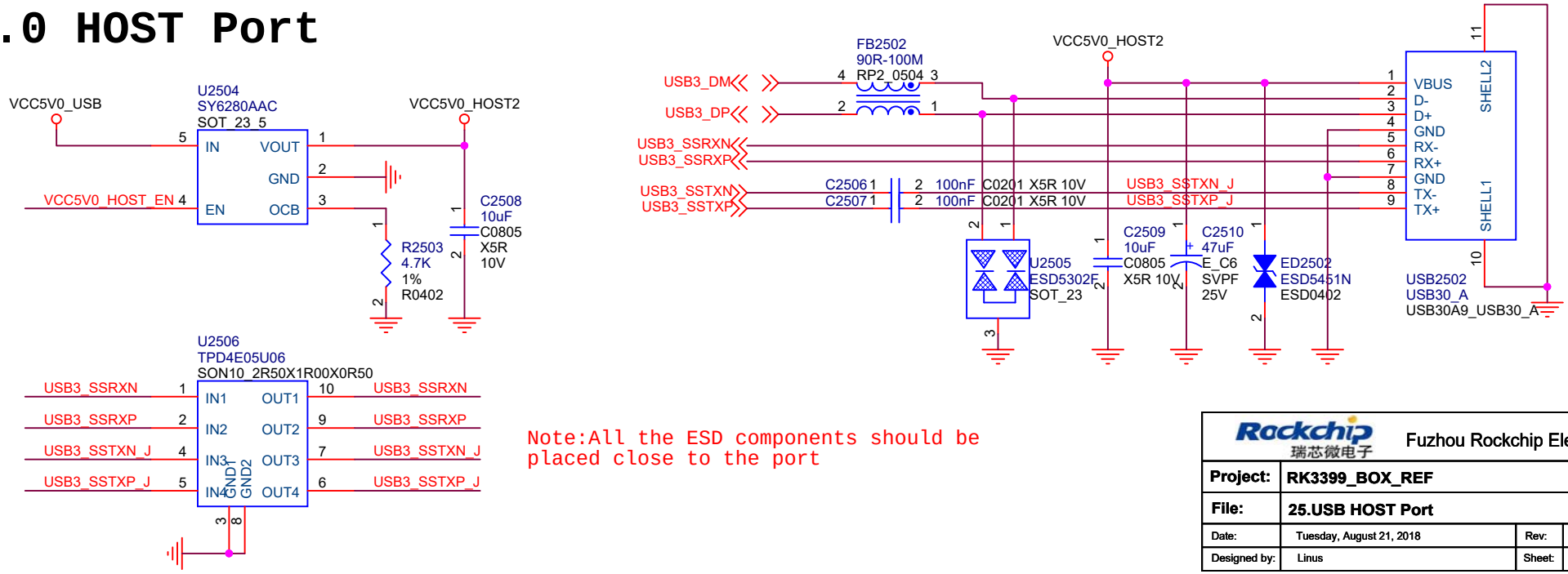


PMIC RK808-D
Trace>1.5A
Trace>2.0A
Trace>1.5A
DDR3:1.5V
DDR3L:1.35V
LPDDR3:1.25V(Default)
LPDDR4:1.13V
R2108 R2107
DDR3 100K 200K
DDR3L 43K 120K
LPDDR3 51K 200K
LPDDR4 27K 200K
Choose one of the following options:
Option1
Can keep system time after shutdown;
Option2
Can't keep system time after shutdown;
Choose one of the following options, it's used for auto-boot when DC plug in, it can be deleted if no need;
Option1
Auto-boot when DC plug in, can be shutdown only by power-off
Option2
Auto-boot when DC plug in, can be shutdown both by power button or power-off
Option
Use power button for boot/shutdown,sleep and wakeup, it can be delete if no need;
Over-temperature Protection & RESET
Power of VDD_CPU_B
Trace>4.5A
Power of VDD_GPU
Trace>4.0A
Power of VCC3V3_SYS
Trace>2.0A
Power of VDD_LOG
Trace>1.0A
VDD_LOG:
Min=0.8V;
Default=0.9V;
Max=1.4V;
Note:
The PWM parameter needs to be modified according to the LOG_DVS_PWM power supply,please refer to RK3399 design guide
Power of VCCA_0V9
Power of VCC3V0_SD
Rockchip
Fuzhou Rockchip Electronics
Project: RK3399_BOX_REF
File: 21.Power-PMIC RK808-D
Date: Tuesday, August 21, 2018
Rev: V1.3
Sheet: 19 of 45
Designed by: Linus

USB2.0 HOST Port



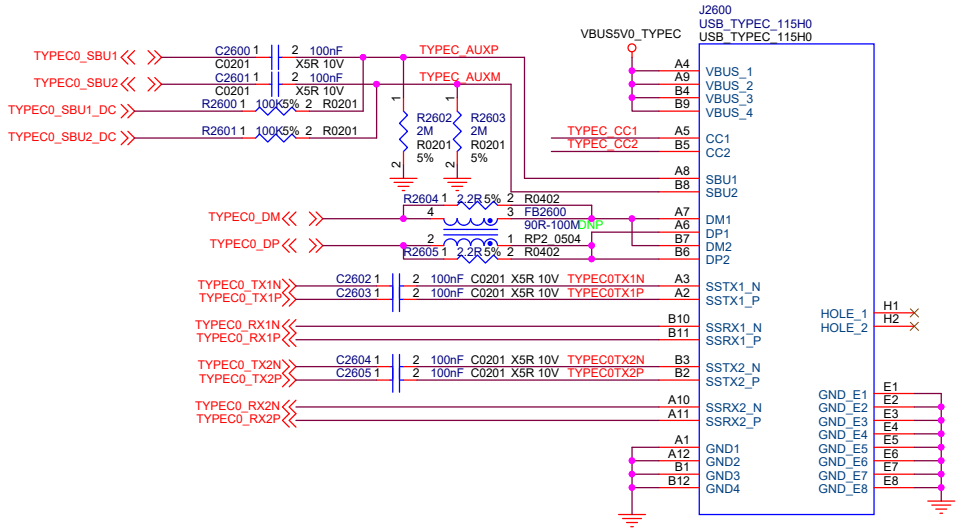
USB3.0 HOST Port



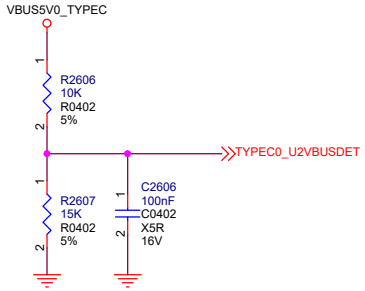
Note:All the ESD components should be placed close to the port

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	25.USB HOST Port		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	20 of 45

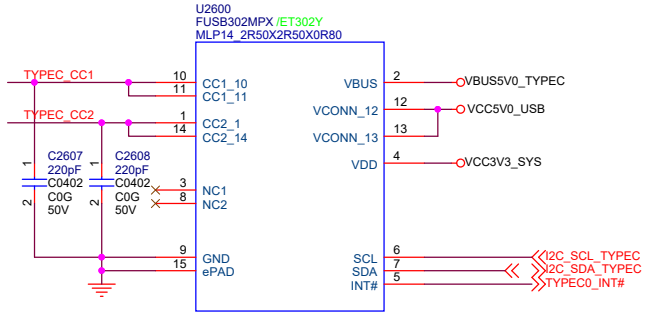
USB Type-C Port

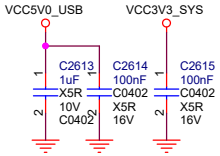


USB Detection

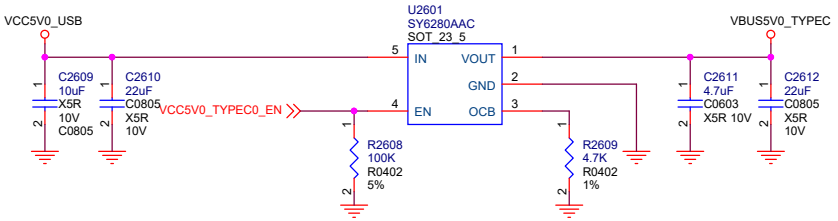


USB Type-C CC CTRL



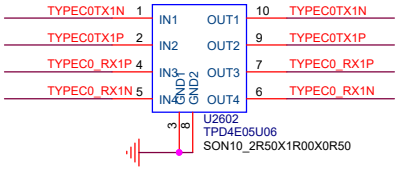


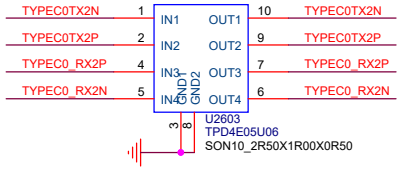
USB Type-C Power

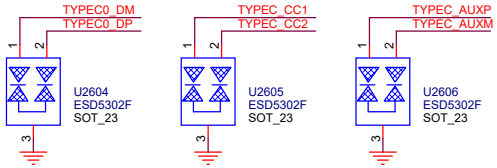


ESD

Note:All the ESD components should be placed close to the port and Cj<=0.4pF



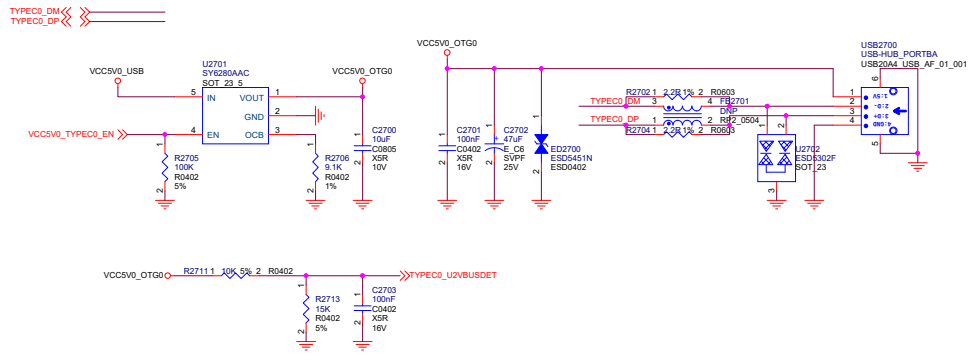




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	26.USB Type-C Port		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	21 of 45

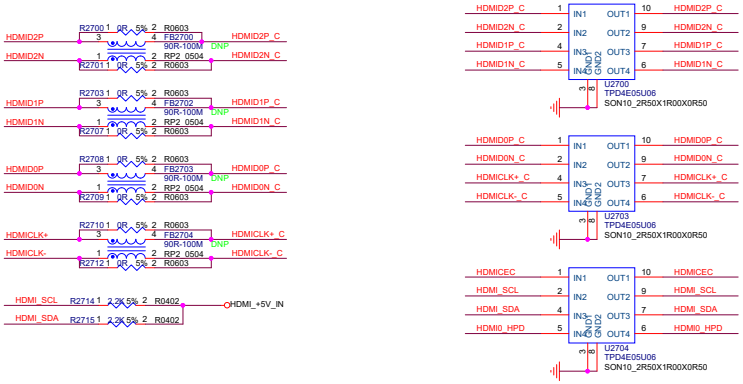
USB Port

Note:USB Port for firmware download is necessary, so it can not be deleted

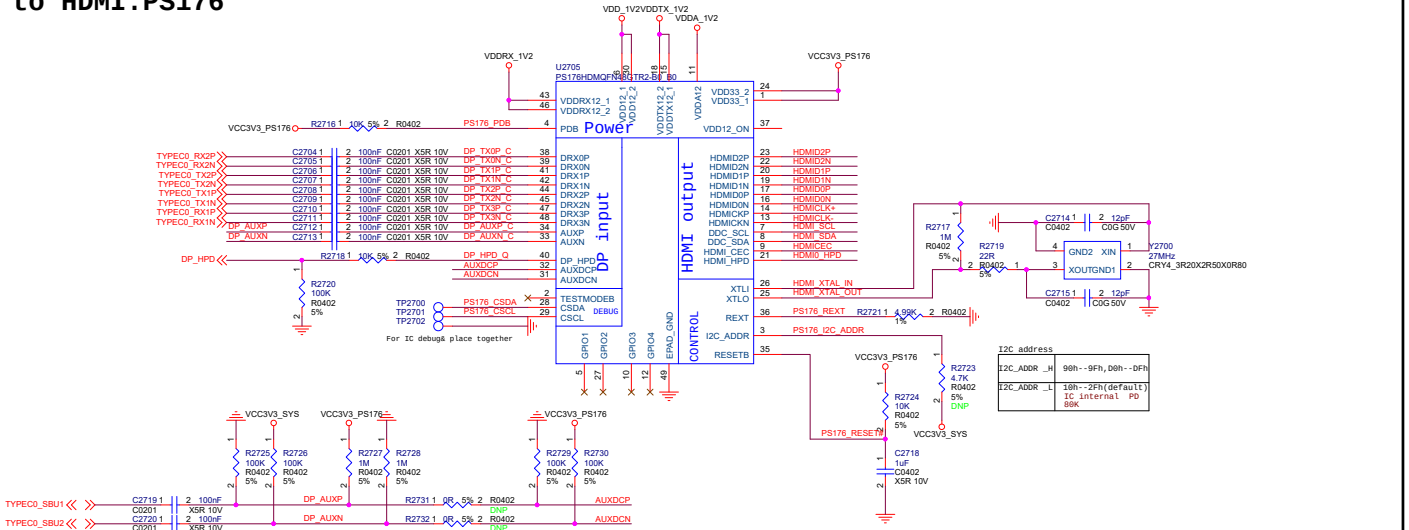


Common Choke and ESD

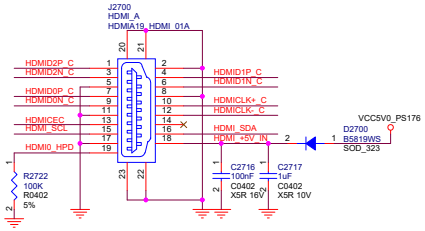
Note:All the ESD components should be placed close to the port



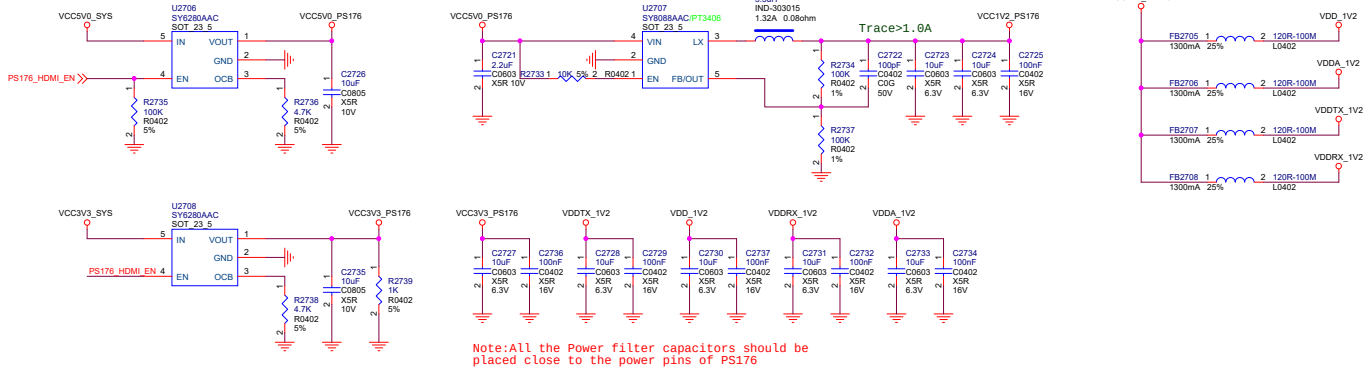
DP to HDMI:PS176



HDMI Output Port



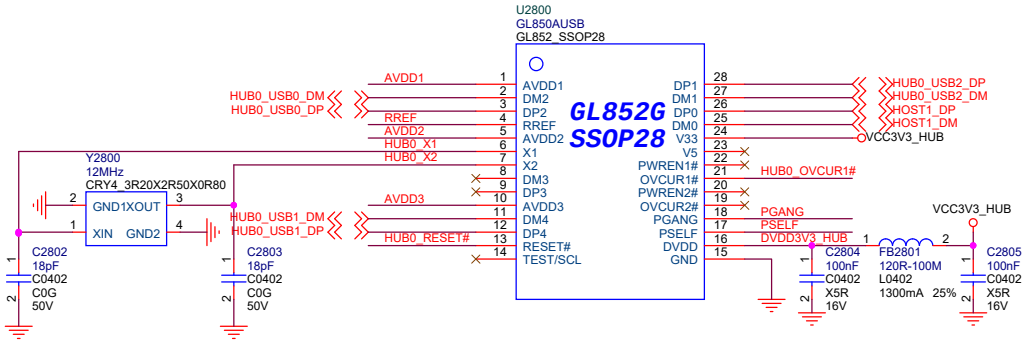
PS176 Power

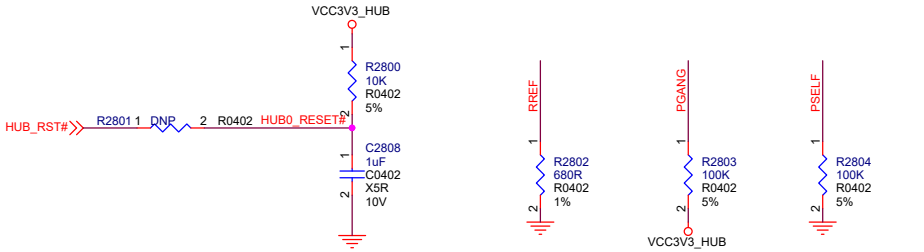


Note:All the Power filter capacitors should be placed close to the power pins of PS176

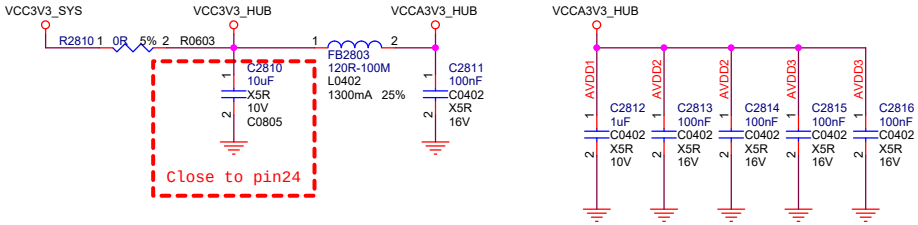
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	27.USB Type-C Alt Mode(option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	22 of 45

USB2.0 HUB



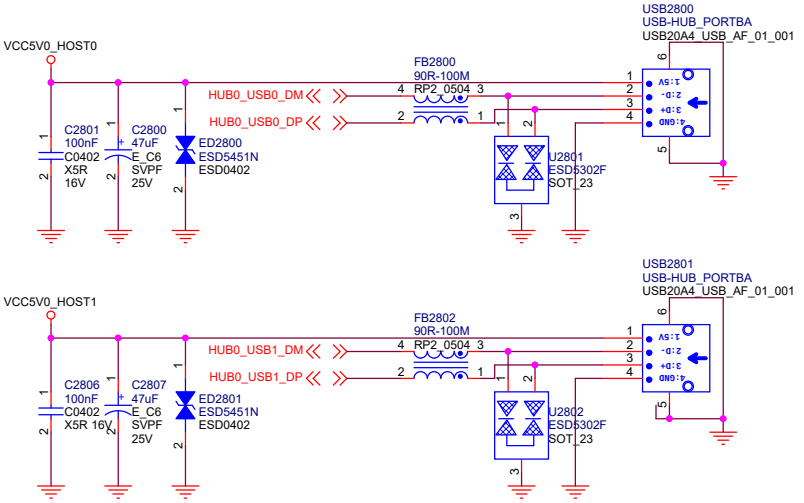


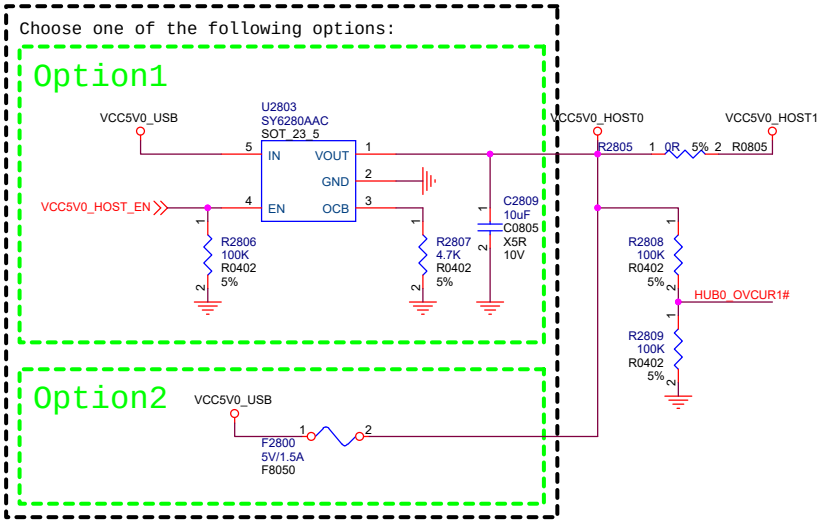
HUB Power



Note:All the Power filter capacitors should be placed close to the power pins of GL852G

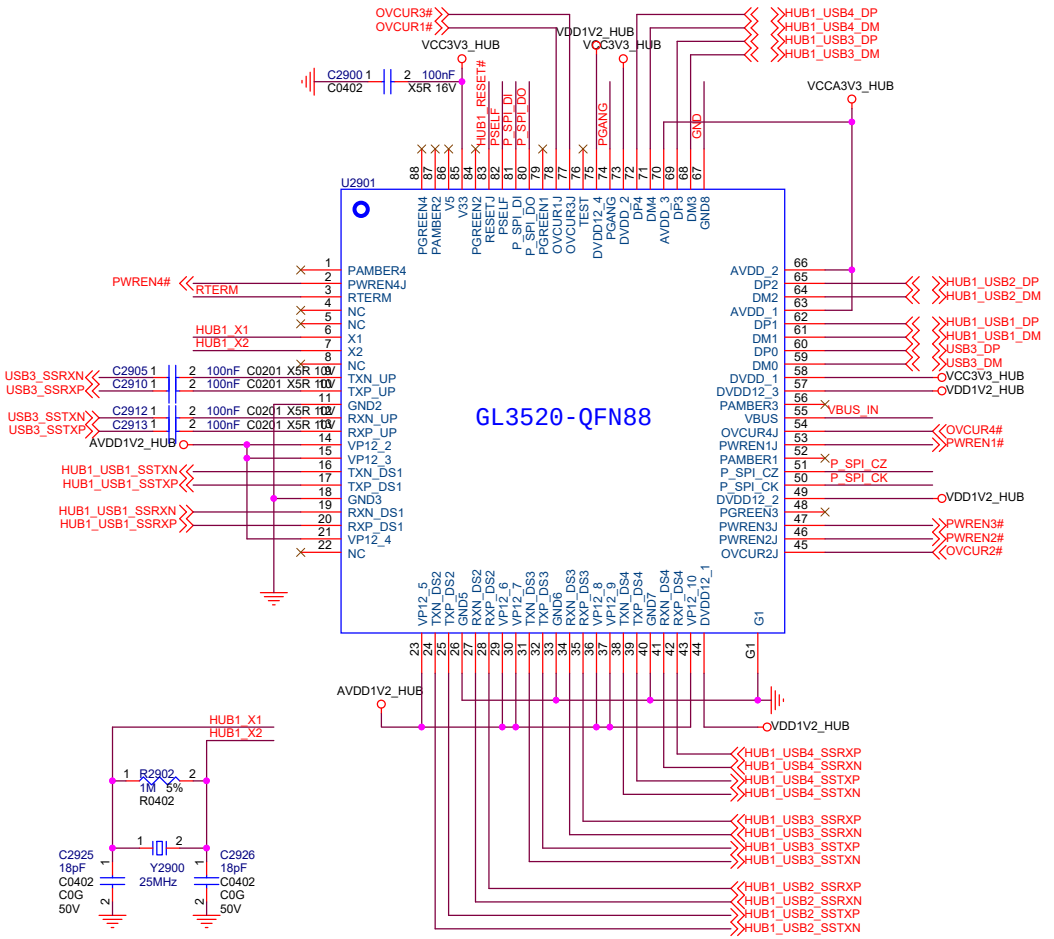
USB2.0 Port

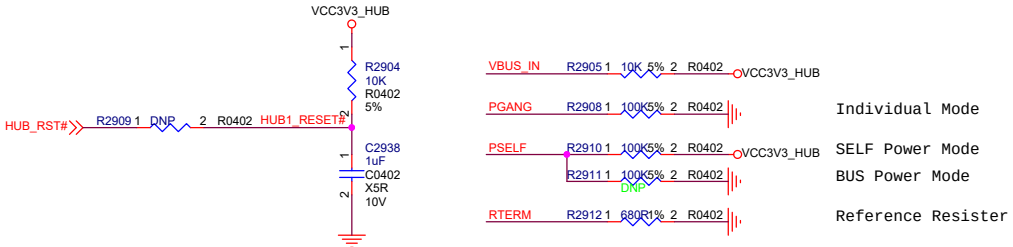




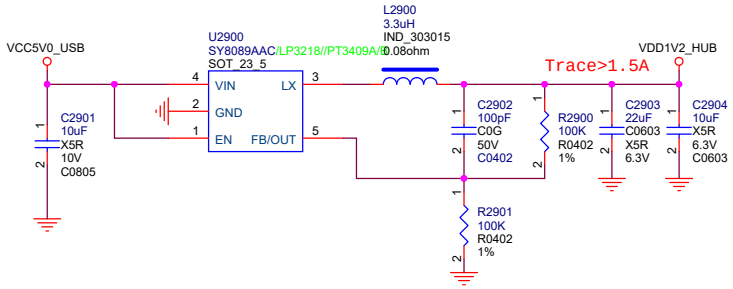
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	28.USB2.0 HUB-GL85x (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	23 of 45

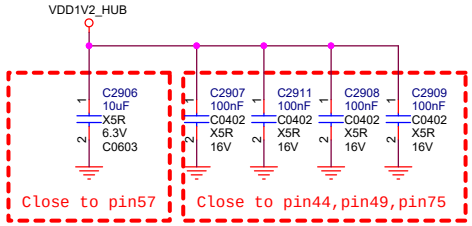
USB3.0 HUB

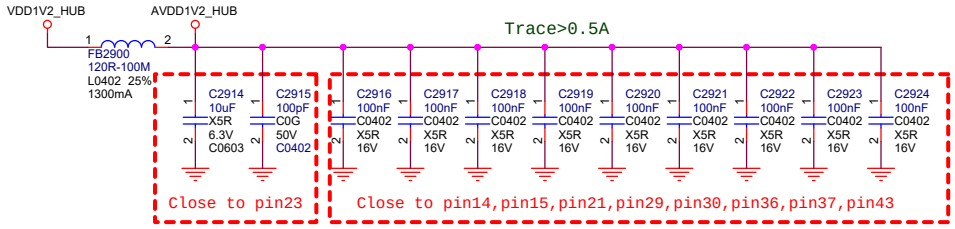


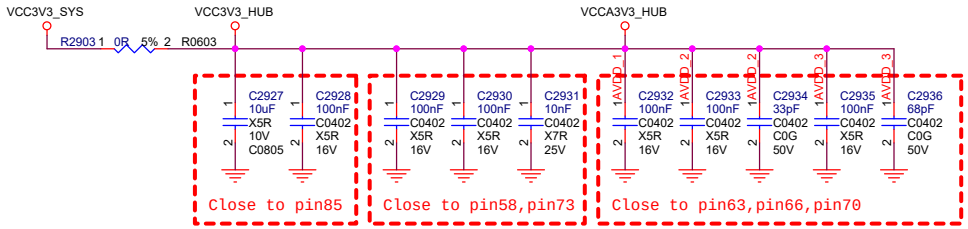


HUB Power

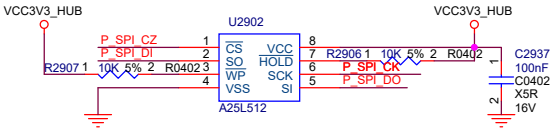








SPI Flash



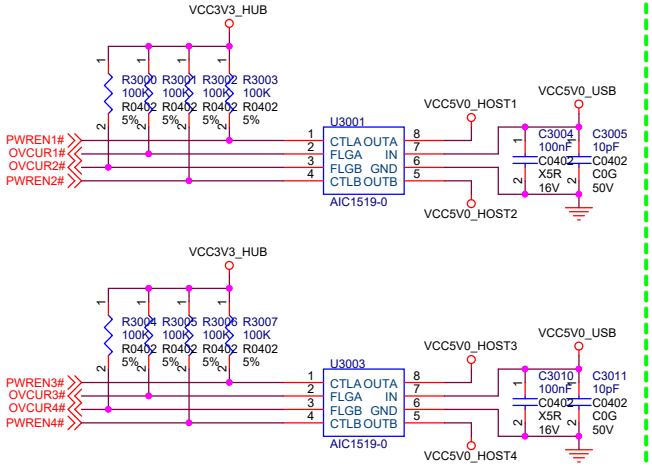
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	29.USB3.0 HUB-GL3523-1 (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	24 of 45

Port Power

Choose one of the following options:

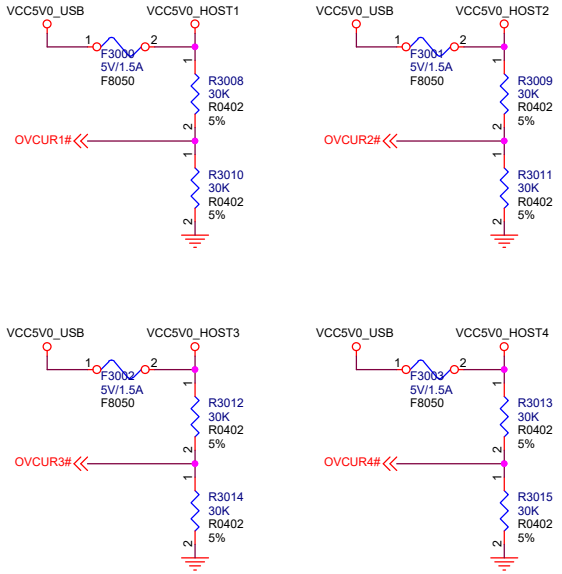
Option1

Power Switch CIRCUIT



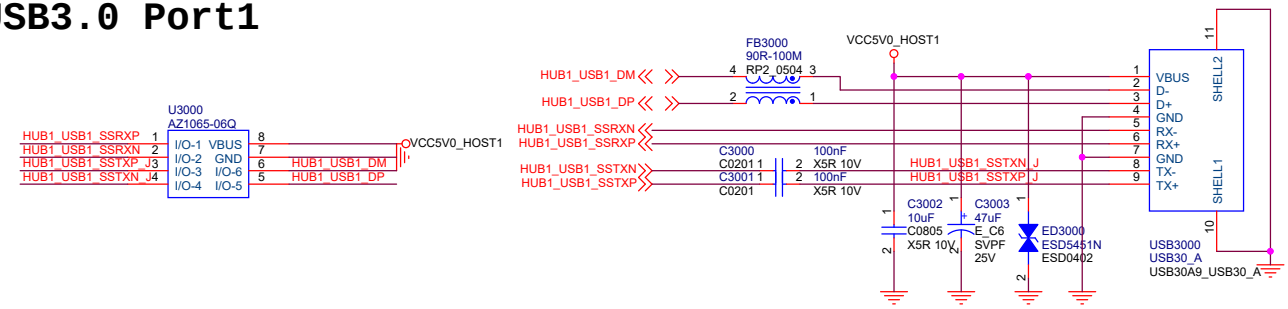
Option2

POLY-FUSE CIRCUIT

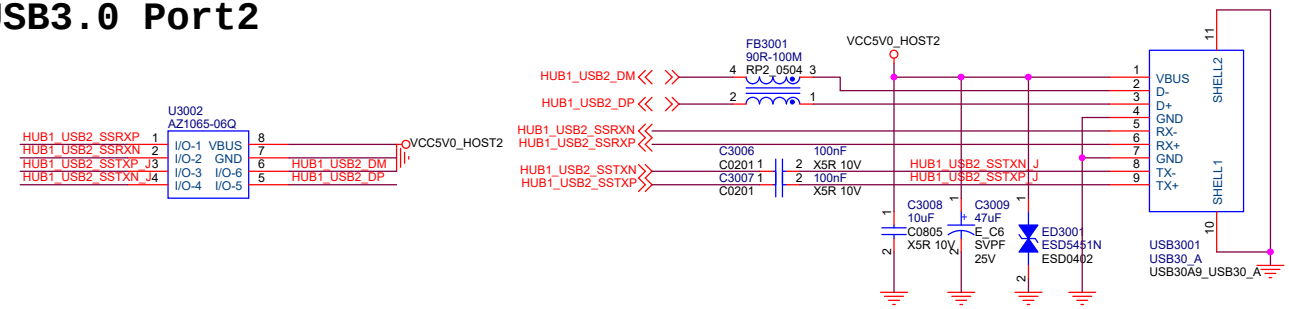


Note:OVCUR1#~4# Floating : Non-Removable (Compound device)

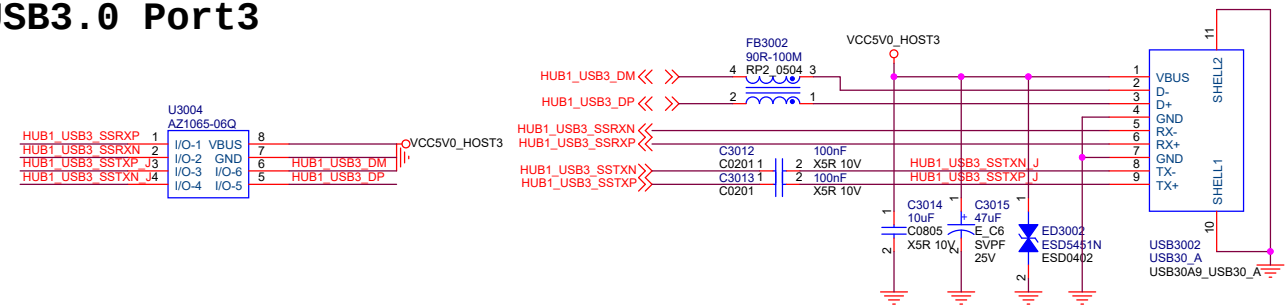
USB3.0 Port1



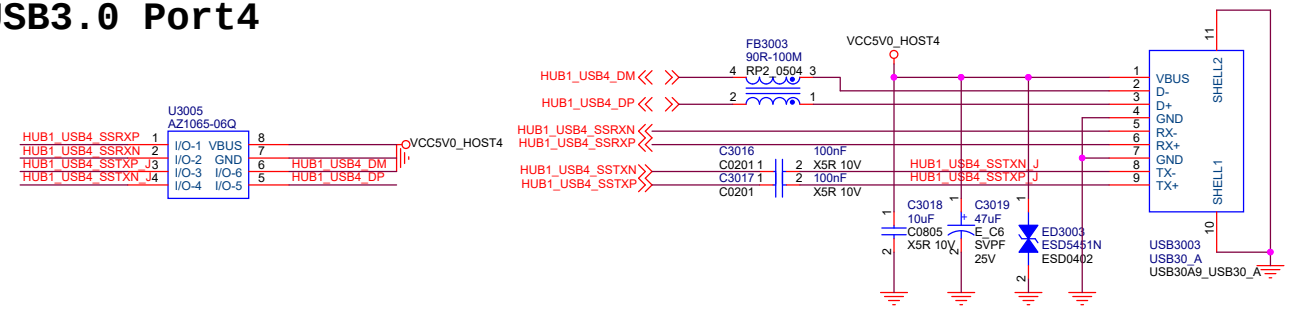
USB3.0 Port2



USB3.0 Port3



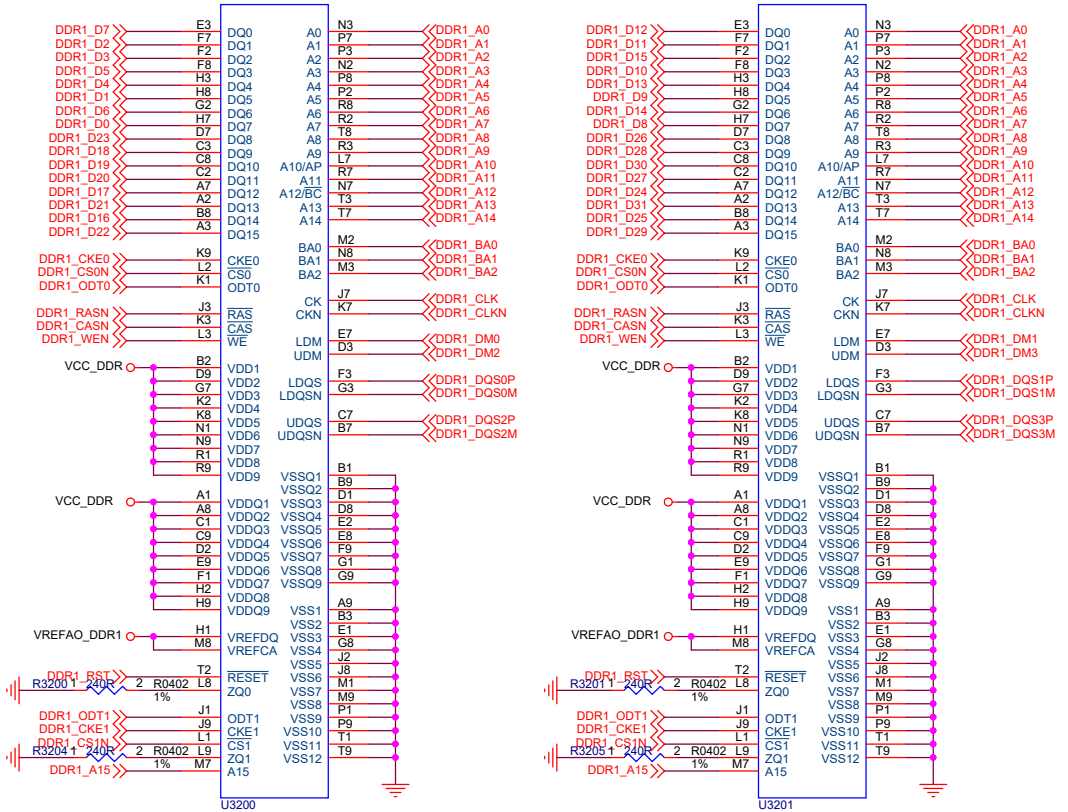
USB3.0 Port4

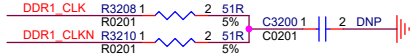


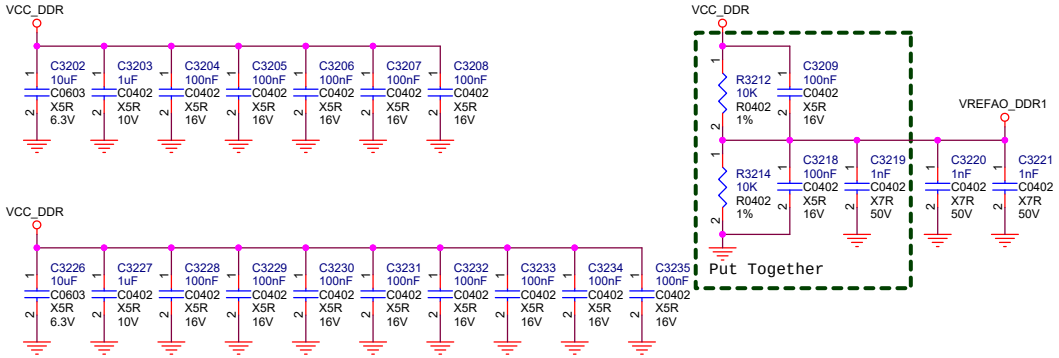
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	30.USB3.0 HUB-GL3523-2 (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	25 of 45

DDR3 4x16bit

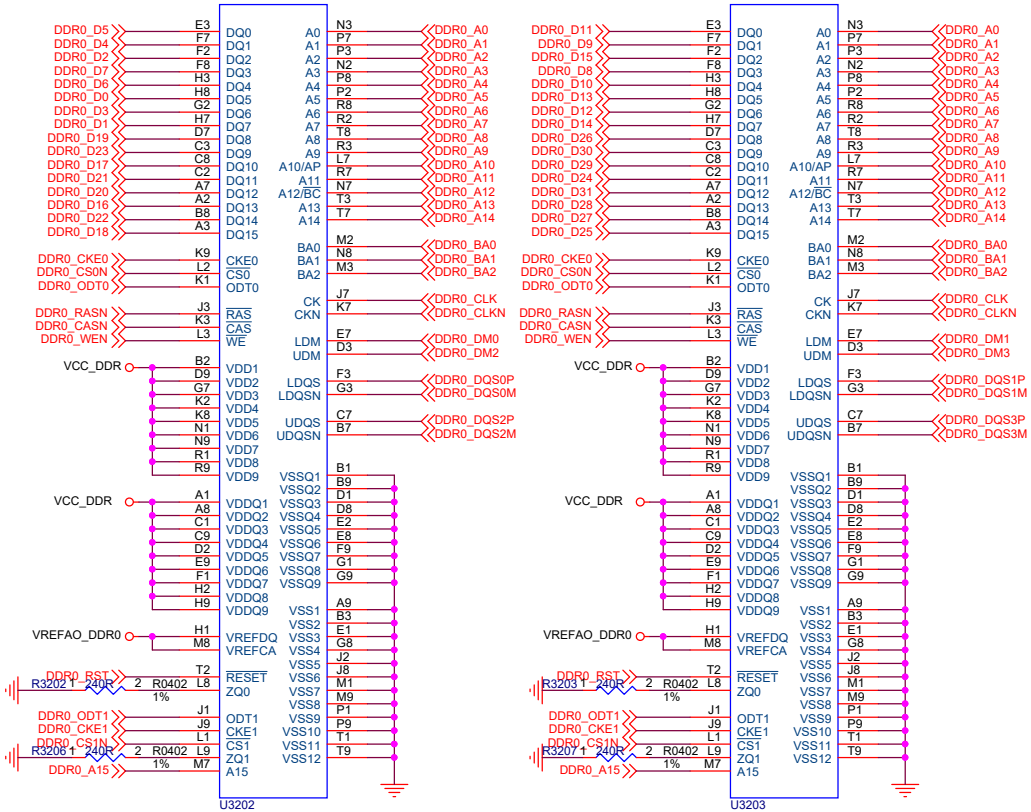
Note:The simulation frequency of the template is 800MHz.
Remind: Refer to the latest AVL for parts selection.

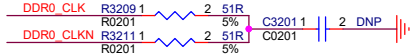


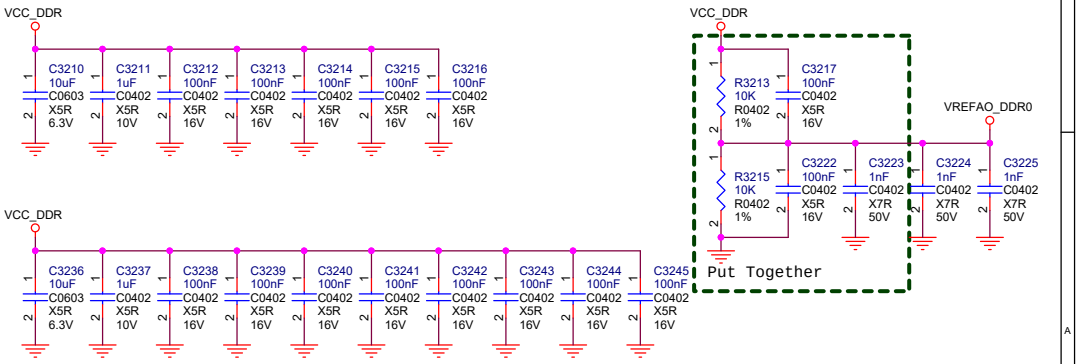




Note:All the Power filter capacitors should be placed close to the power pins of DDR





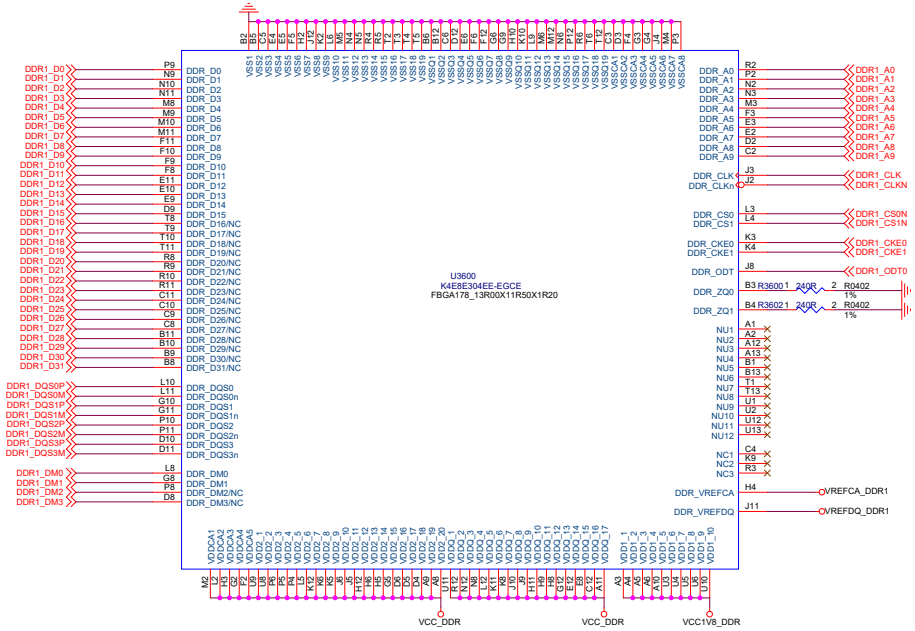


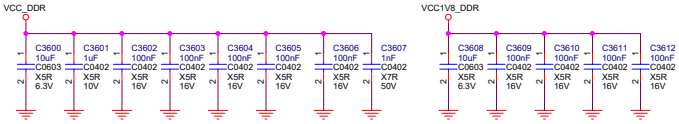
Note:All the Power filter capacitors should be placed close to the power pins of DDR

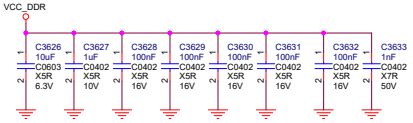
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	32.RAM-DDR3 4x16bit(option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	26 of 45

LPDDR3 2x32bit 178ball

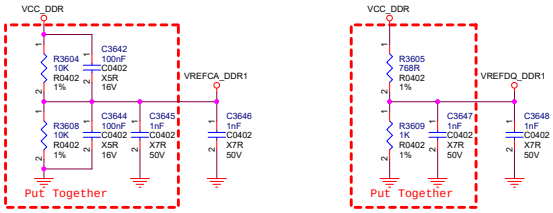
Note:The simulation frequency of the template is 800MHz.
Remind: Refer to the latest AVL for parts selection.





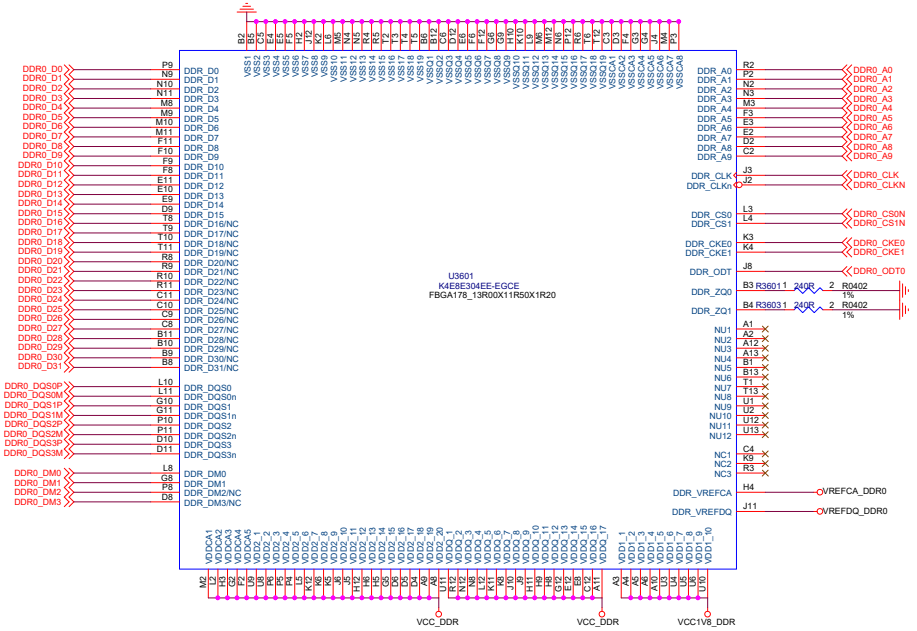


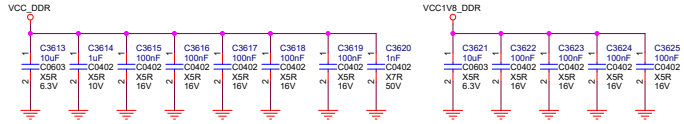
Note:All the Power filter capacitors should be placed close to the power pins of DDR

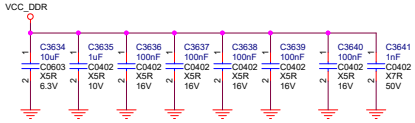


Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

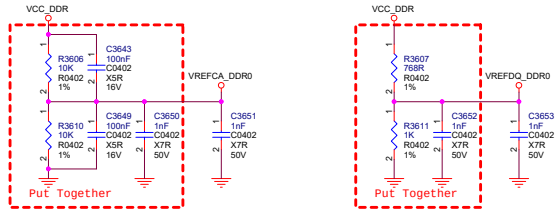
eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V





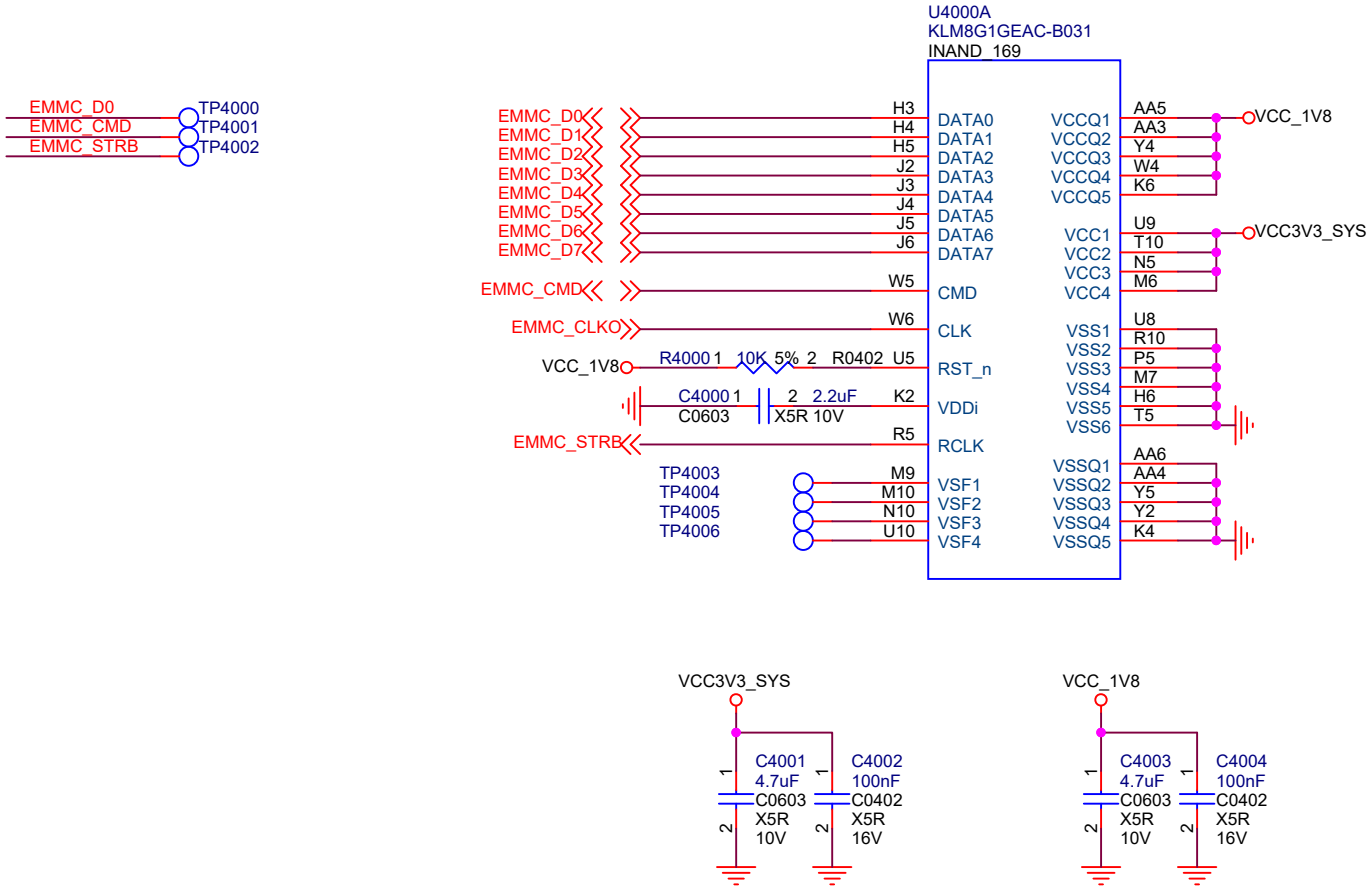


Note:All the Power filter capacitors should be placed close to the power pins of DDR



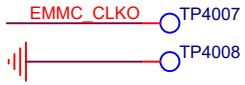
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	36.RAM-LPDDR3(178P)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	27 of 45

eMMC FLASH



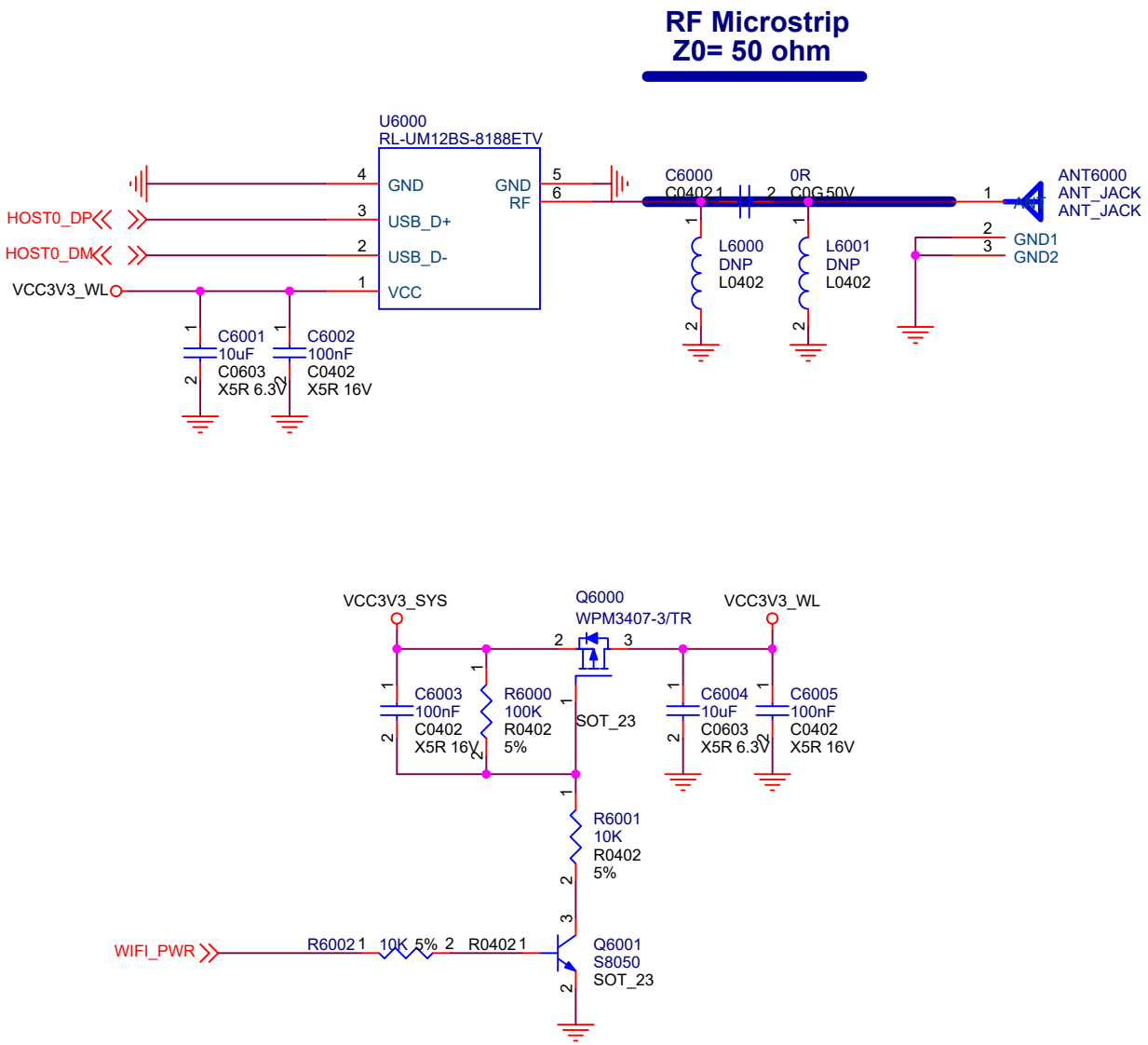
Note:All the Power filter capacitors should be placed close to the power pins of eMMC

Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	40.Memory-eMMC		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	28 of 45

USB WIFI MODULE



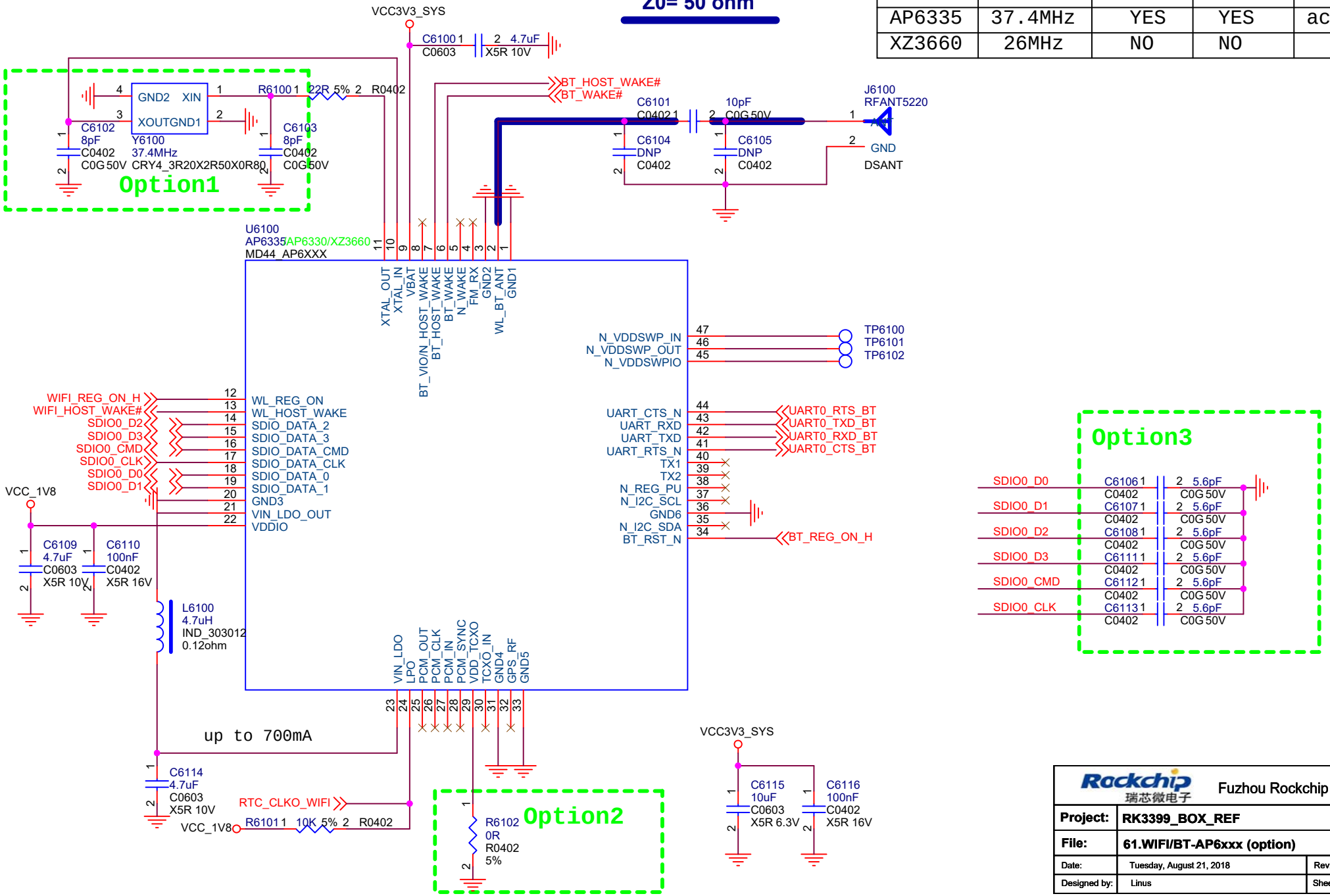
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	60.WIFI-USB (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	29 of 45

SDIO WIFI/BT MODULE

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

YES:should mounted; NO:don't mounted

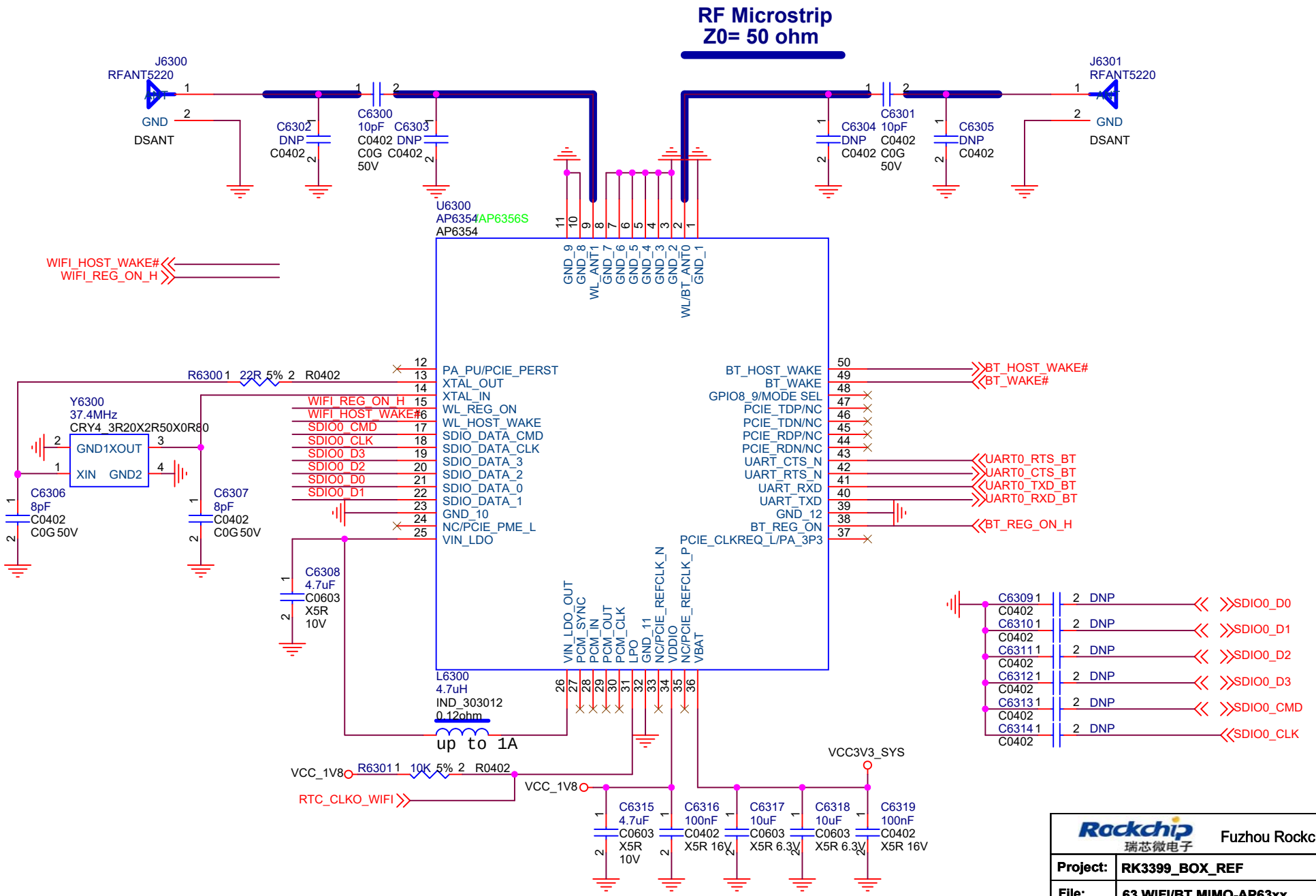
	Option1	Option2	Option3	
AP6212	26MHz	NO	NO	
AP6330	26MHz	NO	NO	
AP6335	37.4MHz	YES	YES	ac
XZ3660	26MHz	NO	NO	



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	61.WIFI/BT-AP6xxx (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	30 of 45

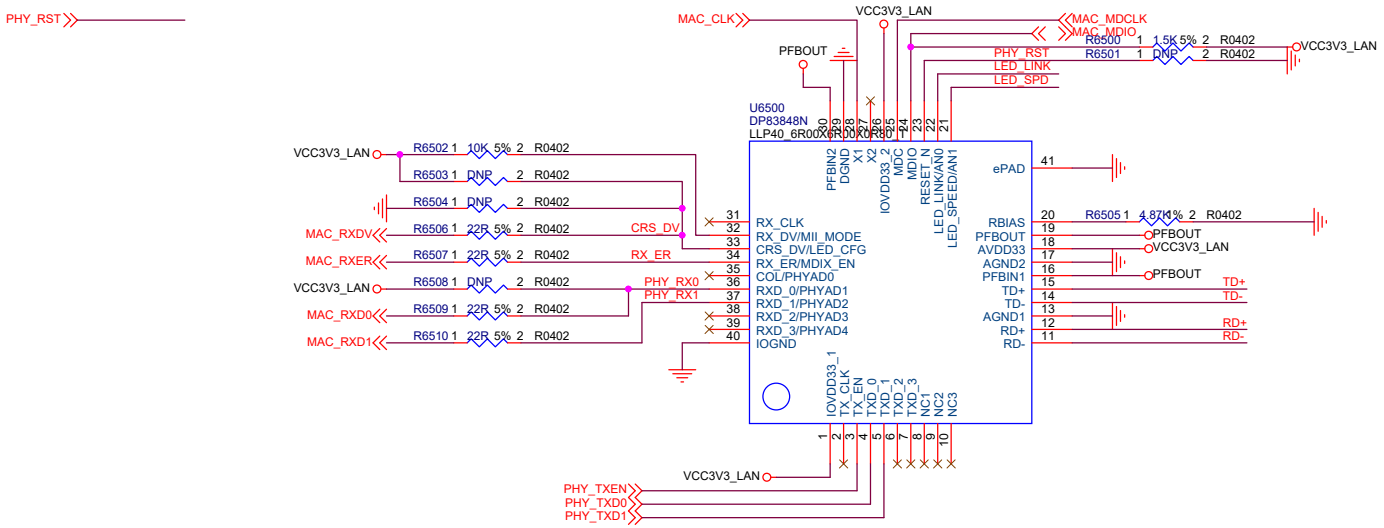
SDIO WIFI/BT MODULE-MIMO

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

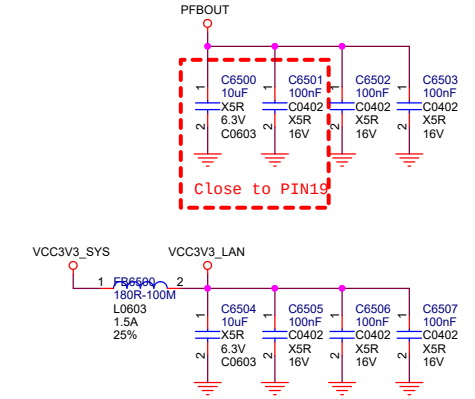


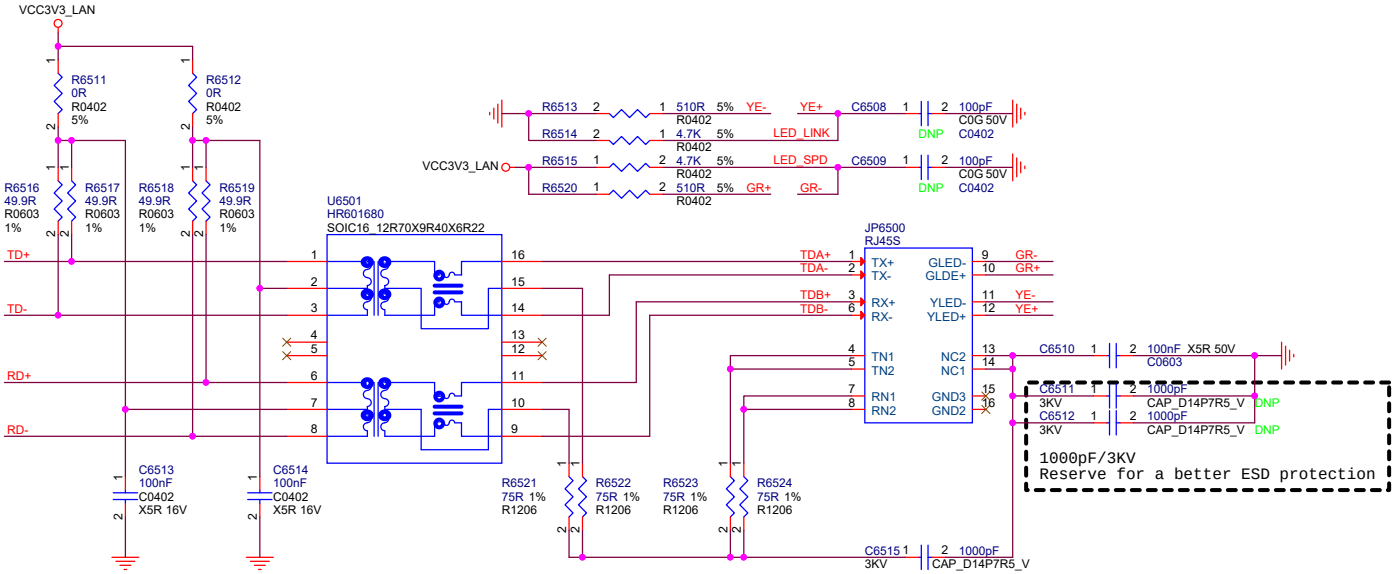
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	63.WIFI/BT MIMO-AP63xx		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	31 of 45

EMAC 10/100 MII Ethernet PHY



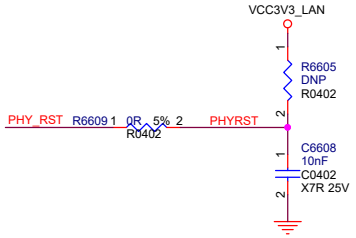
Power

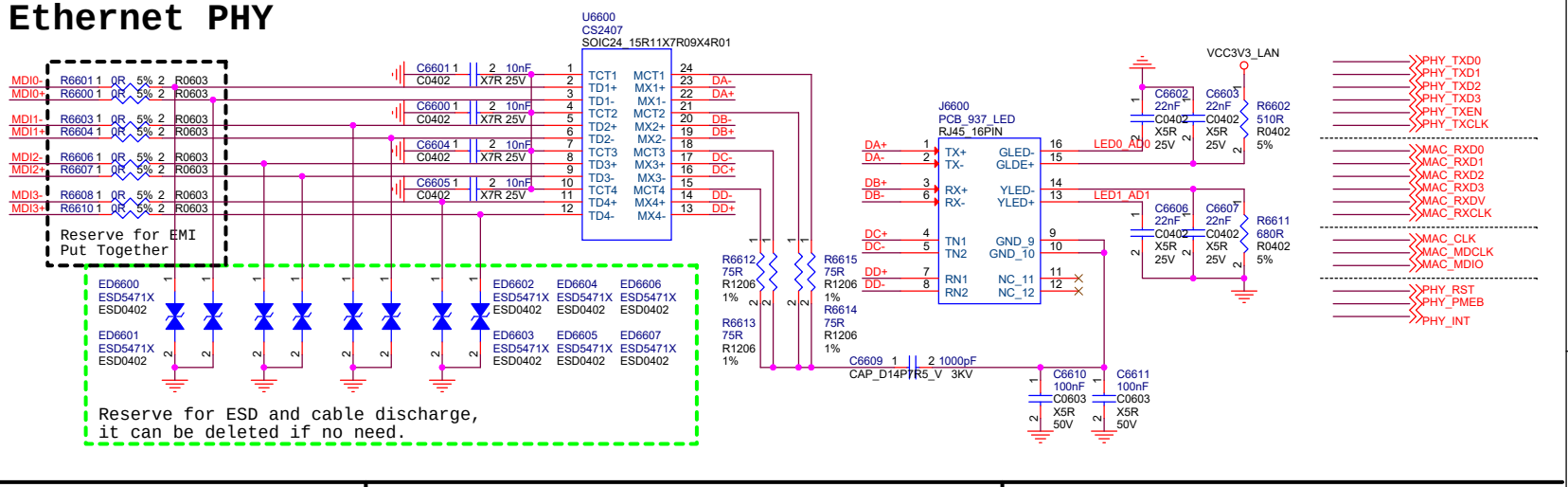


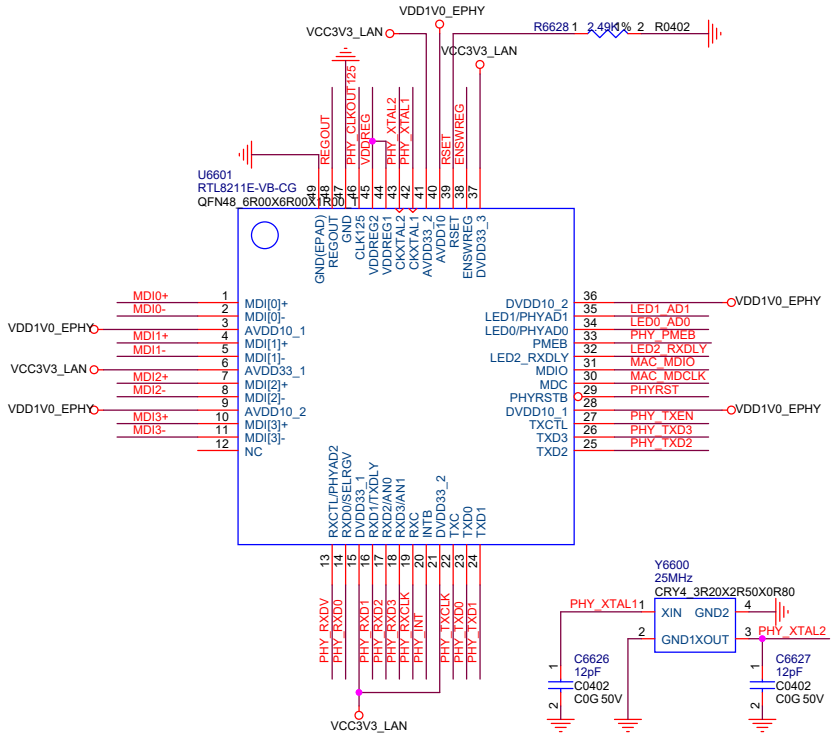


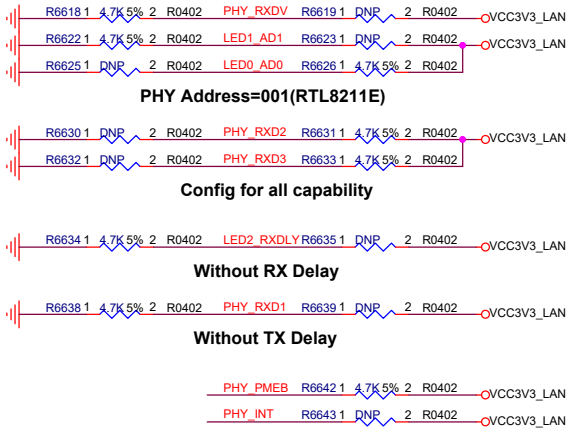
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	65.EMAC-DP83848N (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	32 of 45

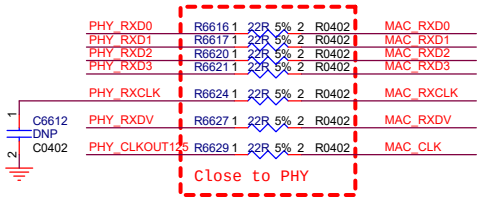
GMAC 10/100/1000 RGMII Ethernet PHY

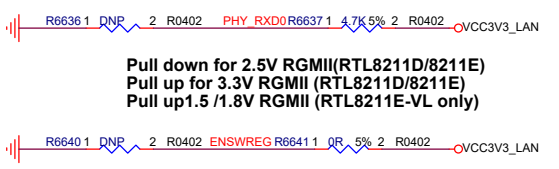


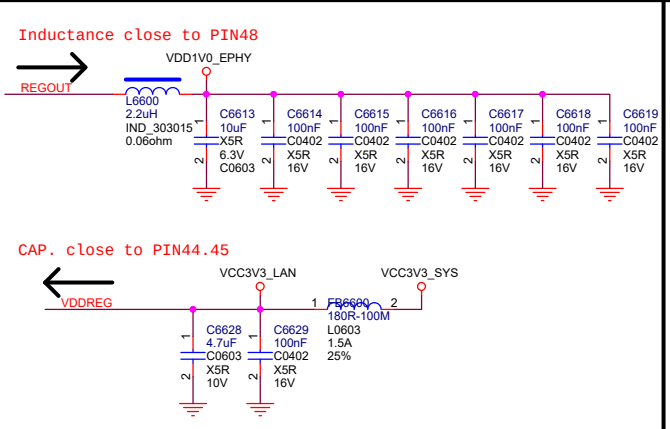


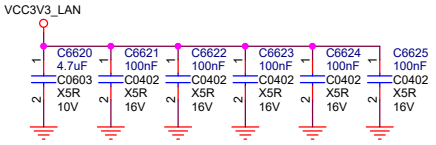






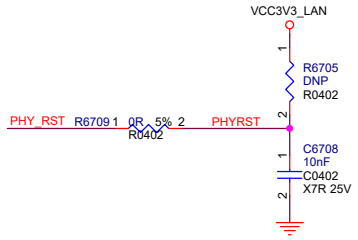




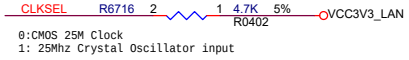


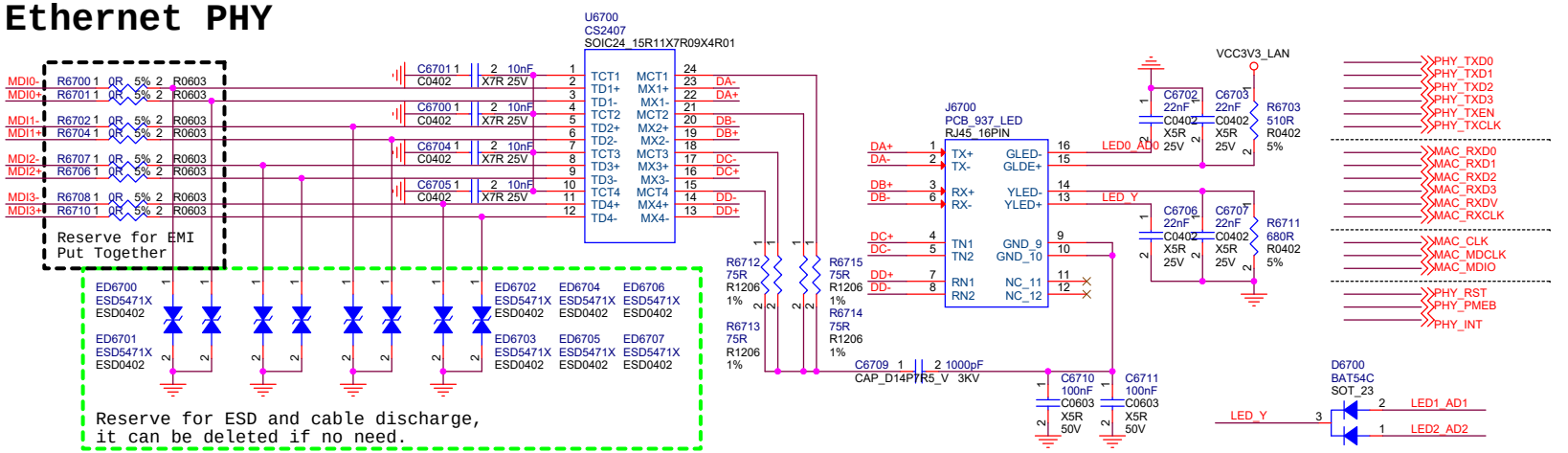
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	66.GMAC-RTL8211E		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	33 of 45

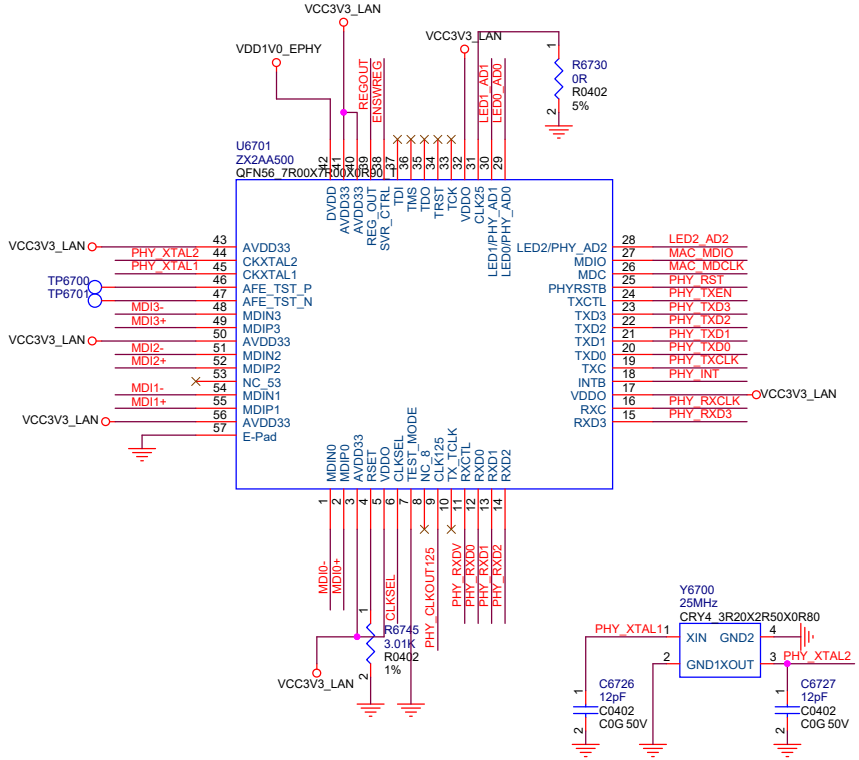
GMAC 10/100/1000 RGMII Ethernet PHY

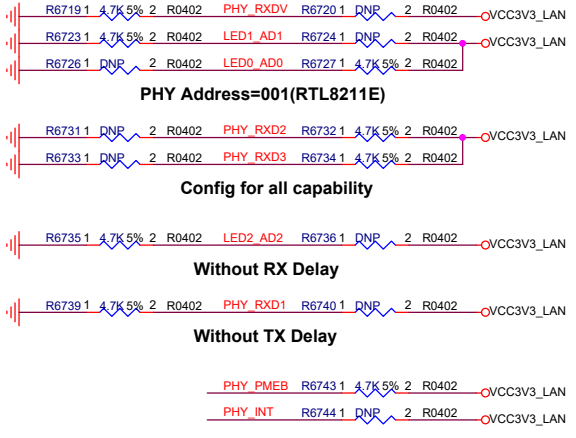


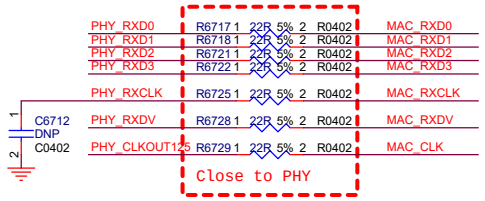
Clock select

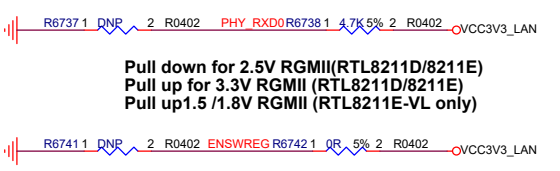


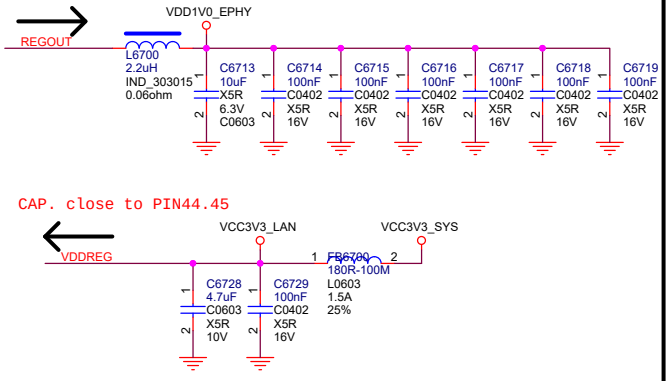


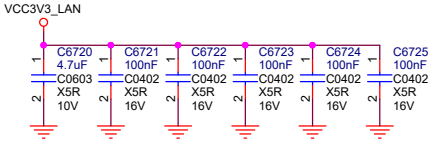






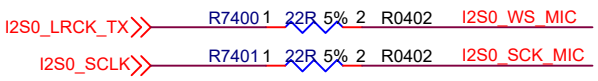




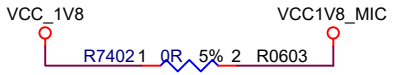


Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF
File:	67.GMAC-ZX2AA500 (option)
Date: Tuesday, August 21, 2018	Rev: V1.3
Designed by: Linus	Sheet: 34 of 45

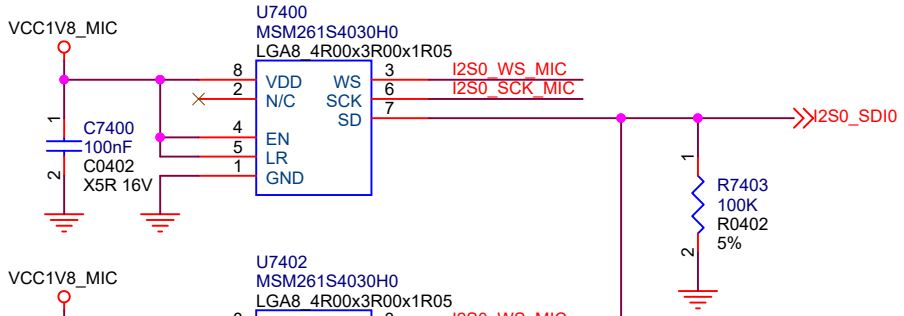
Microphone Array

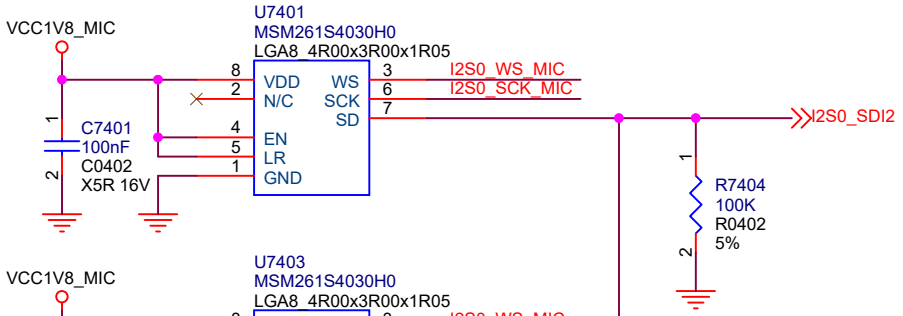


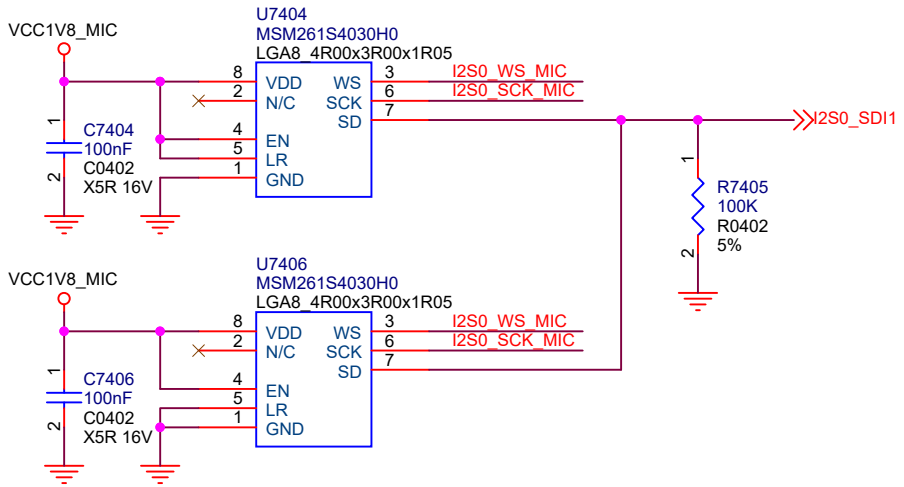
Power

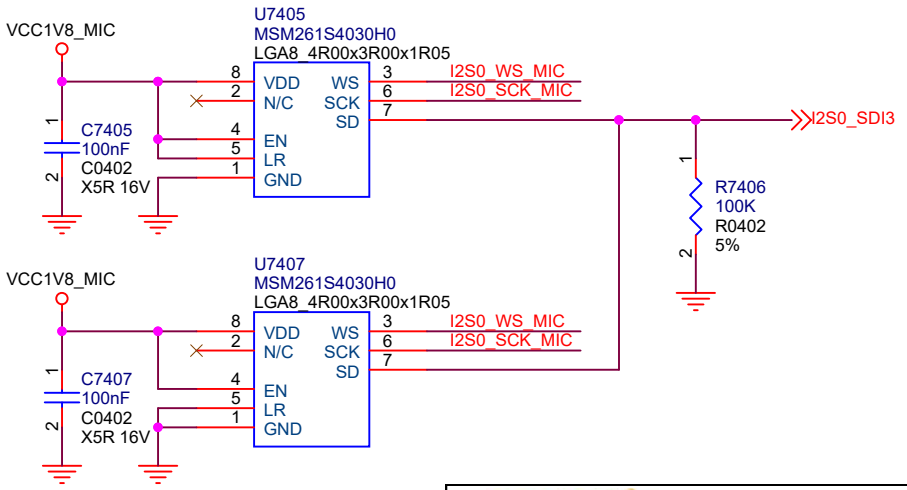


Note:
If it have the audio daughter board, please use independent power supply replace.





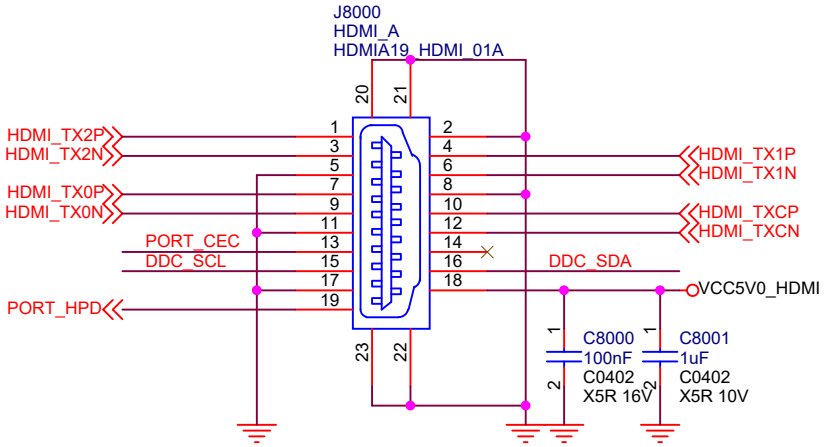


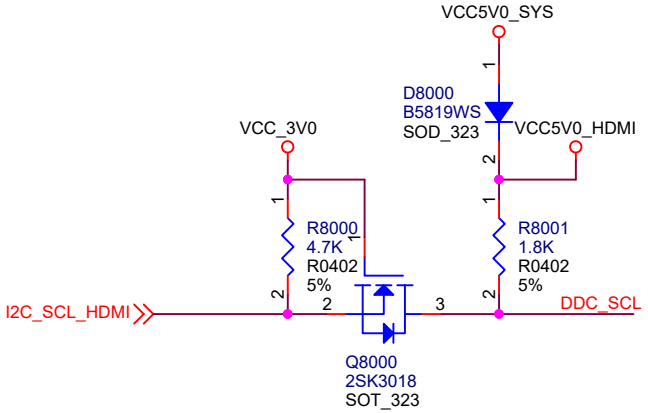


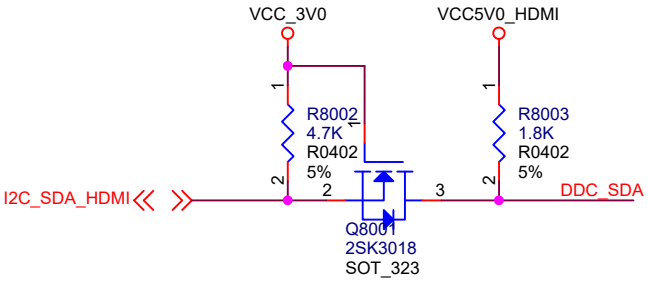
Note:The SDI line should have a 100kohm PD resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	74.Microphone Array		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	35 of 45

HDMI Output

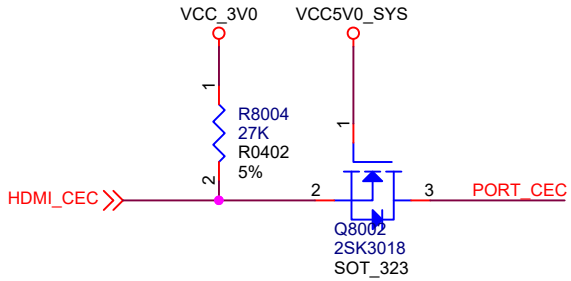






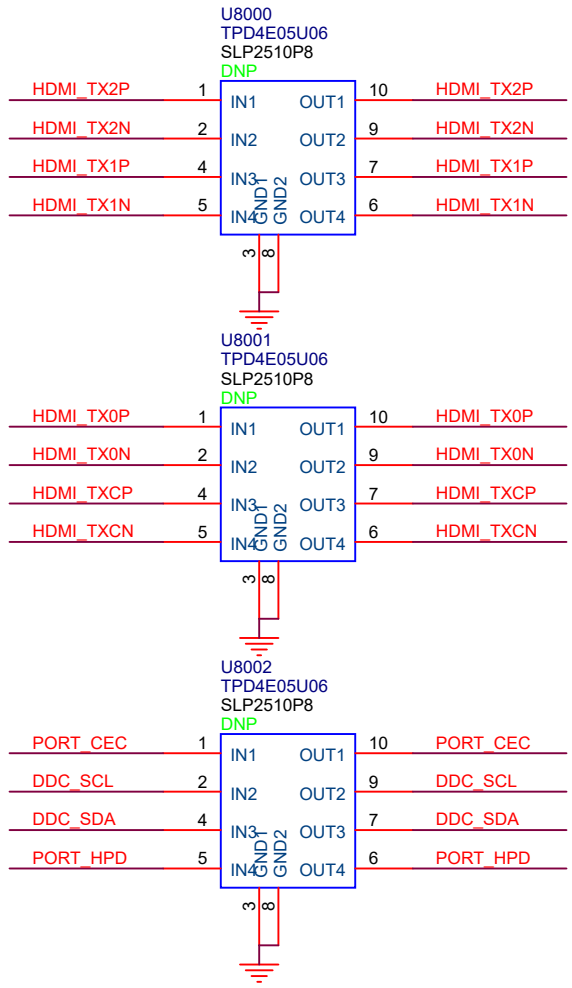
Option

Use for HDMI CEC function,
it can be deleted if no need;



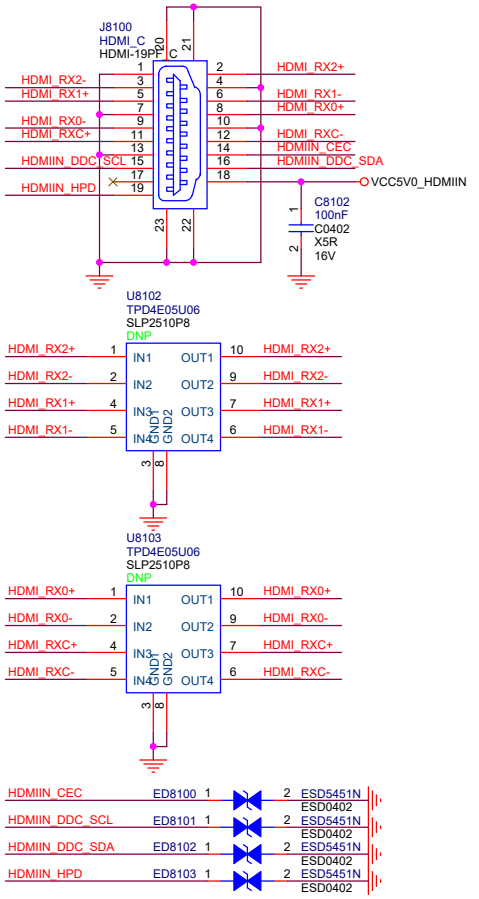
ESD

Note:All the ESD components should be placed close to the port and Cj<=0.4pF

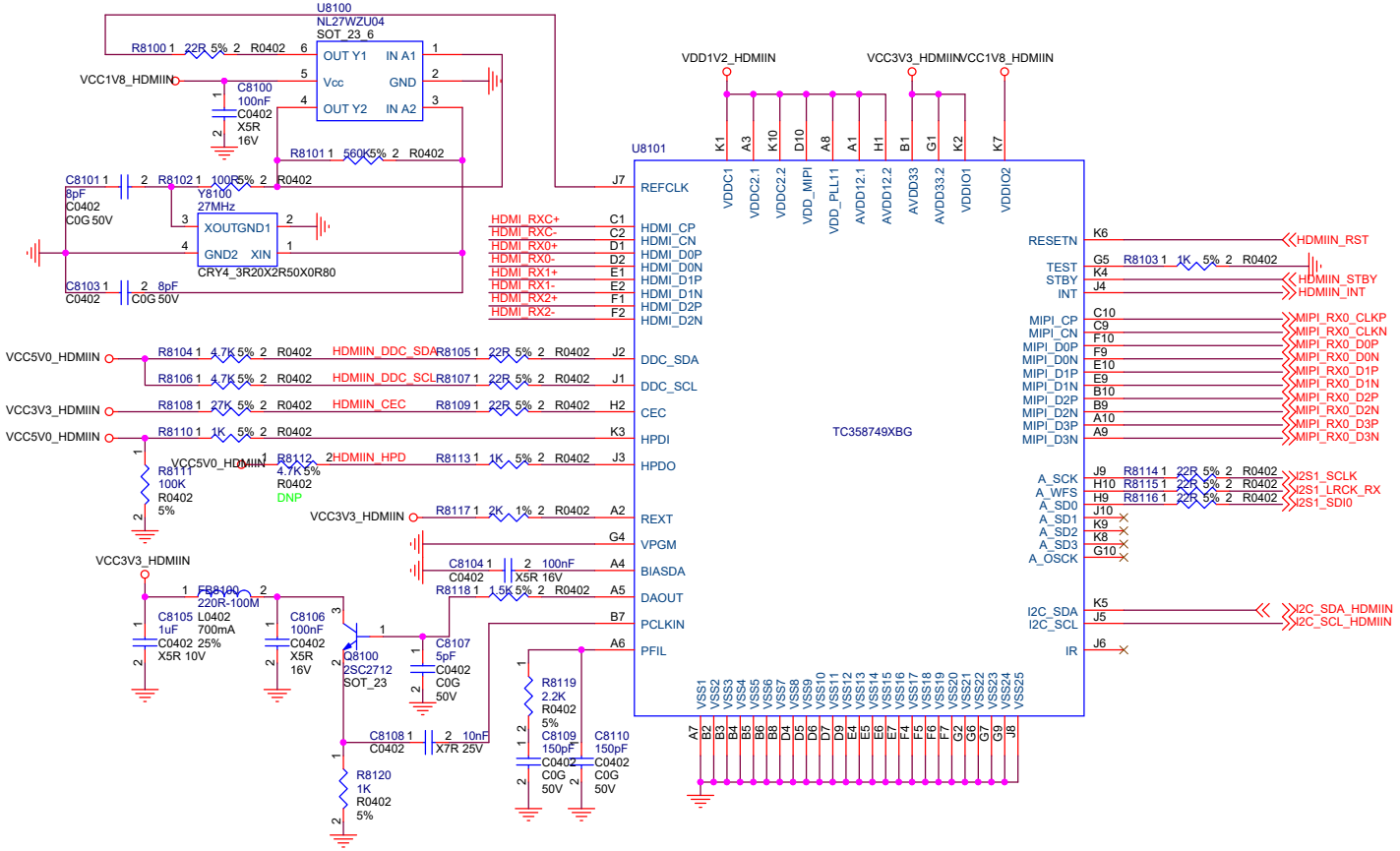


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	80.HDMI Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	36 of 45

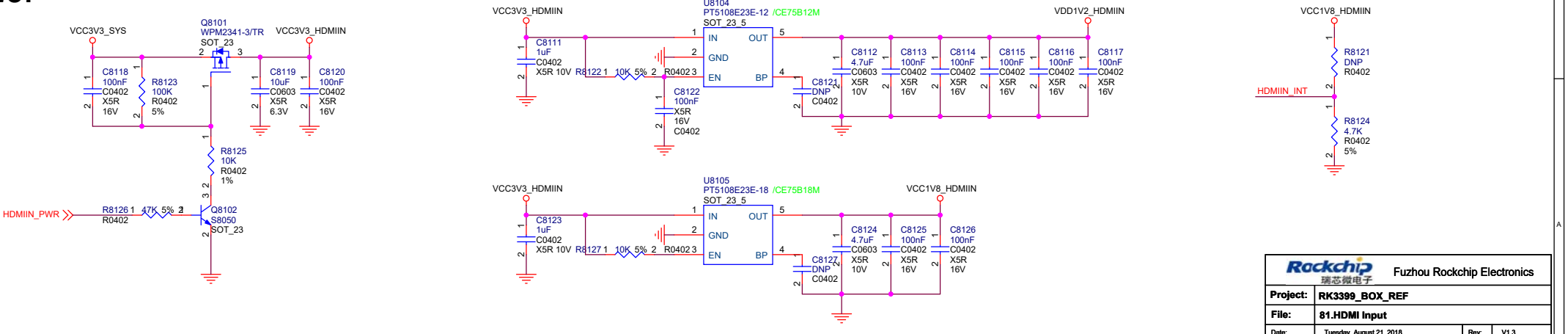
HDMI INPUT



HDMI to MIPI:TC358749XBG

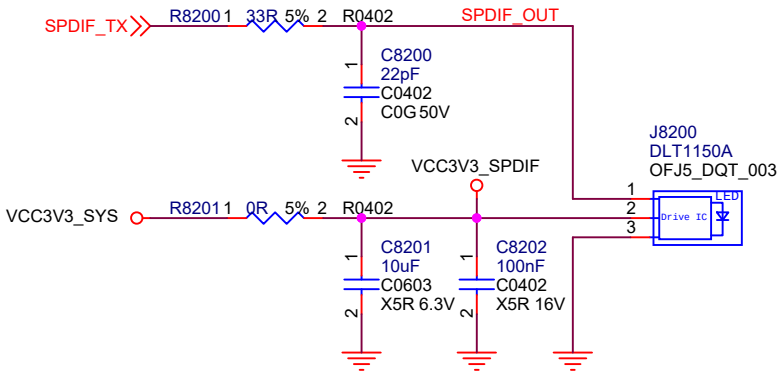


Power



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	81.HDMI Input		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	37 of 45

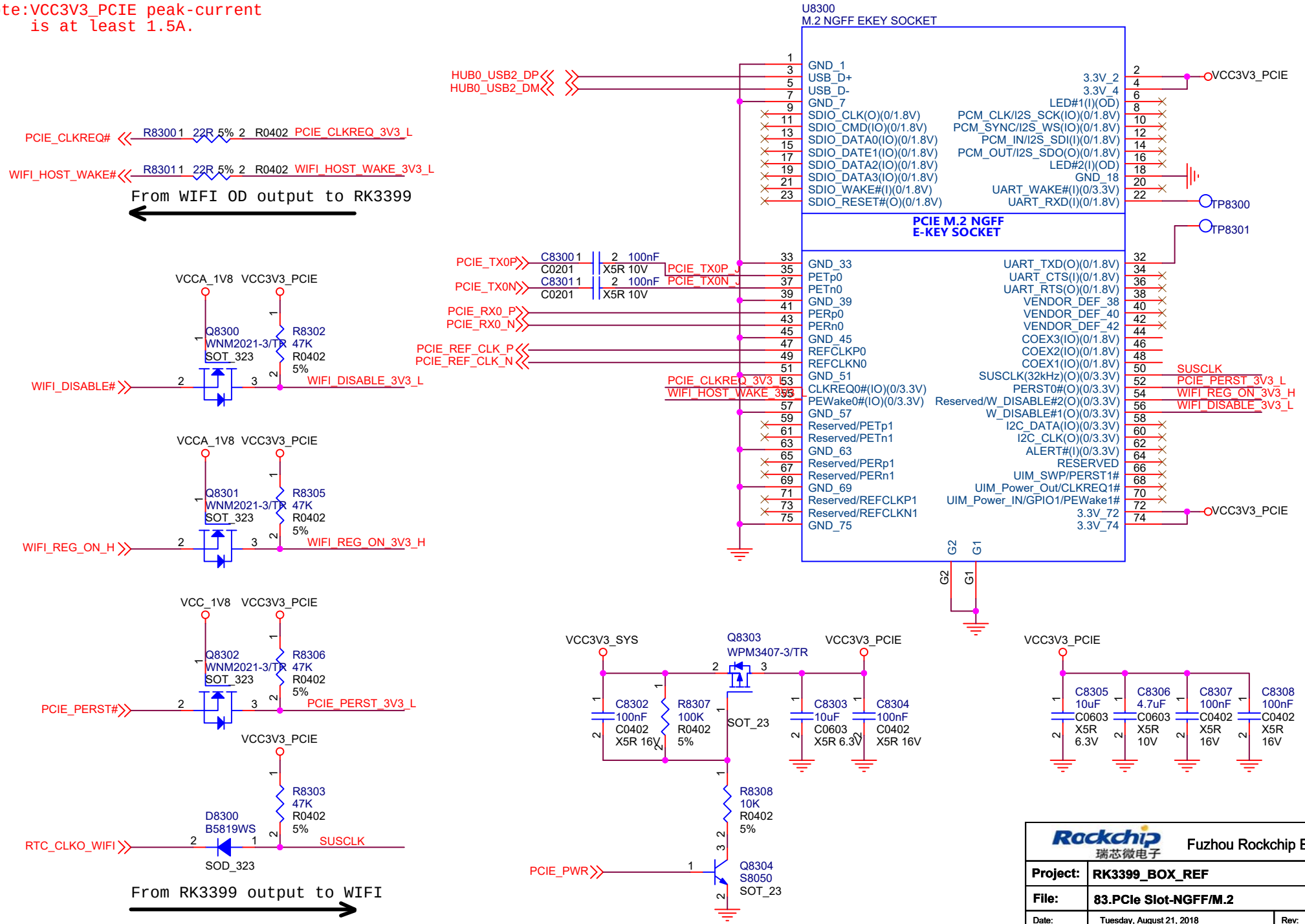
SPDIF OUT



Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
File:	82.SPDIF Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	38 of 45

PCIe Slot-NGFF/M.2

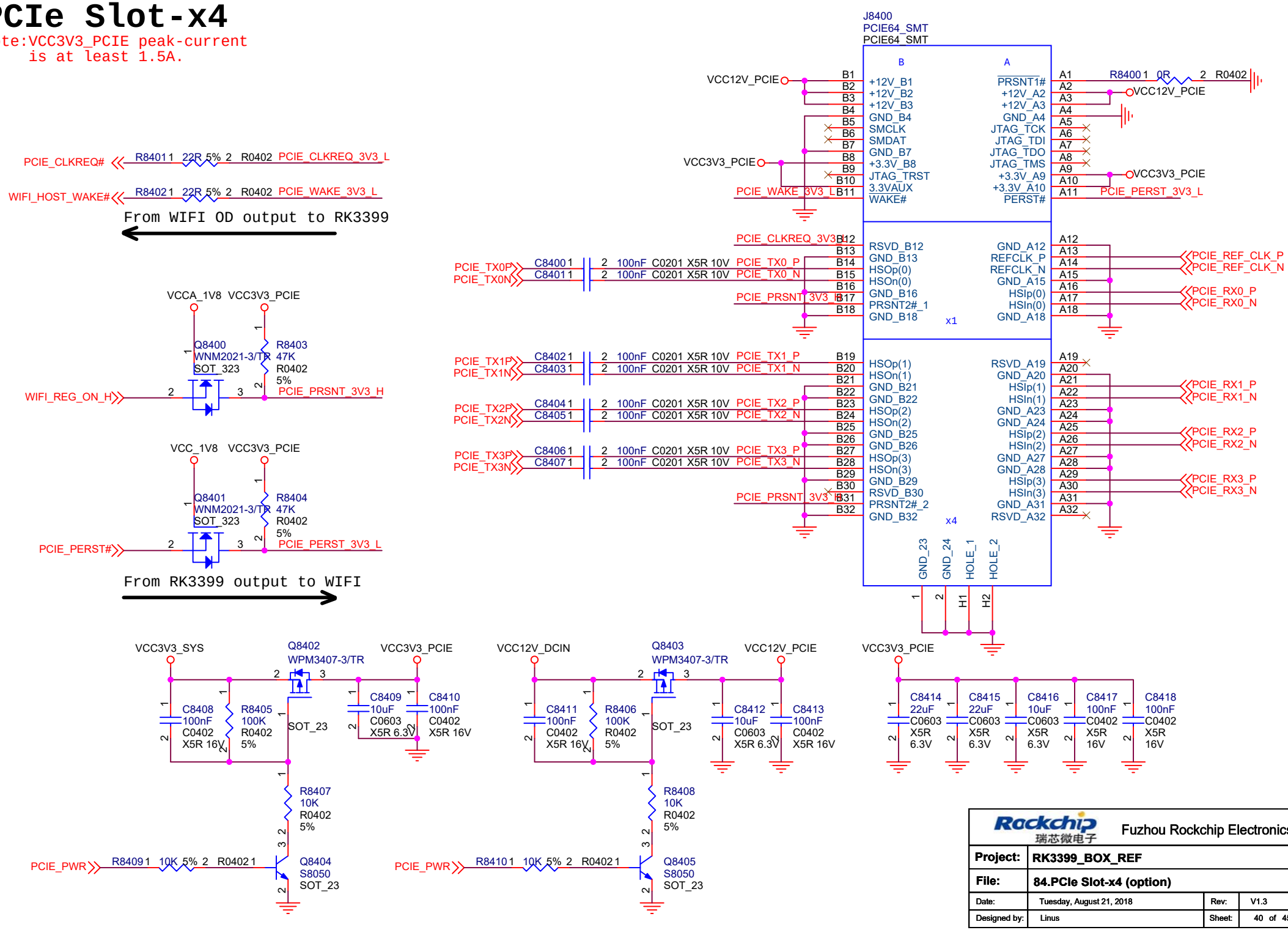
Note:VCC3V3_PCIE peak-current
is at least 1.5A.



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	83.PCIe Slot-NGFF/M.2		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	39 of 45

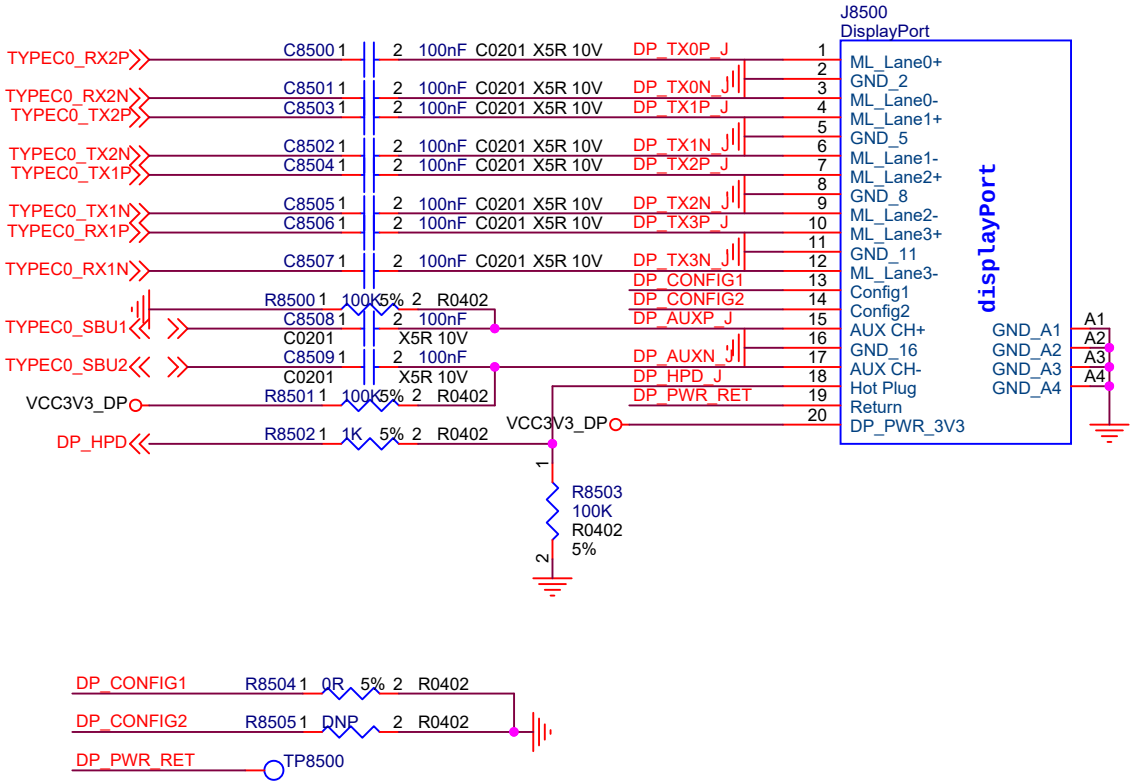
PCIe Slot-x4

Note:VCC3V3_PCIE peak-current
is at least 1.5A.

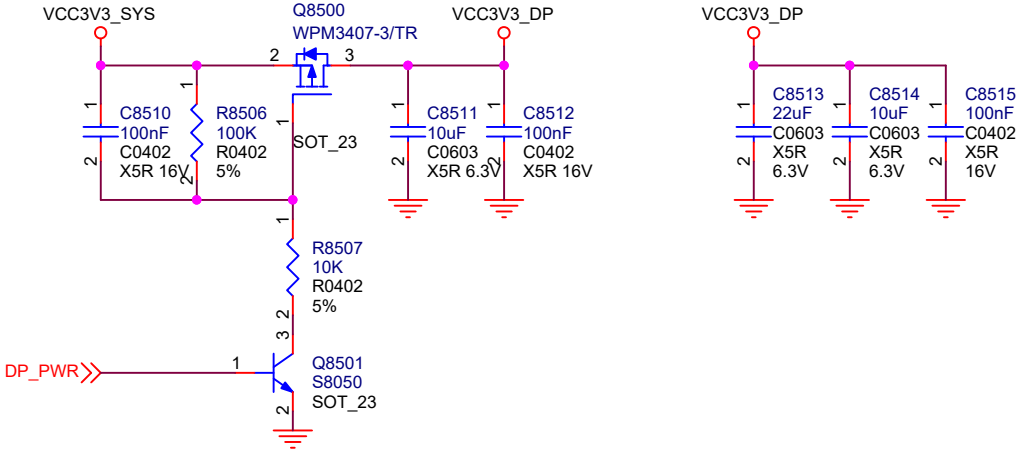


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399_BOX_REF
File:	84.PCIe Slot-x4 (option)
Date:	Tuesday, August 21, 2018
Rev:	V1.3
Designed by:	Linus
Sheet:	40 of 45

DP Output

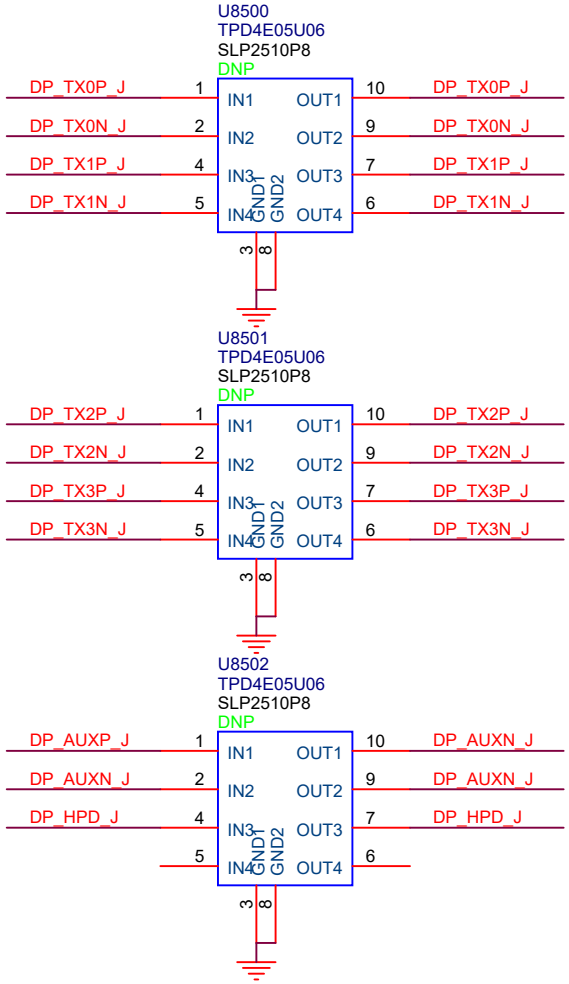


Power



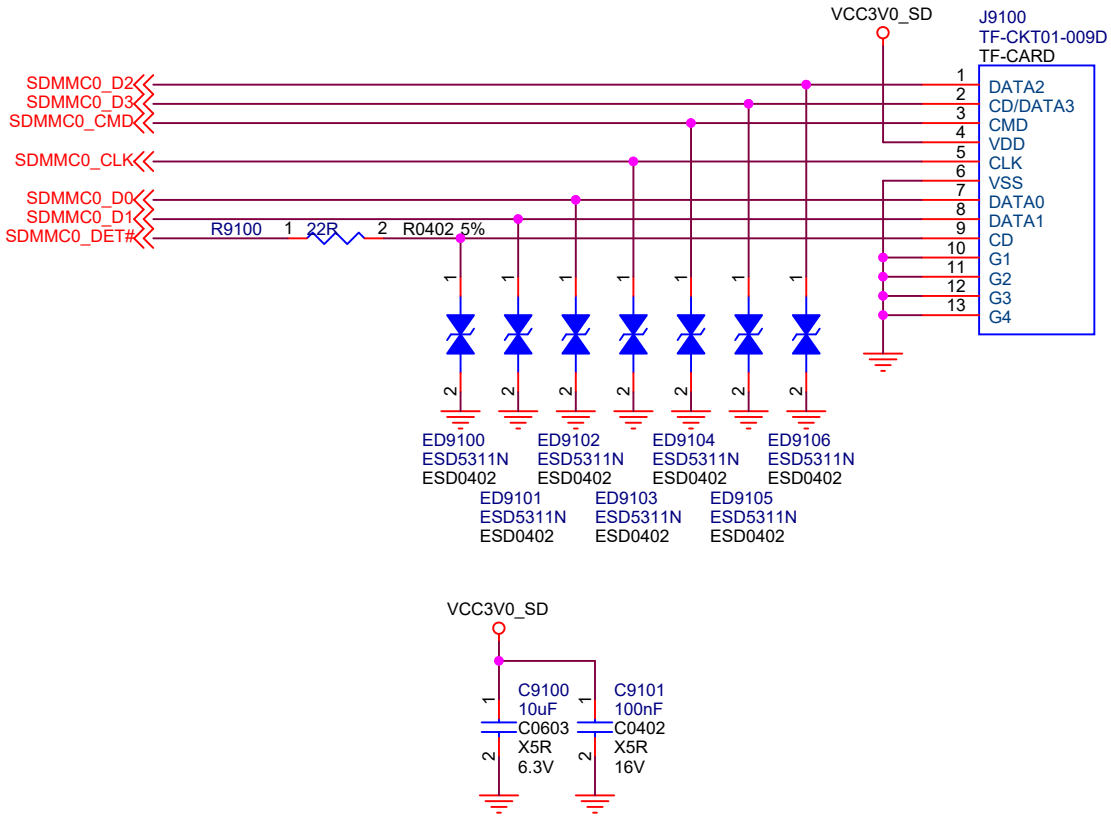
ESD

Note:All the ESD components should be placed close to the port and Cj<=0.4pF

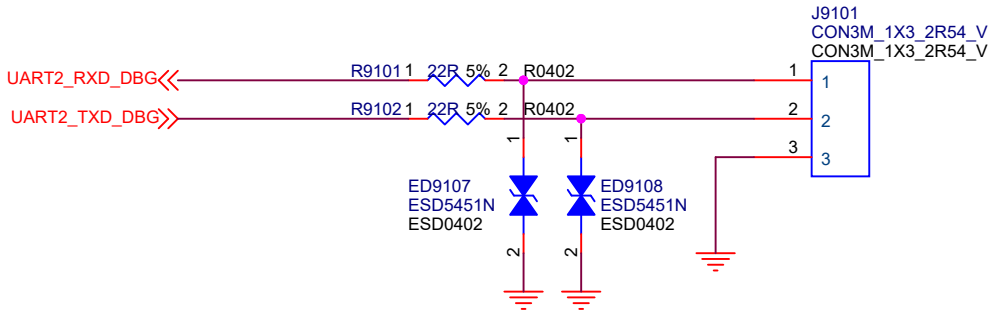


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	85.DP Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	41 of 45

TF CARD

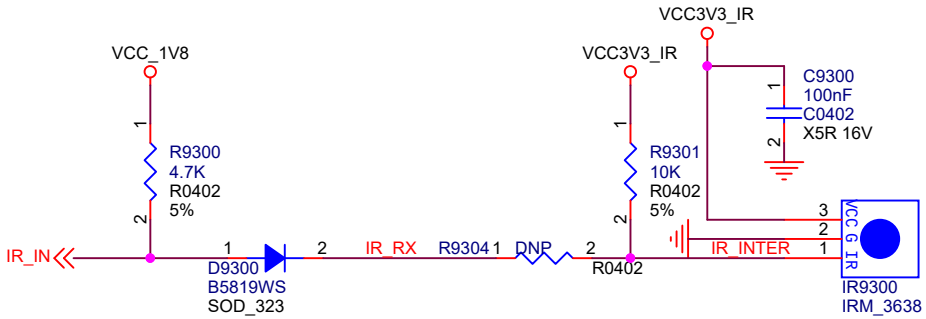


UART for debug



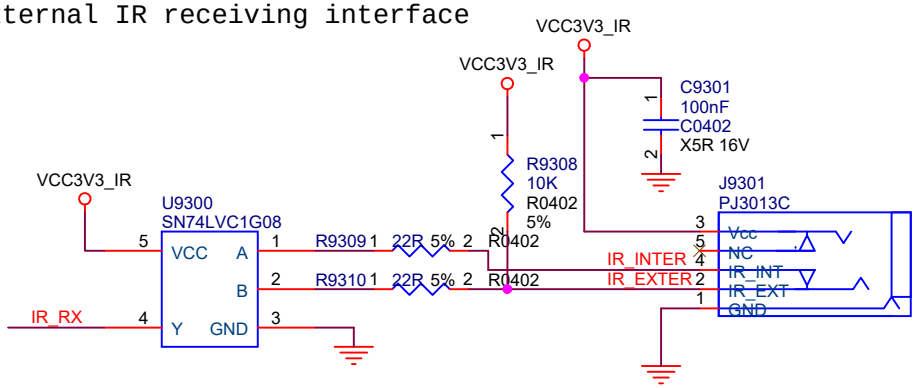
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	91.TF Card/UART		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	42 of 45

IR Receiver

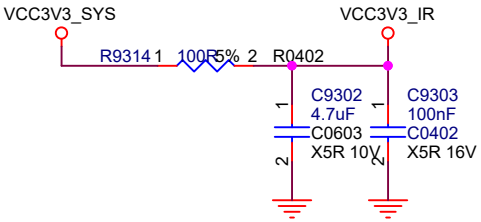


Option

External IR receiving interface

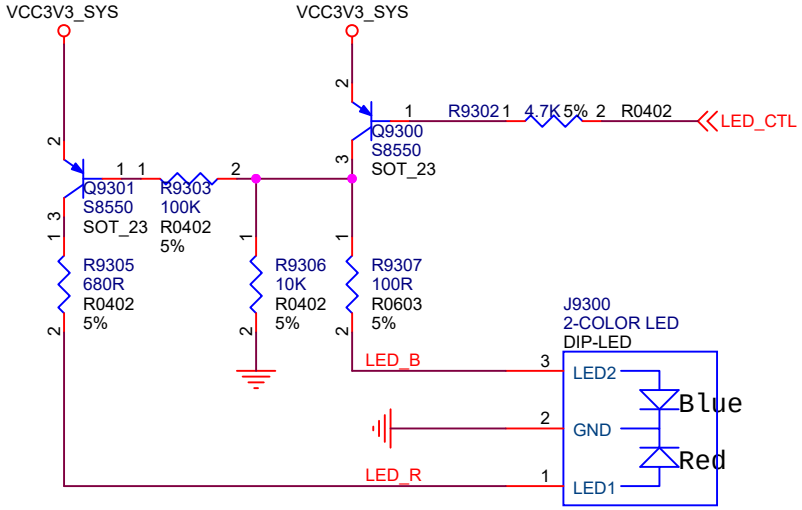


IR Power



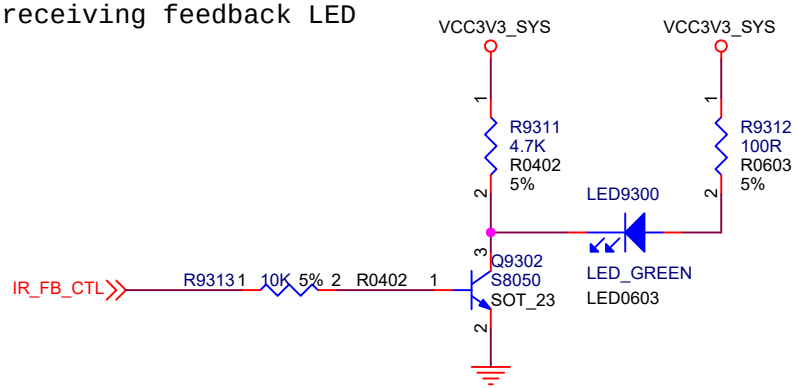
LED

Note:
Blue LED shows work states,
Red LED shows shutdown states



Option

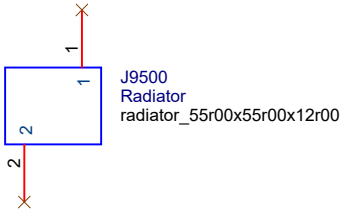
IR receiving feedback LED

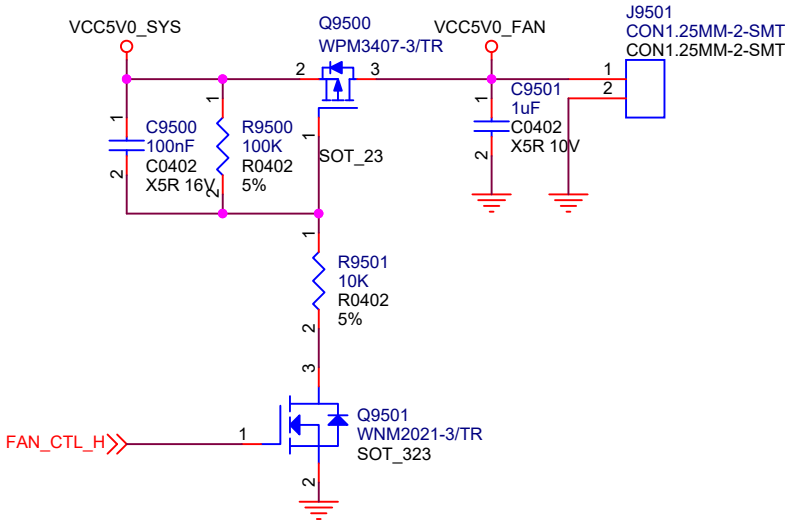


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	93.IR Receiver/LED Controller		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	43 of 45

HEATSINK/FAN(option)

Note:Power for FAN,It can be deleted if no need.

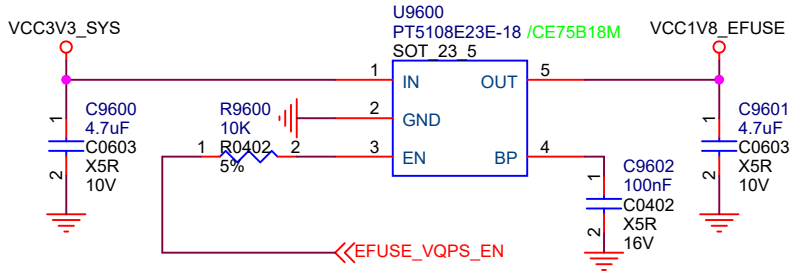




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	95.HEATSINK/FAN (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	44 of 45

eFUSE(option)

Note:Power for eFUSE Program,it is recommended to
reserve on the tooling.It can be deleted if no need.



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_BOX_REF		
File:	96.eFUSE (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	45 of 45