


Reference Schematic For RK3399

RK3399_BOX_REF_V1.3
20180821

 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	00.Cover Page		
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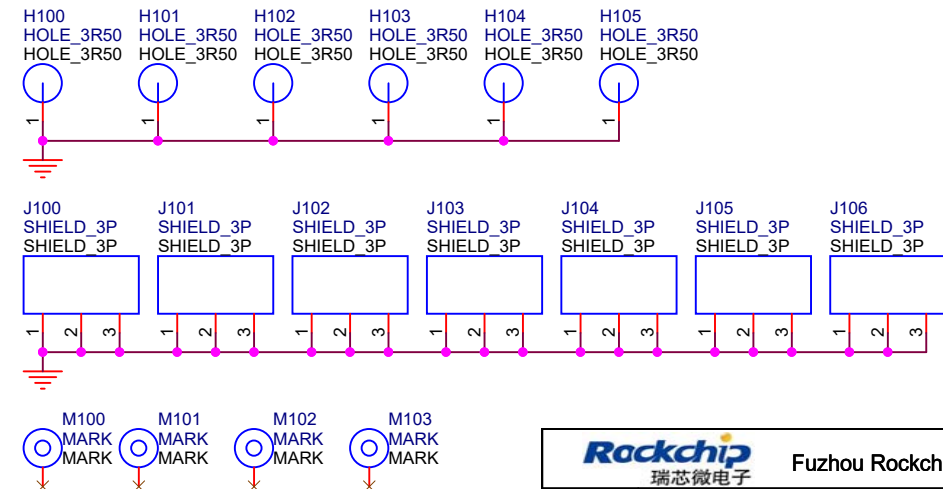
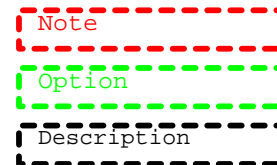
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Page44	---95.HEATSINK/FAN(option)
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6 LAYERS PCB STACK (e.g. PCB=1.0mm)

TOP	Prepreg 1080*1 (75um)	Silkscreen (25um) 1oz(35um)
GND1	Prepreg 2116*1 (115um)	Hoz(18um)
POWER	Adjust Core (465um)	Hoz(18um)
SIGNAL	Prepreg 2116*1 (115um)	Hoz(18um)
GND2	Prepreg 1080*1 (75um)	Hoz(18um)
BOTTOM		1oz(35um) Silkscreen (25um)

Note:

1: If the Value or option of the component properties is DNP, indicating do not mounted

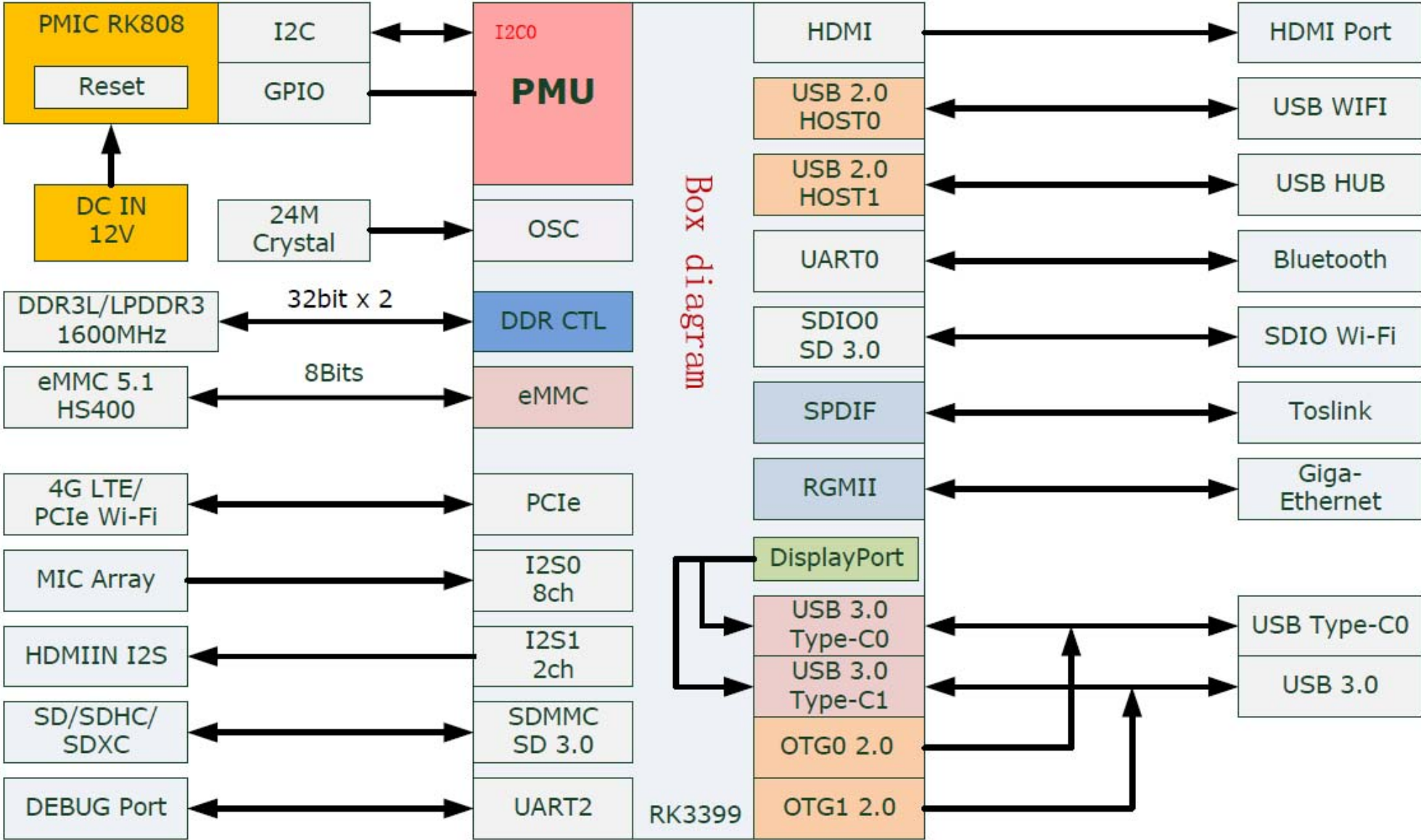


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Revision History


Version	Date	Author	Change Note	Approved
V1.0	2017.01.12	Linus.Lin	First edition	
V1.1	2017.05.12	Linus.Lin	Please refer to the document of 《RK3399_BOX_REF_V11_20170512 Modify Notes》	
V1.2	2017.12.18	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_v12_20171218.xlsx》	
V1.3	2018.08.21	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_v13_20180821.xlsx》	

Block Diagram



I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808-D	0x1b	PMIC	100kHz,400KHz
					Silergy SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					Silergy SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8	Toshiba TC358749XBG		HDMI Transmit	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	RESERVE					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_TYPEC I2C_SCL_TYPEC	VCC_1V8	Fairchild FUSB302B ETEK ET302Y	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					




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Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuiol_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLD03
Part E	PMUIO2	pmul830_gpiolabcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLD03
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLD06 RK808-D VLD08
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCCIO_SD	RK808-D VLD04



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Project:

RK3399_BOX_REF

File:

05.Power Domain Map

Date:

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Designed by:

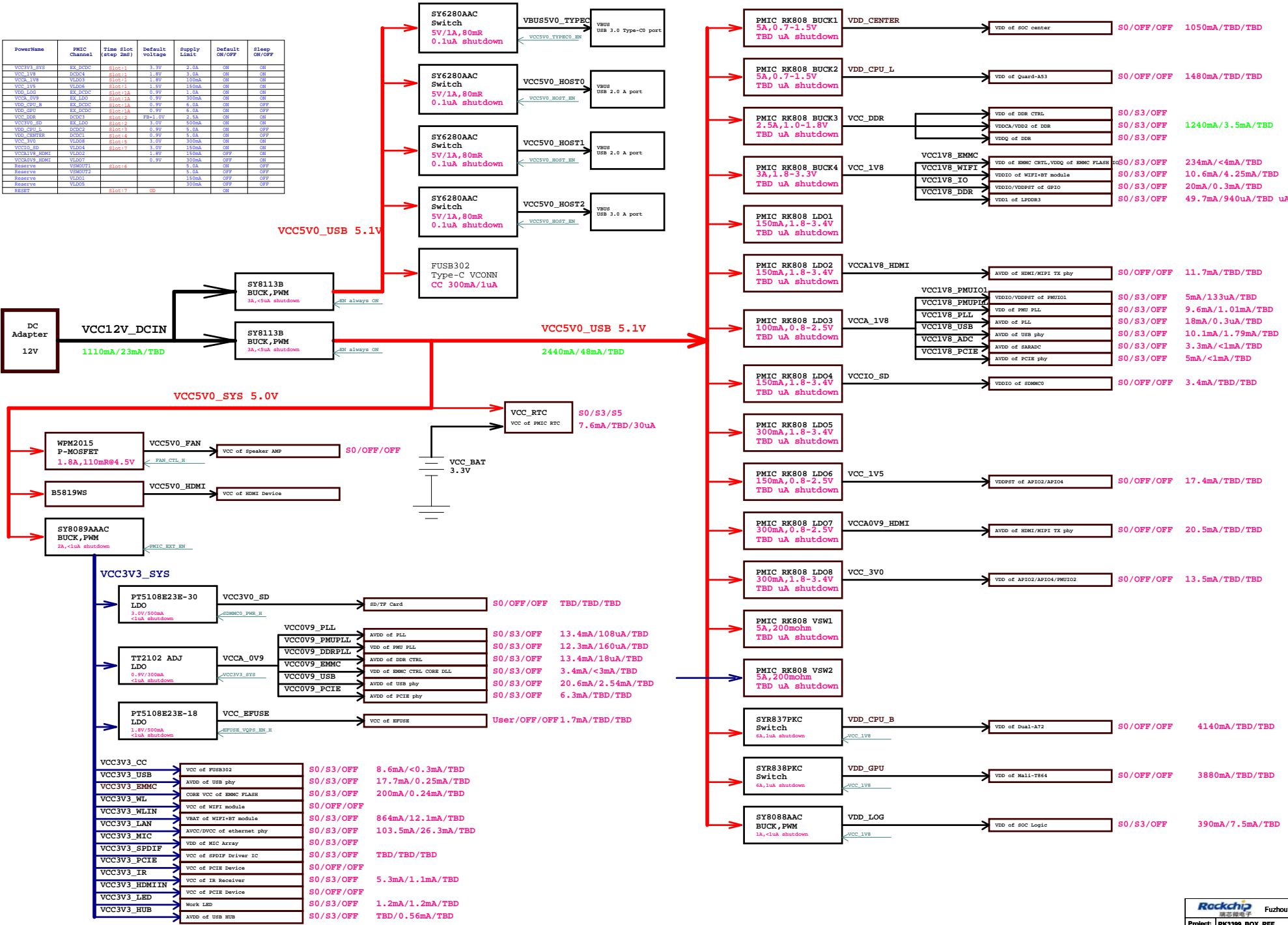
Linus

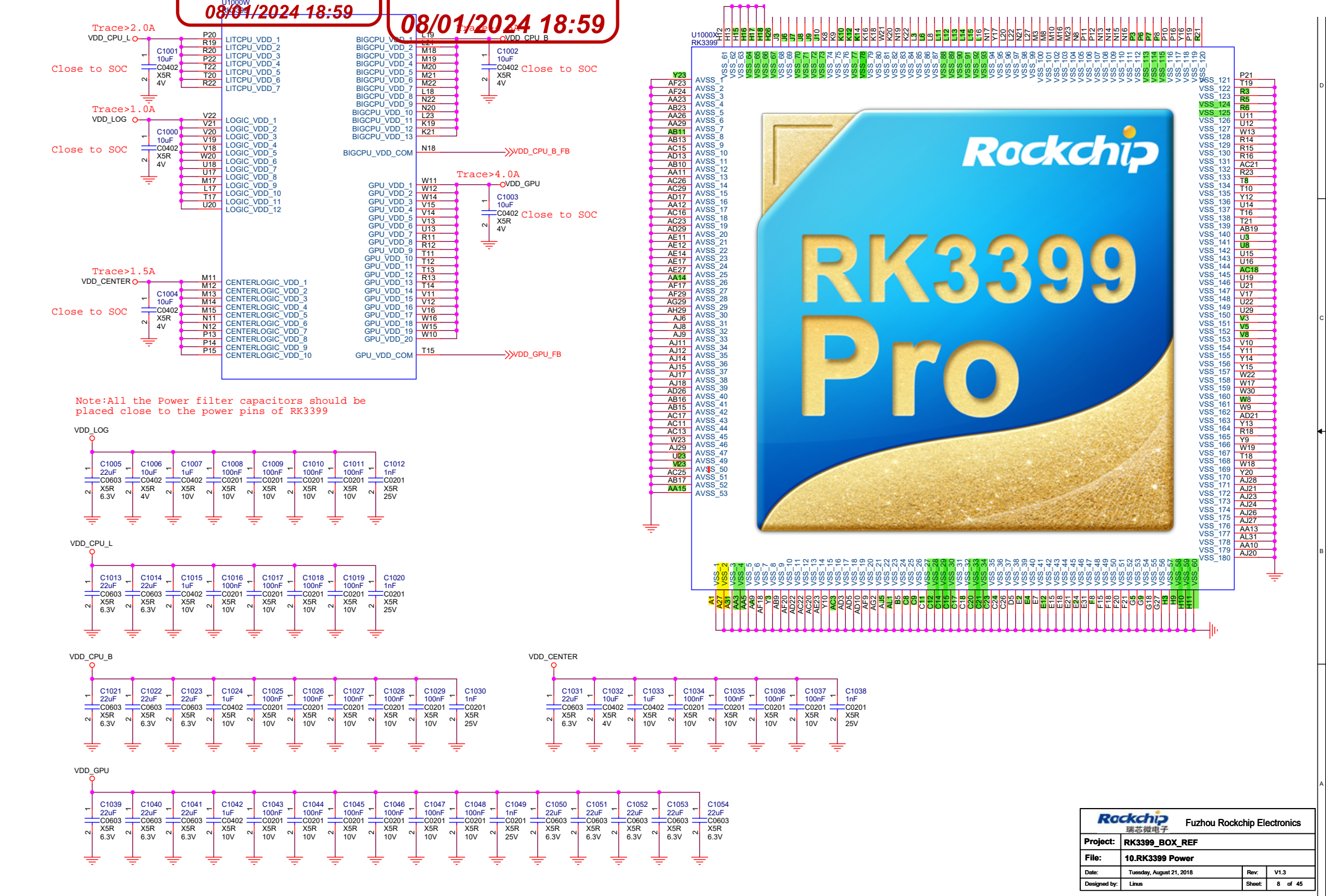
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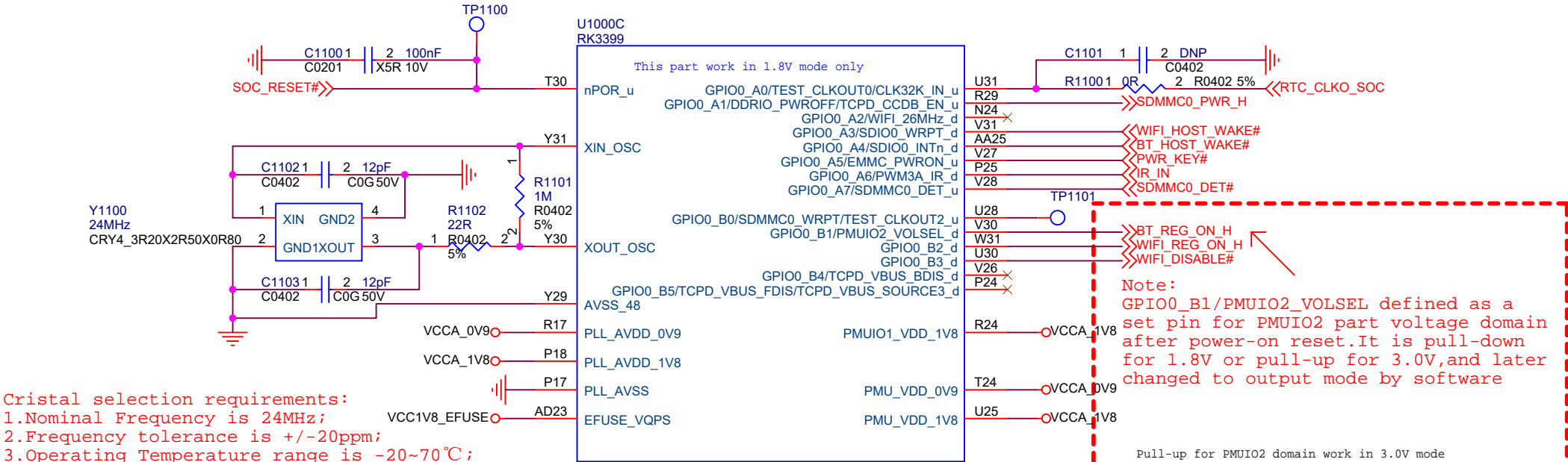
RK808-D Power Diagram and Sequence

PowerName	CHC Channel	Time Slot (sec 2ms)	Default Voltage	Supply Limit	Default On/OFF	Sleep On/OFF
VCCP11_500	BA_220C2	Slot1-1	1.2V	2.0A	ON	ON
VCCP12_500	BA_220C2	Slot1-1	1.8V	2.0A	ON	ON
VCCP13_500	BA_220C2	Slot1-1	1.5V	100mA	ON	ON
VCC_15V	VLAD05	Slot1-1	1.5V	150mA	ON	ON
VCCP14_500	BA_220C2	Slot1-1	0.9V	2.0A	ON	ON
VCCP15_500	BA_1450	Slot1-1A	0.8V	300mA	ON	ON
VCCP16_500	BA_1450	Slot1-1A	0.9V	6.0A	ON	ON
VCC_PSP	BA_220C2	Slot1-1A	0.8V	2.0A	ON	OFF
VCCP17_500	BA_220C2	Slot1-1	1.8V	2.0A	ON	ON
VCCP18_500	BA_1450	Slot1-2	1.0V	500mA	ON	ON
VCC_PSP2	CD002	Slot1-3	0.8V	5.0A	ON	OFF
VCCP19_500	BA_220C2	Slot1-1	1.5V	2.0A	ON	ON
VCC_3V3	VLAD05	Slot1-5	3.0V	500mA	ON	ON
VCCP20_500	BA_220C2	Slot1-1	0.9V	2.0A	ON	ON
VCCP21_500	VLAD02	Slot1-7	0.9V	150mA	OFF	ON
VCCP22_500	BA_220C2	Slot1-1	1.5V	300mA	ON	ON
Reserve1	TRM0017	Slot1-6	1.8V	1.0A	ON	OFF
Reserve2	TRM0017	Slot1-6	0.9V	5.0A	ON	OFF
Reserve3	VLAD01		1.5V	500mA	OFF	OFF
Reserve4	VLAD05		3.0V	150mA	OFF	OFF
Reserve5		Slot1-7	OD	300mA	OFF	OFF



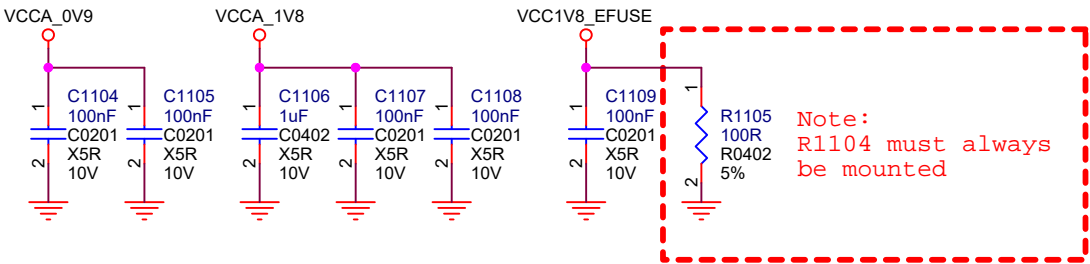
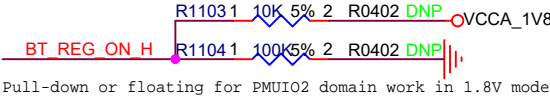


RK3399_C




- Cristal selection requirements:
- 1.Nominal Frequency is 24MHz;
 - 2.Frequency tolerance is +/-20ppm;
 - 3.Operating Temperature range is -20~70℃;
 - 4.Equivalent resistance < 60ohm;

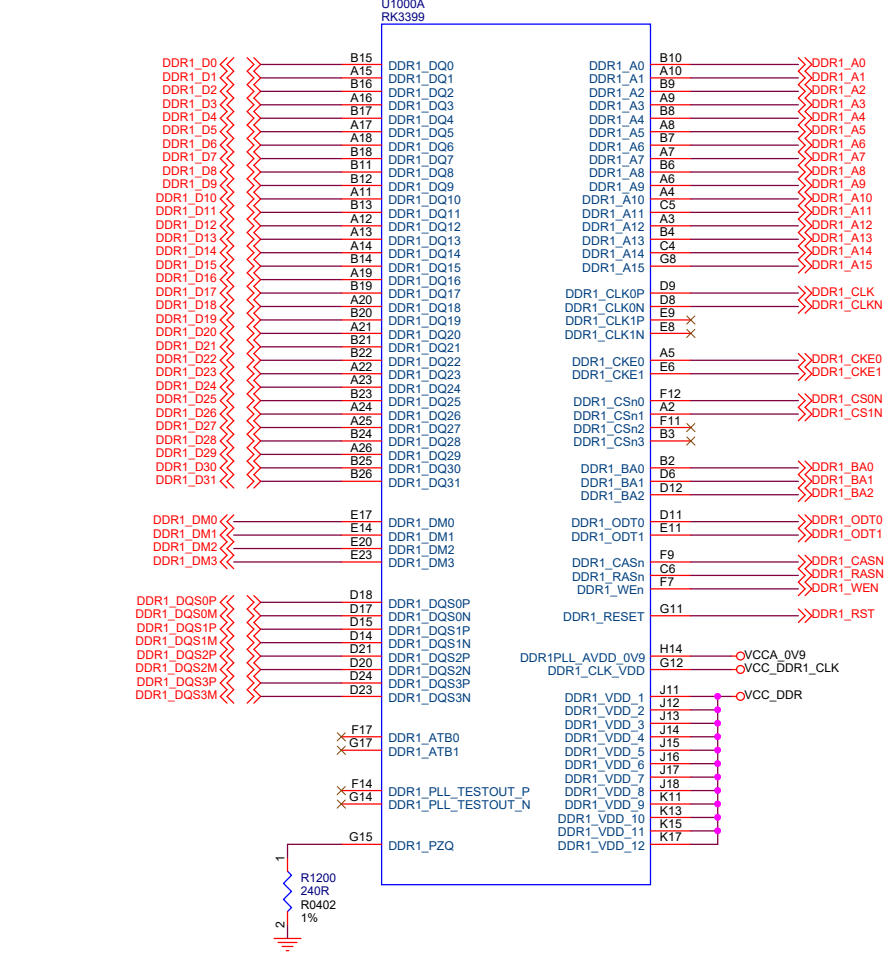
Pull-up for PMUIO2 domain work in 3.0V mode



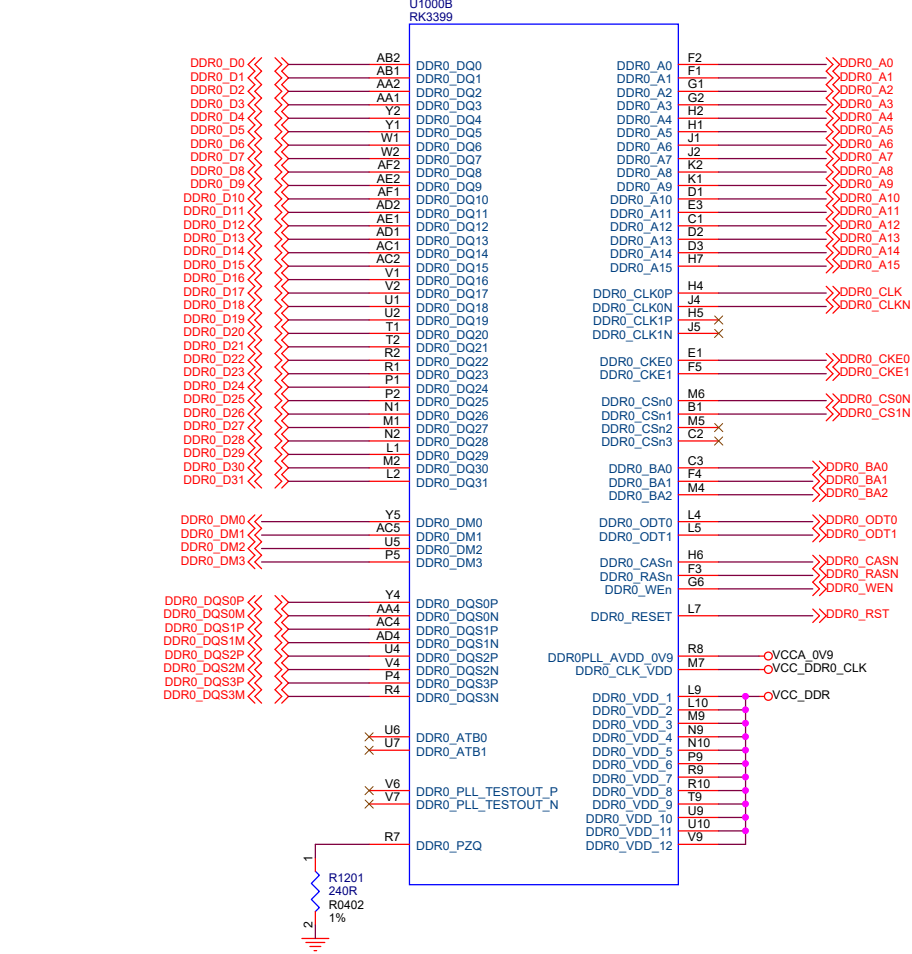
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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RK3399_A

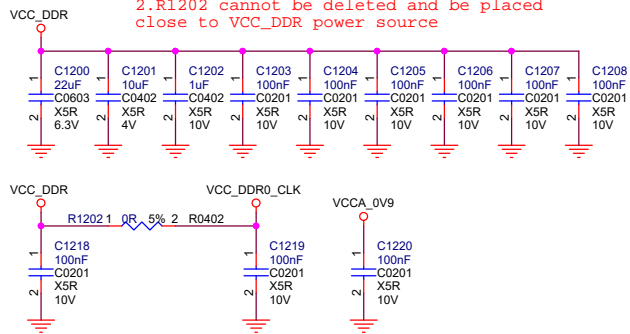


RK3399_B



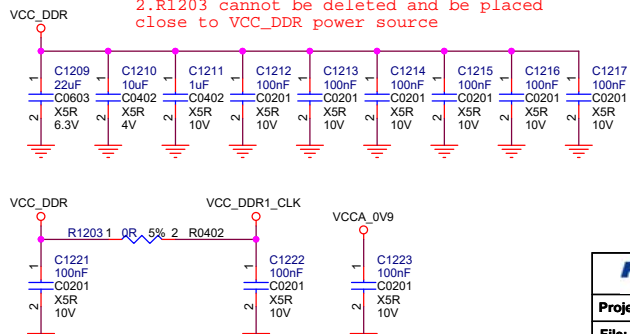
DDR FILTER


Note:
1.All the Power filter capacitors should be placed close to the power pins of RK3399
2.R1202 cannot be deleted and be placed close to VCC_DDR power source



DDR FILTER

Note:
1.All the Power filter capacitors should be placed close to the power pins of RK3399
2.R1203 cannot be deleted and be placed close to VCC_DDR power source

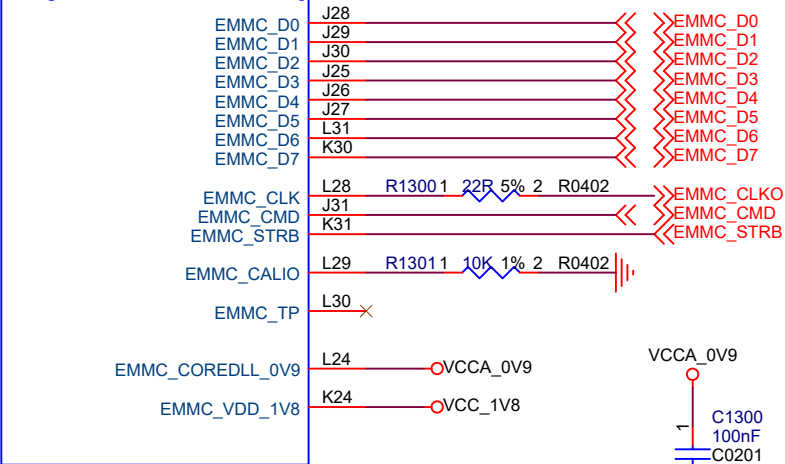


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RK3399_H

U1000H
RK3399

This part work in 1.8V mode only



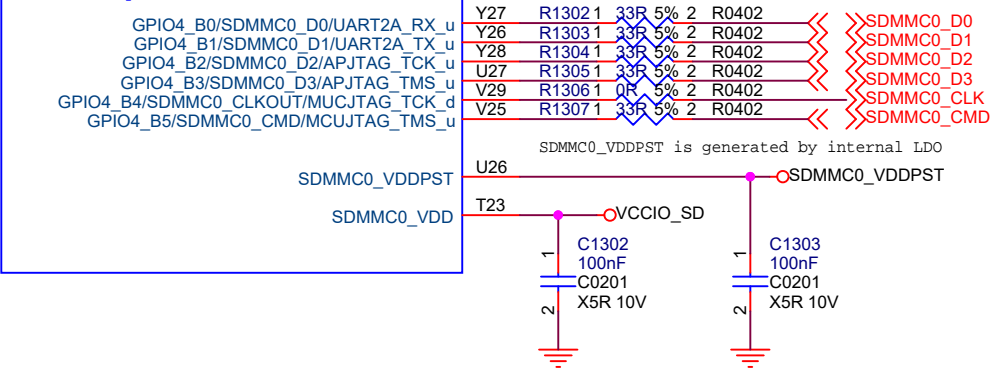
- EMMC design rules:
- 1.Data[0:3],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
 - 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
 - 3.Max trace length < 3.93inchs;
 - 4.Trace impedance 50ohm+/-10%;
 - 5.The distance between other signals follows the 3W rule;
 - 6.R1300 should be place close to RK3399;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_F


U1000F
RK3399

This part work in 1.8V/3.0V auto

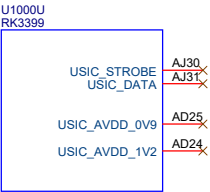


- SDMMC design rules:
- 1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
 - 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
 - 3.Max trace length < 3.93inchs;
 - 4.Trace impedance 50ohm+/-10%;
 - 5.The distance between other signals follows the 3W rule;

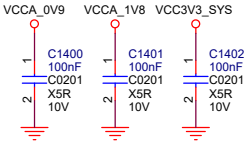
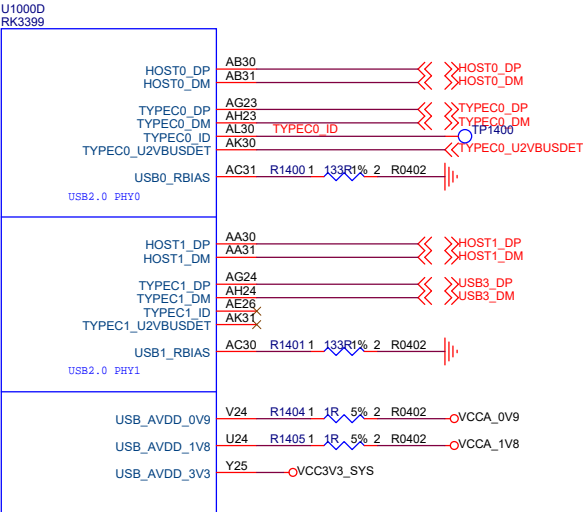
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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RK3399_U



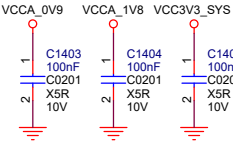
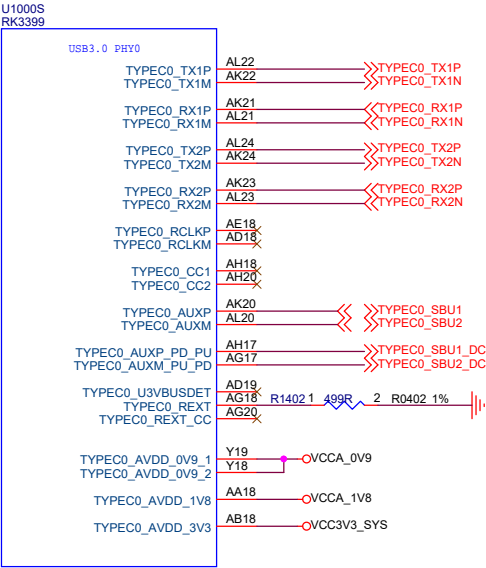
RK3399_D



Note: All the Power filter capacitors should be placed close to the power pins of RK3399

USB2.0 design rules:
1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

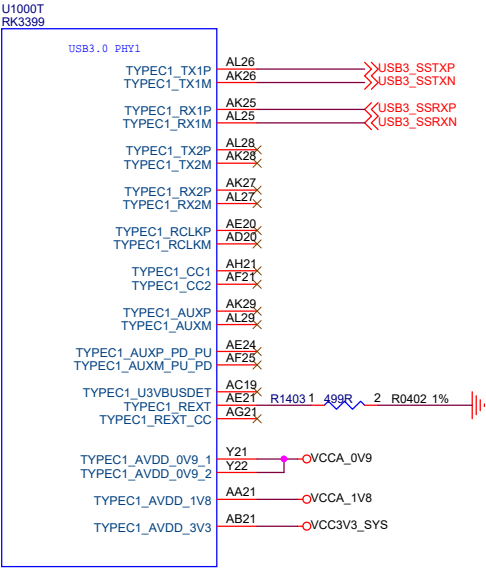
RK3399_S




Note: All the Power filter capacitors should be placed close to the power pins of RK3399

USB3.0 design rules:
1. Max intra-pair skew < 4ps;
2. Max length skew between TX and RX < 1.6ns;
3. Max trace length < 6inchs;
4. Max allowed via < 4;
5. Trace impedance 90ohm+/-10%;
6. The distance between other signals follows the 3W rule;

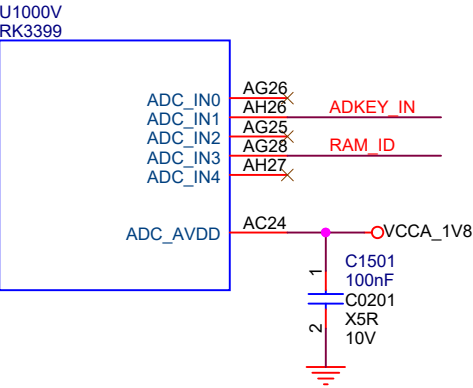
RK3399_T



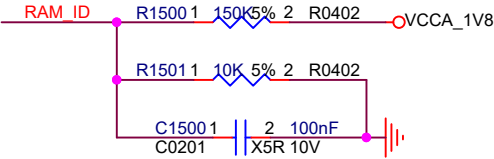
DP design rules:
1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

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RK3399_V

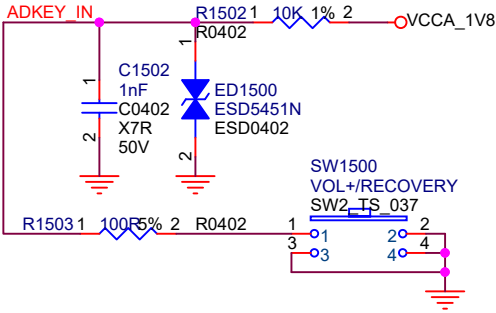


Note:All the Power filter capacitors should be placed close to the power pins of RK3399



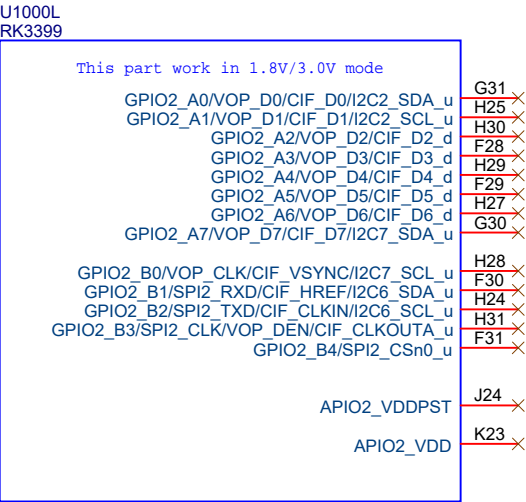
	RAM ID	R1500 PU	R1501 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K

KEY

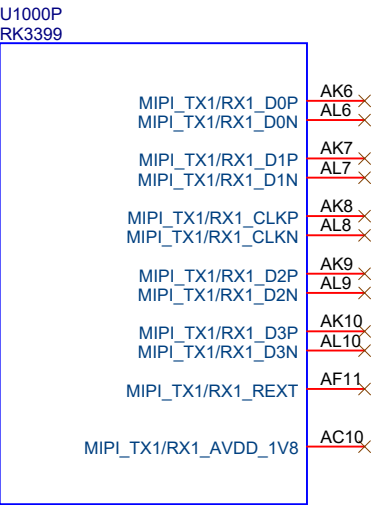


Note:
1.If ADKEY_IN=0V at power-on reset,
then system will enter into Recovery mode.
2.R1503,SW1500,ED1500 can be deleted if no need at Mass Production

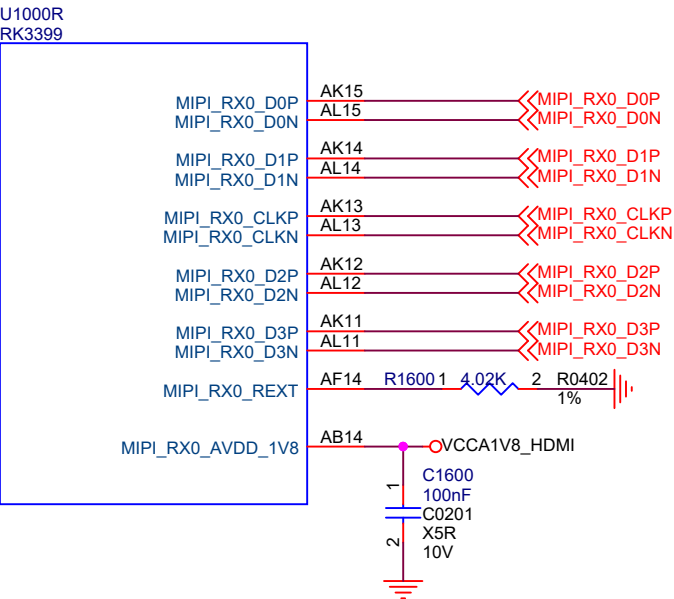
RK3399_L



RK3399_P




RK3399_R



MIPI design rules:

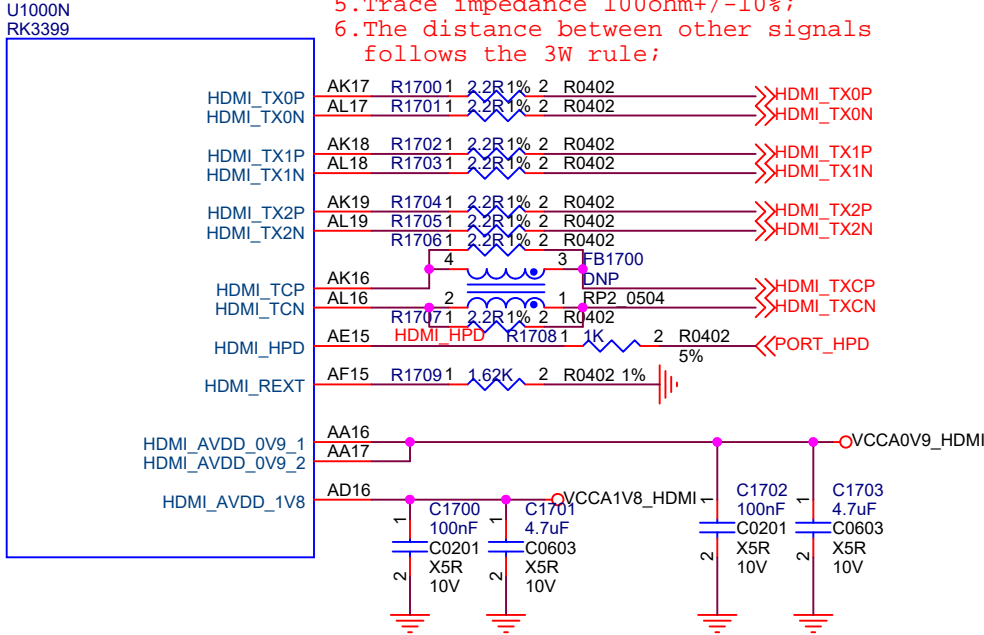
- 1.Max intra-pair skew < 4ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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File:	16.RK3399 DVP Interface		
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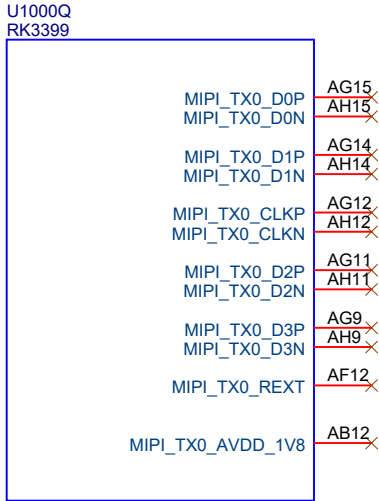
RK3399_N

HDMI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 80ps;
3.Max trace length < 9.8inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

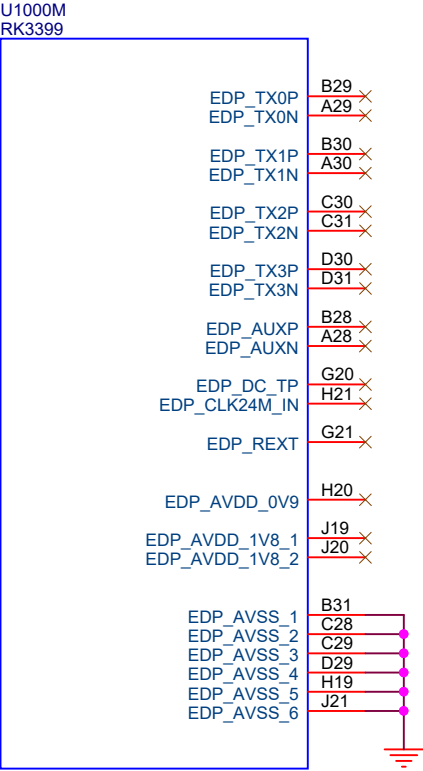


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_Q



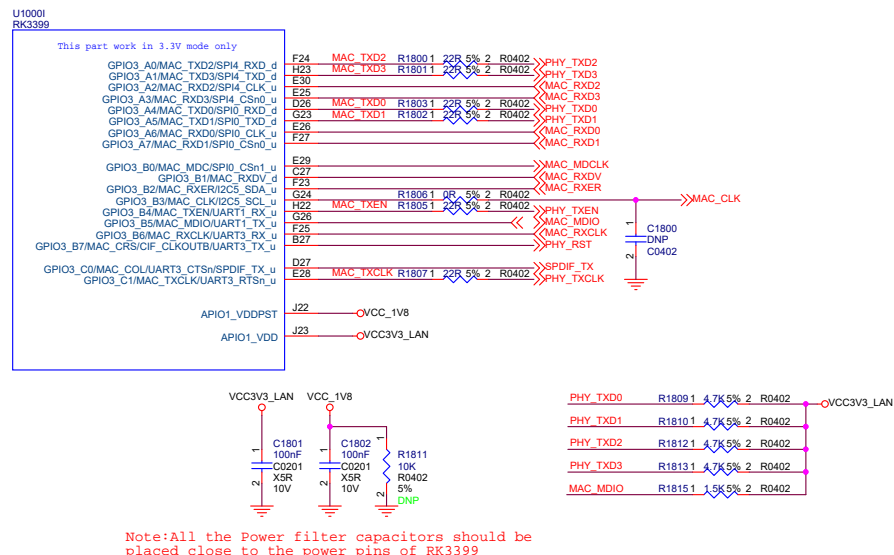
RK3399_M



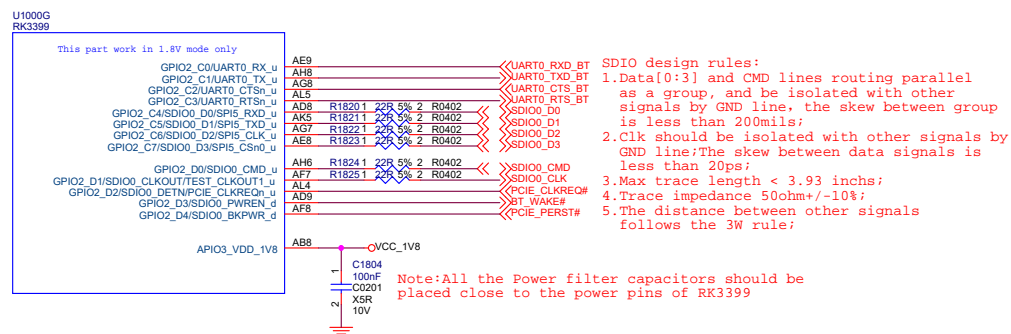
eDP design rules:
1.Max intra-pair skew <4 ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

<div><div><div>Rockchip</div><div>瑞芯微电子</div></div><div>Fuzhou Rockchip Electronics</div></div>			
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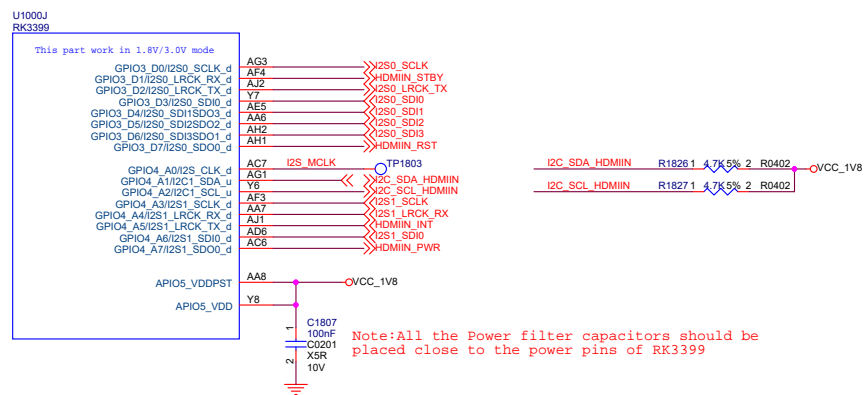
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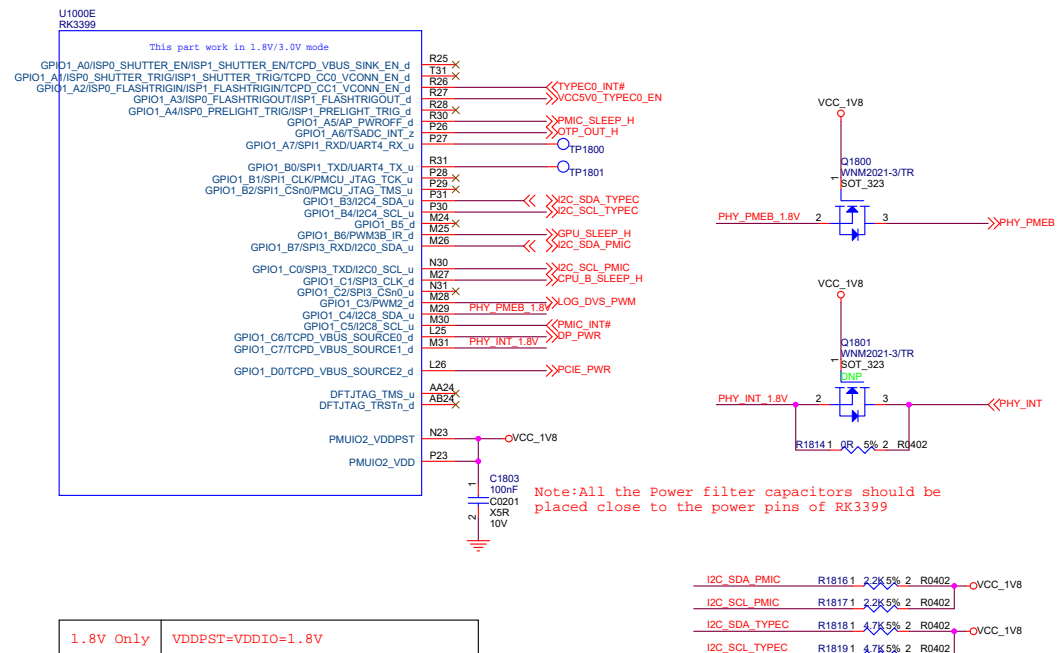
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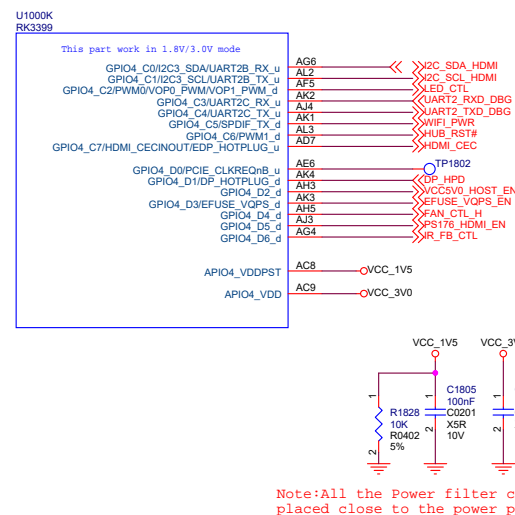
RK3399_J



RK3399_E

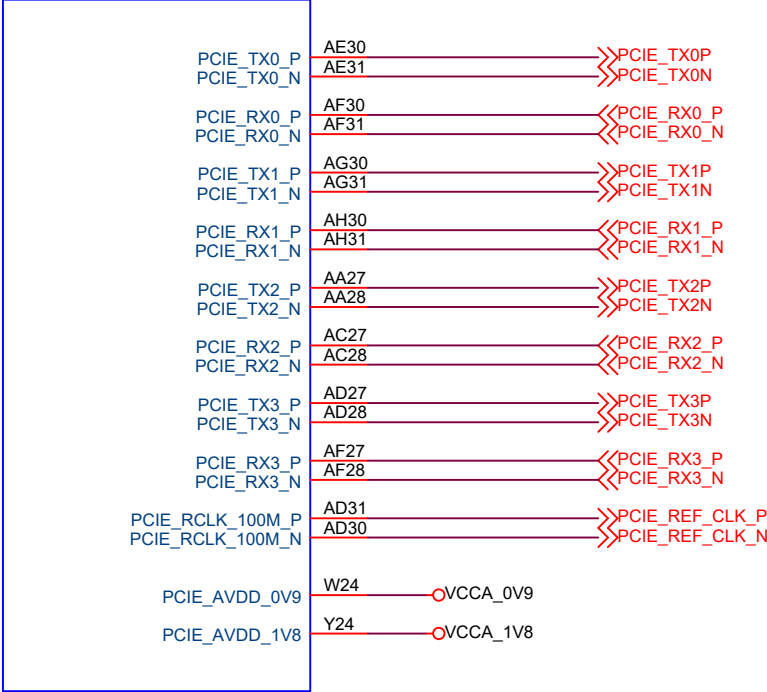


RK3399 K

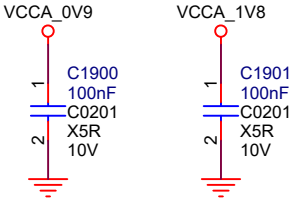


RK3399_O

U10000
RK3399



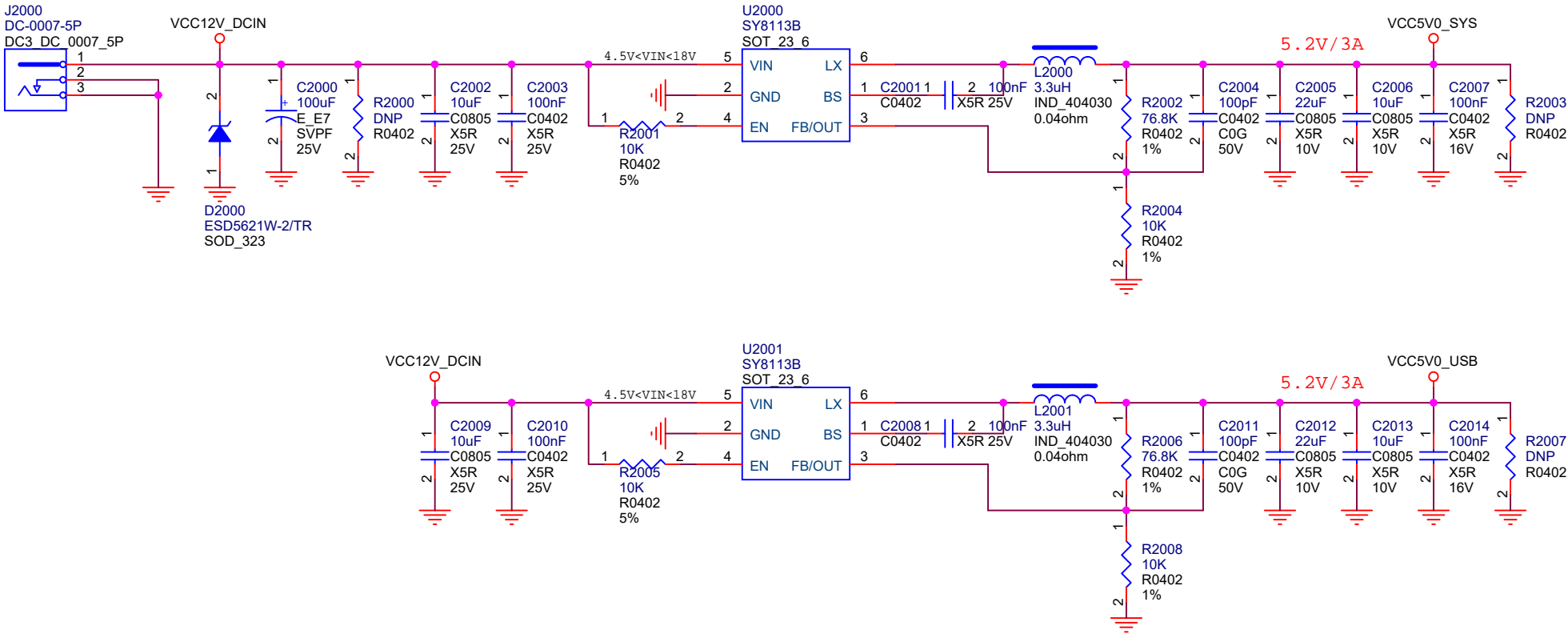
PCIE design rules:
1.Max intra-pair skew < 4ps;
2.Max inter-pair skew < 1.6ns;
3.Max trace length < 14inches;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

<div>Rockchip</div> <div>瑞芯微电子</div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	19.RK3399_PCIE		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	17 of 45

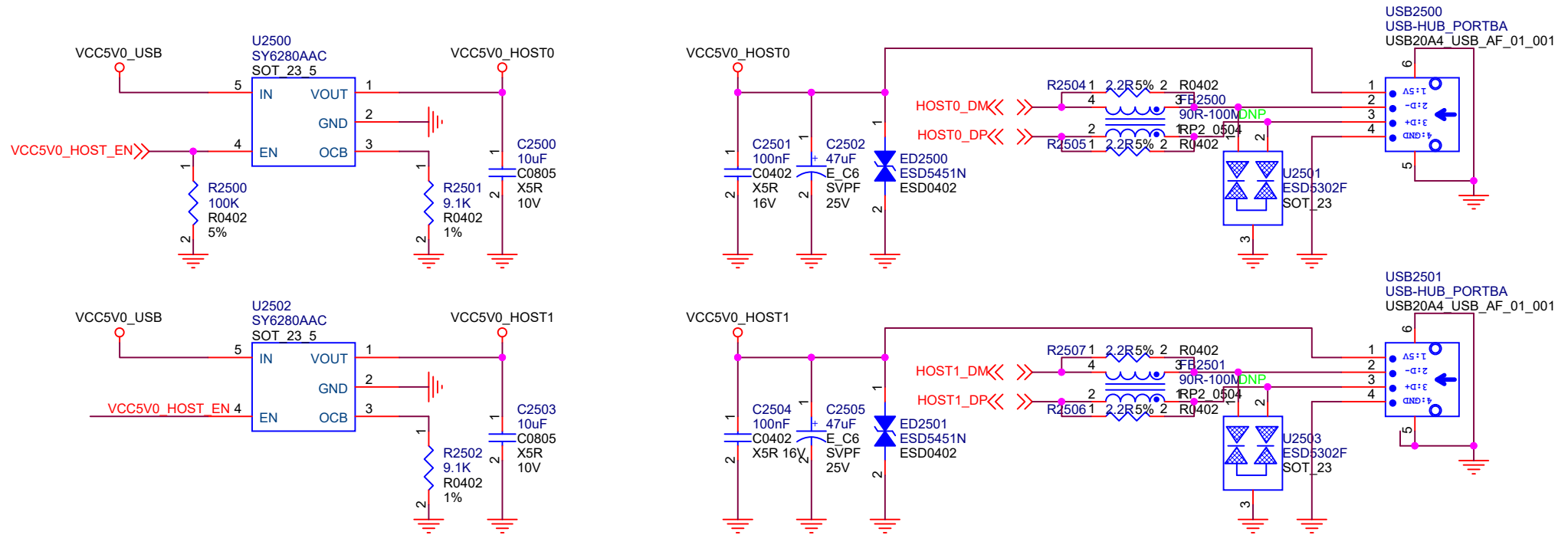
DC IN & SYSTEM Power



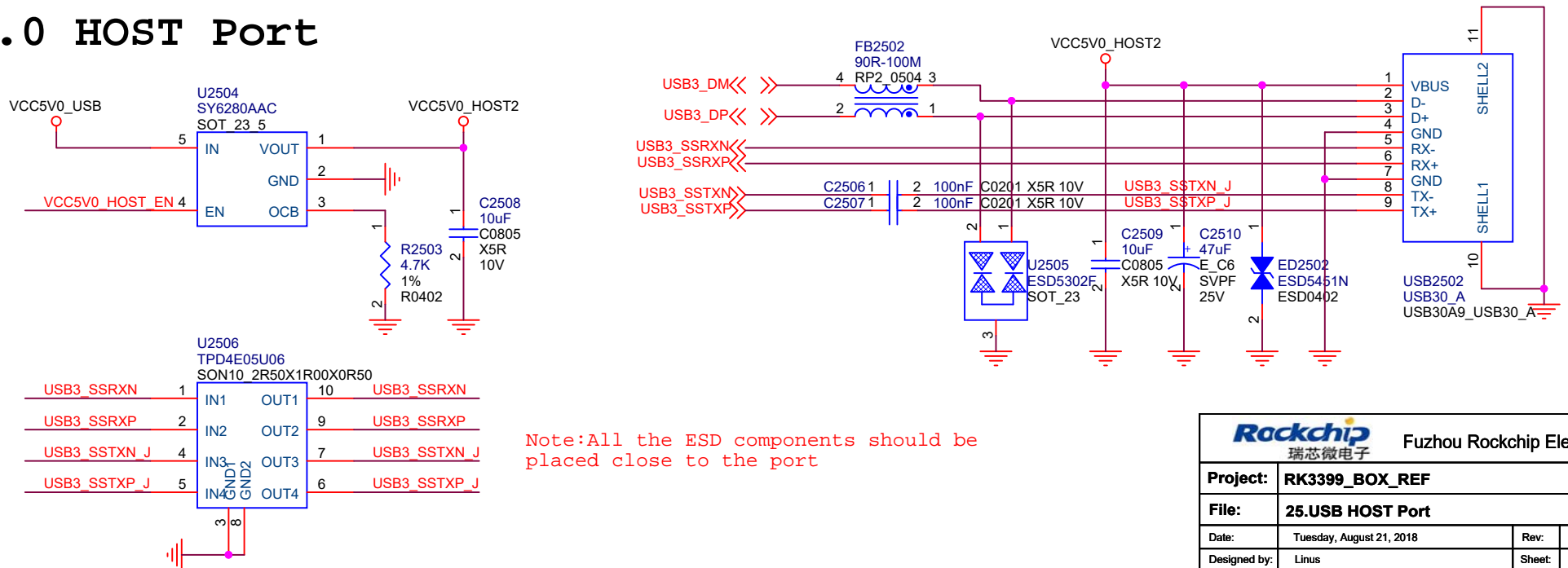
Note: If use USB3.0 HUB, U2001 must support over 3A current

<div><div>Rockchip</div><div>瑞芯微电子</div></div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	20.Power-DC IN		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	18 of 45

USB2.0 HOST Port

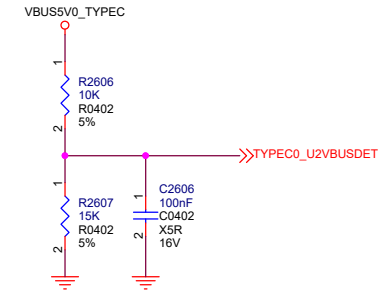


USB3.0 HOST Port



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	25.USB HOST Port		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	20 of 45

USB Detection



USB Type-C Power

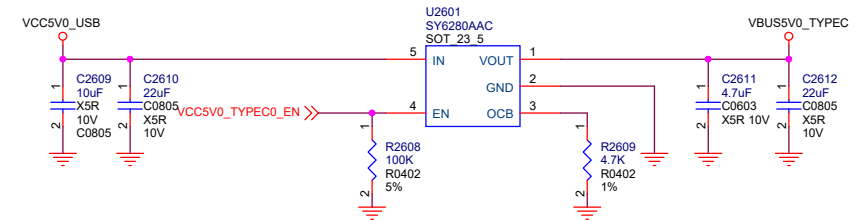


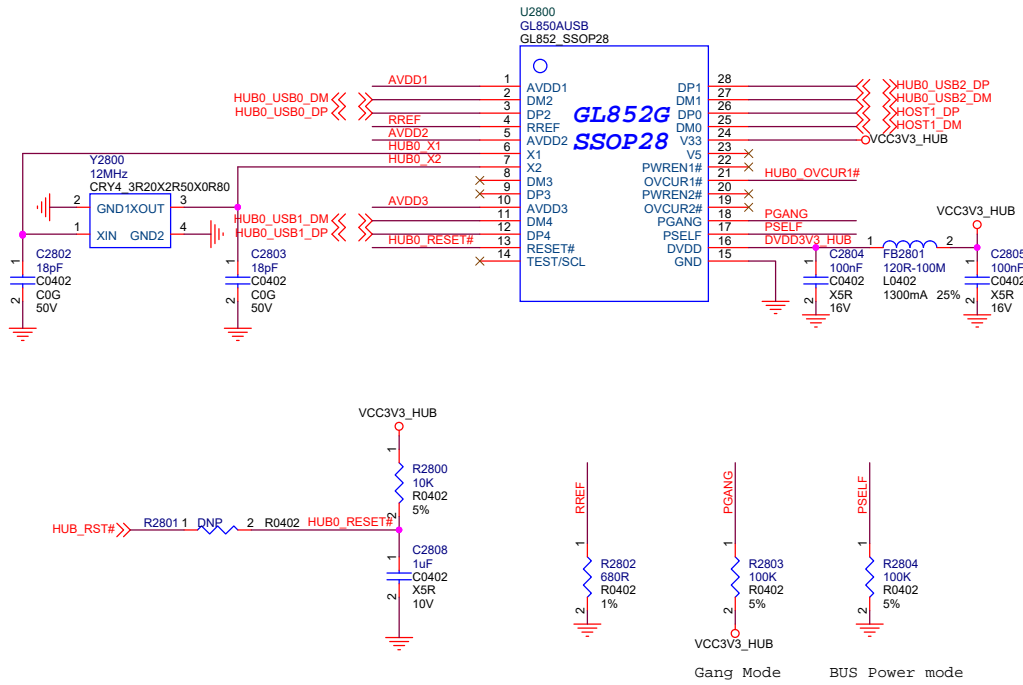
Diagram 1: U2604 ESD5302F SOT_23. Pin 1 is connected to TYPEC0_DM and TYPEC0_DP. Pin 2 is connected to ground. Pin 3 is connected to ground.

Diagram 2: U2605 ESD5302F SOT_23. Pin 1 is connected to TYPEC CC1 and TYPEC CC2. Pin 2 is connected to ground. Pin 3 is connected to ground.

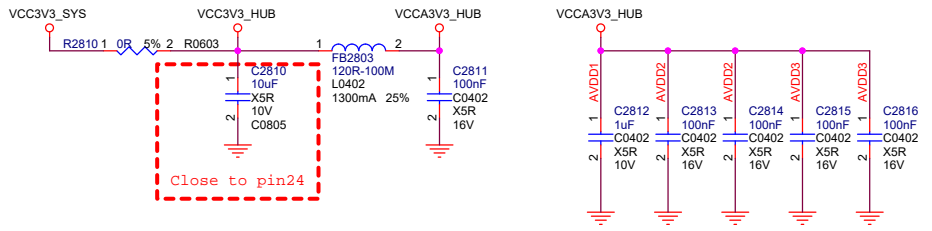
Diagram 3: U2606 ESD5302F SOT_23. Pin 1 is connected to TYPEC AUXP and TYPEC AUXM. Pin 2 is connected to ground. Pin 3 is connected to ground.

		Fuzhou Rockchip Electronics	
Project: RK3399_BOX_REF			
File: 26.USB Type-C Port			
Date:	Tuesday, August 21, 2016	Rev:	V1.3
Designed by:	Linus	Sheet:	21 of 45

USB2.0 HUB

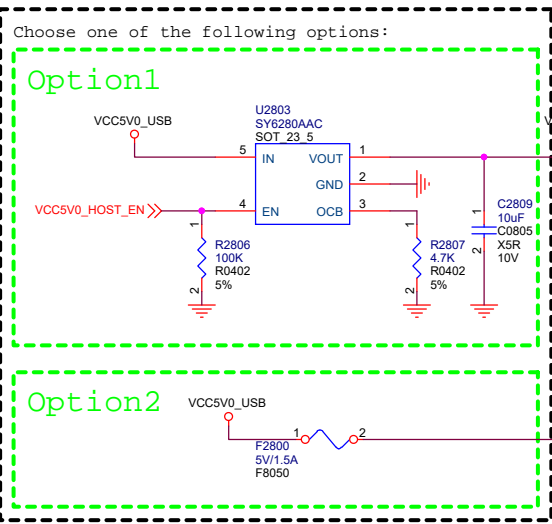
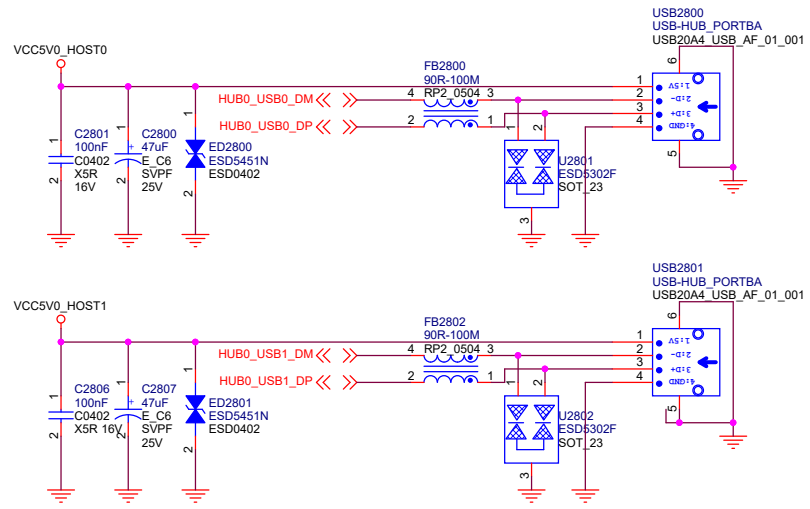


HUB Power

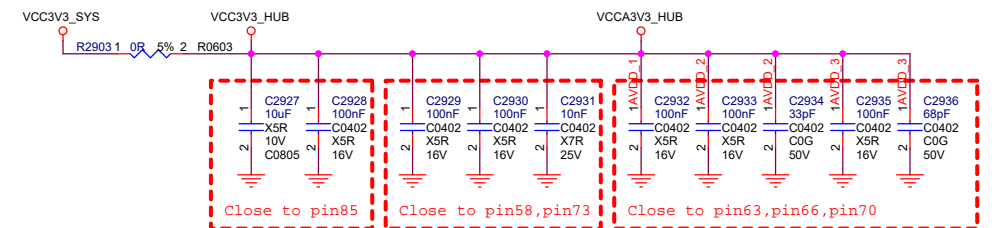
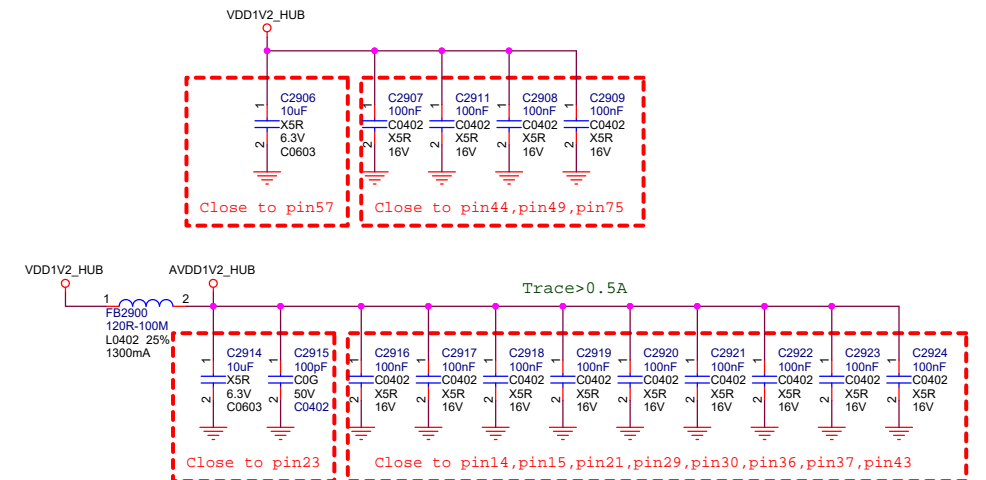
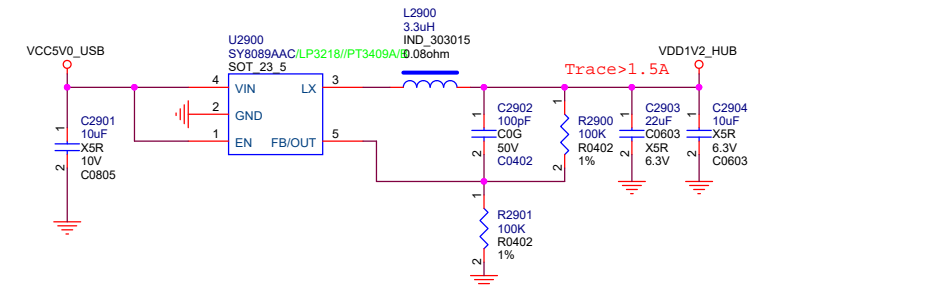
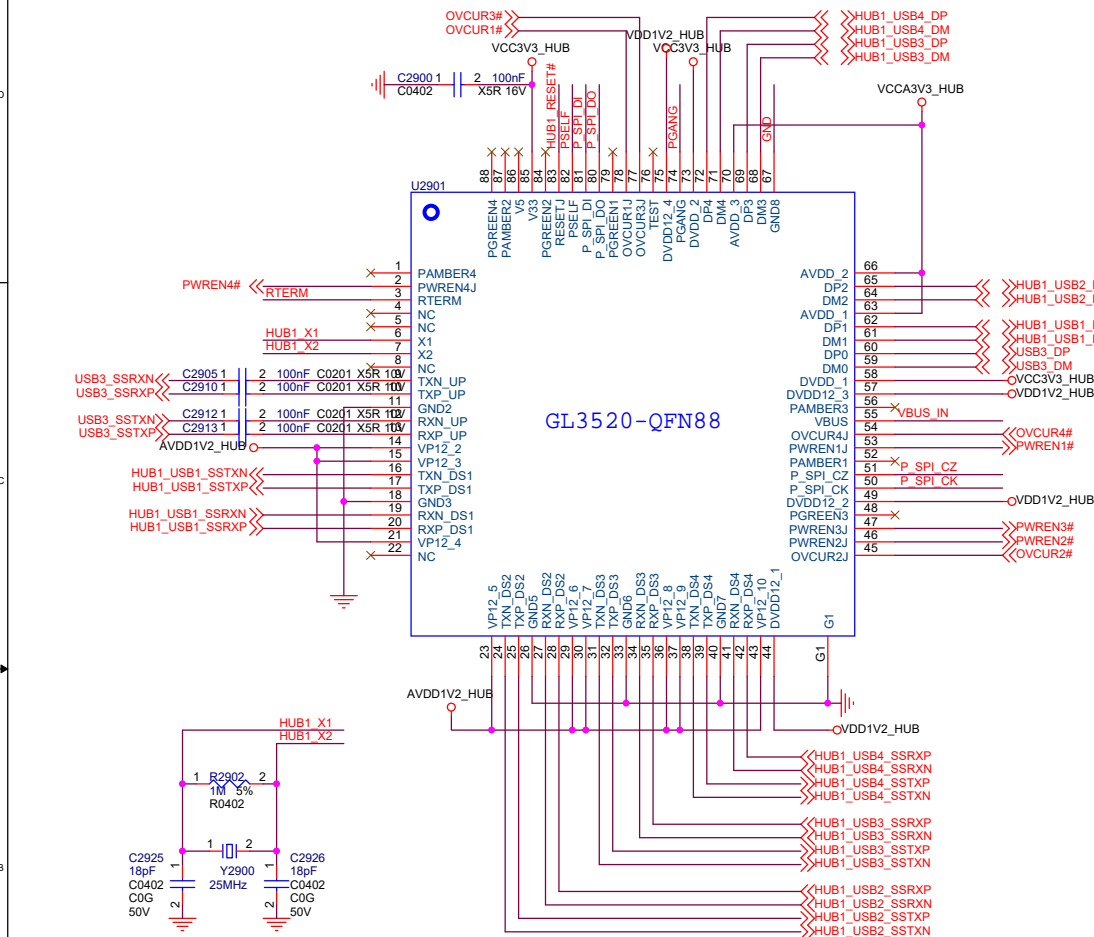


Note:All the Power filter capacitors should be placed close to the power pins of GL852G

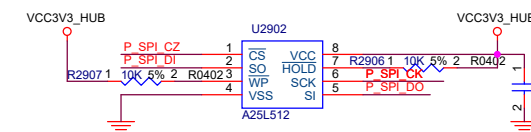
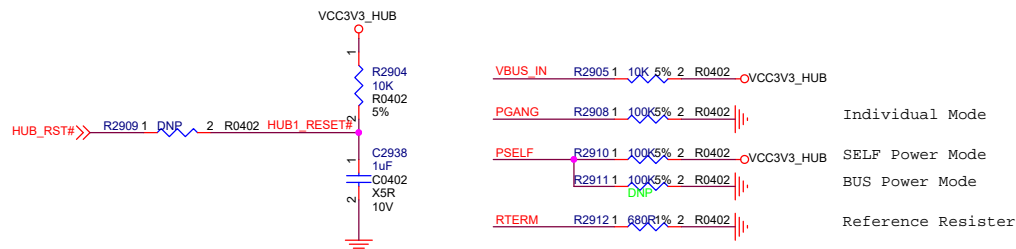
USB2.0 Port




HUB Power



SPI Flash



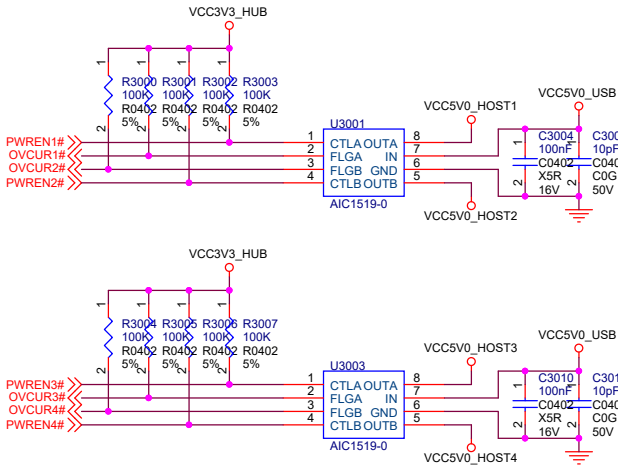
		Fuzhou Rockchip Electronics	
Project:		RK3399_BOX_REF	
File:		29.USB3.0 HUB-GL3523-1 (option)	
Date:		Tuesday, August 21, 2018	Rev: V1.3
Designed by:		Linus	Sheet: 24 of 45

Port Power

Choose one of the following options:

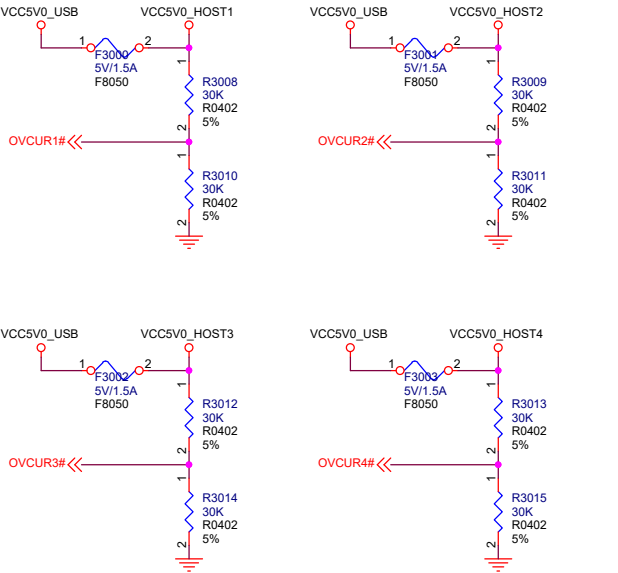
Option1

Power Switch CIRCUIT



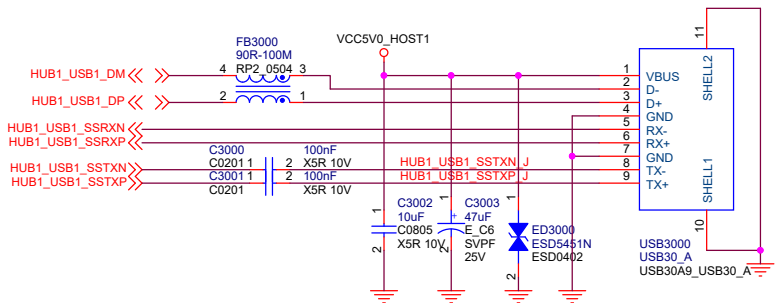
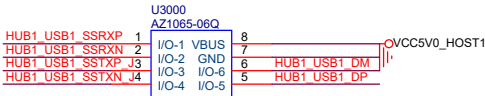
Option2

POLY-FUSE CIRCUIT

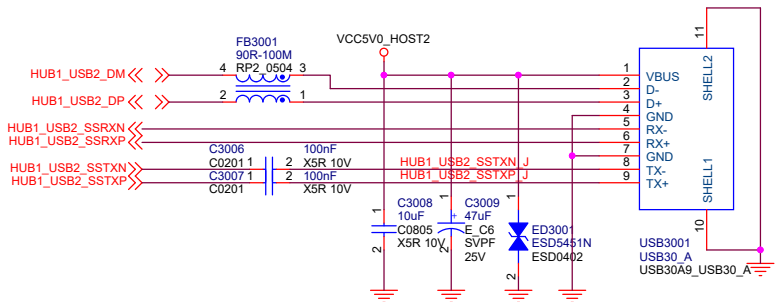
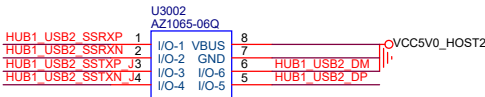


Note:OVCUR1#~4# Floating : Non-Removable (Compound device)

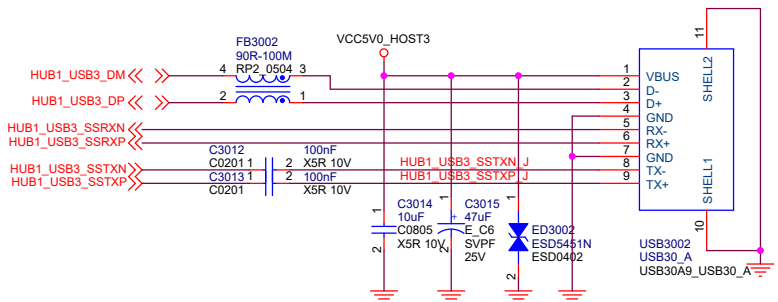
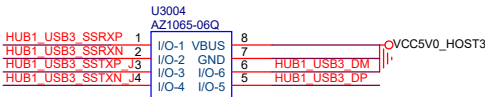
USB3.0 Port1



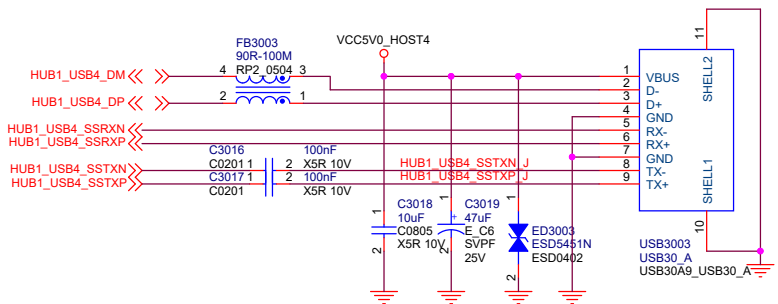
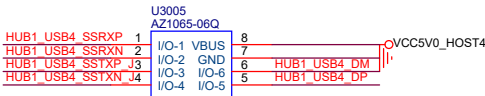
USB3.0 Port2



USB3.0 Port3

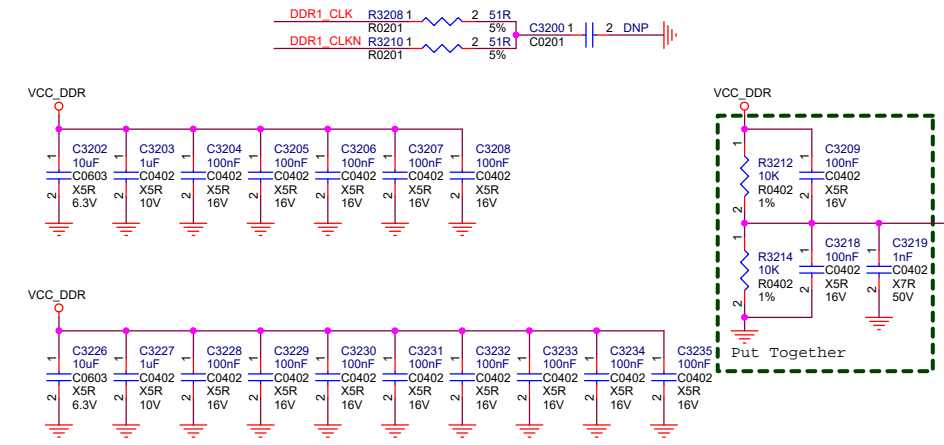
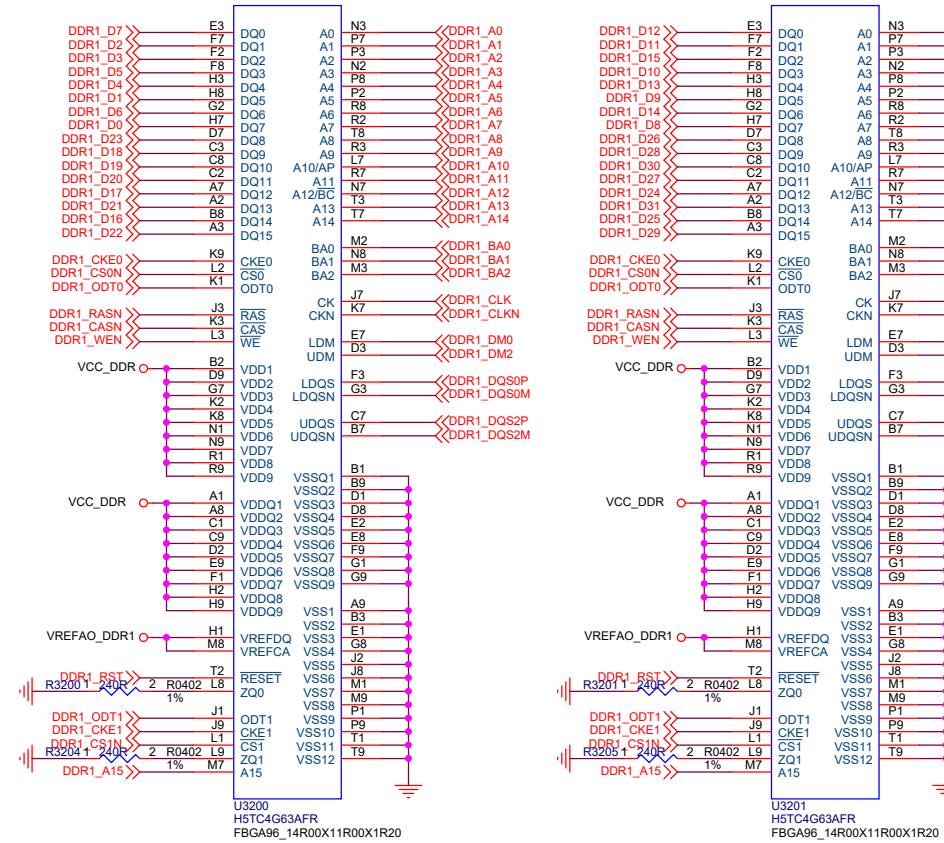


USB3.0 Port4

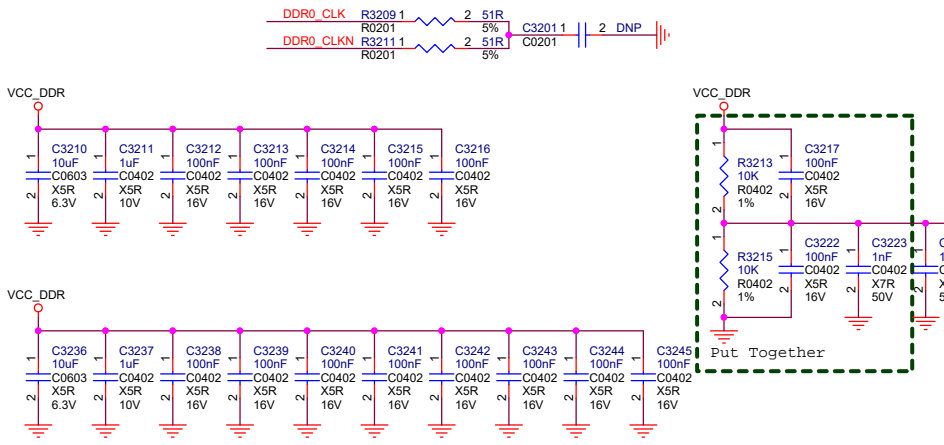
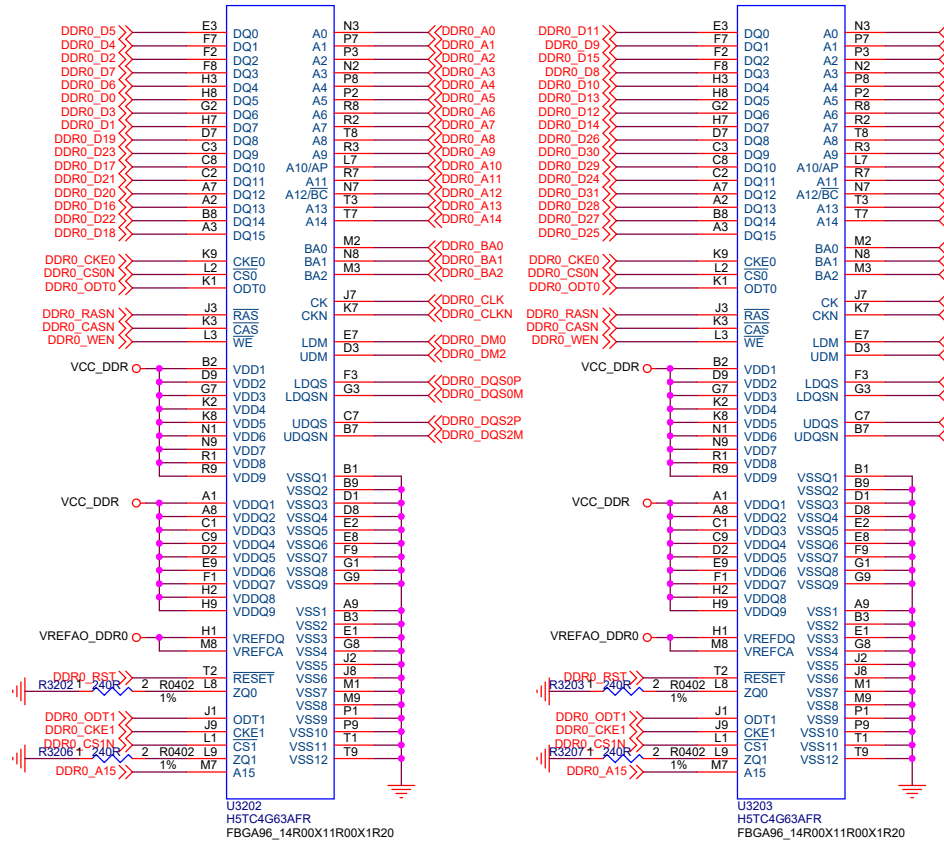


DDR3 4x16bit

Note:The simulation frequency of the template is 800MHz.
Remind: Refer to the latest AVL for parts selection.



Note:All the Power filter capacitors should be placed close to the power pins of DDR

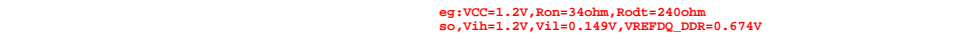
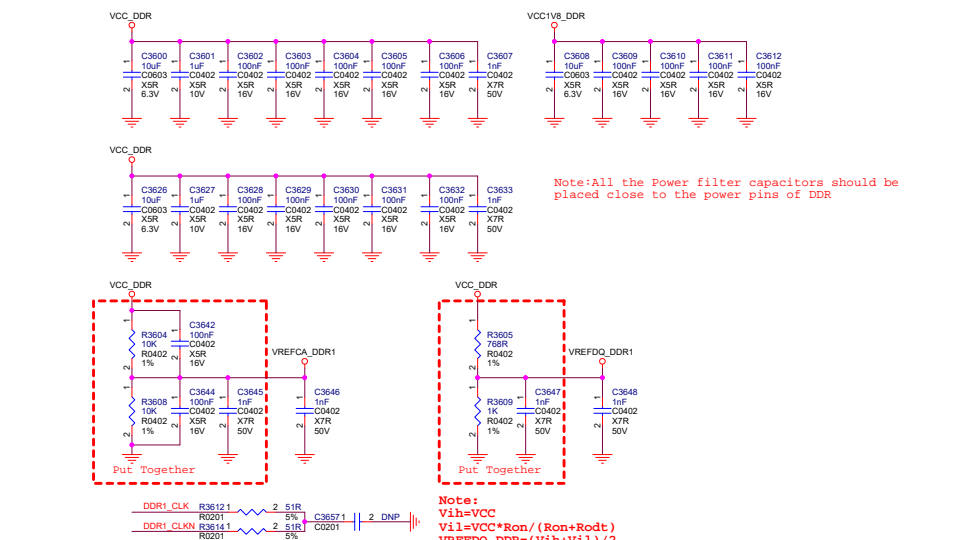
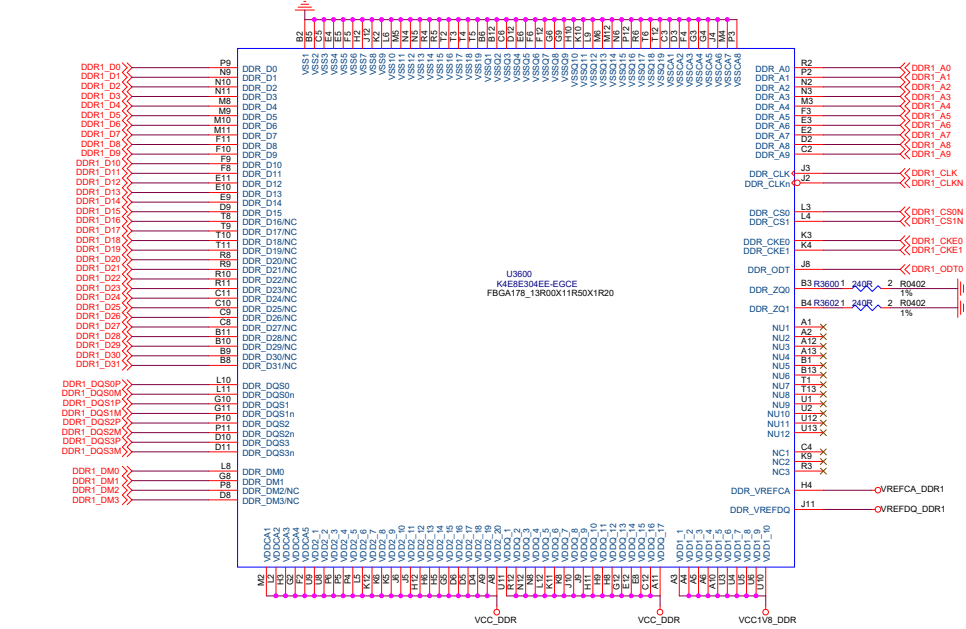


Note:All the Power filter capacitors should be placed close to the power pins of DDR

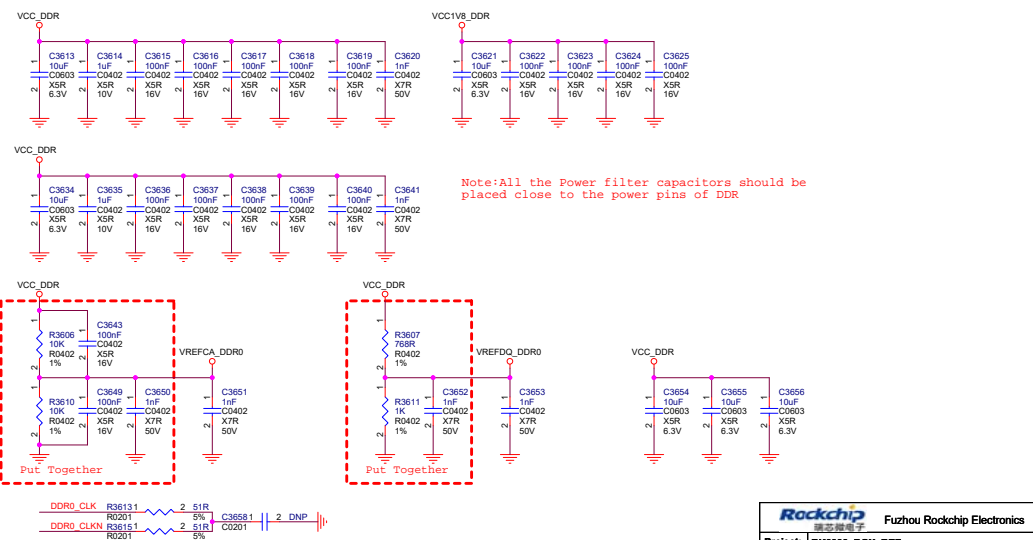
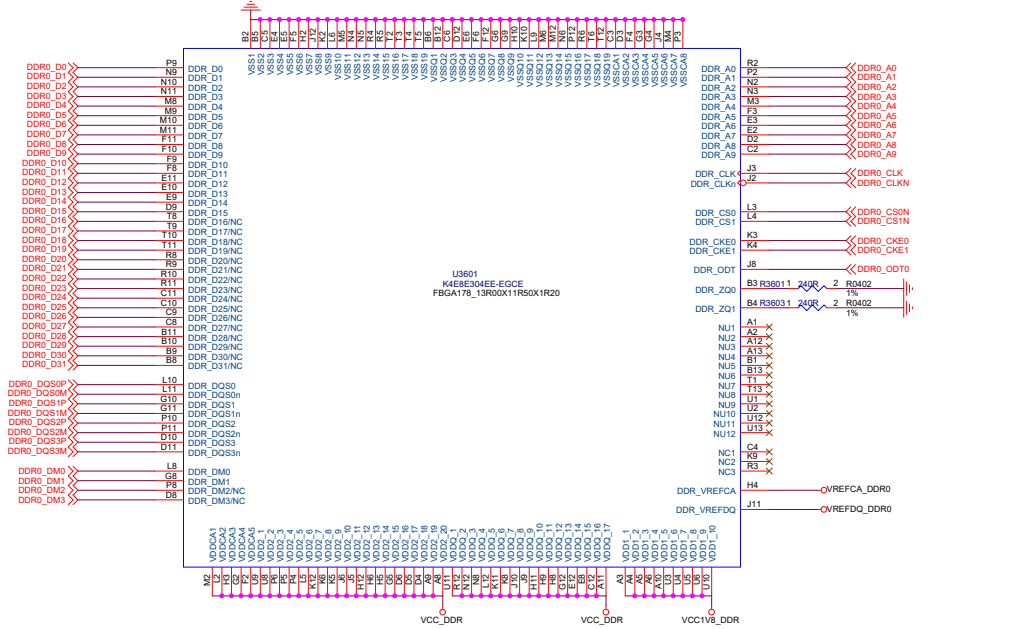
LPDDR3 2x32bit 178ball1

Note:The simulation frequency of the template is 800MHz.

Remind: Refer to the latest AVL for parts selection.

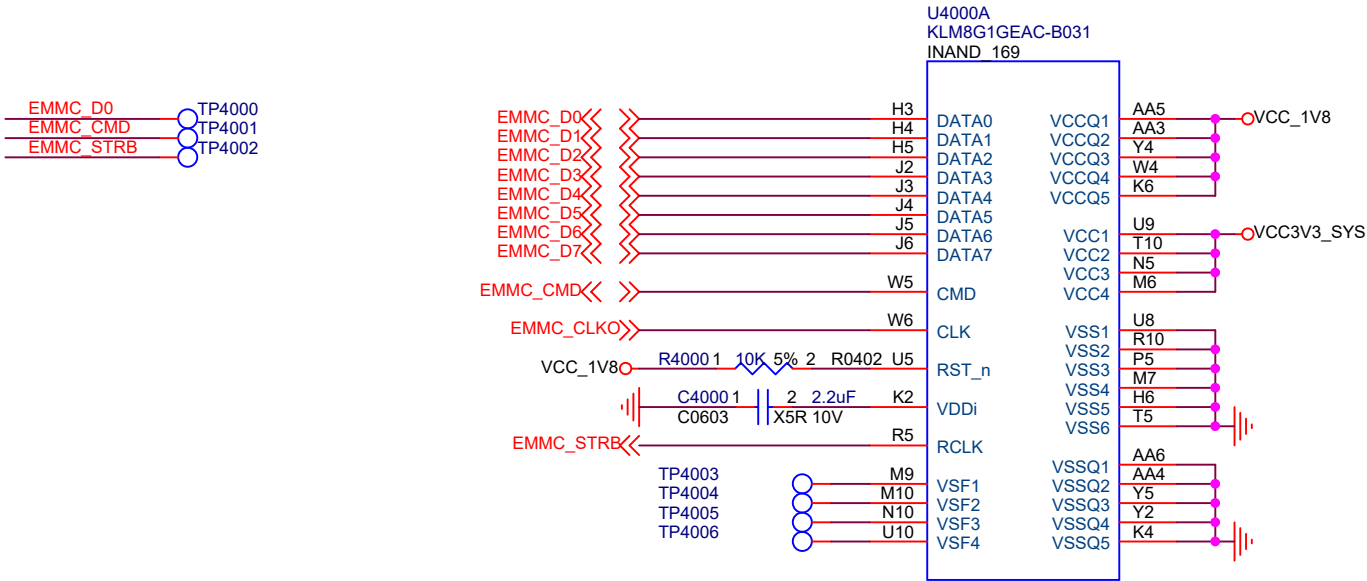


eg:VCC=1.2V,Ron=34ohm,Rodd=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

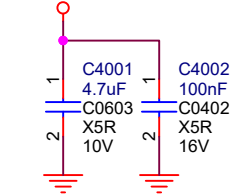


eg:VCC=1.2V,Ron=34ohm,Rodd=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

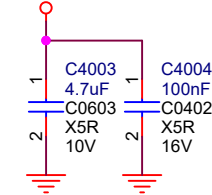
eMMC FLASH



VCC3V3_SYS

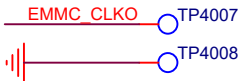



VCC_1V8



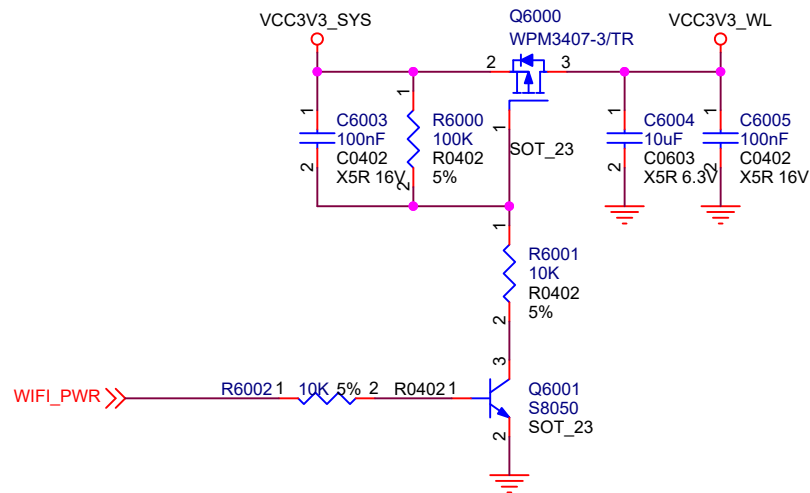
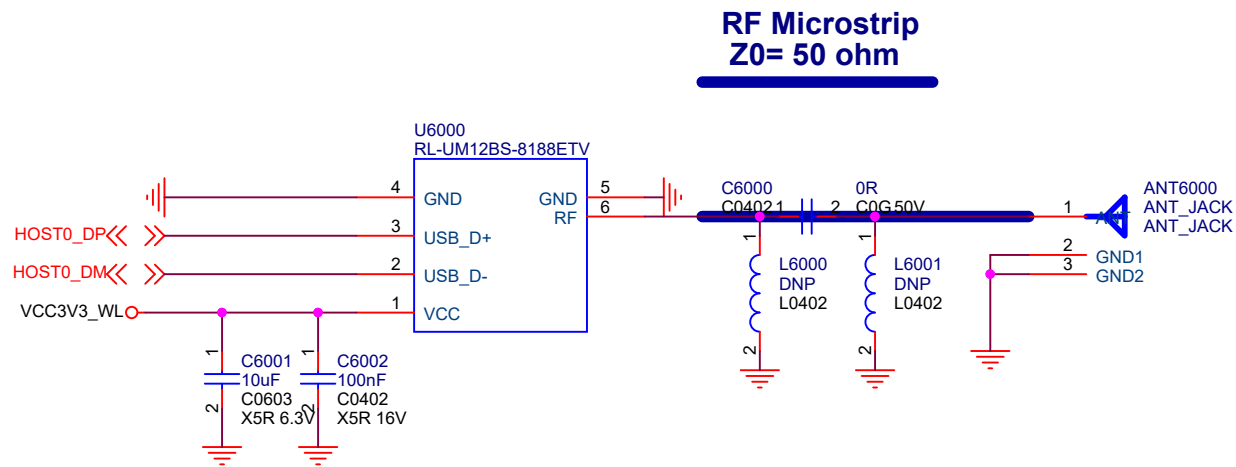
Note: All the Power filter capacitors should be placed close to the power pins of eMMC


Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	40.Memory-eMMC		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	28 of 45

USB WIFI MODULE



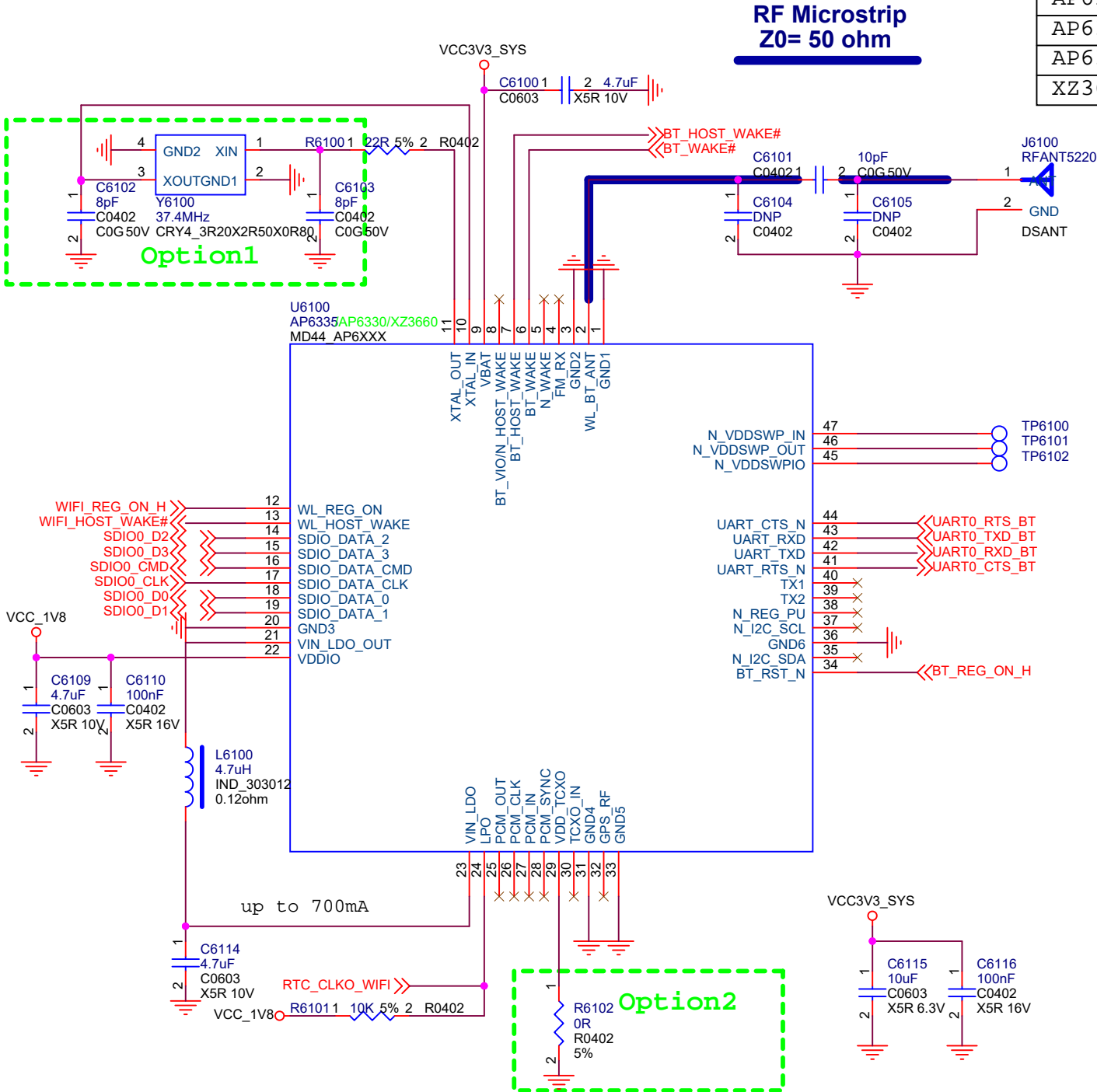
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	60.WIFI-USB (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	29 of 45


SDIO WIFI/BT MODULE

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

YES:should mounted; NO:don't mounted

	Option1	Option2	Option3	
AP6212	26MHz	NO	NO	
AP6330	26MHz	NO	NO	
AP6335	37.4MHz	YES	YES	ac
XZ3660	26MHz	NO	NO	





Fuzhou Rockchip Electronics

Project:

RK3399_BOX_REF

File:

61.WIFI/BT-AP6xxx (option)

Date:

Tuesday, August 21, 2018

Rev:

V1.3

Designed by:

Linus

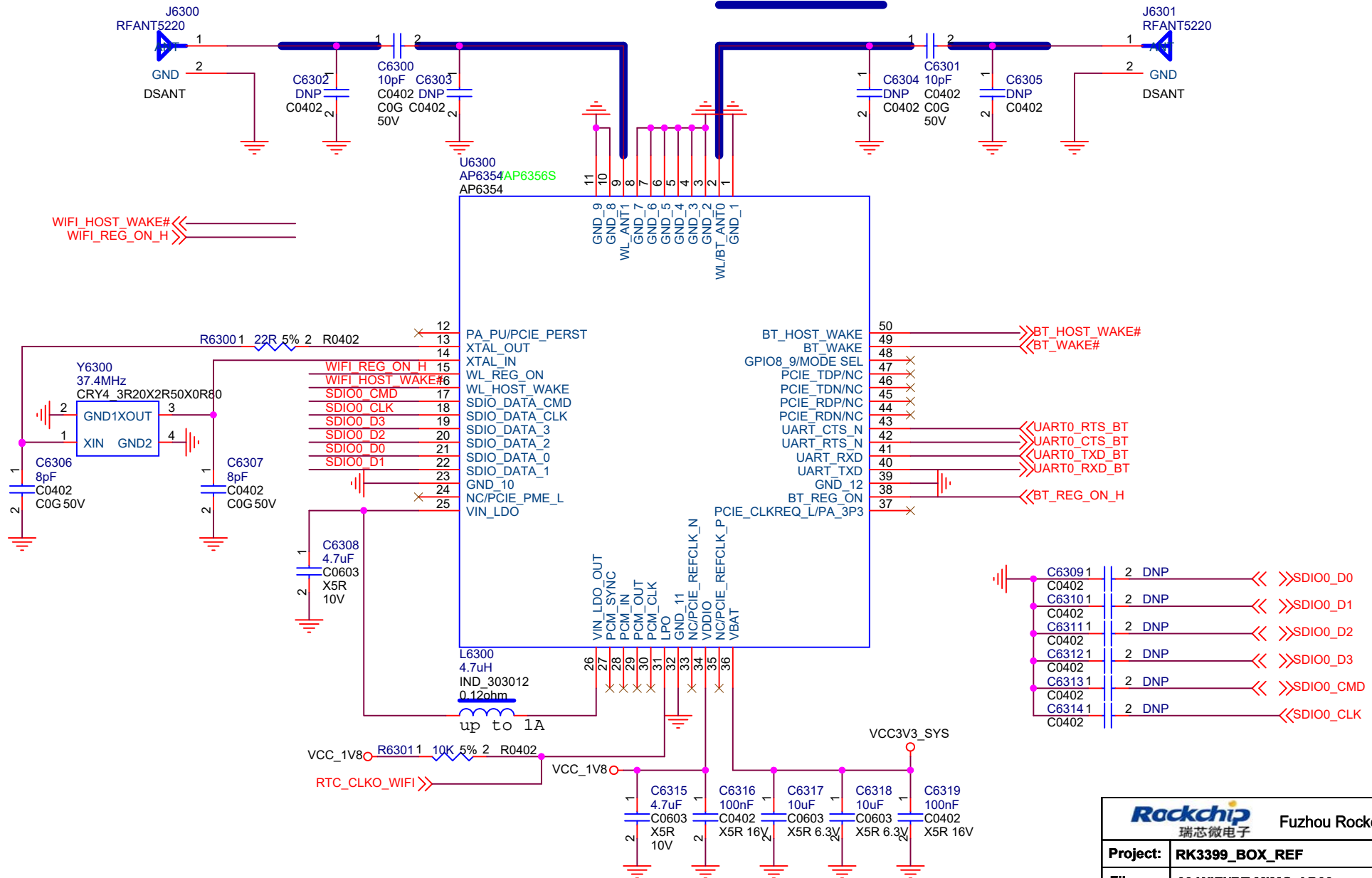
Sheet:

30 of 45

SDIO WIFI/BT MODULE-MIMO

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

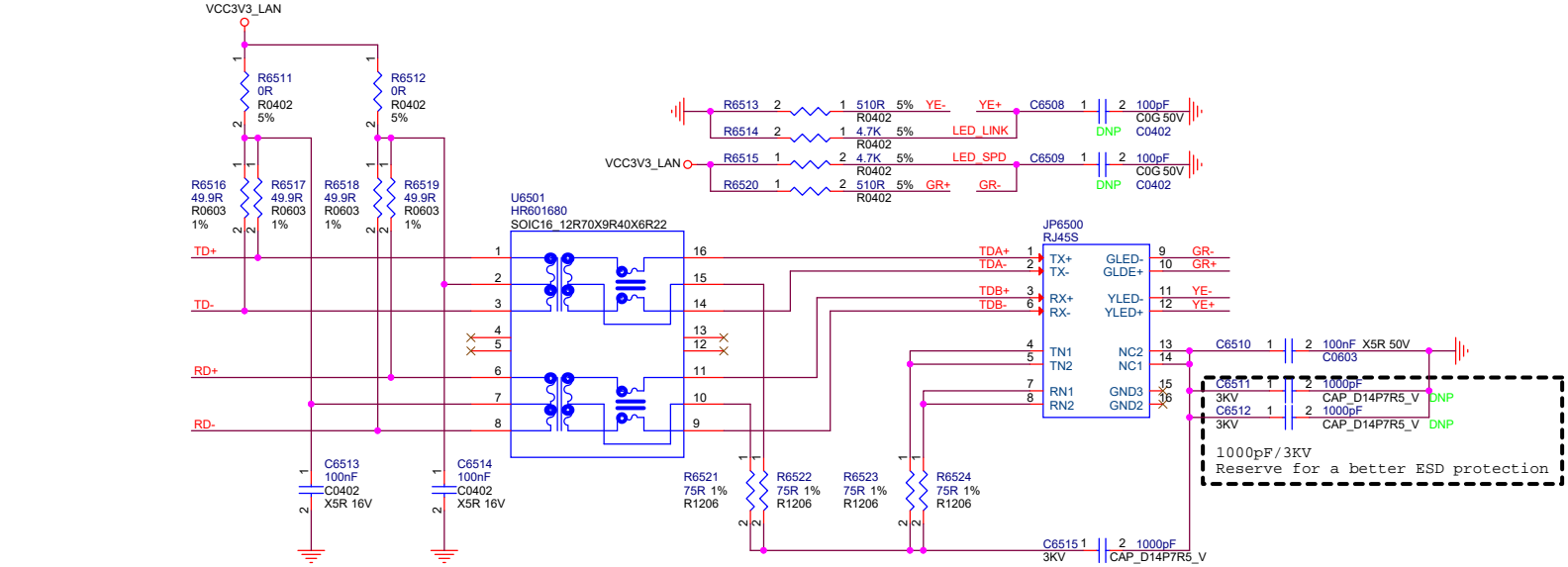
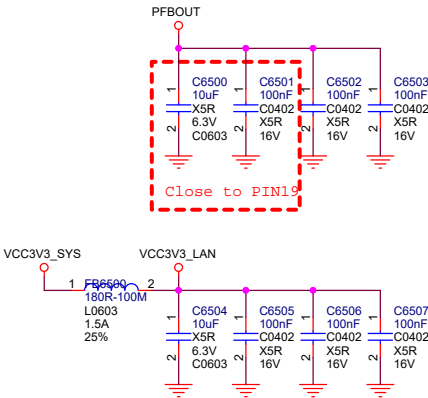
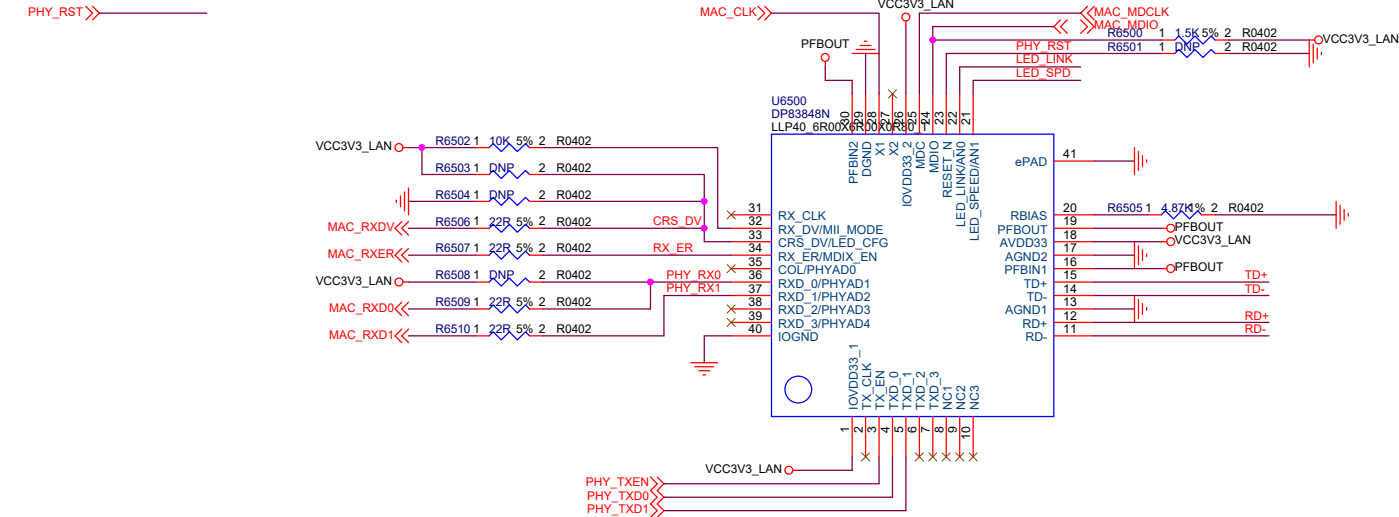
RF Microstrip
Z0= 50 ohm



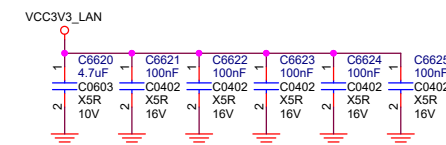
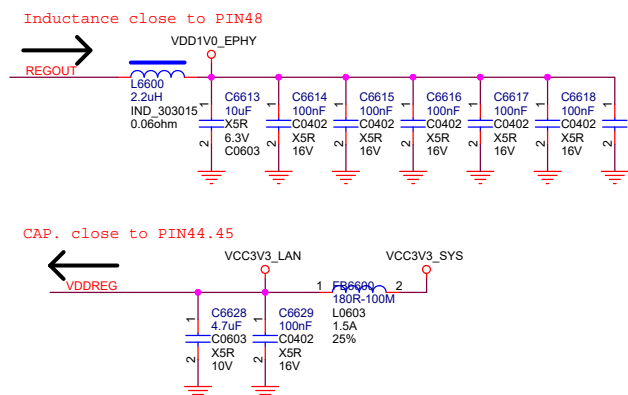
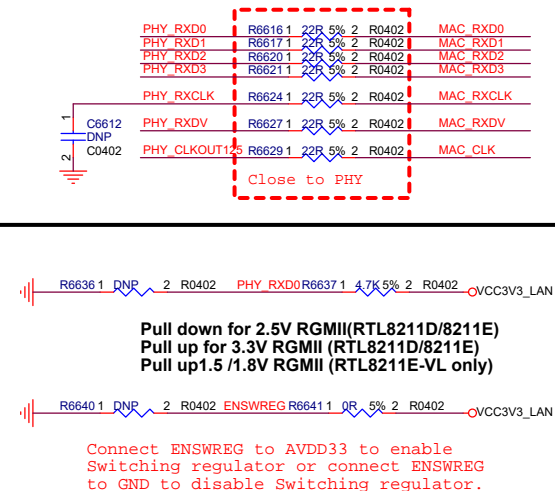
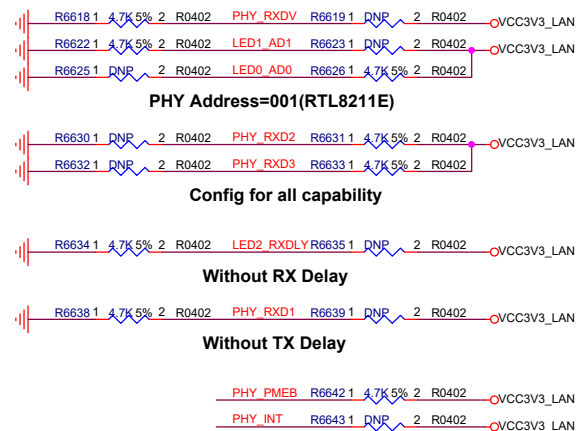
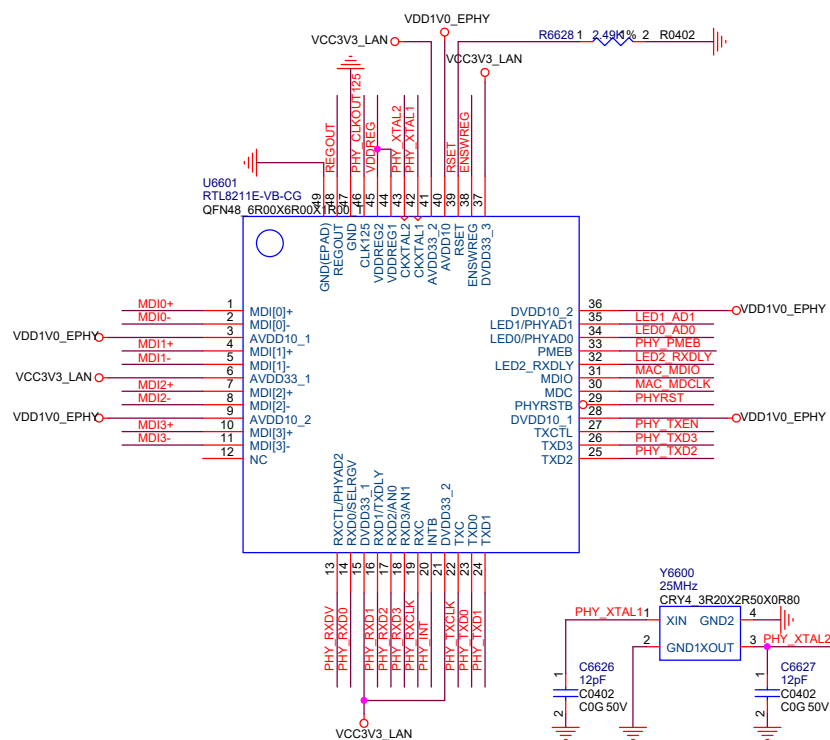
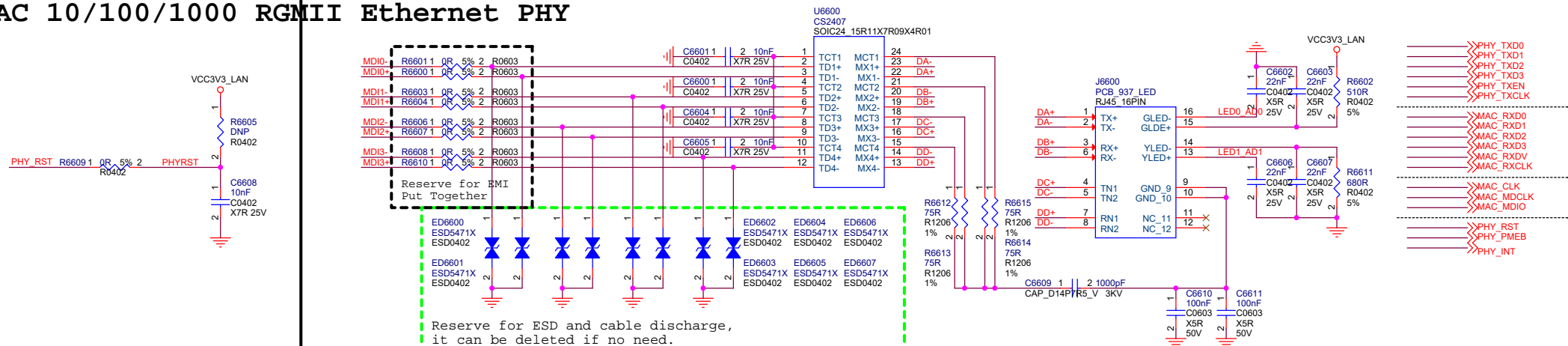
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	63.WIFI/BT MIMO-AP63xx		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	31 of 45

EMAC 10/100 MII Ethernet PHY

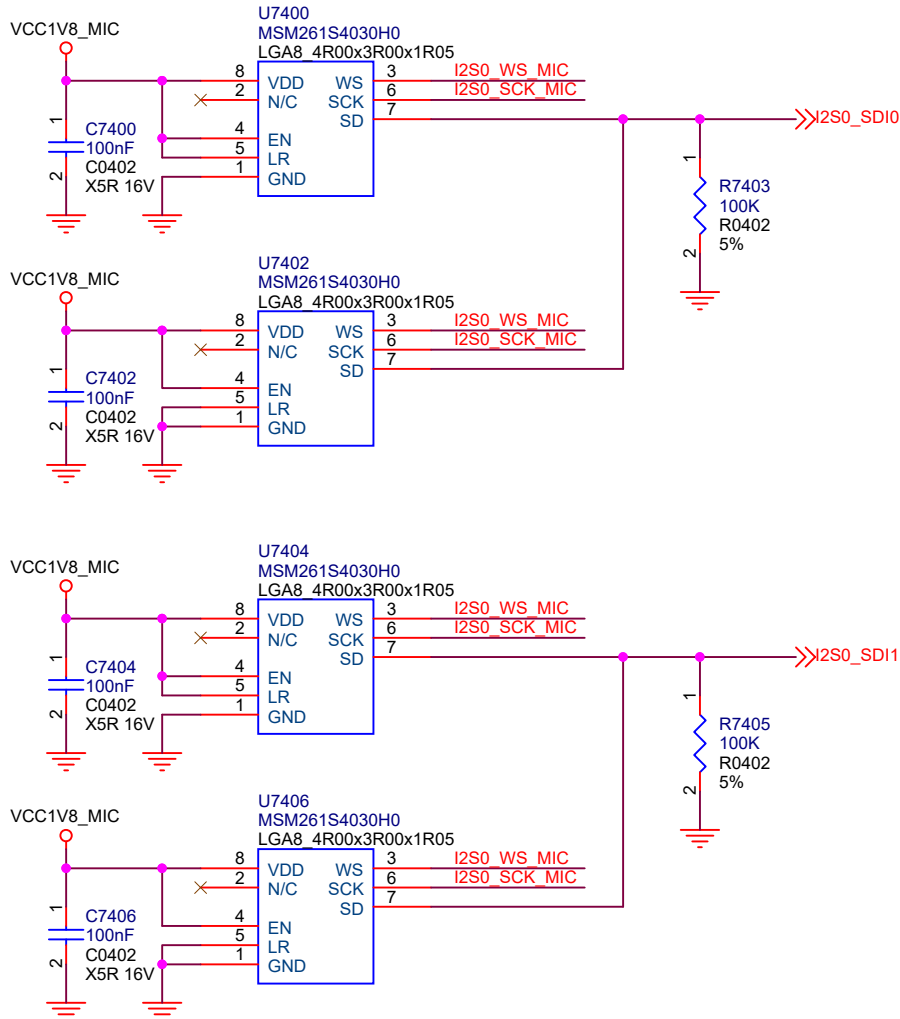
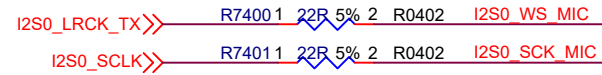
Power



GMAC 10/100/1000 RGMII Ethernet PHY

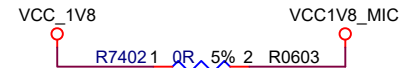


Microphone Array

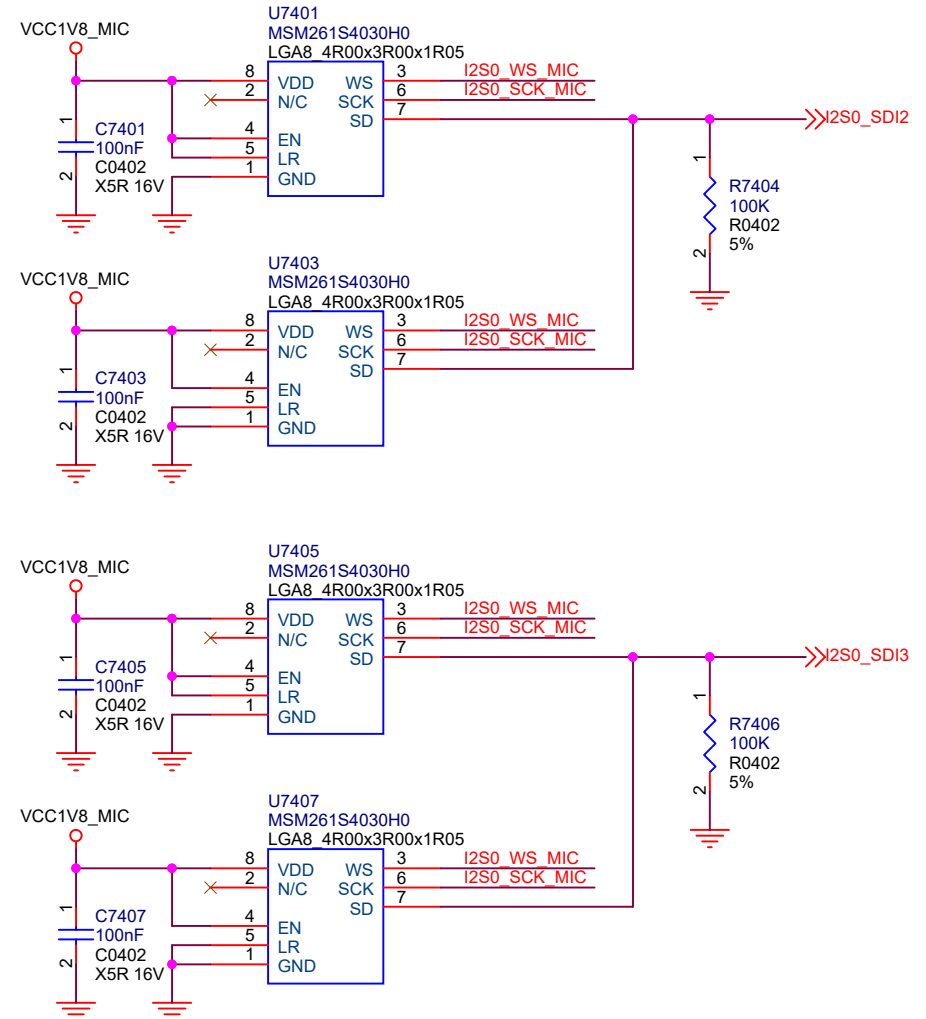


Note: The SDI line should have a 100kohm PD resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.

Power

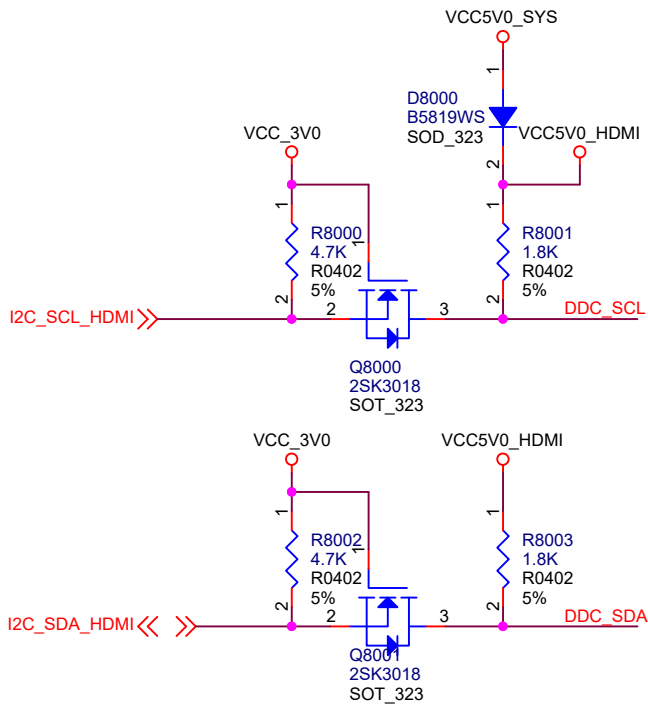
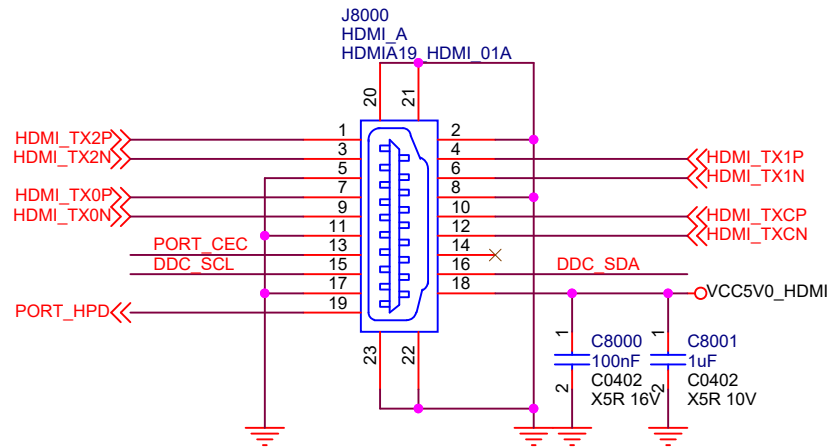


Note:
If it have the audio daughter board,
please use independent power
supply replace.



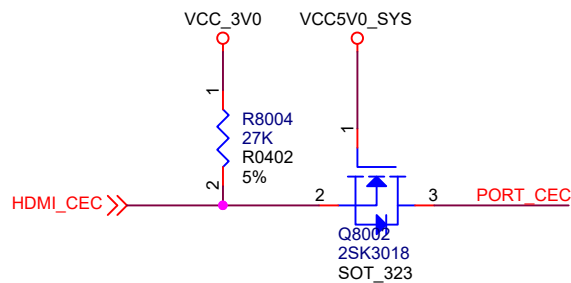
 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
File:	74.Microphone Array		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	35 of 45

HDMI Output



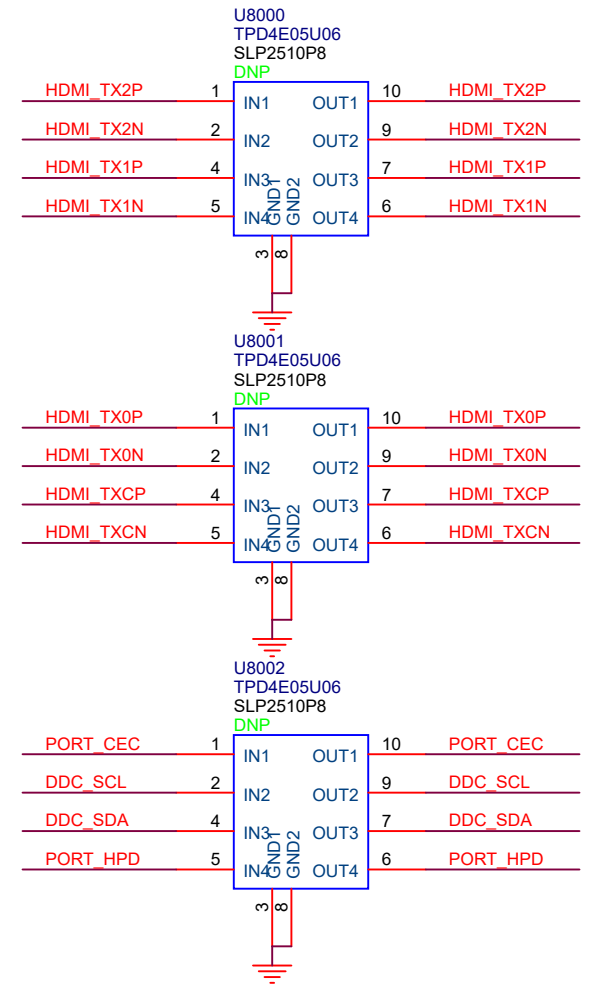
Option

Use for HDMI CEC function,
it can be deleted if no need;



ESD

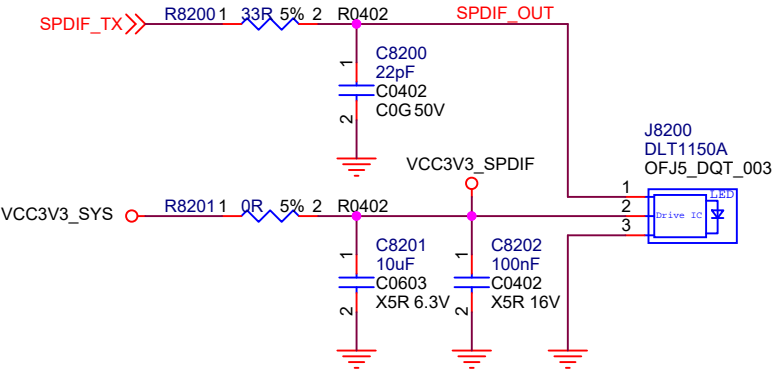
Note: All the ESD components should be placed close to the port and $C_j \leq 0.4\text{pF}$




Fuzhou Rockchip Electronics

Project:	RK3399_BOX_REF		
File:	80.HDMI Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	36 of 45

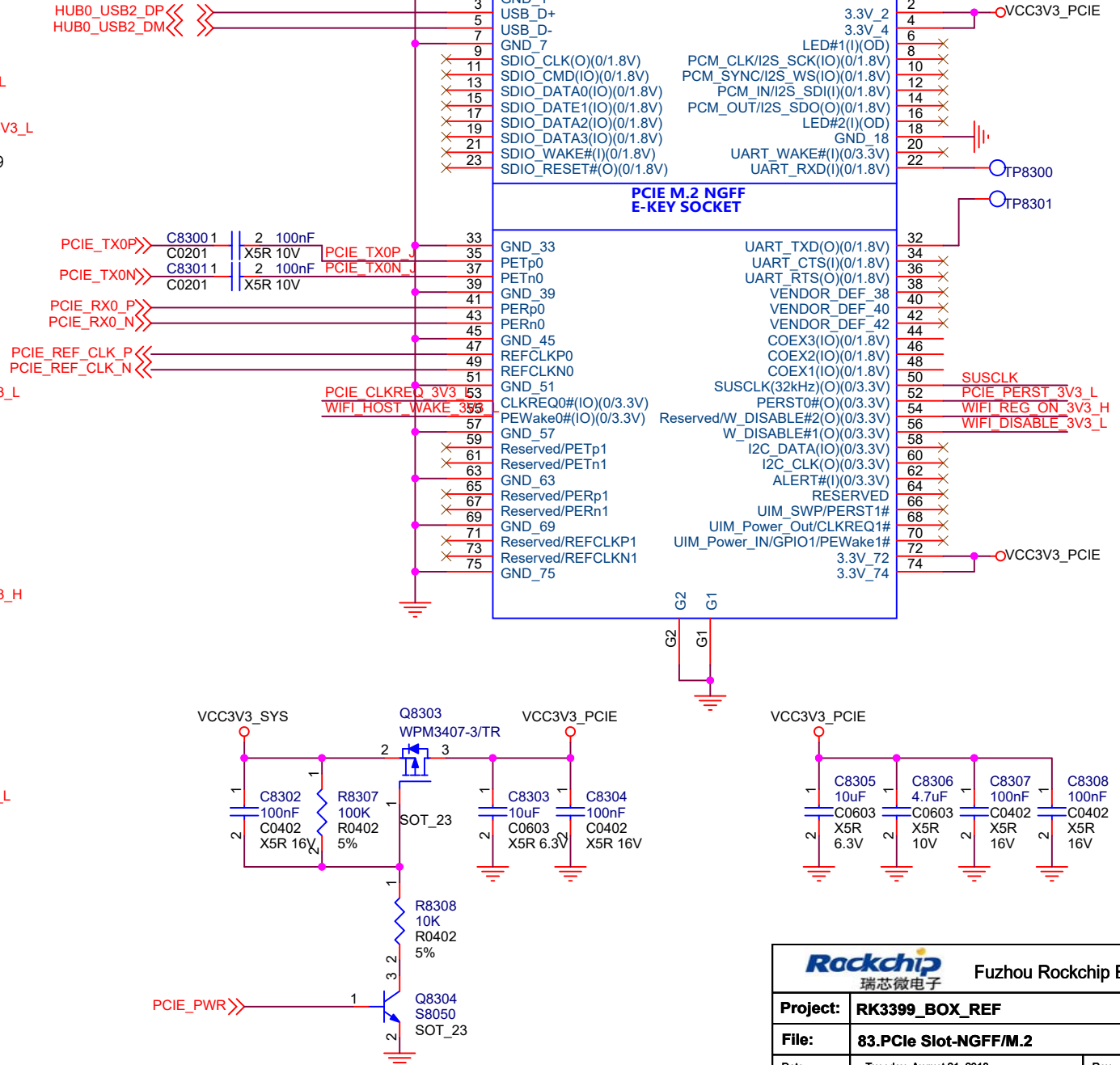
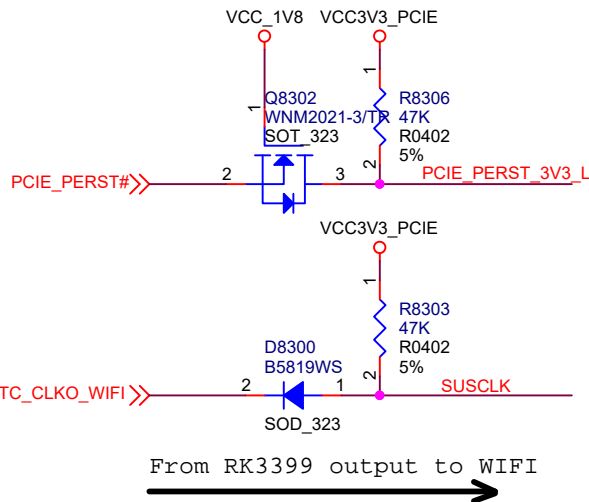
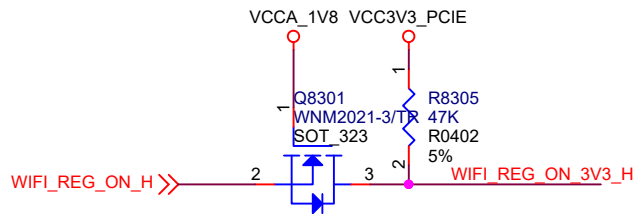
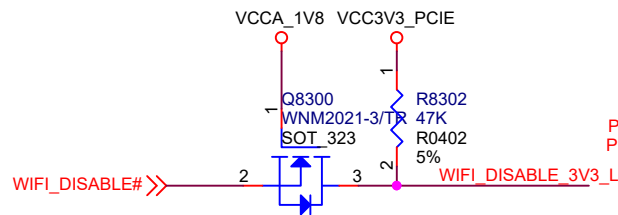
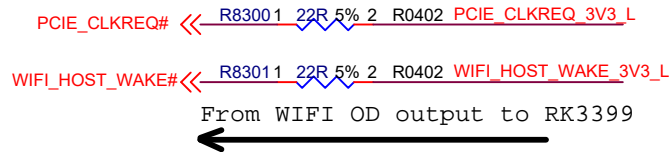
SPDIF OUT



		Fuzhou Rockchip Electronics	
瑞芯微电子			
Project:	RK3399_BOX_REF		
File:	82.SPDIF Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	38 of 45

PCIe slot-NGFF/M.2

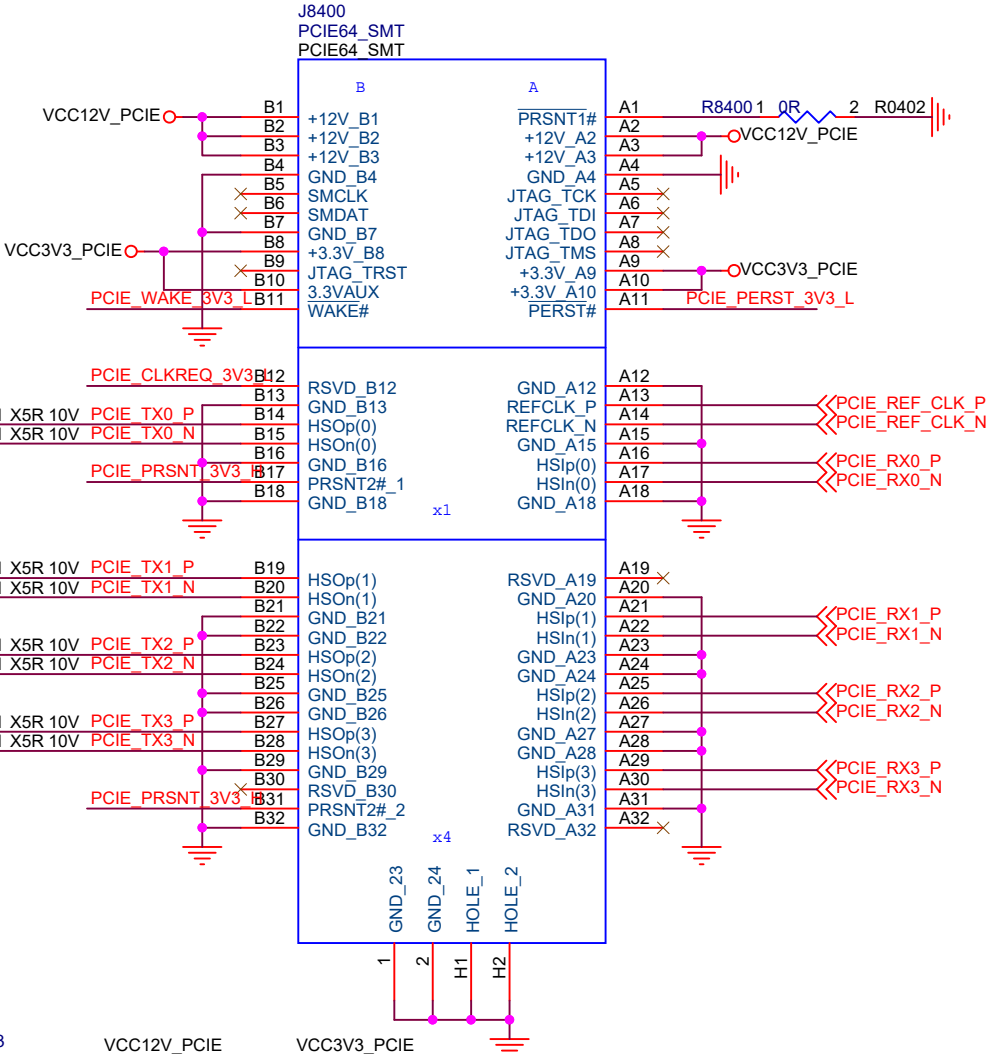
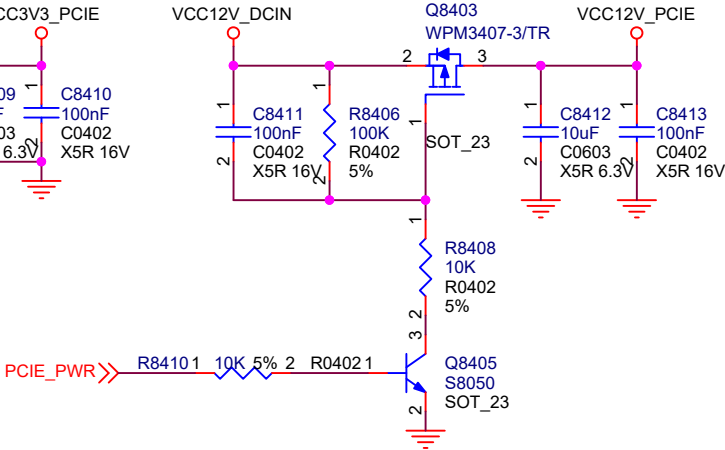
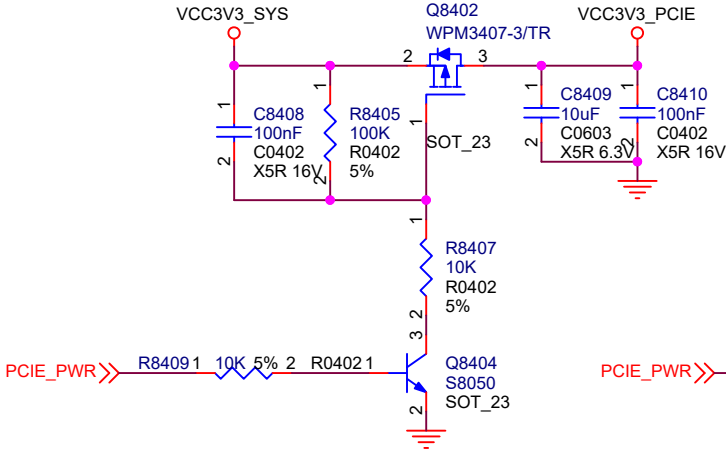
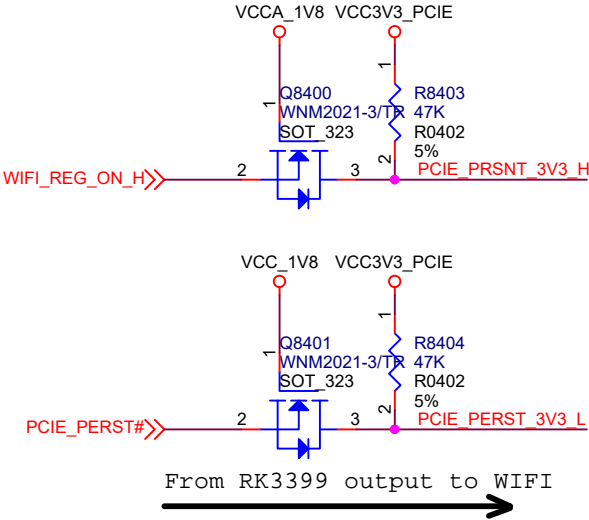
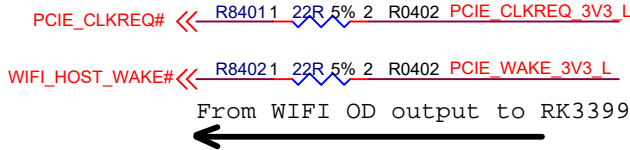
Note:VCC3V3_PCIE peak-current
is at least 1.5A.



Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
File:	83.PCIE Slot-NGFF/M.2		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	39 of 45

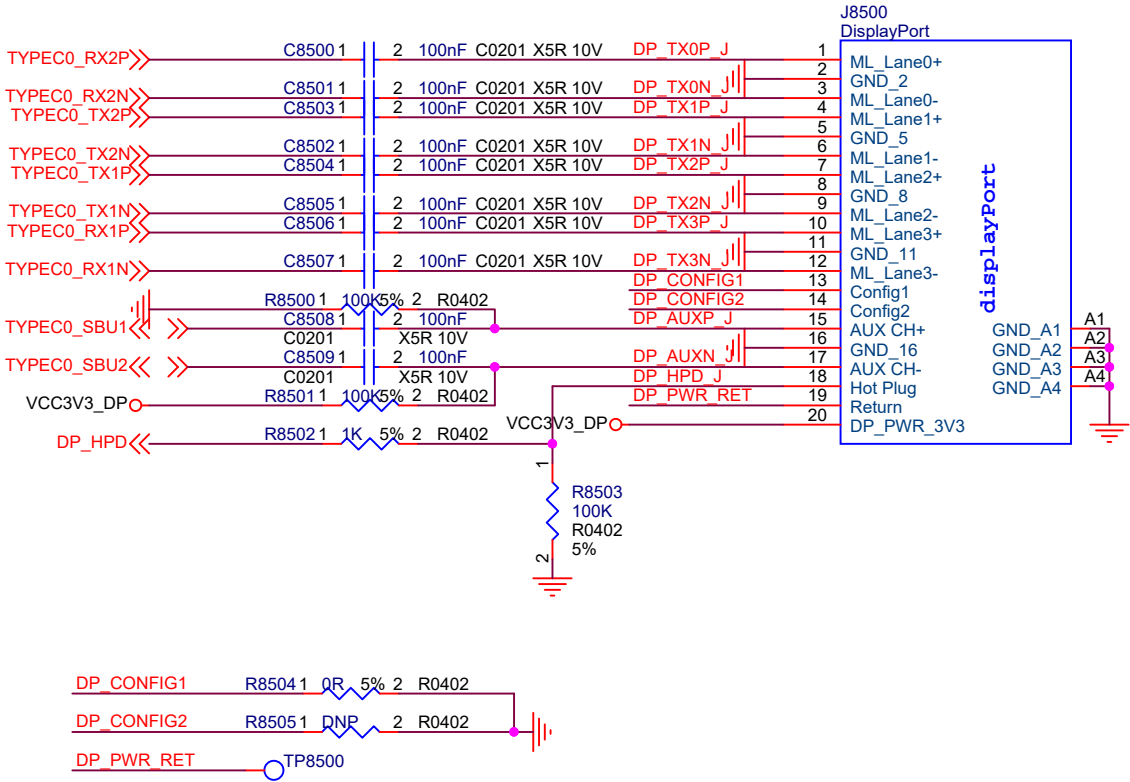
PCIe slot-x4

Note:VCC3V3_PCIE peak-current is at least 1.5A.

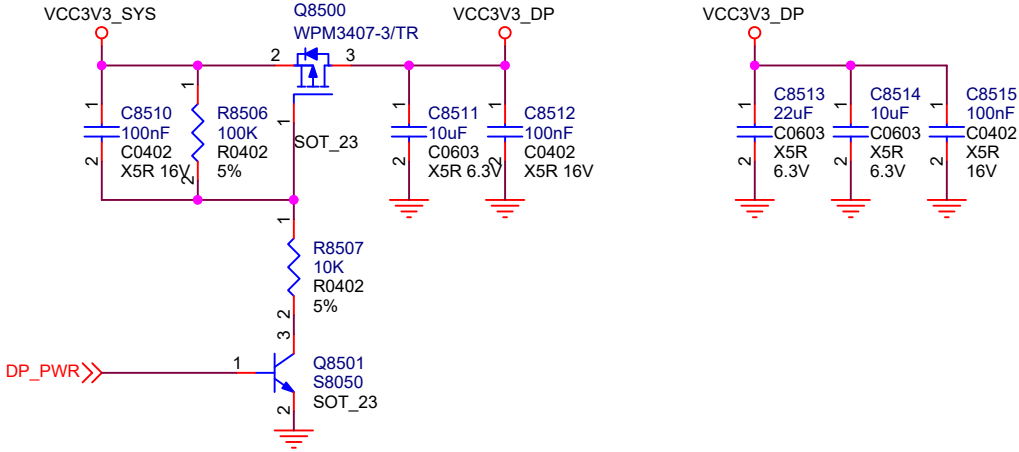


<div>Rockchip</div> <div>瑞芯微电子</div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	84.PCIE Slot-x4 (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	40 of 45

DP Output

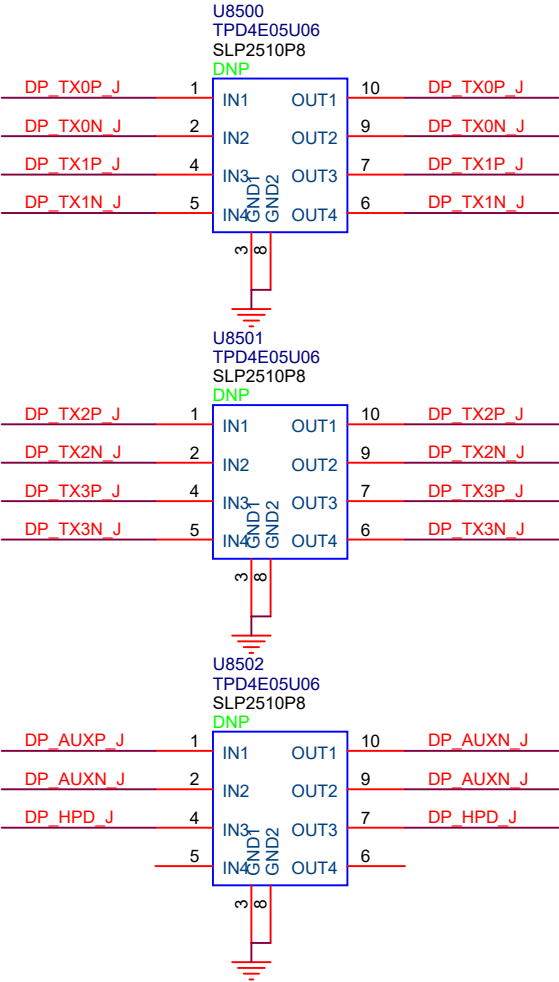


Power



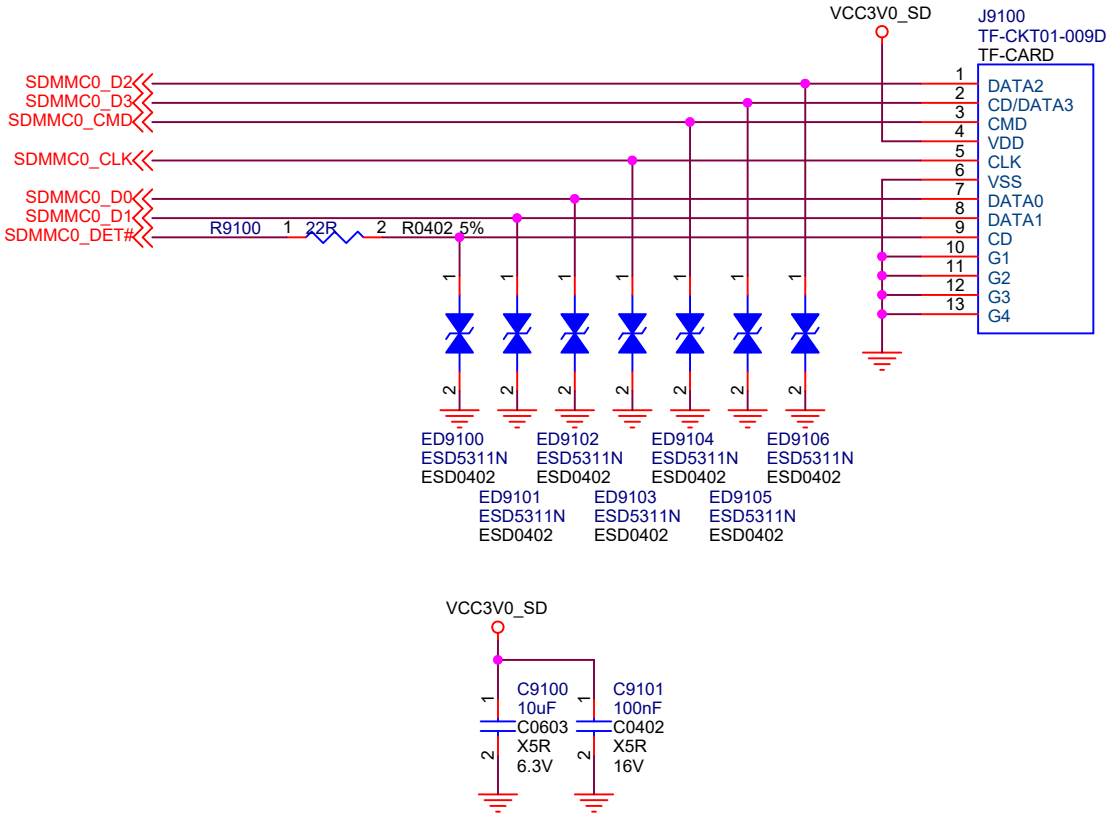
ESD

Note: All the ESD components should be placed close to the port and $C_j \leq 0.4\text{pF}$

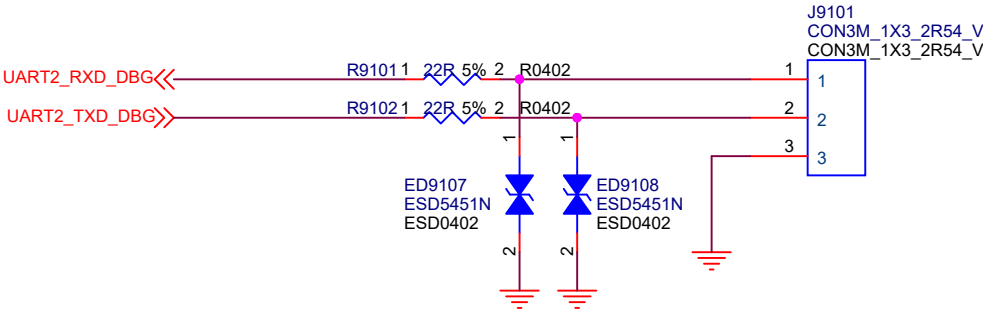


Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
File:	85.DP Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	41 of 45

TF CARD

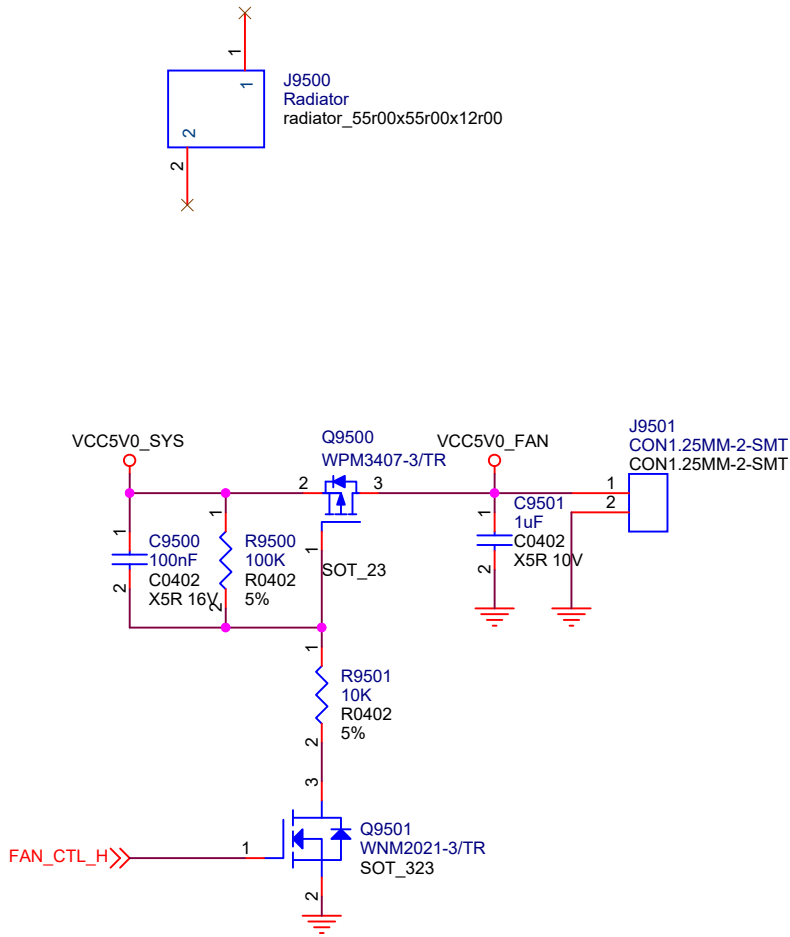


UART for debug



HEATSINK/FAN(option)

Note:Power for FAN,It can be deleted if no need.



<div><div>Rockchip</div><div>瑞芯微电子</div></div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	95.HEATSINK/FAN (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	44 of 45

eFUSE(option)

Note:Power for eFUSE Program,it is recommended to reserve on the tooling.It can be deleted if no need.

