


Reference Schematic For RK3399

RK3399_BOX_REF_V1.3
20180821



瑞芯微电子

Fuzhou Rockchip Electronics

Project:	RK3399_BOX_REF		
File:	00.Cover Page		
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Designed by:	Linus	Sheet:	1 of 45

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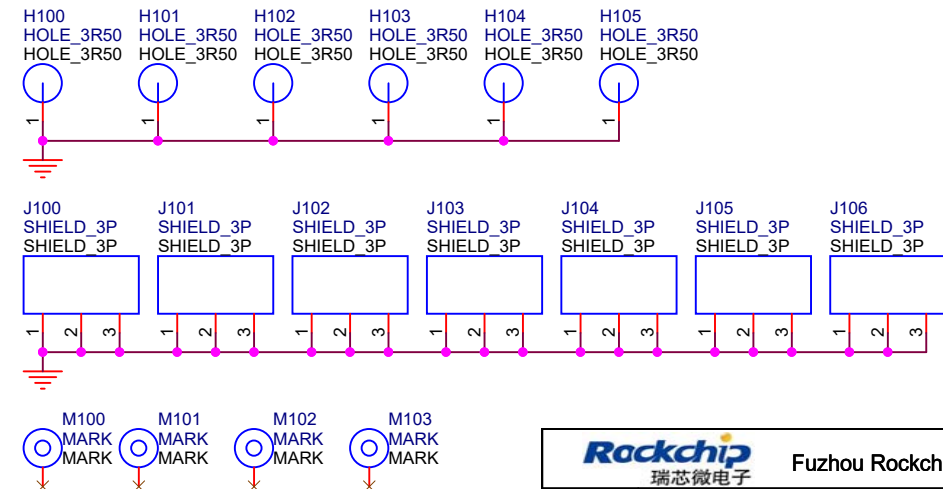
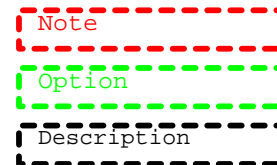
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Page44	---95.HEATSINK/FAN(option)
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6 LAYERS PCB STACK (e.g. PCB=1.0mm)

TOP	Prepreg	1080*1	(75um)	Silkscreen (25um) 1oz(35um)
GND1	Prepreg	2116*1	(115um)	Hoz(18um)
POWER				Hoz(18um)
	Adjust Core		(465um)	
SIGNAL	Prepreg	2116*1	(115um)	Hoz(18um)
GND2	Prepreg	1080*1	(75um)	Hoz(18um)
BOTTOM				1oz(35um) Silkscreen (25um)

Note:

1: If the Value or option of the component properties is DNP, indicating do not mounted

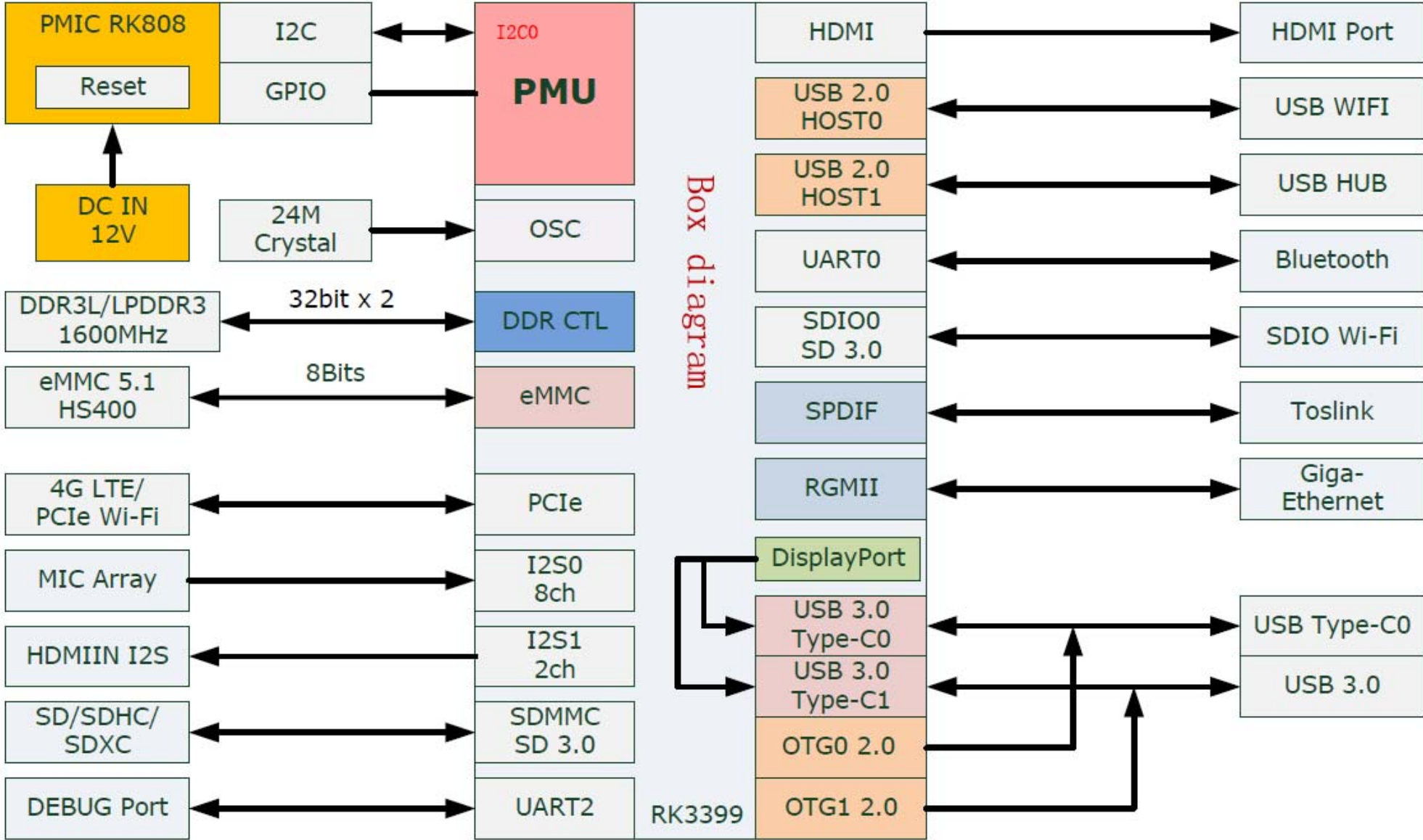


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Revision History


Version	Date	Author	Change Note	Approved
V1.0	2017.01.12	Linus.Lin	First edition	
V1.1	2017.05.12	Linus.Lin	Please refer to the document of 《RK3399_BOX_REF_V11_20170512 Modify Notes》	
V1.2	2017.12.18	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_v12_20171218.xlsx》	
V1.3	2018.08.21	Linus.Lin	Please refer to the document of 《RK3399（BOX）硬件发布说明及文件列表_v13_20180821.xlsx》	

Block Diagram



I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808-D	0x1b	PMIC	100kHz,400KHz
					Silergy SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					Silergy SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8	Toshiba TC358749XBG		HDMI Transmit	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	RESERVE					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_TYPEC I2C_SCL_TYPEC	VCC_1V8	Fairchild FUSB302B ETEK ET302Y	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					



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04.I2C Map

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Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuiol_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLD03
Part E	PMUIO2	pmul830_gpiolabcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLD03
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLD06 RK808-D VLD08
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCCIO_SD	RK808-D VLD04



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05.Power Domain Map

Date:

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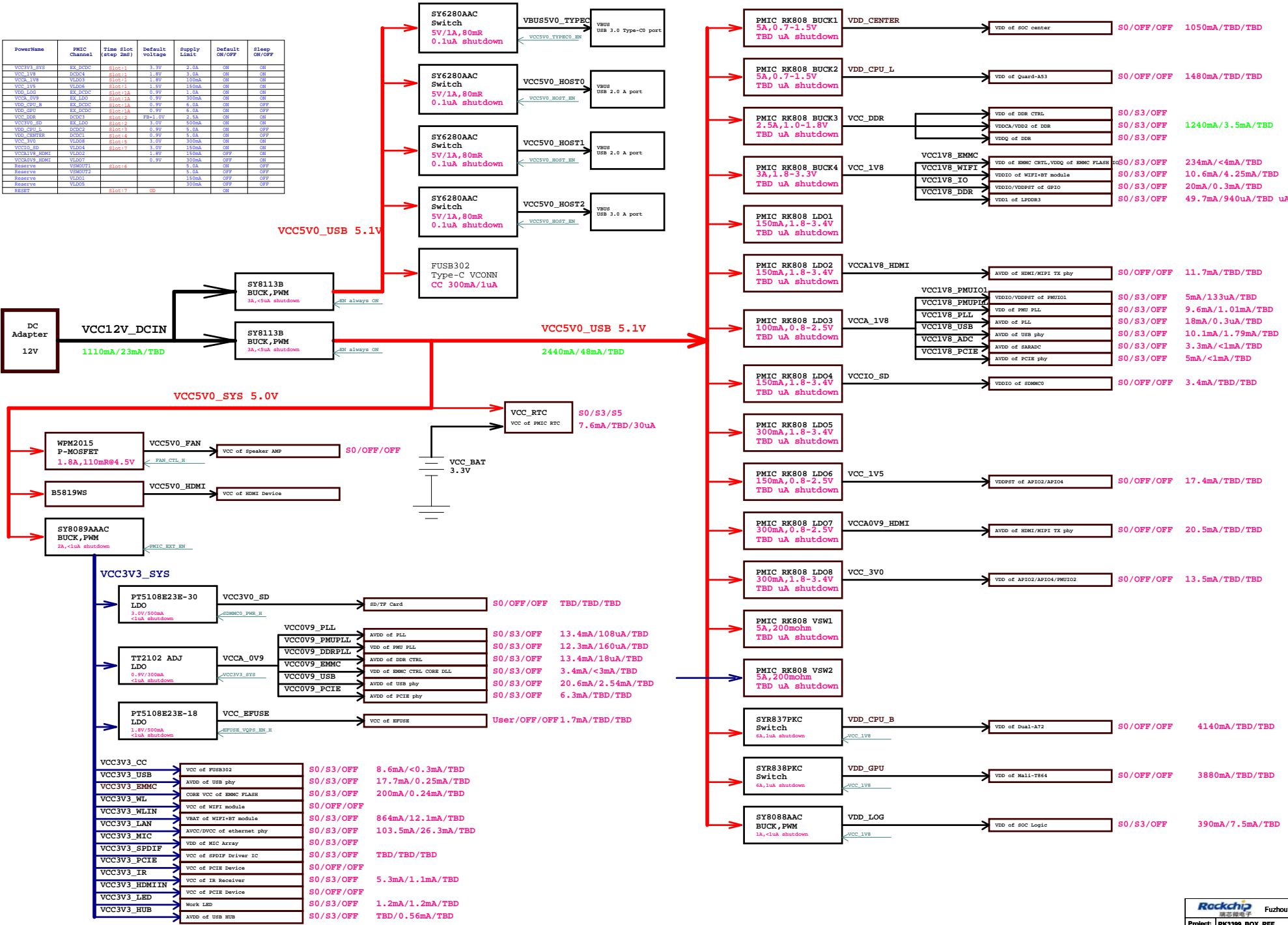
Linus

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RK808-D Power Diagram and Sequence

PowerName	CHC Channel	Time Slot (sec 2ms)	Default Voltage	Supply Limit	Default On/OFF	Sleep On/OFF
VCCP11_500	BA_220C2	Slot1-1	1.2V	2.0A	ON	ON
VCCP12_500	BA_220C2	Slot1-1	1.8V	2.0A	ON	ON
VCCP13_500	BA_220C2	Slot1-1	1.5V	100mA	ON	ON
VCC_15V	VLAD05	Slot1-1	1.5V	150mA	ON	ON
VCCP14_500	BA_220C2	Slot1-1	0.9V	2.0A	ON	ON
VCCP15_500	BA_1450	Slot1-1A	0.8V	300mA	ON	ON
VCCP16_500	BA_1450	Slot1-1A	0.9V	6.0A	ON	ON
VCC_PSP	BA_220C2	Slot1-1A	0.8V	2.0A	ON	OFF
VCCP17_500	BA_220C2	Slot1-1	1.8V	2.0A	ON	ON
VCCP18_500	BA_1450	Slot1-2	1.0V	500mA	ON	ON
VCC_PSP2	CD002	Slot1-3	0.8V	5.0A	ON	OFF
VCCP19_500	BA_220C2	Slot1-1	1.5V	2.0A	ON	ON
VCC_3V3	VLAD05	Slot1-5	3.0V	500mA	ON	ON
VCCP20_500	BA_220C2	Slot1-1	0.9V	150mA	ON	ON
VCCP21_500	VLAD02	Slot1-6	1.8V	150mA	OFF	ON
VCCP22_500	BA_220C2	Slot1-1	0.9V	300mA	ON	ON
Reserve1	TRM0017	Slot1-6	1.5V	1.0A	ON	OFF
Reserve2	TRM0017	Slot1-6	0.8V	5.0A	ON	OFF
Reserve3	VLAD01		1.5V	150mA	OFF	OFF
Reserve4	VLAD05		3.0V	300mA	OFF	OFF
Reserve5		Slot1-7	OD	100mA	OFF	OFF




Trace>4.5A

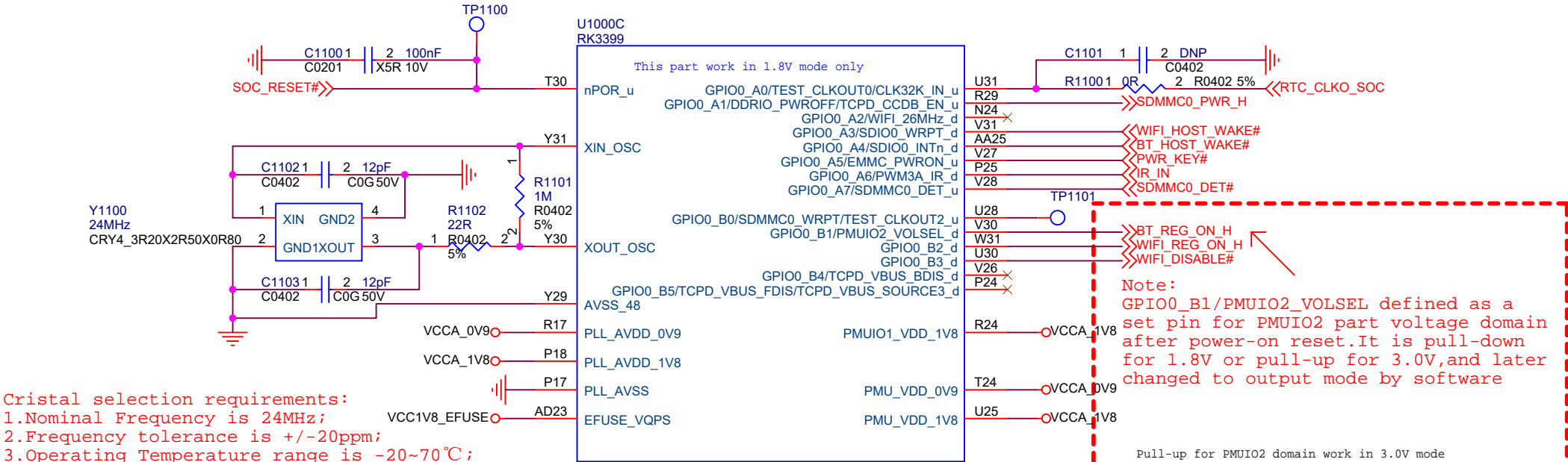


The figure displays four schematic diagrams of power planes, each showing a series of capacitors connected to a common power rail. The components and their values are as follows:

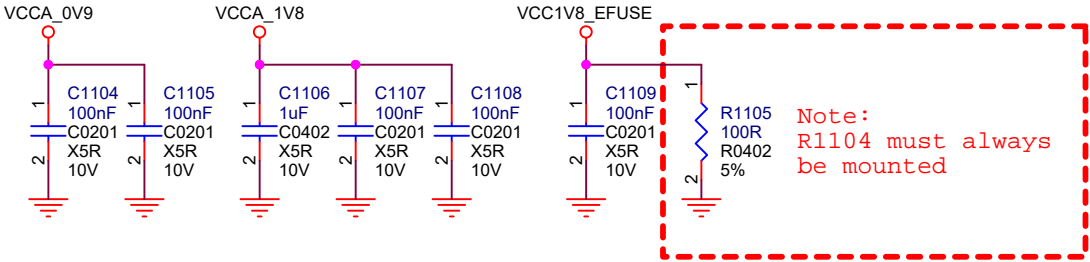
- VDD_LOG:** C1005 (22uF, X5R, 6.3V), C1006 (10uF, X5R, 4V), C1007 (1uF, C0402, 10V), C1008 (100nF, C0201, 10V), C1009 (100nF, C0201, 10V), C1010 (100nF, C0201, 10V), C1011 (100nF, C0201, 10V), C1012 (1nF, X5R, 25V).
- VDD_CPU_L:** C1013 (22uF, X5R, 6.3V), C1014 (22uF, C0603, X5R, 6.3V), C1015 (1uF, C0402, X5R, 10V), C1016 (100nF, C0201, X5R, 10V), C1017 (100nF, C0201, X5R, 10V), C1018 (100nF, C0201, X5R, 10V), C1019 (100nF, C0201, X5R, 10V), C1020 (1nF, C0201, X5R, 25V).
- VDD_CPU_B:** C1021 (22uF, X5R, 6.3V), C1022 (22uF, C0603, X5R, 6.3V), C1023 (22uF, C0603, X5R, 6.3V), C1024 (1uF, C0402, X5R, 10V), C1025 (100nF, C0201, X5R, 10V), C1026 (100nF, C0201, X5R, 10V), C1027 (100nF, C0201, X5R, 10V), C1028 (100nF, C0201, X5R, 10V).
- VDD_CPU:** C1039 (22uF, X5R, 6.3V), C1040 (22uF, C0603, X5R, 6.3V), C1041 (22uF, C0603, X5R, 6.3V), C1042 (1uF, C0402, X5R, 10V), C1043 (100nF, C0201, X5R, 10V), C1044 (100nF, C0201, X5R, 10V), C1045 (100nF, C0201, X5R, 10V), C1046 (100nF, C0201, X5R, 10V).

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RK3399_C



Cristal selection requirements:
1.Nominal Frequency is 24MHz;
2.Frequency tolerance is +/-20ppm;
3.Operating Temperature range is -20~70℃;
4.Equivalent resistance < 60ohm;



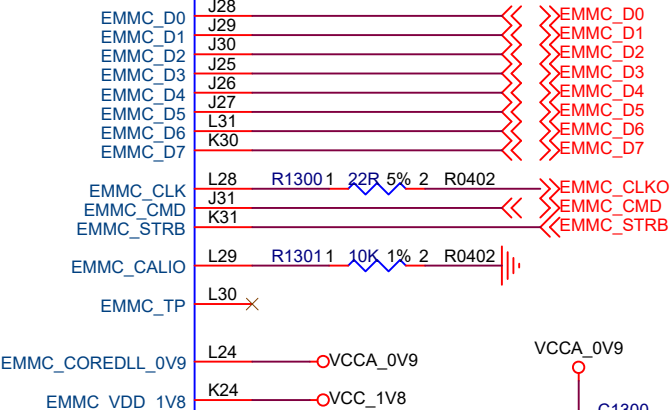
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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File:	11.RK3399 PMU Controller		
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RK3399_H

U1000H
RK3399

This part work in 1.8V mode only



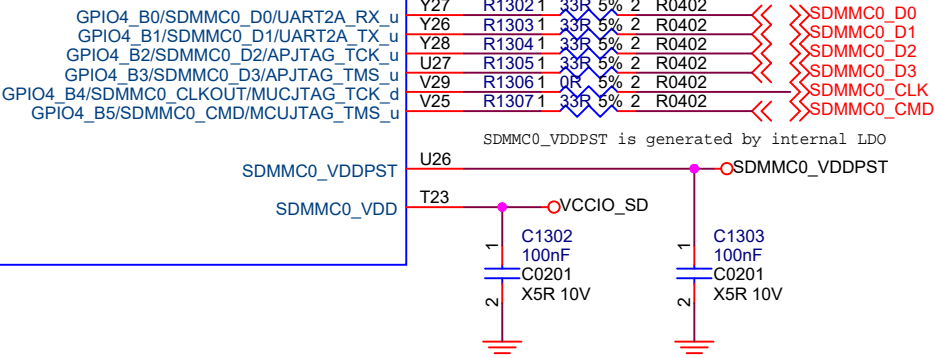
- EMMC design rules:
- 1.Data[0:3],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
 - 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
 - 3.Max trace length < 3.93inchs;
 - 4.Trace impedance 50ohm+/-10%;
 - 5.The distance between other signals follows the 3W rule;
 - 6.R1300 should be place close to RK3399;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_F


U1000F
RK3399

This part work in 1.8V/3.0V auto

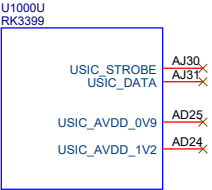


- SDMMC design rules:
- 1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
 - 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
 - 3.Max trace length < 3.93inchs;
 - 4.Trace impedance 50ohm+/-10%;
 - 5.The distance between other signals follows the 3W rule;

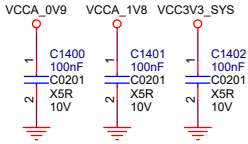
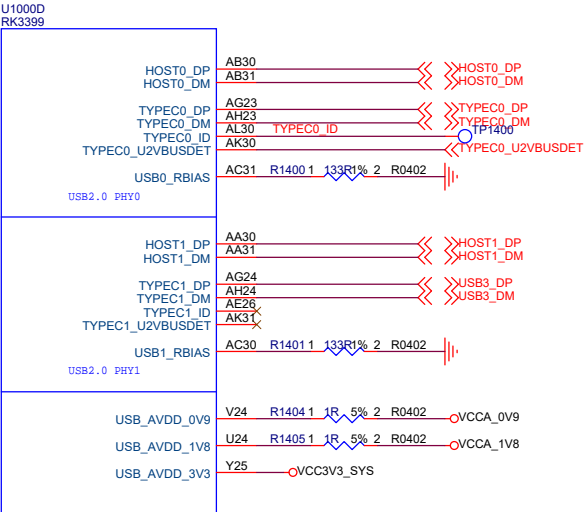
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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File:	13.RK3399 FLASH/SDMMC Controlle		
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RK3399_U



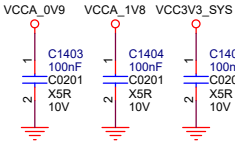
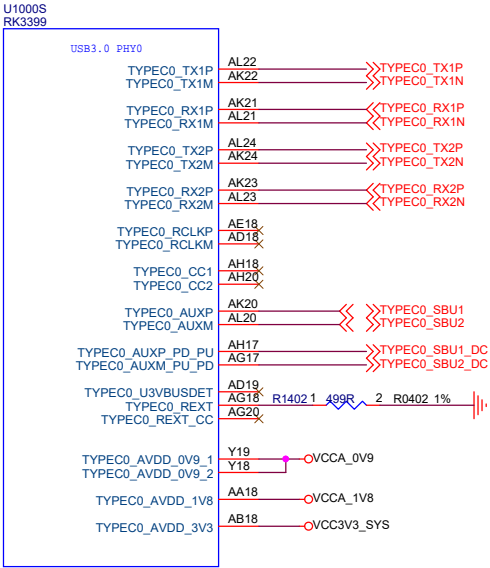
RK3399_D



Note: All the Power filter capacitors should be placed close to the power pins of RK3399

USB2.0 design rules:
1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

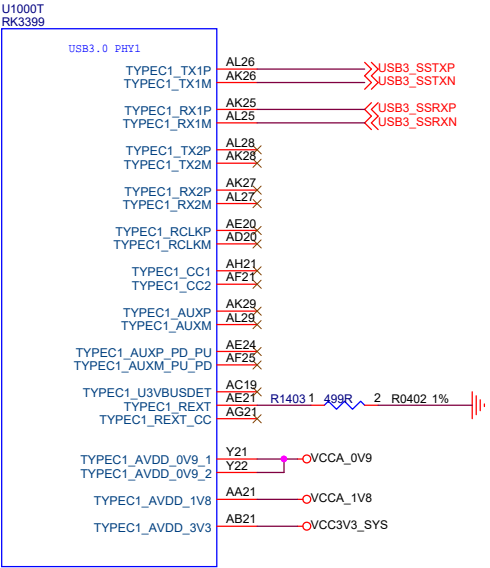
RK3399_S




Note: All the Power filter capacitors should be placed close to the power pins of RK3399

USB3.0 design rules:
1. Max intra-pair skew < 4ps;
2. Max length skew between TX and RX < 1.6ns;
3. Max trace length < 6inchs;
4. Max allowed via < 4;
5. Trace impedance 90ohm+/-10%;
6. The distance between other signals follows the 3W rule;

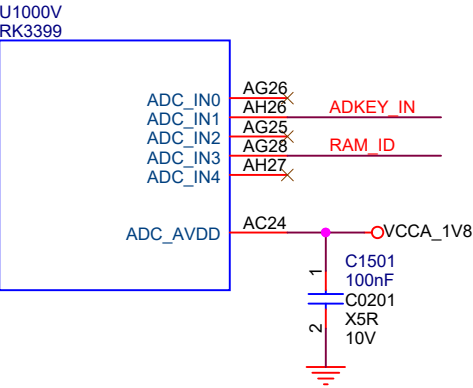
RK3399_T



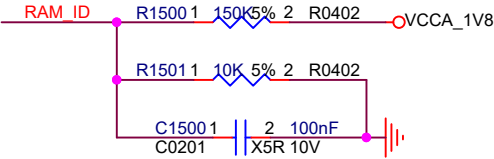
DP design rules:
1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

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RK3399_V

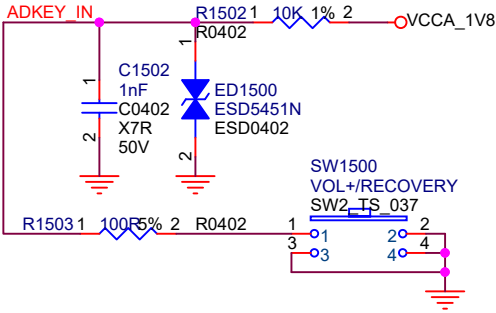


Note:All the Power filter capacitors should be placed close to the power pins of RK3399



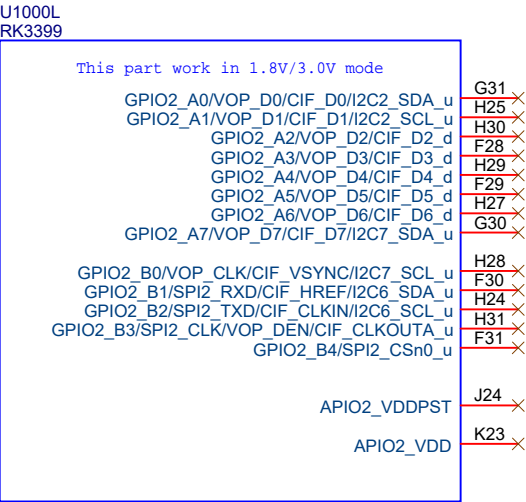
	RAM ID	R1500 PU	R1501 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K

KEY

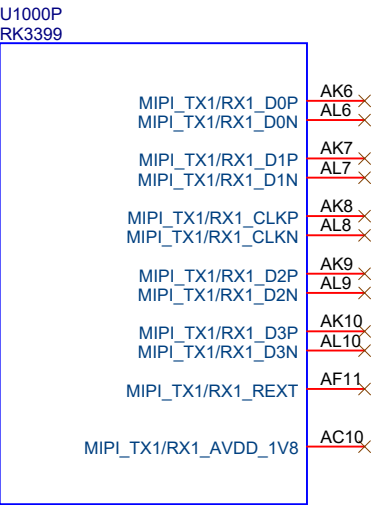


Note:
1.If ADKEY_IN=0V at power-on reset,
then system will enter into Recovery mode.
2.R1503,SW1500,ED1500 can be deleted if no need at Mass Production

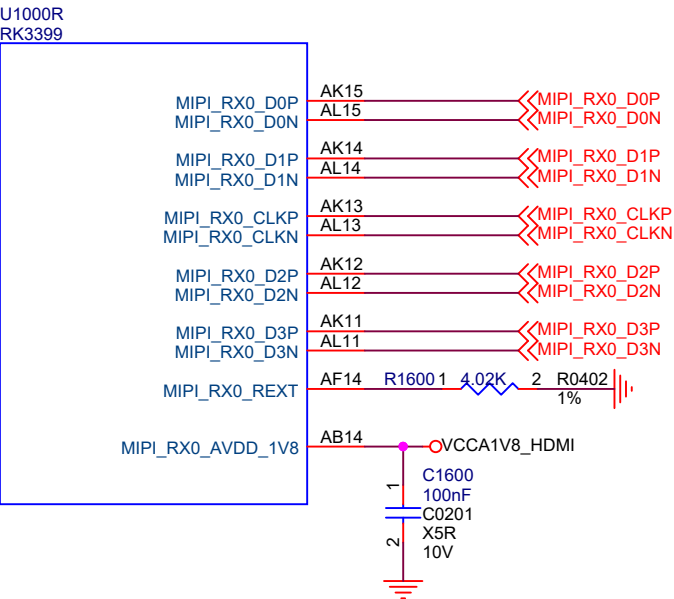
RK3399_L



RK3399_P



RK3399_R



MIPI design rules:

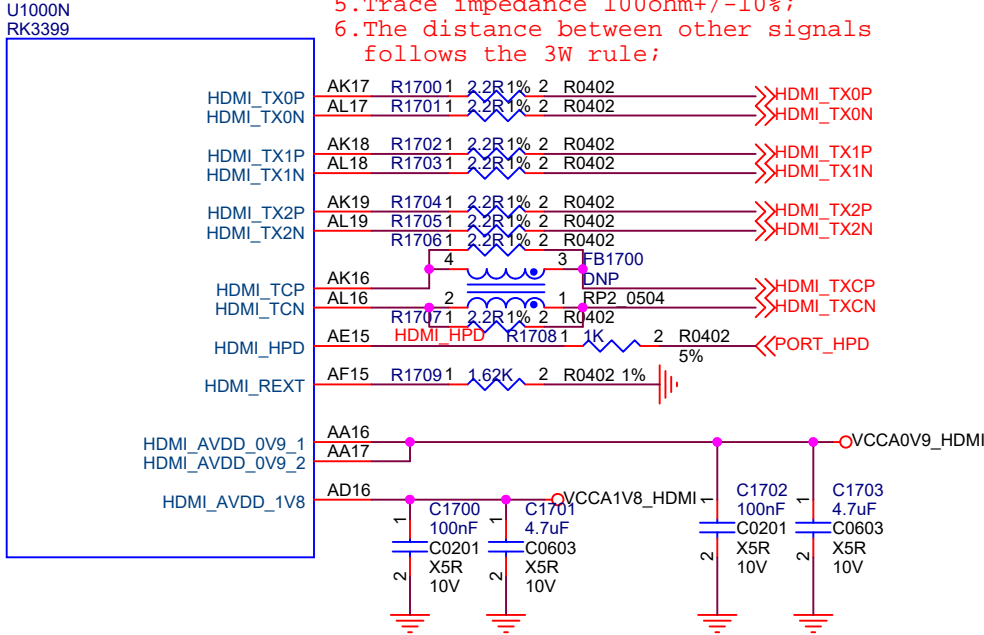
- 1.Max intra-pair skew < 4ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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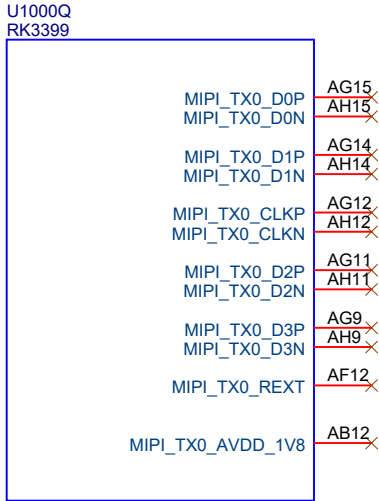
RK3399_N

HDMI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 80ps;
3.Max trace length < 9.8inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

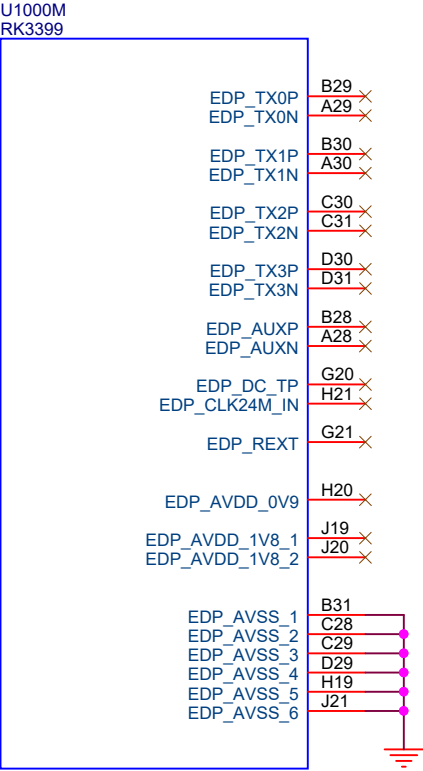


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_Q



RK3399_M

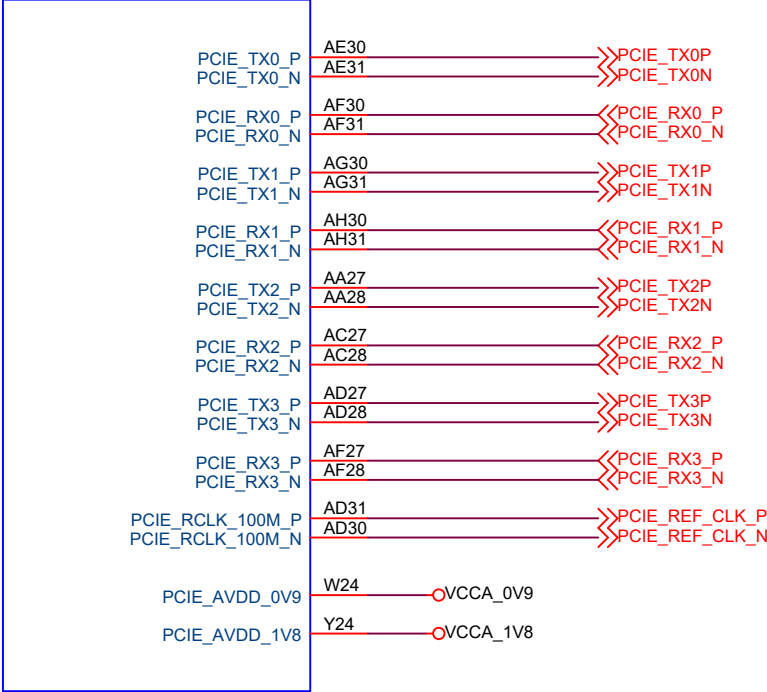


eDP design rules:
1.Max intra-pair skew <4 ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

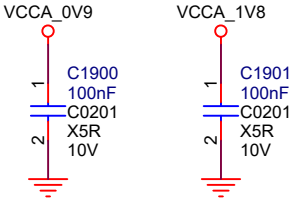
<div><div><div>Rockchip</div><div>瑞芯微电子</div></div><div>Fuzhou Rockchip Electronics</div></div>			
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RK3399_O


U10000
RK3399



PCIE design rules:
1.Max intra-pair skew < 4ps;
2.Max inter-pair skew < 1.6ns;
3.Max trace length < 14inches;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

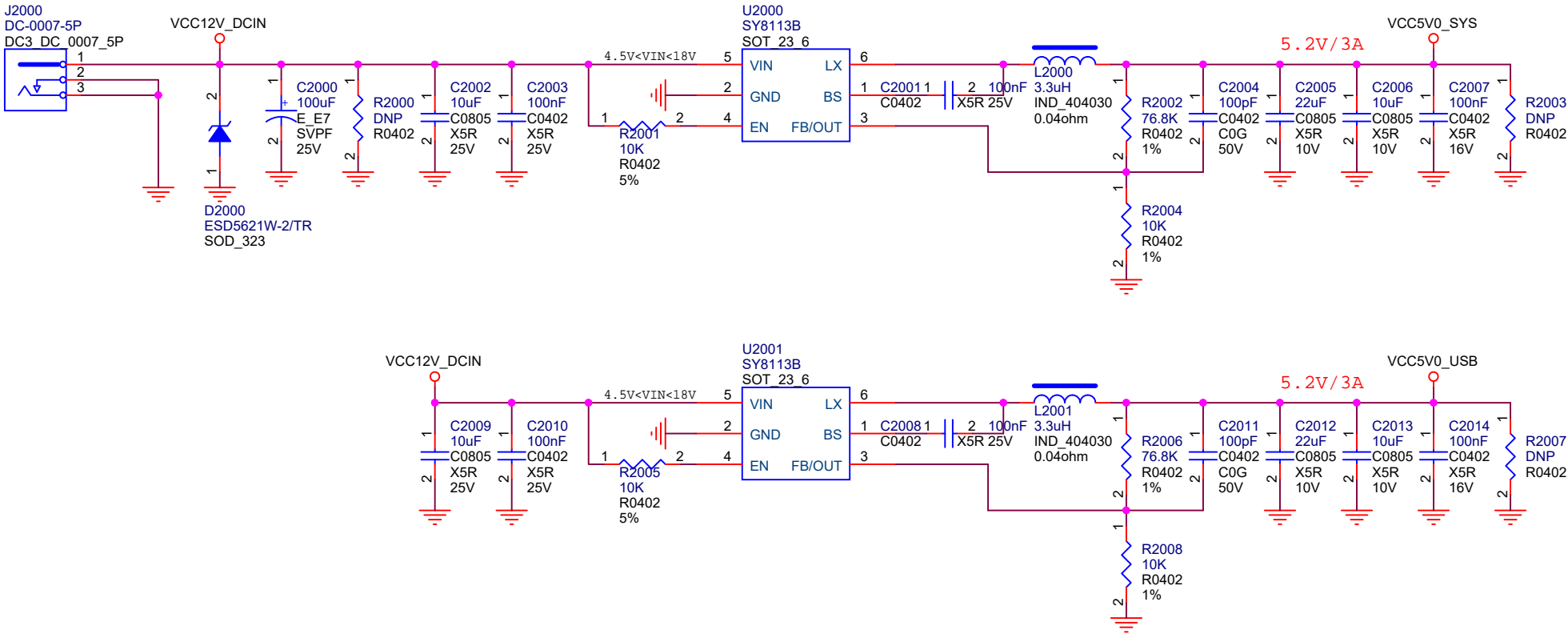


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File:	19.RK3399 PCIE		
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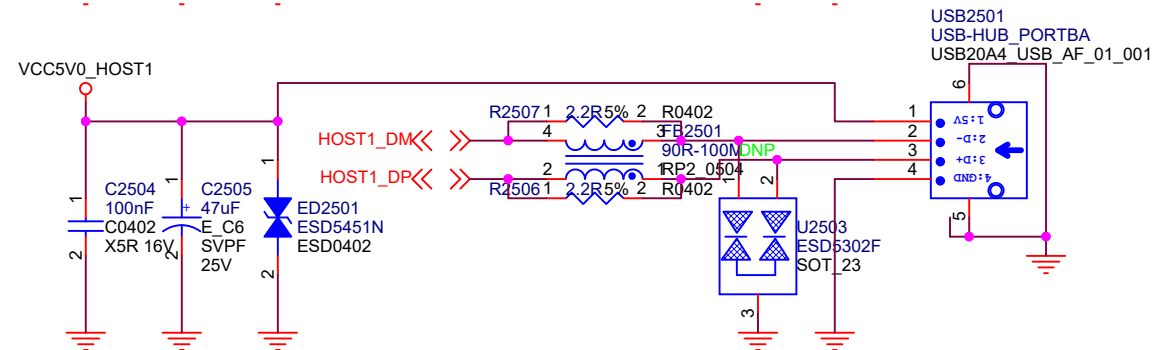
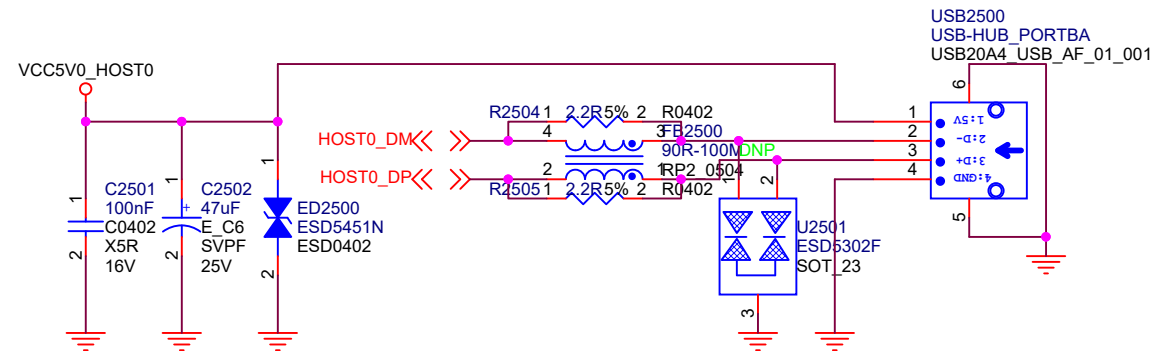
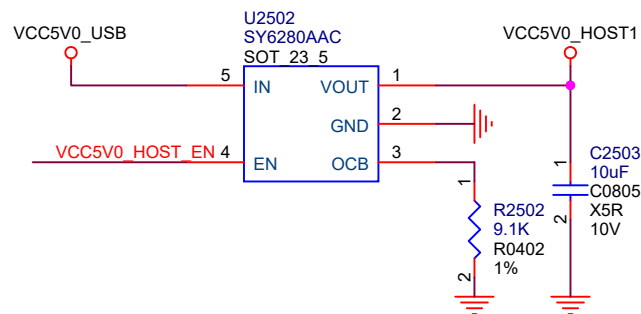
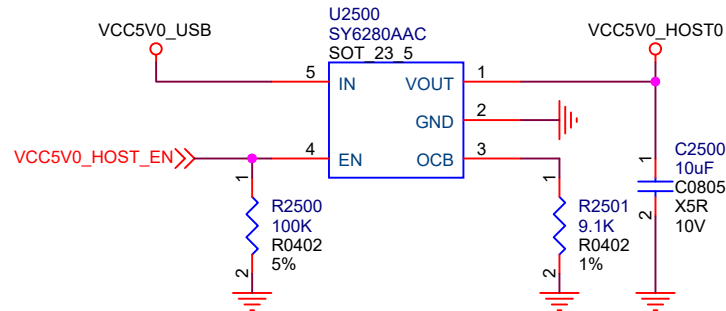
DC IN & SYSTEM Power



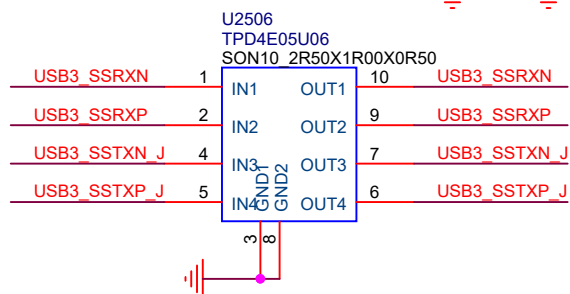
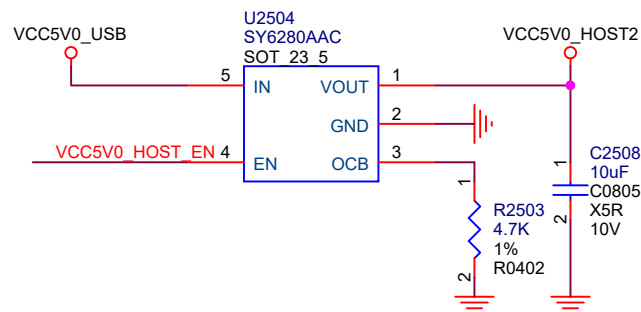
Note: If use USB3.0 HUB, U2001 must support over 3A current

<div><div>Rockchip</div><div>瑞芯微电子</div></div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	20.Power-DC IN		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	18 of 45

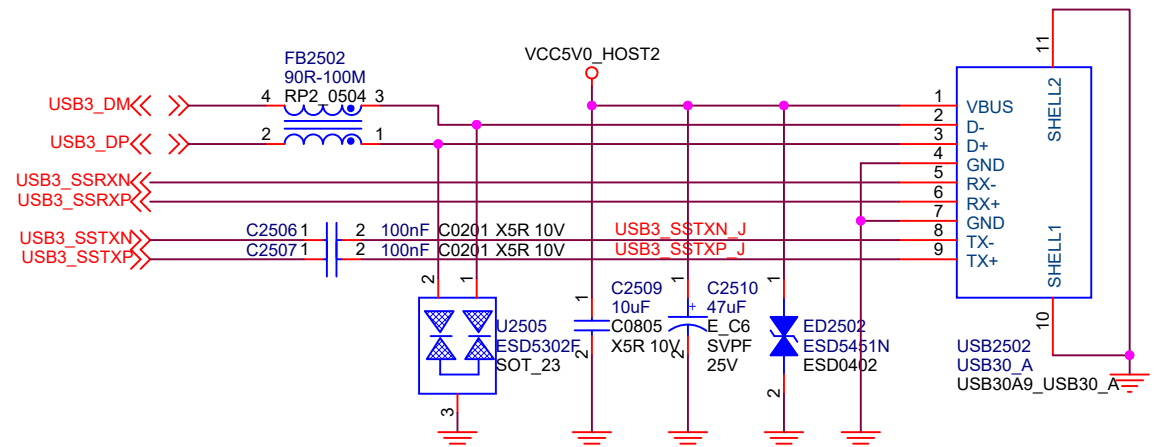
USB2.0 HOST Port



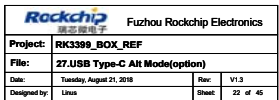
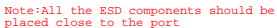
USB3.0 HOST Port



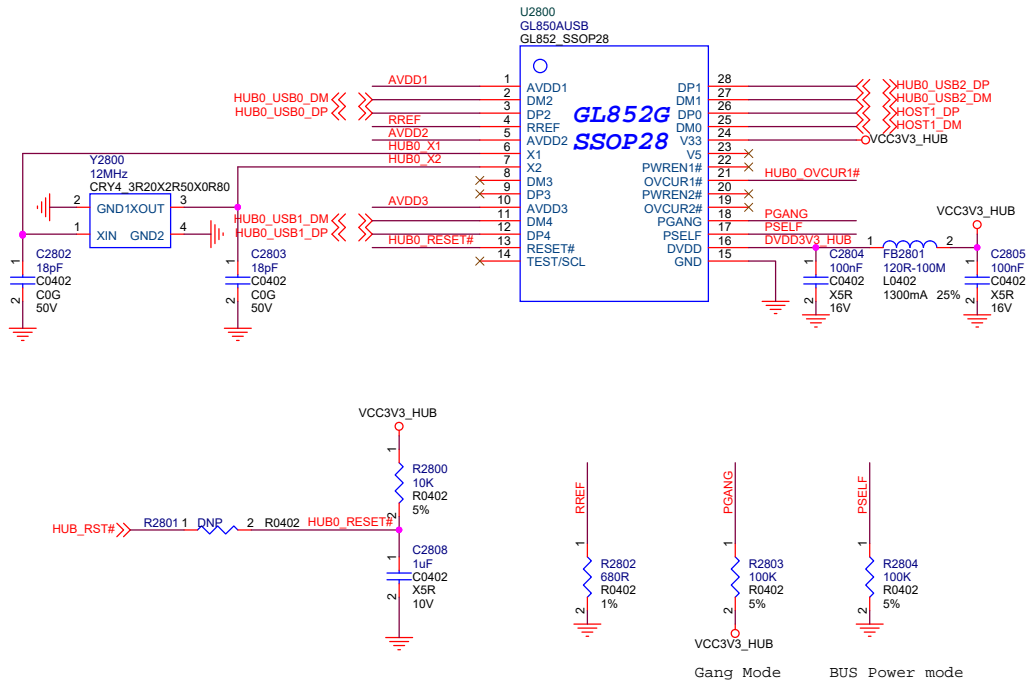
Note: All the ESD components should be placed close to the port



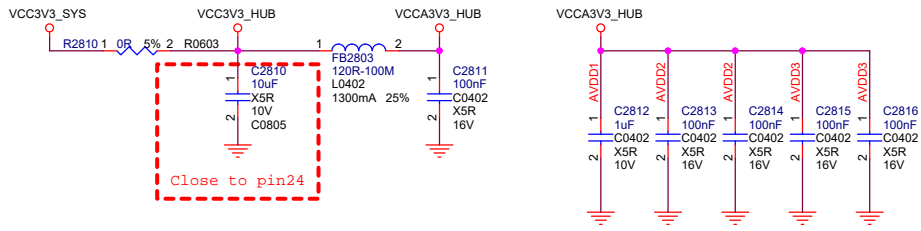
Note:USB Port for firmware download is necessary,
so it can not be deleted



USB2.0 HUB

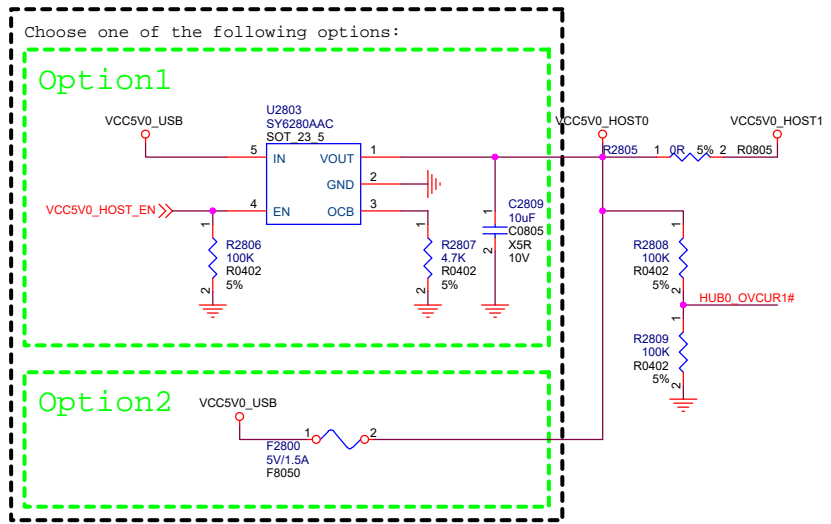
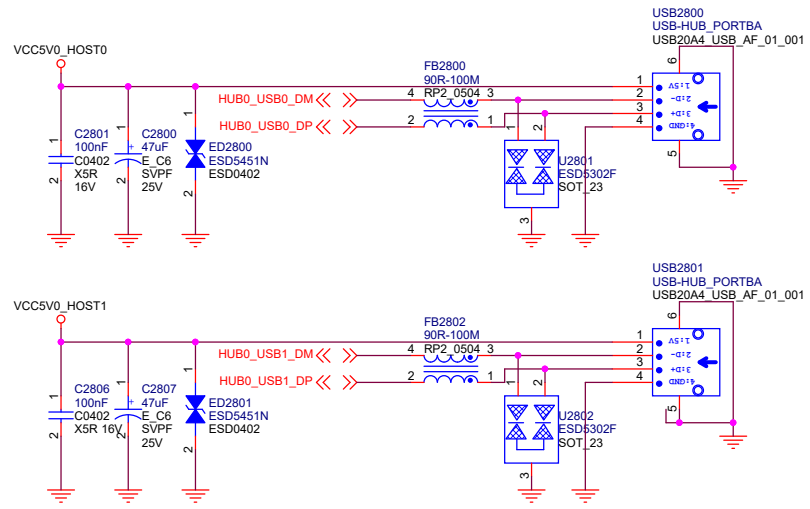


HUB Power

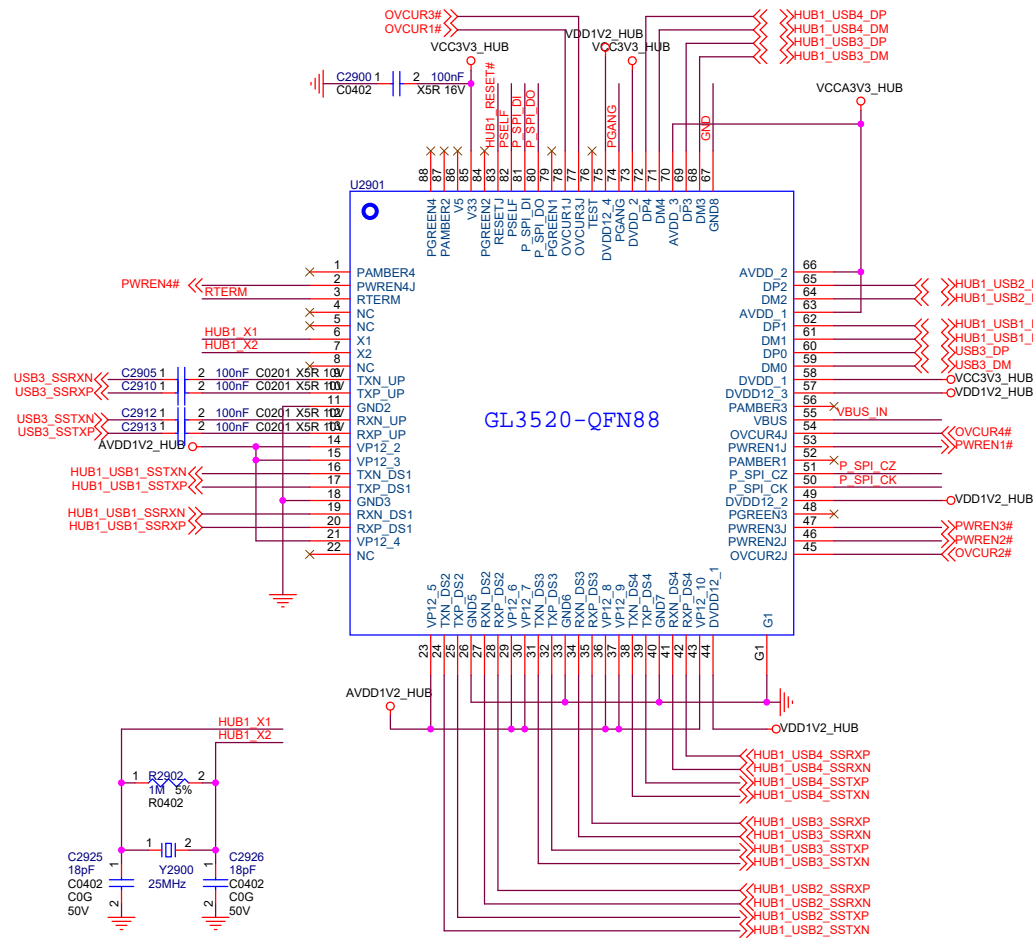


Note:All the Power filter capacitors should be placed close to the power pins of GL852G

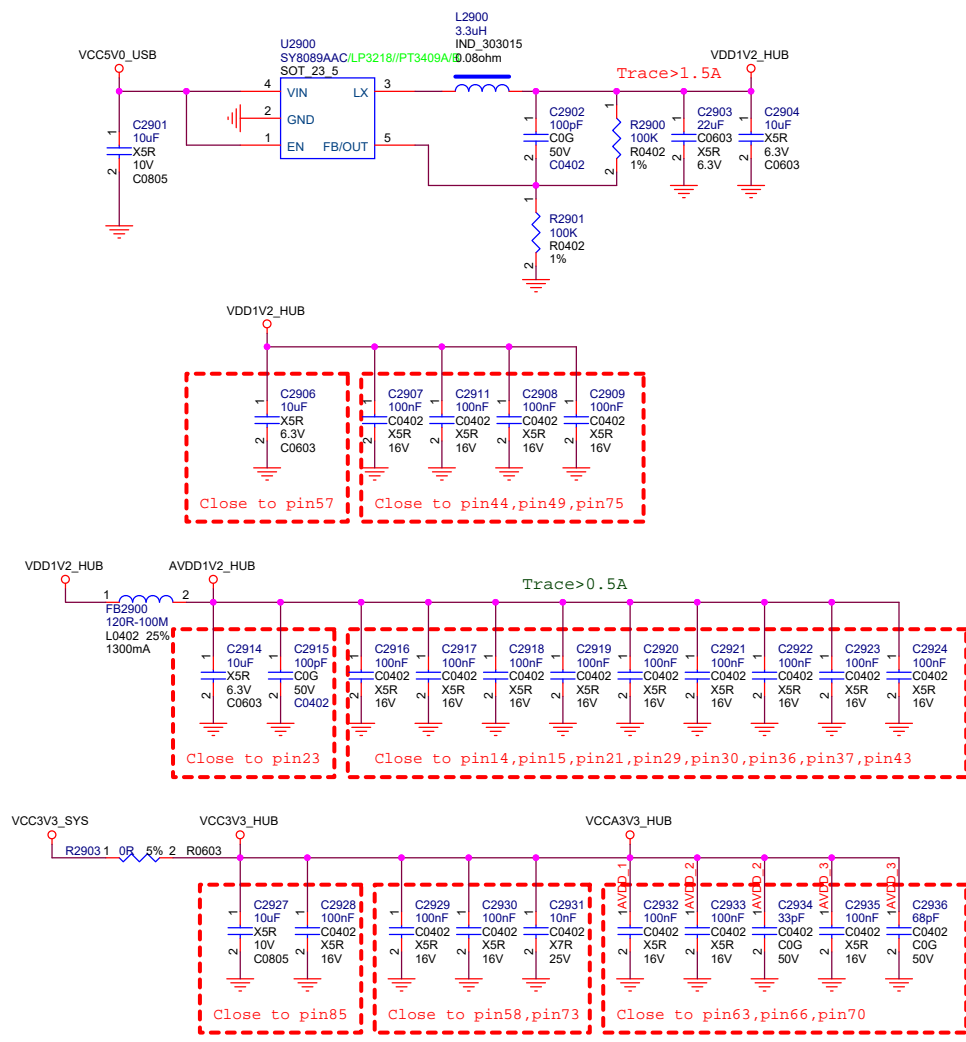
USB2.0 Port



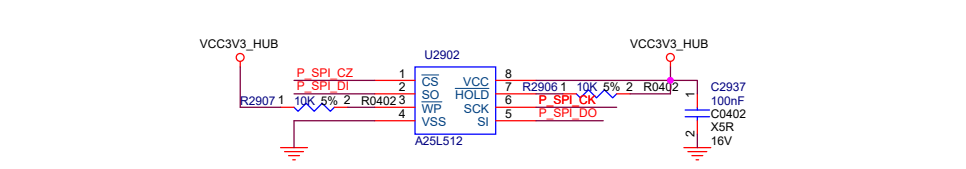
USB3.0 HUB



HUB Power



SPI Flash

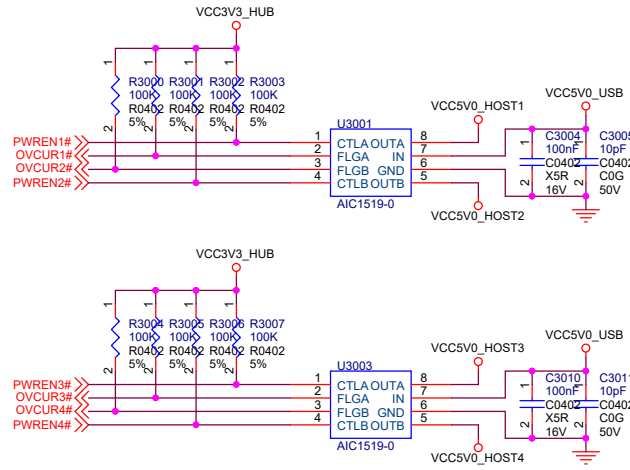


Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:		RK3399_BOX_REF	
File:		29.USB3.0 HUB-GL3523-1 (option)	
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linux	Sheet:	24 of 45

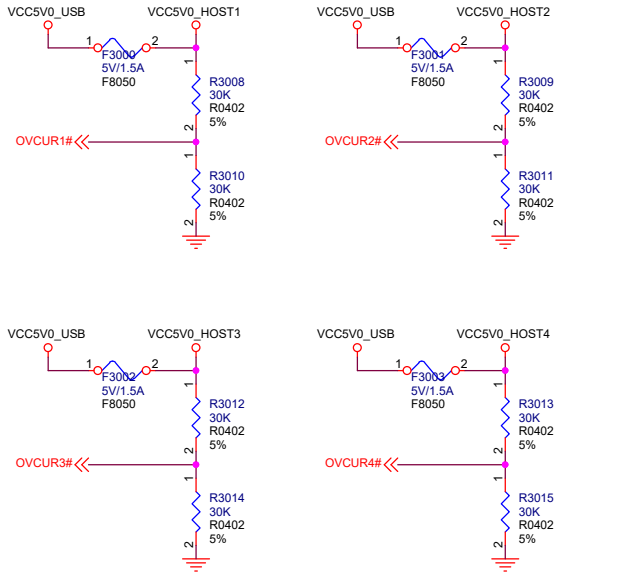
Port Power

Choose one of the following options:

Option1
Power Switch CIRCUIT

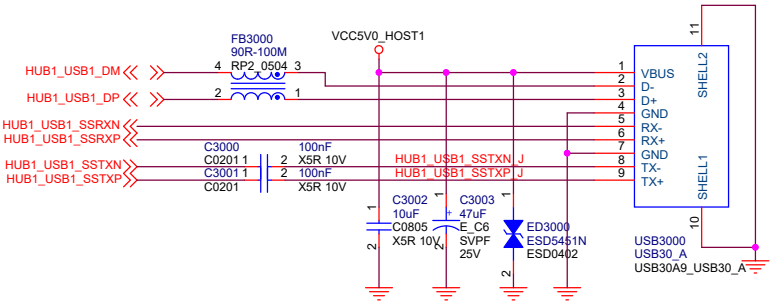
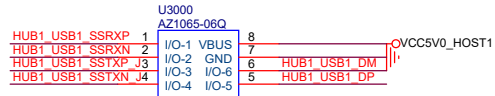


Option2
POLY-FUSE CIRCUIT

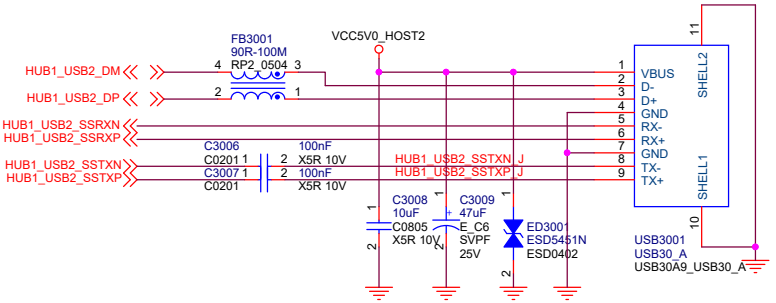
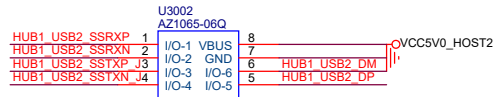


Note:OVCUR1#~4# Floating : Non-Removable (Compound device)

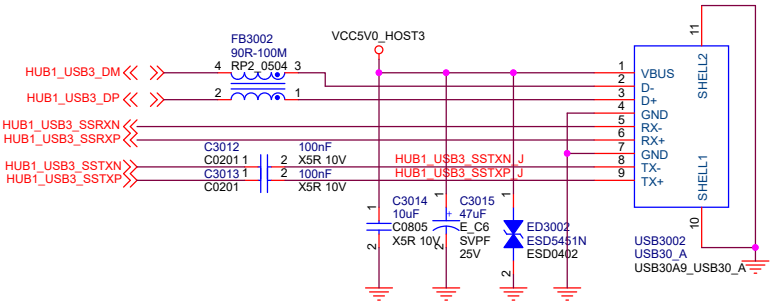
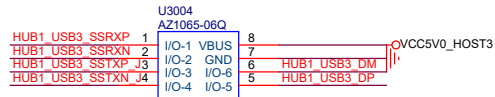
USB3.0 Port1



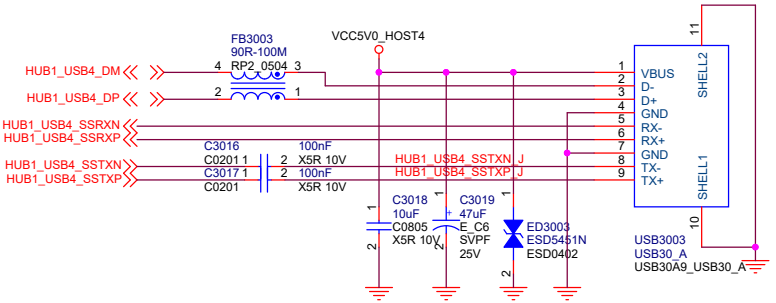
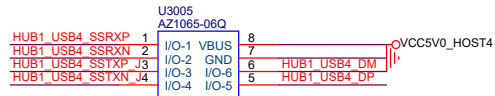
USB3.0 Port2



USB3.0 Port3

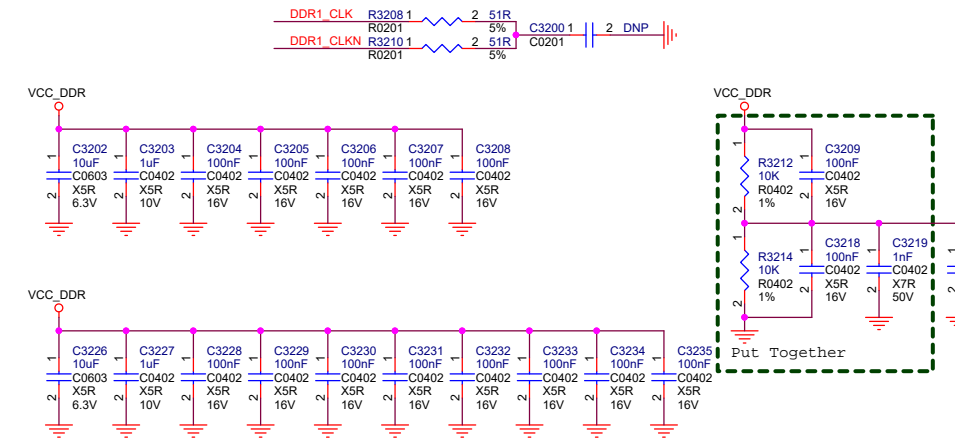
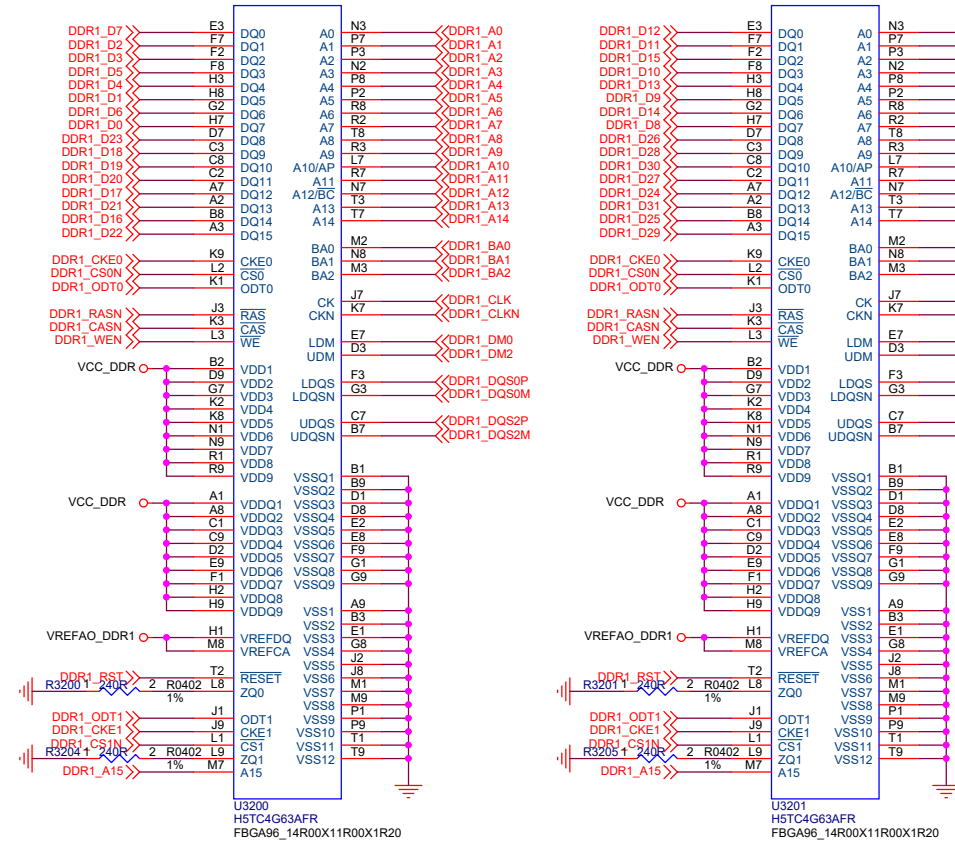


USB3.0 Port4

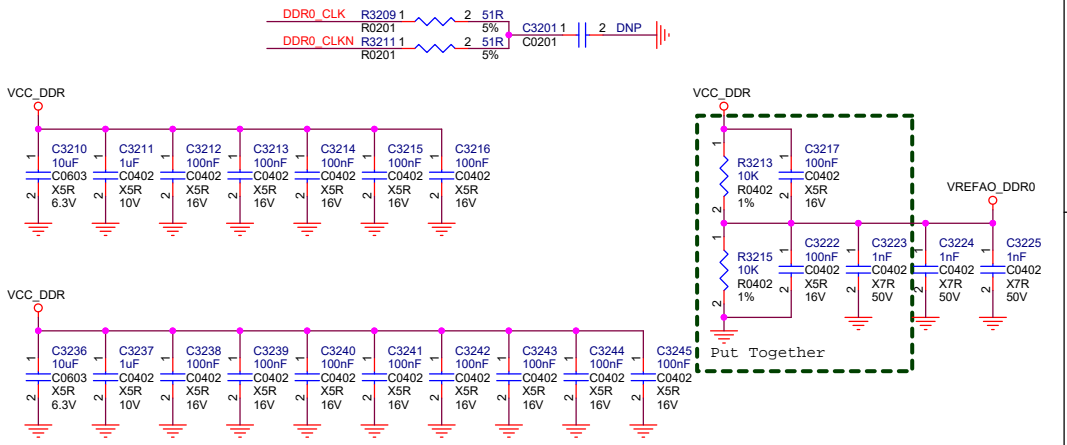
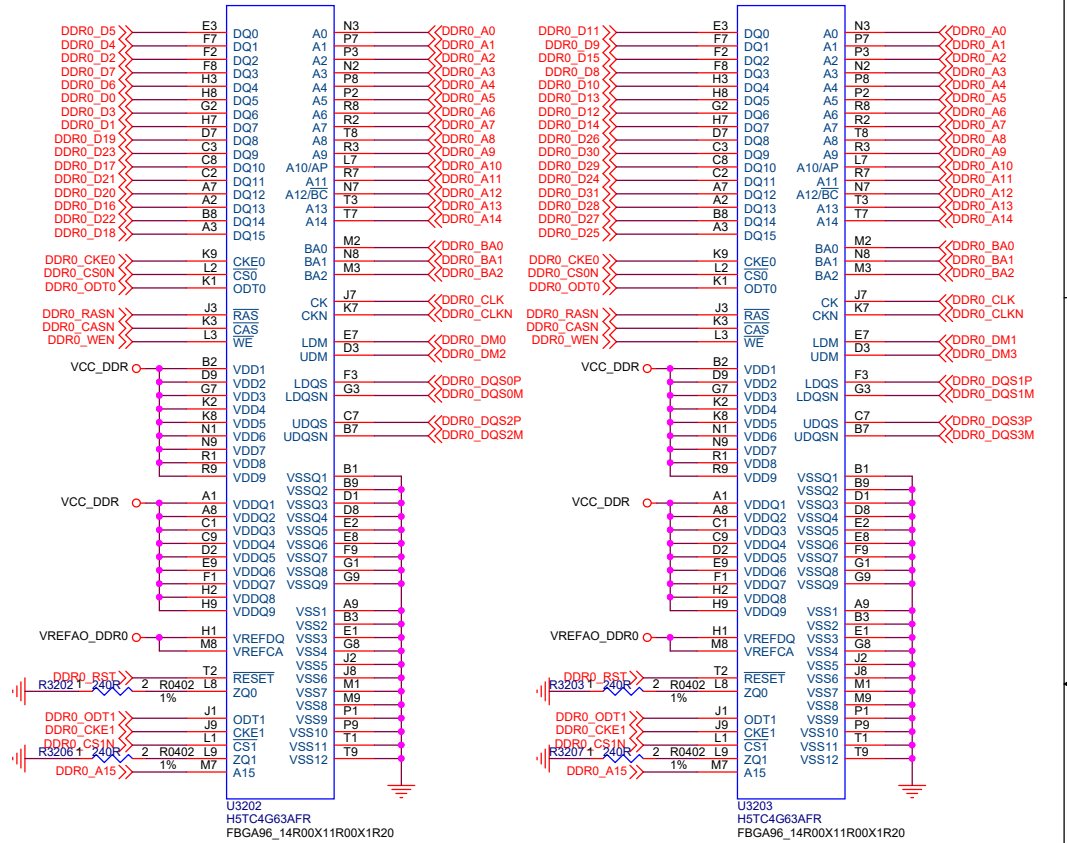


DDR3 4x16bit

Note:The simulation frequency of the template is 800MHz.
Remind: Refer to the latest AVL for parts selection.



Note:All the Power filter capacitors should be placed close to the power pins of DDR

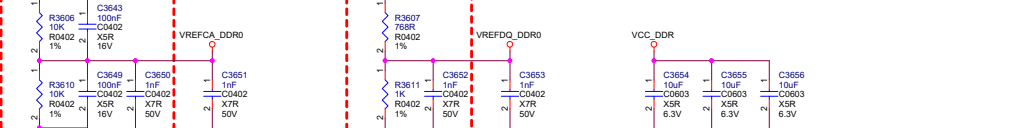
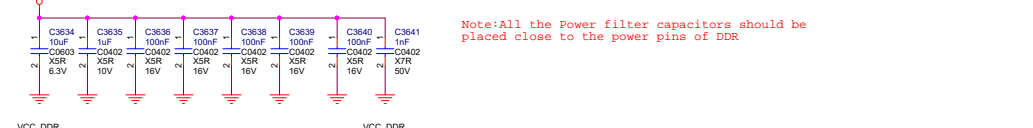
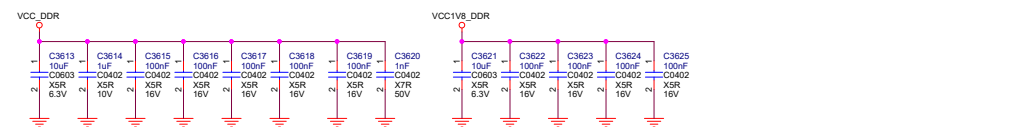
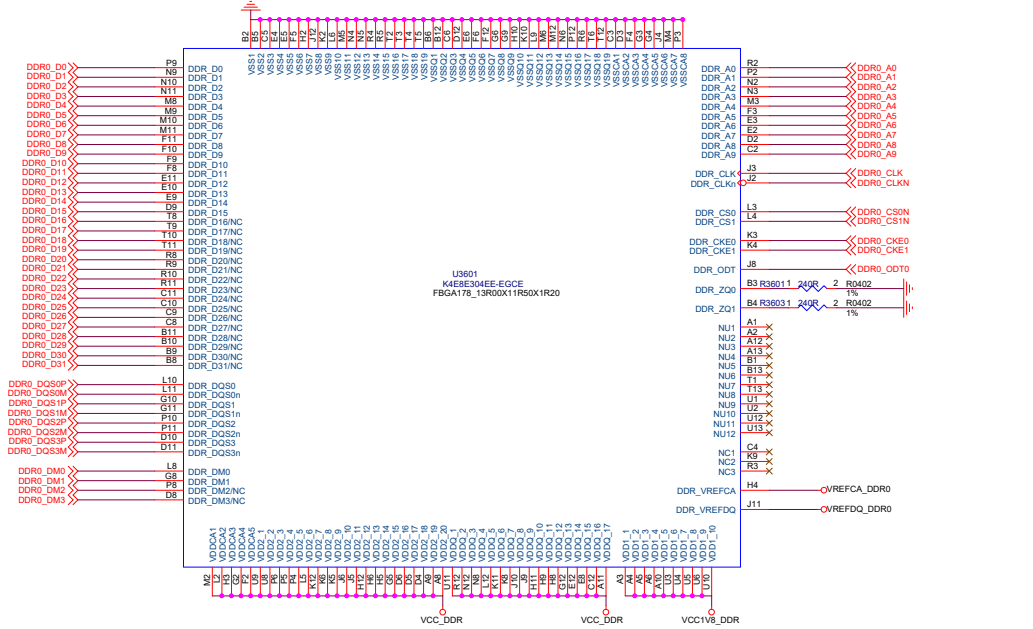
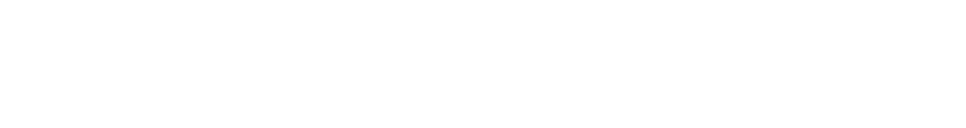
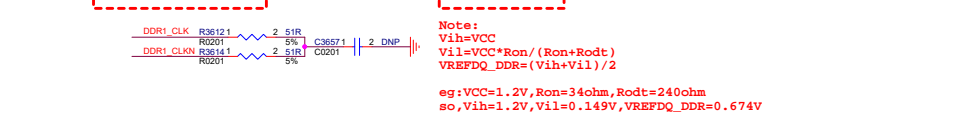
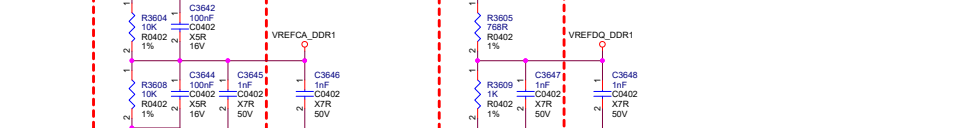
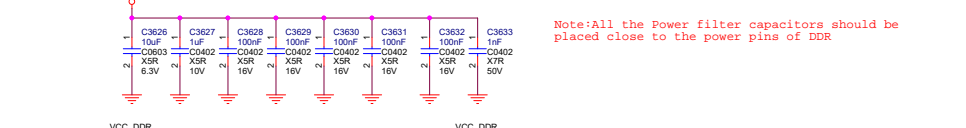
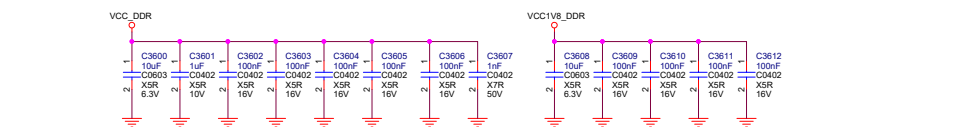
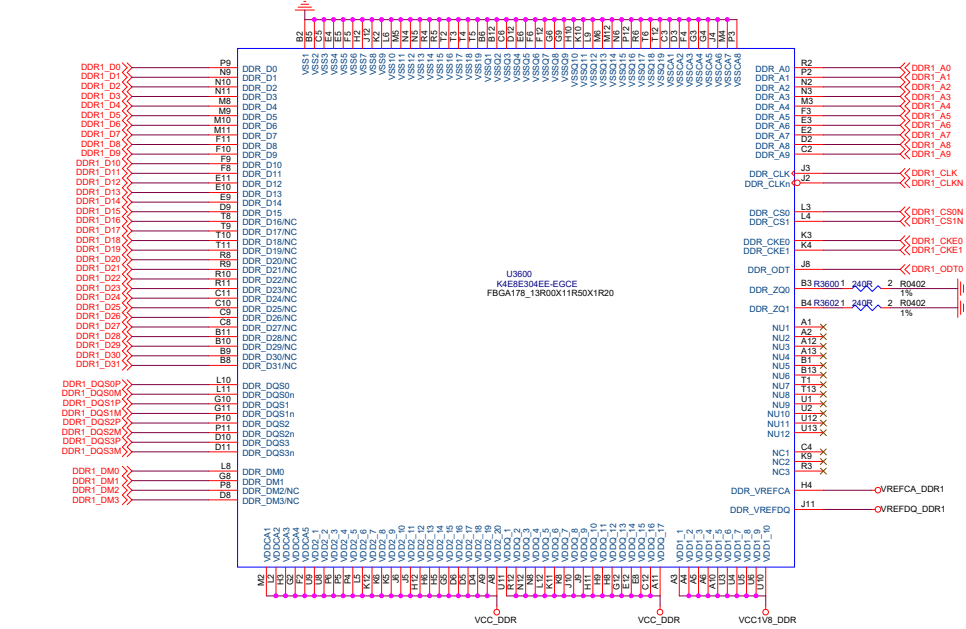


Note:All the Power filter capacitors should be placed close to the power pins of DDR

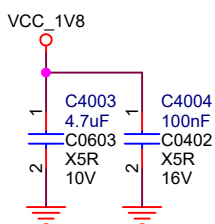
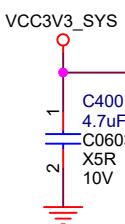
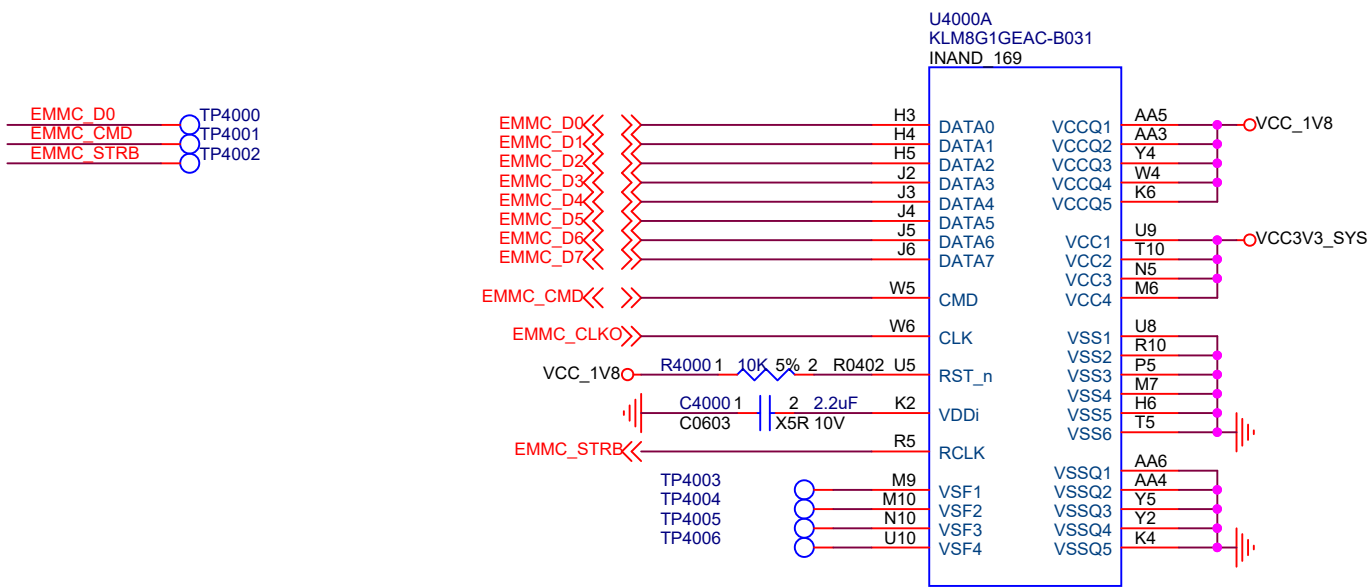
LPDDR3 2x32bit 178ball1

Note:The simulation frequency of the template is 800MHz.

Remind: Refer to the latest AVL for parts selection.



eMMC FLASH



Note: All the Power filter capacitors should be placed close to the power pins of eMMC

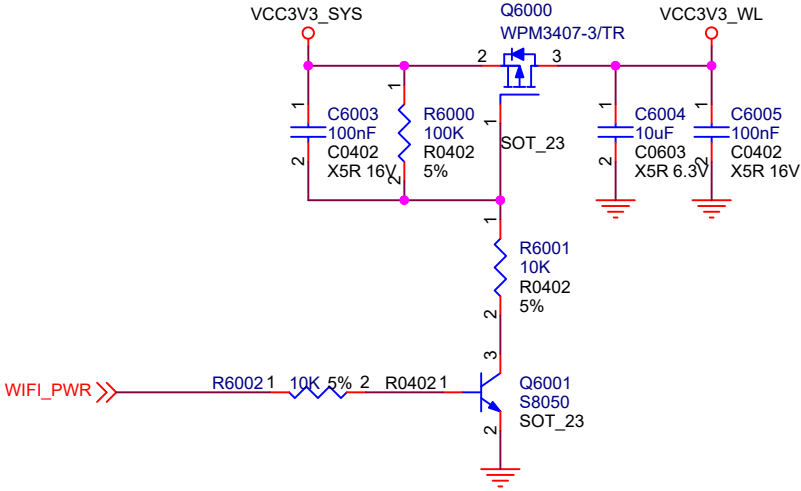
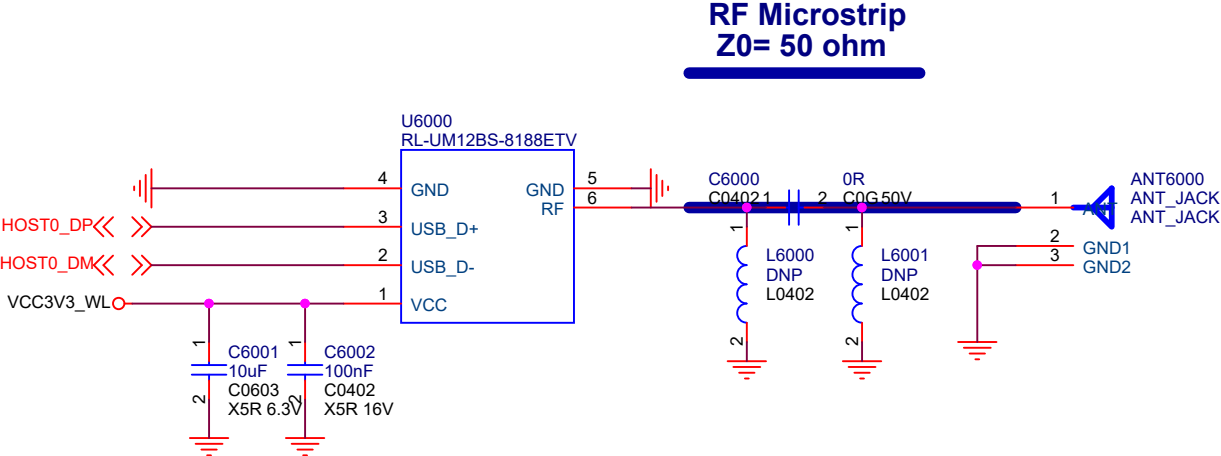
Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.


EMMC_CLKO TP4007

TP4008

<div><div>Rockchip</div><div>瑞芯微电子</div></div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	40.Memory-eMMC		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	28 of 45

USB WIFI MODULE





Fuzhou Rockchip Electronics

瑞芯微电子

Project:	RK3399_BOX_REF		
File:	60.WIFI-USB (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	29 of 45

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

	Option1	Option2	Option3	
AP6212	26MHz	NO	NO	
AP6330	26MHz	NO	NO	
AP6335	37.4MHz	YES	YES	ac
XZ3660	26MHz	NO	NO	

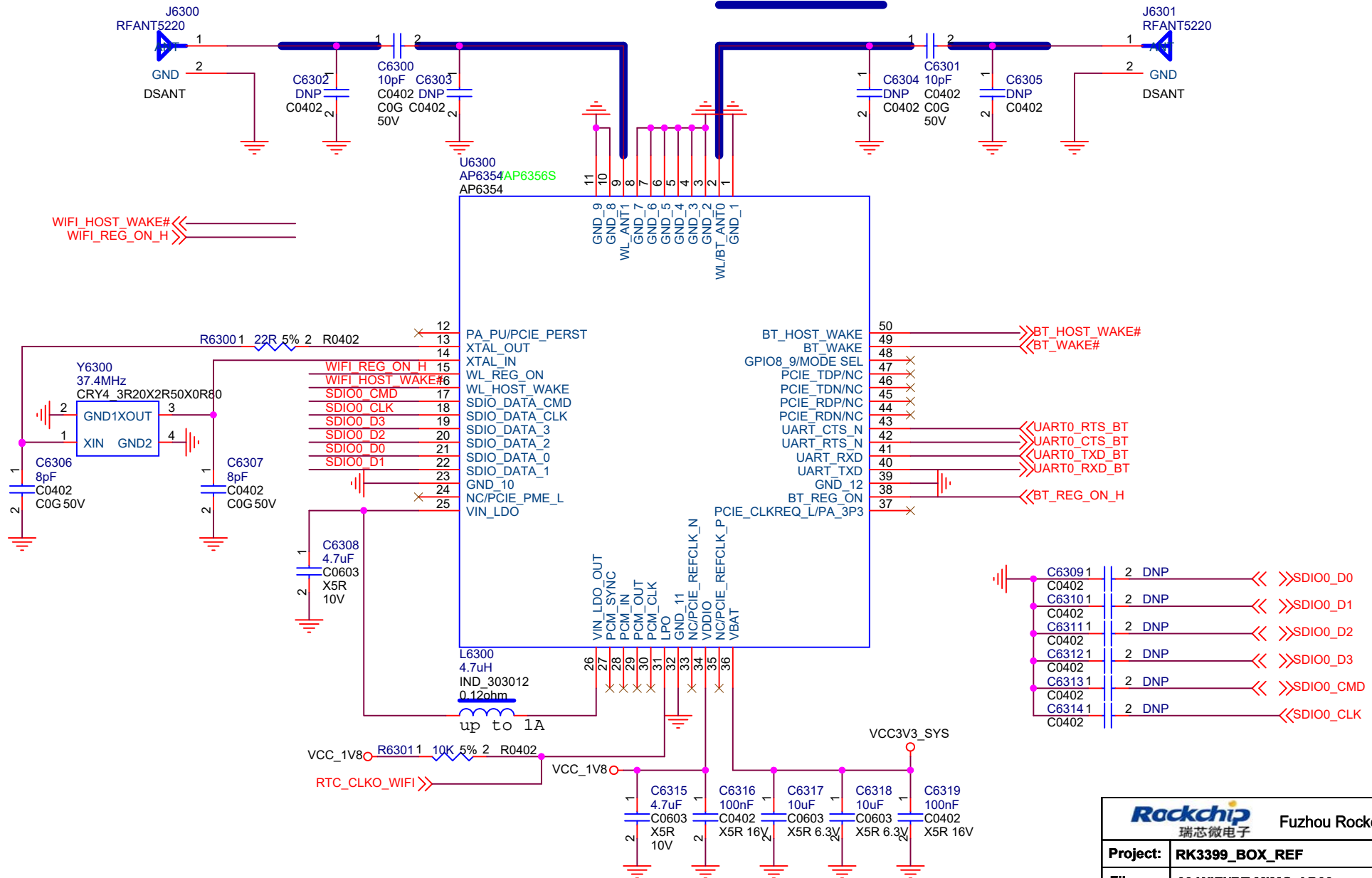


Signal	Pin	Device	Value
SDIO0_D0	C6106	1	2 5.6pF
	C0402		C0G 50V
SDIO0_D1	C6107	1	2 5.6pF
	C0402		C0G 50V
SDIO0_D2	C6108	1	2 5.6pF
	C0402		C0G 50V
SDIO0_D3	C6111	1	2 5.6pF
	C0402		C0G 50V
SDIO0_CMD	C6112	1	2 5.6pF
	C0402		C0G 50V
SDIO0_CLK	C6113	1	2 5.6pF
	C0402		C0G 50V

SDIO WIFI/BT MODULE-MIMO

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.

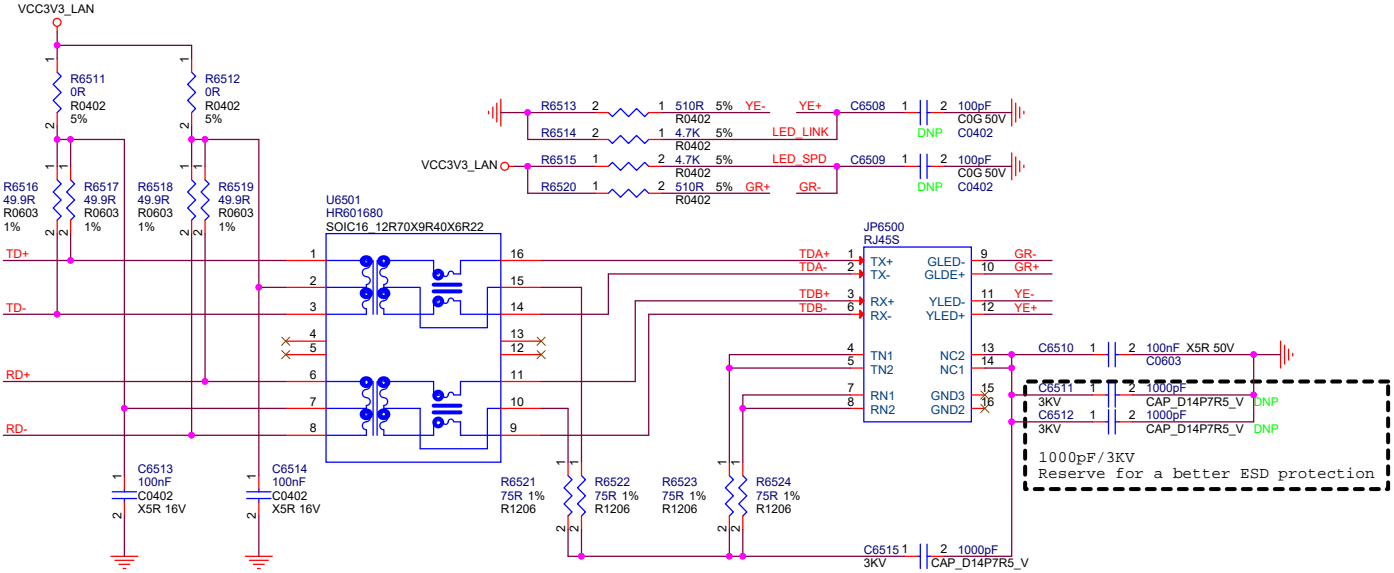
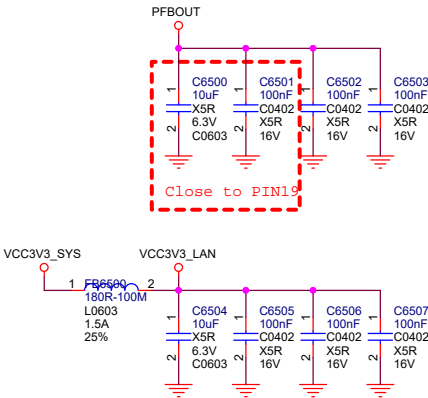
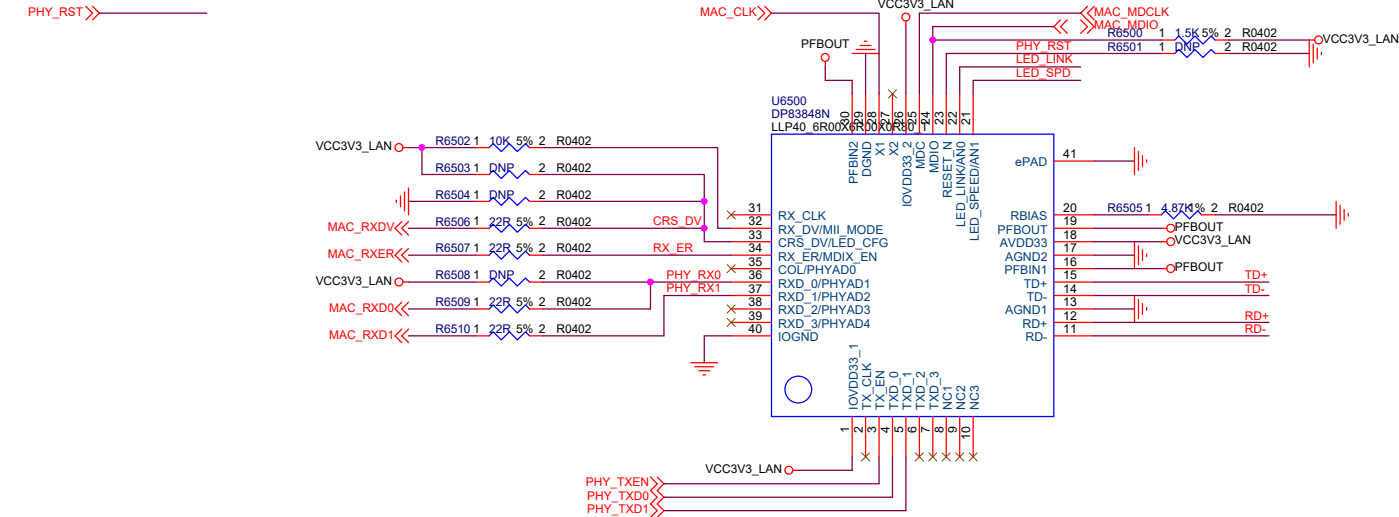
RF Microstrip
Z0= 50 ohm



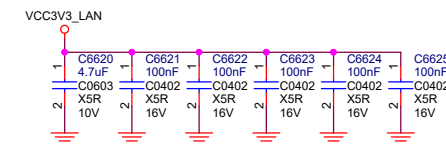
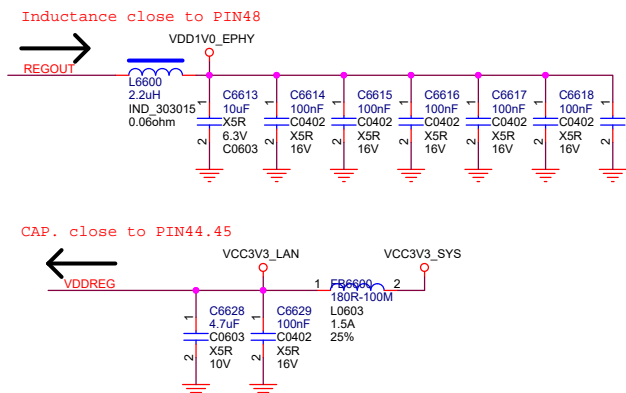
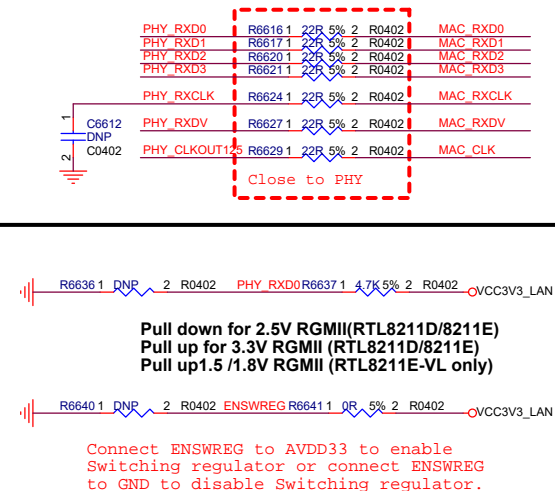
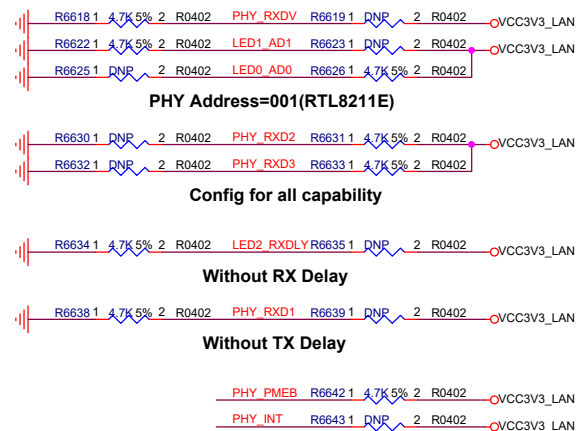
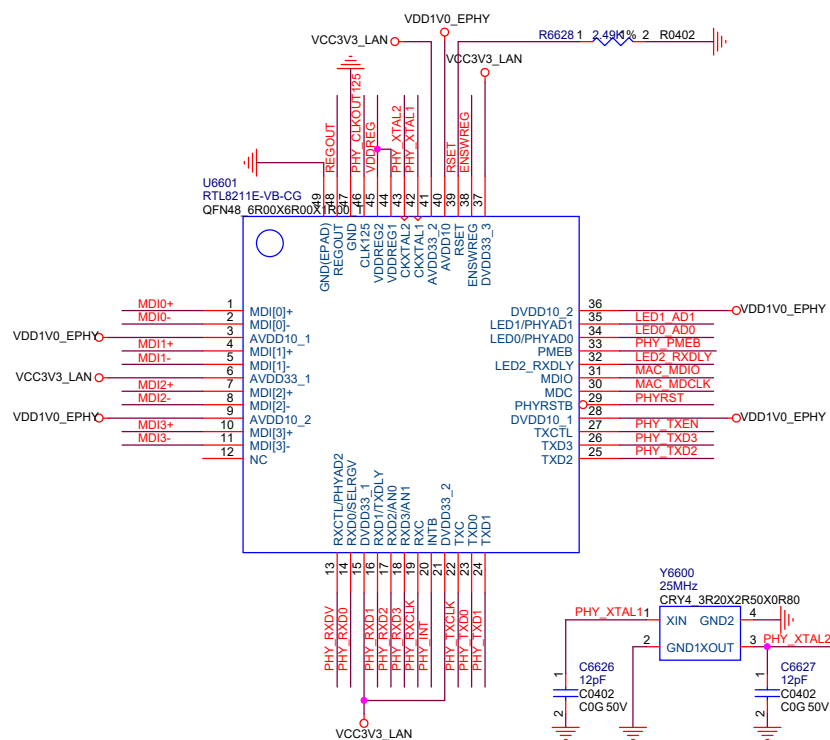
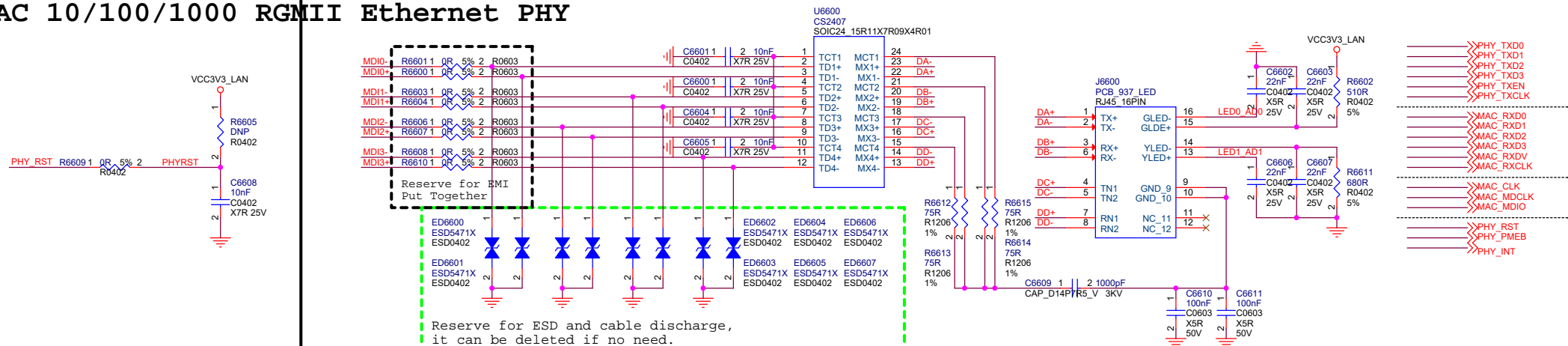
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399_BOX_REF		
File:	63.WIFI/BT MIMO-AP63xx		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	31 of 45

EMAC 10/100 MII Ethernet PHY

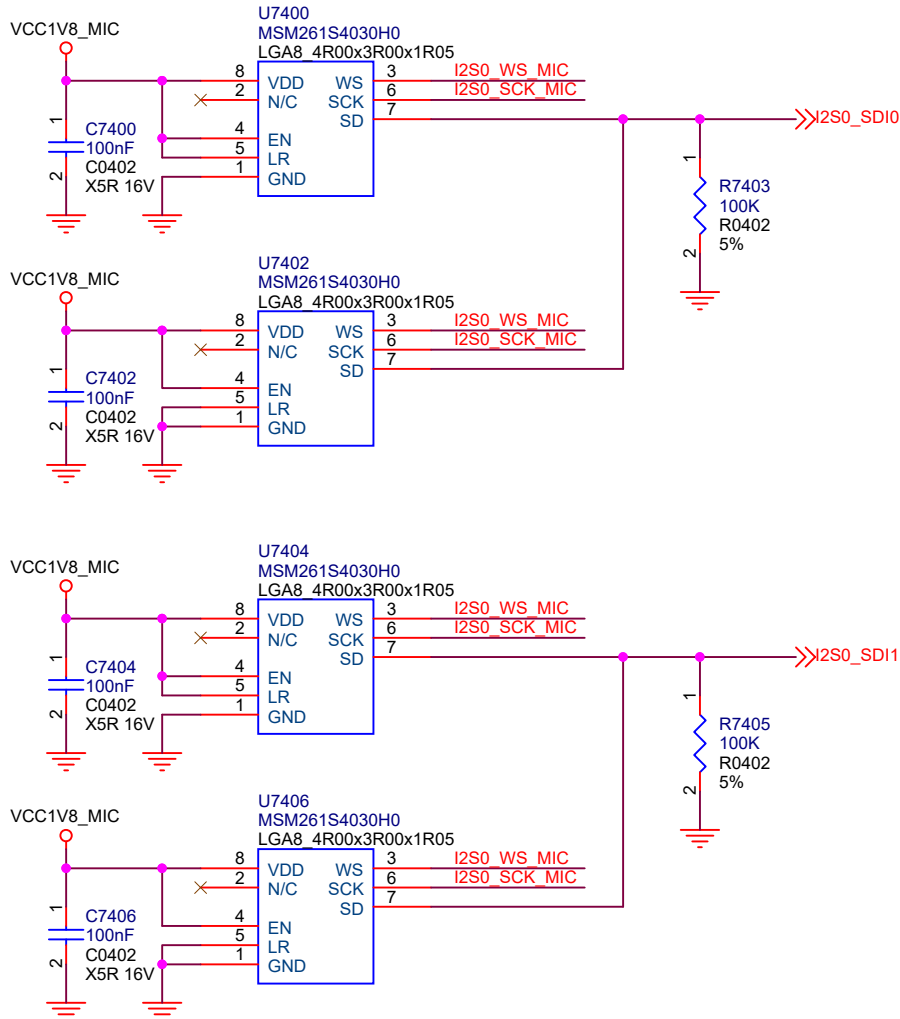
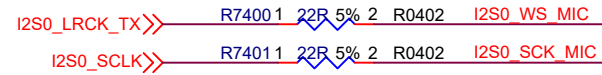
Power



GMAC 10/100/1000 RGMII Ethernet PHY

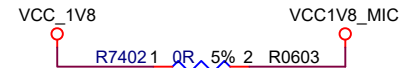


Microphone Array

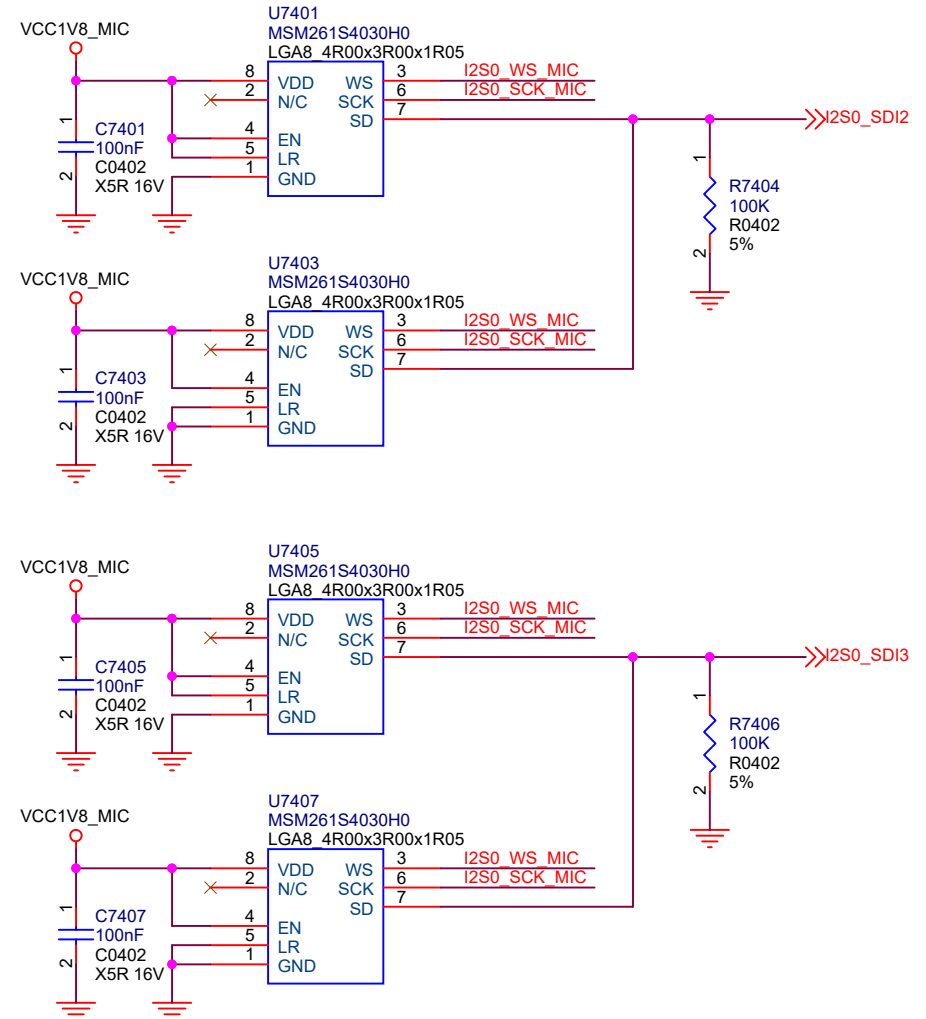



Note: The SDI line should have a 100kohm PD resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.

Power



Note:
If it have the audio daughter board,
please use independent power
supply replace.



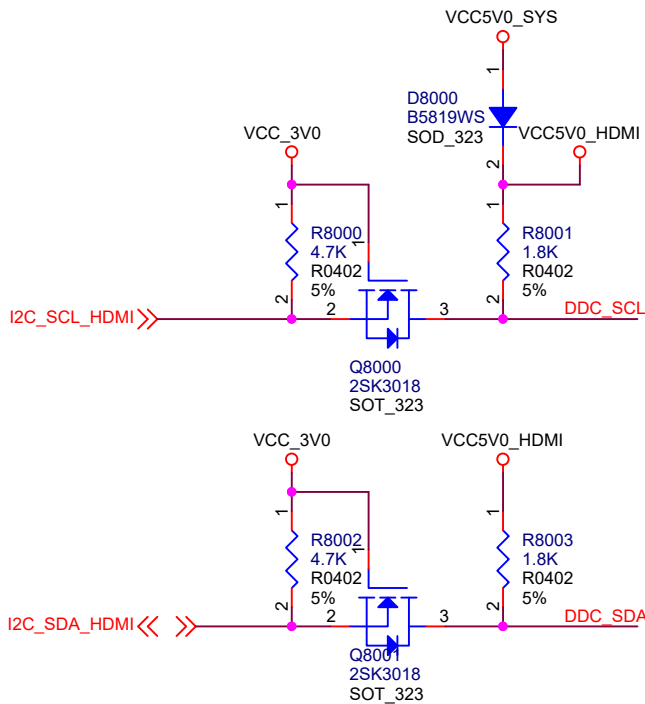
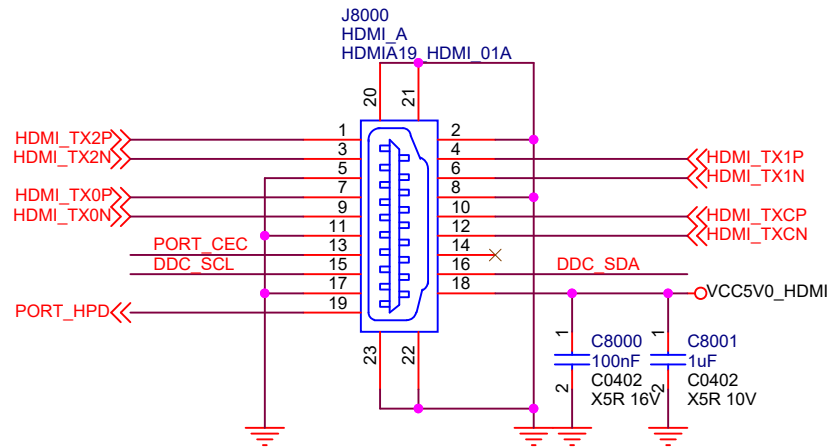


瑞芯微电子

Fuzhou Rockchip Electronics

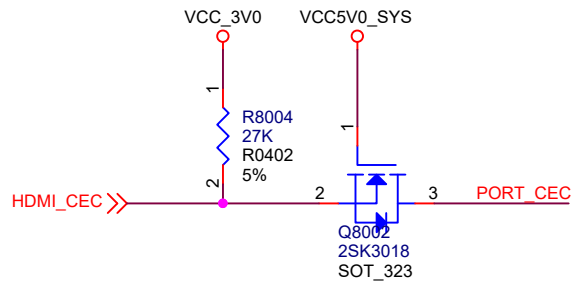
Project:	RK3399_BOX_REF		
File:	74.Microphone Array		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	35 of 45

HDMI Output



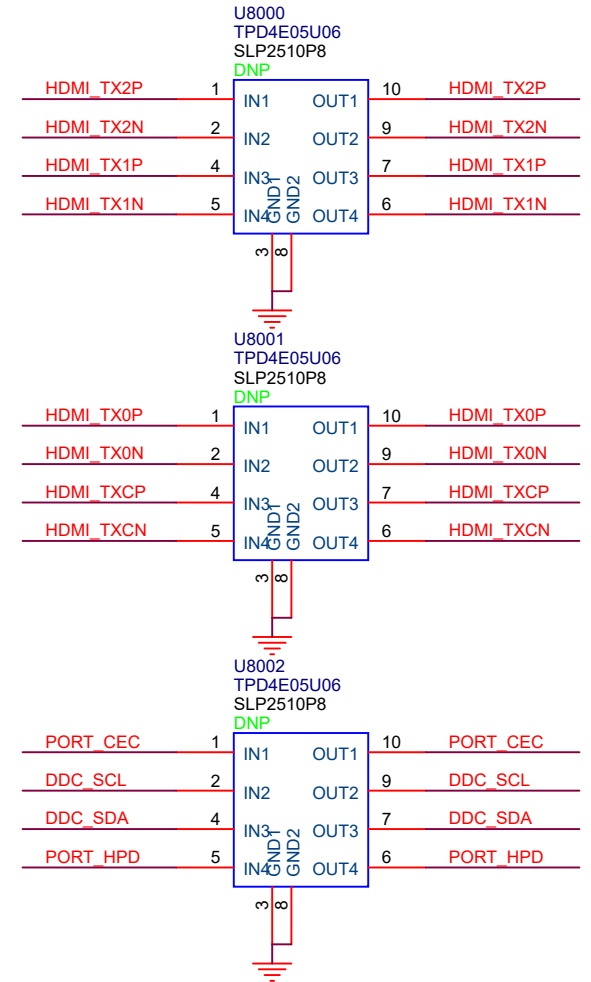
Option

Use for HDMI CEC function,
it can be deleted if no need;



ESD

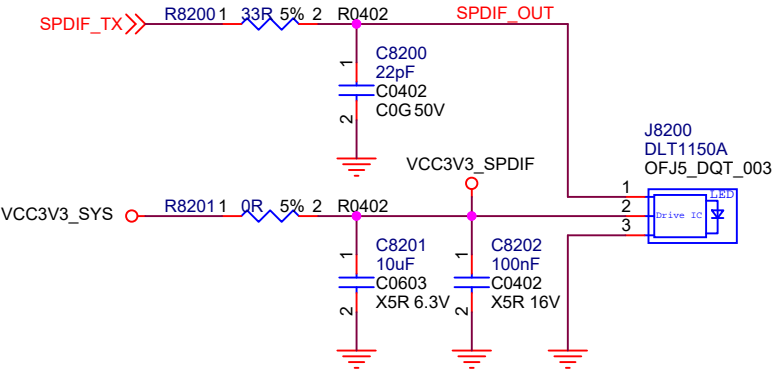
Note: All the ESD components should be placed close to the port and $C_j \leq 0.4\text{pF}$




Fuzhou Rockchip Electronics

Project:	RK3399_BOX_REF		
File:	80.HDMI Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	36 of 45

SPDIF OUT





瑞芯微电子

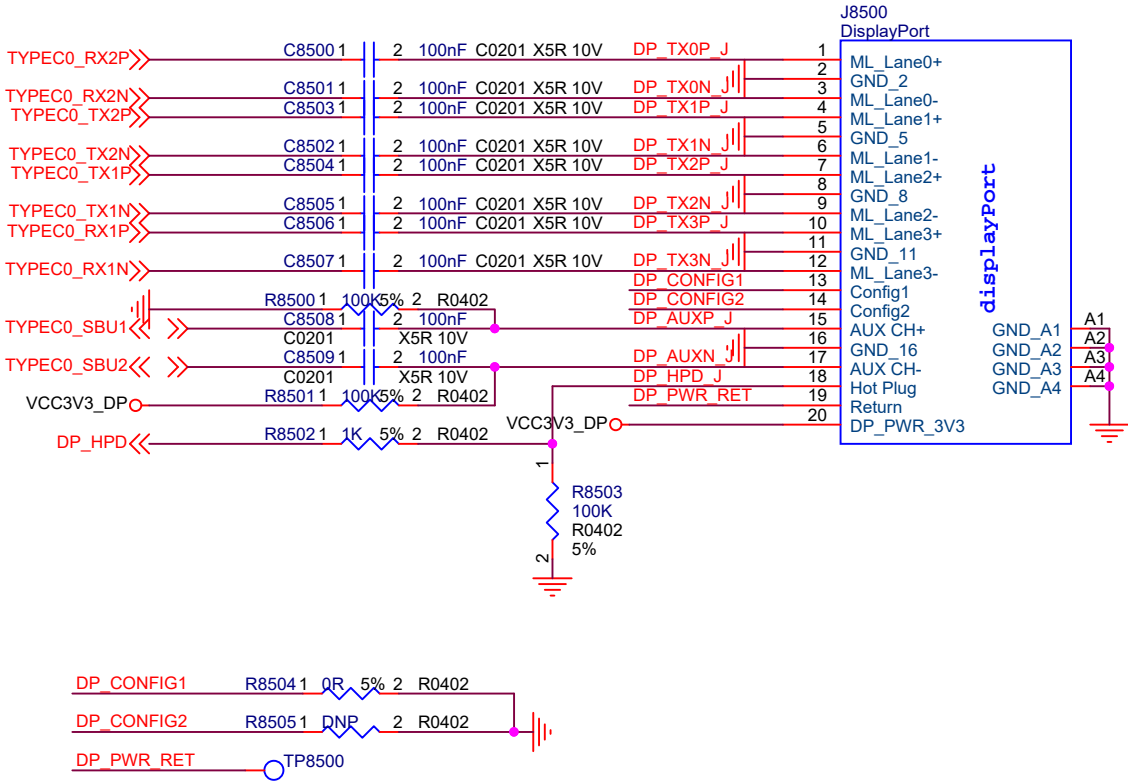
Fuzhou Rockchip Electronics

Project:	RK3399_BOX_REF		
File:	82.SPDIF Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	38 of 45

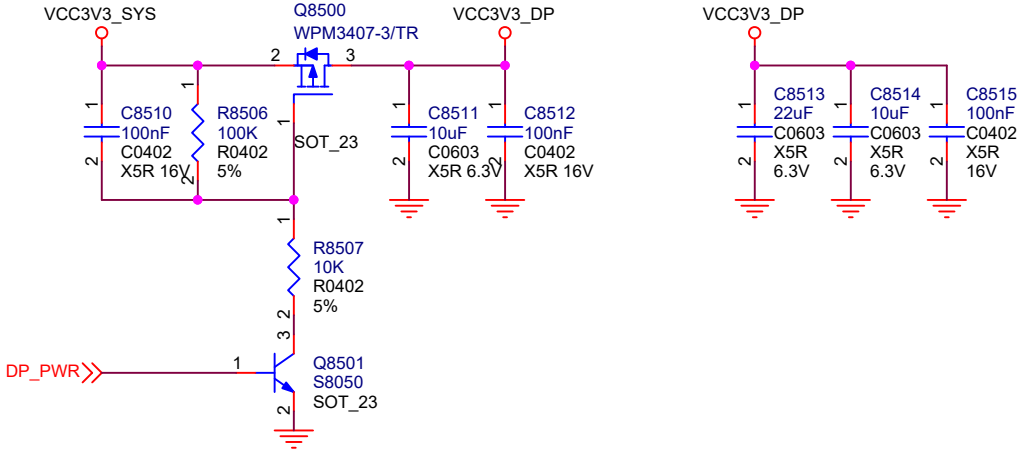
39 of 45

Sheet:	40 of 45
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DP Output

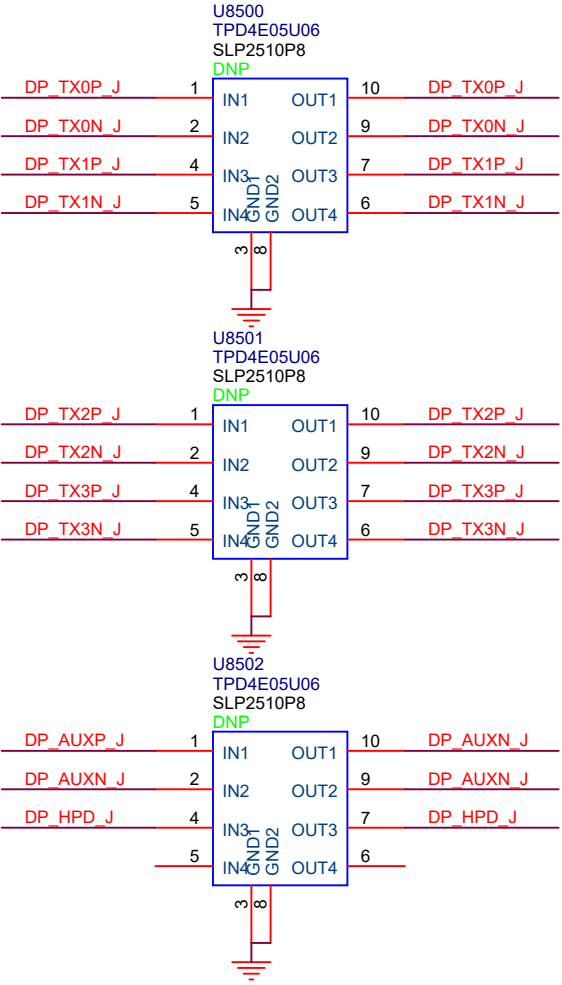


Power



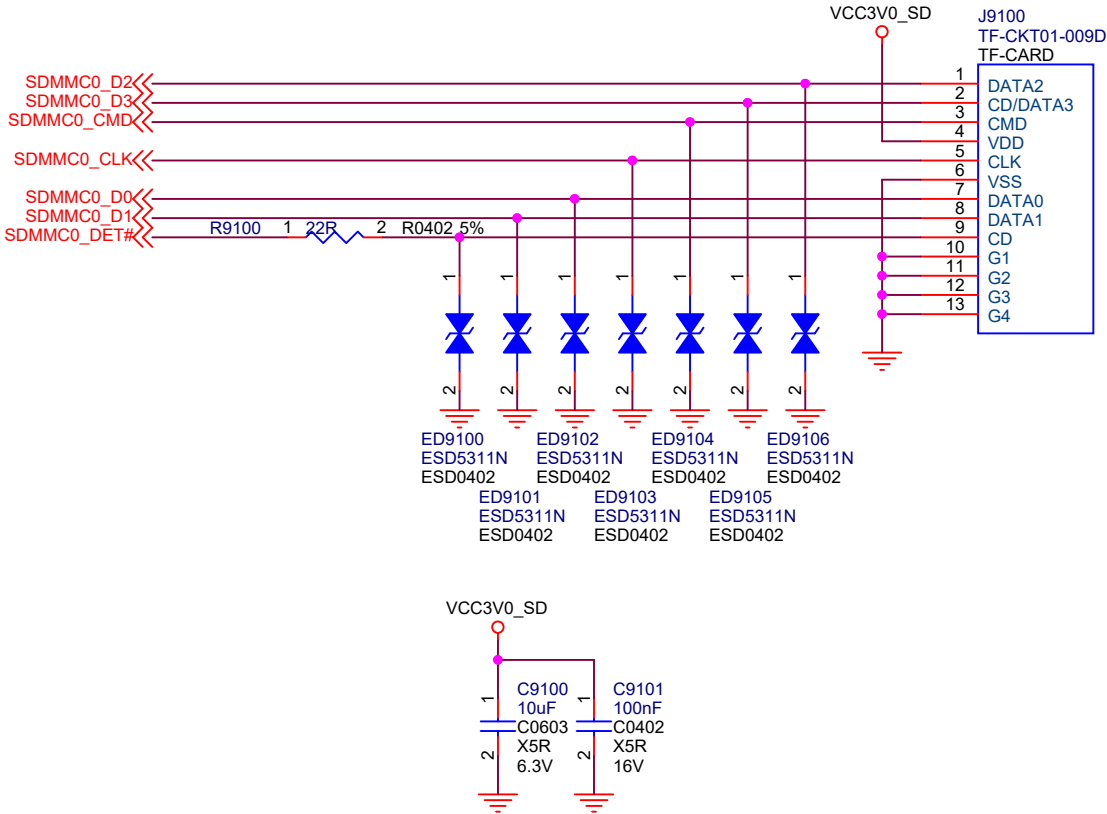
ESD

Note: All the ESD components should be placed close to the port and $C_j \leq 0.4\text{pF}$

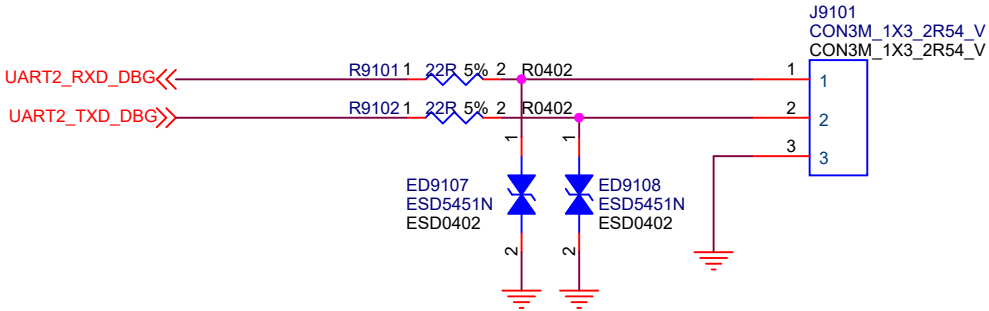


<div>Rockchip</div> <div>瑞芯微电子</div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	85.DP Output		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	41 of 45

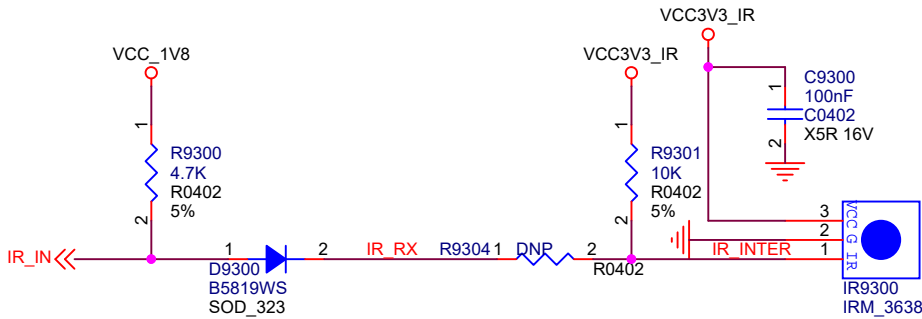
TF CARD



UART for debug

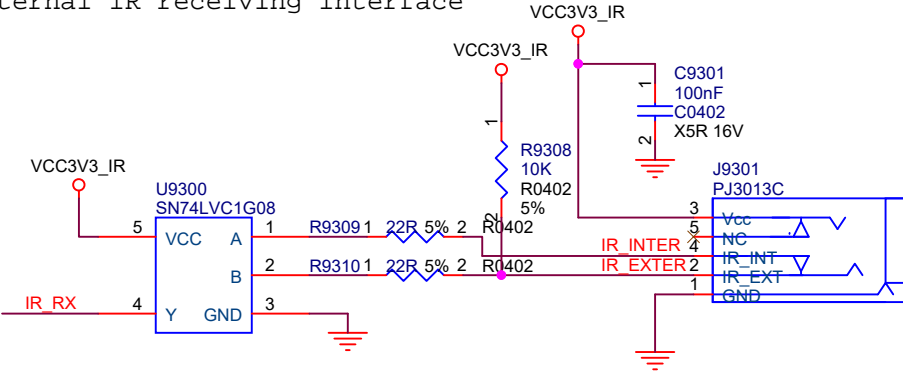


IR Receiver

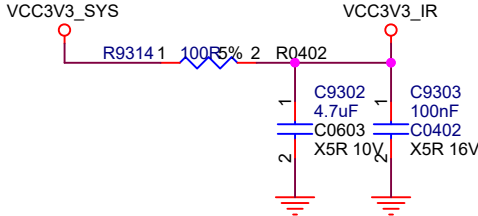


Option

External IR receiving interface

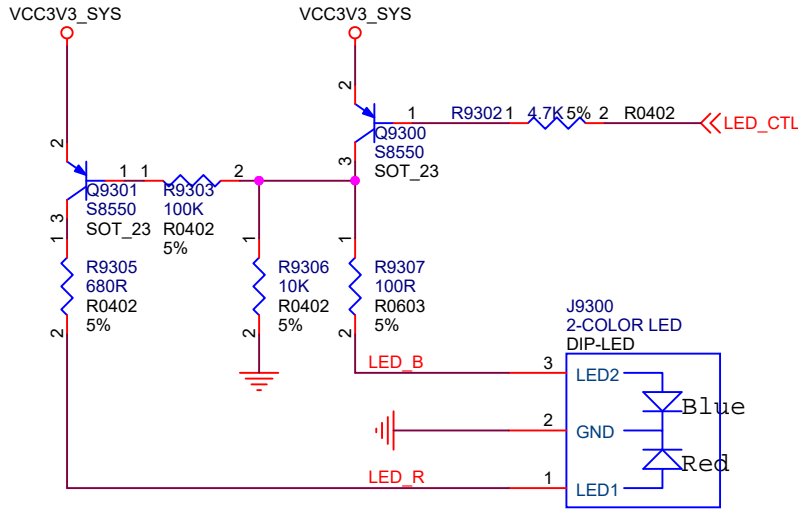


IR Power



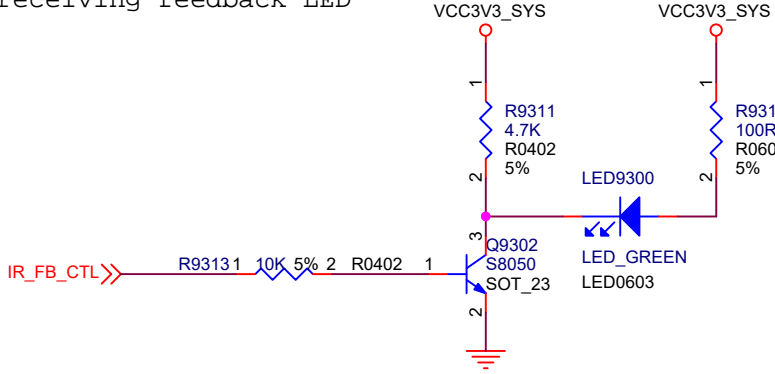
LED


Note:
Blue LED shows work states,
Red LED shows shutdown states



Option

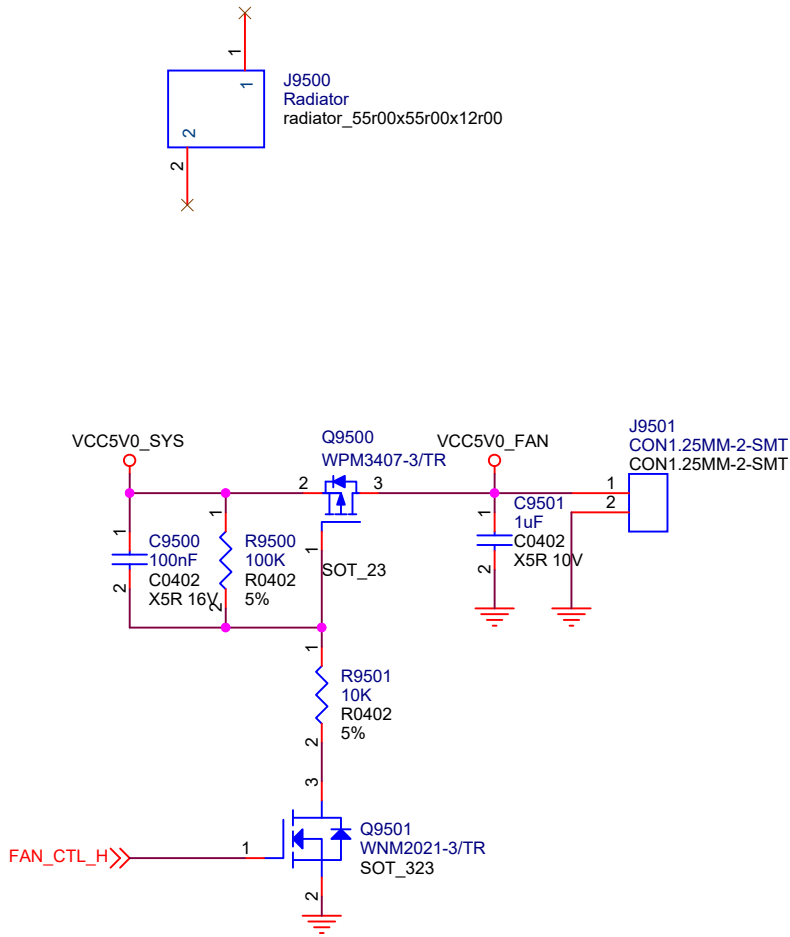
IR receiving feedback LED



 Fuzhou Rockchip Electronics			
Project:	RK3399_BOX_REF		
File:	93.IR Receiver/LED Controller		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	43 of 45

HEATSINK/FAN(option)

Note:Power for FAN,It can be deleted if no need.



<div><div>Rockchip</div><div>瑞芯微电子</div></div> <div>Fuzhou Rockchip Electronics</div>			
Project:	RK3399_BOX_REF		
File:	95.HEATSINK/FAN (option)		
Date:	Tuesday, August 21, 2018	Rev:	V1.3
Designed by:	Linus	Sheet:	44 of 45

eFUSE(option)

Note:Power for eFUSE Program,it is recommended to reserve on the tooling.It can be deleted if no need.

