

Reference Schematics For RK3588S

RK3588S_Tablet_Demo_SCH

Main Functions Introduction

- 1) Charger: 1Cell Battery_QC
- 2) PMIC: 1 x RK806-1+DiscretePower
- 3) RAM: 2 x 32bits LPDDR4/4x
- 4) ROM: eMMC5.1(Default)
- 5) Support: 1 x Type-C 3.0(with DP function)
- 6) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
- 7) Support: 1 x 2Lanes MIPI DPHY RX Camera
- 8) Support: 1 x 4Lanes MIPI D/CPHY TX
- 9) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
- 11) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
- 12) Support: 2 x PDM MIC Array
- 13) Support: Gyroscope+G-sensor+Ambient Light+Proximity

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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Description

Note

Option

Notes

NOTE 1:

Component parameter description

1. DNP stands for component not mounted temporarily

2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:

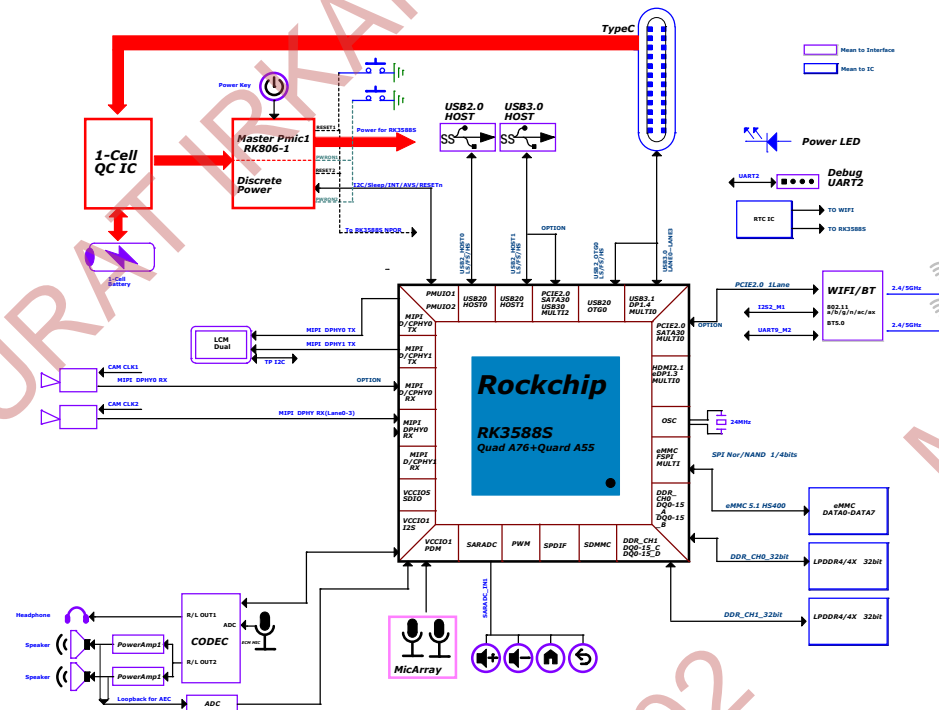
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Revision History

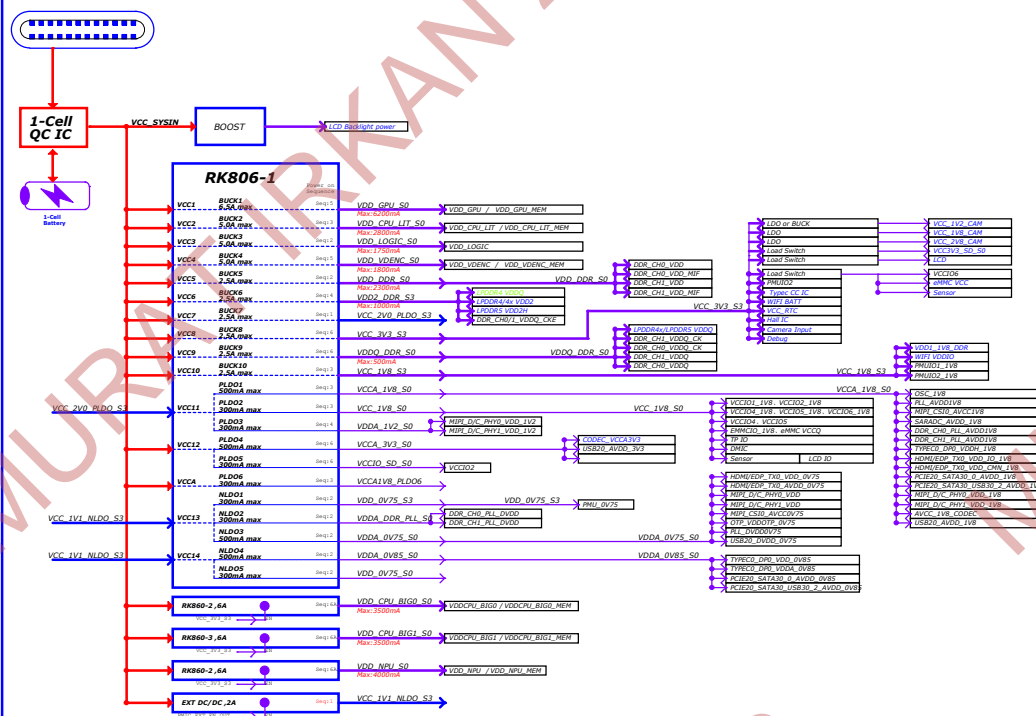
Version	Date	By	Change Dscription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.Wei	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203，L2205，L2207，L2300，L2301，L2302电感由0.22uH(TDK)改为0.24uH(Sunlord); L2201的电感由0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。	



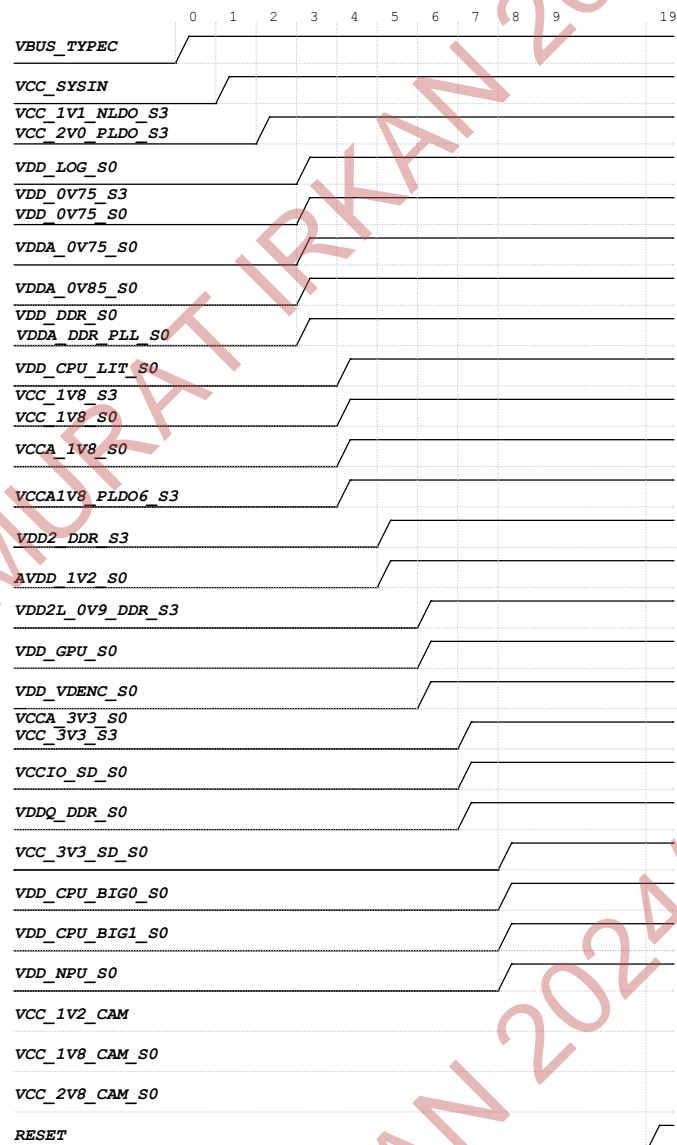
RK3588S Tablet Demo Block Diagram for 1-Cell Charger



Power tree for 1-Cell Charger



Power Sequence

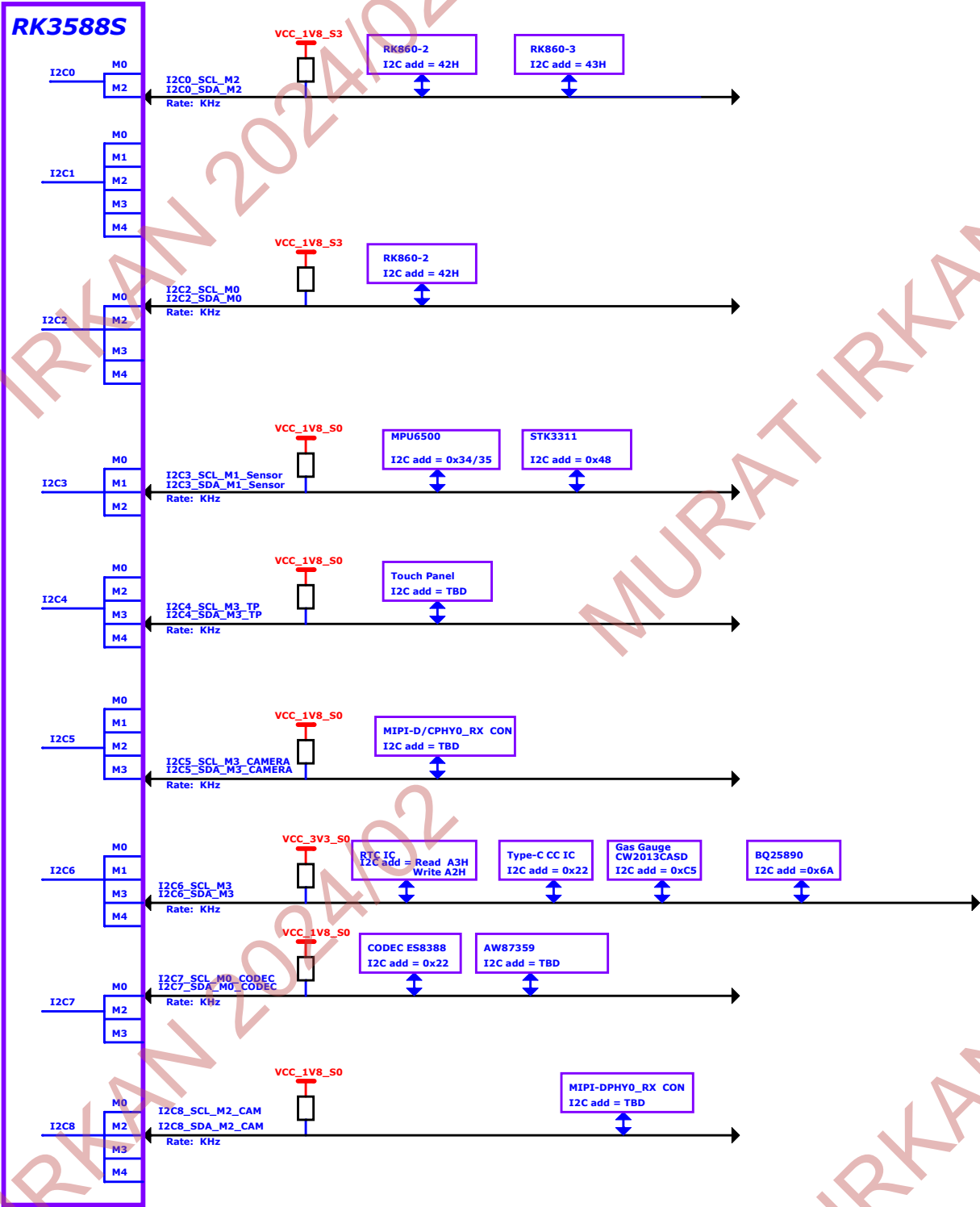


Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

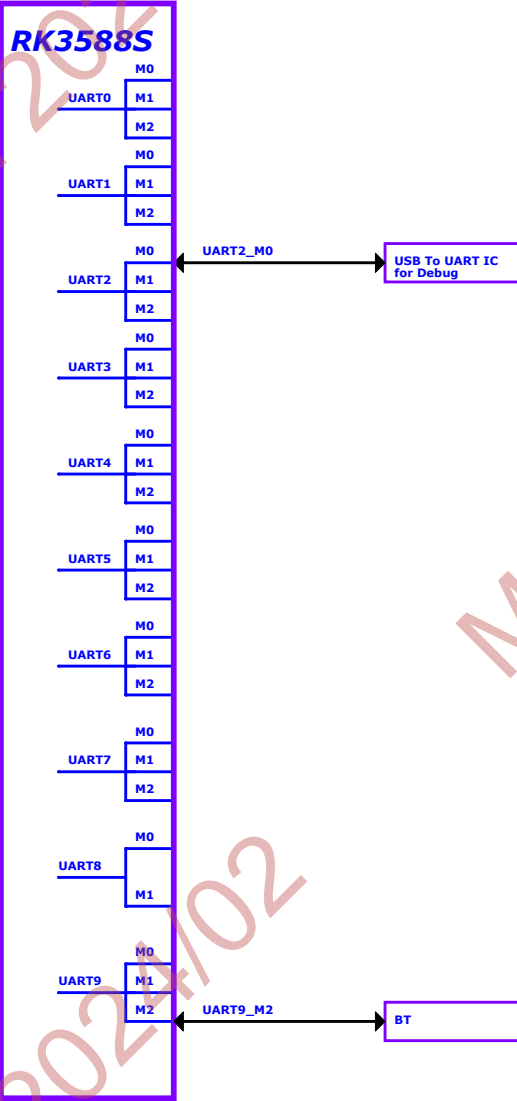
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
EMMCIO	Pin V35 V36	1.8V Only	PMUIO2	VCC_1V8_S3	1.8V
	Pin AC35		EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin AC36				
	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_1V8_S0	1.8V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_1V8_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin A134	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin A133 AM33		VCCIO6	VCC_3V3_S0	3.3V

I2C MAP



UART MAP

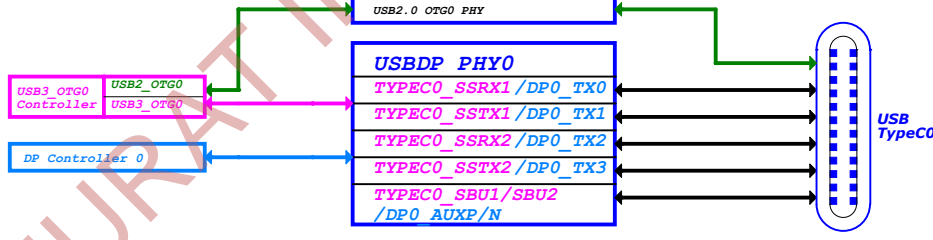


USB Controller Configure Table

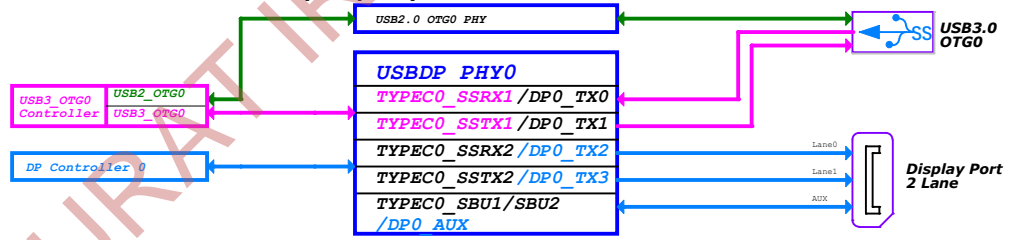
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUX0	TYPEC0_SBU1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEC0_SBU2/DP0_AUX0	TYPEC0_SBU2	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEC0_SSRX12/DP0_TX0P	TYPEC0_SSRX1P	DP0_TX0P	DP0_TX0P	TYPEC0_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P
	TYPEC0_SSRX1N/DP0_TX0M	TYPEC0_SSRX1N	DP0_TX0M	DP0_TX0M	TYPEC0_SSRX1N	DP0_TX0M	DP0_TX0M	DP0_TX0M	DP0_TX0M	DP0_TX0M
USB30 OTG0 Device or Host	TYPEC0_SSTX1N/DP0_TX1P	TYPEC0_SSTX1P	DP0_TX1P	DP0_TX1P	TYPEC0_SSTX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P
	TYPEC0_SSTX1N/DP0_TX1M	TYPEC0_SSTX1N	DP0_TX1M	DP0_TX1M	TYPEC0_SSTX1N	DP0_TX1M	DP0_TX1M	DP0_TX1M	DP0_TX1M	DP0_TX1M
	TYPEC0_SSRX2P/DP0_TX2P	TYPEC0_SSRX2P	DP0_TX2P	DP0_TX2P	TYPEC0_SSRX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEC0_SSRX2N/DP0_TX2M	TYPEC0_SSRX2N	DP0_TX2M	DP0_TX2M	TYPEC0_SSRX2N	DP0_TX2M	DP0_TX2M	DP0_TX2M	DP0_TX2M	DP0_TX2M
USB30 OTG0 Device or Host	TYPEC0_SSTX2P/DP0_TX3P	TYPEC0_SSTX2P	DP0_TX3P	DP0_TX3P	TYPEC0_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEC0_SSTX2N/DP0_TX3M	TYPEC0_SSTX2N	DP0_TX3M	DP0_TX3M	TYPEC0_SSTX2N	DP0_TX3M	DP0_TX3M	DP0_TX3M	DP0_TX3M	DP0_TX3M
	TYPEC0_SBU1/DP0_AUX0	TYPEC0_SBU1	DP0_AUX0	DP0_AUX0	TYPEC0_SBU1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEC0_SBU2/DP0_AUX0	TYPEC0_SBU2	DP0_AUX0	DP0_AUX0	TYPEC0_SBU2	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
USB30 OTG0 Device or Host	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_RXP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP
	PCIE20_2_RXN/SATA30_2_RXN/USB30_2_RXN	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_RXP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP
	PCIE20_2_RXN/SATA30_2_RXN/USB30_2_RXN	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP	TYPEC0_OTG0_DP
USB20 HOST0	USB20_HOST0_DP		USB20_HOST0_DP							
	USB20_HOST0_DP		USB20_HOST0_DP							
	USB20_HOST0_DP		USB20_HOST0_DP							
	USB20_HOST0_DP		USB20_HOST0_DP							
USB20 HOST1	USB20_HOST1_DP				USB20_HOST1_DP					
	USB20_HOST1_DP				USB20_HOST1_DP					
	USB20_HOST1_DP				USB20_HOST1_DP					
	USB20_HOST1_DP				USB20_HOST1_DP					

Note:
DP Lane swap enable
0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

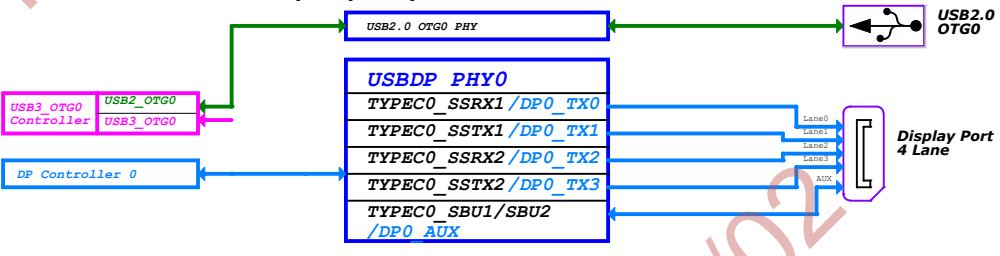
Config0: TypeC0 (With DP function)



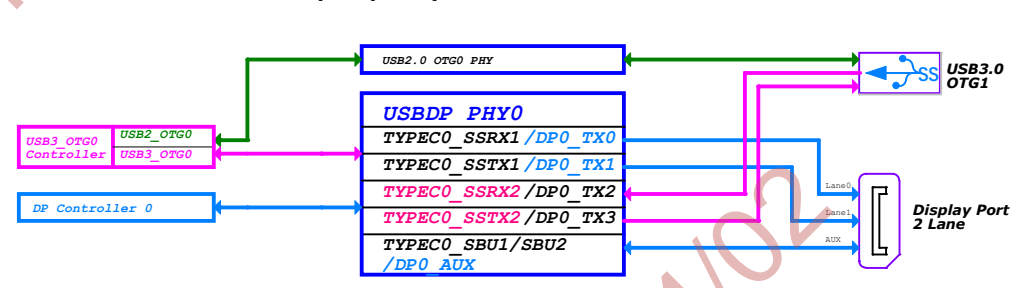
Config3:(Default) USB3.0 OTG0 + DP0 2Lane(Swap ON)



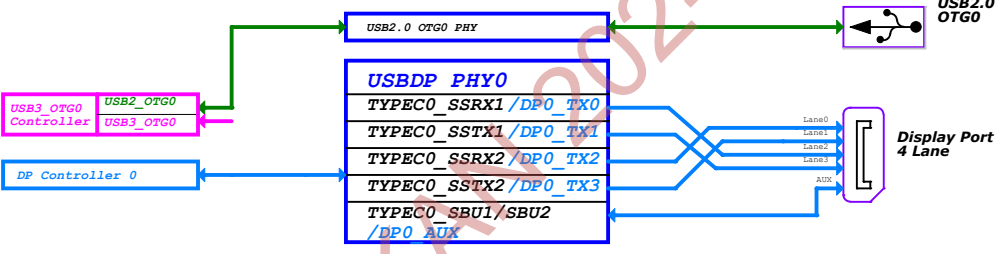
Config1: USB2.0 OTG0 + DP0 4Lane(Swap OFF)



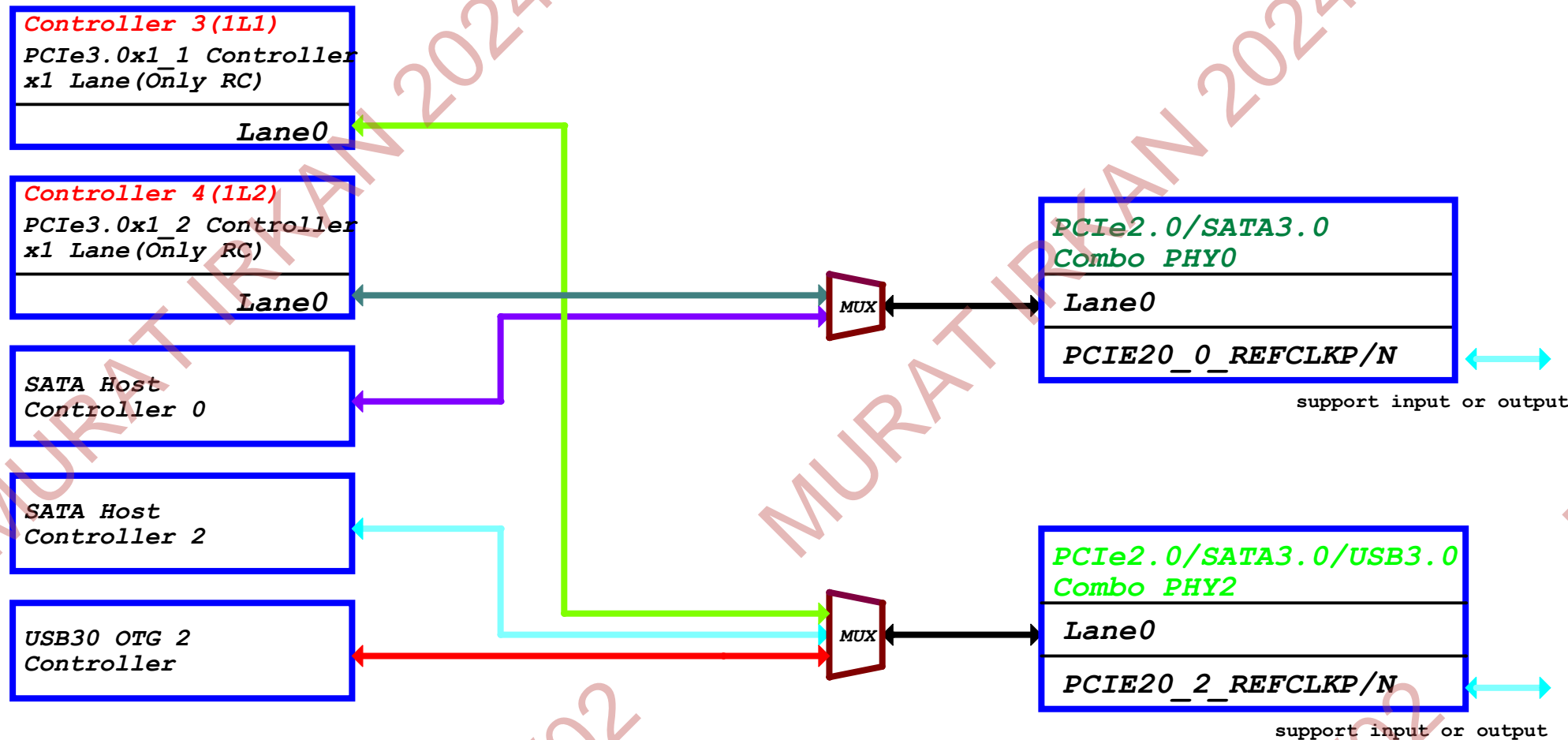
Config4: USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2: USB2.0 OTG0 + DP0 4Lane(Swap ON)



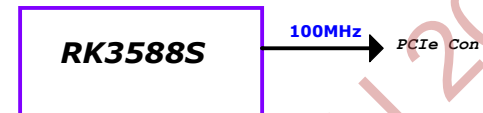
PCIe/SATA Connector Diagram



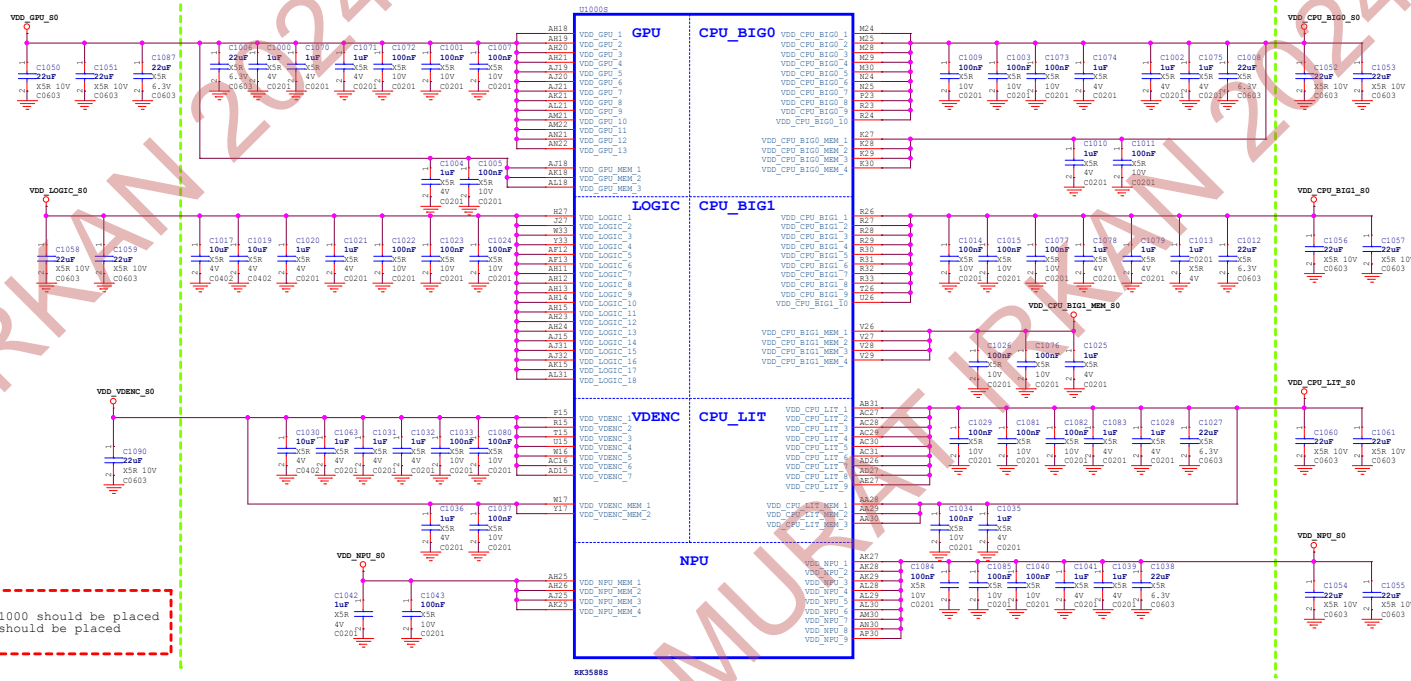
PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ M* PCIE20X1_1_WAKEN M* PCIE20X1_1_PERSTN M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ M* PCIE20X1_2_WAKEN M* PCIE20X1_2_PERSTN M* PCIE20X1_2_BUTTON_RSTN

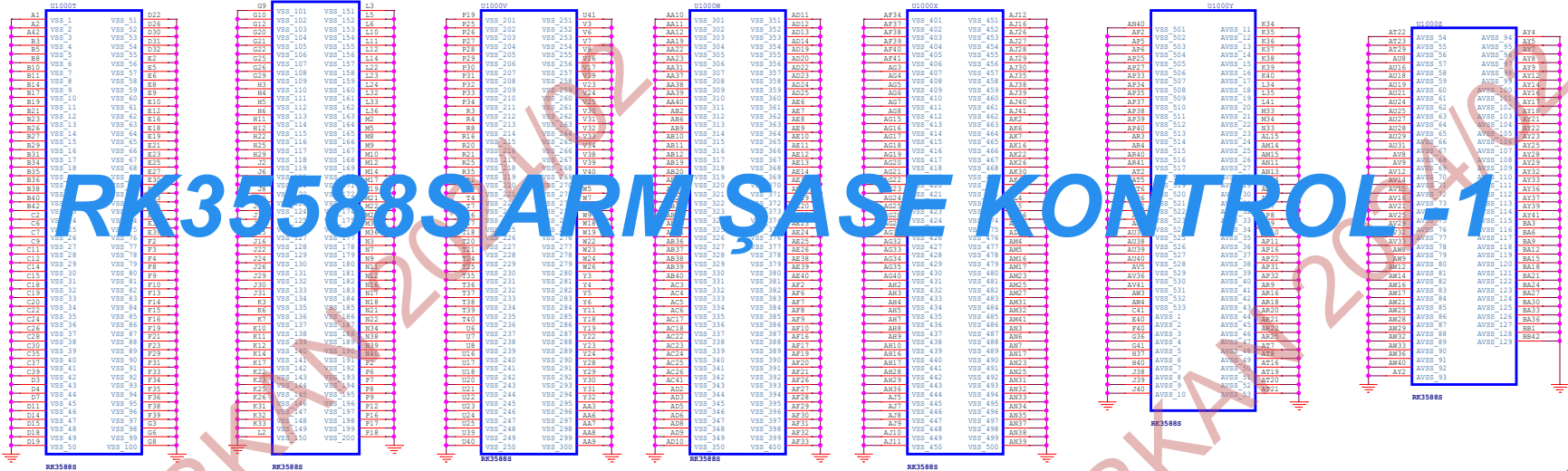
PCIe2.0 REFCLK



Note:
PCIE20_*_REFCLKP/N is output or input gpio
M*=Mean to M0 or M1 or M2,it's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.



RK3588S

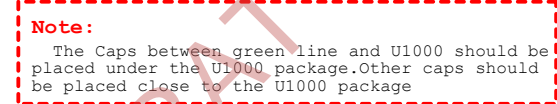


Note:
Adjusted the load capacitance according to the crystal specification

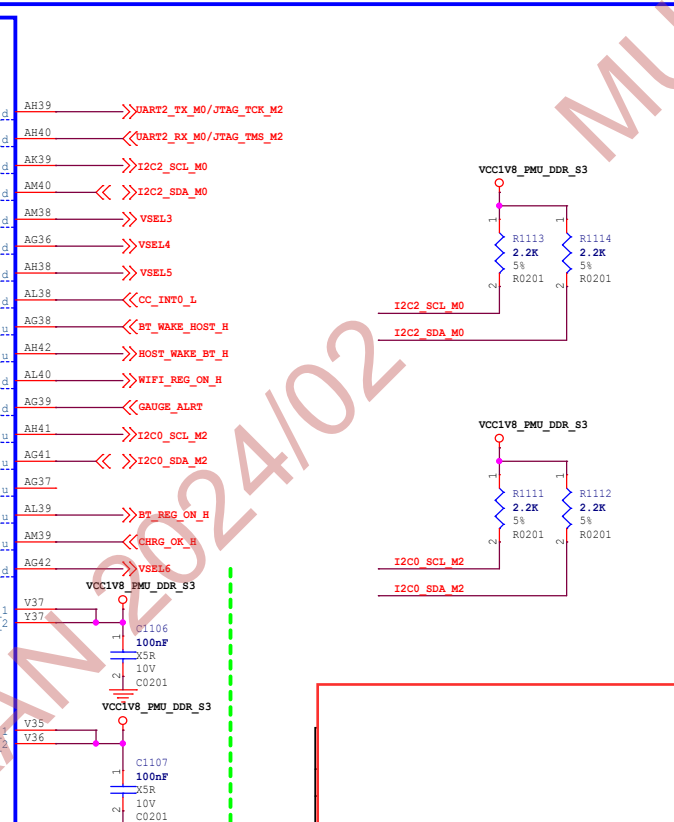
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$$

Total $CL \leq 12pF$



WIRK



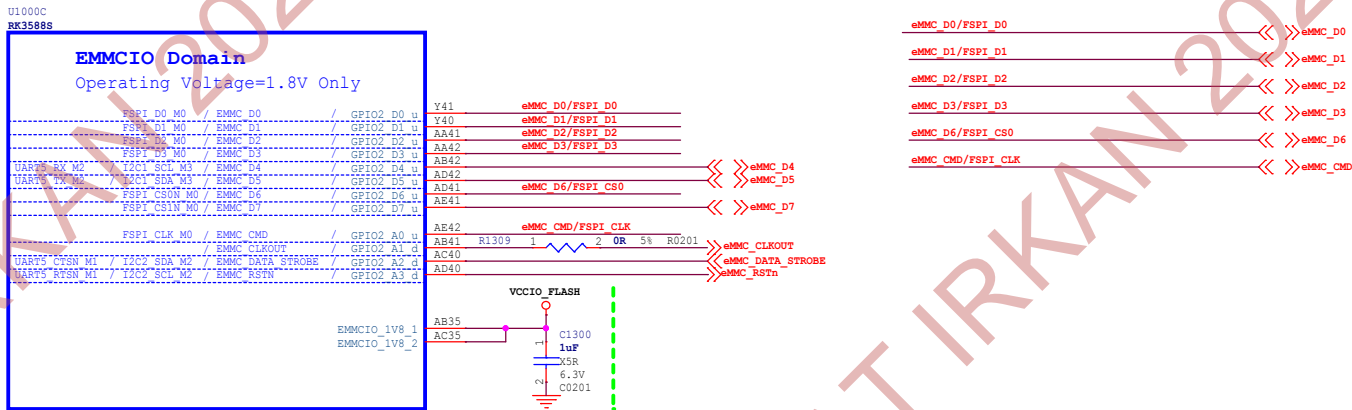
RK3588S (DDR PHY)

LPDDR4-MICRON 32GB

U1000A RK3588S



RK3588S (EMMCIO Domain)



RK3588S (VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (USB3.0/DP1.4)

USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

U1000L RK3588S

USB 3.0 OTG of TYPECO /DP1.4 ALT

USB:U3/Gen1
DP:RBR/HBR/HBR2/HBR3

TYPECO_SBU1/DP0_AUXP BA8
TYPECO_SBU2/DP0_AUXN BB8
TYPECO_SSRX1P/DP0_TX0P BB10
TYPECO_SSRX1N/DP0_TX0N BA10
TYPECO_SSTX1P/DP0_TX1P BB11
TYPECO_SSTX1N/DP0_TX1N BA11

TYPECO_SSRX2P/DP0_TX2P BB13
TYPECO_SSRX2N/DP0_TX2N BA13
TYPECO_SSTX2P/DP0_TX3P BB14
TYPECO_SSTX2N/DP0_TX3N BA14

TYPECO_DP0_REXT

TYPECO_DP0_VDD_OV85

TYPECO_DP0_VDDA_OV85_1
TYPECO_DP0_VDDA_OV85_2

TYPECO_DP0_VDDH_1V8

TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +10%
For Typec

USB30 Differential Pair: DATE:90 Ohm +10%
For USB30
DP Differential Pair: DATE:100 Ohm +10%
For DP

Do not delete!!!
If TYPECO is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must
be connected externally
Power: Must supply power

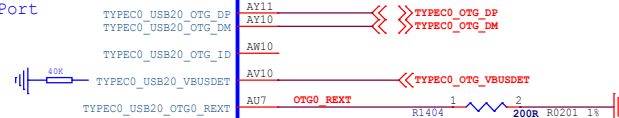
RK3588S (USB2.0)

U1000K RK3588S

USB2.0 OTG of TYPECO

HS/FS/LS

Download Port



USB2.0 HOST0

HS/FS/LS

USB2.0 HOST1

HS/FS/LS

USB2.0 POWER



USB20 Differential Pair:
DATE:90 Ohm +10%

Note:

The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

TYPECO_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

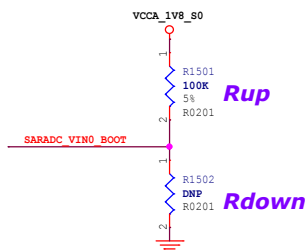
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

```

———>> SARADC_VIN1_KEY/RECOVERY
———>> SARADC_VIN2_LCD_ID
———>> SARADC_VIN4_BATT_TC_L

```



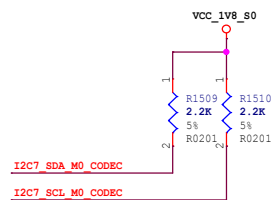
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

U1000C RK3588S

VCCIO1 Domain
Operating Voltage=1.8V Only

SPI4 MISO M0 / UART3 RX M0 /	I2C3 SDA M0 /	GPIO1 C0_2	R38
SPI4 MOSI M0 / UART3 TX M0 /	I2C3 SCL M0 /	GPIO1 C1_2	N41
SPI4 CLK M0 / UART3 FCSN	PWM0 IR M2 / I2C4 SDA M4 /	I2S0 SDIO1	U36
SPI4 CS0 M0 / UART3 CS0N	I2C4 SCL M4 /	GPIO1 D2_3	M42
SPI4 CS1 M0 / UART3 CS1N	PWM11 IR M2 / PDMS SDIO M0 /	GPIO1 C4_5	U35
UART4 RPSN	I2C3 SCL M3 / I2S0 LRCK	GPIO1 C5_6	F39
PWM15 IR M2 / I2C4 SDA M4 /	PDMS CLK0 M0 /	GPIO1 C6_7	M41
UART4 CSN	I2C4 SCL M4 / I2S0 SDO0	GPIO1 C6_3	F41
	I2C7 SCL M4 /	GPIO1 C7_8	
SPI1 MISO M2 / UART6 TX M2 /	I2C7 SCL M0 / I2S0 SDO1	GPIO1 D0_9	U37
SPI1 MOSI M2 / UART6 RX M2 /	I2C7 SCL M0 / PDMS SDIO M0 / I2S0 SDO2/I2S0 SDI1	GPIO1 D1_9	U38
SPI1 CLK M2 / UART6 FCSN	PWM0 MI / I2C1 SCL M4 /	GPIO1 D1_0	F40
SPI1 CS0 M2 / UART6 CS0N	I2C1 SCL M4 / PDMS SDIO M0 / I2S0 SDO3/I2S0 SDI2	GPIO1 D2_3	R39
SPI1 CS1 M2 / UART6 CS1N	PWM1 MI / I2C1 SDA M4 /	GPIO1 D3_4	N42
SPI1 CS2 M2 / UART6 CS2N	PWM11 MI / I2C1 SDA M4 /	GPIO1 D4_5	F38
SPI1 CS3 M2 / UART6 CS3N	PWM11 MI / I2C1 SDA M4 /	GPIO1 D5_6	
SPI1 CS4 M2 / UART6 CS4N	PWM11 MI / I2C1 SDA M4 /	GPIO1 D5_7	

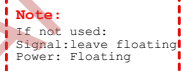
VCC1V8_S0
 H31
 C1508
 100nF
 X5R
 10V
 C0201



Note:

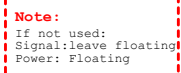
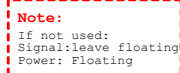
Caps of between dashed green lines and U1000 should be placed under the U1000 package

U1000N RK3588S



Note: When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package



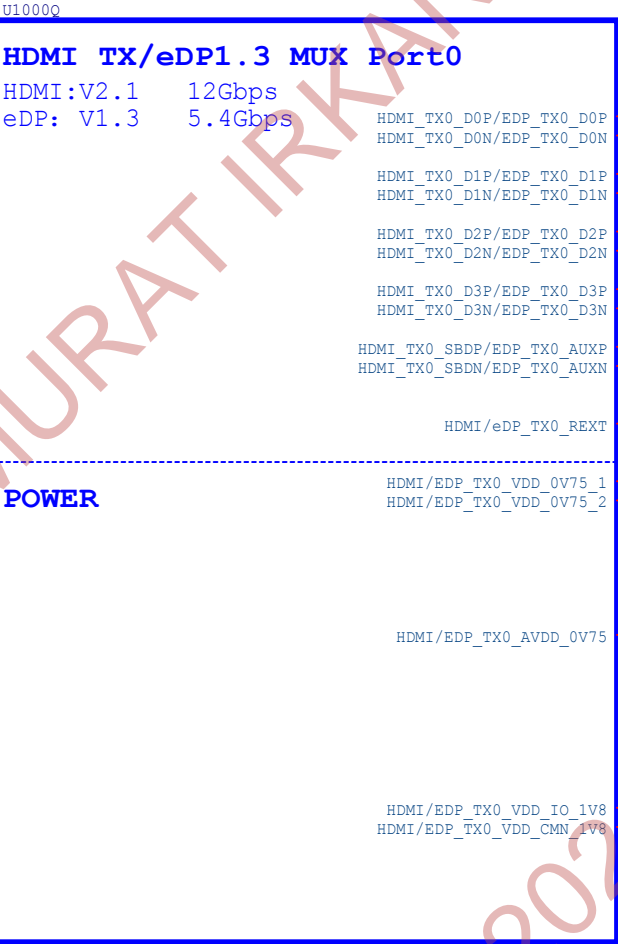
RK3588S (HDMI2.1 TX/eDP1.3 TX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm $\pm 10\%$

HDMI TX
100 Ohm $\pm 10\%$



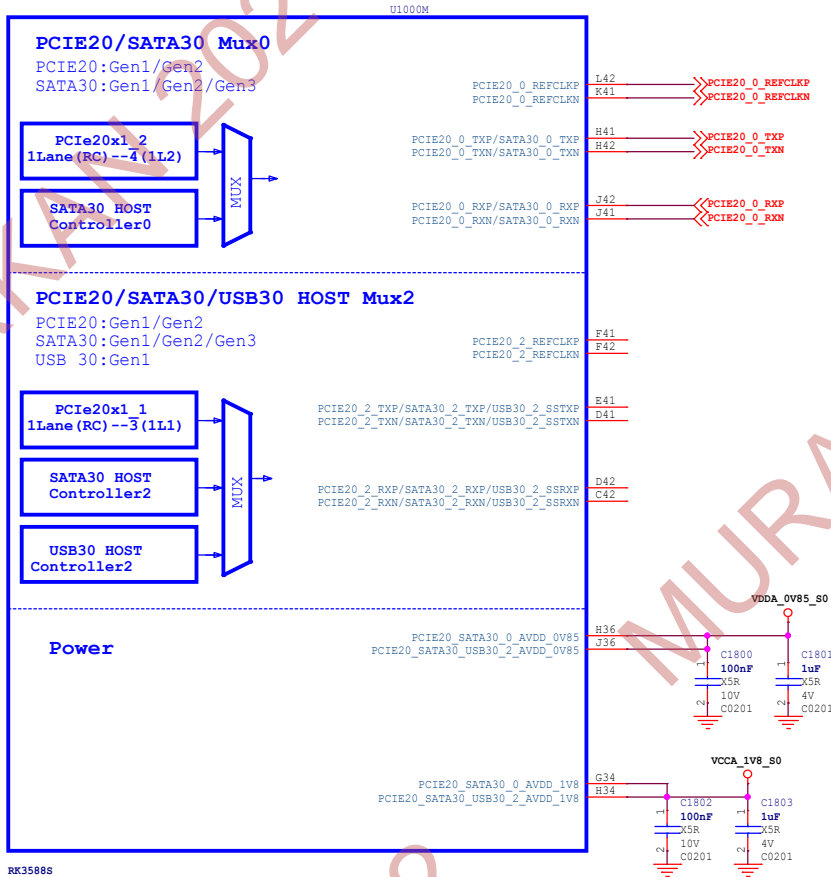
Note:

If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

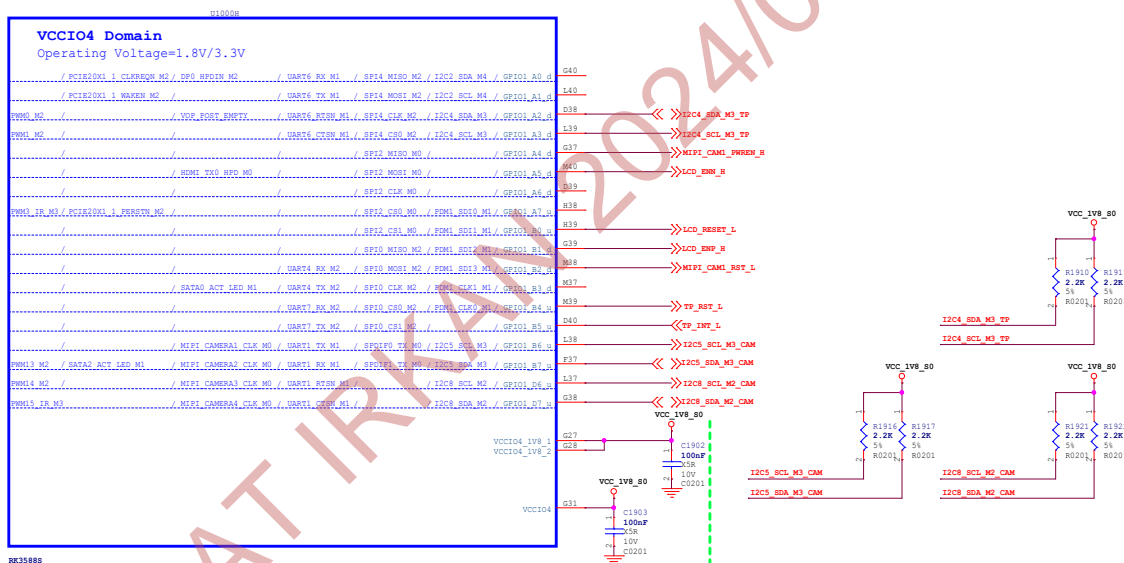
RK3588S (PCIE20/SATA30/USB30)



PCIE2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ M* PCIE20X1_1_WAKEN M* PCIE20X1_1_PERSTN M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ M* PCIE20X1_2_WAKEN M* PCIE20X1_2_PERSTN M* PCIE20X1_2_BUTTON_RSTN

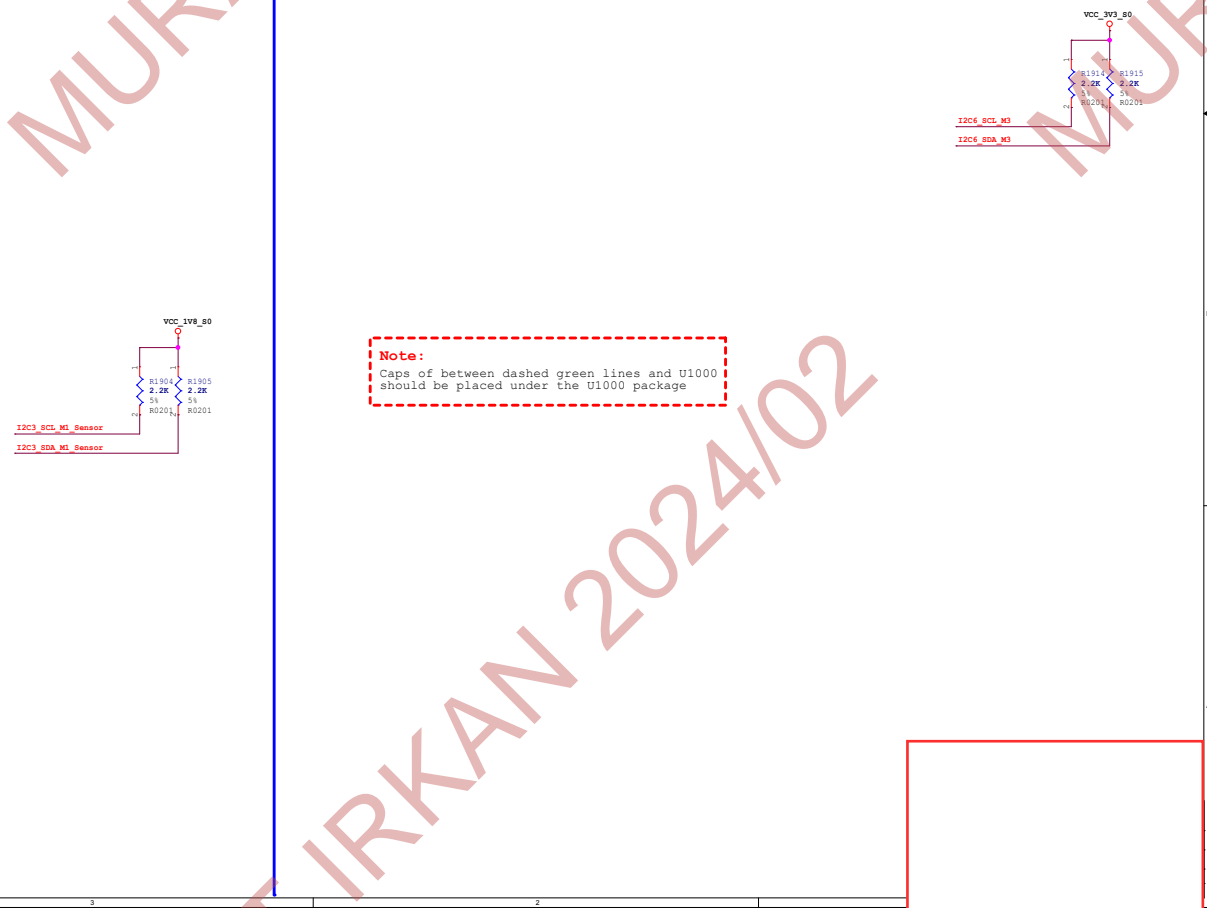
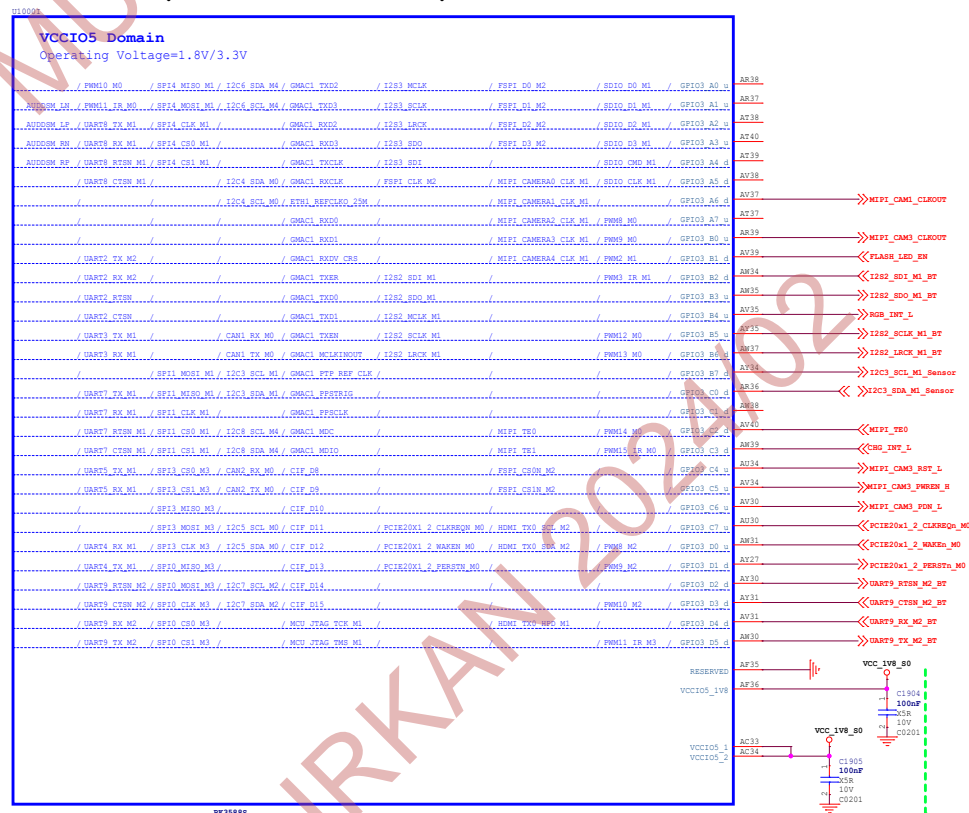
RK3588S (VCCIO4 Domain)



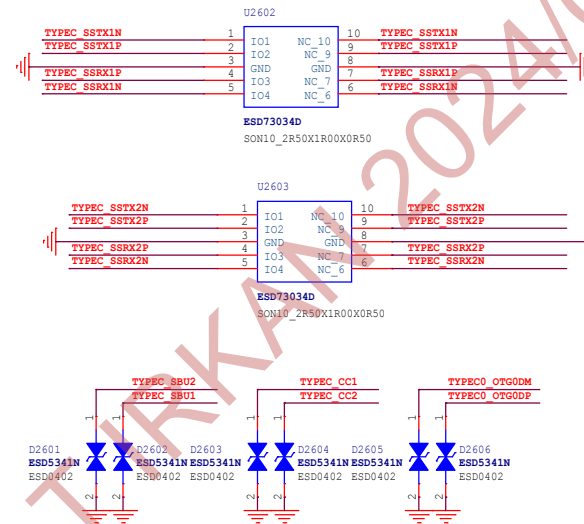
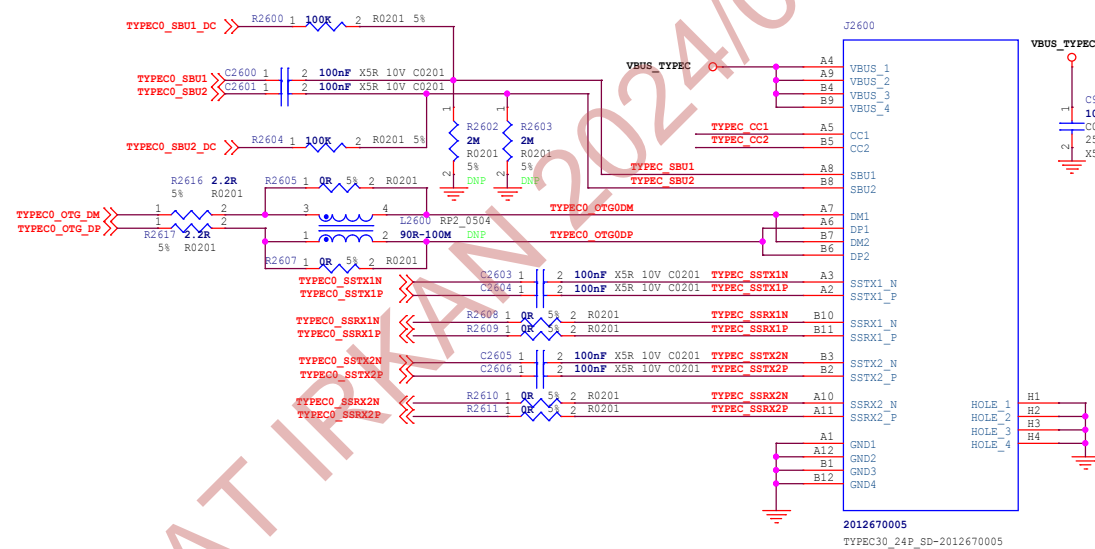
RK3588S (VCCIO6 Domain)



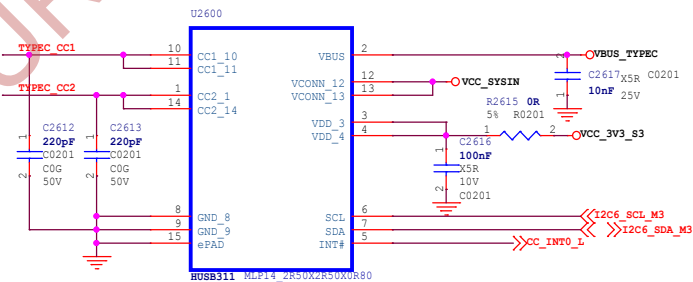
RK3588S (VCCIO5 Domain)



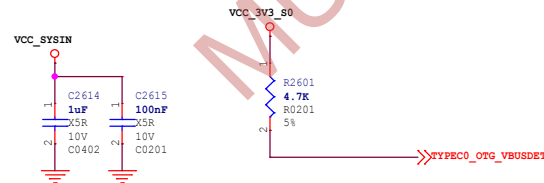
USB Type-C Port



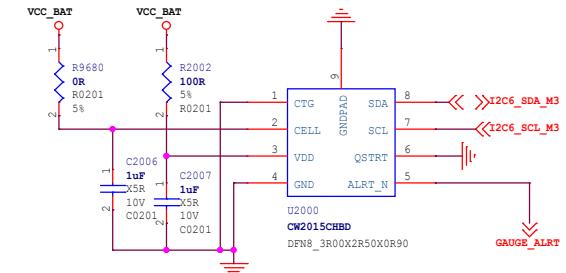
USB Type-C CC CTRL



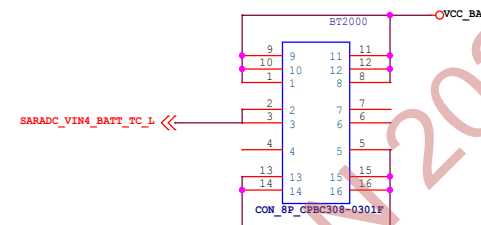
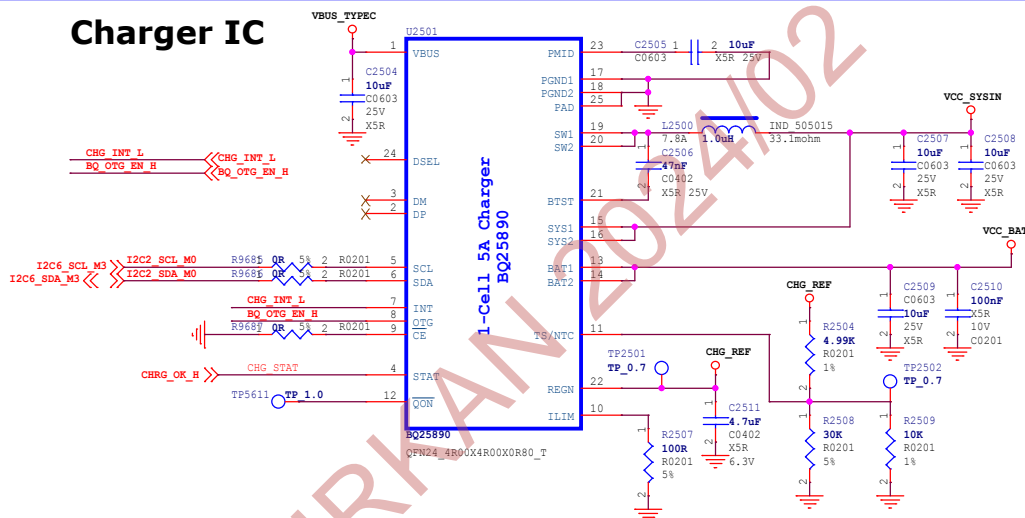
USB Detection



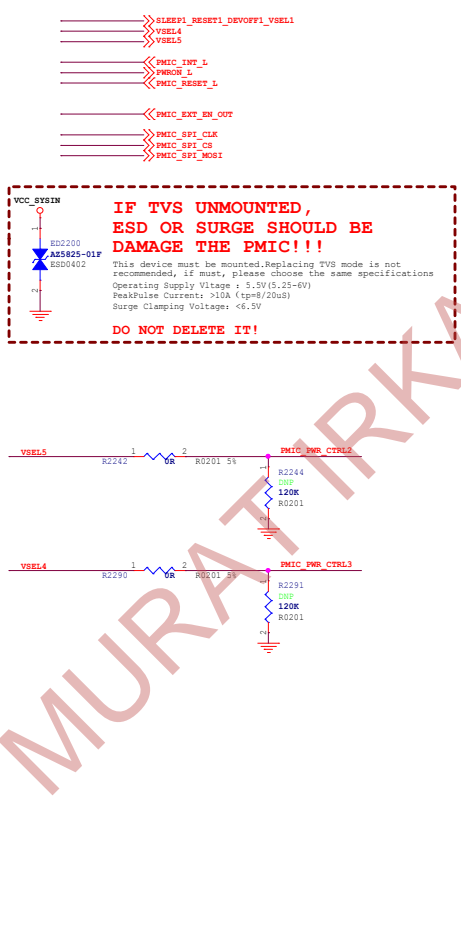
Gas Gauge



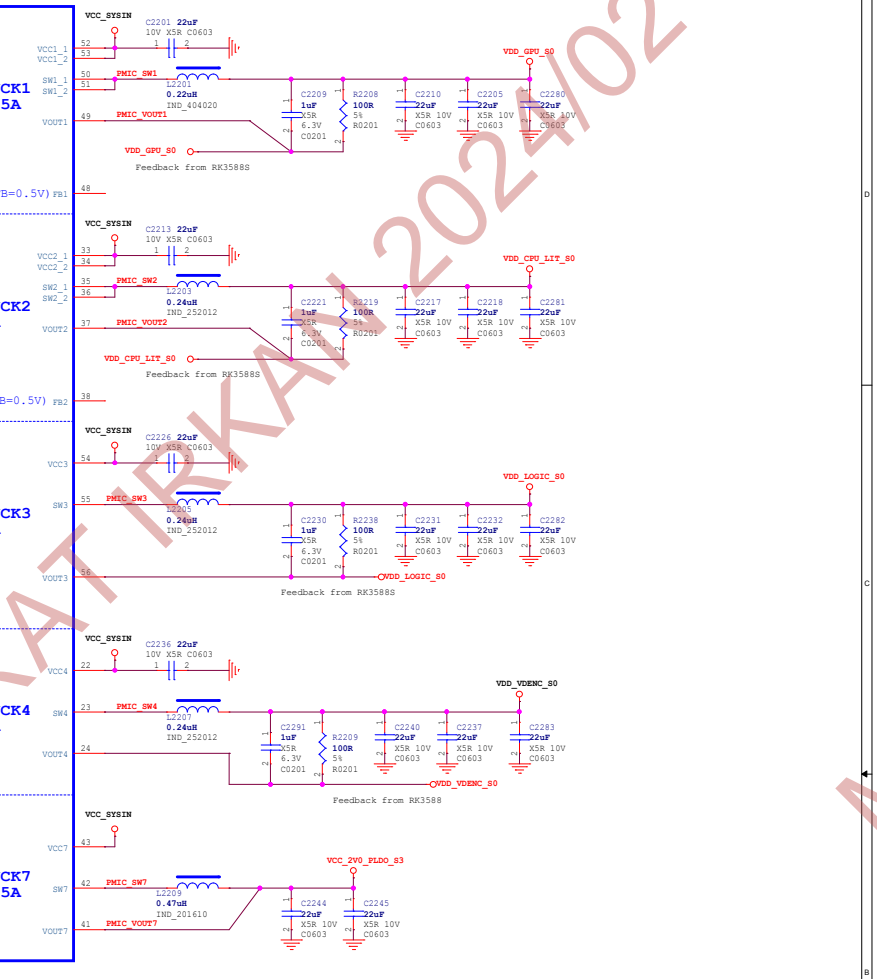
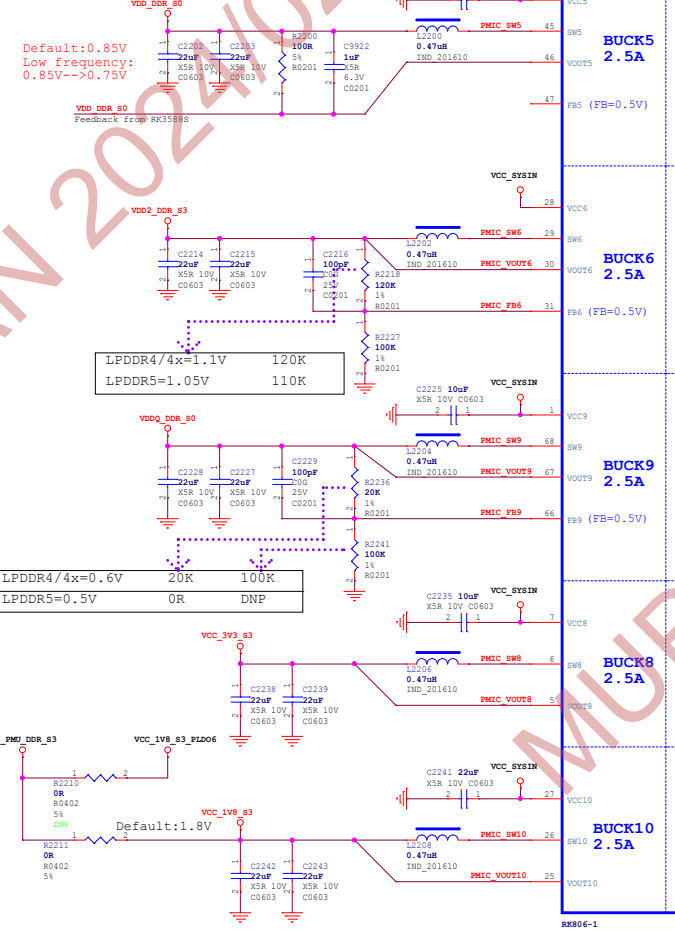
Charger IC



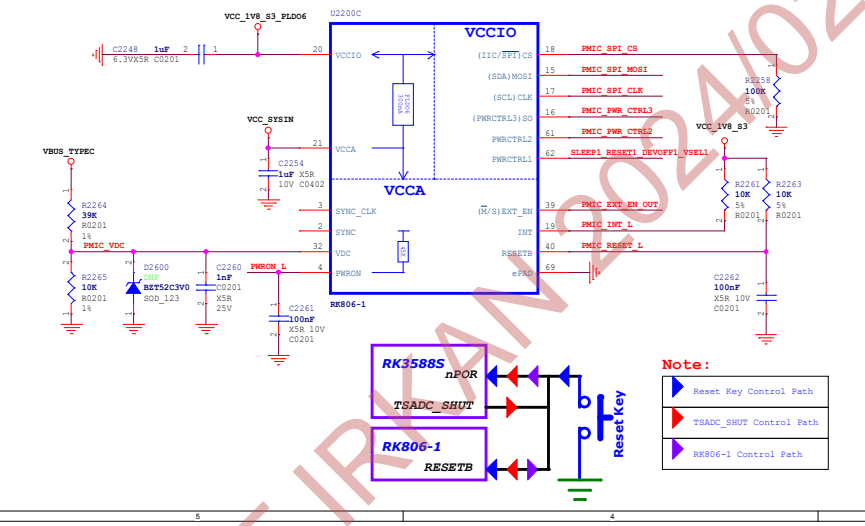
PMIC1 RK806-1



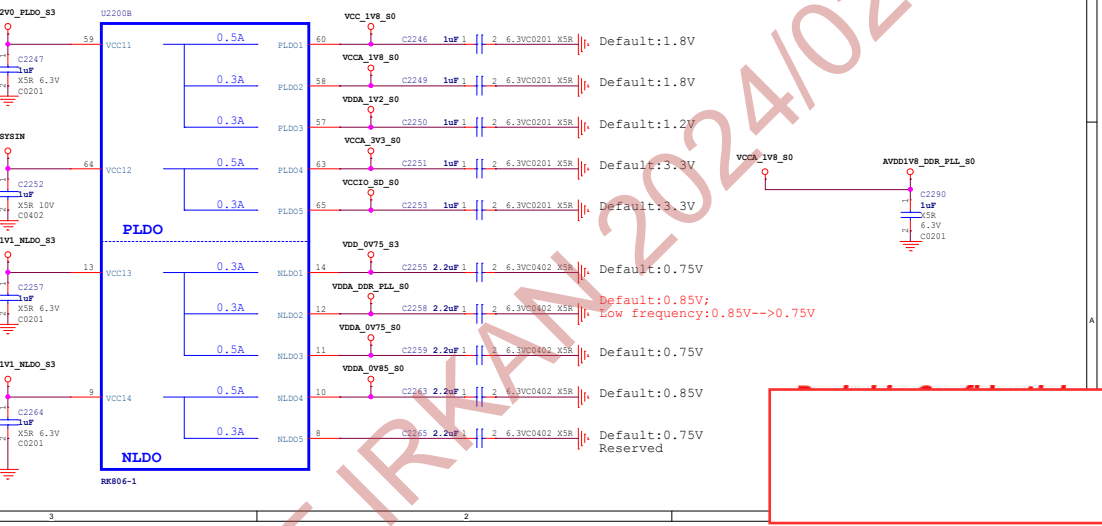
PMIC RK806-1 BUCK



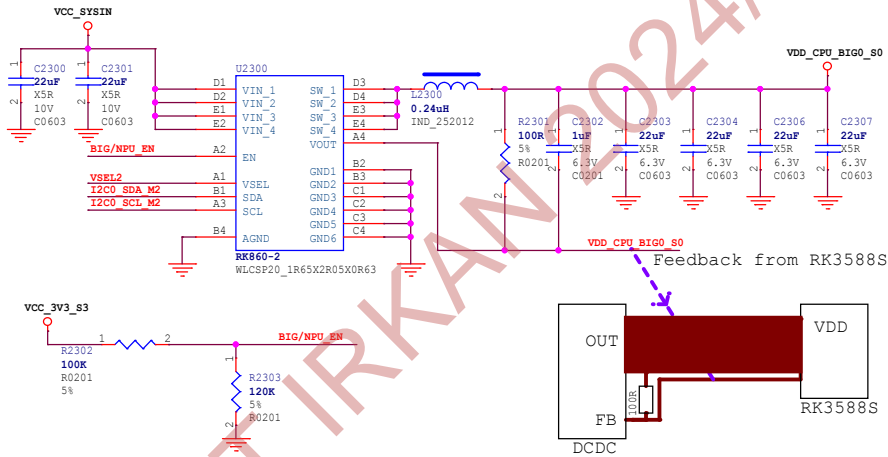
PMIC RK806-1 Management



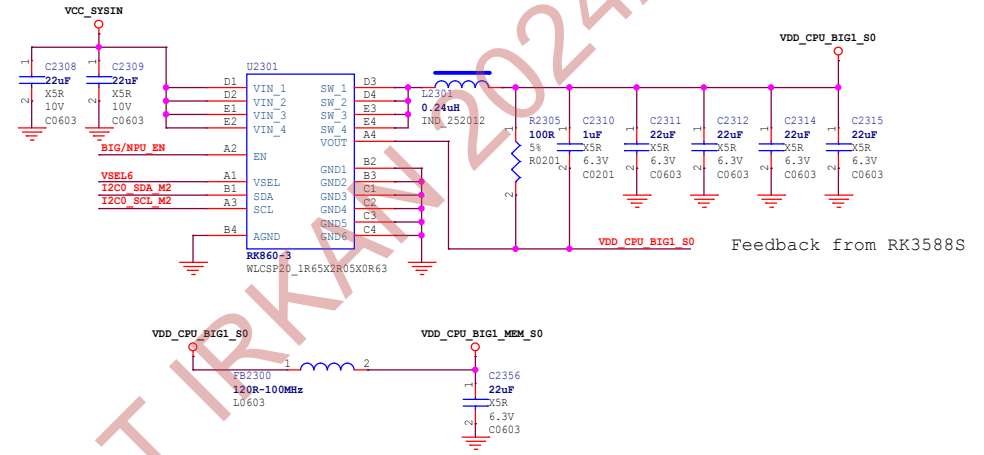
PMIC RK806-1 LDO



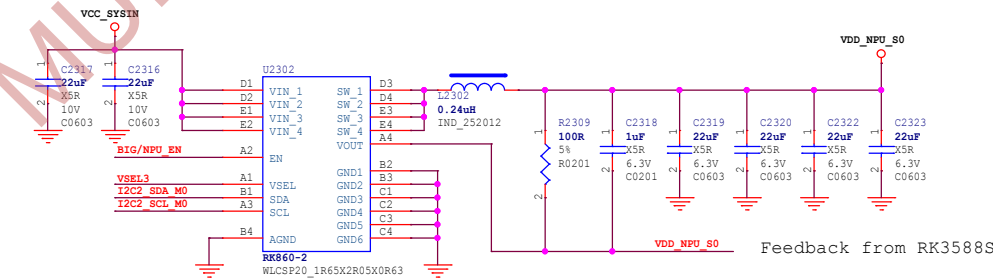
VDD_CPU_BIG0



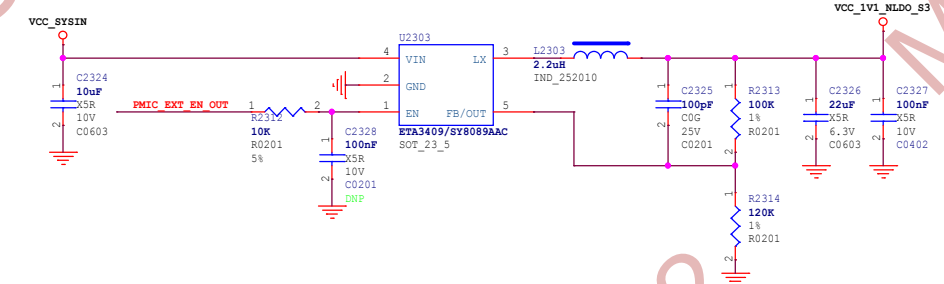
VDD_CPU_BIG1



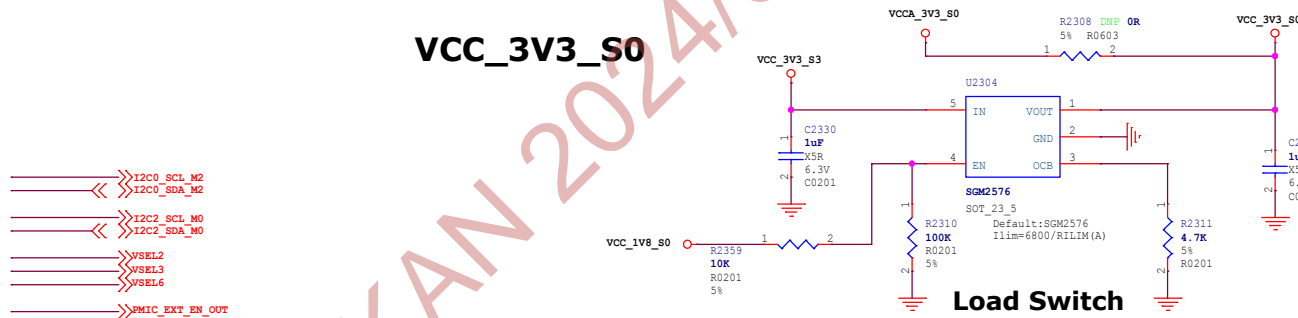
VDD_NPU



VCC_1V1_NLDO

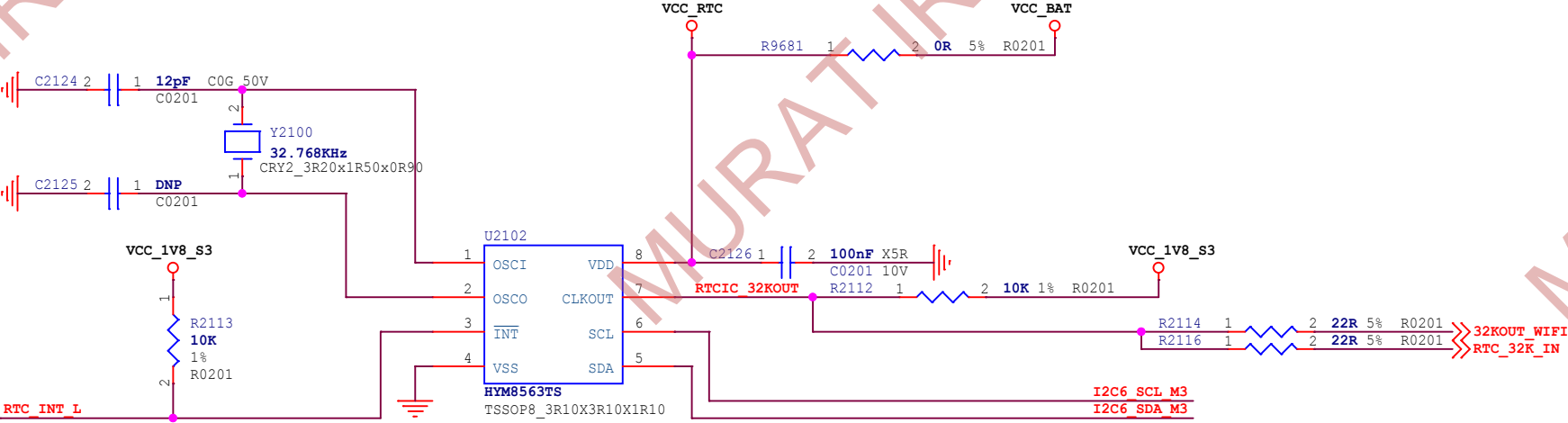


VCC_3V3_S0



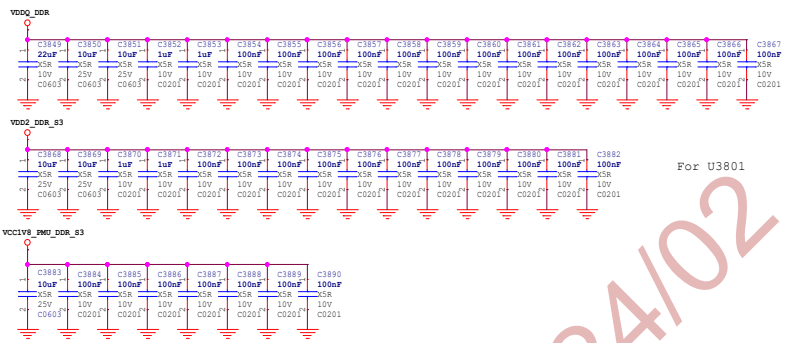
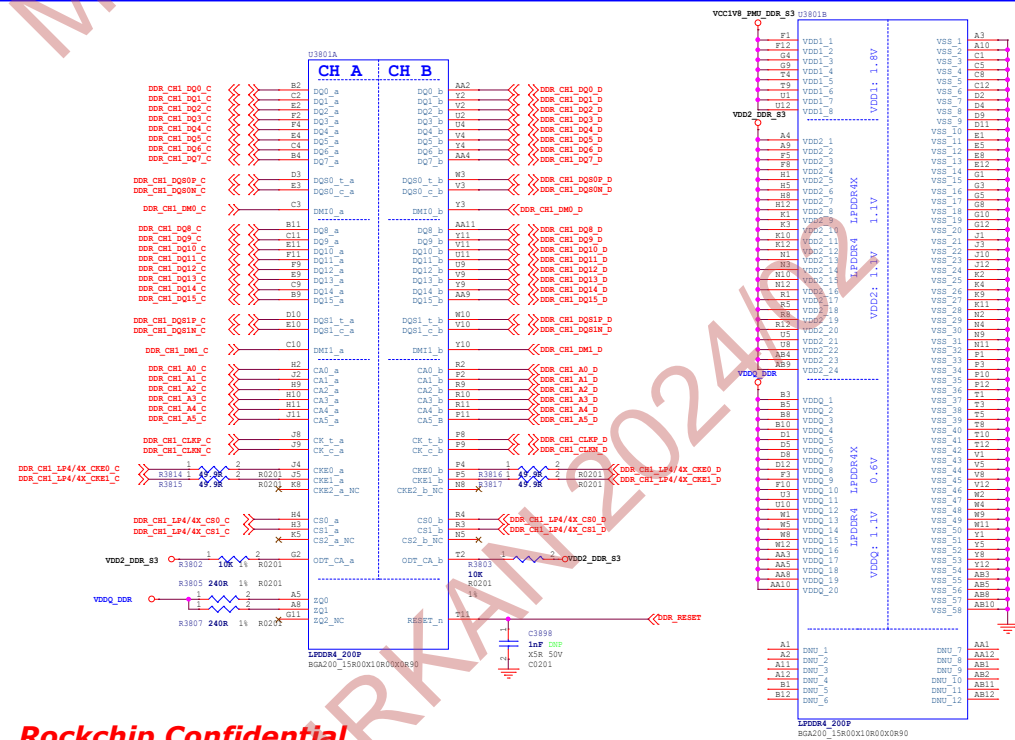
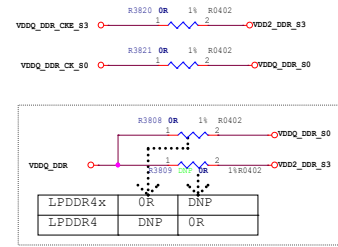
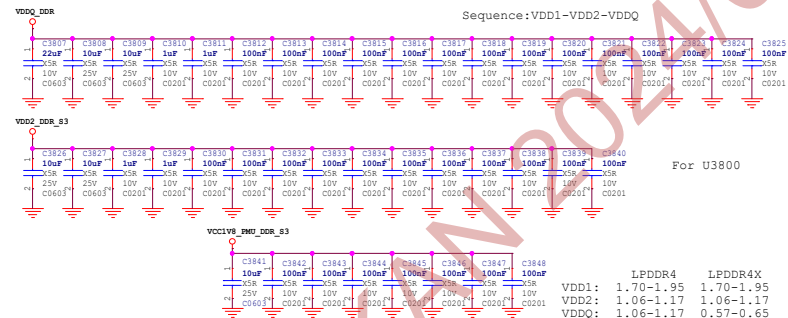
RTC IC

RTC_INT_L
I2C6_SCL_M3
I2C6_SDA_M3

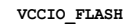


Address:Read A3H,Write A2H

U3800A	
CH A	CH B



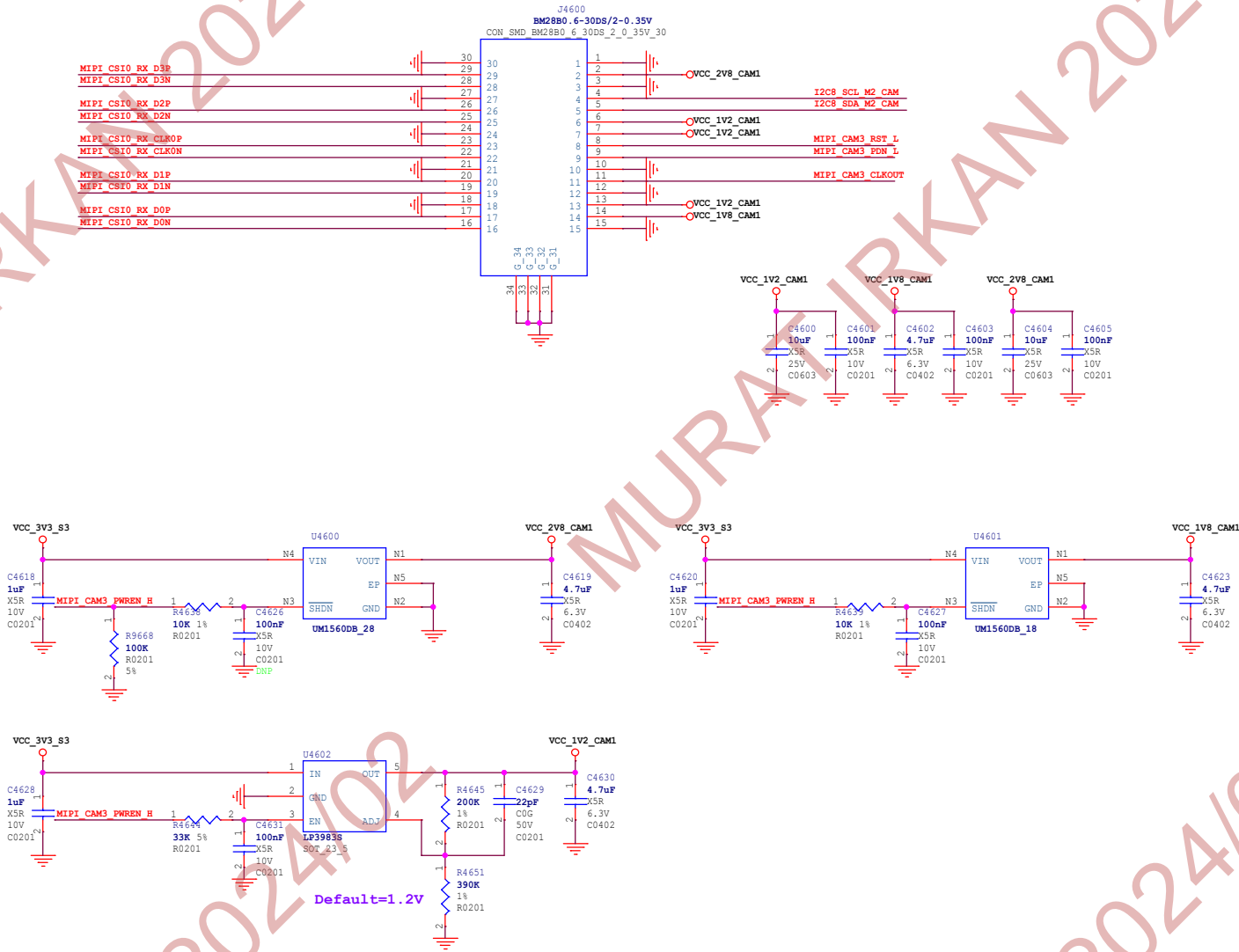
U4000B



BGA153 13R00X11R50X0R90 2L

MIPI-CSIO_RX

前摄: OV16A10-GA5A-Z



VI-Camera DPHY_RX

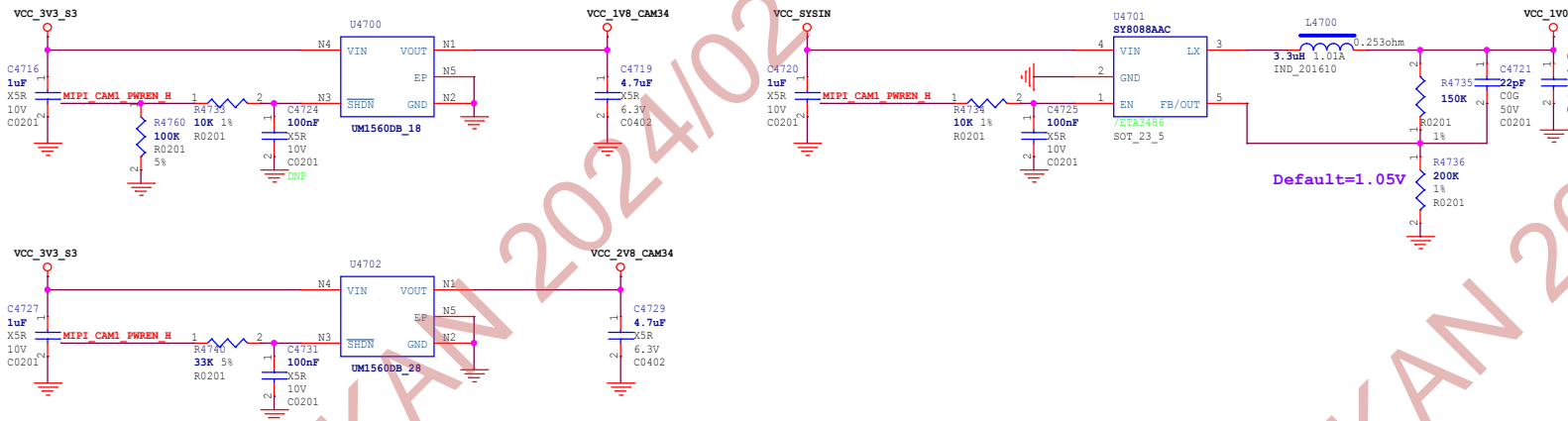
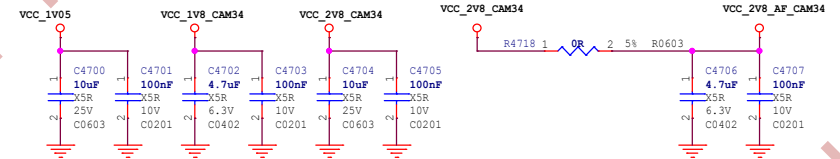
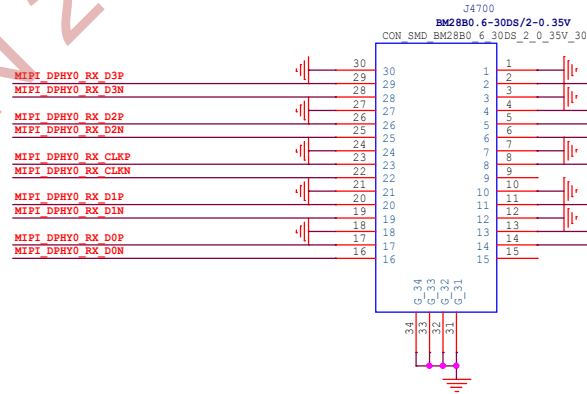
后摄: S5K3L6XX03-FGX9

MIIPI_DPHY0_RX_CLKP
MIIPI_DPHY0_RX_CLKN
MIIPI_DPHY0_RX_D0P
MIIPI_DPHY0_RX_D0N
MIIPI_DPHY0_RX_D1P
MIIPI_DPHY0_RX_D1N
MIIPI_DPHY0_RX_D2P
MIIPI_DPHY0_RX_D2N
MIIPI_DPHY0_RX_D3P
MIIPI_DPHY0_RX_D3N

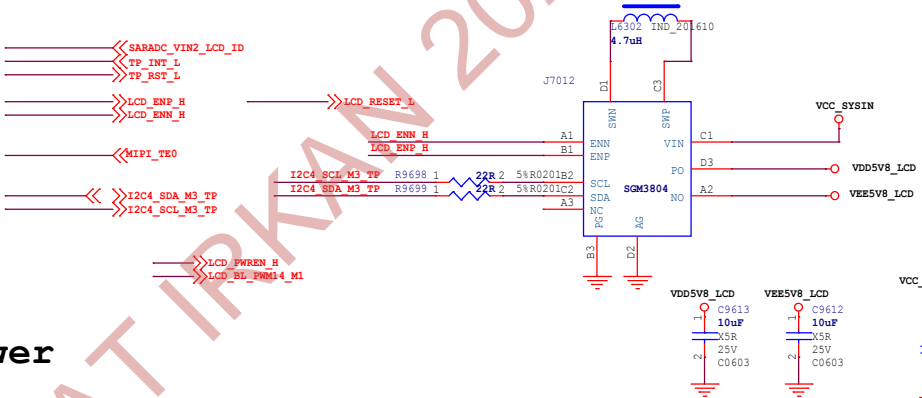
MIIPI_CAM1_CLKROUT

MIIPI_CAM1_PWREN_H
MIIPI_CAM1_RST_L

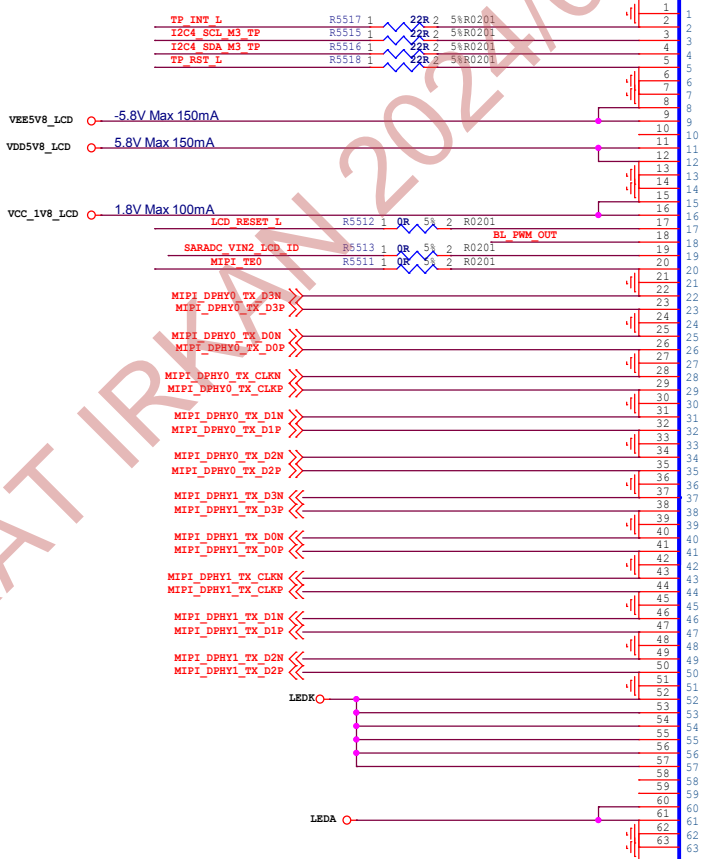
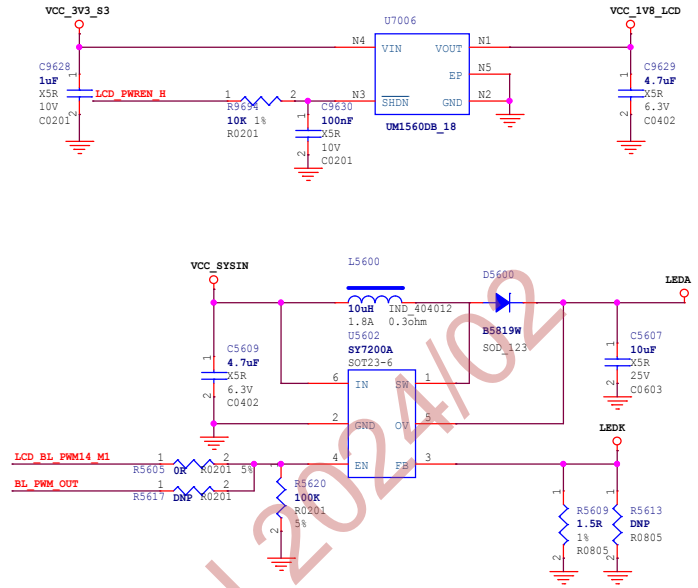
I2C5_SCL_M3_CAM
I2C5_SDA_M3_CAM



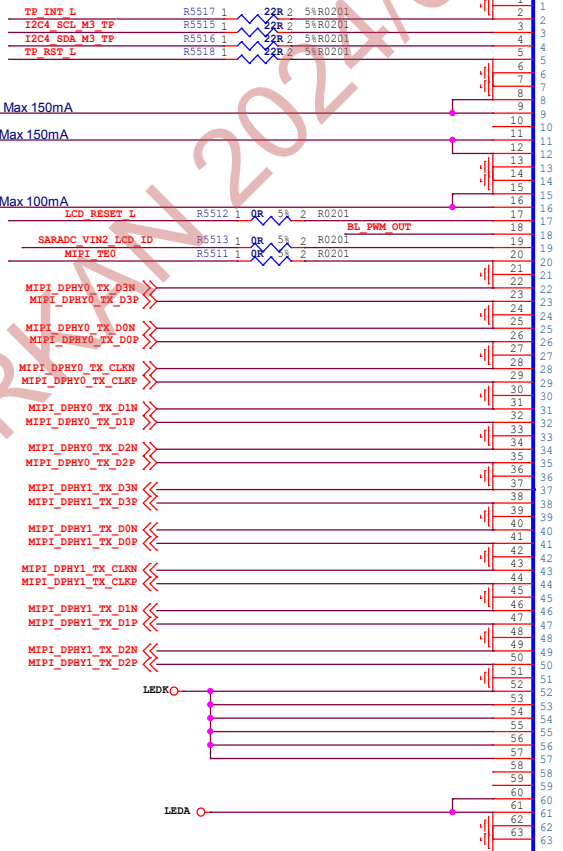
MIPI DPHY TX



Power



J5500
FH35C-61S-0.3SHW
CON SMD FH35C-61S-0.3SHW



PCIE WIFI6/BT Module-2T2R

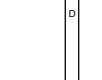
NOTE:
Adjust the load capacitor
according to the crystal spec.

50 Ohm RF trace

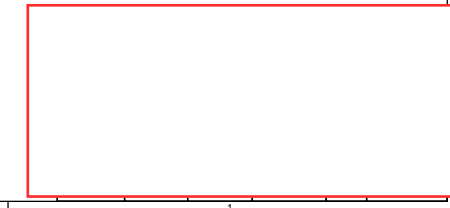
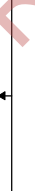
This standalone BT-ANT is reserved for AP6275PR3. Leave PIN48 float for AP6275P, of which BT-ANT is mux with WIFI.

32.768KHZ:
+/-25ppm/30-70%/1.8V

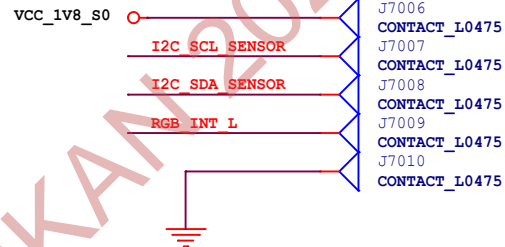
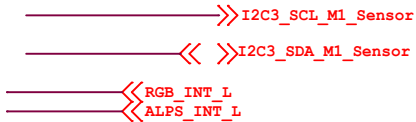
2



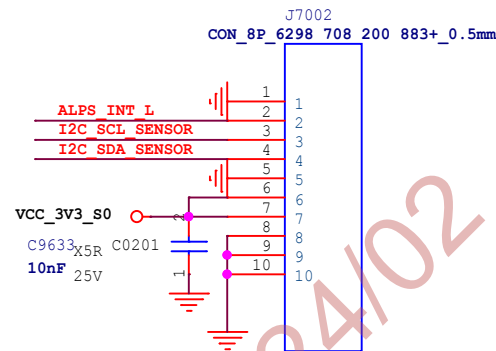
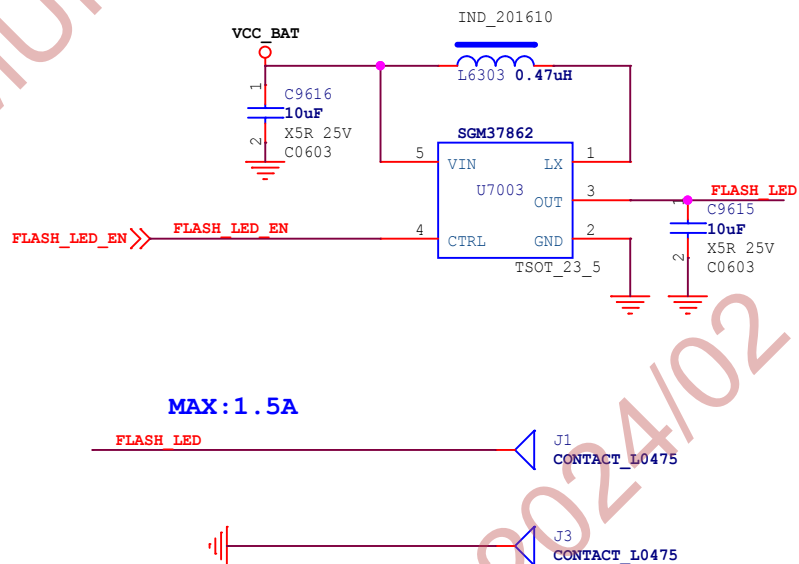
c



Sensor

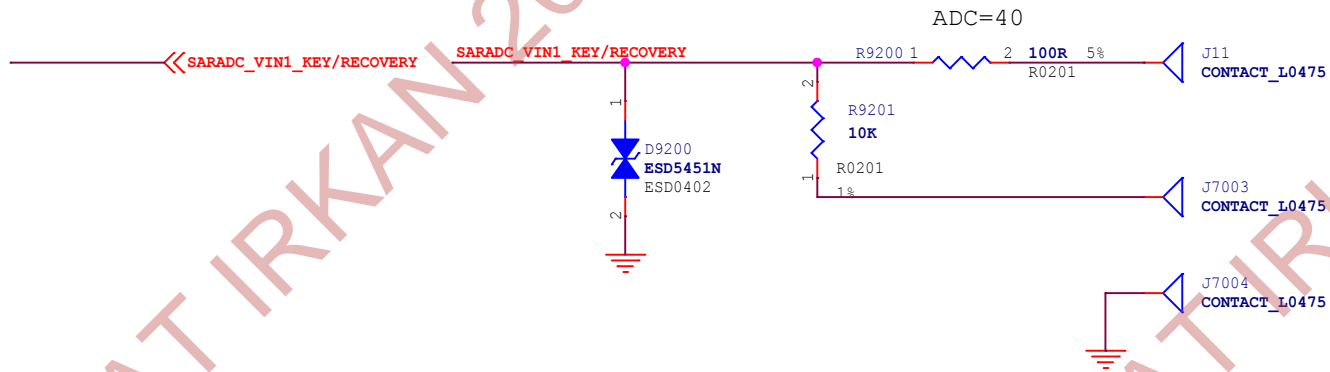


PLS+ALS



Flashlight

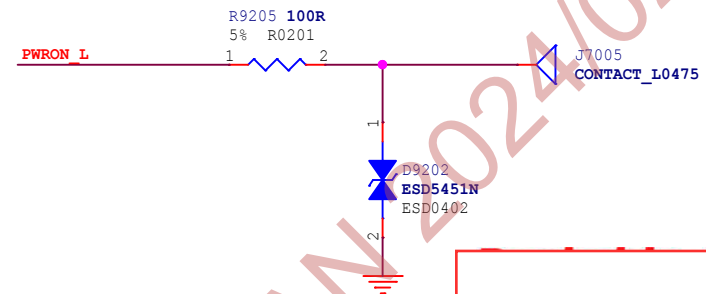
KEY Array



Reset_Key

RESET_L
PWRON_L

PWR_Key



UART Debug

JTAG Debug

UART2_TX_M0/JTAG_TCK_M2
UART2_RX_M0/JTAG_TMS_M2

UART2_TX_M0/JTAG_TCK_M2 R9300 1 2 22R R0201 5% UART_TX
UART2_RX_M0/JTAG_TMS_M2 R9301 1 2 22R R0201 5% UART_RX

