RK3328

Datasheet

Revision 1.1
Mar. 2017

Revision History

Date	Revision	Description
2017-01-17	1.0	Initial released
2017-03-09	1.1	Updated section "Package Thermal Characteristics"

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NOTICE

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Chapter 1 Introduction

1.1 Overview

RK3328 is a high-performance Quad-core application processor designed for Smart STB (Set Top Box) including OTT/IPTV/DVB. It is a high-integration and cost efficient SOC for 4K HDR STB.

Quad-core Cortex-A53 is integrated with separate Neon and FPU coprocessor, also with shared L2 Cache. The Quad-core GPU supports high-resolution display and game.

Lots of high-performance interface to get very flexible solution, such as multi-channel display including HDMI2.0a and TV Encoder (CVBS). TrustZone and crypto hardware are integrated for security. 32bits DDR3/DDR3L/DDR4/LPDDR3 provides high memory bandwidth.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third-party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Quad-core ARM Cortex-A53 CPU
- Full implementation of the ARM architecture v8-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- In-order pipeline with symmetric dual-issue of most instructions
- Unified system L2 cache
- Include VFP v3 hardware to support single and double-precision operations
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- TrustZone technology support
- Full CoreSight debug solution
- One separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
    - PD_A53: Cortex-A53 + Neon + FPU + L1 I/D Cache of core 2/3
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
    - BootROM
    - Internal SRAM
- External off-chip memory$^{\text{①}}$
    - DDR3/DDR3L/LPDDR3/DDR4
    - SPI Flash
    - eMMC
    - SD

1.2.3 Internal Memory

- Internal BootRom
    - Support system boot from the following device:
        - ◆ SPI Flash interface
        - ◆ eMMC interface
        - ◆ SDMMC interface (SDMMC0 only)

- ■ Support system code download by the following interface:
  - ◆ USB OTG interface (Device mode)
- ● Internal SRAM
  - ■ Size: 36KB

1.2.4 External Memory or Storage device

- ● Dynamic Memory Interface (DDR3/DDR3L/LPDDR3/DDR4)
  - ■ Compatible with JEDEC standards
  - ■ Compatible with DDR3-1866 / DDR3L-1866 / LPDDR3 / DDR4
  - ■ Support 32-bit data width, 2 ranks (chip selects), max 4GB addressing space per rank; total addressing space is 4GB(max) also
  - ■ Programmable timing parameters to support SDRAM from various vendors
  - ■ Low power modes, such as power-down and self-refresh for SDRAM
  - ■ Compensation for board delays and variable latencies through programmable pipelines
  - ■ Programmable output and ODT impedance with dynamic PVT compensation

- ● eMMC Interface
  - ■ Compatible with standard iNAND interface
  - ■ Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
  - ■ Support block size from 1 to 65535Bytes
  - ■ Support three data bus width: 1-bit, 4-bit or 8-bit
  - ■ <mark>Support up to HS200; but not support CMD Queue and HS400</mark>

- ● SD/MMC Interface
  - ■ There are 2 SD/MMC interface
  - ■ Compatible with SD3.0, MMC ver4.51
  - ■ Support block size from 1 to 65535Bytes
  - ■ Data bus width is 4bits

1.2.5 System Component

- ● CRU (clock & reset unit)
  - ■ Support clock gating control for individual components
  - ■ One oscillator with 24MHz clock input
  - ■ Support global soft-reset control for whole SoC, also individual soft-reset for each component

- ● Timer
  - ■ Six 64bits timers with interrupt-based operation for non-secure application
  - ■ Two 64bits timers with interrupt-based operation for secure application
  - ■ Support two operation modes: free-running and user-defined count
  - ■ Support timer work state checkable

- ● PWM
  - ■ Four on-chip PWMs with interrupt-based operation
  - ■ Programmable pre-scaled operation to bus clock and then further scaled
  - ■ Embedded 32-bit timer/counter facility
  - ■ Support capture mode
  - ■ Support continuous mode or one-shot mode
  - ■ Provides reference mode and output various duty-cycle waveform

- ● Watchdog
  - ■ 32-bit watchdog counter
  - ■ Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - ■ WDT can perform two types of operations when timeout occurs:

- ◆ Generate a system reset
- ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- ■ Programmable reset pulse length
- ■ Totally 16 defined-ranges of main timeout period

- ● Interrupt Controller
  - ■ Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components
  - ■ Support 16 software-triggered interrupts
  - ■ Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A53, both are low-level sensitive
  - ■ Support different interrupt priority for each interrupt source, and they are always software-programmable

- ● Trust Execution Environment system
  - ■ Support TrustZone technology for the following components
    - ◆ Cortex-A53, support security and non-security mode, switch by software
    - ◆ BUS_DMAC, support some dedicated channels work only in security mode
    - ◆ Secure OTP, only can be accessed by Cortex-A53 in secure mode
    - ◆ Internal memory, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)

  - ■ Cipher engine
    - ◆ Support AES 128/192/256
    - ◆ Supports the DES (ECB and CBC modes) and TDES (EDE and DED) algorithms
    - ◆ Supports MD5, SHA-1 and SHA-256 HASH algorithms
    - ◆ Support PKA(RSA) 512/1024/2048 bit Exp Modulator
    - ◆ Support 160-bit Pseudo Random Number Generator (PRNG)
    - ◆ Support 256-bit True Random Number Generator (TRNG)
  - ■ Support secure OTP
  - ■ Support secure boot
  - ■ Support secure debug
  - ■ Support secure OS

1.2.6 Video CODEC

- ● Video Decoder
  - ■ MMU embedded
  - ■ Real-time decoding of MPEG-1/2/4, H.264, H.265/HEVC, VC-1, AVS, AVS+
  - ■
  - ■ H.264/AVC Base/Main/High/High10 profile @ level 5.1; up to 4Kx2K @ 60fps
  - ■ H.265/HEVC Main/Main10 profile @ level 5.1 High-tier; up to 4Kx2K @ 60fps
  - ■ VP9, up to 4Kx2K @ 60fps
  - ■ VP8, up to 1080P @ 60fps
  - ■ MPEG-1, ISO/IEC 11172-2, up to 1080P @ 60fps
  - ■ MPEG-2, ISO/IEC 13818-2, SP@ML, MP@HL, up to 1080P @ 60fps
  - ■ MPEG-4, ISO/IEC 14496-2, SP@L0-3, ASP@L0-5, up to 1080P @ 60fps
  - ■ VC-1, SP@ML, MP@HL, AP@L0-3, up to 1080P @ 60fps
  - ■ MVC is supported based on H.264 or H.265, up to 1080P @ 60fps

- ● H.264 Video Encoder
  - ■ Support video encoder for H.264 at BP/MP/HP @ level4.2
  - ■ Resolution and frame rate are up to 1920x1080 @ 30FPS[®]
  - ■ 1x1080p @ 30fps or 2x720p @ 30fps encoding
  - ■ Only support I and P slices, not B slices

- H.265 Video Encoder
  - Capable of encoding HEVC Main Profile @ L5.0 High-tier
  - Resolution and frame rate are up to 1920x1080 @ 30FPS^②
  - 1x1080p @ 30fps or 2x720p @ 30fps encoding
  - Only support I and P slices, not B slices
  - In-loop deblocking filtering
  - Loop filtering across slice
  - Noise reduction
  - Rate Control: VBR, CBR and ABR; ROI support

1.2.7 Audio CODEC

- MP3, AAC, WMA, FLAC, OGG, Dolby Digital, Dolby Digital Plus

1.2.8 JPEG CODEC

- JPEG decoder
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI (region of image) decode
  - Embedded memory management unit(MMU)

1.2.9 Image Enhancement Processor (IEP)

- Data format support
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - YUV up/down sampling

- De-interlace
  - Max resolution is up to 1920x1080
  - Configurable high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode

1.2.10 Graphics Engine

- 3D Graphics Engine:
  - OpenGL ES 1.1 and 2.0, OpenVG1.1

- 2D Graphics Engine:
  - Support Pixel Format conversion between BT.601 and BT.709
  - Max resolution is 3840x2160
  - BitBLT, operation with two data source
  - Color fill with gradient fill, and pattern fill
  - High-performance scaling and rotation concurrently
  - Monochrome expansion for text rendering
  - New comprehensive per-pixel alpha (color/alpha channel separately)
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, pattern mask, fading
  - Dither operation
  - 0, 90, 180 and 270-degree rotation
  - x-mirror and y-mirror rotation operation

1.2.11 Video input interface

- TS interface
  - Support one TS input channel (serial mode or parallel mode)
  - Support 4 TS input mode: sync/valid mode in the case of serial TS input, nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input
  - Supports 2 TS sources: demodulators and local memory
  - Supports one PTI (Programmable Transport Interface):

- ◆ 64 PID filters
- ◆ TS descrambling with 16 sets of Control Word under CSA v2.0 standard
- ◆ 16 PES/ES filters with PTS/DTS extraction and ES start code detection
- ◆ 4/8 PCR extraction channels
- ◆ 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
- ◆ PID done and error interrupts for each channel
- ◆ PCR/DTS/PTS extraction interrupt for each channel
- Supports 1 PVR (Personal Video Recording) output channel
- 1 built-in multi-channel DMA Controller
- Independent MMU for this module

- Camera Interface
  - Support up to 5M pixels
  - 8bits BT656(PAL/NTSC) interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422, YUV420 output format with separately Y and UV space
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

1.2.12 Display interface

- Display interface
  - Support HDMI 2.0a output up to 4K@60Hz
  - TV interface: TV encoder and DAC for CVBS

- HDMI
  - Compliant with HDMI 2.0a
  - Support up to 4k x 2k @ 60Hz
  - Support 3D video formats
  - Support 4K P60 YCbCr444, YCbCr422, YCbCr420 in 10-bit and 12-bit display
  - Support HDCP 1.4 and 2.2

- TV out interface
  - 10-bit resolution DAC
  - Composite (CVBS) output
  - 480i/576i standard definition output

1.2.13 Video Output Processor

- There is one VOP (Video Output Processor)
- 24-bit (RGB888 YCbCr444), 30-bit (RGB101010, YCbCr 420, YCbCr 444)
- Max output resolution 4K for HDMI, 480i/576i for CVBS
- 4 display layers:
- ◆ Display layers: Win0, Win1, HWC and background
- ◆ One background layer with programmable 24bits color
- ◆ There are two OSD/video layers (win0/win1)
  - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444,YCbCr 420 10bit，YCbCr 422 10bit，YCbCr 444 10bit
  - maximum resolution is 4096x2304, support virtual display
  - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
  - 256 level alpha blending (pre-multiplied alpha support)
  - Support transparency color key
  - Support BG, RG, RB swap, x/y mirror
  - Support TV Encoder for PAL and NTSC
  - YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
  - YCbCr2RGB(BT2020)

- RGB2YCbCr(BT601/BT709)
- RGB2YCbCr(BT2020)
- Conversion between BT2020 and BT709/601
- Win0 and Win1 layer overlay exchangeable
- Support replication (16bits to 24bits) and dithering (24bits to 16bits/ 18bits) operation
- Blank and blank display
- HDR is supported with HDR10 and HLG modes
- Support tone mapping between HDR and SDR, including HDR2SDR and SDR2HDR

1.2.14 Audio Interface

- I2S0/I2S1 with 8ch
  - I2S0/I2S1 supports up to 8 channels (8xTX or 8xRX)
  - I2S0 is connected to HDMI internally, while I2S1 is for external device
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- I2S2/PCM with 2ch
  - Up to 2 channels (2xTX and 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time

- PDM
  - Up to 8 channels

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support bi-phase format stereo audio data output
  - Support 16 to 31-bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20 and 24-bit audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

- Audio codec
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo
  - Integrated digital interpolation and decimation filter
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz

1.2.15 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- Smart Card
  - support card activation and deactivation
  - support cold/warm reset

- support Answer to Reset(ATR) response reception
- support T0 for asynchronous half-duplex character transmission
- support T1 for asynchronous half-duplex block transmission
- support automatic operating voltage class selection
- support adjustable clock rate and bit (baud) rate
- support configurable automatic byte repetition

- GMAC 10/100/1000M Ethernet Controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - There are 2 controllers, one is connected to internal FE PHY, the other is for external PHY device
  - Supports both full-duplex and half-duplex operation
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Handles automatic retransmission of Collision frames for transmission

- Ethernet PHY
  - Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
  - Supporting both full and half duplex for either 10 or 100 Mb/s data rate
  - Auto MDIX capable
  - Supports wake-on-LAN, EEE
  - 100Base-FX support
  - Supports auto-negotiation

- USB 2.0
  - Built-in 2 USB 2.0 interfaces, one supports OTG
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB 3.0 Host
  - Support up to 64 devices
  - Support 1 interrupter
  - Support 1 USB2.0 port and 1 Super-Speed port
  - Support standard or open-source xHCI and class driver
  - Support xHCI Debug Capability

- SPI interface
  - Support serial-master and serial-slave mode, software-configurable
  - Support 1 chip-select output in serial-master mode

- I2C interface
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus.

- UART Controller
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or another special baud rate
  - Support auto flow control mode

● One IR remote controller input channel

1.2.16 Others

● Multiple group of GPIO
  ■ All of GPIOs can be used to generate interrupt to CPU

● Temperature Sensor(TS-ADC)
  ■ The SAR ADC up to 50KS/s sampling rate
  ■ -20~120℃ temperature range and 5℃ temperature resolution

● OTP
  ■ Support standby mode
  ■ Provide inactive mode, VP must be 0V or Floating in this mode.

● Package Type
  ■ TFBGA395L (body: 14mm x 14mm; ball size: 0.3mm; ball pitch: 0.65mm)

Notes:
① *DDR3/LPDDR2/LPDDR3/DDR4 are not used simultaneously*
② *Actual maximum frame rate will depend on the clock frequency and system bus performance*
③ *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.3 Block Diagram

The following diagram shows the basic block diagram.
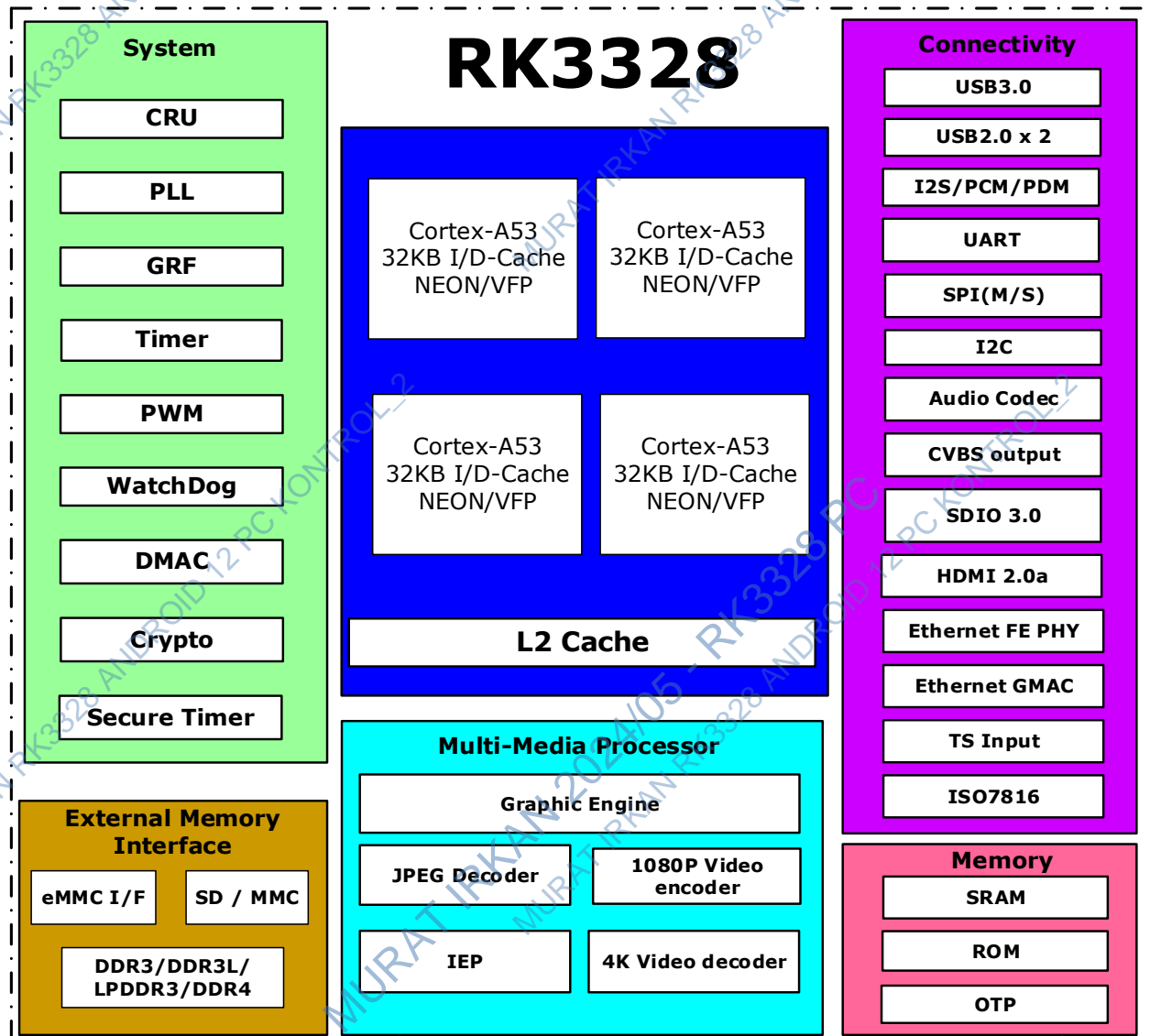
Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RK3328	RoHS	TFBGA395L	1190	4K Quad core processor with HDR

2.2 Top Marking

Rockchip

RK3328

ABCXXXXXX DEFG

The first pin

Rockchip : Brand Name

RKXXXX : Chip Name

ABC : Subcontractor Code
XXXXXX : Die Lot NO #
DEFG : Date Code
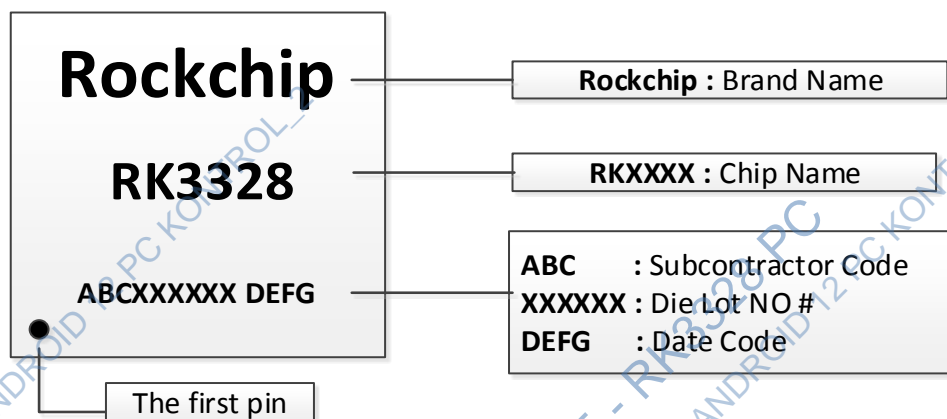
Fig.2-1 Package definition

2.3 TFBGA395L Dimension

PIN #1

A

D

B

2X

aaa C

E

aaa C

2X
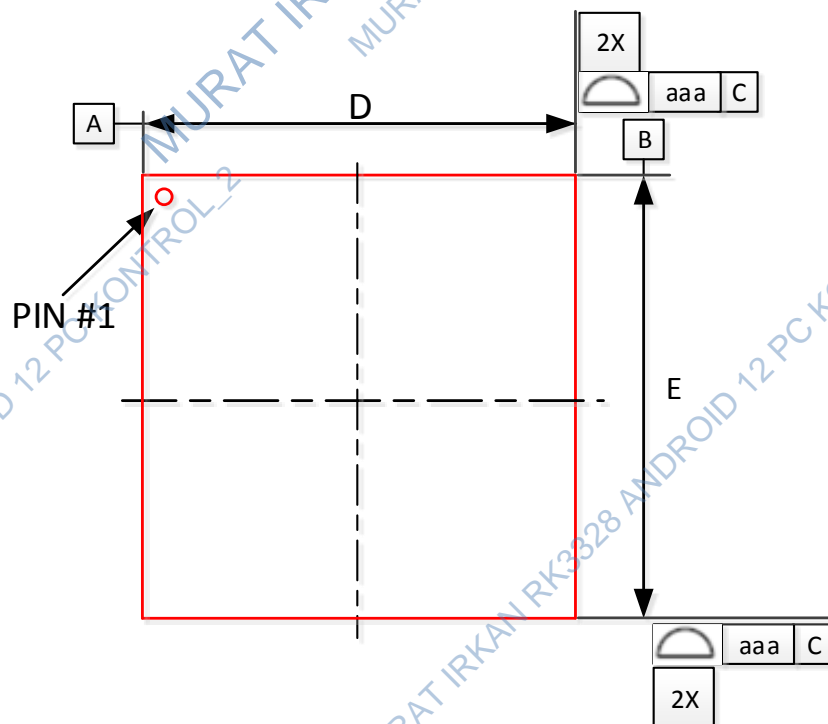
Fig.2-2 Package Top View
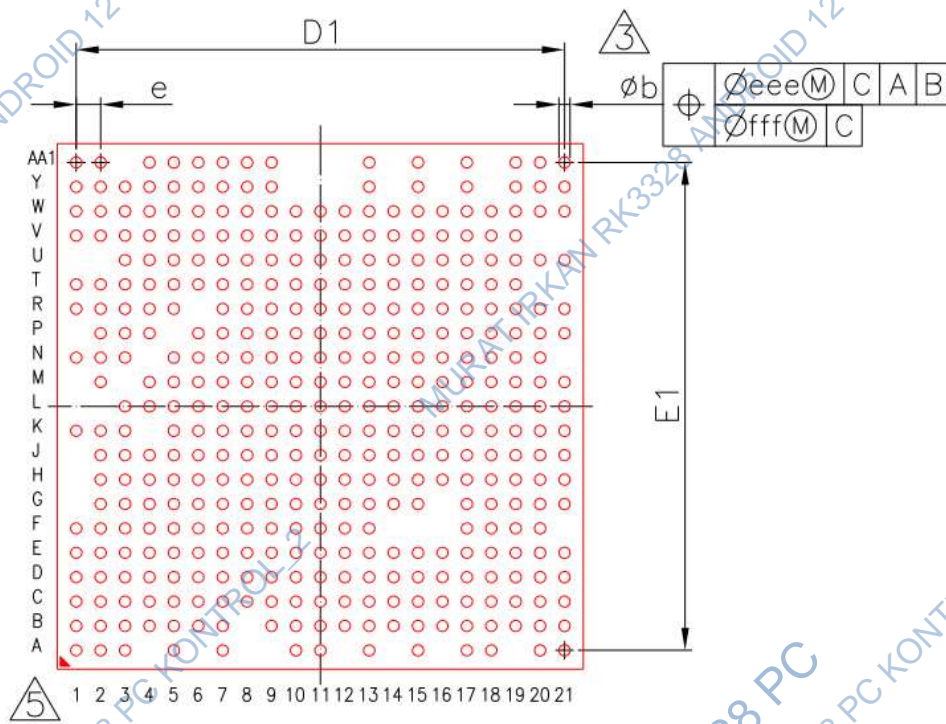
Fig.2-3 Package bottom view
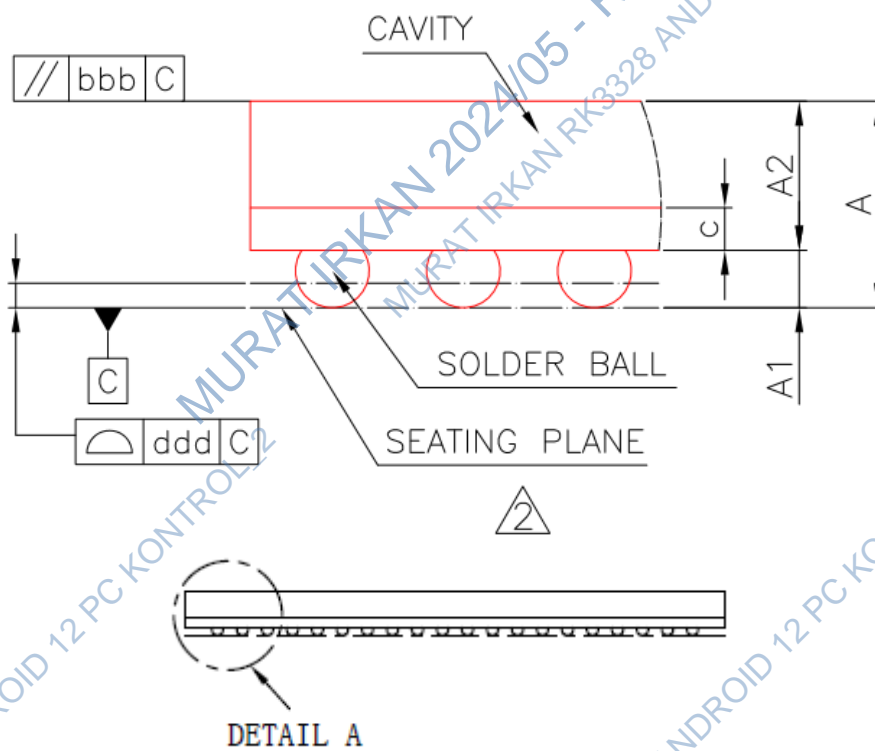
Fig.2-4 Package side view

Symbol	Dimension in mm			Dimension in inch		
	MIN	NORMAL	MAX	MIN	NORMAL	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
C	0.22	0.26	0.30	0.009	0.010	0.012
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	---	13.00	---	---	0.512	---
E1	---	13.00	---	---	0.512	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
ccc	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		

Fig.2-5 Package dimension

2.4 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS1	DDR_DQ7	DDR_DQS0_N	NP	DDR_DQS1_N	NP	DDR_DQ1	NP	NP	DDR_DQ21	DDR_DQ23	NP
B	DDR_DQ8	DDR_DQ3	DDR_DQS0_P	VSS3	DDR_DQS1_P	DDR_DM0	DDR_DQ6	NP	DDR_DQ4	DDR_DQ11	DDR_DQ20	DDR_DQ19
C	VSS6	DDR_DQ10	VSS7	DDR_DQ14	DDR_DQ2	VSS8	DDR_DQ5	DDR_DQ9	VSS9	DDR_DQ13	VSS10	DDR_DQ24
D	GPIO3_A5/TSP_D1/...	GPIO3_A1/TSP_FAIL/...	VSS15	DDR_DQ12	DDR_DM1	VSS16	DDR_DQ0	VSS17	DDR_DQ15	DDR_DM3	VSS18	DDR_DQ28
E	GPIO3_A2/TSP_CLK/...	GPIO3_A4/TSP_D0/...	GPIO3_A0/TSP_VALID/...	VSS22	VSS23	VSS24	VSS25	VSS26	VSS27	VSS28	VSS29	VSS30
F	GPIO3_A7/TSP_D3/...	GPIO3_A6/TSP_D2/...	GPIO3_B0/TSP_D4...	VSS37	VSS38	VSS39	VSS40	VSS41	VSS42	VDD_DDRIO_1	VDD_DDRIO_2	VDD_DDRIO_3
G	NP	VSS45	VSS46	VSS47	USB30_EXTR	VSS48	VSS49	VSS50	VSS51	VDD_DDRIO_5	VDD_DDRIO_6	VDD_DDRIO_7
H	NP	USB30_TXN	USB30_TXP	VSS56	PLL_AVDD_1V8	VCCIO6	PLL_DVDD_1V0	VSS57	VSS58	VSS59	VSS60	VSS61
J	NP	USB30_RXP	USB30_RXN	VSS66	USB30_AVDD_1V8	USB30_AVDD_3V3	USB30_DVDD_1V0	VSS67	VSS68	VSS69	VSS70	VSS71
K	USB30_DP	USB30_DM	VSS76	NP	VSS77	VCCIO_PMU	USB30_VBUS	VSS78	VSS79	VSS80	VSS81	VSS82
L	NP	NP	GPIO0_A0/...	VSS86	VSS87	VSS88	VSS89	VSS90	VSS91	VSS92	VSS93	VSS94
M	NP	VDAC_IOUT	NP	HDMI_EXTR	VDD_PMU	HDMI_AVDD_1V0	VSS101	VSS102	VSS103	VSS104	VSS105	VSS106

	1	2	3	4	5	6	7	8	9	10	11	12
N	CODEC_AOR	GPIO_MUTE	VSS109	NP	CODEC_AVDD_1V8	VDAC_AVDD_1V8	VSS110	VSS111	VDD_LOGIC_1	VDD_LOGIC_2	VDD_LOGIC_3	VSS112
P	NP	CODEC_AOL	VSS116	VDAC_IREF	NP	HDMI_AVDD_1V8	VSS117	VSS118	VDD_LOGIC_4	VDD_LOGIC_5	VDD_LOGIC_6	VSS119
R	XIN24M	VSS121	GPIO0_A2/...	CODEC_AVSS	VSS122	NP	VSS123	VSS124	VDD_LOGIC_7	VDD_LOGIC_8	VDD_LOGIC_9	VSS125
T	XOUT24M	VSS127	VSS128	CODEC_VCM	USB20_AVDD_3V3	USB20_VBUS	VCCIO1	VSS129	VSS130	VSS131	VSS132	VSS133
U	NP	NP	GPIO0_A4/HDMI_HPD	VSS134	USB20_AVDD_1V8	FEPHY_AVDD_1V8	VCCIO3	VSS135	VSS136	GPIO1_A0/...	VSS137	VCCIO4
V	I2C3_SCL/HDMI_SCL	HDMI_CEC	I2C3_SDA/HDMI_SDA	VSS141	USB20_DVDD_1V0	FEPHY_AVDD_1V0	FEPHY_EXTRES	VSS142	GPIO0_D3/SPDIF_TX_M0	GPIO1_A5...	VSS143	GPIO1_D2/...
W	VSS144	HDMI_TXCLKN	VSS145	VSS146	VSS147	USB20_EXTR	VSS148	VSS149	VSS150	GPIO0_D6/...	GPIO1_A1/...	GPIO1_A6/...
Y	HDMI_TXCLKP	HDMI_TX0N	HDMI_TX1N	HDMI_TX1P	HDMI_TX2P	USB0_DM	USB1_DM	FEPHY_RXP	FEPHY_TXP	NP	NP	NP
AA	VSS151	HDMI_TX0P	NP	HDMI_TX2N	VSS152	USB0_DP	USB1_DP	FEPHY_RXN	FEPHY_TXN	NP	NP	NP

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

13	14	15	16	17	18	19	20	21	
DDR_DQS2_N	NP	DDR_DQS3_N	NP	DDR_DQ31	DDR_DQ30	NP	DDR3_CLKN/DDR4_CLKN	VSS2	A
DDR_DQS2_P	VSS4	DDR_DQS3_P	VSS5	DDR_DQ22	DDR_DQ27	DDR_DQ26	DDR3_CLKP/DDR4_CLKP	DDR3_RESETn/DDR4_RESETN	B
DDR_DQ29	VSS11	DDR_DQ17	DDR_DQ18	VSS12	VSS13	VSS14	DDR3_CSN0/DDR4_ACTn	DDR3_BA0/DDR4_BG0	C
DDR_DQ25	VSS19	DDR_DM2	DDR_DQ16	VSS20	VSS21	DDR3_RASn/DDR4_CKE	DDR3_A7/DDR4_A11	DDR3_A5/DDR4_A8	D
VSS31	VSS32	VSS33	VSS34	VSS35	DDR3_ODT0/DDR4_Wen/DDR4_A14	VSS36	DDR3_A3/DDR4_A6	DDR3_BA2/DDR4_BA0	E
VDD_DDRIO_4	NP	NP	NP	VSS43	DDR3_A13/DDR4_A2	DDR3_A9/DDR4_A0	VSS44	NP	F
VDD_DDRIO_8	VSS52	VSS53	NP	VSS54	VSS55	DDR3_A0/DDR4_A10	DDR3_A11/DDR4_A3	DDR3_A14/DDR4_A1	G
VSS62	VSS63	VSS64	VDD_DDRIO_9	VSS65	DDR3_A2/DDR4_A4	DDR3_WEn/DDR4_BG1	DDR3_A6/DDR4_A7	DDR3_A4/DDR4_A5	H
VSS72	VSS73	VDD_DDRIO_10	VDD_DDRIO_11	VSS74	DDR3_CASn/DDR4_A12	DDR3_A15/DDR4_ODT0	VSS75	DDR3_A12/DDR4_BA1	J
VSS83	VSS84	VDD_DDRIO_12	VDD_DDRIO_13	VSS85	DDR3_A1/DDR4_A9	DDR3_A8/DDR4_A13	DDR3_BA1/DDR4_CASn/DDR4_A15	DDR3_A10/DDR4_CS0n	K
VSS95	VSS96	VSS97	VSS98	VSS99	DDR3_CSN1/DDR4_CS1N	DDR3_ODT1/DDR4_ODT1	DDR3_CKE/DDR4_RASn/DDR4_A16	VSS100	L
VSS107	VSS108	TEST	SARADC_AVDD_1V8	SARADC_IN1	SARADC_IN0	GPIO2_A6/PWM2	GPIO2_D2/USB20_DRV	GPIO2_A2/IR_RX/POWERSTATE2	M

13	14	15	16	17	18	19	20	21	
VSS113	VSS114	VSS115	OTP_VCC18	GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0	GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1	GPIO2_A4/PWM0/I2C1_SDA	GPIO2_A5/PWM1/I2C1_SCL	NP	N
VDD_CORE_1	VDD_CORE_2	VSS120	EFUSE_VP	GPIO2_D0/I2C0_SCL/FEPHY_LED_LINK_M1	GPIO2_C1/I2S1_LRCK_TX/SPDIF_TX_M1/TSP_D6_M1/CIF_D6_M1	GPIO2_A0/UART2_TX_M1/POWERSTATE0	GPIO2_A1/UART2_RX_M1/POWERSTATE1	NPOR	P
VDD_CORE_3	VDD_CORE_4	VSS126	VCCIO5	GPIO2_D1/I2C0_SDA/FEPHY_LED_DATA_M1	GPIO2_C2/I2S1_SCLK/PDM_CLK_M0/TSP_D7_M1/CIF_D7_M1	GPIO3_C6/EMMC_PWREN	GPIO3_C3/EMMC_CMD	GPIO3_C5/EMMC_CLKOUT	R
VDD_CORE_5	VDD_CORE_6	VDD_CORE_7	GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL	VCCIO2	GPIO3_C1/EMMC_D6	GPIO3_C2/EMMC_D7	NP	NP	T
VSS138	VSS139	VSS140	GPIO2_C3/I2S1_SDI/PDM_SDIO_M0/CARD_CLK_M1	GPIO2_A3/EFUSE_PWREN/POWERSTATE3	GPIO2_D7/EMMC_D4	GPIO0_A7/EMMC_D0	GPIO2_D4/EMMC_D1	GPIO2_D5/EMMC_D2	U
GPIO1_B3/UART0_CTSN/GMAC_RXD0_M1	GPIO1_D4/CLK32KOUT_M1	GPIO2_C0/I2S1_LRCK_RX/TSP_D5_M1/CIF_D5_M1	GPIO2_C6/I2S1_SDIO3/PDM_SDI3_M0/CARD_IO_M1	GPIO2_C5/I2S1_SDIO2/PDM_SDI2_M0/CARD_DET_M1	GPIO2_C4/I2S1_SDIO1/PDM_SDI1_M0/CARD_RST_M1	GPIO2_D6/EMMC_D3	NP	NP	V
GPIO1_A2/SDMMC0_D2/JTAG_TCK	GPIO1_B2/UART0_RTSN/GMAC_RXD1_M1	GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1	GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1	GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDI0_M1	GPIO1_B7/SDMMC1_D1/GMAC_RXD2_M1	GPIO1_B6/SDMMC1_D0/GMAC_RXD3_M1	GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1	GPIO3_C0/EMMC_D5	W
GPIO1_A4/SDMMC0_CMD	NP	GPIO1_B0/UART0_RX/GMAC_TXD1_M1	NP	GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDI2_M1	NP	GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1	GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1	GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1	Y
GPIO1_A3/SDMMC0_D3/JTAG_TMS	NP	GPIO1_B1/UART0_TX/GMAC_TXD0_M1	NP	GPIO1_D0/I2S2_SDI_M0/GMAC_RXER_M1/PDM_SDI1_M1	NP	GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1	GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1	VSS153	AA
13	14	15	16	17	18	19	20	21	

Fig.2-6 Ball Map

2.5 Pin Number Order

Table 2-1 Pin Number Order Information

No.	Pin name	No.	Pin name
A1	VSS1	B10	DDR_DQ11
A2	DDR_DQ7	B11	DDR_DQ20
A3	DDR_DQS0_N	B12	DDR_DQ19
A5	DDR_DQS1_N	B13	DDR_DQS2_P
A7	DDR_DQ1	B14	VSS4
A10	DDR_DQ21	B15	DDR_DQS3_P
A11	DDR_DQ23	B16	VSS5
A13	DDR_DQS2_N	B17	DDR_DQ22
A15	DDR_DQS3_N	B18	DDR_DQ27
A17	DDR_DQ31	B19	DDR_DQ26
A18	DDR_DQ30	B20	DDR3_CLKP/DDR4_CLKP
A20	DDR3_CLKN/DDR4_CLKN	B21	DDR3_RESETn/DDR4_RESETN
A21	VSS2	C1	VSS6
AA1	VSS151	C2	DDR_DQ10
AA13	GPIO1_A3/SDMMC0_D3/JTAG_TMS	C3	VSS7
AA15	GPIO1_B1/UART0_TX/GMAC_TXD0_M1	C4	DDR_DQ14
AA17	GPIO1_D0/I2S2_SDI_M0/GMAC_RXER_M1/PDM_SDI1_M1	C5	DDR_DQ2
AA19	GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1	C6	VSS8
AA2	HDMI_TX0P	C7	DDR_DQ5
AA20	GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1	C8	DDR_DQ9
AA21	VSS153	C9	VSS9
AA4	HDMI_TX2N	C10	DDR_DQ13
AA5	VSS152	C11	VSS10
AA6	USB0_DP	C12	DDR_DQ24
AA7	USB1_DP	C13	DDR_DQ29
AA8	FEPHY_RXN	C14	VSS11
AA9	FEPHY_TXN	C15	DDR_DQ17
B1	DDR_DQ8	C16	DDR_DQ18
B2	DDR_DQ3	C17	VSS12
B3	DDR_DQS0_P	C18	VSS13
B4	VSS3	C19	VSS14
B5	DDR_DQS1_P	C20	DDR3_CSN0/DDR4_ACTn
B6	DDR_DM0	C21	DDR3_BA0/DDR4_BG0
B7	DDR_DQ6	D1	GPIO3_A5/TSP_D1/CIF_D1/SDMMC0EXT_D1/UART1_RTSN/USB3PHY_DEBUG5
B9	DDR_DQ4	D2	GPIO3_A1/TSP_FAIL/CIF_HREF/SDMMC0EXT_DET/SPI_TXD_M2/USB3PHY_DEBUG2/I2S2_SDO_M1

No.	Pin name	No.	Pin name
D3	VSS15	E17	VSS35
D4	DDR_DQ12	E18	DDR3_ODT0/DDR4_Wen/DDR4_A14
D5	DDR_DM1	E19	VSS36
D6	VSS16	E20	DDR3_A3/DDR4_A6
D7	DDR_DQ0	E21	DDR3_BA2/DDR4_BA0
D8	VSS17	F1	GPIO3_A7/TSP_D3/CIF_D3/SDMMC0EXT_D3/UART1_CTSN/USB3PHY_DEBUG7
D9	DDR_DQ15	F2	GPIO3_A6/TSP_D2/CIF_D2/SDMMC0EXT_D2/UART1_RX/USB3PHY_DEBUG6
D10	DDR_DM3	F3	GPIO3_B0/TSP_D4/CIF_D4/SPI_CSN0_M2/I2S2_LRCK_TX_M1/USB3PHY_DEBUG8/I2S2_LRCK_RX_M1
D11	VSS18	F4	VSS37
D12	DDR_DQ28	F5	VSS38
D13	DDR_DQ25	F6	VSS39
D14	VSS19	F7	VSS40
D15	DDR_DM2	F8	VSS41
D16	DDR_DQ16	F9	VSS42
D17	VSS20	F10	VDD_DDRIO_1
D18	VSS21	F11	VDD_DDRIO_2
D19	DDR3_RASn/DDR4_CKE	F12	VDD_DDRIO_3
D20	DDR3_A7/DDR4_A11	F13	VDD_DDRIO_4
D21	DDR3_A5/DDR4_A8	F17	VSS43
E1	GPIO3_A2/TSP_CLK/CIF_CLKIN/SDMMC0EXT_CLK/SPI_RXD_M2/USB3PHY_DEBUG3/I2S2_SDI_M1	F18	DDR3_A13/DDR4_A2
E2	GPIO3_A4/TSP_D0/CIF_D0/SDMMC0EXT_D0/UART1_TX/USB3PHY_DEBUG4	F19	DDR3_A9/DDR4_A0
E3	GPIO3_A0/TSP_VALID/CIF_VSYNC/SDMMC0EXT_CMD/SPI_CLK_M2/USB3PHY_DEBUG1/I2S2_SCLK_M1	F20	VSS44
E4	VSS22	G2	VSS45
E5	VSS23	G3	VSS46
E6	VSS24	G4	VSS47
E7	VSS25	G5	USB30_EXTR
E8	VSS26	G6	VSS48
E9	VSS27	G7	VSS49
E10	VSS28	G8	VSS50
E11	VSS29	G9	VSS51
E12	VSS30	G10	VDD_DDRIO_5
E13	VSS31	G11	VDD_DDRIO_6
E14	VSS32	G12	VDD_DDRIO_7
E15	VSS33	G13	VDD_DDRIO_8
E16	VSS34	G14	VSS52

No.	Pin name	No.	Pin name
G15	VSS53	J11	VSS70
G17	VSS54	J12	VSS71
G18	VSS55	J13	VSS72
G19	DDR3_A0/DDR4_A10	J14	VSS73
G20	DDR3_A11/DDR4_A3	J15	VDD_DDRIO_10
G21	DDR3_A14/DDR4_A1	J16	VDD_DDRIO_11
H2	USB30_TXN	J17	VSS74
H3	USB30_TXP	J18	DDR3_CASn/DDR4_A12
H4	VSS56	J19	DDR3_A15/DDR4_ODT0
H5	PLL_AVDD_1V8	J20	VSS75
H6	VCCIO6	J21	DDR3_A12/DDR4_BA1
H7	PLL_DVDD_1V0	K1	USB30_DP
H8	VSS57	K2	USB30_DM
H9	VSS58	K3	VSS76
H10	VSS59	K5	VSS77
H11	VSS60	K6	VCCIO_PMU
H12	VSS61	K7	USB30_VBUS
H13	VSS62	K8	VSS78
H14	VSS63	K9	VSS79
H15	VSS64	K10	VSS80
H16	VDD_DDRIO_9	K11	VSS81
H17	VSS65	K12	VSS82
H18	DDR3_A2/DDR4_A4	K13	VSS83
H19	DDR3_WEn/DDR4_BG1	K14	VSS84
H20	DDR3_A6/DDR4_A7	K15	VDD_DDRIO_12
H21	DDR3_A4/DDR4_A5	K16	VDD_DDRIO_13
J2	USB30_RXP	K17	VSS85
J3	USB30_RXN	K18	DDR3_A1/DDR4_A9
J4	VSS66	K19	DDR3_A8/DDR4_A13
J5	USB30_AVDD_1V8	K20	DDR3_BA1/DDR4_CASn/DDR4_A15
J6	USB30_AVDD_3V3	K21	DDR3_A10/DDR4_CS0n
J7	USB30_DVDD_1V0	L3	GPIO0_A0/CLKOUT_WIFI_M0
J8	VSS67	L4	VSS86
J9	VSS68	L5	VSS87
J10	VSS69	L6	VSS88

No.	Pin name	No.	Pin name
L7	VSS89	N6	VDAC_AVDD_1V8
L8	VSS90	N7	VSS110
L9	VSS91	N8	VSS111
L10	VSS92	N9	VDD_LOGIC_1
L11	VSS93	N10	VDD_LOGIC_2
L12	VSS94	N11	VDD_LOGIC_3
L13	VSS95	N12	VSS112
L14	VSS96	N13	VSS113
L15	VSS97	N14	VSS114
L16	VSS98	N15	VSS115
L17	VSS99	N16	OTP_VCC18
L18	DDR3_CSN1/DDR4_CS1N	N17	GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0
L19	DDR3_ODT1/DDR4_ODT1	N18	GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1
L20	DDR3_CKE/DDR4_RASn/DDR4_A16	N19	GPIO2_A4/PWM0/I2C1_SDA
L21	VSS100	N20	GPIO2_A5/PWM1/I2C1_SCL
M2	VDAC_IOUT	P2	CODEC_AOL
M4	HDMI_EXTR	P3	VSS116
M5	VDD_PMU	P4	VDAC_IREF
M6	HDMI_AVDD_1V0	P6	HDMI_AVDD_1V8
M7	VSS101	P7	VSS117
M8	VSS102	P8	VSS118
M9	VSS103	P9	VDD_LOGIC_4
M10	VSS104	P10	VDD_LOGIC_5
M11	VSS105	P11	VDD_LOGIC_6
M12	VSS106	P12	VSS119
M13	VSS107	P13	VDD_CORE_1
M14	VSS108	P14	VDD_CORE_2
M15	TEST	P15	VSS120
M16	SARADC_AVDD_1V8	P16	EFUSE_VP
M17	SARADC_IN1	P17	GPIO2_D0/I2C0_SCL/FEPHY_LED_LINK_M1
M18	SARADC_IN0	P18	GPIO2_C1/I2S1_LRCK_TX/SPDIF_TX_M1/TSP_D6_M1/CIF_D6_M1
M19	GPIO2_A6/PWM2	P19	GPIO2_A0/UART2_TX_M1/POWERSTATE0
M20	GPIO2_D2/USB20_DRV	P20	GPIO2_A1/UART2_RX_M1/POWERSTATE1
M21	GPIO2_A2/IR_RX/POWERSTATE2	P21	NPOR
N1	CODEC_AOR	R1	XIN24M
N2	GPIO_MUTE	R2	VSS121
N3	VSS109	R3	GPIO0_A2/CLKOUT_GMAC_M0/SPDIF_TX_M2
N5	CODEC_AVDD_1V8	R4	CODEC_AVSS

No.	Pin name	No.	Pin name
R5	VSS122	U3	GPIO0_A4/HDMI_HPD
R7	VSS123	U4	VSS134
R8	VSS124	U5	USB20_AVDD_1V8
R9	VDD_LOGIC_7	U6	FEPHY_AVDD_1V8
R10	VDD_LOGIC_8	U7	VCCIO3
R11	VDD_LOGIC_9	U8	VSS135
R12	VSS125	U9	VSS136
R13	VDD_CORE_3	U10	GPIO1_A0/SDMMC0_D0/UART2_TX_M0
R14	VDD_CORE_4	U11	VSS137
R15	VSS126	U12	VCCIO4
R16	VCCIO5	U13	VSS138
R17	GPIO2_D1/I2C0_SDA/FEPHY_LED_DATA_M1	U14	VSS139
R18	GPIO2_C2/I2S1_SCLK/PDM_CLK_M0/TSP_D7_M1/CIF_D7_M1	U15	VSS140
R19	GPIO3_C6/ EMMC_PWREN	U16	GPIO2_C3/I2S1_SDI/PDM_SDI0_M0/CARD_CLK_M1
R20	GPIO3_C3/ EMMC_CMD	U17	GPIO2_A3/EFUSE_PWREN/POWERSTATE3
R21	GPIO3_C5/ EMMC_CLKOUT	U18	GPIO2_D7/ EMMC_D4
T1	XOUT24M	U19	GPIO0_A7/ EMMC_D0
T2	VSS127	U20	GPIO2_D4/ EMMC_D1
T3	VSS128	U21	GPIO2_D5/ EMMC_D2
T4	CODEC_VCM	V1	I2C3_SCL/HDMI_SCL
T5	USB20_AVDD_3V3	V2	HDMI_CEC
T6	USB20_VBUS	V3	I2C3_SDA/HDMI_SDA
T7	VCCIO1	V4	VSS141
T8	VSS129	V5	USB20_DVDD_1V0
T9	VSS130	V6	FEPHY_AVDD_1V0
T10	VSS131	V7	FEPHY_EXTRES
T11	VSS132	V8	VSS142
T12	VSS133	V9	GPIO0_D3/SPDIF_TX_M0
T13	VDD_CORE_5	V10	GPIO1_A5/SDMMC0_DETN
T14	VDD_CORE_6	V11	VSS143
T15	VDD_CORE_7	V12	GPIO1_D2/I2S2_LRCK_RX_M0/CLKOUT_GMAC_M2/PDM_SDI3_M1
T16	GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL	V13	GPIO1_B3/UART0_CTSN/GMAC_RXD0_M1
T17	VCCIO2	V14	GPIO1_D4/CLK32KOUT_M1
T18	GPIO3_C1/ EMMC_D6	V15	GPIO2_C0/I2S1_LRCK_RX/TSP_D5_M1/CIF_D5_M1
T19	GPIO3_C2/ EMMC_D7	V16	GPIO2_C6/I2S1_SDIO3/PDM_SDI3_M0/CARD_IO_M1

No.	Pin name	No.	Pin name
V17	GPIO2_C5/I2S1_SDIO2/PDM_SDI2_M0/CARD_DET_M1	Y8	FEPHY_RXP
V18	GPIO2_C4/I2S1_SDIO1/PDM_SDI1_M0/CARD_RST_M1	Y9	FEPHY_TXP
V19	GPIO2_D6/ EMMC_D3	Y13	GPIO1_A4/SDMMC0_CMD
W1	VSS144	Y15	GPIO1_B0/UART0_RX/GMAC_TXD1_M1
W2	HDMI_TXCLKN	Y17	GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDI2_M1
W3	VSS145	Y19	GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1
W4	VSS146	Y20	GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1
W5	VSS147	Y21	GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1
W6	USB20_EXTR		
W7	VSS148		
W8	VSS149		
W9	VSS150		
W10	GPIO0_D6/FEPHY_LED_SPEED10/SDMMC0_PWREN_M1		
W11	GPIO1_A1/SDMMC0_D1/UART2_RX_M0		
W12	GPIO1_A6/SDMMC0_CLK/TEST_CLK0		
W13	GPIO1_A2/SDMMC0_D2/JTAG_TCK		
W14	GPIO1_B2/UART0_RTSN/GMAC_RXD1_M1		
W15	GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1		
W16	GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1		
W17	GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDI0_M1		
W18	GPIO1_B7/SDMMC1_D1/GMAC_RXD2_M1		
W19	GPIO1_B6/SDMMC1_D0/GMAC_RXD3_M1		
W20	GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1		
W21	GPIO3_C0/EMMC_D5		
Y1	HDMI_TXCLKP		
Y2	HDMI_TX0N		
Y3	HDMI_TX1N		
Y4	HDMI_TX1P		
Y5	HDMI_TX2P		
Y6	USB0_DM		
Y7	USB1_DM		

2.6 Power/Ground IO Description

RK3328 ARM ŞASE(GND)

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
GND	A1 A21 AA1 AA21 AA5 B4 B14 B16 C1 C3 C6 C9 C11 C14 C17 C18 C19 D3 D6 D8 D11 D14 D17 D18 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E19 F4 F5 F6 F7 F8 F9 F17 F20 G2 G3 G4 G6 G7 G8 G9 G14 G15 G17 G18 H4 H8 H9 H10 H11 H12 H13 H14 H15 H17 J4 J8 J9 J10 J11 J12 J13 J14 J17 J20 K3 K5 K8 K9 K10 K11 K12 K13 K14 K17 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 L16 L17 L21 M7 M8 M9 M10 M11 M12 M13 M14 N3 N7 N8 N12 N13 N14 N15 P3 P7 P8 P12 P15 R2 R5 R7 R8 R12 R15 T2 T3 T8 T9 T10 T11 T12 U4 U8 U9 U11 U13 U14 U15 V4 V8 V11 W1 W3 W4 W5 W7 W8 W9	Internal Core Ground, Digital IO Ground,
VDD_CORE	H5 J5 J6 M6 M16 N5 N6 P6 T5 U5 U6 V6	ARM Core Power
VDD_LOGIC	M5 N9 N10 N11 P9 P10 P11 P13 P14 R9 R10 R11 R13 R14 T13 T14 T15	GPU, Logic Power
VCCIO1	T7	VCCIO1 Power Domain Power
VCCIO2	T17	VCCIO2 Power Domain Power
VCCIO3	U7	VCCIO3 Power Domain Power
VCCIO4	U12	VCCIO4 Power Domain Power
VCCIO5	R16	VCCIO5 Power Domain Power
VCCIO6	H6	VCCIO6 Power Domain Power
VCCIO_PMU	K6	PMU VCCIO Power Domain Power
VDD_DDRIO	F10 F11 F12 F13 G10 G11 G12 G13 H16 J15 J16 K15 K16	DDR PHY Power
PLL_DVDD_1V0	H7	PLL digital Power
PLL_AVDD_1V8	H5	PLL IO Power
USB20_DVDD_1V0	V5	USB OTG2.0/Host2.0 Digital Power
USB20_AVDD_1V8	U5	USB OTG2.0/Host2.0 Analog Power
USB20_AVDD_3V3	T5	USB OTG2.0/Host2.0 Analog Power
USB30_DVDD_1V0	J7	USB 3.0 Digital Power
USB30_AVDD_1V8	J5	USB 3.0 Analog Power
USB30_AVDD_3V3	J6	USB 3.0 Analog Power

Group	Ball#	Descriptions
CODEC_AVDD_1V8	N5	Audio Codec Analog Power
CODEC_AVSS	R4	Audio Codec Analog Ground
HDMI_AVDD_1V0	M6	HDMI PHY Analog Power
HDMI_AVDD_1V8	P6	HDMI PHY Analog Power
FEPHY_AVDD_1V0	V6	FEPHY Logic Analog Power
FEPHY _AVDD_1V8	U6	FEPHY Analog Power
VDAC_AVDD_1V8	N6	VDAC Analog Power

2.7 Function IO Description

Table 2-3 Function IO description

Pin Name	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	IO Type	IO Def	Pull	Default Current	INT
GPIO0_A0/CLKOUT_WIFI_M0	gpio0_a0	clkout_wifim0					I/O	I	down	4mA	√
GPIO0_A2/CLKOUT_GMAC_M0/SPDIF_TX_M2	gpio0_a2	clkout_gmacm0	spdif_txm2				I/O	I	down	4mA	√
GPIO0_A4/HDMI_HPD	gpio0_a4	hdmi_hpd					I/O	I	down	4mA	√
GPIO0_D3/SPDIF_TX_M0	gpio0_d3	spdif_txm0					I/O	I	down	4mA	√
GPIO0_D6/FEPHYLED_SPEED10/FEPHYLED_DUPLEX/SDMMC0_PWREN_M1	gpio0_d6	fephyled_speed10	fephyled_duplex	sdmmc0_pwrenm1			I/O	I	down	4mA	√
GPIO1_A0/SDMMC0_D0/UART2_TX_M0	gpio1_a0	sdmmc0_d0	uart2dbg_txm0				I/O	I	up	8mA	√
GPIO1_A1/SDMMC0_D1/UART2_RX_M0	gpio1_a1	sdmmc0_d1	uart2dbg_rxm0				I/O	I	up	8mA	√
GPIO1_A2/SDMMC0_D2/JTAG_TCK	gpio1_a2	sdmmc0_d2	jtag_tck				I/O	I	up	8mA	√
GPIO1_A3/SDMMC0_D3/JTAG_TMS	gpio1_a3	sdmmc0_d3	jtag_tms				I/O	I	up	8mA	√
GPIO1_A4/SDMMC0_CMD	gpio1_a4	sdmmc0_cmd					I/O	I	up	8mA	√
GPIO1_A5/SDMMC0_DETN	gpio1_a5	sdmmc0_detn					I/O	I	up	8mA	√
GPIO1_A6/SDMMC0_CLKOUT/TEST_CLK0	gpio1_a6	sdmmc0_clkout	test_clk0				I/O	I	down	8mA	√
GPIO1_B0/UART0_RX/GMAC_TXD1_M1	gpio1_b0	uart0_rx	gmac_txd1m1				I/O	I	up	4mA	√
GPIO1_B1/UART0_TX/GMAC_TXD0_M1	gpio1_b1	uart0_tx	gmac_txd0m1				I/O	I	up	4mA	√
GPIO1_B2/UART0_RTSN/GMAC_RXD1_M1	gpio1_b2	uart0_rtsn	gmac_rxd1m1				I/O	I	down	4mA	√
GPIO1_B3/UART0_CTSN/GMAC_RXD0_M1	gpio1_b3	uart0_ctsn	gmac_rxd0m1				I/O	I	down	4mA	√
GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1	gpio1_b4	sdmmc1_clkout	gmac_txclkm1				I/O	I	down	8mA	√
GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1	gpio1_b5	sdmmc1_cmd	gmac_rxclkm1				I/O	I	up	8mA	√
GPIO1_B6/SDMMC1_D0/GMAC_RXD3_M1	gpio1_b6	sdmmc1_d0	gmac_rxd3m1				I/O	I	up	8mA	√
GPIO1_B7/SDMMC1_D1/GMAC_RXD2_M1	gpio1_b7	sdmmc1_d1	gmac_rxd2m1				I/O	I	up	8mA	√
GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1	gpio1_c0	sdmmc1_d2	gmac_txd3m1				I/O	I	up	8mA	√
GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1	gpio1_c1	sdmmc1_d3	gmac_txd2m1				I/O	I	up	8mA	√
GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1	gpio1_c2	sdmmc1_pwren	gmac_crsm1				I/O	I	down	4mA	√
GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1	gpio1_c3	sdmmc1_detn	gmac_mdiom1	pdm_fsyncm1			I/O	I	up	4mA	√

Pin Name	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	IO Type	IO Def	Pull	Default Current	INT
GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1	gpio1_c5	i2s2_mclk	gmac_clkm1				I/O	I	down	4mA	√
GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1	gpio1_c6	i2s2_sclkm0	gmac_rxdvm1	pdm_clkm1			I/O	I	up	4mA	√
GPIO1_C7/I2S2_LRCKTX_M0/GMAC_MDC_M1/PDM_SDI0_M1	gpio1_c7	i2s2_lrcktxm0	gmac_mdcm1	pdm_sdi0m1			I/O	I	down	4mA	√
GPIO1_D0/I2S2_SDI_M0/GMAC_RXER_M1/PDM_SDI1_M1	gpio1_d0	i2s2_sdim0	gmac_rxerm1	pdm_sdi1m1			I/O	I	down	4mA	√
GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDI2_M1	gpio1_d1	i2s2_sdom0	gmac_txenm1	pdm_sdi2m1			I/O	I	down	4mA	√
GPIO1_D2/I2S2_LRCKRX_M0/CLKOUT_GMAC_M2/PDM_SDI3_M1	gpio1_d2	i2s2_lrckrxm0	clkout_gmacm2	pdm_sdi3m1			I/O	I	down	4mA	√
GPIO1_D4/CLK32KOUT_M1	gpio1_d4	clk32k_outm1					I/O	I	down	4mA	√
GPIO2_A0/UART2_TX_M1	gpio2_a0	uart2dbg_txm1					I/O	I	down	4mA	√
GPIO2_A1/UART2_RX_M1	gpio2_a1	uart2dbg_rxm1					I/O	I	up	4mA	√
GPIO2_A2/PWM_IR	gpio2_a2	pwm_ir					I/O	I	up	4mA	√
GPIO2_A3/EFUSE_PWREN	gpio2_a3	efuse_pwren					I/O	I	up	4mA	√
GPIO2_A4/PWM0/I2C1_SDA	gpio2_a4	pwm0	i2c1_sda				I/O	I	up	4mA	√
GPIO2_A5/PWM1/I2C1_SCL	gpio2_a5	pwm1	i2c1_scl				I/O	I	up	4mA	√
GPIO2_A6/PWM2	gpio2_a6	pwm2					I/O	I	up	4mA	√
GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL	gpio2_b4	spi_csn1m0	flash_vol_sel				I/O	I	up	4mA	√
GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1	gpio2_b7	i2s1_mclk		tsp_syncm1	cif_clkoutm1		I/O	I	down	4mA	√
GPIO2_C0/I2S1_LRCKRX/TSP_D5_M1/CIF_D5_M1	gpio2_c0	i2s1_lrckrx		tsp_d5m1	cif_d5m1		I/O	I	up	4mA	√
GPIO2_C1/I2S1_LRCKTX/SPDIF_TX_M1/TSP_D6_M1/CIF_D6_M1	gpio2_c1	i2s1_lrcktx	spdif_txm1	tsp_d6m1	cif_d6m1		I/O	I	up	4mA	√
GPIO2_C2/I2S1_SCLK/PDM_CLK_M0/TSP_D7_M1/CIF_D7_M1	gpio2_c2	i2s1_sclk	pdm_clkm0	tsp_d7m1	cif_d7m1		I/O	I	down	4mA	√
GPIO2_C3/I2S1_SDI/PDM_SDI0_M0/CARD_CLK_M1	gpio2_c3	i2s1_sdi	pdm_sdi0m0	card_clkm1			I/O	I	up	4mA	√
GPIO2_C4/I2S1_SDIO1/PDM_SDI1_M0/CARD_RST_M1	gpio2_c4	i2s1_sdio1	pdm_sdi1m0	card_rstm1			I/O	I	up	4mA	√
GPIO2_C5/I2S1_SDIO2/PDM_SDI2_M0/CARD_DET_M1	gpio2_c5	i2s1_sdio2	pdm_sdi2m0	card_detm1			I/O	I	up	4mA	√
GPIO2_C6/I2S1_SDIO3/PDM_SDI3_M0/CARD_IO_M1	gpio2_c6	i2s1_sdio3	pdm_sdi3m0	card_iom1			I/O	I	up	4mA	√
GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0	gpio2_c7	i2s1_sdo	pdm_fsyncm0				I/O	I	up	4mA	√
GPIO2_D0/I2C0_SCL/FEPHYLED_LINK_M1	gpio2_d0	i2c0_scl	fephyled_linkm1				I/O	I	up	4mA	√
GPIO2_D1/I2C0_SDA/FEPHYLED_RX_M1/FEPHYLED_TX_M1	gpio2_d1	i2c0_sda	fephyled_rxm1	fephyled_txm1			I/O	I	up	4mA	√
GPIO2_D2/USB2OTG_DRVBUS	gpio2_d2	usb2otg_drvbus					I/O	I	down	4mA	√

Pin Name	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	IO Type	IO Def	Pull	Default Current	INT
GPIO3_A0/TSP_VALID/CIF_VSYNC/SDMMC0EXT_CMD/SPI_CLK_M2/ I2S2_SCLK_M1	gpio3_a0	tsp_valid	cif_vsync	sdmmc0ext_cmd	spi_clkm2	i2s2_sclkm1	I/O	I	up	4mA	√
GPIO3_A1/TSP_FAIL/CIF_HREF/SDMMC0EXT_DET/SPI_TXD_M2/I2 S2_SDO_M1	gpio3_a1	tsp_fail	cif_href	sdmmc0ext_det	spi_txdm2	i2s2_sdom1	I/O	I	up	4mA	√
GPIO3_A2/TSP_CLK/CIF_CLKIN/SDMMC0EXT_CLK/SPI_RXD_M2/I2 S2_SDI_M1	gpio3_a2	tsp_clk	cif_clkin	sdmmc0ext_clkout	spi_rxdm2	i2s2_sdim1	I/O	I	down	4mA	√
GPIO3_A4/TSP_D0/CIF_D0/SDMMC0EXT_D0/UART1_TX	gpio3_a4	tsp_d0	cif_d0	sdmmc0ext_d0	uart1_tx		I/O	I	up	4mA	√
GPIO3_A5/TSP_D1/CIF_D1/SDMMC0EXT_D1/UART1_RTSN	gpio3_a5	tsp_d1	cif_d1	sdmmc0ext_d1	uart1_rtsn		I/O	I	up	4mA	√
GPIO3_A6/TSP_D2/CIF_D2/SDMMC0EXT_D2/UART1_RX	gpio3_a6	tsp_d2	cif_d2	sdmmc0ext_d2	uart1_rx		I/O	I	up	4mA	√
GPIO3_A7/TSP_D3/CIF_D3/SDMMC0EXT_D3/UART1_CTSN	gpio3_a7	tsp_d3	cif_d3	sdmmc0ext_d3	uart1_ctsn		I/O	I	up	4mA	√
GPIO3_B0/TSP_D4/CIF_D4/SPI_CSN0_M2/I2S2_LRCK_TX_M1/I2S 2_LRCK_RX_M1	gpio3_b0	tsp_d4	cif_d4	spi_csn0m2	i2s2_lrcktxm1	i2s2_lrckrxm1	I/O	I	down	4mA	√
GPIO0_A7/EMMC_D0	gpio0_a7	emmc_d0					I/O	I	up	8mA	√
GPIO2_D4/EMMC_D1	gpio2_d4	emmc_d1					I/O	I	up	8mA	√
GPIO2_D5/EMMC_D2	gpio2_d5	emmc_d2					I/O	I	up	8mA	√
GPIO2_D6/EMMC_D3	gpio2_d6	emmc_d3					I/O	I	up	8mA	√
GPIO2_D7/EMMC_D4	gpio2_d7	emmc_d4					I/O	I	up	8mA	√
GPIO3_C0/EMMC_D5	gpio3_c0	emmc_d5					I/O	I	up	8mA	√
GPIO3_C1/EMMC_D6	gpio3_c1	emmc_d6					I/O	I	up	8mA	√
GPIO3_C2/EMMC_D7	gpio3_c2	emmc_d7					I/O	I	up	8mA	√
GPIO3_C3/EMMC_CMD	gpio3_c3	emmc_cmd					I/O	I	up	8mA	√
GPIO3_C5/EMMC_CLKOUT	gpio3_c5	emmc_clkout					I/O	I	up	8mA	√
GPIO3_C6/EMMC_PWREN	gpio3_c6	emmc_pwren					I/O	I	down	8mA	√

Notes:

① Pad types: I = input, O = output, I/O = input/output (bidirectional)

② AP = Analog Power, AG = Analog Ground; DP = Digital Power, DG = Digital Ground;   A = Analog

③ Output Drive Unit is mA, only Digital IO has drive value;

④ Reset state: I = input without any pull resistor,O = output without any pull resistor;

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TCK	I	JTAG interface clock input/SWD interface clock input
	JTAG_TMS	I/O	JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	SDMMC0_CLK	O	sdmmc card clock
	SDMMC0_CMD	I/O	sdmmc card command output and reponse input
	SDMMC0_D[i] (i=0~3)	I/O	sdmmc card data input and output
	SDMMC0_DETN	I	sdmmc card detect signal, 0 represents presence of card

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDMMC1_CLK	O	sdio card clock
	SDMMC1_CMD	I/O	sdio card command output and reponse input
	SDMMC1_D[i] (i=0~3)	I/O	sdio card data input and output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLKOUT	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and reponse input
	EMMC_D[i] (i=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
DDR Interface	CLKP	O	Active-high clock signal to the memory device.
	CLKN	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSNi (i=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASN	O	Active-low row address strobe to the memory device.

Interface	Pin Name	Direction	Description
	CASN	O	Active-low column address strobe to the memory device.
	WEN	O	Active-low write enable strobe to the memory device.
	BAi(i=0,1,2)	O	Bank address signal to the memory device.
	Ai(i=0~15)	O	Address signal to the memory device.
	DQi(i=0~31)	I/O	Bidirectional data line to the memory device.
	DQS[i]_P (i=0~3)	I/O	Active-high bidirectional data strobes to the memory device.
	DQS[i]_N (i=0~3)	I/O	Active-low bidirectional data strobes to the memory device.
	DMi(i=0~3)	O	Active-low data mask signal to the memory device.
	ODTi(i=0,1)	O	On-Die Termination output signal for two chip select.
	RESETN	O	DDR3 reset signal to the memory device

Interface	Pin Name	Direction	Description
SIM Card	CARD_CLK	O	Smart card clock output
	CARD_RST	O	Smart card reset output
	CARD_IO	I/O	Smart card data
	CARD_DET	O	Smart card detect input

Interface	Pin Name	Direction	Description
TSP Interface	TSP_CLK	I/O	TSI reference clock
	TSP_D[i] (i=0~7)	I	TSI data(i=0~7)
	TSP_SYNC	I	TSI synchronizer signal
	TSP_VALID	I	TSI valid signal
	TSP_FAIL	I	TSI fail signal

Interface	Pin Name	Direction	Description
I2S1/PCM Controller	I2S1_MCLK	O	I2S/PCM clock source
	I2S1_SCLK	I/O	I2S/PCM serial clock
	I2S1_LRCKRX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_LRCKTX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_SDI	I	I2S/PCM serial data input
	I2S1_SDO	O	I2S/PCM serial data output
	I2S1_SDIOi (i=1~3)	I/O	Configurable I2S/PCM serial data input / output

Interface	Pin Name	Direction	Description
	I2S2_MCLK	O	I2S/PCM clock source
	I2S2_SCLK	I/O	I2S/PCM serial clock

Interface	Pin Name	Direction	Description
I2S2/PCM Controller	I2S2_LRCKRX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S2_LRCKTX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S2_SDI	I	I2S/PCM serial data input
	I2S2_SDO	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
SPDIF transmitter	SPDIF_TX	O	SPDIF biphase data ouput

Interface	Pin Name	Direction	Description
PDM interface	PDM_CLK	O	PDM sampling clock
	PDM_SDI[i] (i=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
SPI Controller	SPI_CLK	I/O	SPI serial clock
	SPI_CSN[i](i=0,1)	I/O	SPI chip select signal,low active
	SPI_TXD	O	SPI serial data output
	SPI_RXD	I	SPI serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0	O	Pulse Width Modulation output
	PWM1	O	Pulse Width Modulation output
	PWM2	O	Pulse Width Modulation output
	pWM3	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	I2C[i]_SDA (i=0,1,3)	I/O	I2C0 data
	I2C[i]_SCL (i=0,1,3)	I/O	I2C0 clock

Interface	Pin Name	Direction	Description
UART	UART[i]_RX (i=0,1,2)	I	UART0 serial data input
	UART[i]_TX (i=0,1,2)	O	UART0 serial data output

Interface	Pin Name	Direction	Description
GMAC	GMAC_CLK	I/O	RGMII/RMII REC_CLK output or GMAC external clock input
	GMAC_TXCLK	O	Clock for transmission
	GMAC_RXCLK	I	Clock for receive
	GMAC_MDC	O	GMAC management interface clock
	GMAC_MDIO	I/O	GMAC management interface data
	GMAC_TXD[*i*](*i*=0~3)	O	GMAC TX data
	GMAC_RXD[*i*](*i*=0~3)	I	GMAC RX data
	GMAC_TXEN	O	GMAC TX data enable
	GMAC_RXER	I	GMAC RX error signal
	GMAC_RXDV	O	GMAC RX enable
	GMAC_CRS	I	PHY CRS signal
	GMAC_MDIO	I/O	PHY MDC data line
	GMAC_MDC	O	PHY MDC control

Interface	Pin Name	Direction	Description
FE PHY	FEPHY_TXN	I/O	Transmit data - Negative
	FEPHY_TXP	I/O	Transmit data - Positive
	FEPHY_RXP	I/O	Receive data - Positive
	FEPHY_RXN	I/O	Receive data - Negative
	FEPHY_EXTRES	I/O	Connection to reference resistor
	FEPHY_LED_LINK	O	PHY link status
	FEPHY_LED_DATA	O	PHY data transceiver status
	FEPHY_LED_SPEED10	O	PHY speed status

Interface	Pin Name	Direction	Description
USB 2.0	OTG and HOST		Port 0 supports OTG Port 1 supports HOST only
	USB[*i*]_DP (*i*=0~1)	I/O	USB 2.0 Data signal DP
	USB[*i*]_DM (*i*=0~1)	I/O	USB 2.0 Data signal DM
	USB20_EXTR	O	Connect 133 ohm resistor to ground to generate reference current
	USB20_VBUS	I	OTG detect

Interface	Pin Name	Direction	Description
USB 3.0	USB30_TXP USB30_TXN	I/O	USB 3.0 transmission signal DP/DM
	USB30_RXP USB30_RXN	I/O	USB 3.0 receive signal DP/DM
	USB30_DP	I/O	USB 2.0 Data signal DP in USB 3.0 port
	USB30_DM	I/O	USB 2.0 Data signal DM in USB 3.0 port
	USB30_VBUS	I	OTG detect

Interface	Pin Name	Direction	Description
	USB30_EXTR	O	Connect 2.0k ohm resistor to ground to generate reference current

Interface	Pin Name	Direction	Description
HDMI	HDMI_EXTR	O	Connect 2.0k ohm resistor to ground to generate reference current
	HDMI_CEC	I/O	HDMI CEC
	HDMI_SCL	O	HDMI I2C clock
	HDMI_SDA	I/O	HDMI I2C data line
	HDMI_HPD	I/O	HDMI hot plug detect signal
	HDMI_TX0N	O	TMDS channel 0 negative data line
	HDMI_TX0P	O	TMDS channel 0 positive data line
	HDMI_TX1N	O	TMDS channel 1 negative data line
	HDMI_TX1P	O	TMDS channel 1 positive data line
	HDMI_TX2N	O	TMDS channel 2 negative data line
	HDMI_TX2P	O	TMDS channel 2 positive data line
	HDMI_TX3N	O	TMDS negative clock line
	HDMI_TX3P	O	TMDS positive clock line
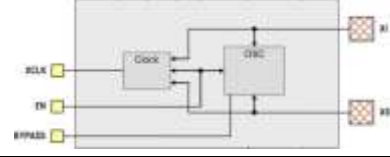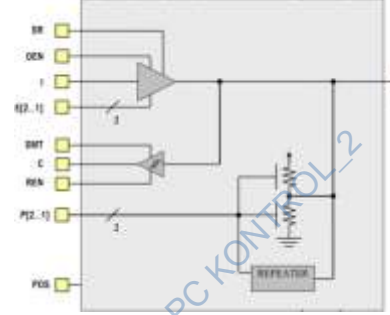
Interface	Pin Name	Direction	Description
Audio CODEC	CODEC_VCM	I	Reference voltage input
	CODEC_AOL	O	Left channel output
	CODEC_AOR	O	Right channel output

Interface	Pin Name	Direction	Description
Video DAC	VDAC_IREF	I/O	Reference current. Output current when using External Reference Resistor or Input Reference Current when using external current source
	VDAC_IOUT	O	Positive output

2.9 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 IO Type List

Type	Diagram	Description	Pin Name
A		Crystal Oscillator with high enable	XIN24M/XOUT24M
B		Tri-state output pad with input, which pull-up/pull-down, slew rate and drive strength is configurable	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Absolute minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute minimum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	VDD_CORE	-0.4	1.48	V
Supply voltage for GPU and core logic	VDD_LOGIC	-0.4	1.26	V
1.0V supply voltage		-0.4	1.19	V
1.8V supply voltage		-0.4	2.18	V
3.3V supply voltage		-0.4	3.99	V
Supply voltage for DDR IO		-0.4	1.79	V
Storage Temperature	Tstg		125	℃
Max Conjunction Temperature	Tj		125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	VDD_CORE	0.95	1.00	1.35	V
Voltage for GPU and core logic	VDD_LOGIC	0.90	1.00	1.15	V
Digital GPIO Power (1.8V only)	VCCIO_PMU, VCCIO1	3.00	3.30	3.63	V
Digital GPIO Power (3.3V/1.8V)	VCCIO2, VCCIO3, VCCIO4	3.00	3.30	3.63	V
	VCCIO5, VCCIO6	1.62	1.8	1.98	
DDR3 IO power	DDR_VDD	1.425	1.5	1.575	V
DDR3L IO Power	DDR_VDD	1.283	1.35	1.417	V
LPDDR3 IO Power	DDR_VDD	1.14	1.2	1.3	V
DDR4 IO Power	DDR_VDD	1.14	1.2	1.3	V
ACODEC Analog Power	CODEC_AVDD_1V8	1.62	1.8	1.98	V
VDAC Analog Power	VDAC_AVDD_1V8	1.62	1.8	1.98	V
HDMI Analog Power (1.0V)	HDMI_AVDD_1V0	0.9	1.0	1.1	V
HDMI Analog Power (1.8V)	HDMI_AVDD_1V8	1.62	1.8	1.98	V
PLL Digital Power	PLL_DVDD_1V0	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD_1V8	1.62	1.8	1.98	V
FEPHY Analog Power (1.0V)	FEPHY_AVDD_1V0	0.9	1.0	1.1	V
FEPHY Analog Power (1.8V)	FEPHY_AVDD_1V8	1.62	1.8	1.98	V

Parameters	Symbol	Min	Typ	Max	Unit
USB 2.0 digital logic Power	USB20_DVDD_1V0	0.90	1.00	1.10	V
USB 2.0 OTG/Host Analog Power (1.8V)	USB20_AVDD_1V8	1.62	1.8	1.98	V
USB 2.0 OTG/Host Analog Power (3.3V)	USB20_AVDD_3V3	3.069	3.3	3.63	V
USB 3.0 digital logic Power	USB30_DVDD_1V0	0.90	1.00	1.10	V
USB 3.0 OTG/Host Analog Power (1.8V)	USB30_AVDD_1V8	1.62	1.8	1.98	V
USB 3.0 OTG/Host Analog Power (3.3V)	USB30_AVDD_3V3	3.069	3.3	3.63	V
OSC input clock frequency		N/A	24	N/A	MHz
Max CPU frequency of A53				1.4	GHz
Max GPU frequency				500	MHz
Ambient Operating Temperature	T_A	0	25	80	℃

Notes:
① *Symbol name is same as the pin name in the io descriptions*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
	Input Low Voltage	Vildq(DC)	TBD		Vref-0.10	V
	Output High Voltage	Voh(DC)	-	-	0.9VDDQ	V
	Output Low Voltage	Vol(DC)	(0.1+0.9Ron/(Rtt+Ron))*VDDQ	-	-	V

	Parameters	Symbol	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD+0.4	V
	Input Low Voltage	Vil_ddr	-0.4	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	0.9xDDR_VDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.1*DDR_VDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 / 54 / 36	120 / 60 / 40	140 / 66 / 44	Ohm
DDR IO @ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	0	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	NA	NA	0.9*DDR_VDD	V
	Output Low Voltage	Vol_ddr	0.1*DDR_VDD	NA	NA	V
DDR IO @DDR4 mode	Input High Voltage	Vihdq(DC)	Vref+0.10		TBD	V
	Input Low Voltage	Vildq(DC)	TBD		Vref-0.10	V
	Output High Voltage	Voh(DC)	-	-	0.9VDDQ	V
	Output Low Voltage	Vol(DC)	(0.1+0.9Ron/(Rtt+Ron))*VDDQ	-	-	V

	Parameters	Symbol	Min	Typ	Max	Unit
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing voltage RT=50Ω	Vswing	400		600	mV
		Vswing_data	400		600	mV
		Vswing_clock	400		600	mV
	Single-ended output high voltage	Vh				mV
			avddtmds-400		avddtmds+10	mV
		Vh_data	avddtmds-400		avddtmds+10	mV
		Vh_clock	avddtmds-400		avddtmds+10	mV
	Single-ended output low voltage	Vl				mV
			avddtmds-1000		avddtmds-400	mV
		Vl_data	avddtmds-1000		avddtmds-400	mV
		Vl_clock	avddtmds-1000		avddtmds-400	mV

Parameters		Symbol	Min	Typ	Max	Unit
	Differential source termination load	Rterm	75		150	Ω

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	800		3200	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	16		3200	MHz
	Lock time	T_{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		250	500	Input clock cycles

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
VDDHV current consumption		Fvco = 1000MHz, @3.3V Current scale as $(Fvco/1GHz)^{1.5}$		1.0	1.2	mA
VDD Current consumption		VDD =1.1V		1.3	1.56	uA/MHz
Power consumption (power-down mode)		PD=HIGH, @27 ℃		13		uA

Notes:

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.7 Electrical Characteristics for USB 3.0 Interface

Table 3-7 Electrical Characteristics for USB 3.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Differential input high voltage	VIH		+150			mV
Differential input low voltage	VIL				-150	mV
Absolute maximum input voltage	VMAX				+1.15	V
Absolute minimum input voltage	VMIN		-0.3			V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
DC input differential termination			80		110	ohms
Duty Cycle	Duty Cycle		45		55	%
Clock source output DC impedance	ZC-DC		40		60	ohms
Absolute single ended crossing point voltage	VCROSS		+250		+550	mV

3.8 Electrical Characteristics for DDR IO

Table 3-8 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0		uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA
DDR IO @LPDDR2/LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-5	0	+5	uA

3.9 Electrical Characteristics for HDMI

Table 3-9 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Trise and Tfall				<200		ps
Frequency Tolerance, max				-300 ~300		ppm
Clock duty cycle			40%		60%	
Power consumption		1080p		60		mA
Power consumption		2160p		100		mA

3.10 Electrical Characteristics for VDAC

Table 3-10 Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
High voltage analog current consumption	IAVDD	Ifs=34mA		39		mA

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Digital current consumption	I$_{VDD}$	Fs=100MHz		0.1		mA
Current consumption in power down, analog	I$_{AVDD}$			10		uA
Current consumption in power down, digital	I$_{VDD}$			1		uA

3.11 Electrical Characteristics for TSADC

Table 3-11 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution				5		℃
Temperature Range			-10		120	℃
Analog power	I$_{AVDD}$	Fs= 50KS/s		190		uA
Digital power	I$_{VDD}$	Fs= 50KS/s		10		uA
Clock Frequency	Fclk	Fclk			50	KHz
Power Down Current from Analog	I$_{AVDD}$	Power down		1		uA
Power Down Current from Digital	I$_{VDD}$	Power down		1		uA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	19.0	(℃/W)
Junction-to-board thermal resistance	θ_{JB}	11.6	(℃/W)
Junction-to-case thermal resistance	θ_{JC}	5.3	(℃/W)

Note: The testing PCB is 4 layers, 95mmx95mm, 1.6mm thickness, Ambient temperature is 25℃.