

GA102 GF SKU P-BOARD

370W, 7.4inch STD PCB, 320b, GDDR6x x16 10GB

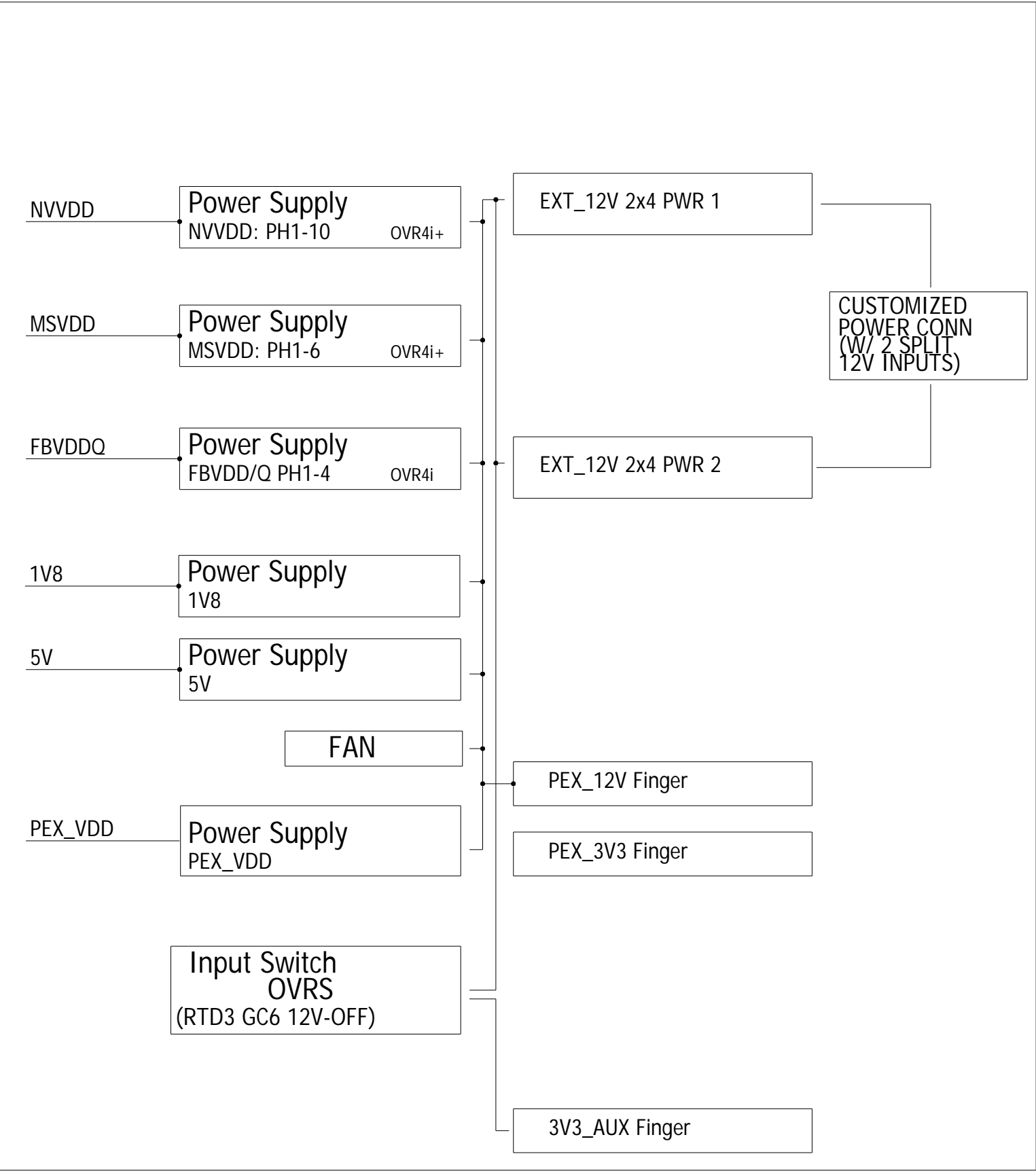
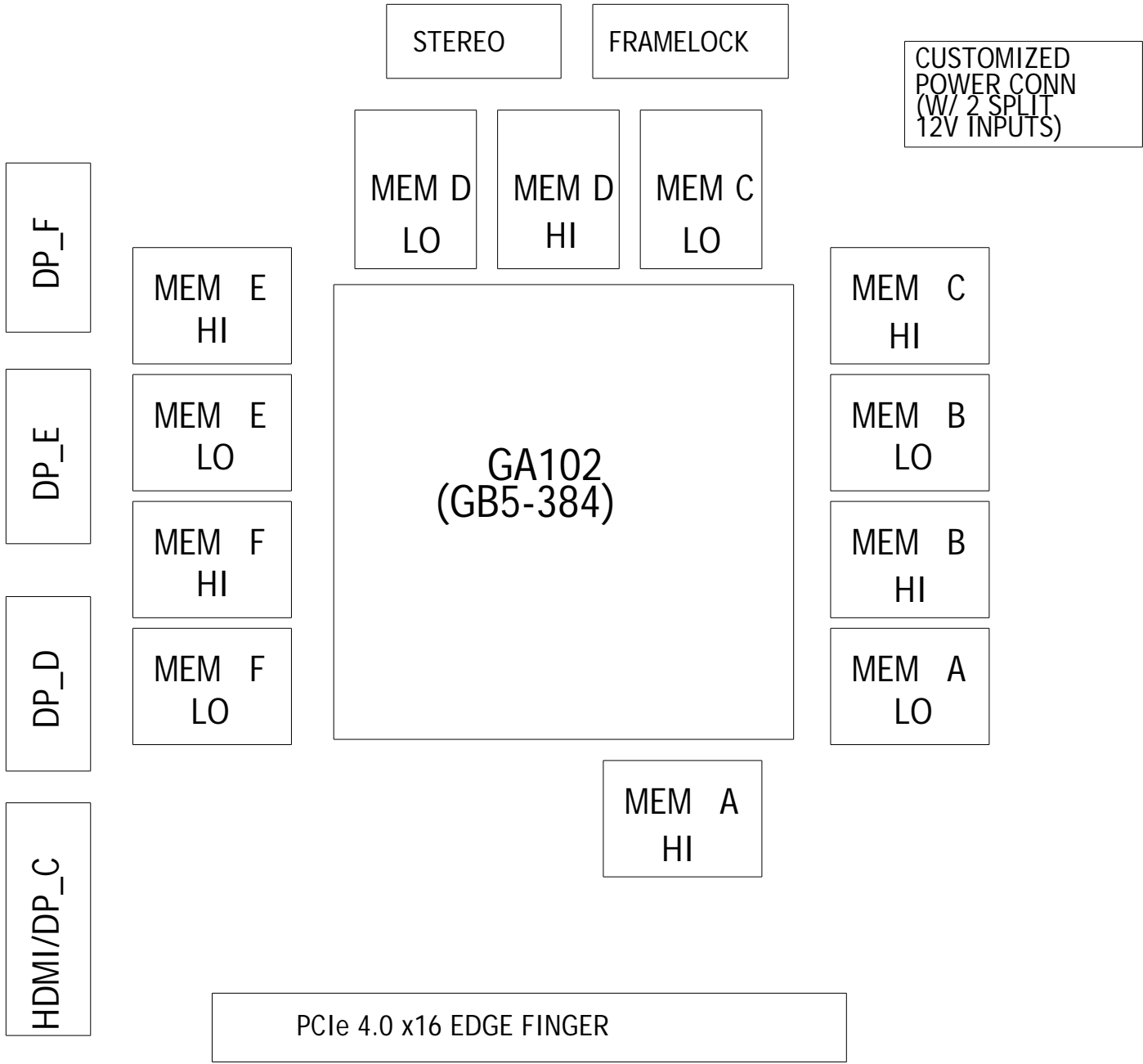
DP + DP + DP + HDMI

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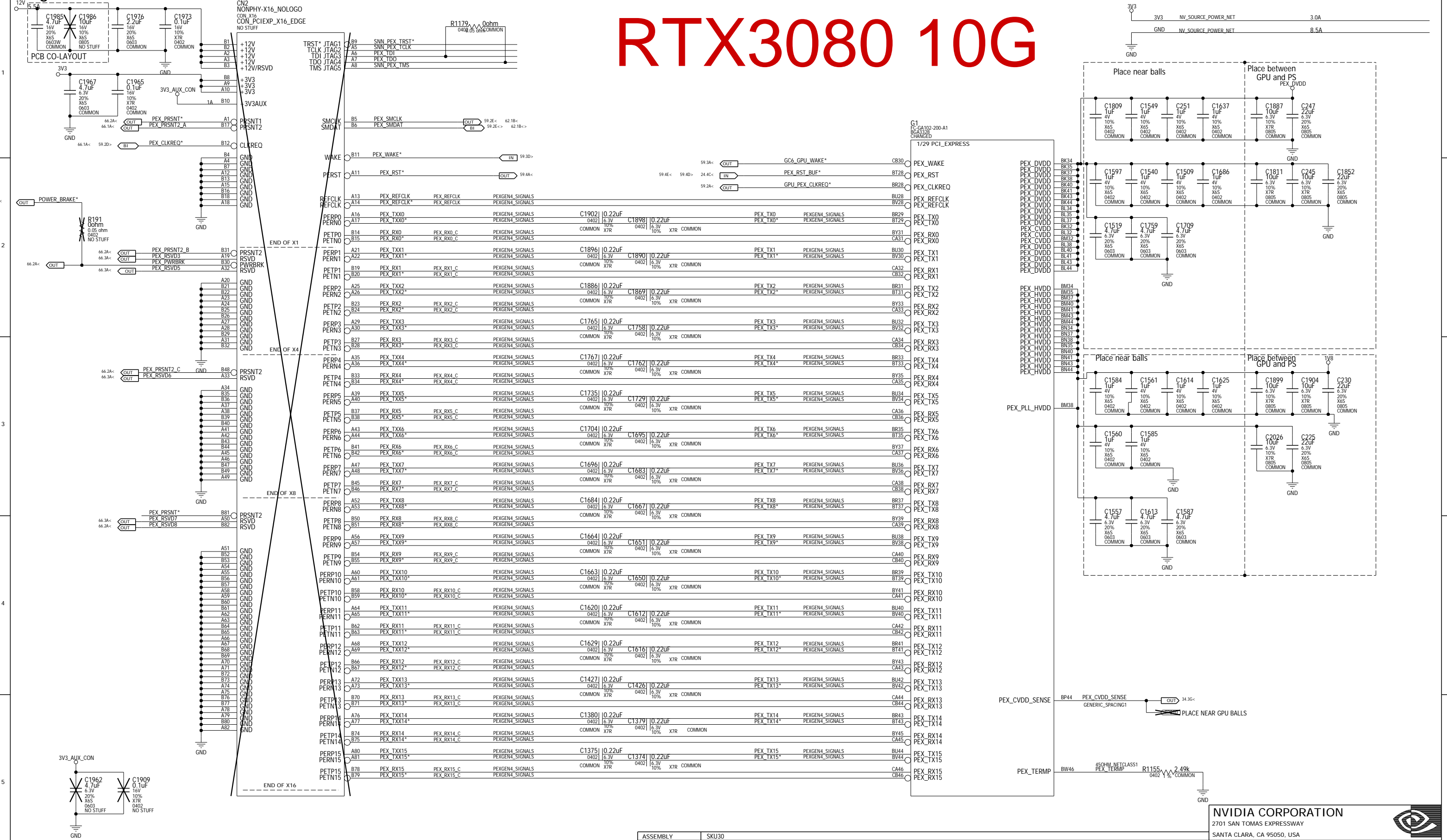
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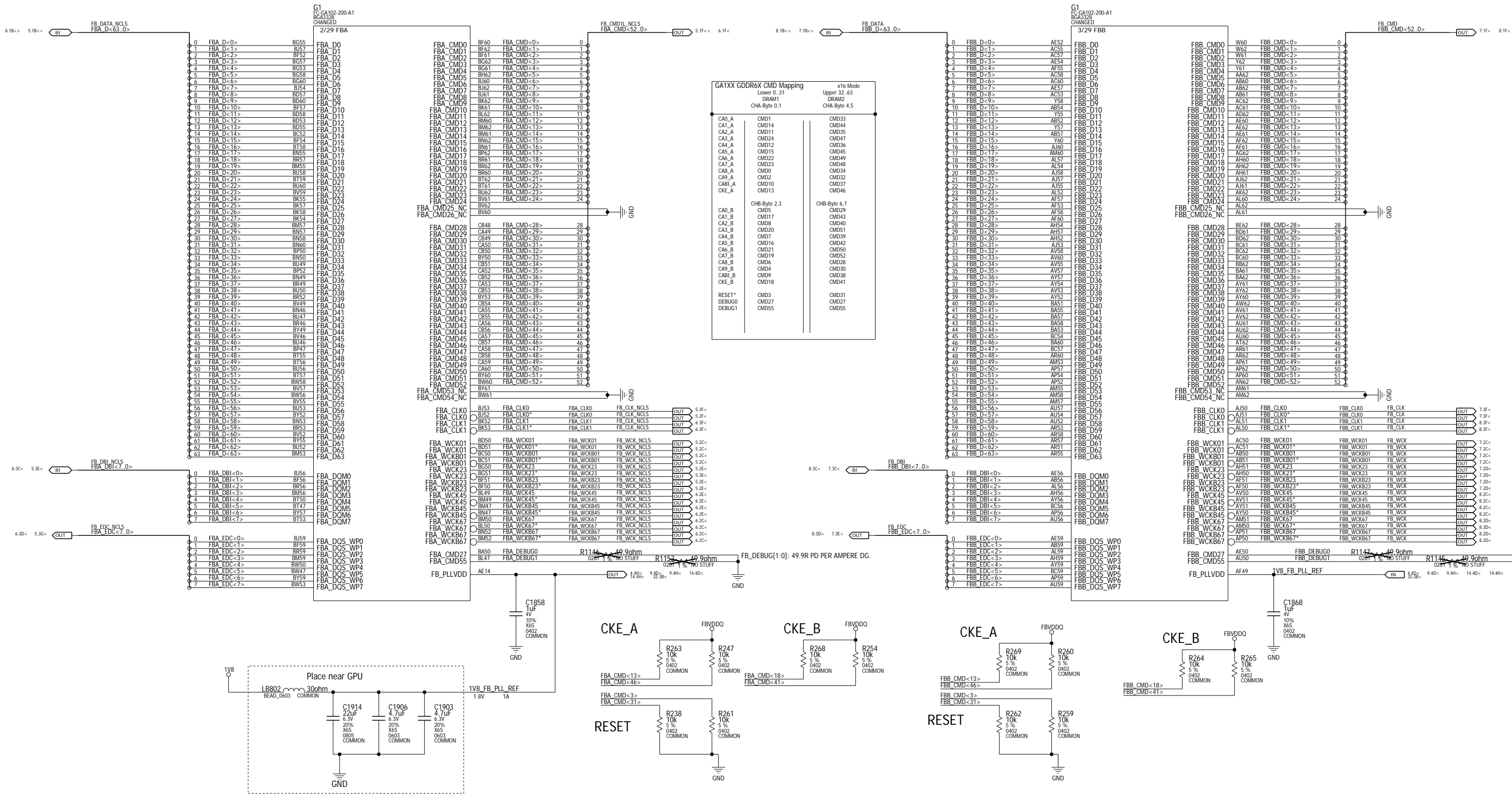
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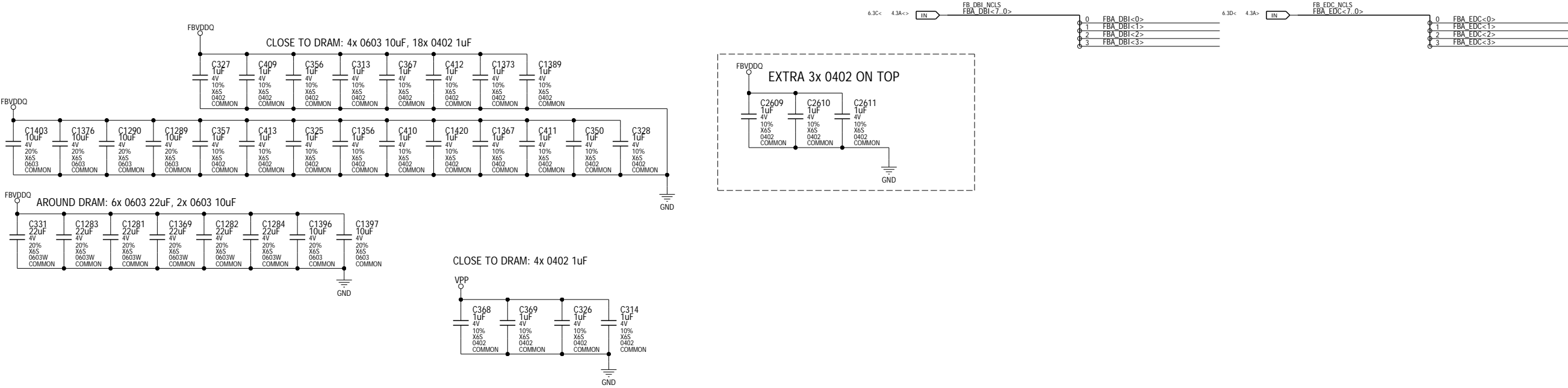
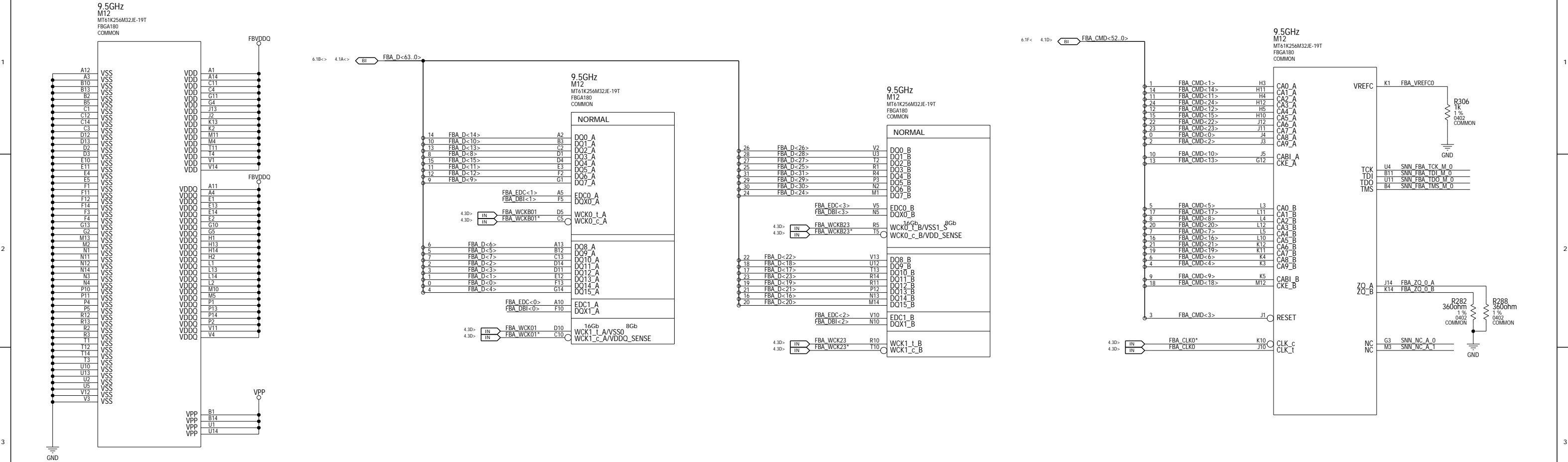
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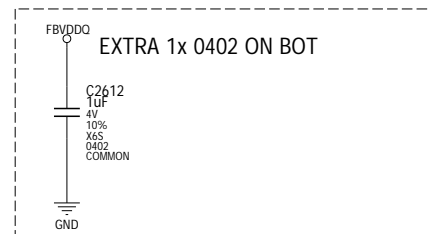
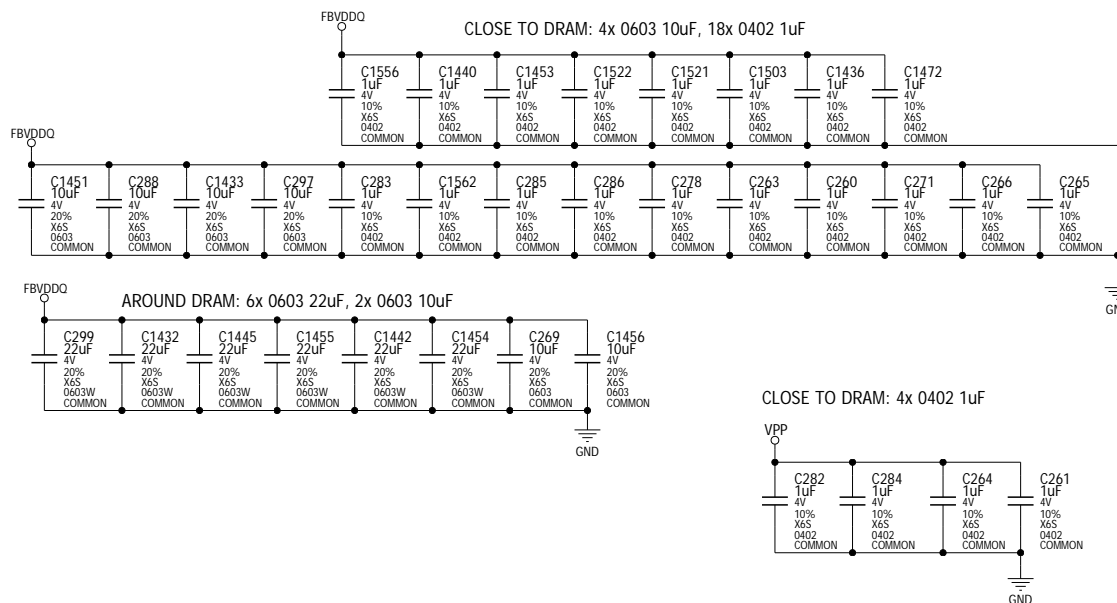
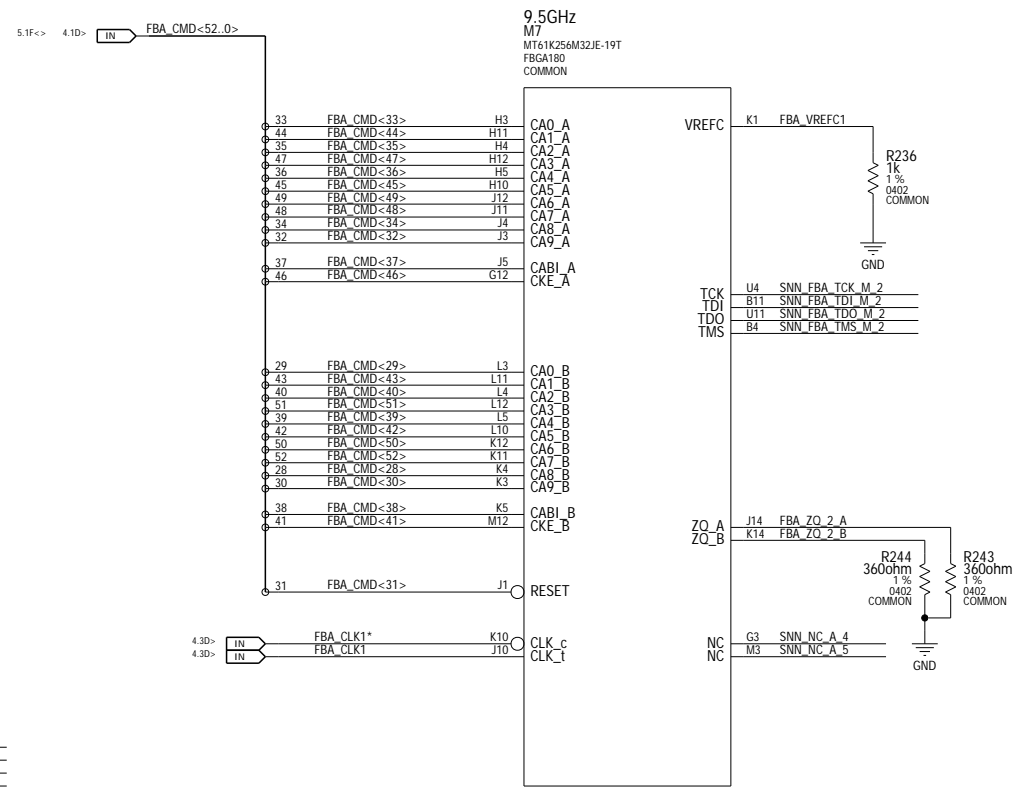
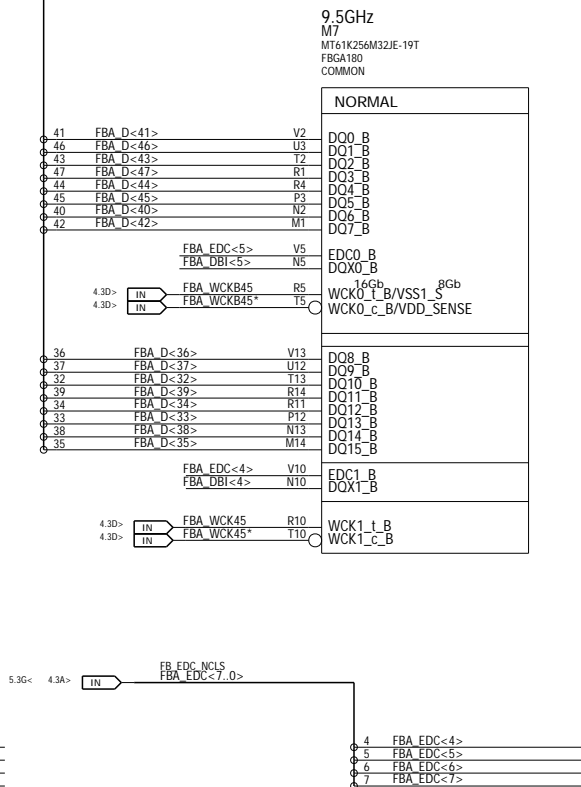
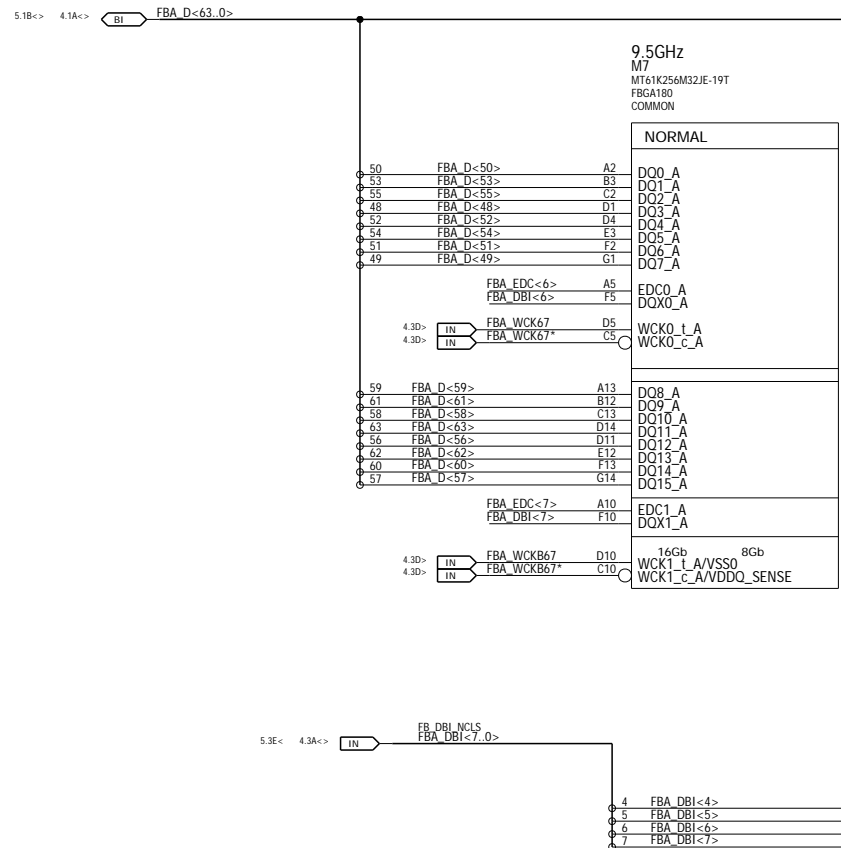
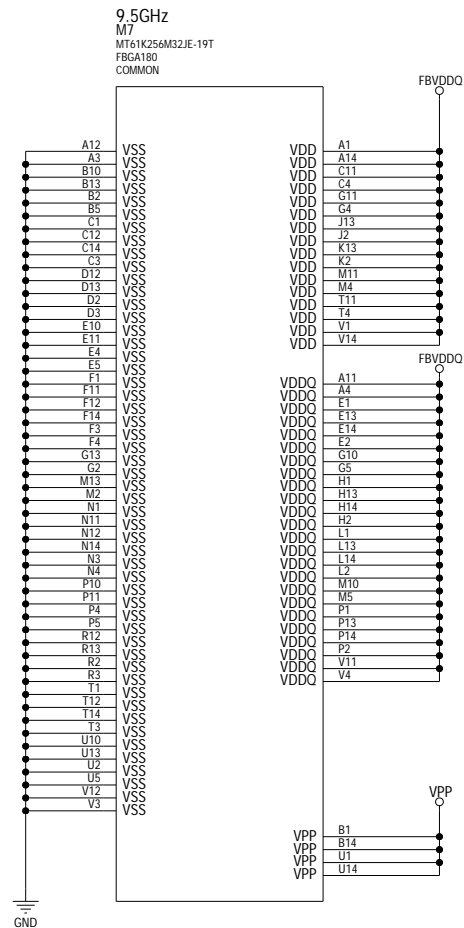


RTX3080 10G

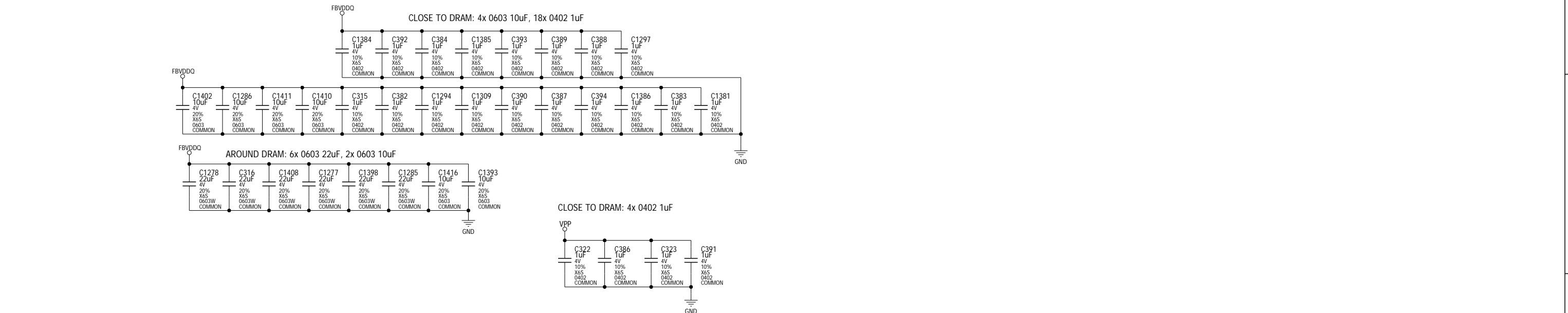
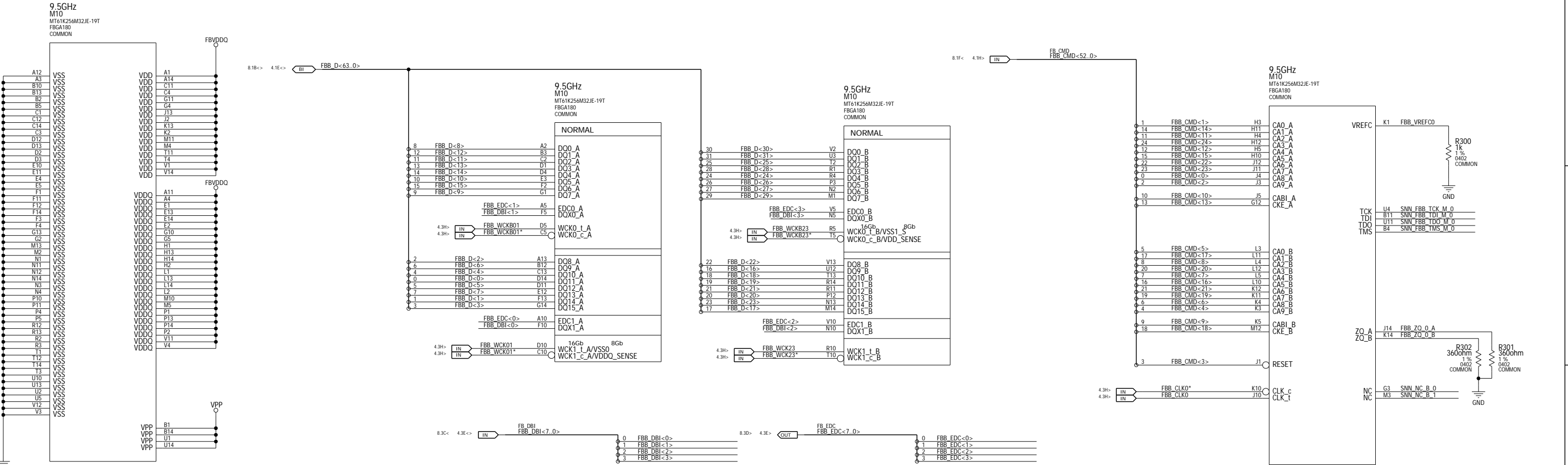




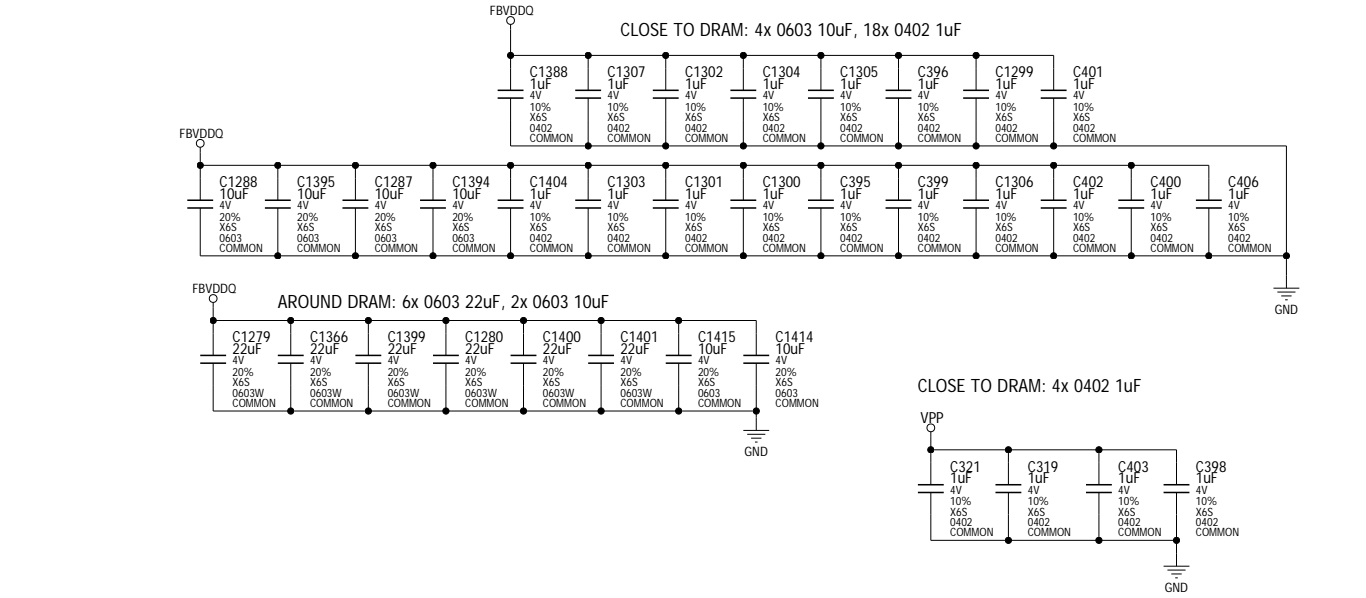
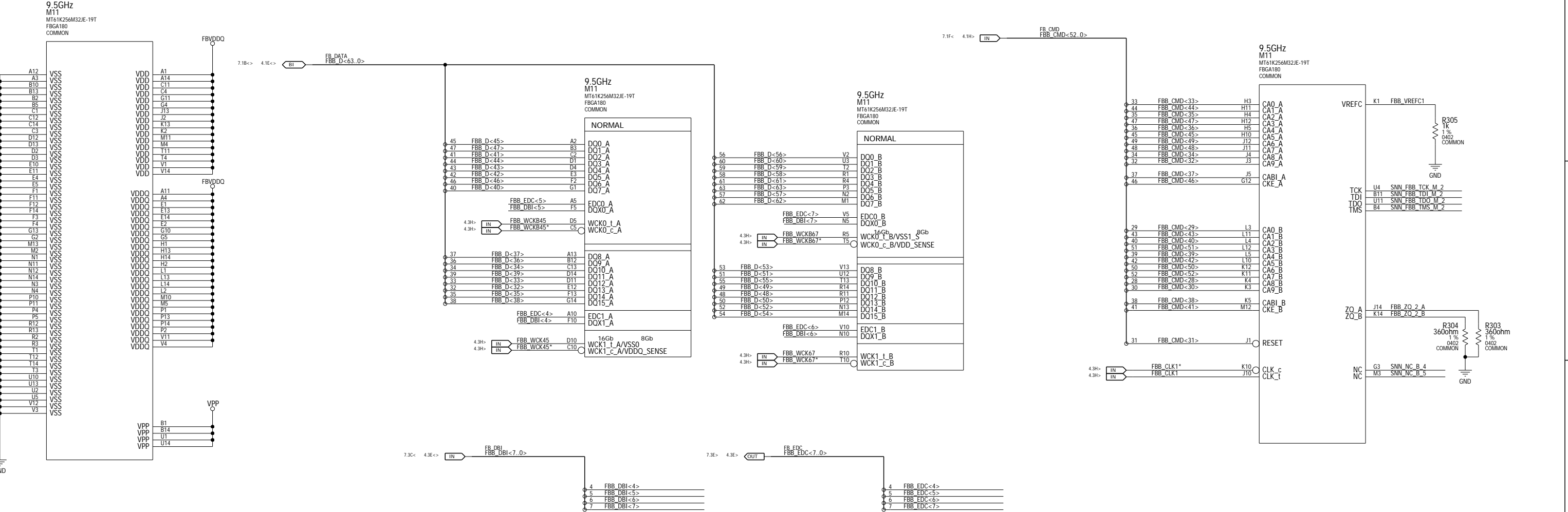


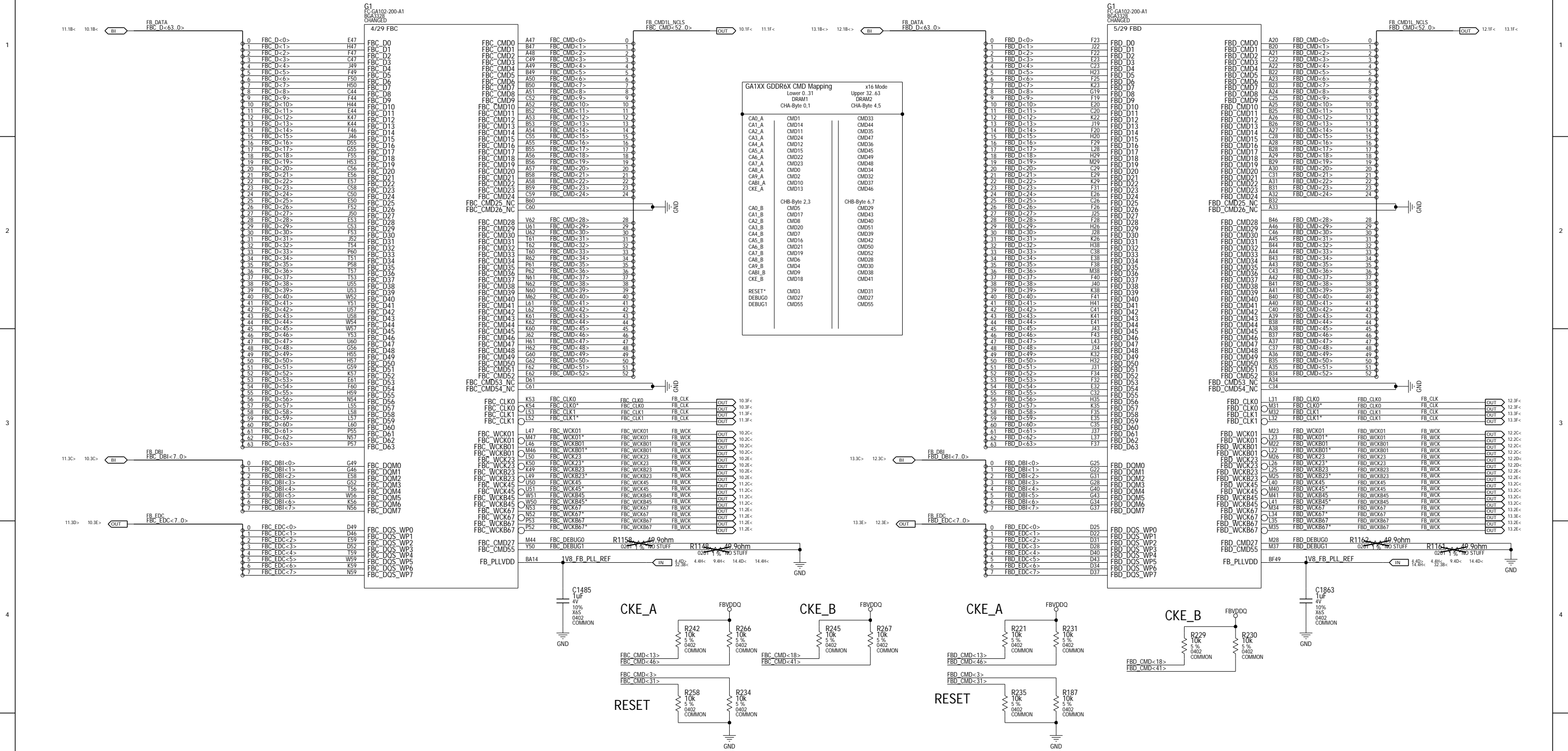


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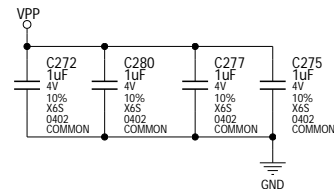
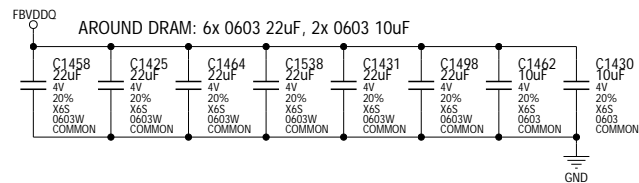
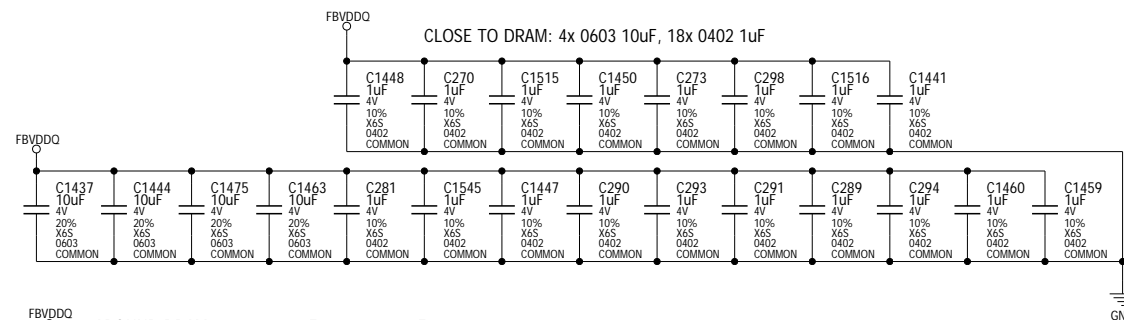
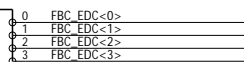
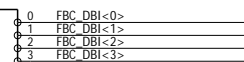
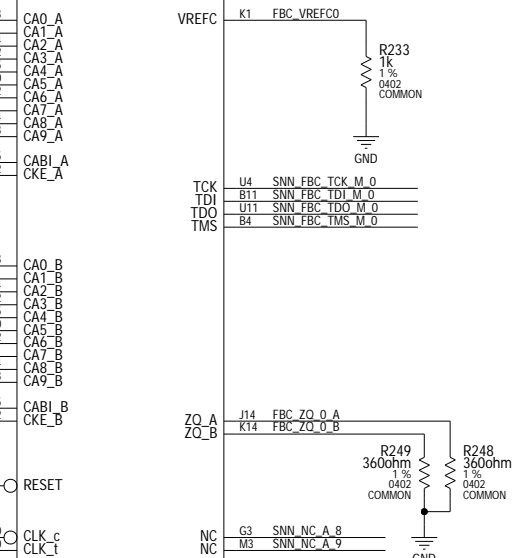
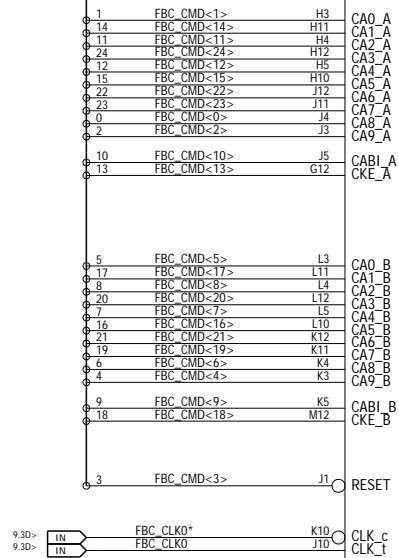
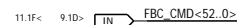
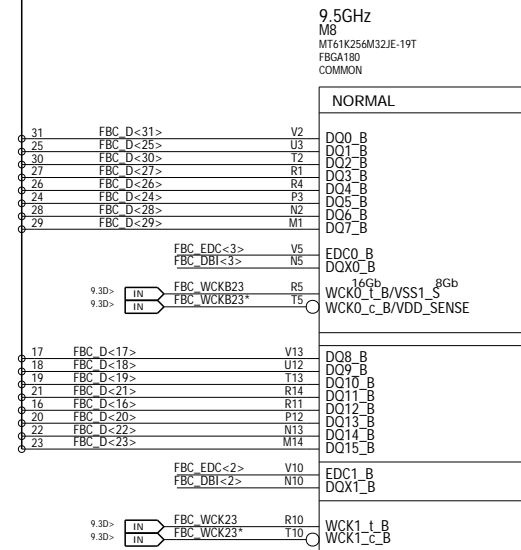
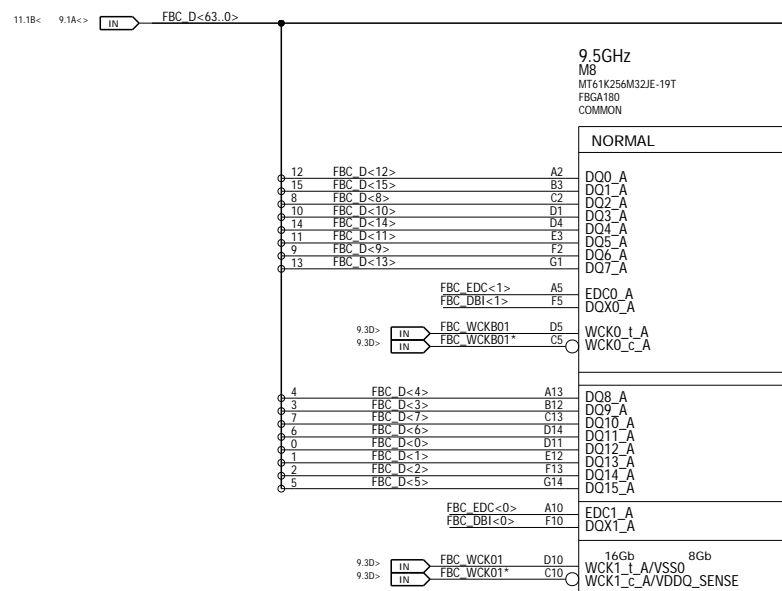
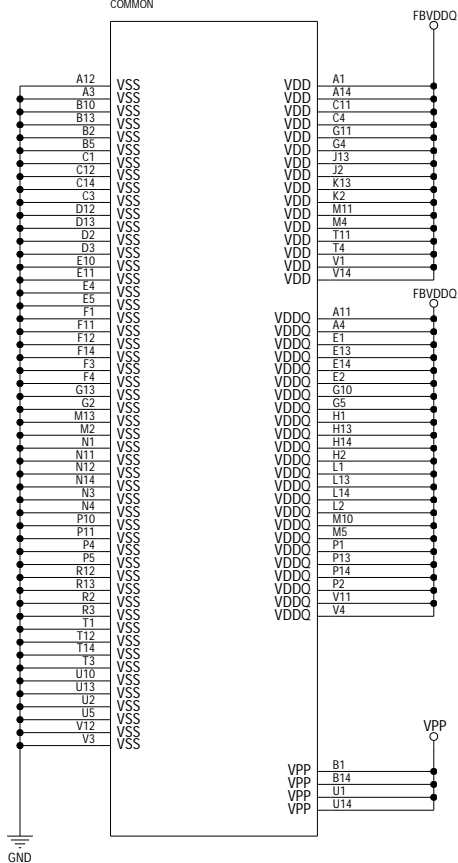
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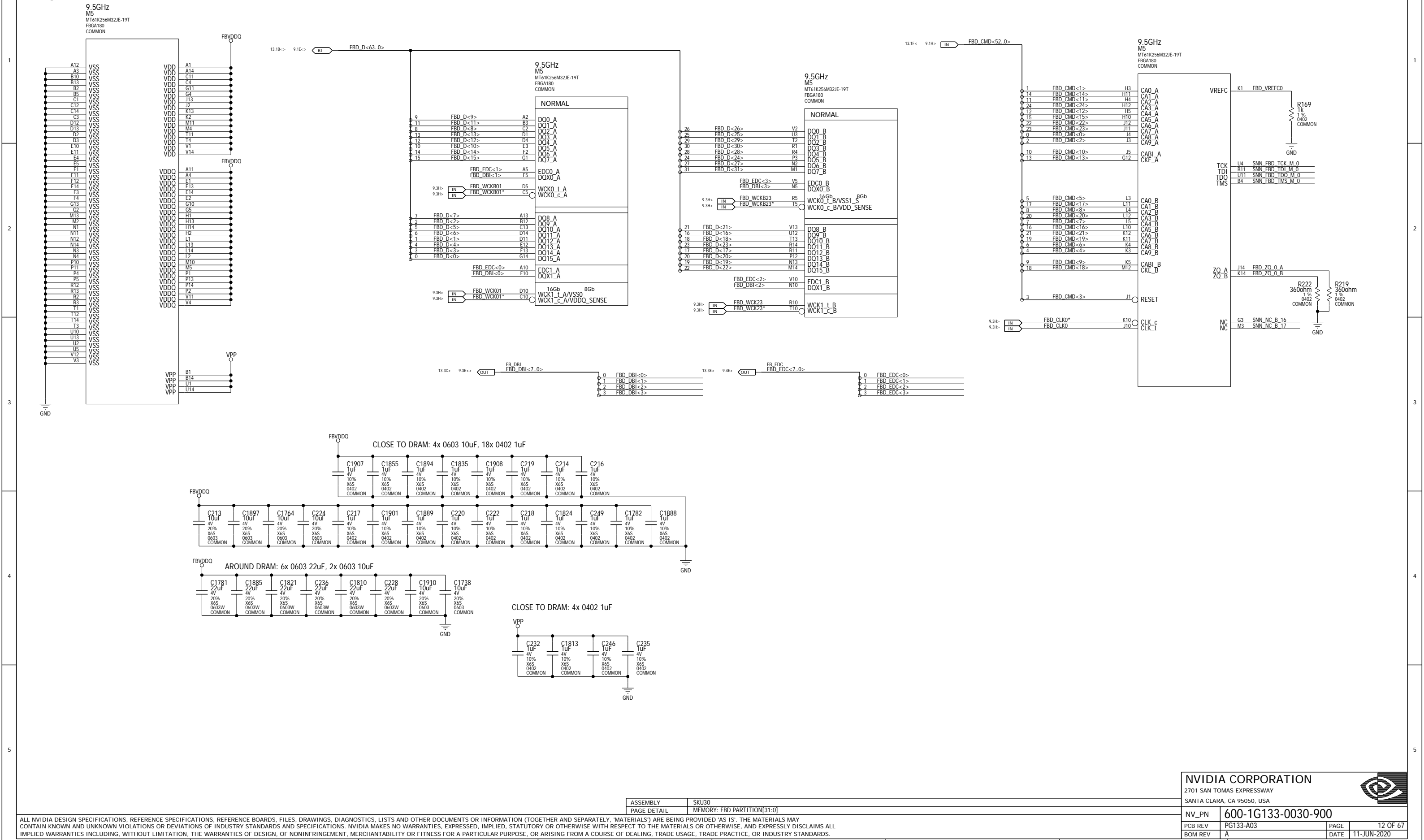
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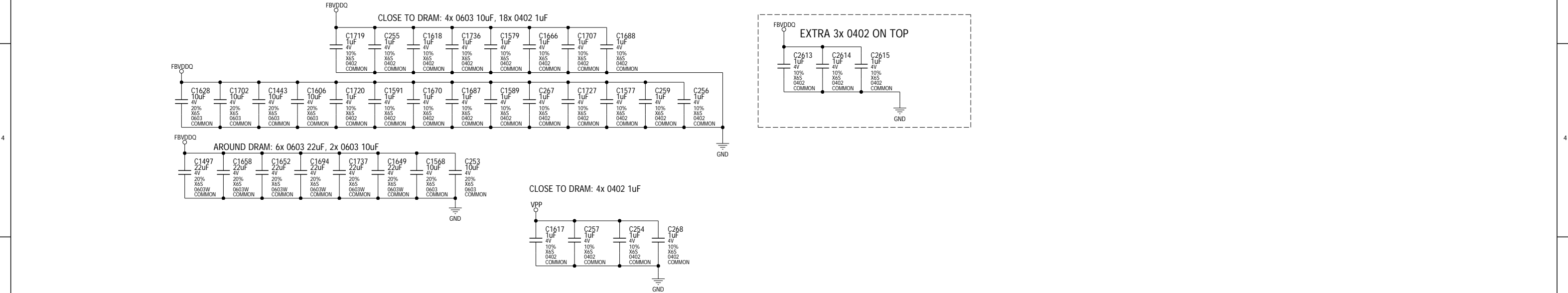
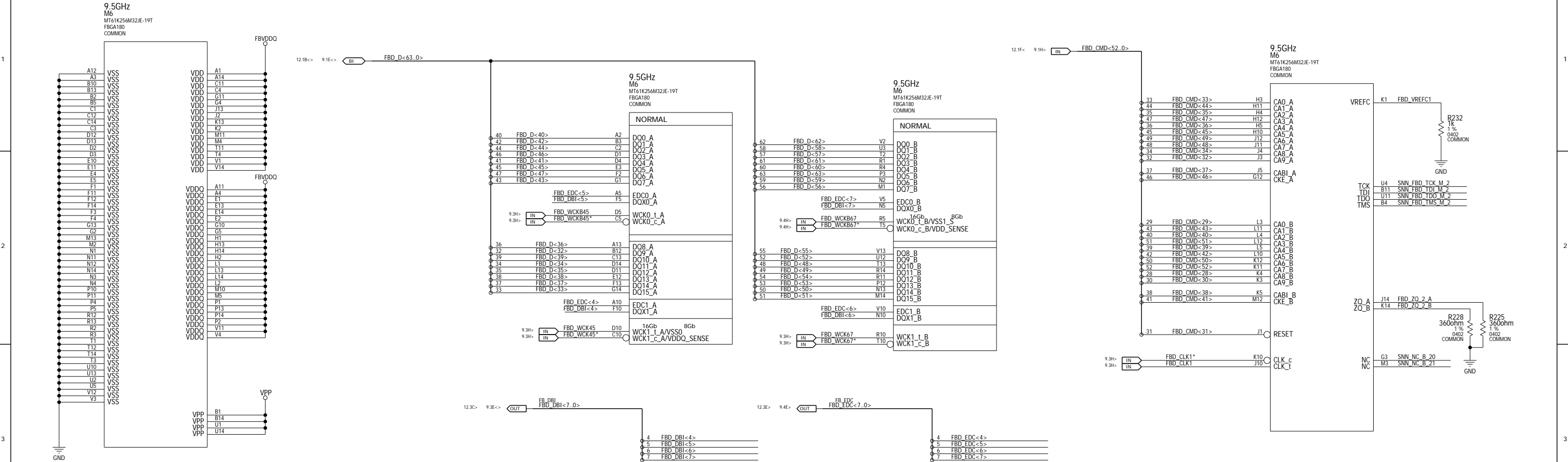




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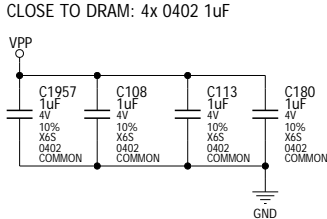
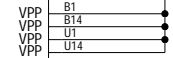
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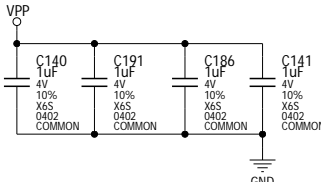
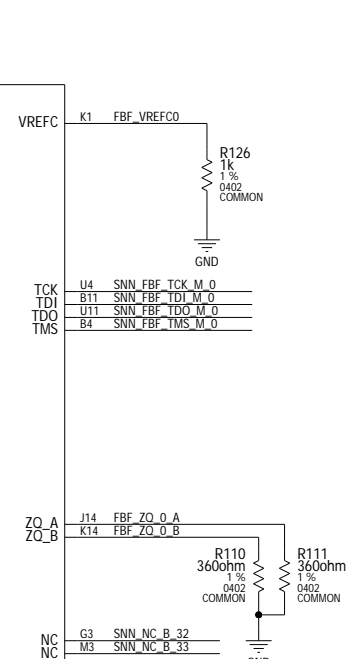
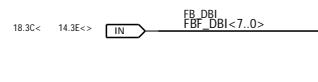
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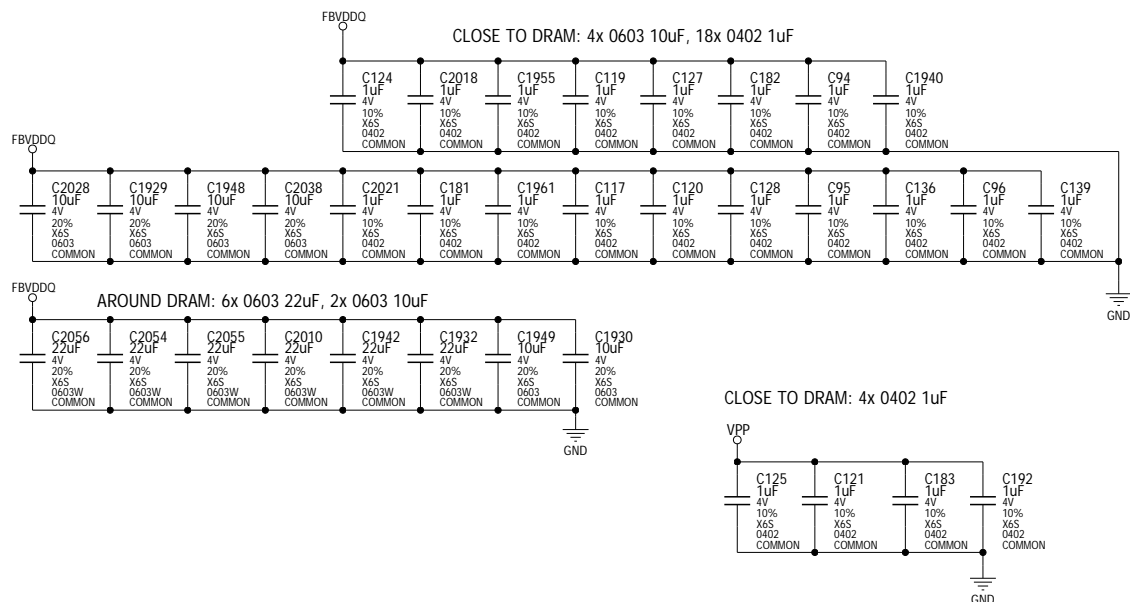
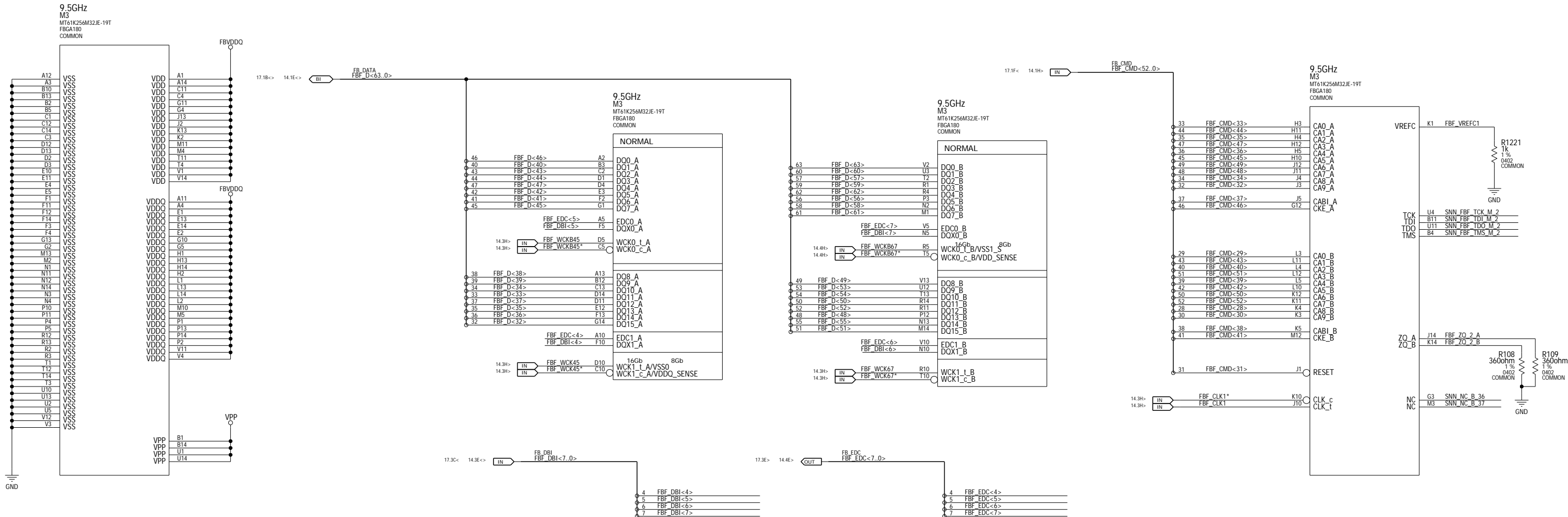
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ASSEMBLY	SKU30
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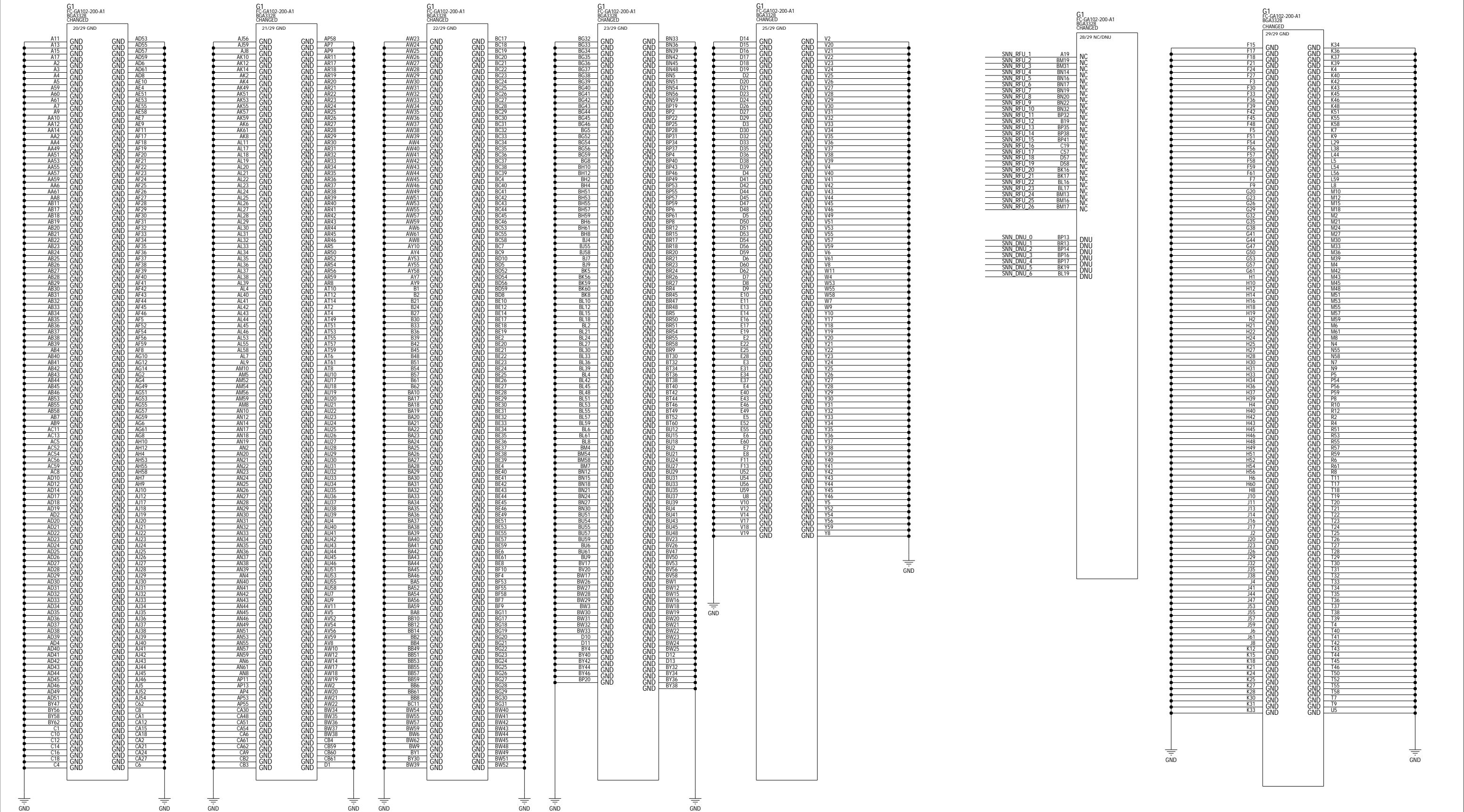
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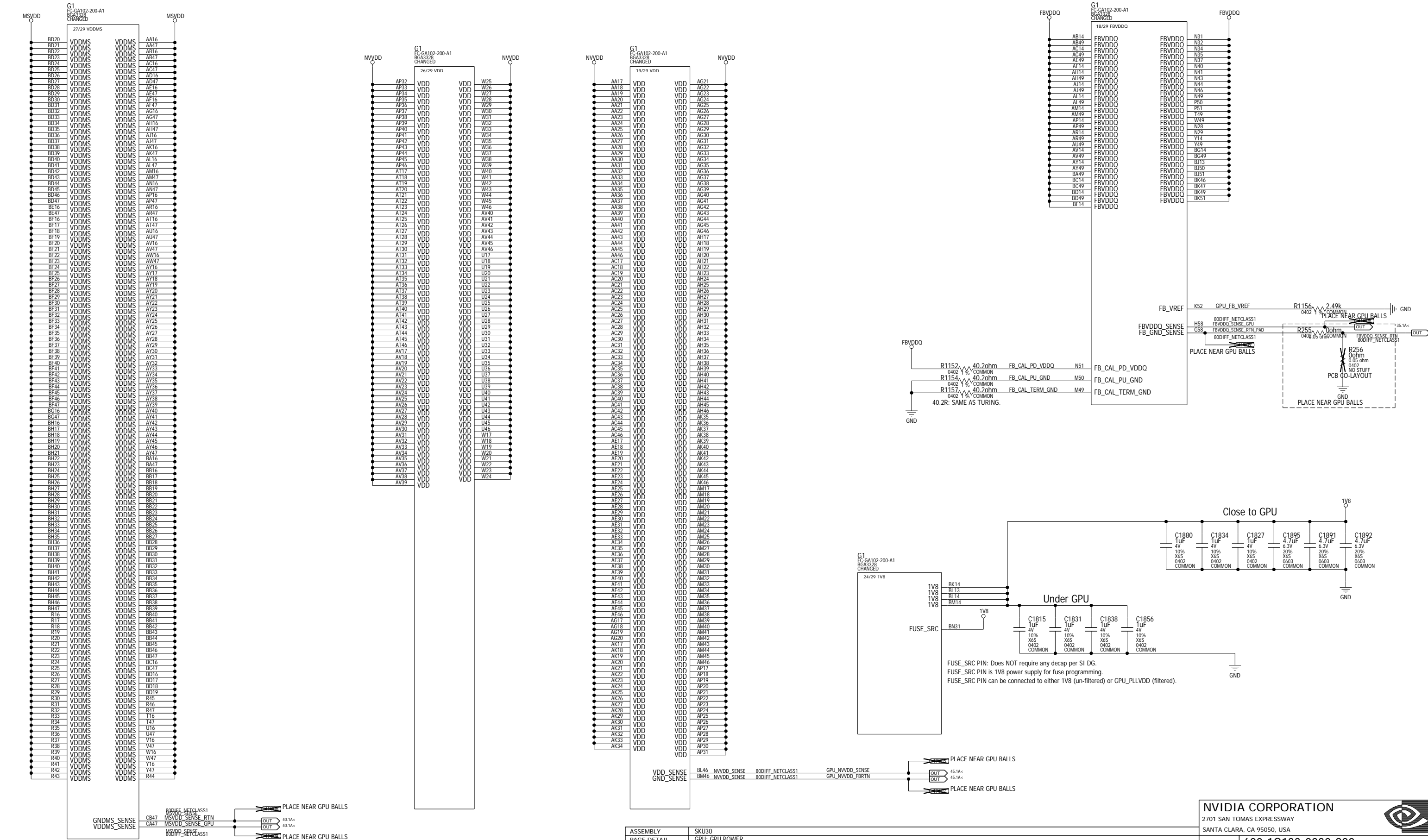
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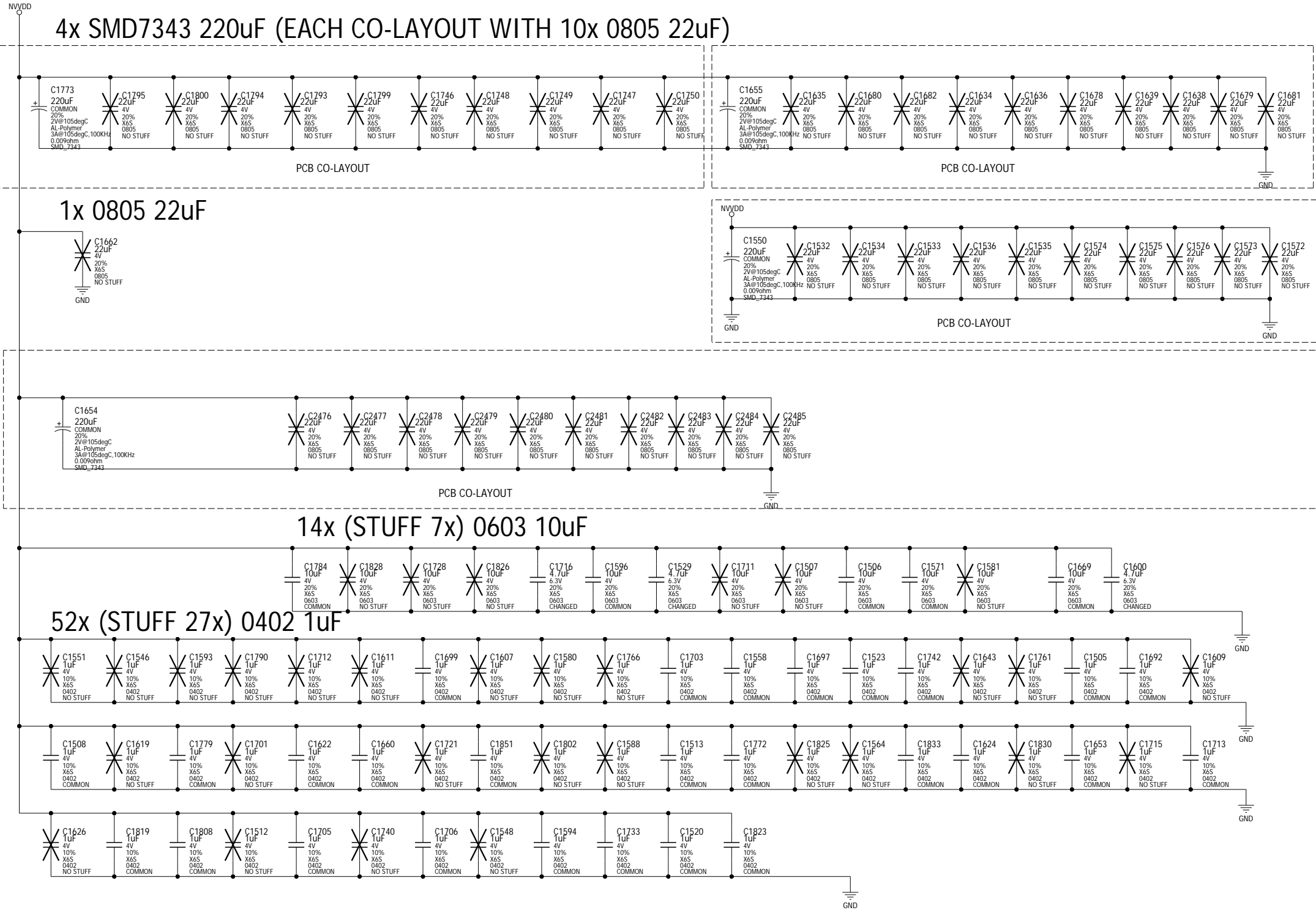
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NVVDD UNDER GPU



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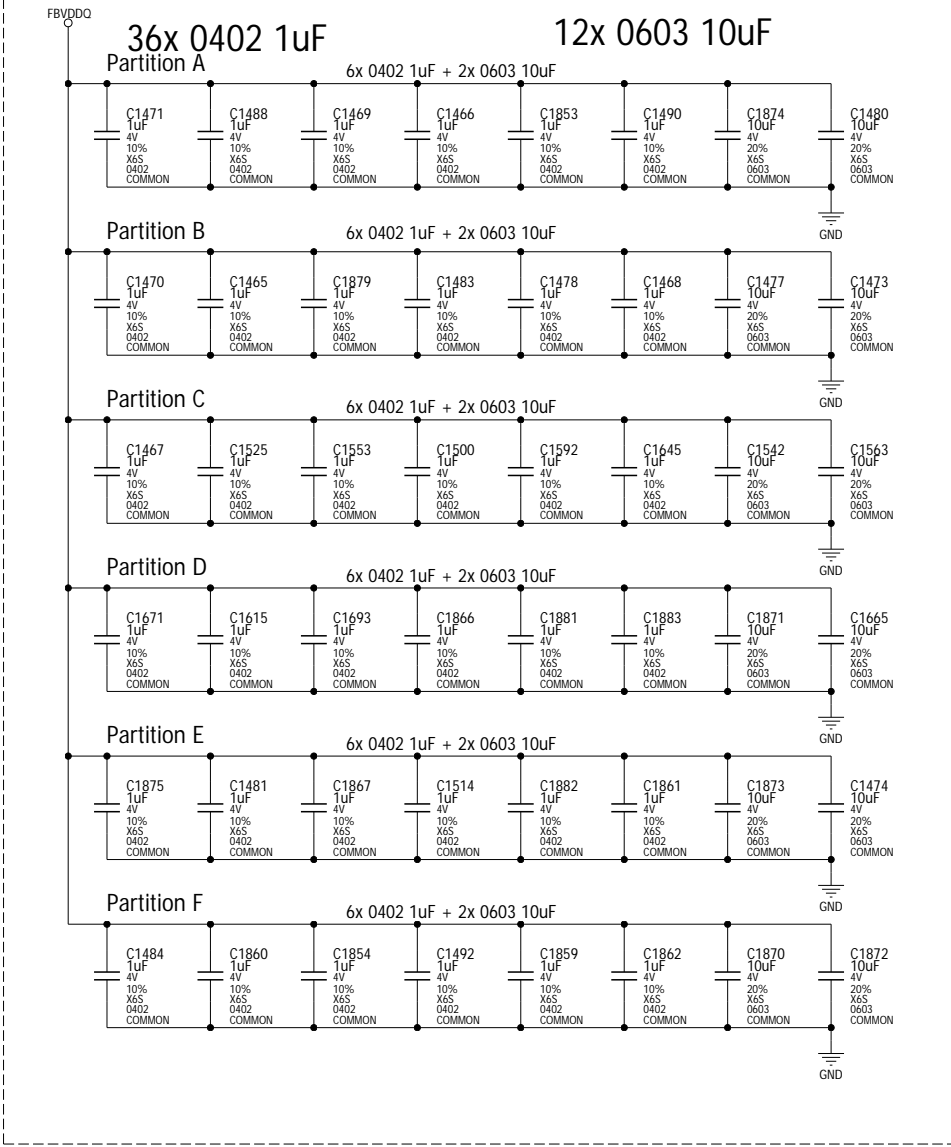
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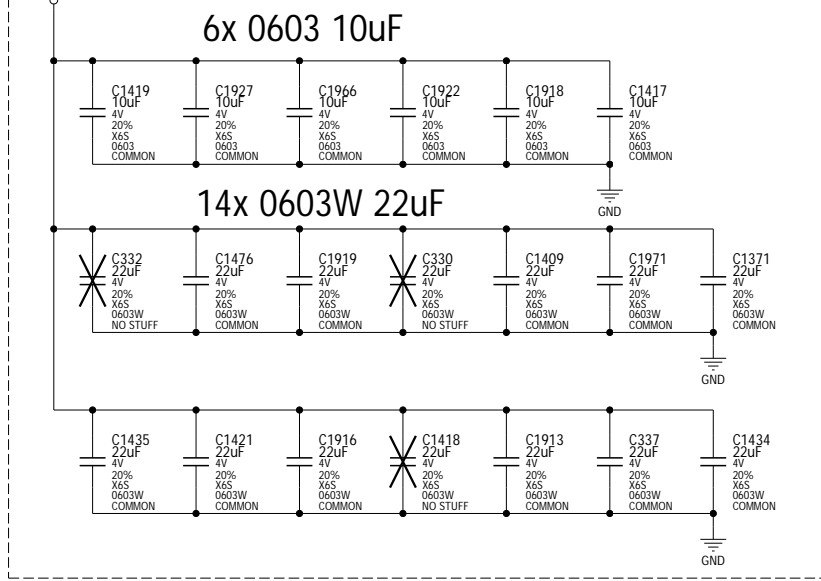
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FBVDDQ

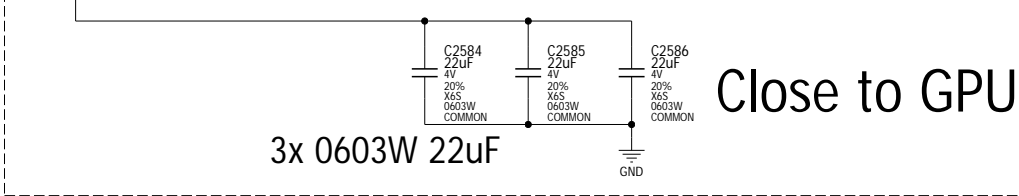
Under GPU



Close to GPU



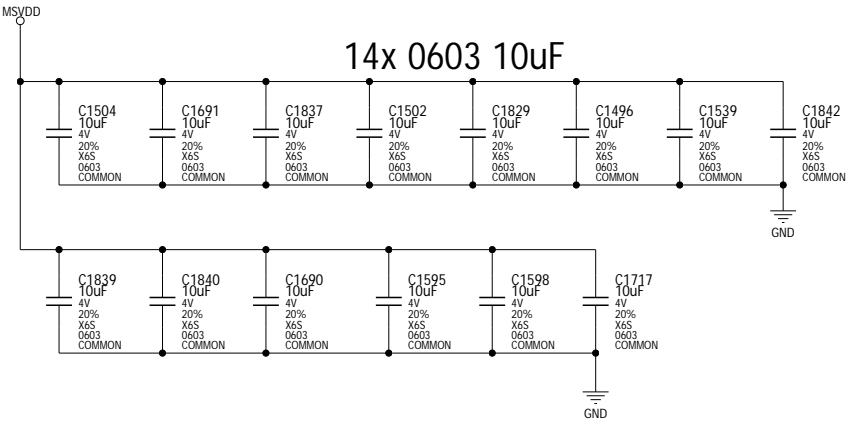
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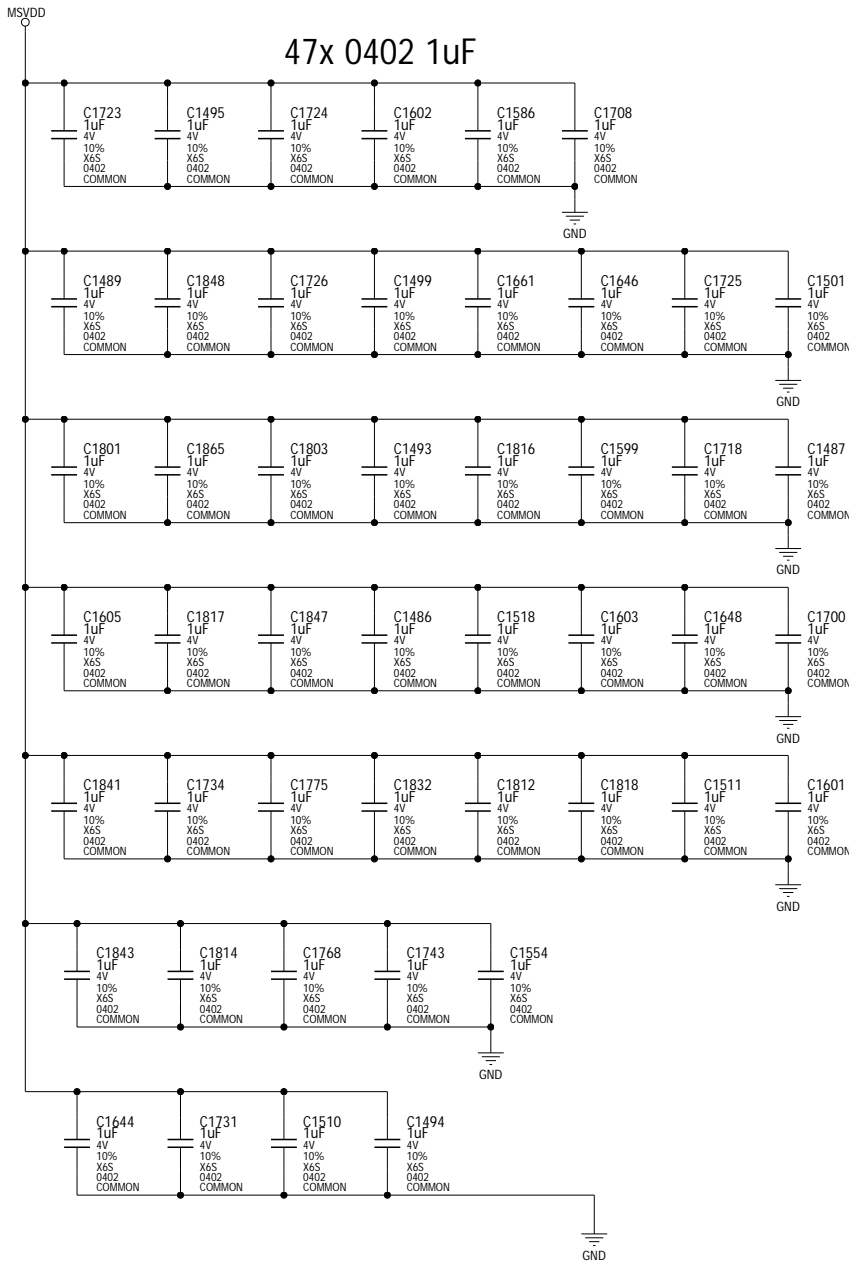
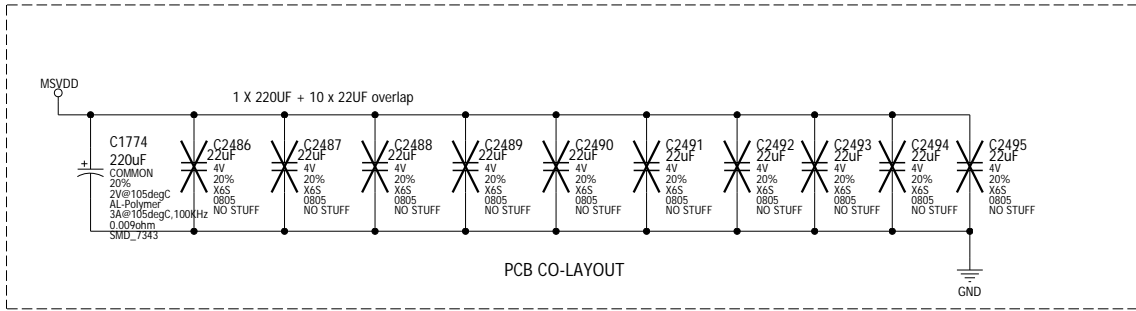
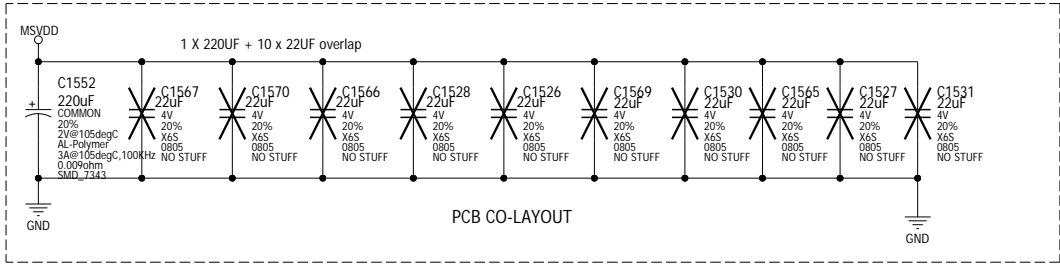
Page 23: GPU: MSVDD DECOUPLING

MSVDD

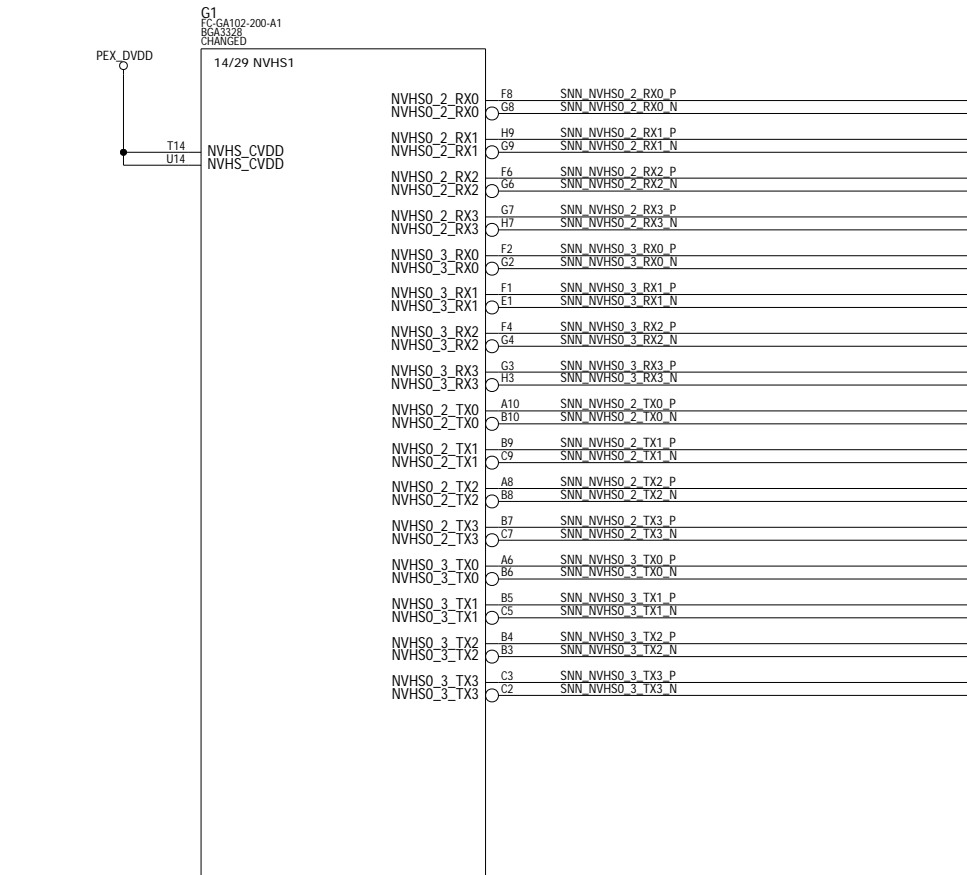
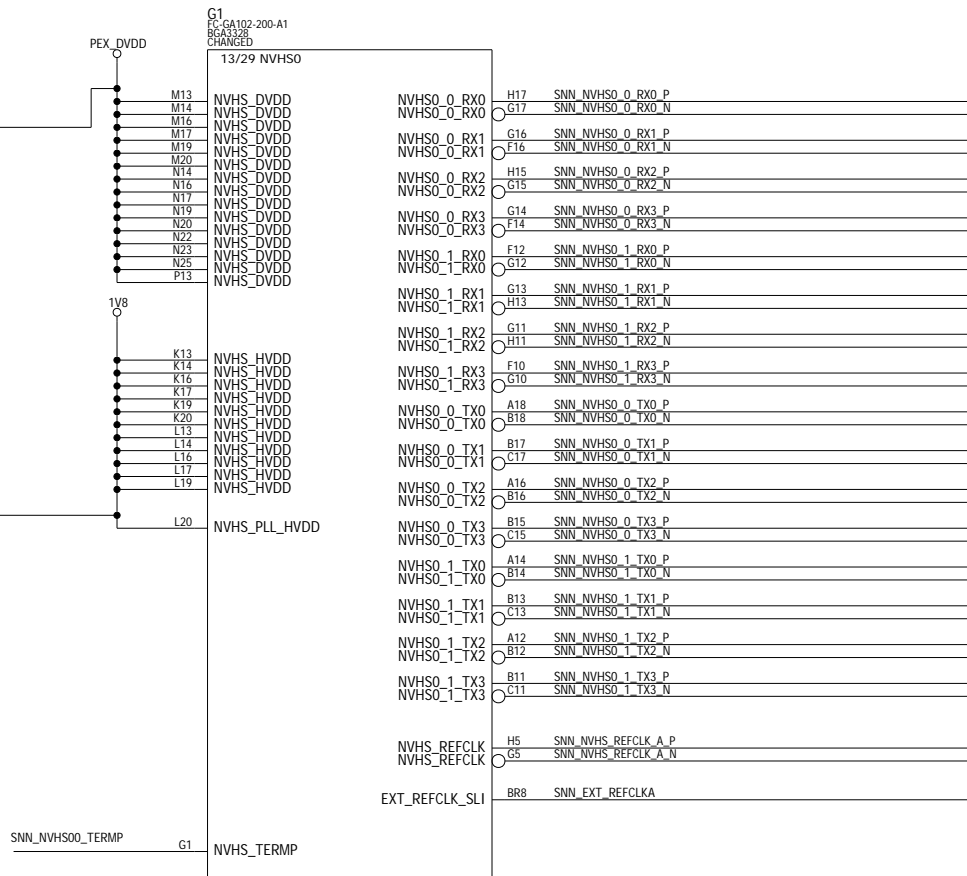
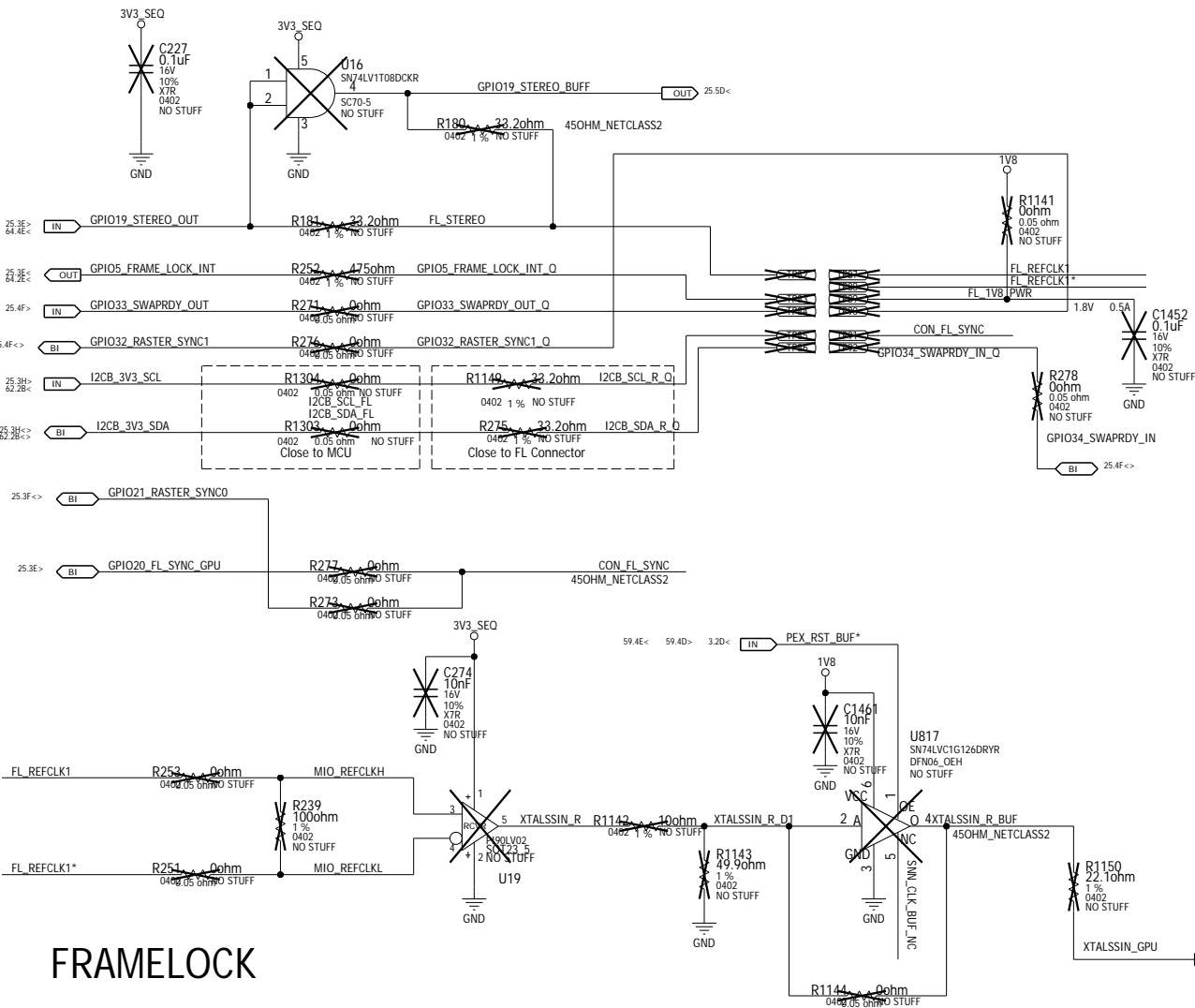
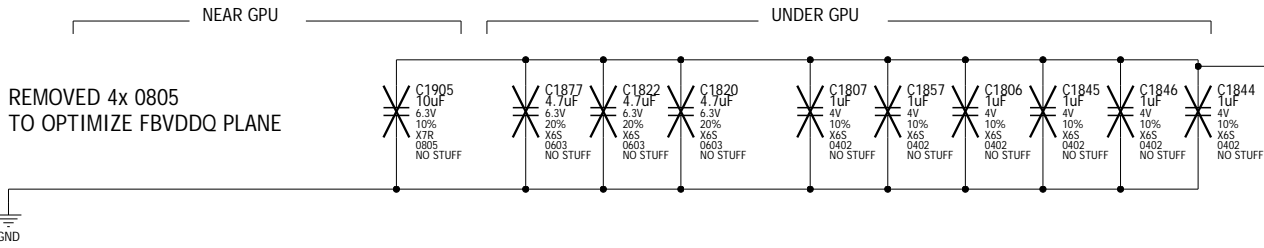
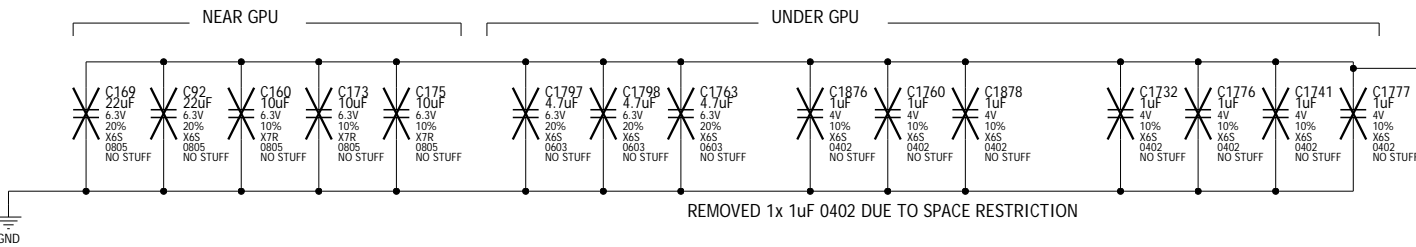
UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION



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PAGE DETAIL	GPU: NVHS x16, FRAMELOCK

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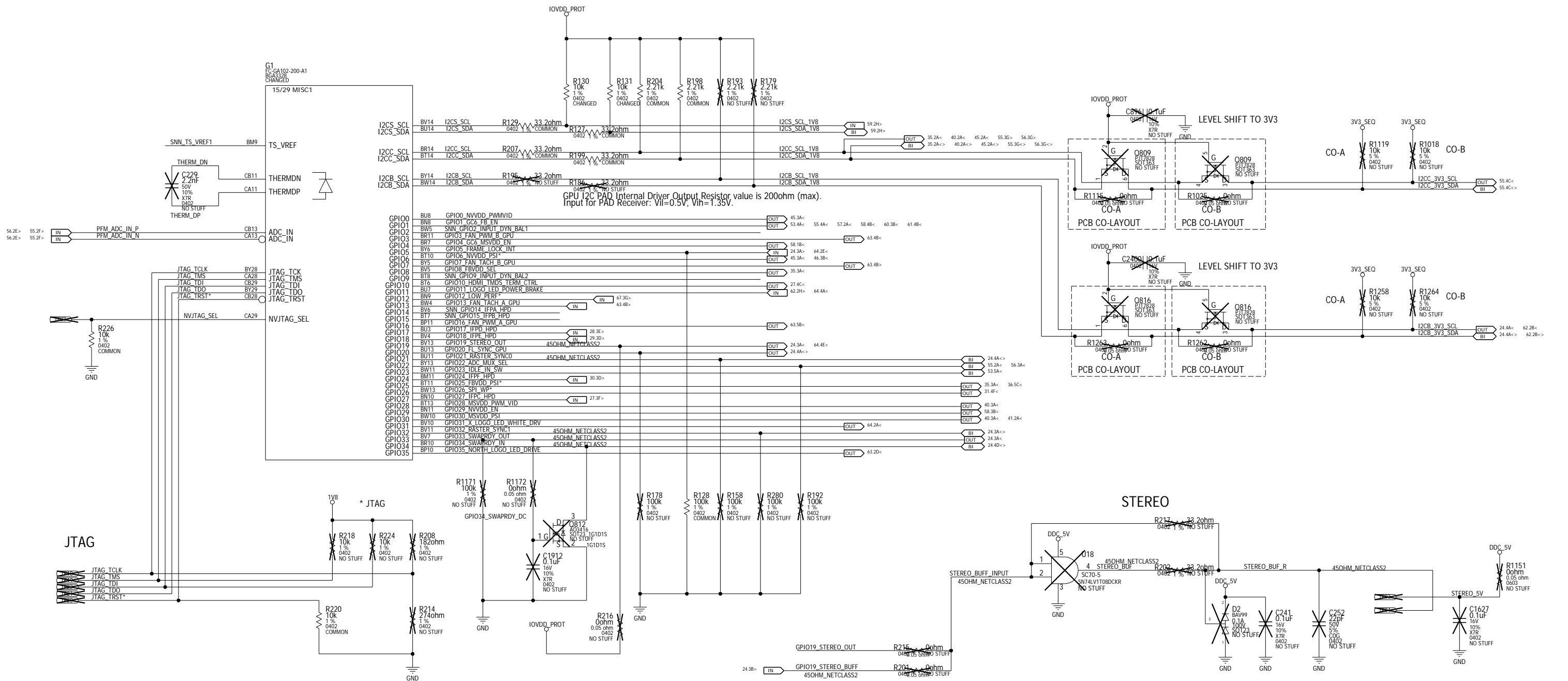
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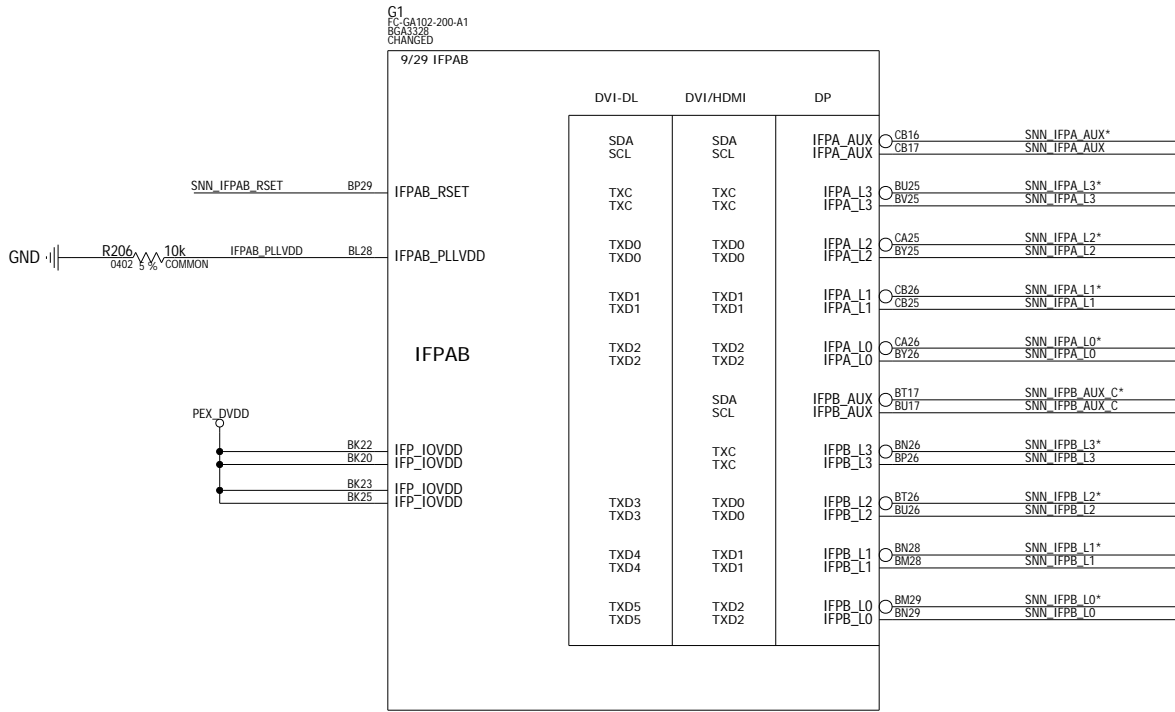


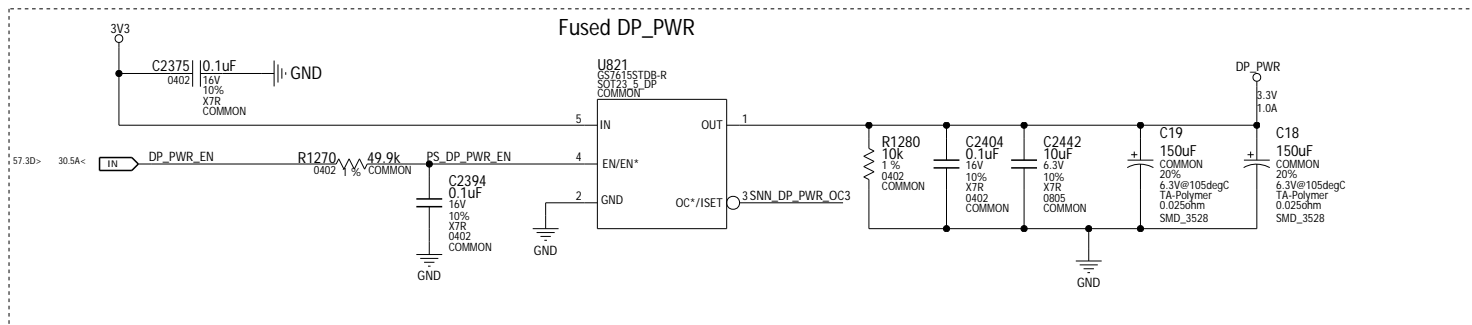
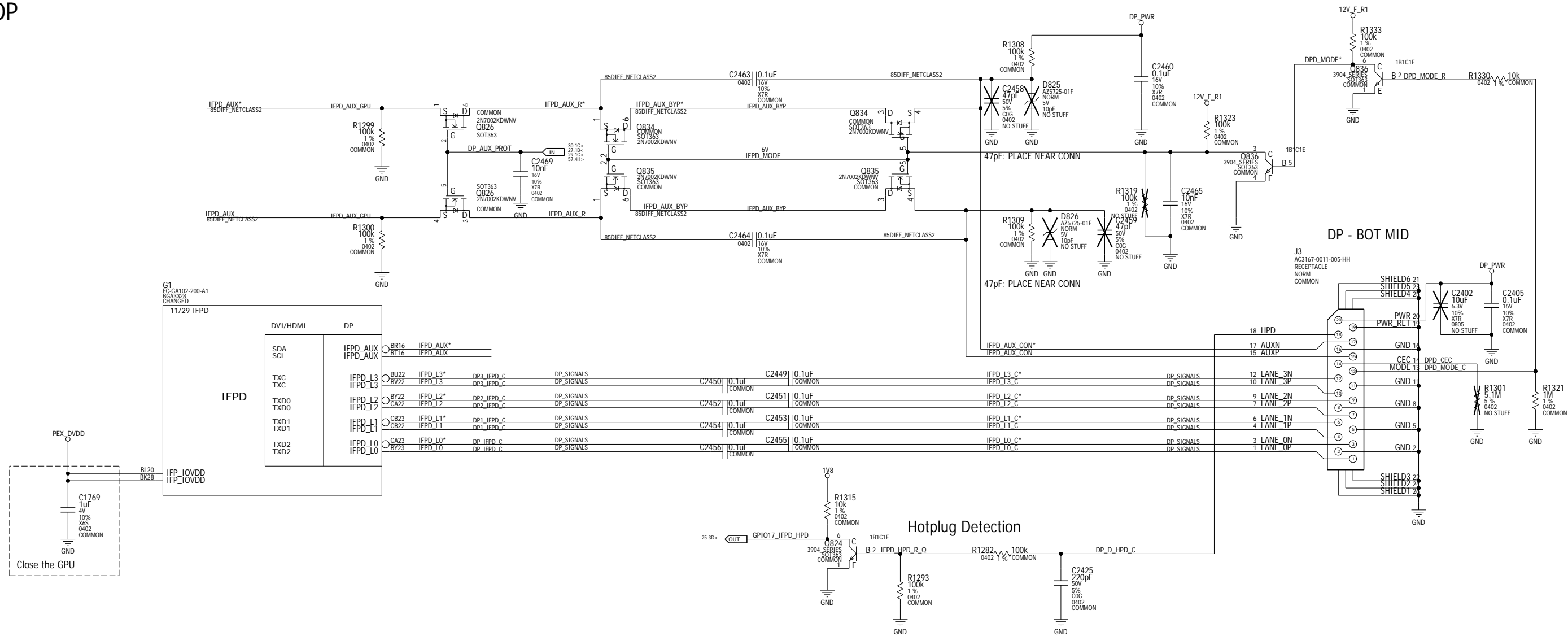
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REMOVED CYA FUSE_SRC LOAD SWITCH.




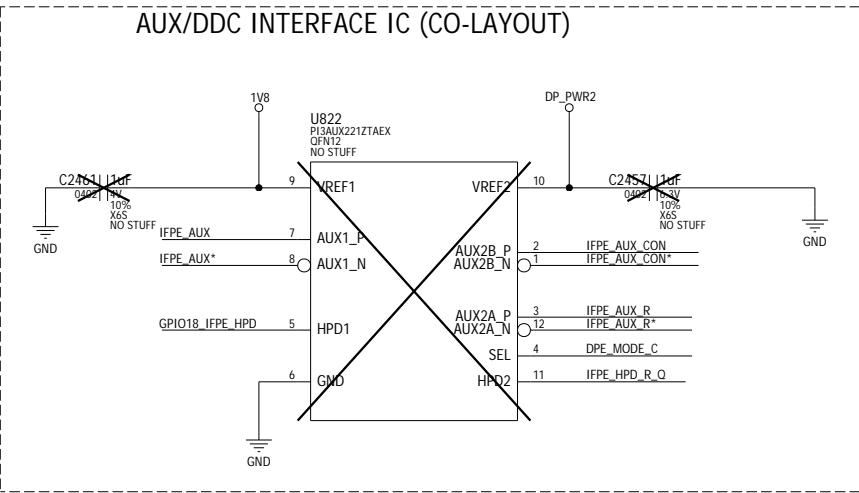
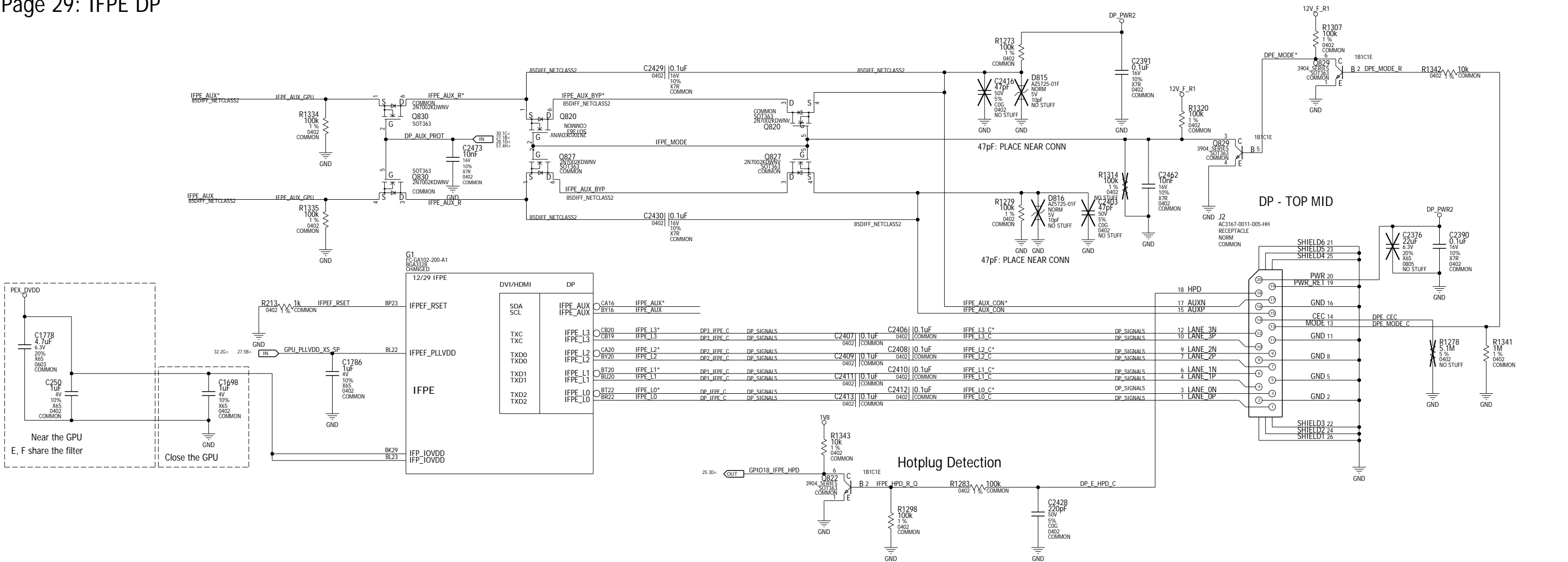


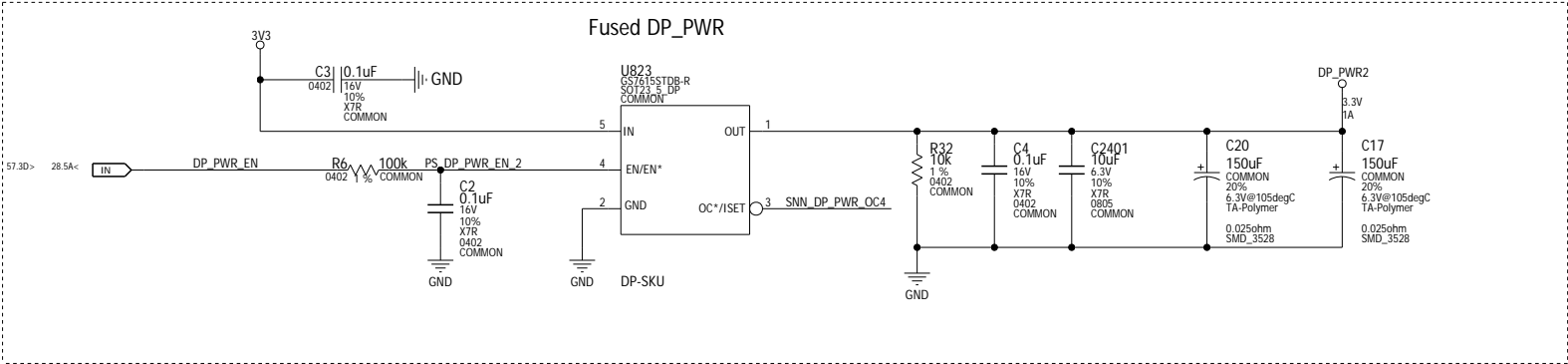
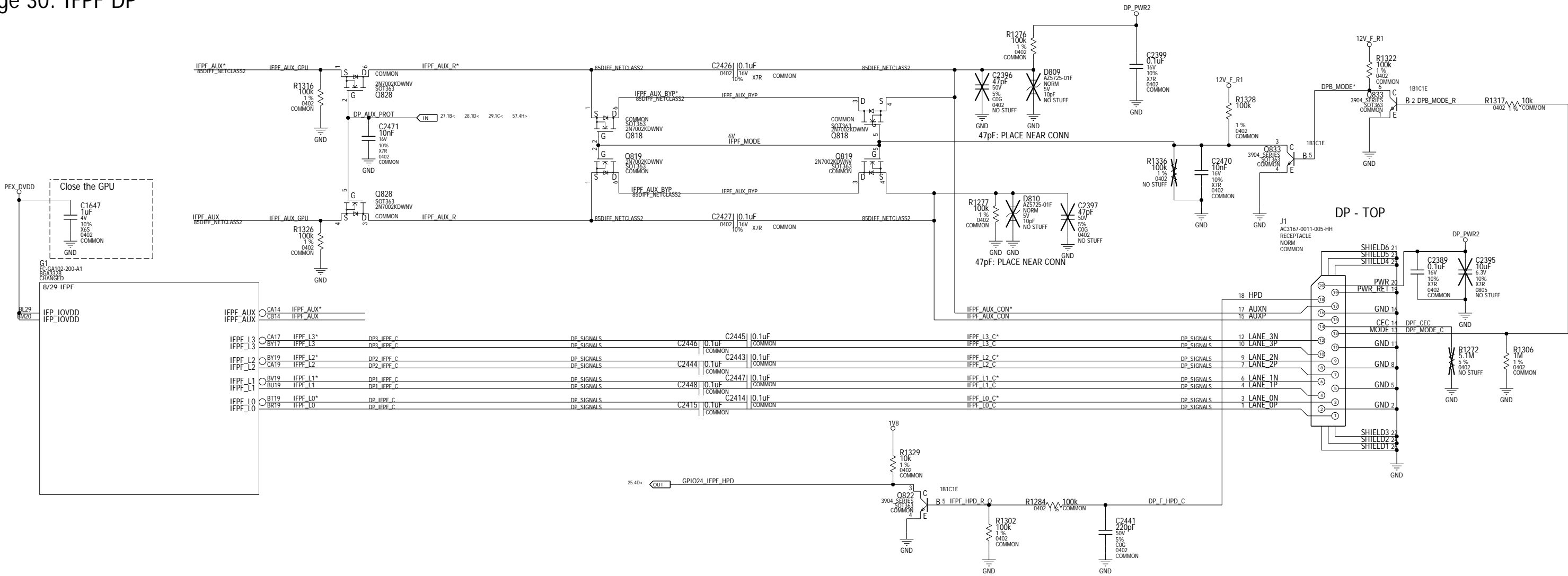


ASSEMBLY	SKU30
PAGE DETAIL	IFPD D

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Page 31: MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
M	H	L	01110	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

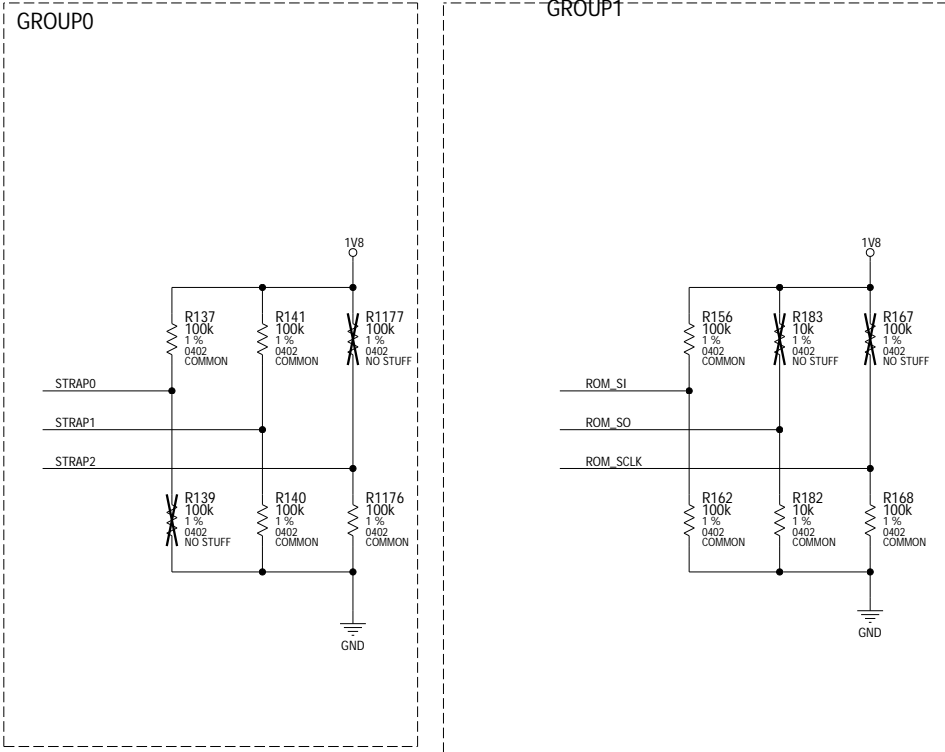
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

<-A01 PCB

<-OLD

<-DISMISSED

<-LATEST A02/A03 PCB



GROUP1 ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN0/1=33%/33%, FS_OVERT ENABLE
H	H	H	0111	FAN0/1=66%/66%, FS_OVERT ENABLE

<-DEFAULT

GROUP2 STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

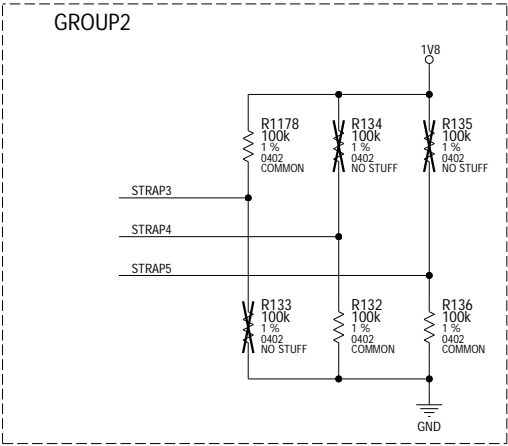
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

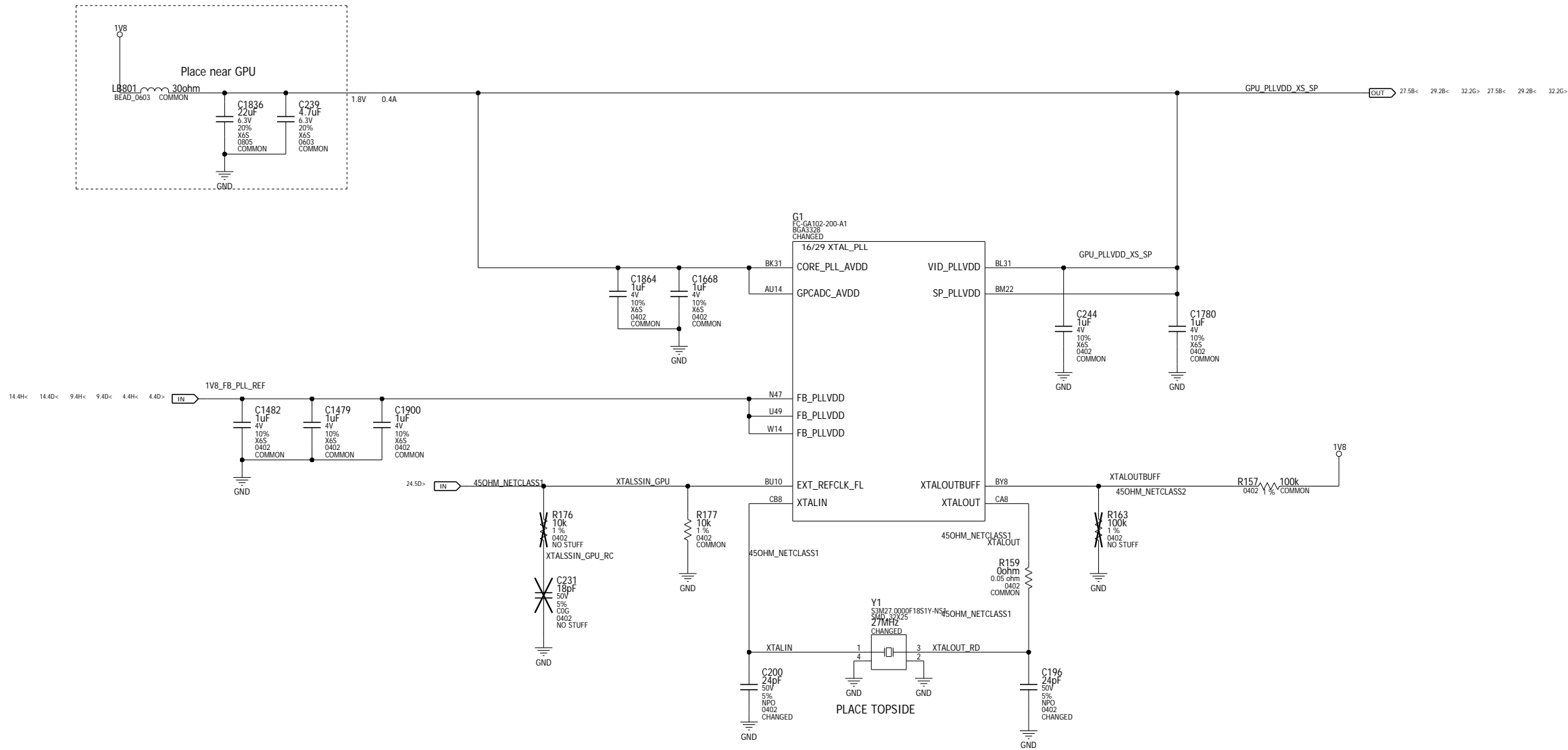
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

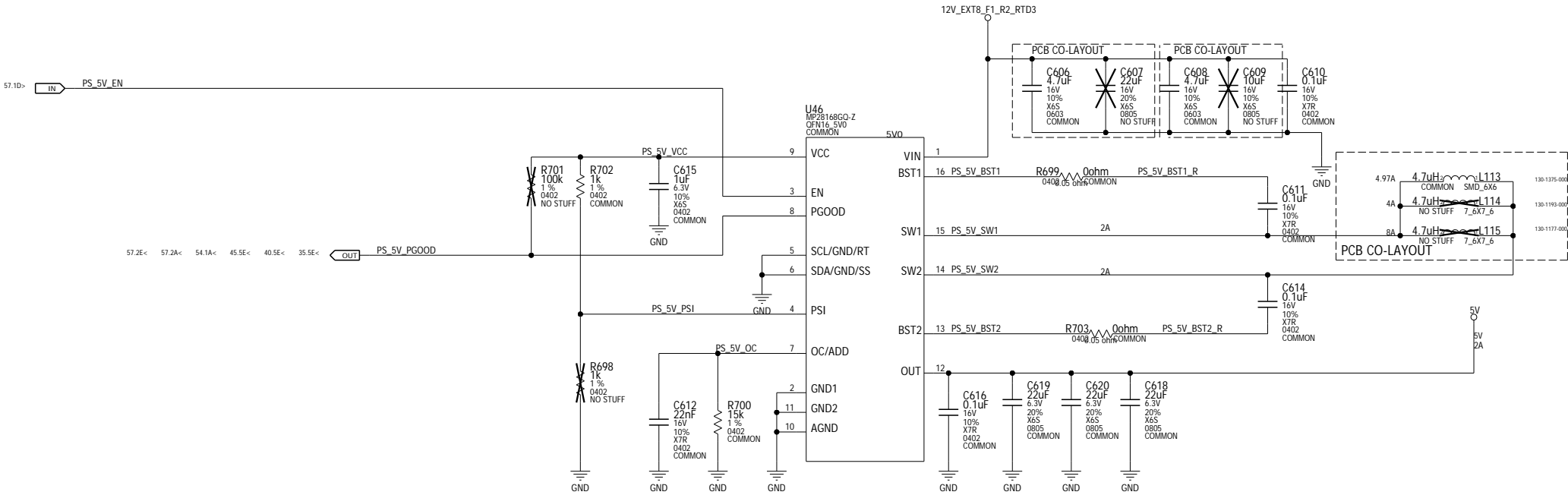
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

<-Default



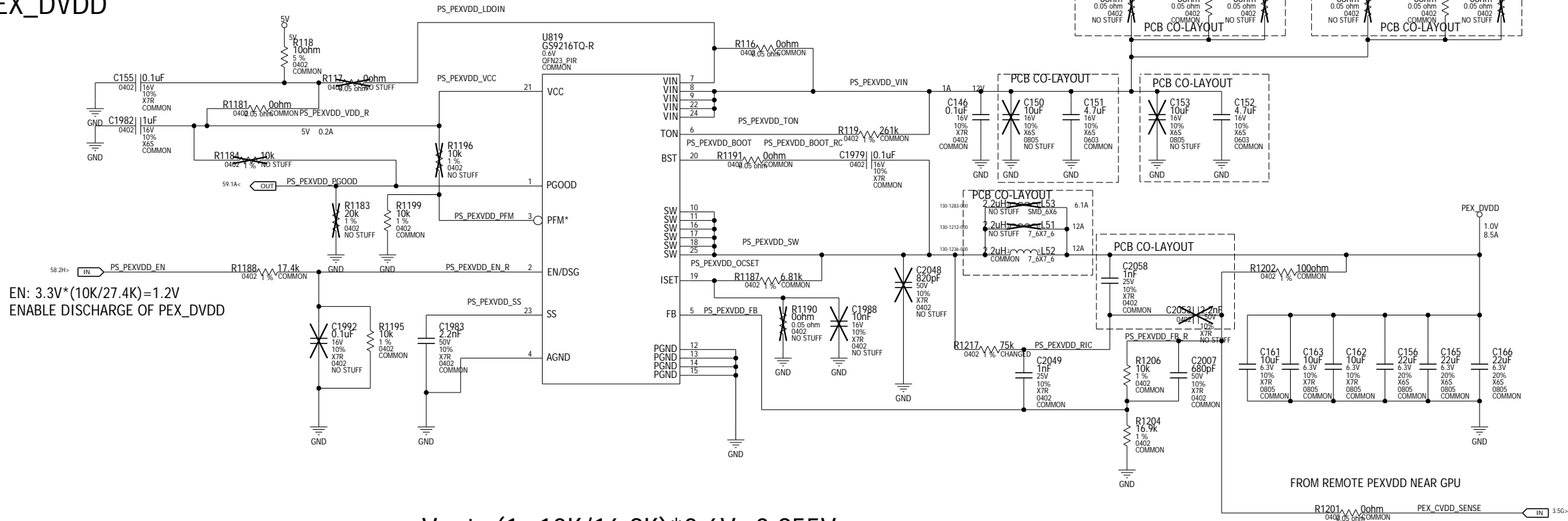
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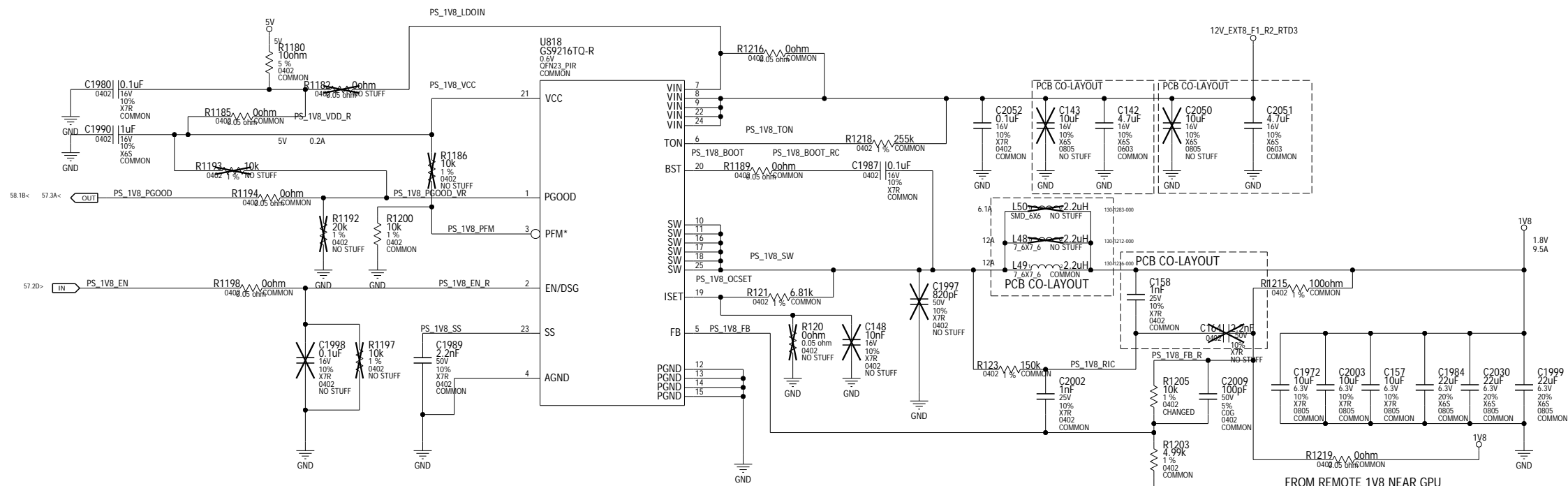
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PEX_DVDD



$$V_{out} = (1 + 10K/16.9K) * 0.6V = 0.955V$$

1V8



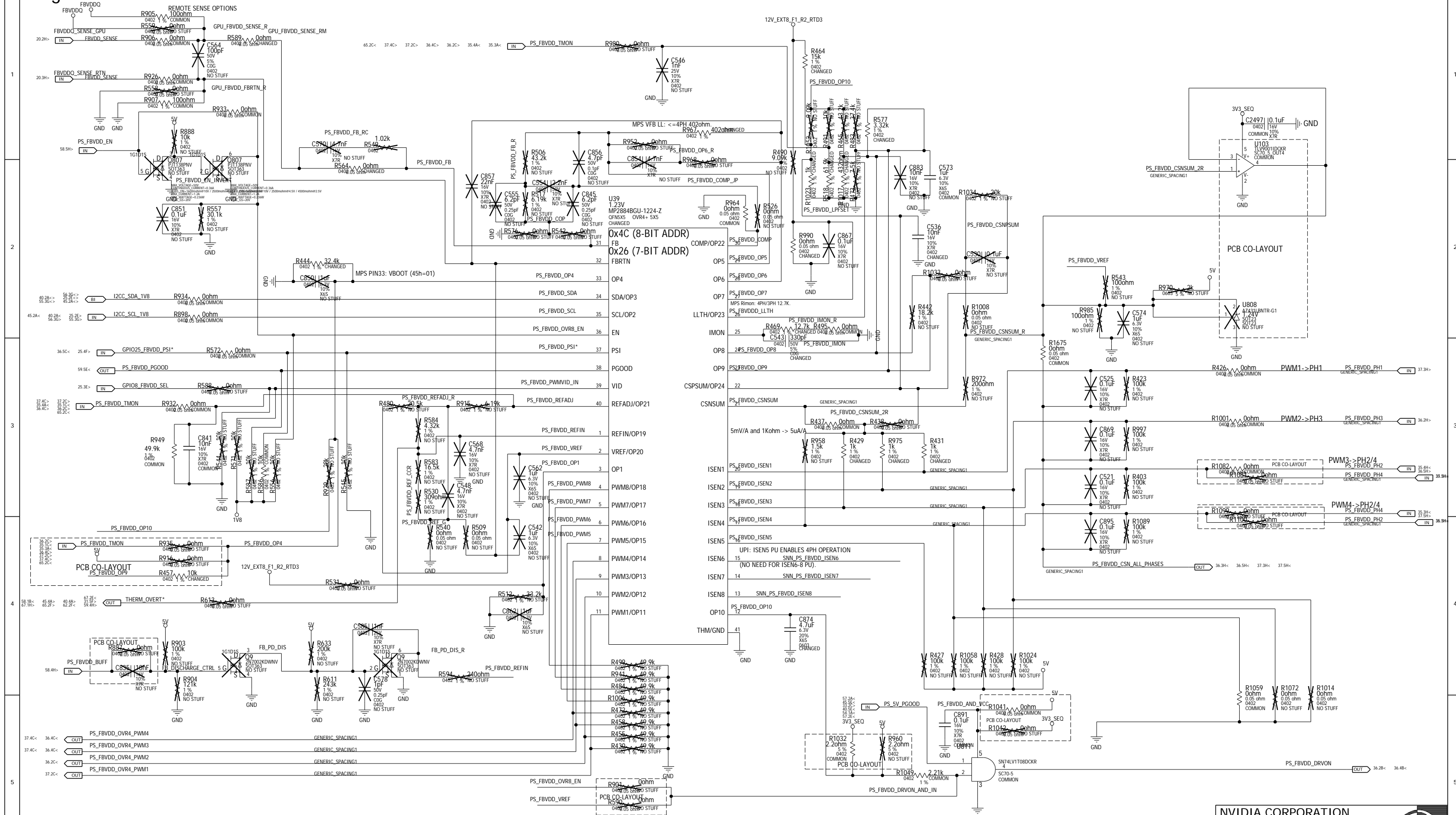
$$V_{out} = (1 + 10K/4.99K) * 0.6V = 1.802V$$

ASSEMBLY	SKU30
PAGE DETAIL	PS: PEX_DVDD, 1V8

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NV_PN	600-1G133-0030-900		
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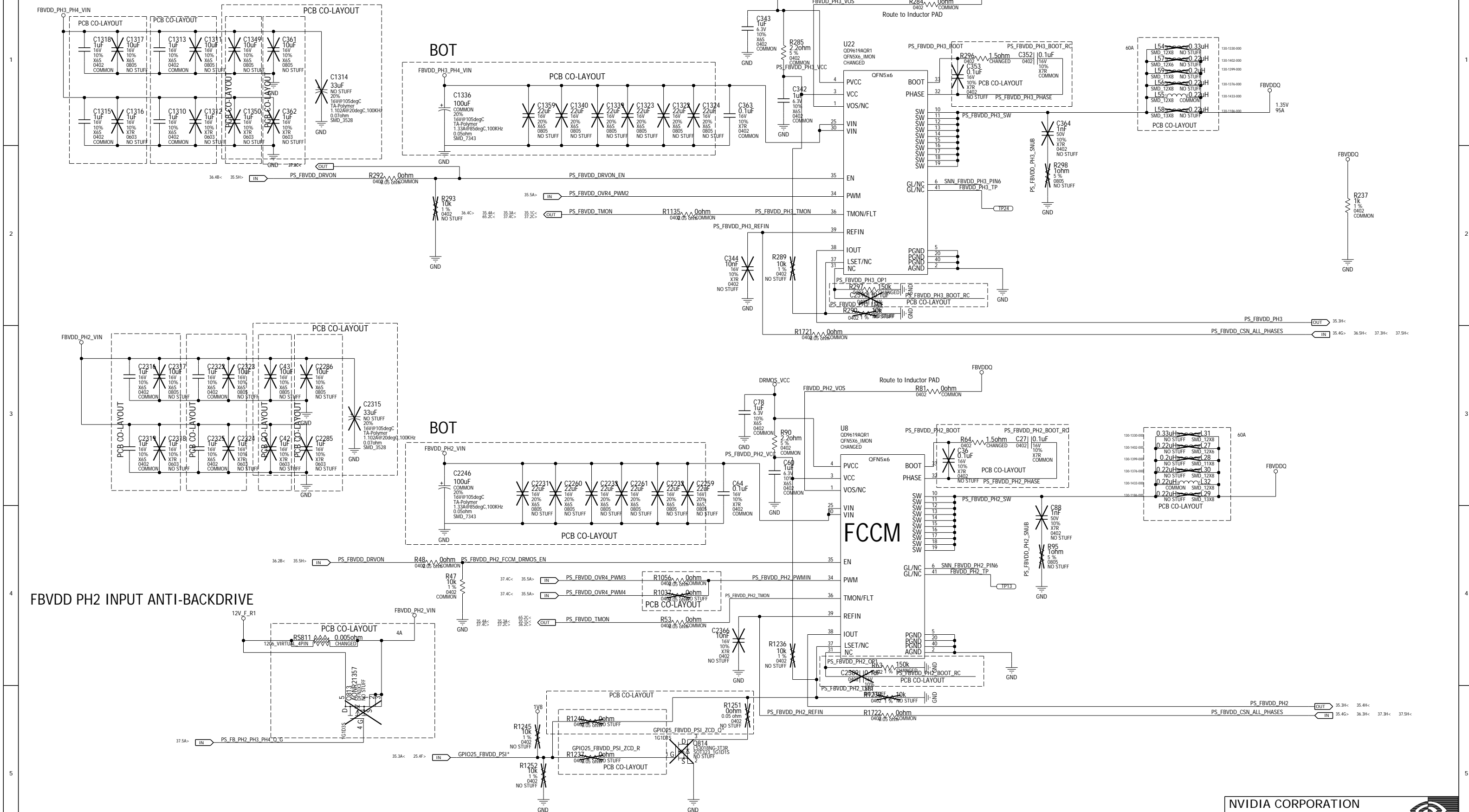
Page 35: PS: FBVDD Controller



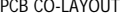
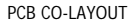
ASSEMBLY	SKU30
PAGE DETAIL	PS: FBVDD CONTROLLER OVR4i

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
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
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PCB REV	PG133-A03	PAGE	35 OF 67	
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12V_EXT8_F1_R2_RTD3

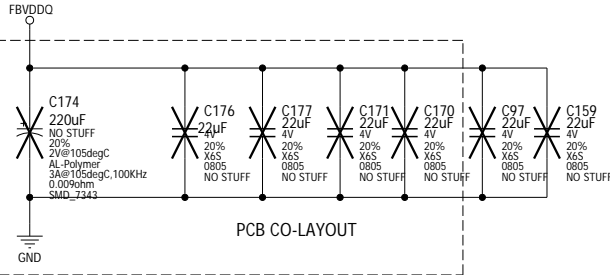


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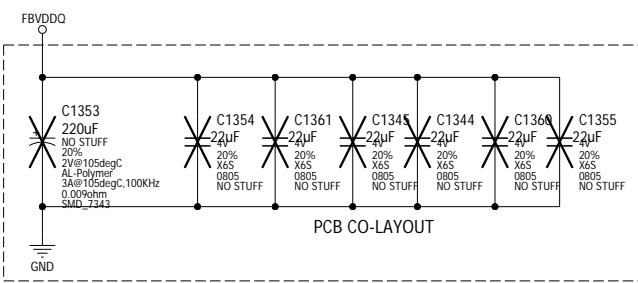
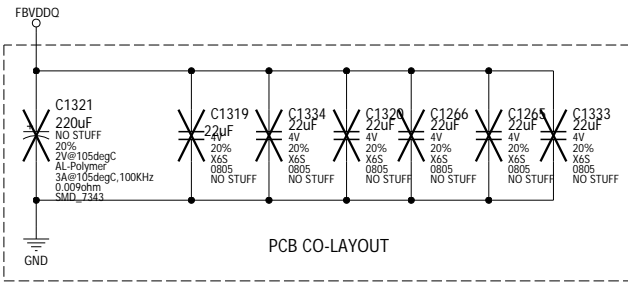
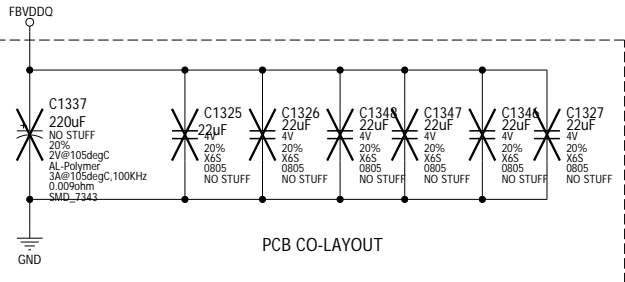
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-1G133-0030-900		
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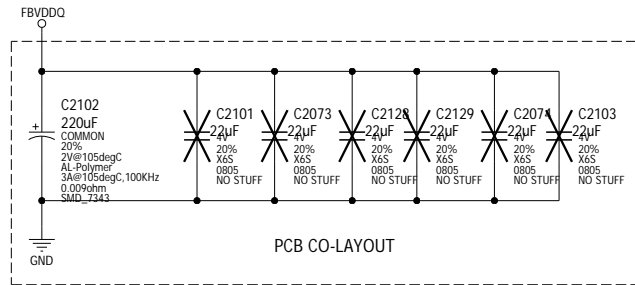
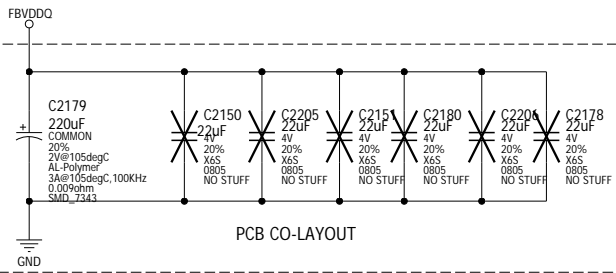
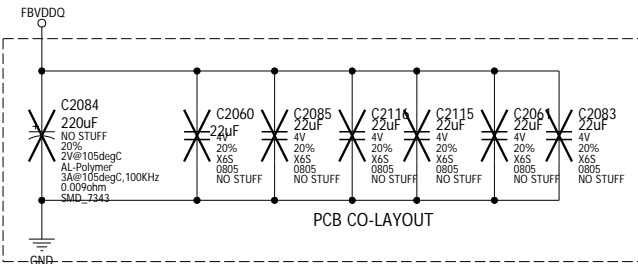
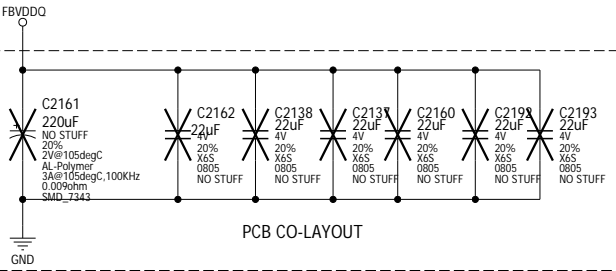
PLACE NEAR POWER SUPPLY
8x SMD7343 330uF CO-LAYOUT WITH 48x 0805 22uF



TOP WEST OF PCB

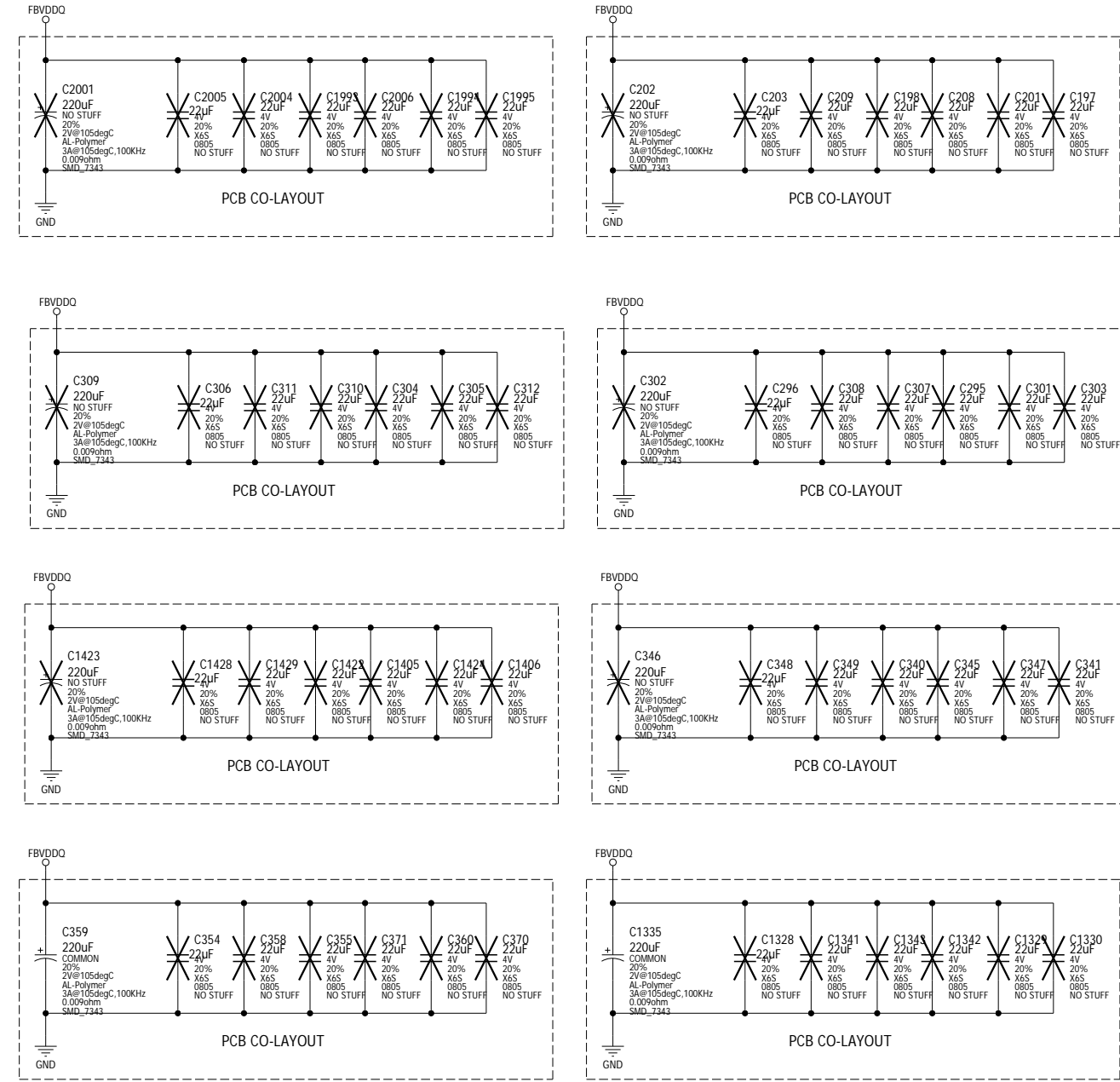


BACK WEST OF PCB



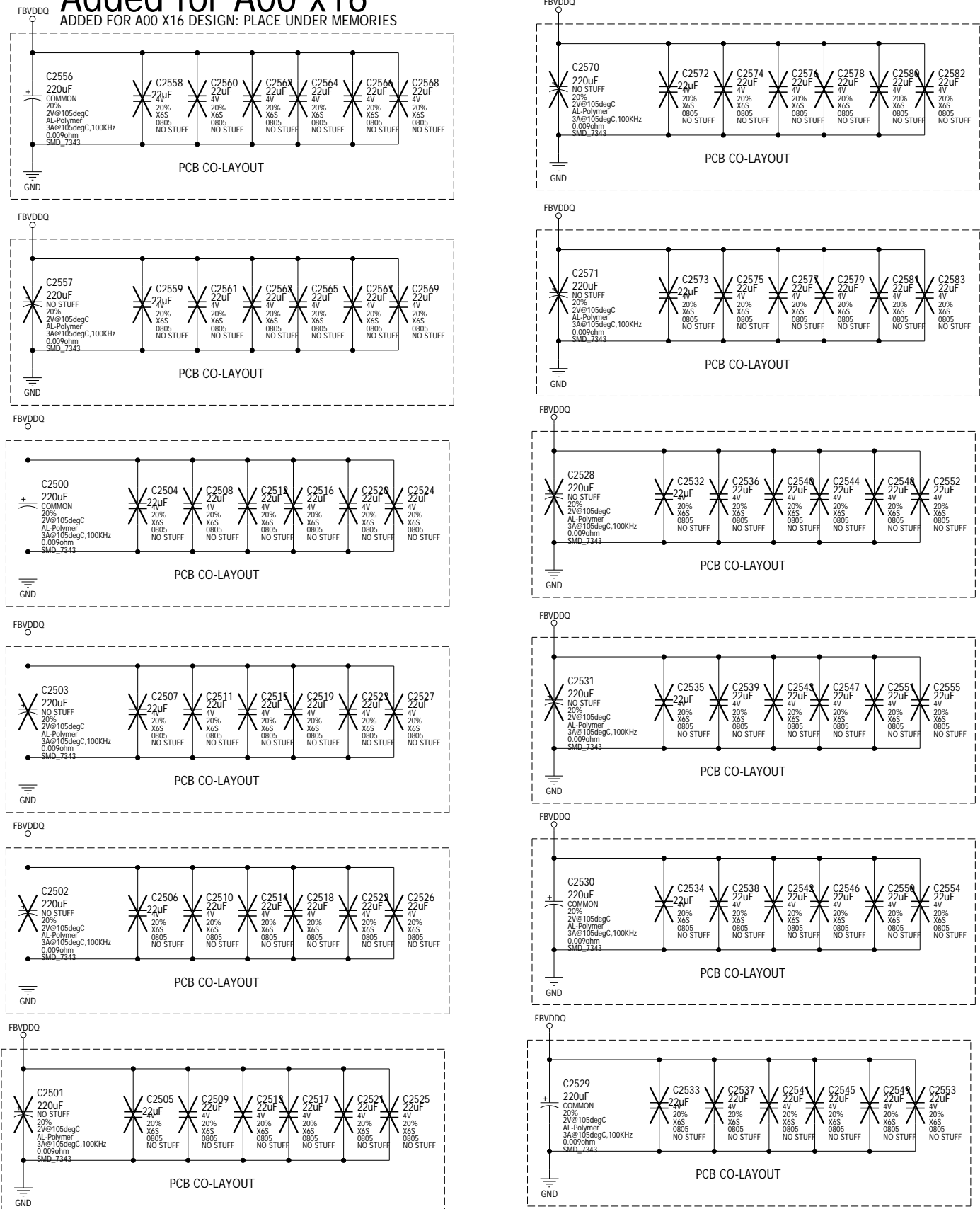
BACK EAST OF PCB

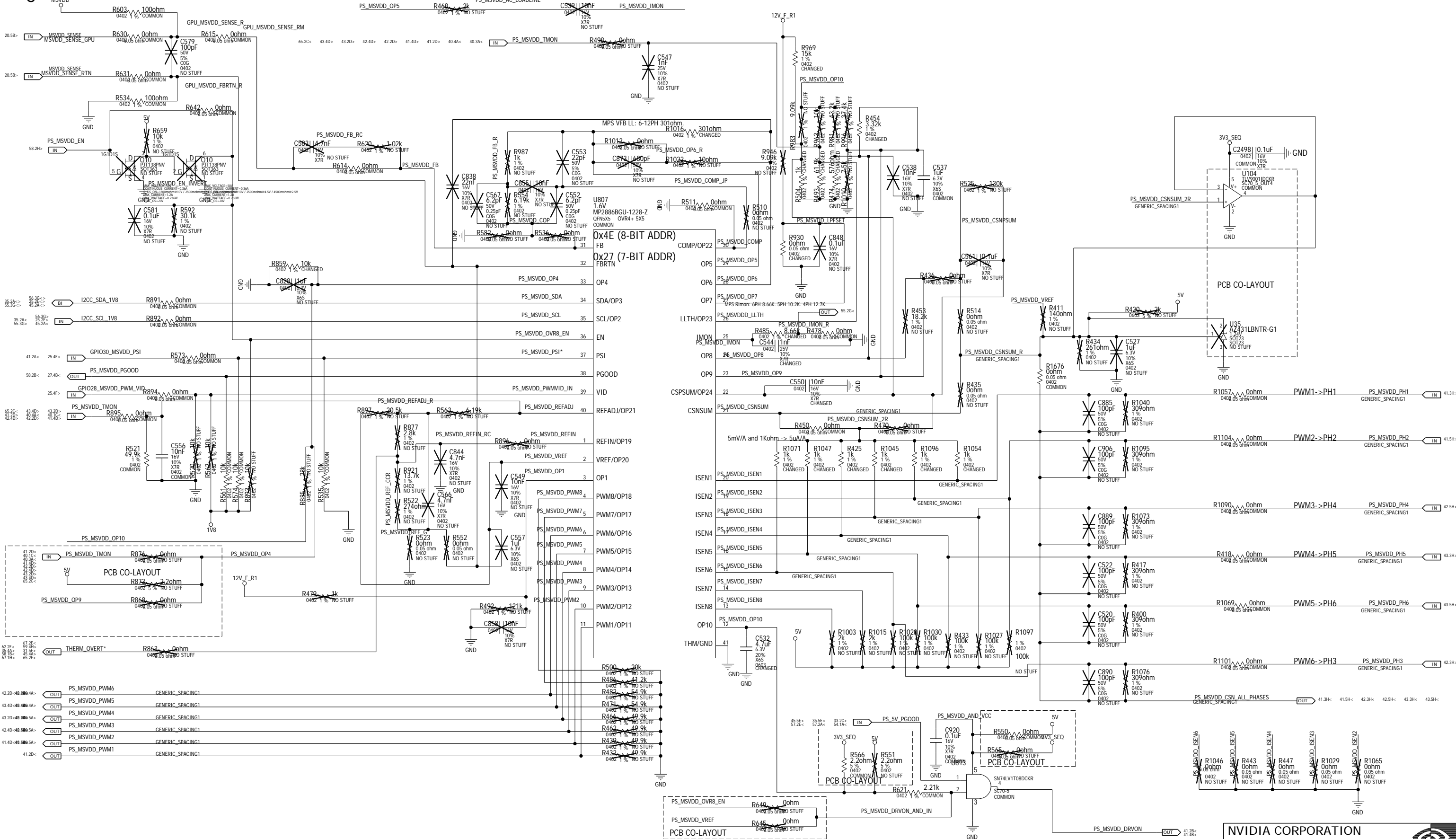
PLACE NEAR MEMORY



Added for A00 x16


ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES

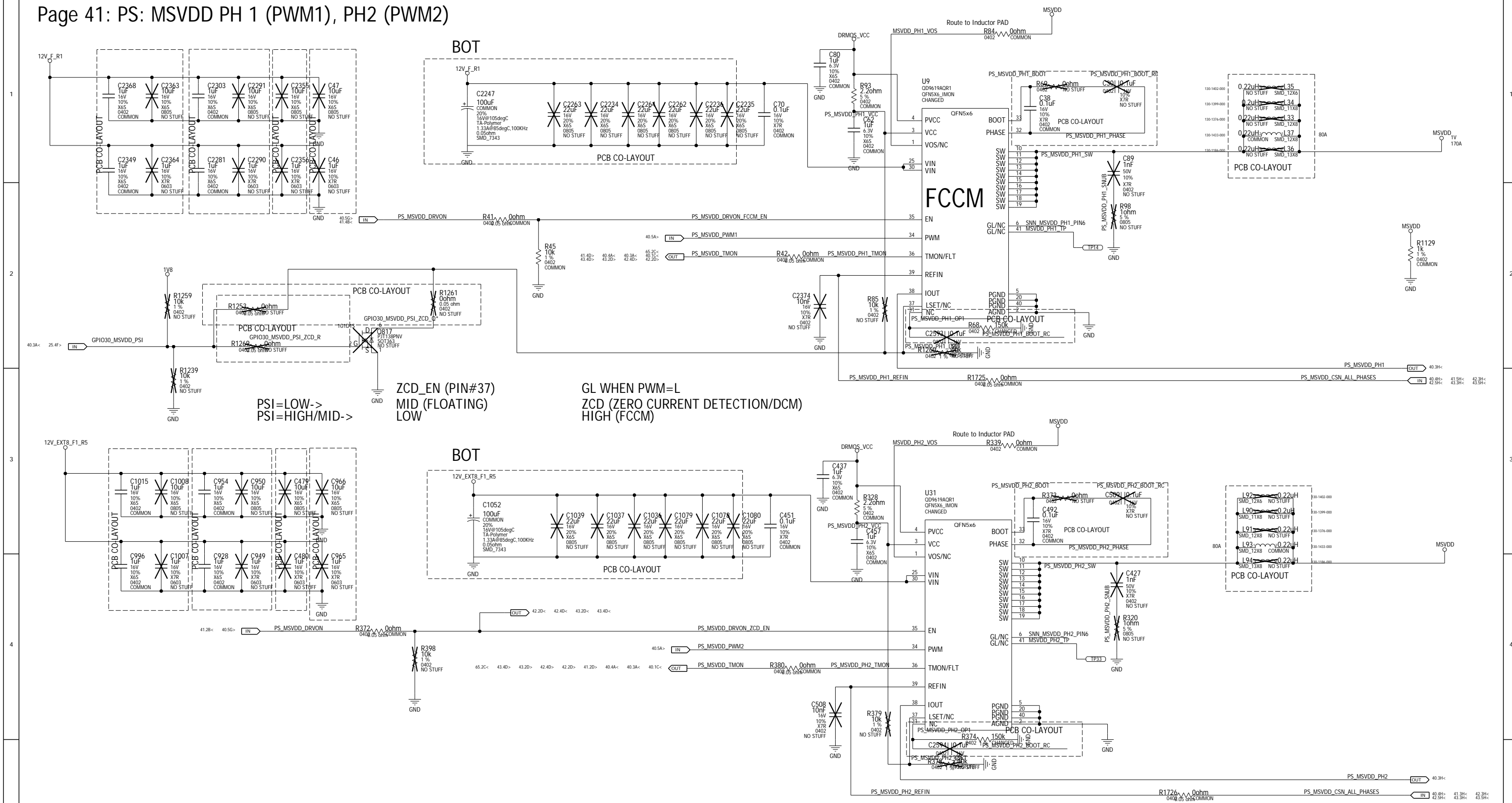




ASSEMBLY	SKU30
PAGE DETAIL	PS: MSVDD CONTROLLER OVR4i+

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NV_PN	600-1G133-0030-900		
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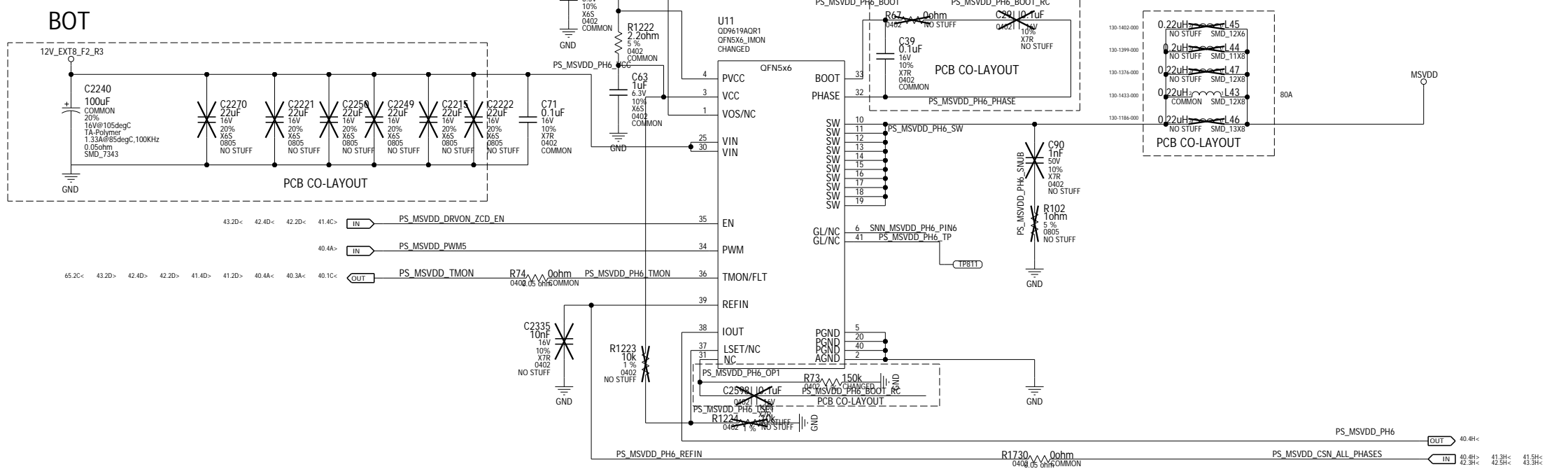
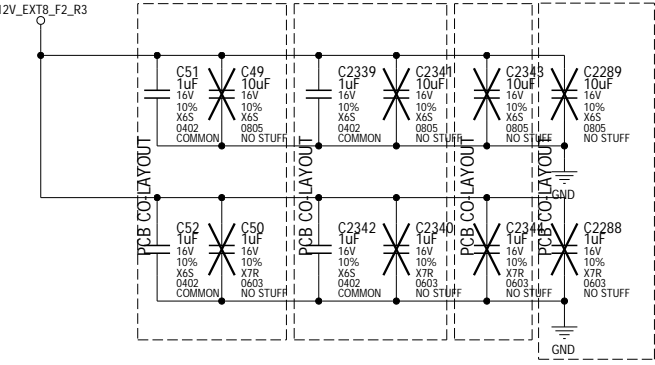
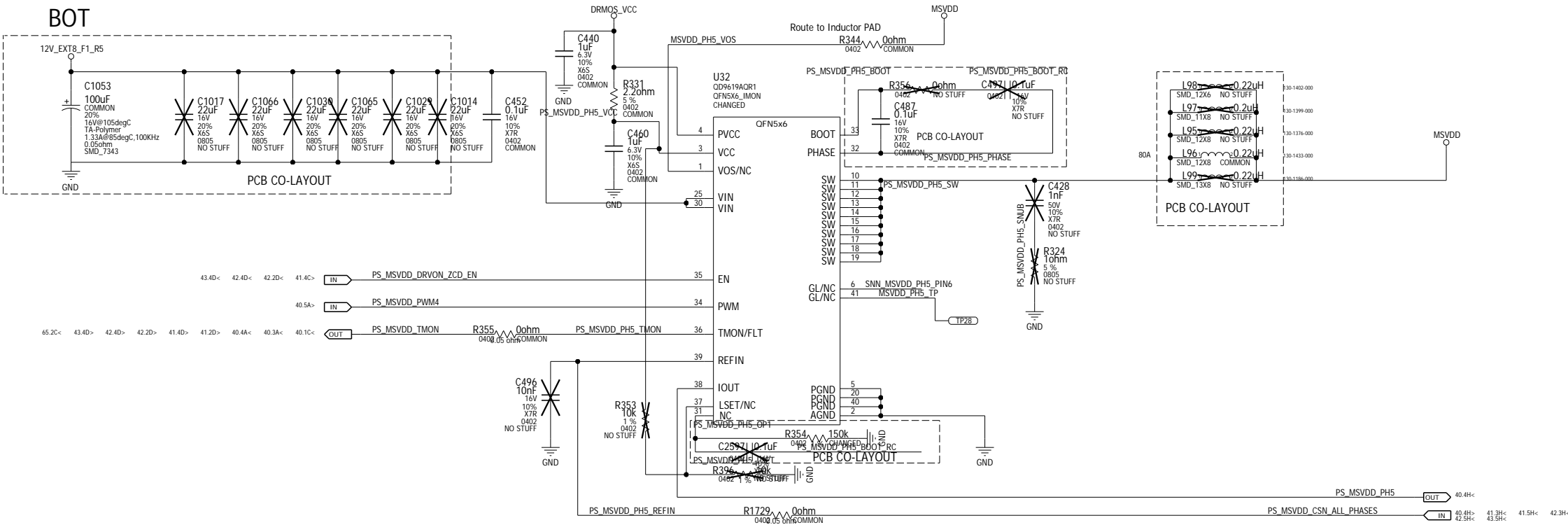
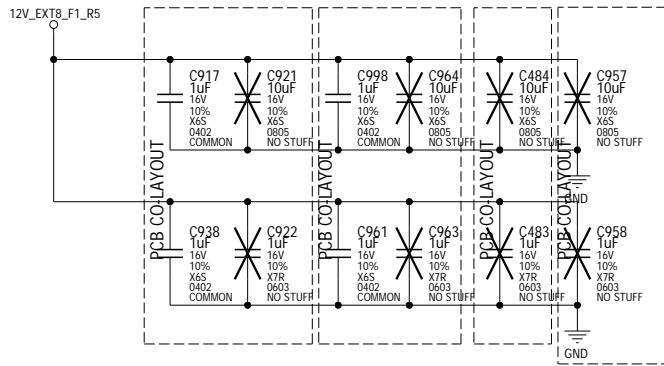




ASSEMBLY	SKU30
PAGE DETAIL	PS: MSVDD PH3 (PWM6) and PH4 (PWM3)

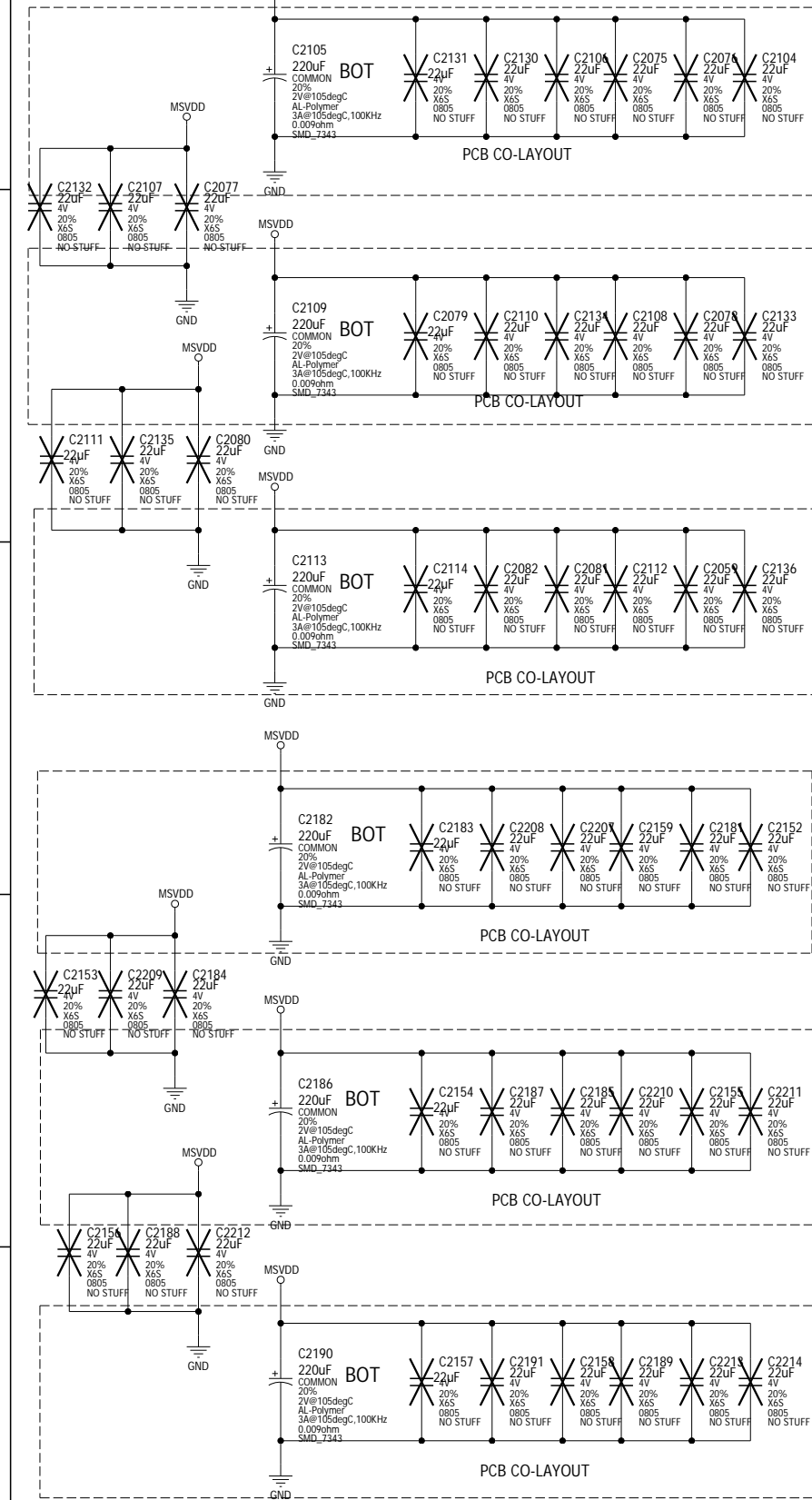
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Page 43: PS:MSVDD PH 5 (PWM4), PH 6 (PWM5)



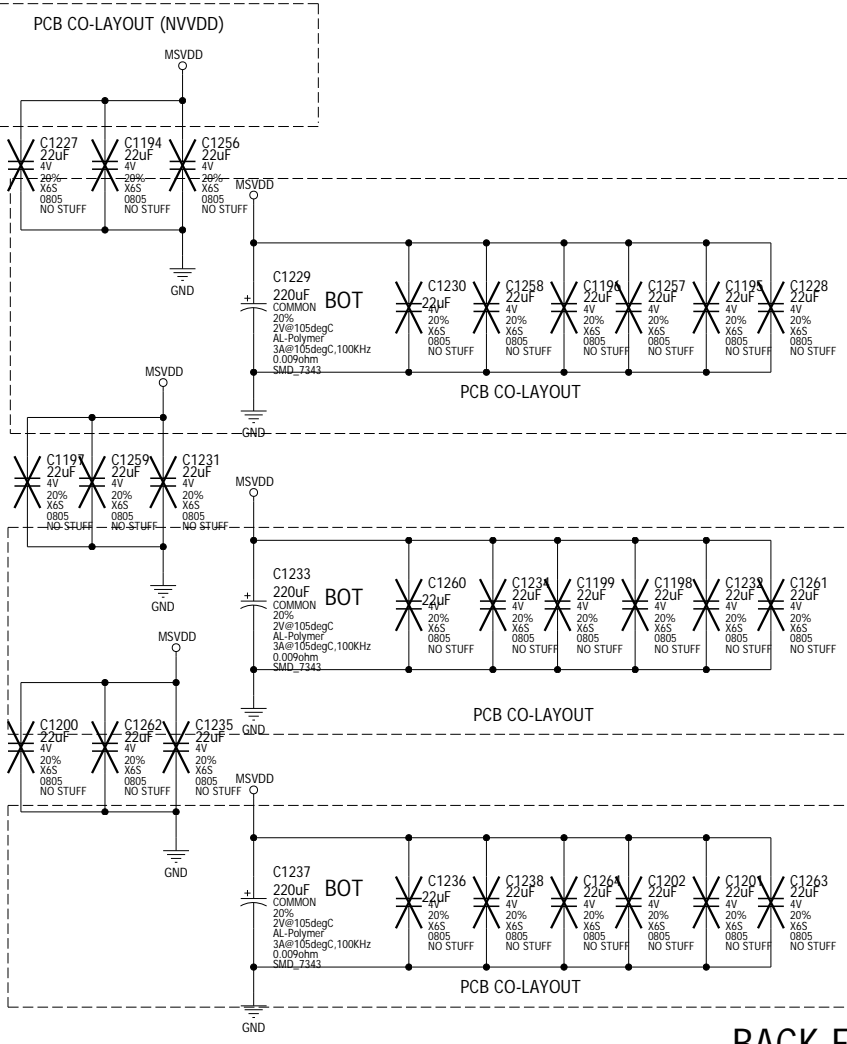
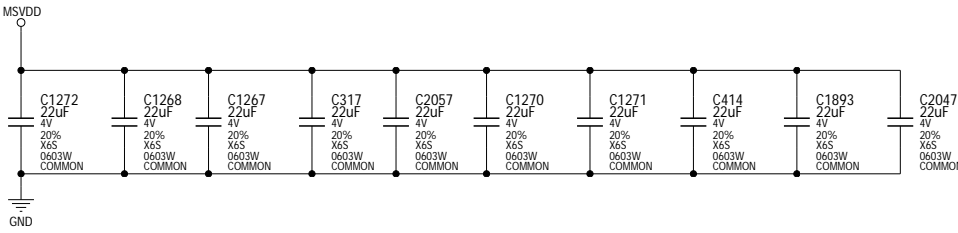
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Page 44: PS: MSVDD OUTPUT CAP
12x SMD7343 330uF CO-LAYOUT WITH 72x 0805 22uF

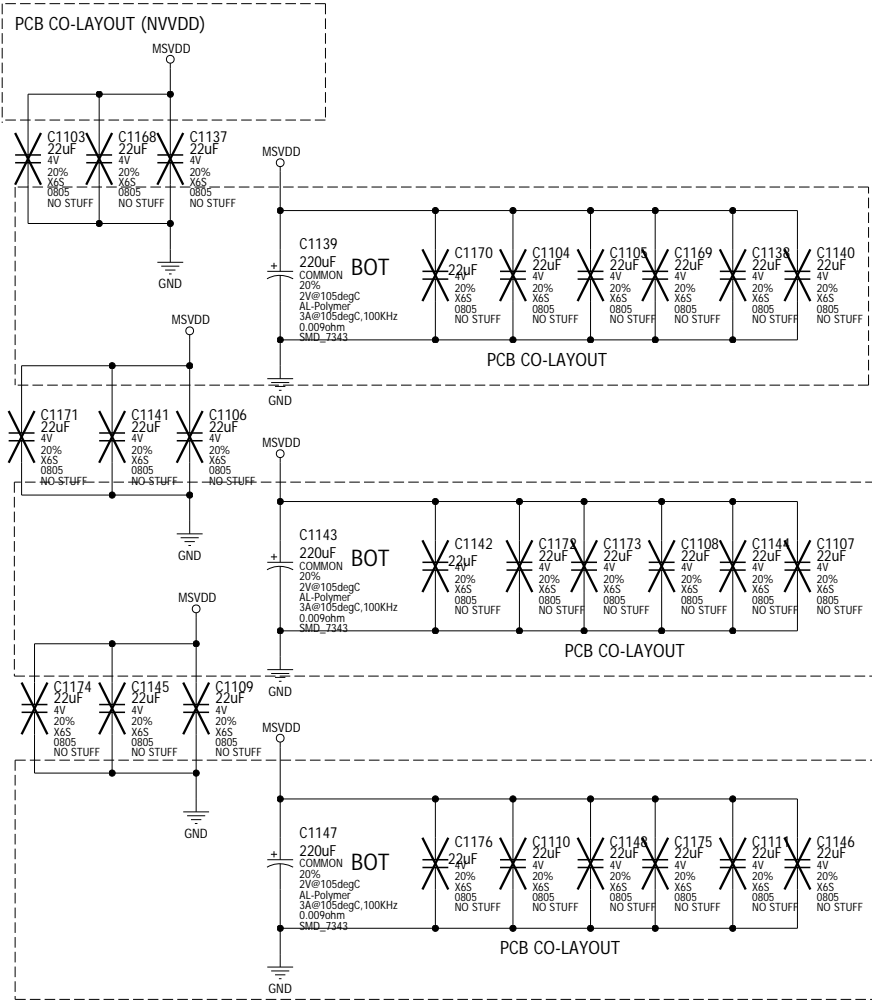
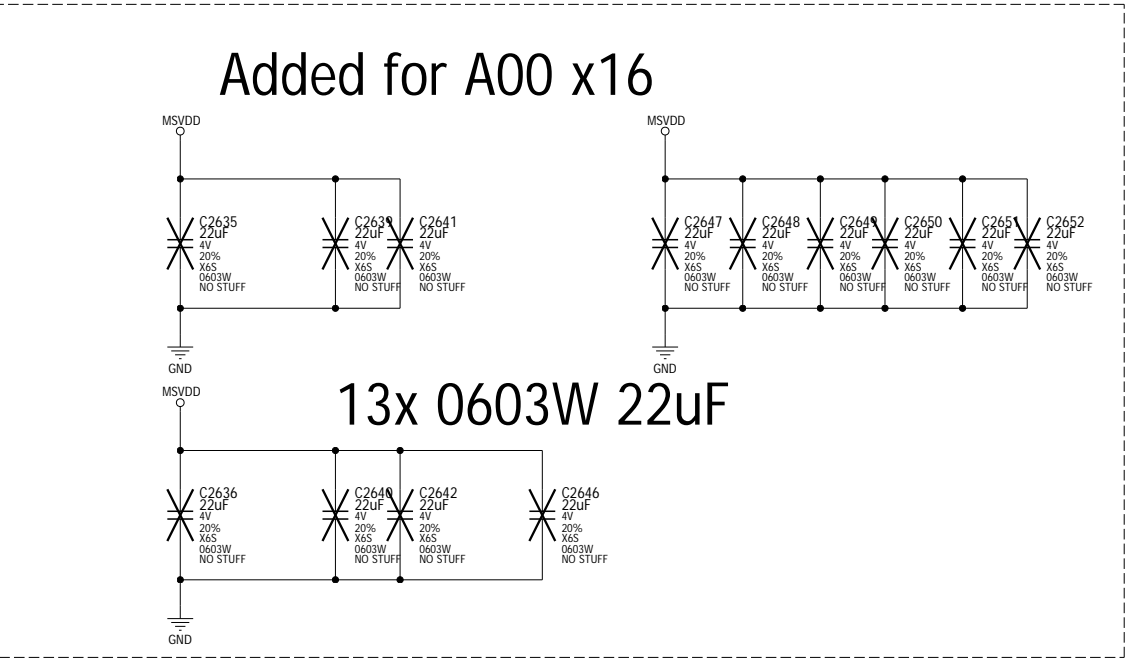


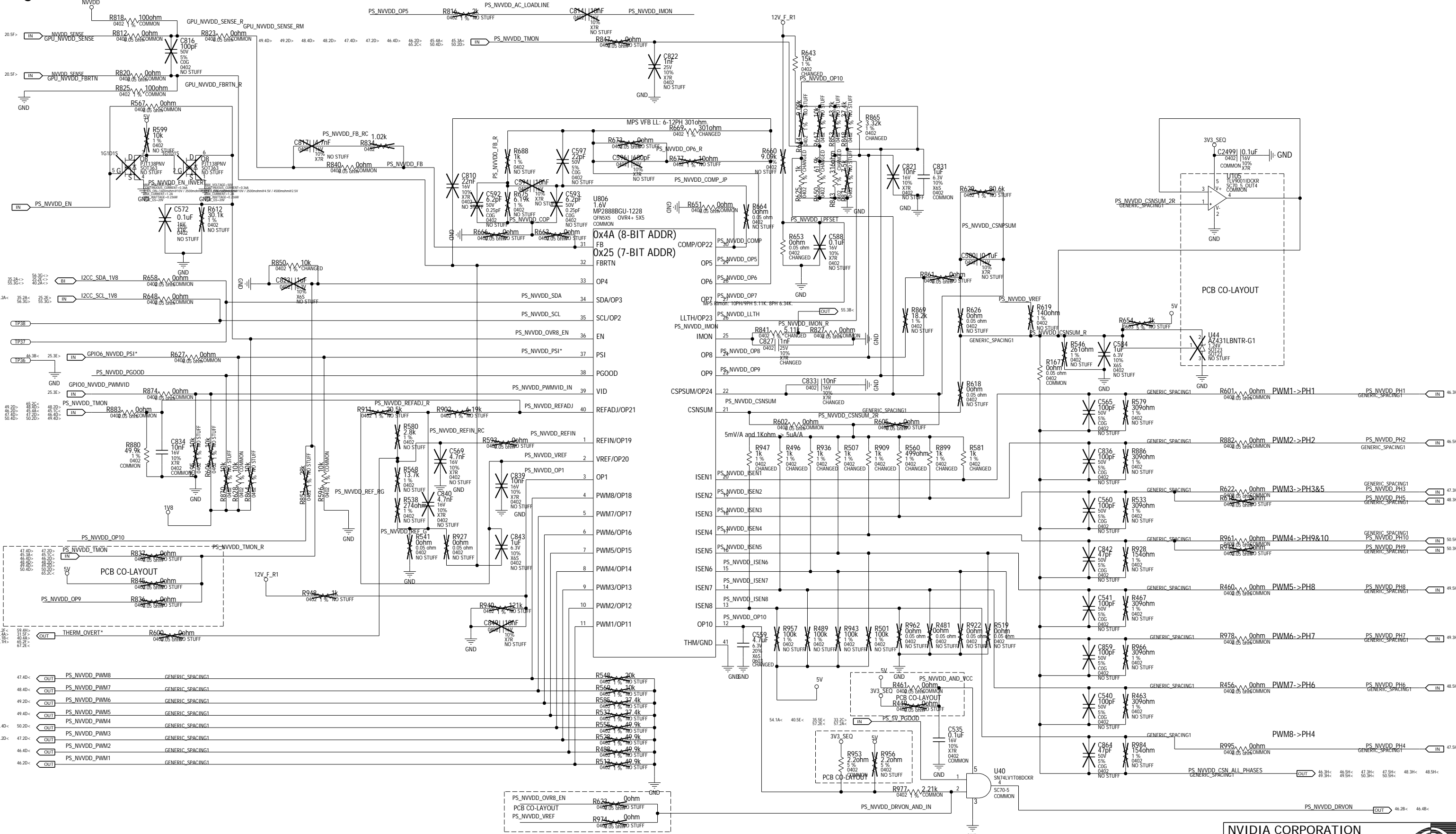
BACK WEST OF PCB

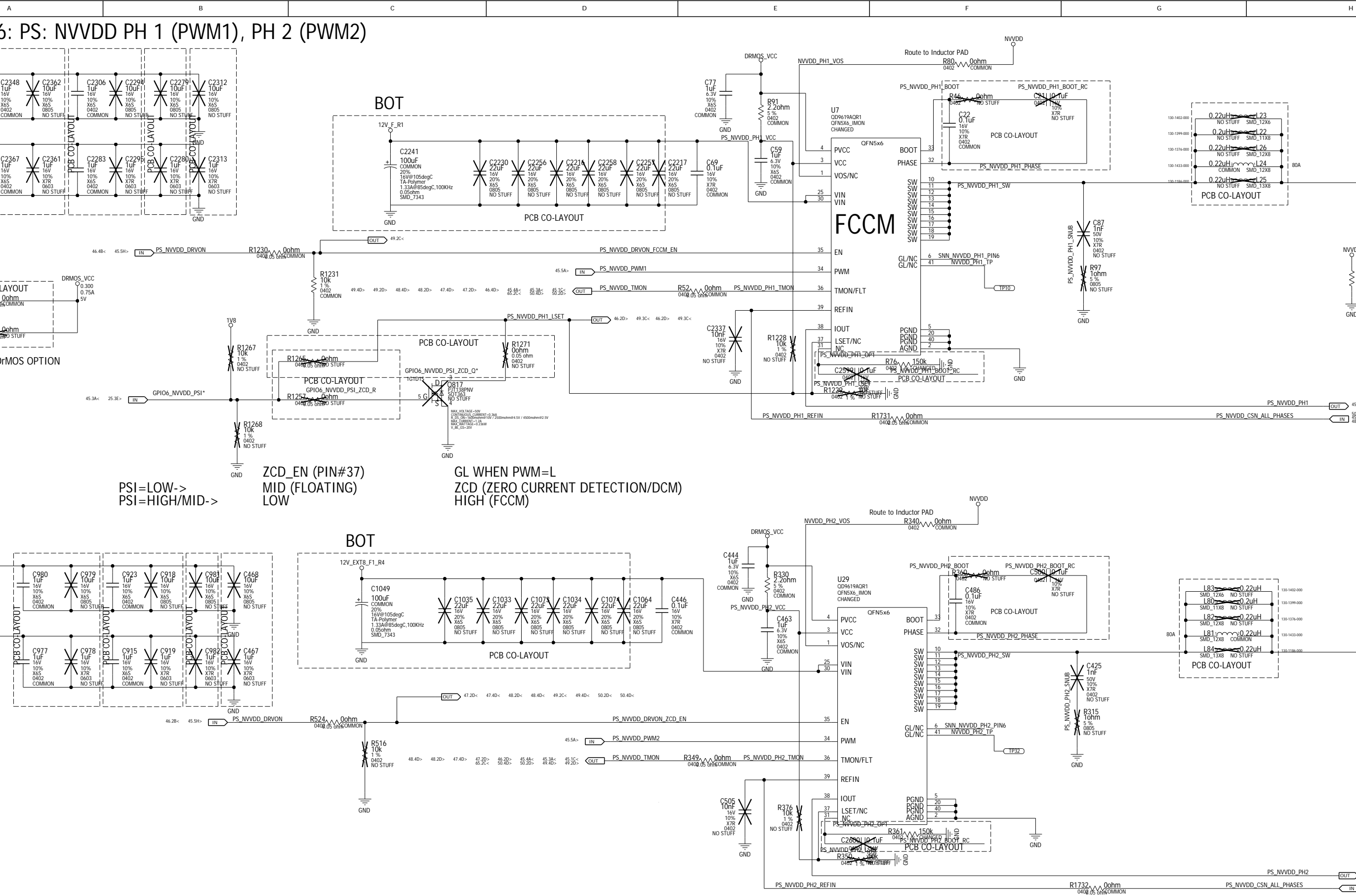
10x 0603W 22uF BETWEEN GPU AND VRM



BACK EAST OF PCB

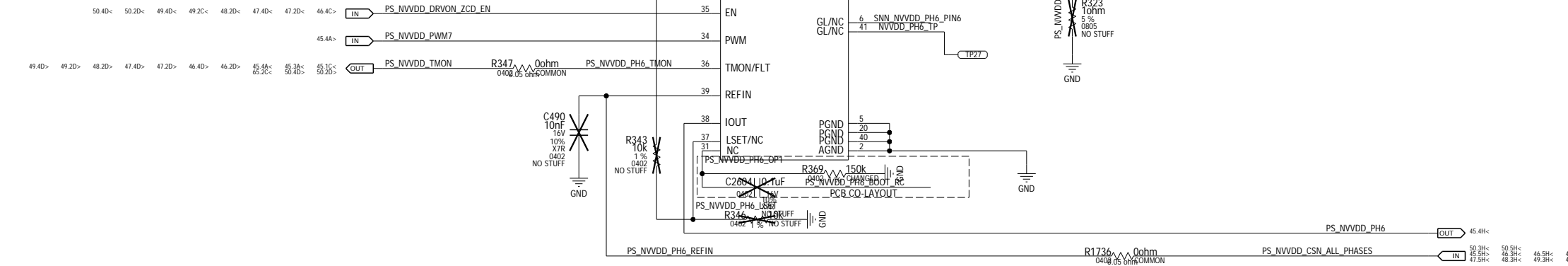
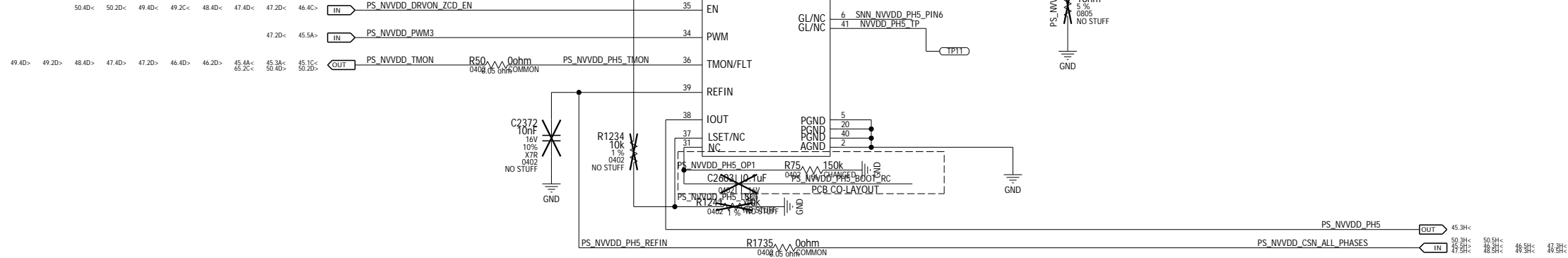
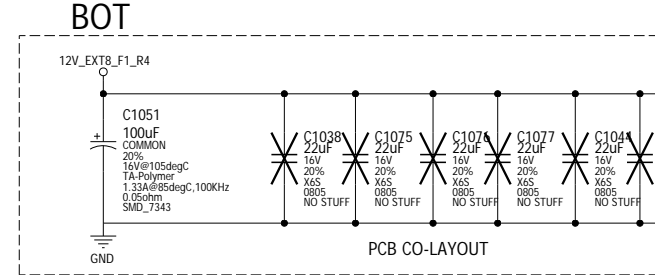
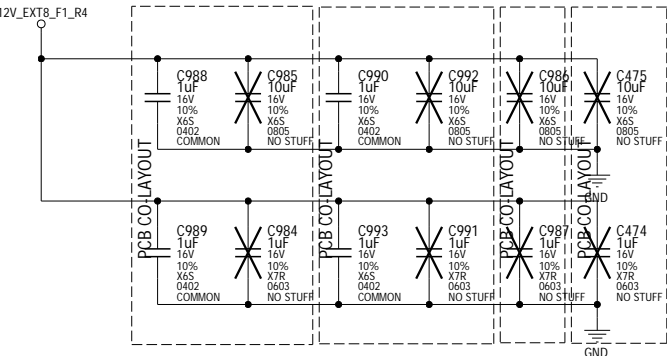
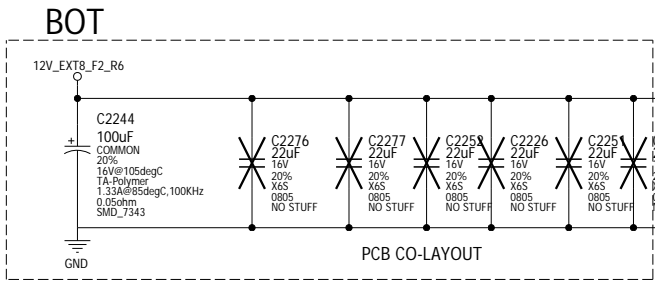
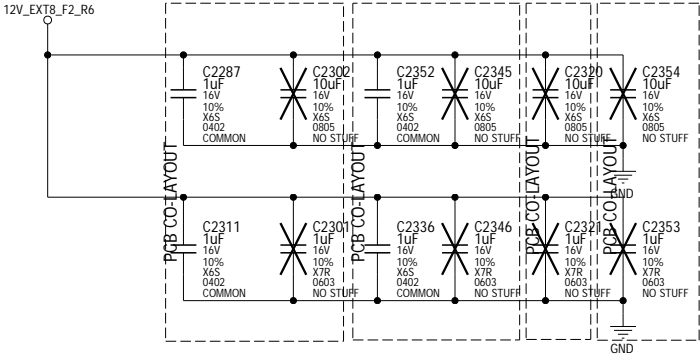






ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH1 (PWM1) and PH2 (PWM2)

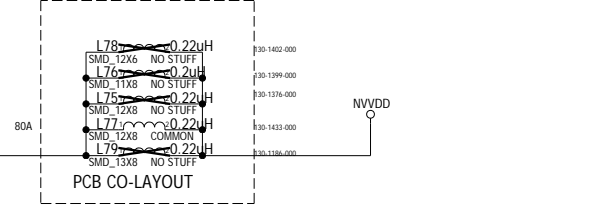
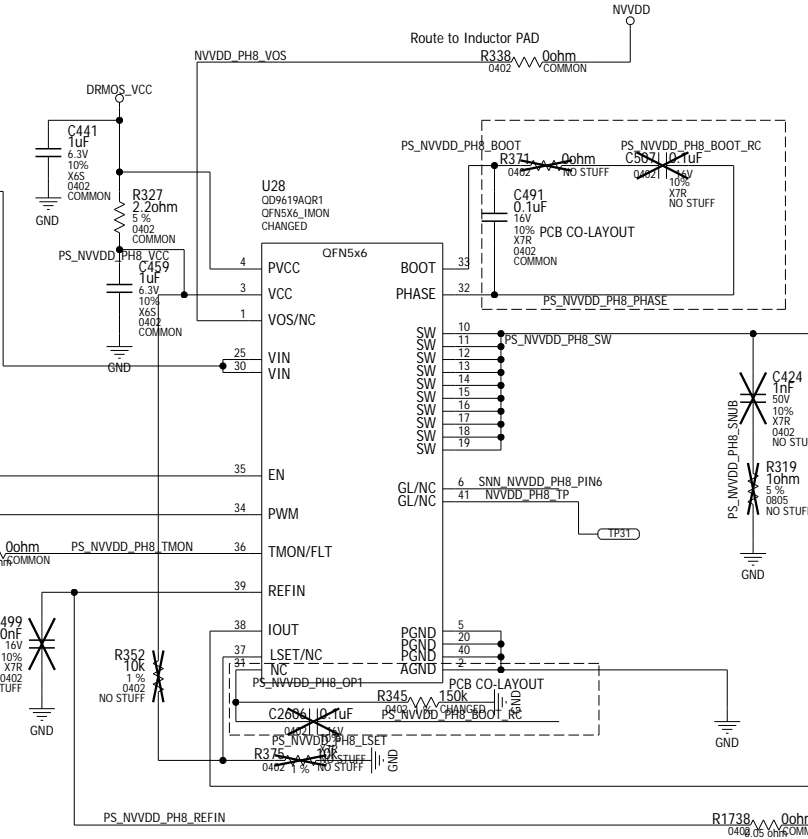
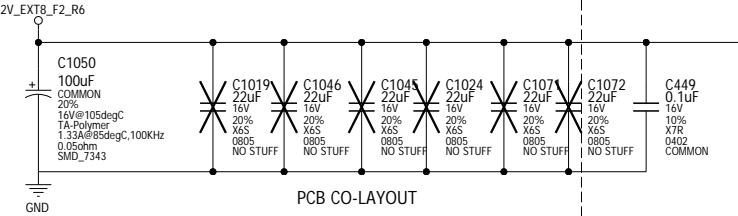
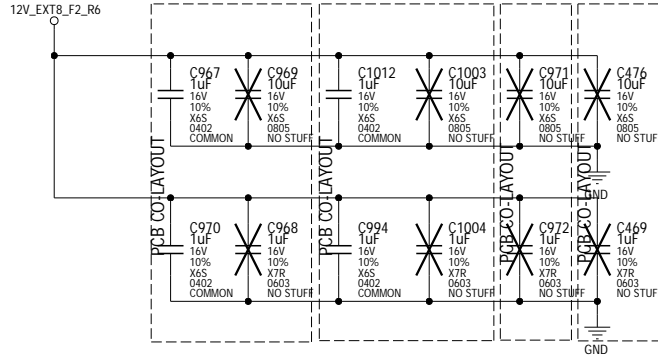
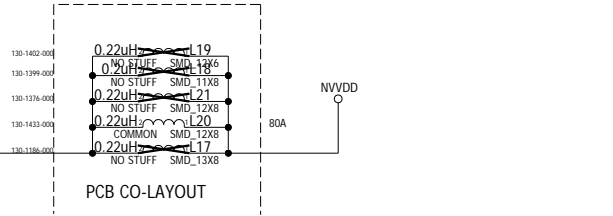
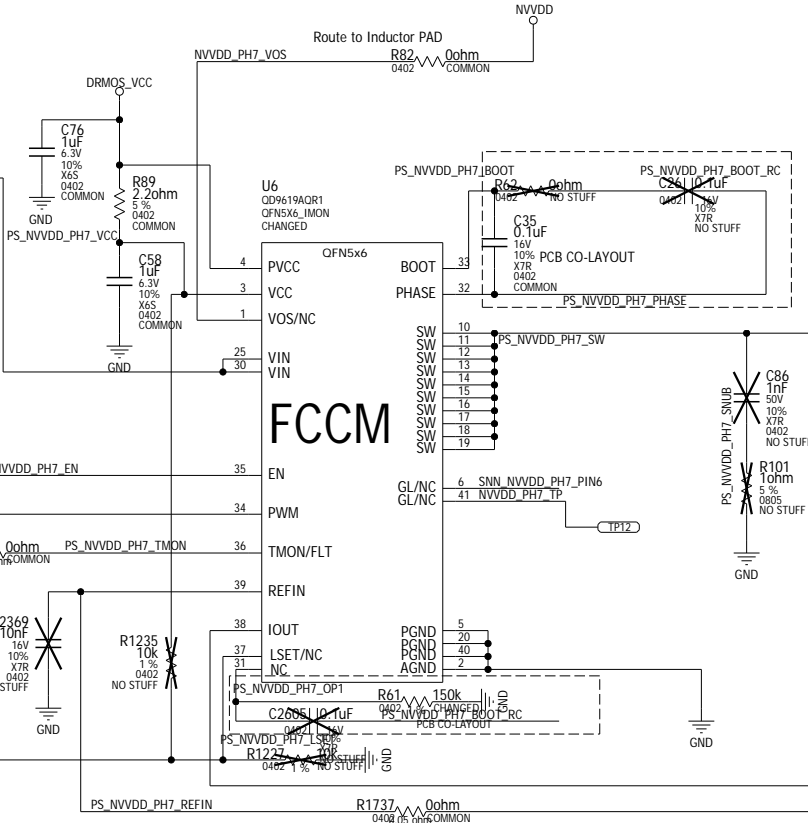
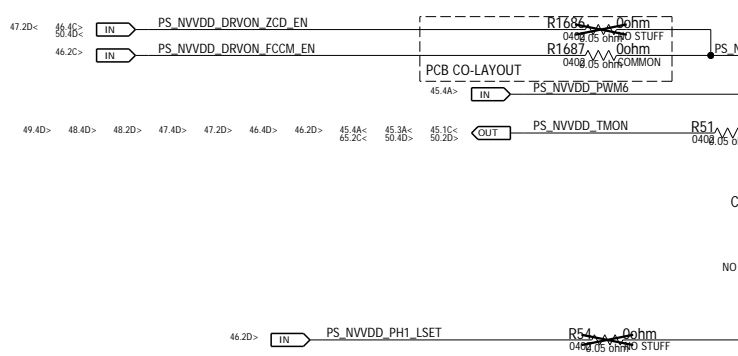
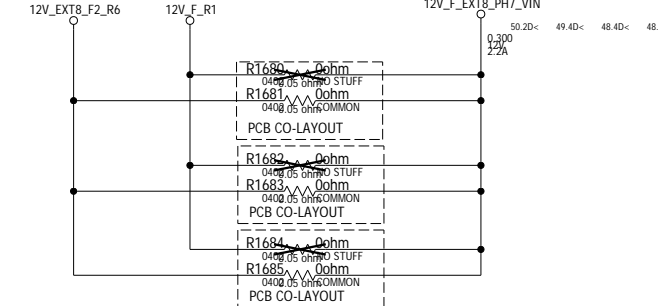
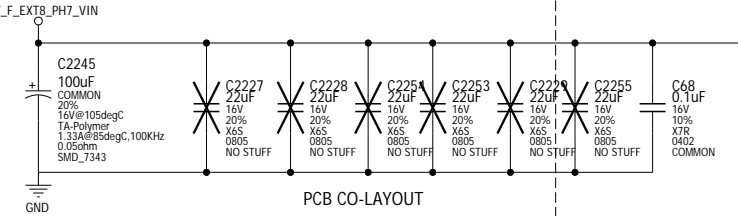
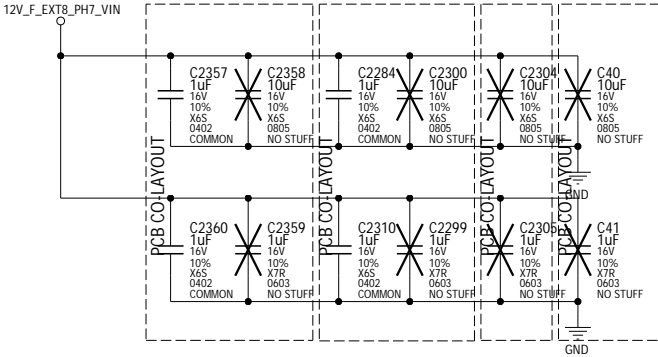
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ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH5 (PWM3) and PH6 (PWM7)

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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Page 49: PS: NVVDD PH 7 (PWM6), PH8 (PWM5)



ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH7 (PWM6) and PH8 (PWM5

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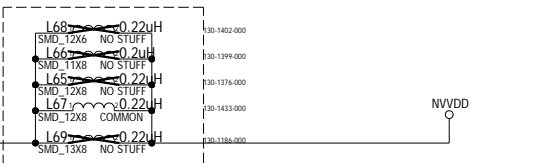
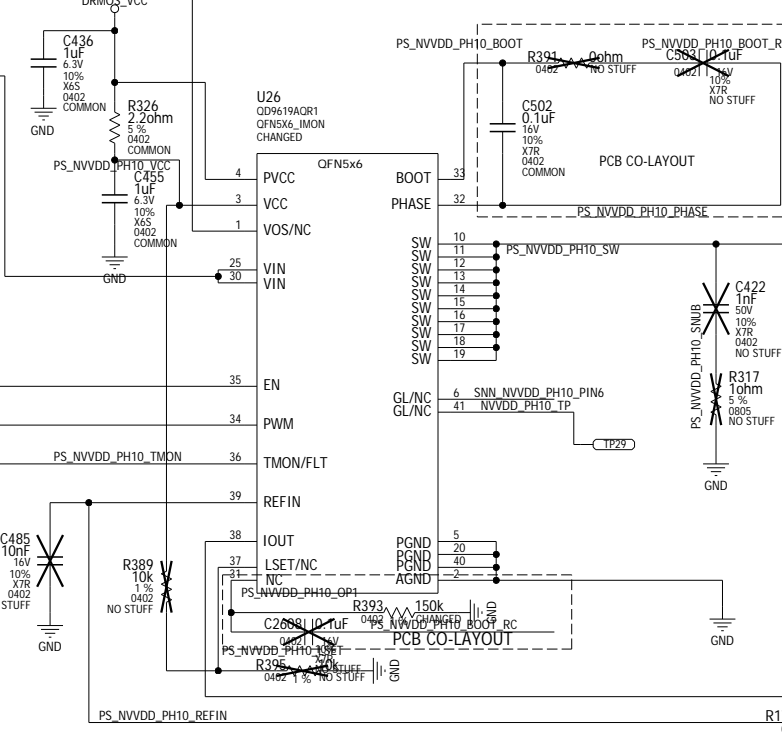
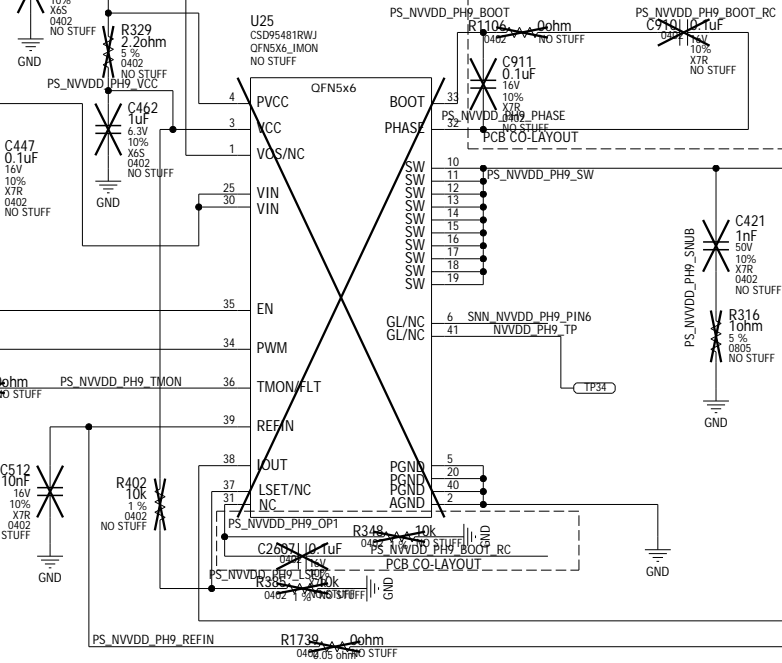
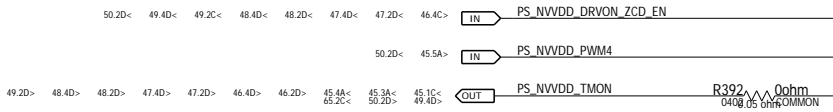
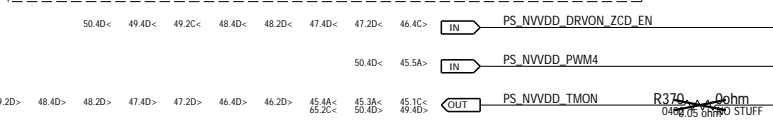
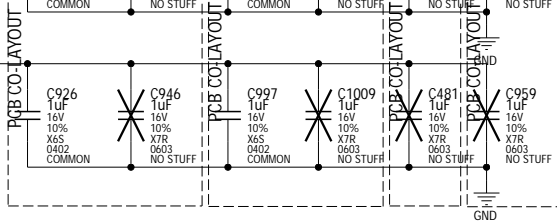
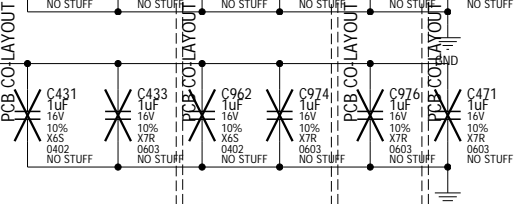
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ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH9 (PWM4), PH10 (PWM4)

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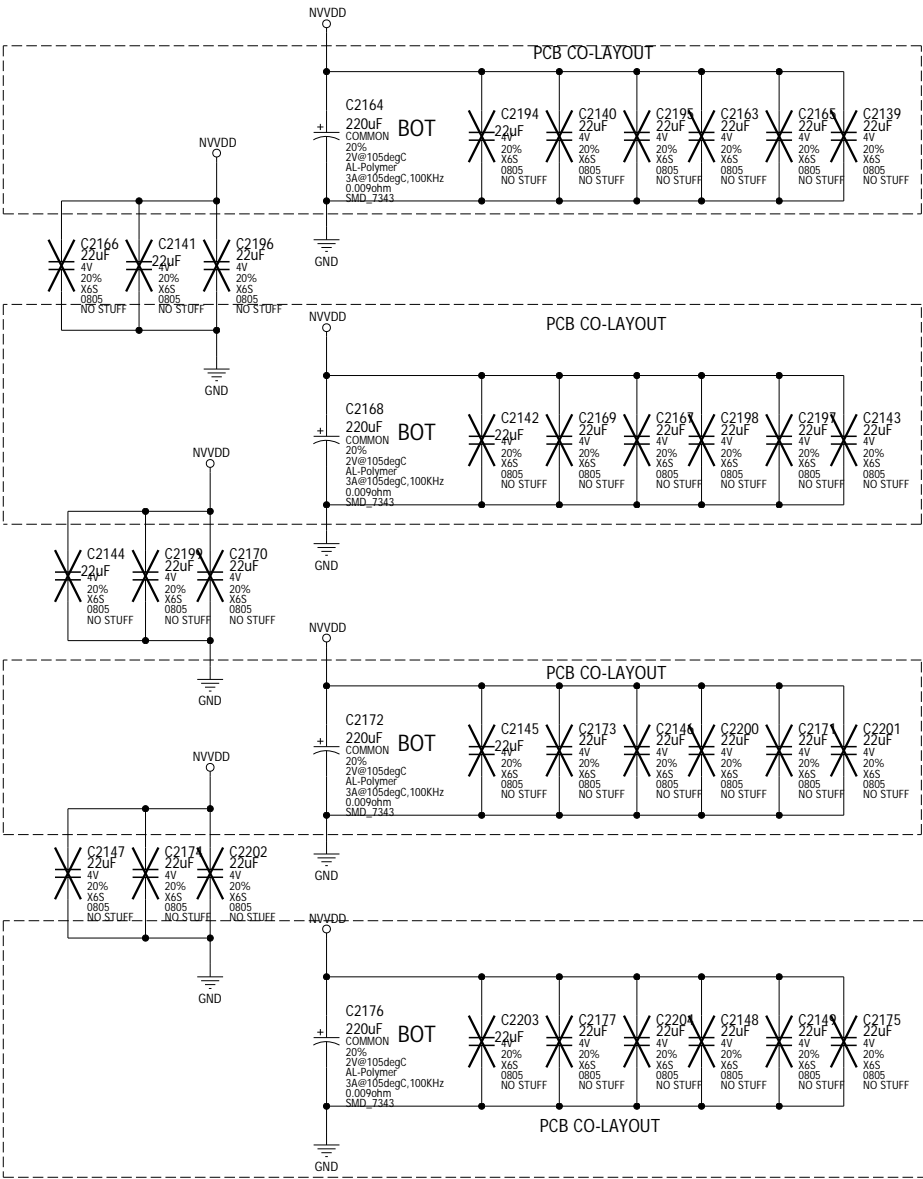


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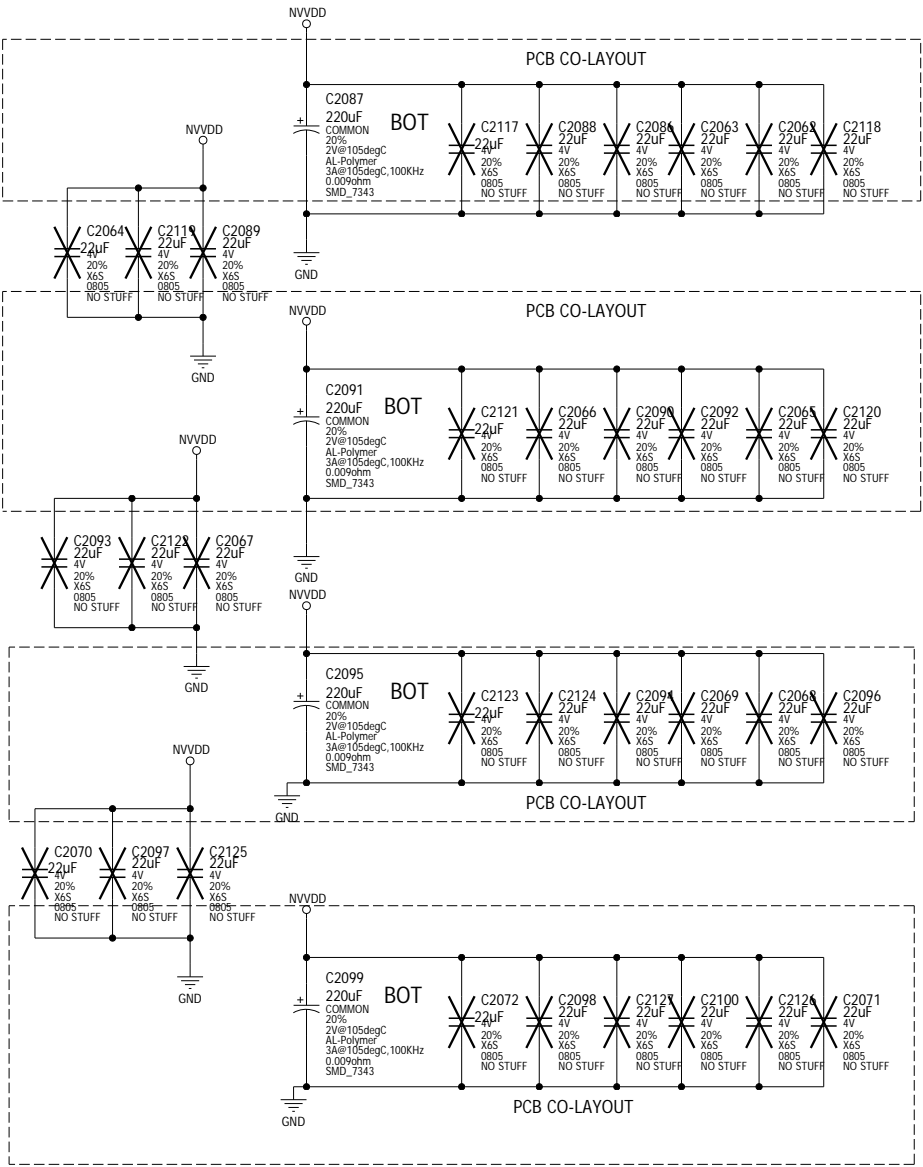
600-1G133-0030-900

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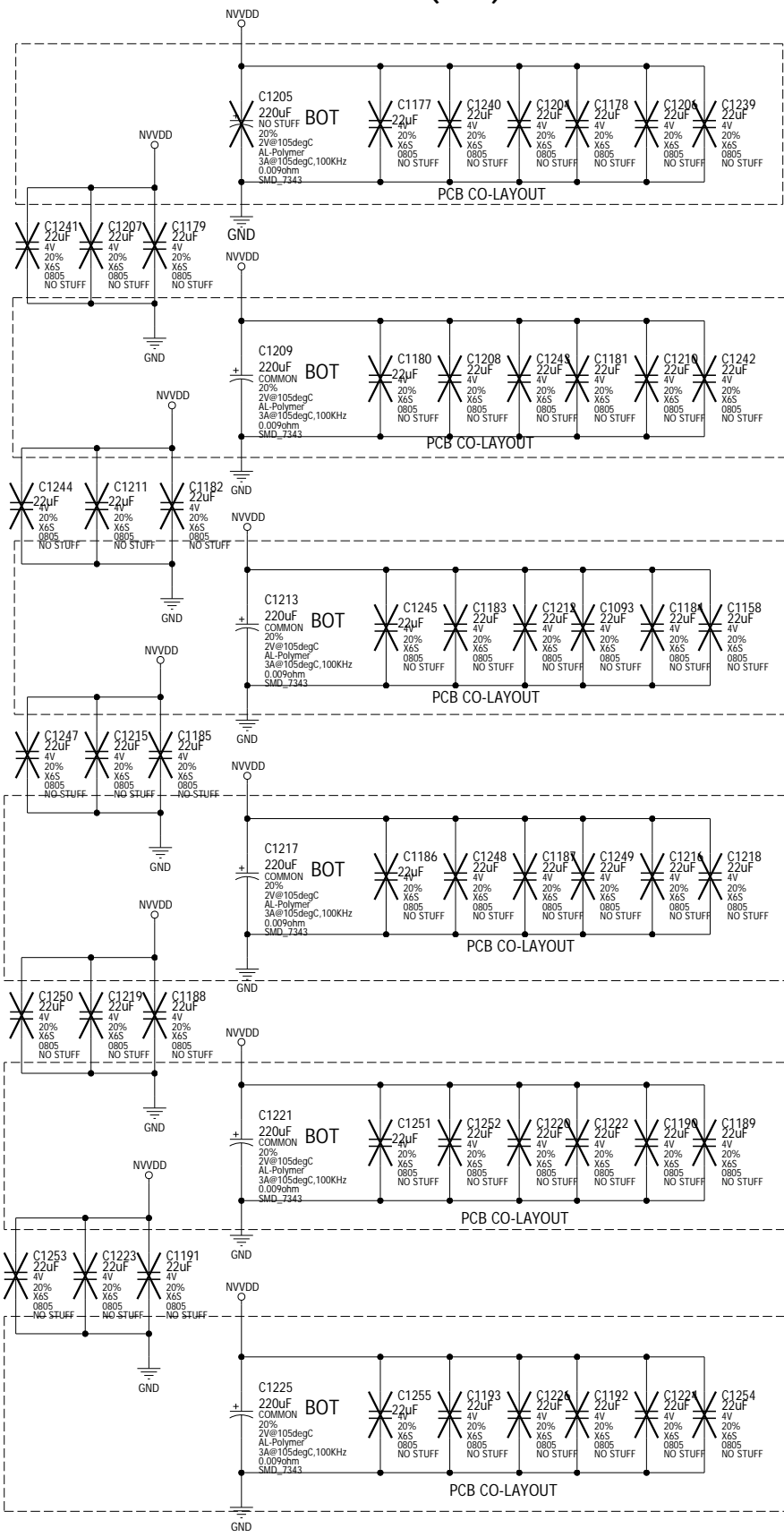
20x SMD7343 220uF CO-LAYOUT WITH 120x 0805 22uF



BACK WEST OF PCB

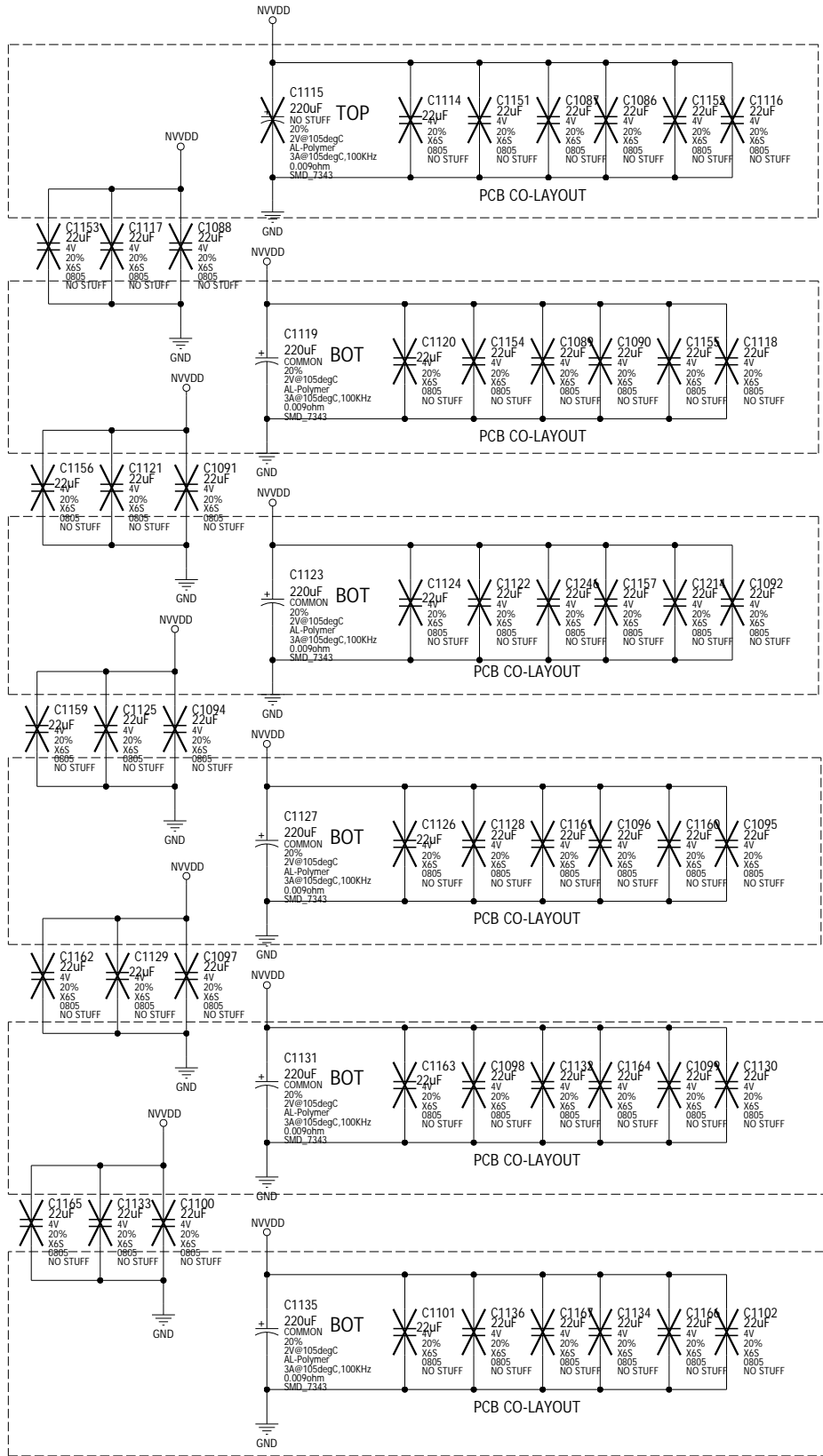
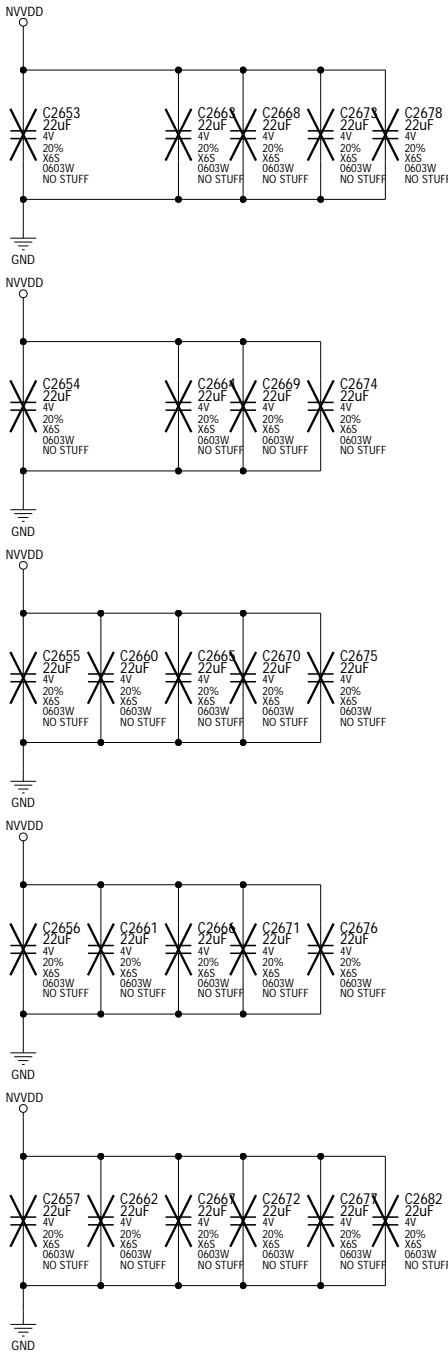


BACK WEST OF PCB



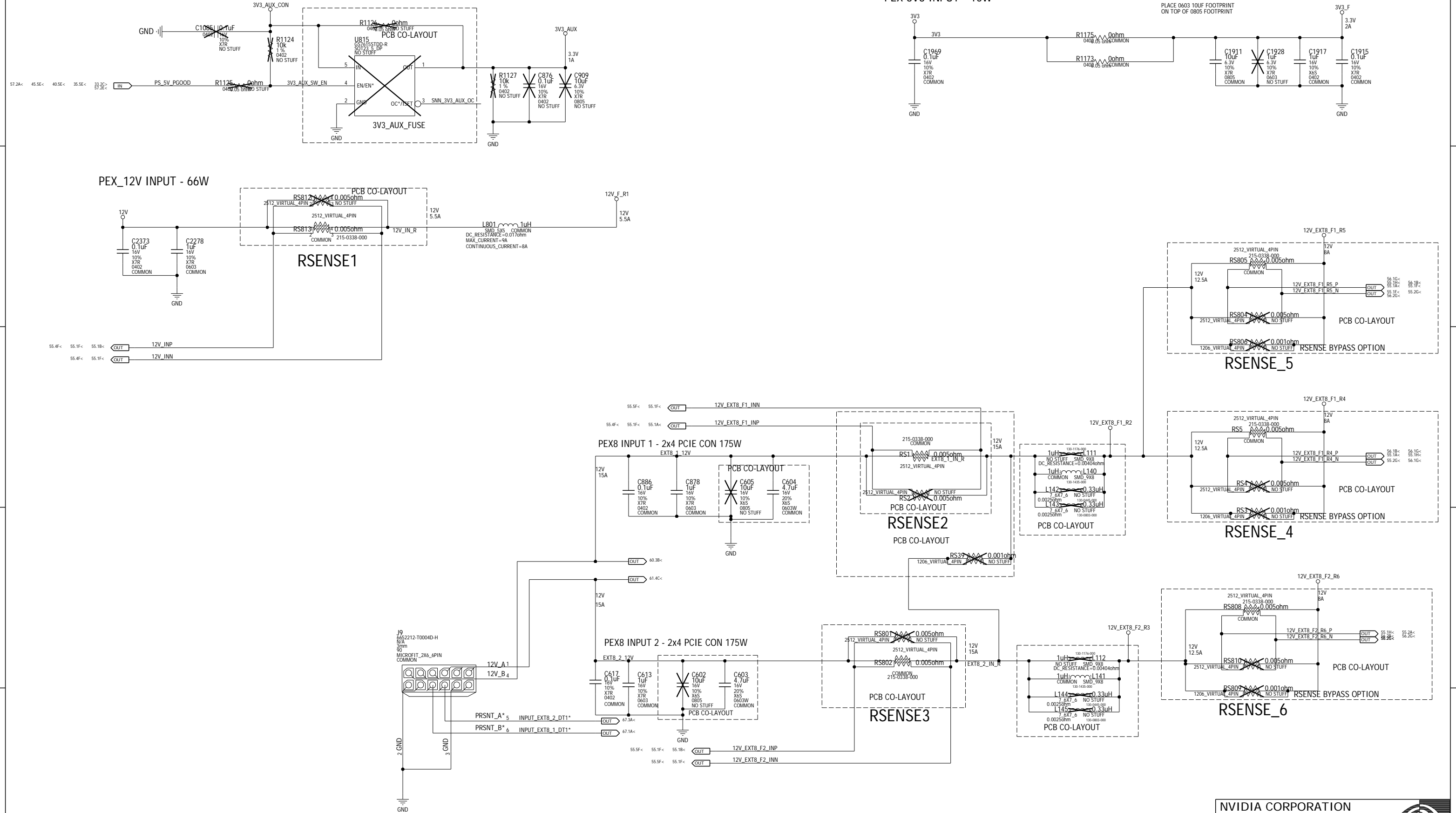
BACK EAST OF PCB

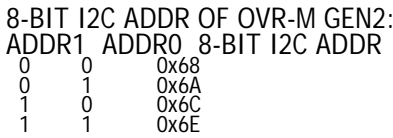
Added for A00 x16
25x 0603W 22uF



BACK EAST OF PCB

Page 54: PS: INPUTS, FILTERING, MONITORING





OVR-M GEN2 SUPPORT

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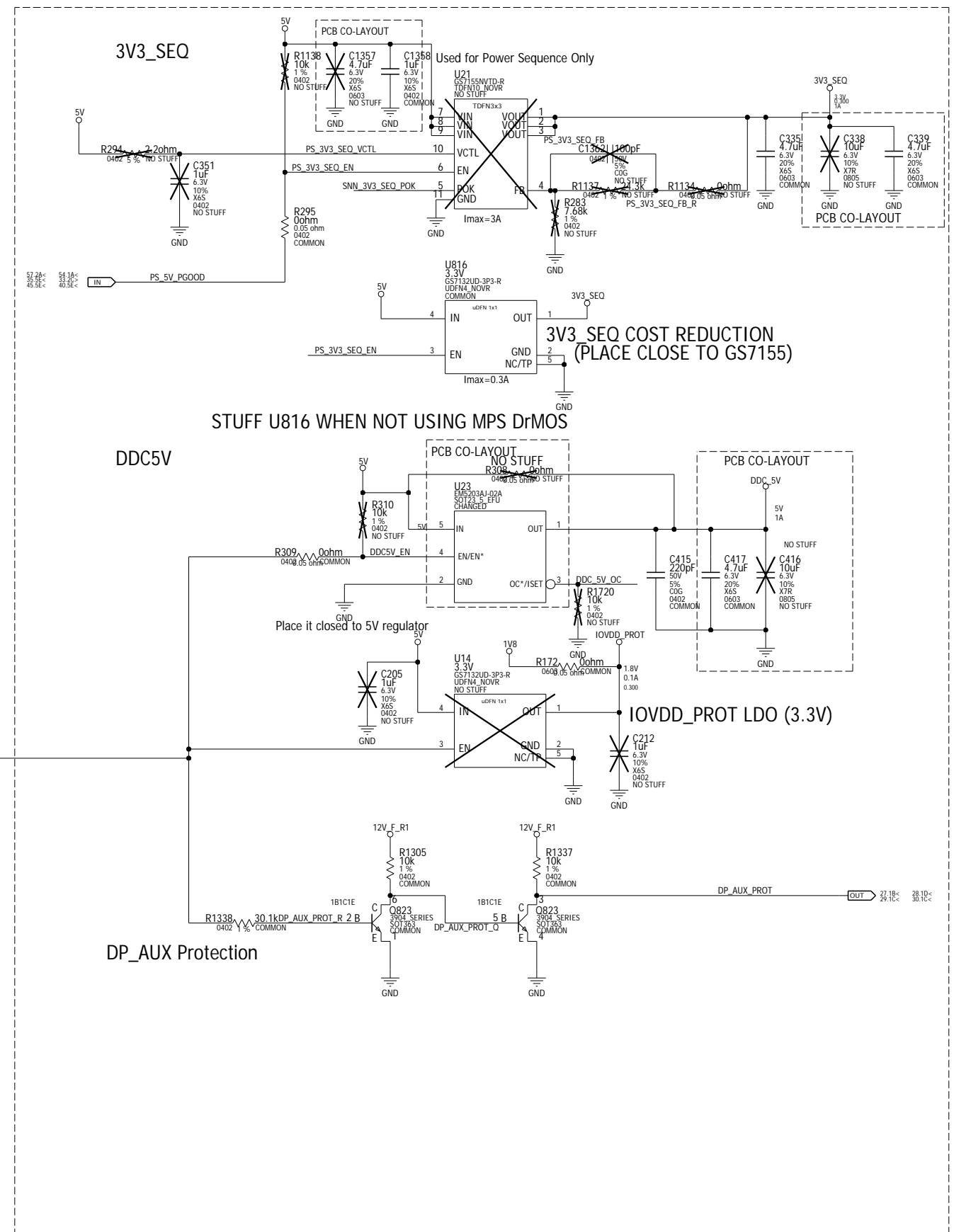
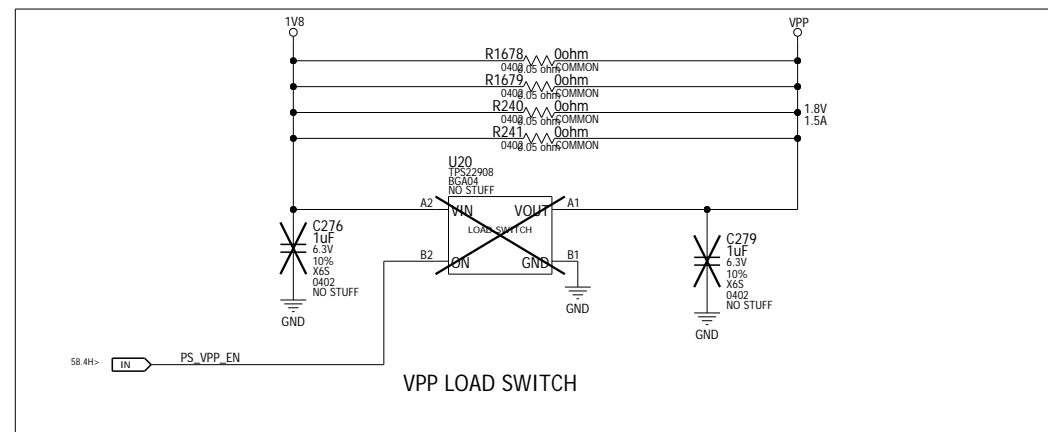
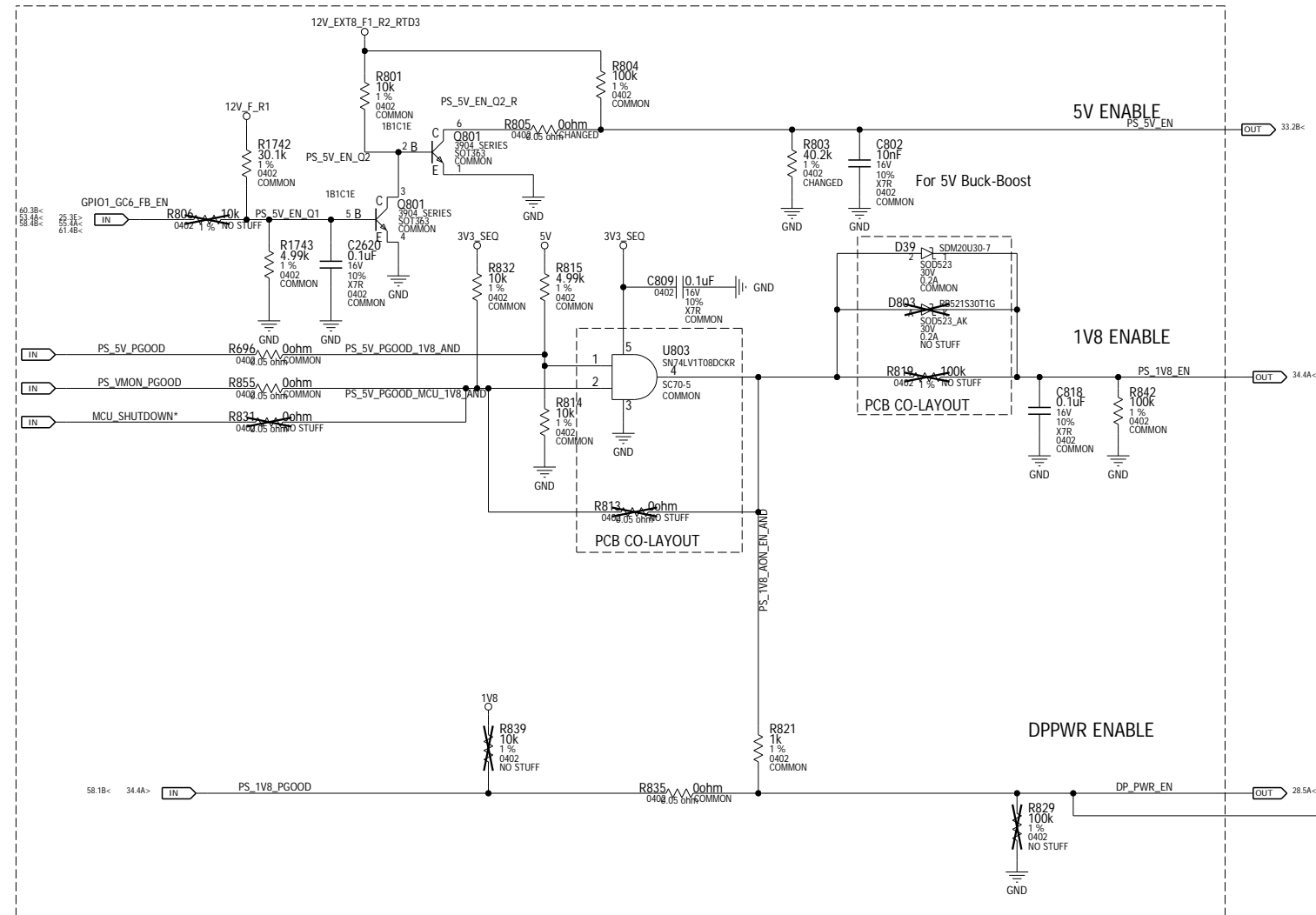
PCB REV	PG133-A03	PAGE	55 OF 67
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2

4

5

OVR-M can support 1.8V signaling without issues



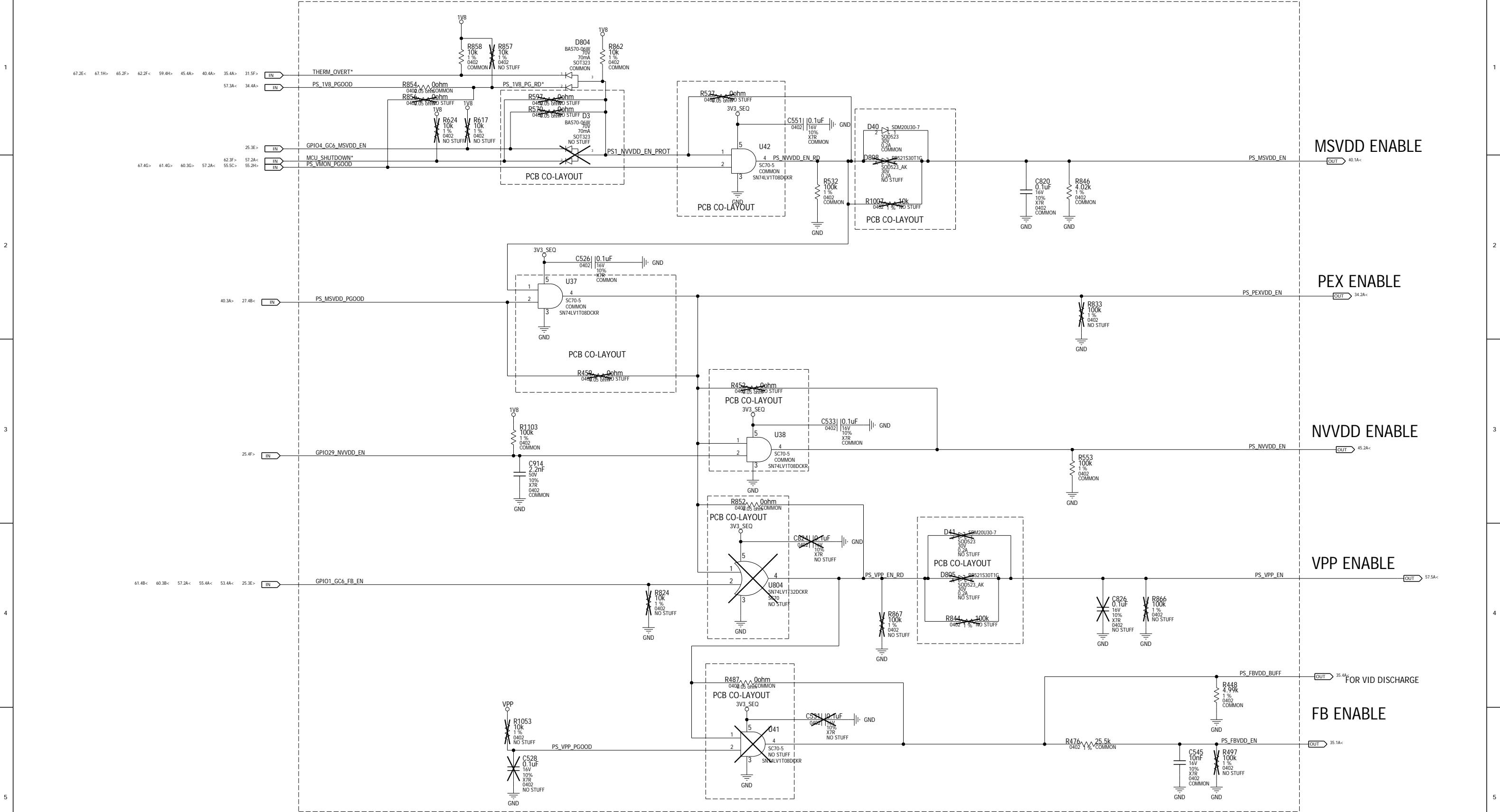
ASSEMBLY	SKU30
PAGE DETAIL	SEQ: 5V/1V8 EN & VPP LOAD SW

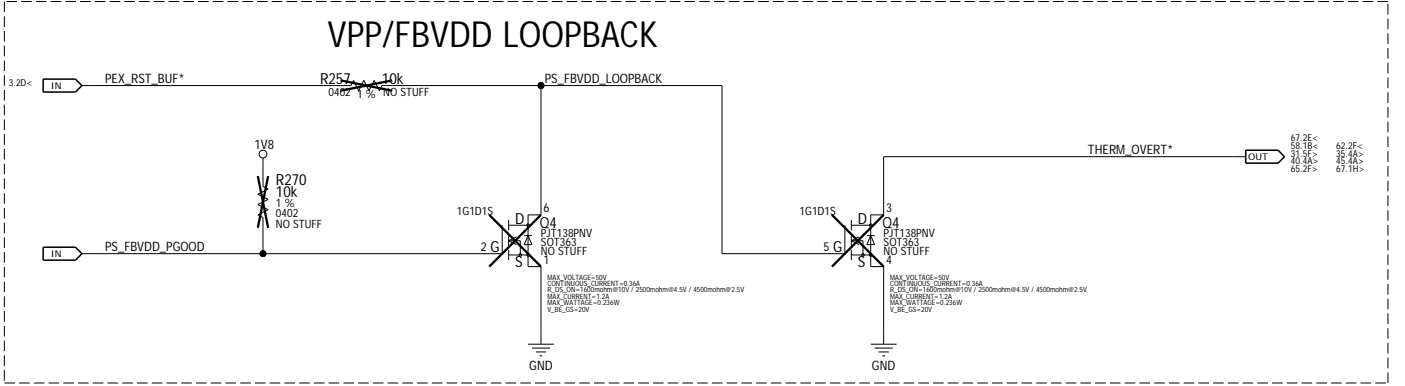
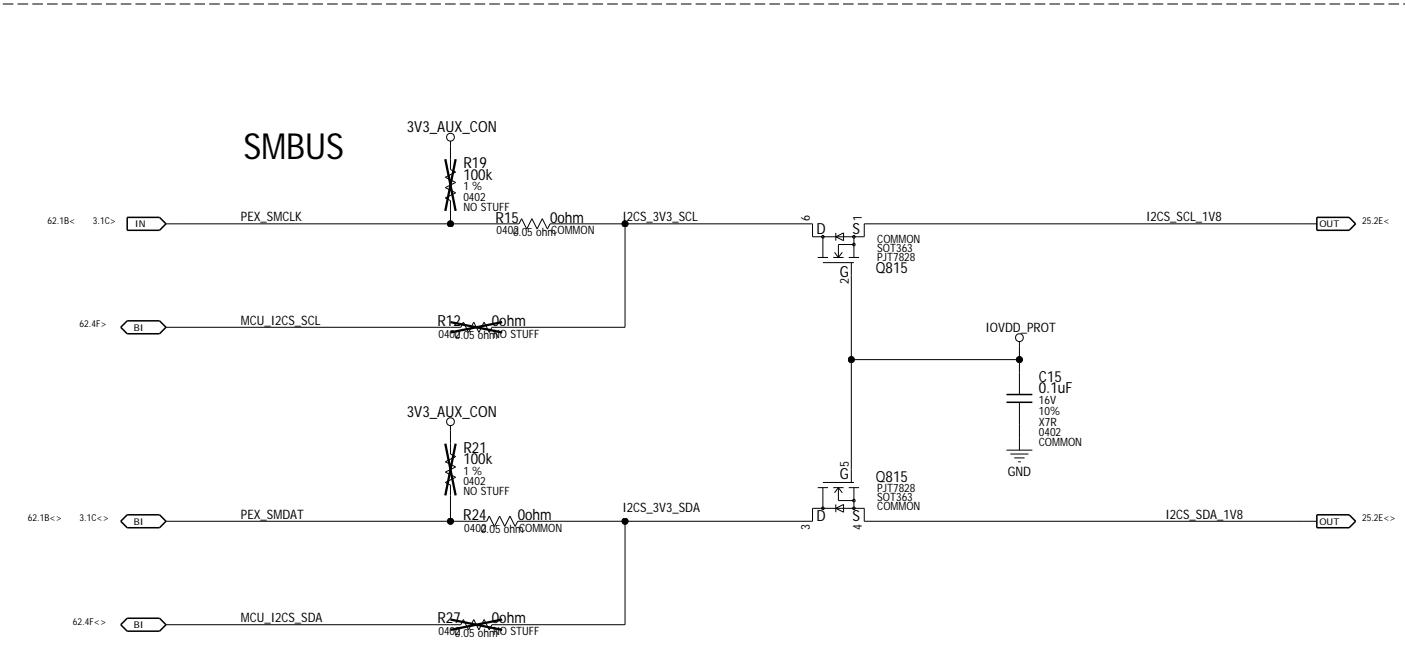
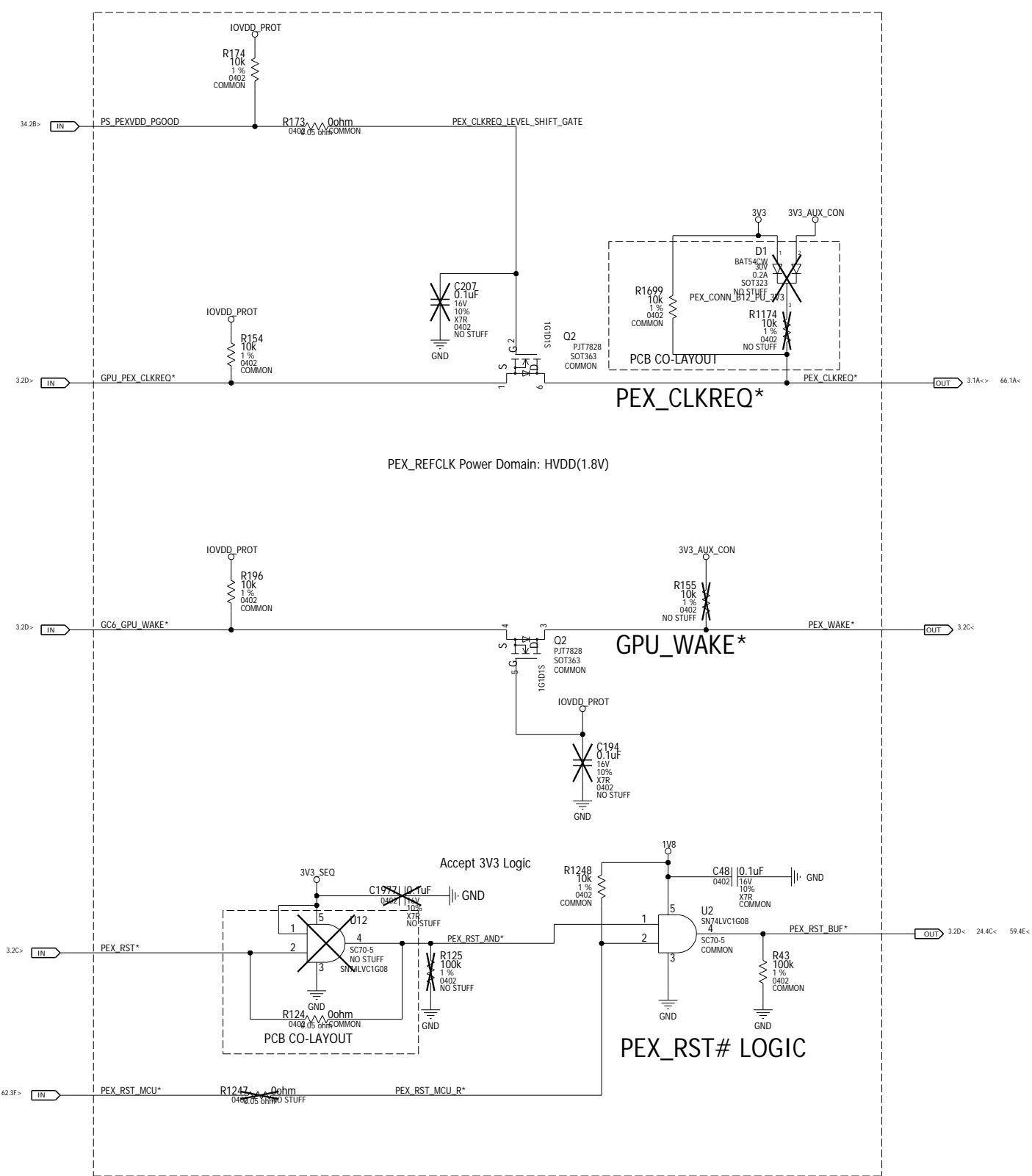
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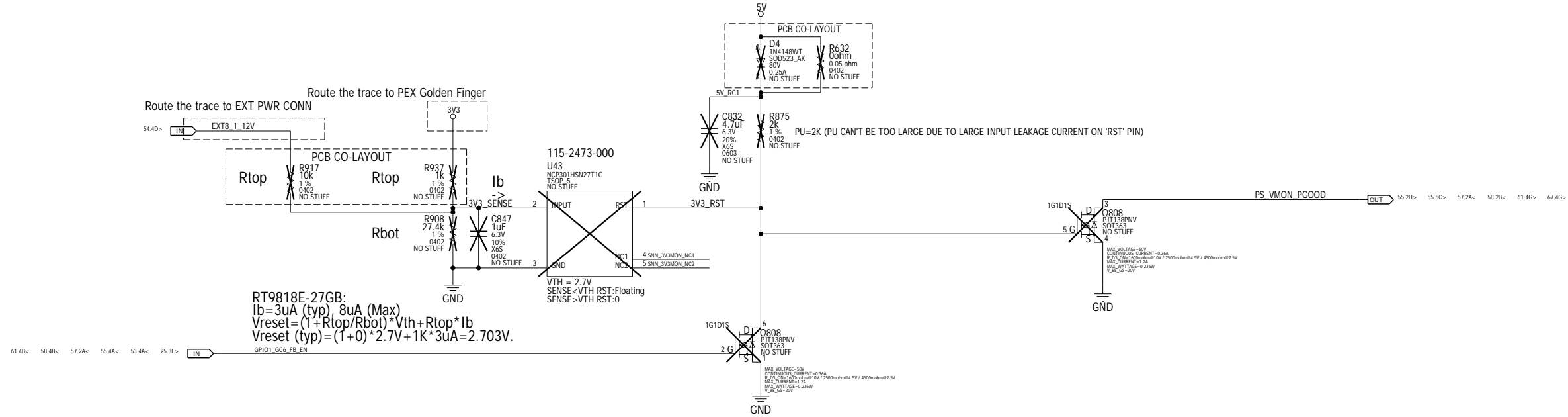




PEX3V3 or EXT8-1-12V Monitor

$V_{th}=2.7V$ (+/- 0.0405V/1.5%). $V_{phys}(Typ)=0.01 \cdot V_{th}$, $V_{phys}(Max)=0.016 \cdot V_{th}$

- 1) Suppose that at $t=0s$, V_{in} is greater than $(2.7V + V_{hys})$, $V_{reset}=LOW$. After V_{in} decreases to $2.7V (+/- 0.0405V)$, $V_{reset}=floating$.
- 2) Suppose that at $t=0s$, V_{in} is smaller than $(2.7V)$, $V_{reset}=floating$. After V_{in} increases to $[2.7V (+/- 0.0405V) + V_{hys}]$, $V_{reset}=LOW$.



ASSEMBLY	SKU30
PAGE DETAIL	SEQ: 3V3_PEX VOLTAGE MONITOR

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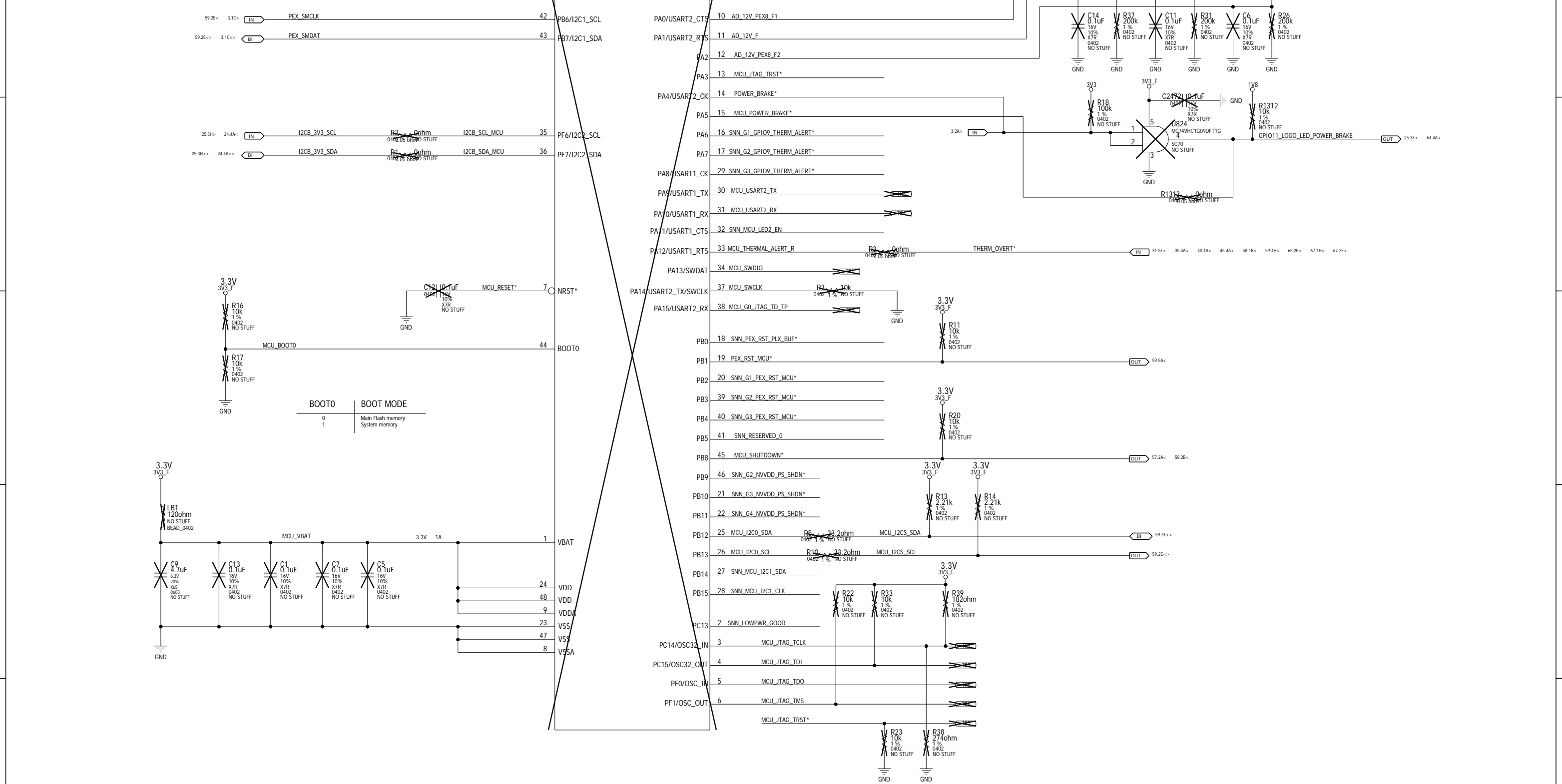
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2-PIN LED HEADER FOR NORTH LOGO LED (WHITE)

White LED: Preliminary Vf = 2.7V-3.3V @ 20mA

NORTH LOGO LED (WHITE)

GPIO35_NORTH_LOGO_LED_DRIVE

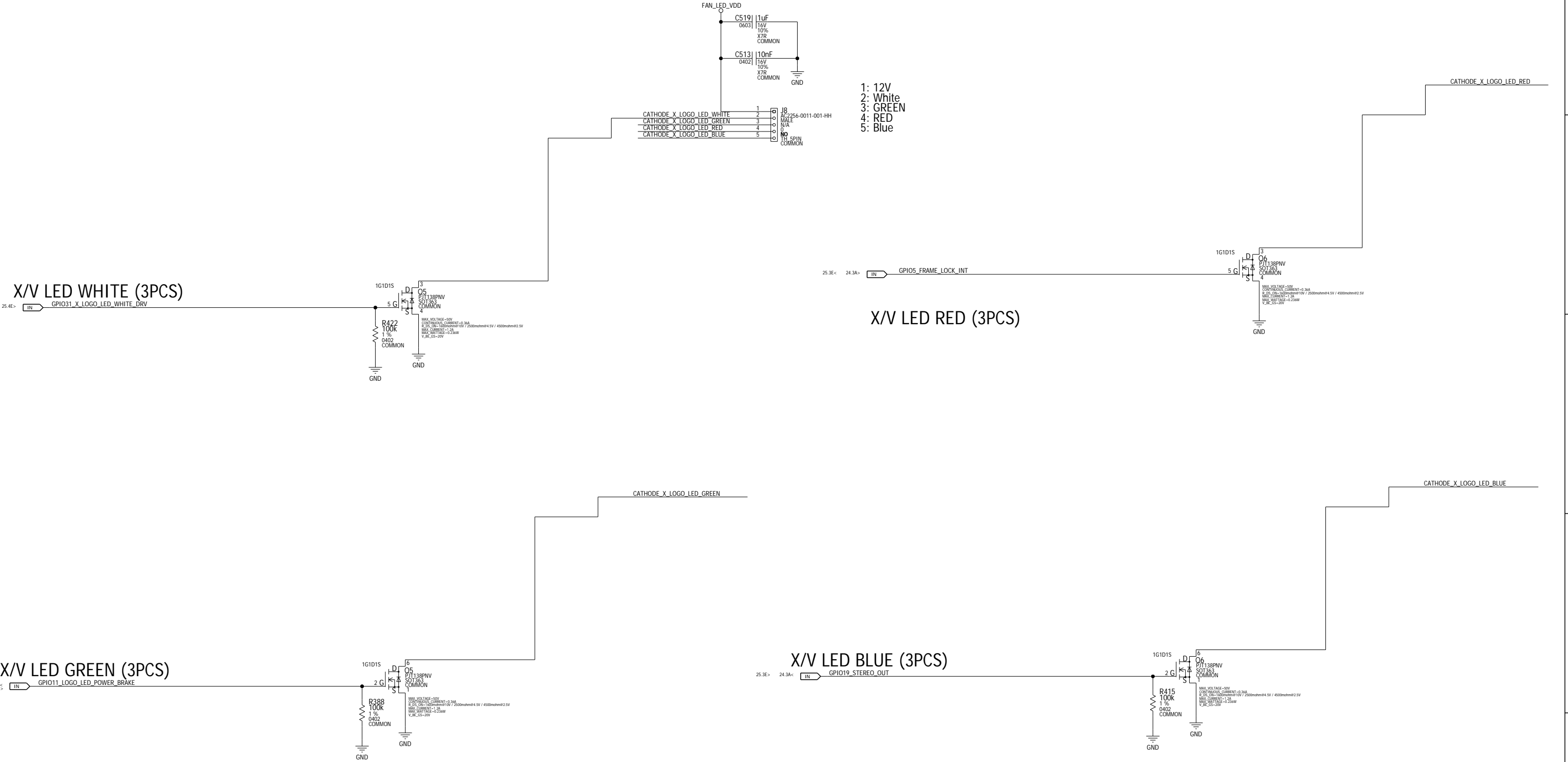
PCB CO-LAYOUT

DUAL FAN 6-PIN FFC HEADERS W/ 0.5MM PITCH

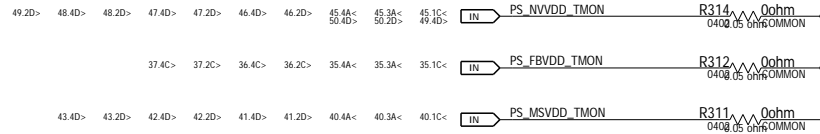
FAN B (RIGHT)

FAN A (LEFT)

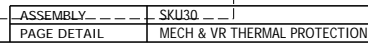
5-PIN POGO-PIN HEADERS FOR 'X/V' LEDS




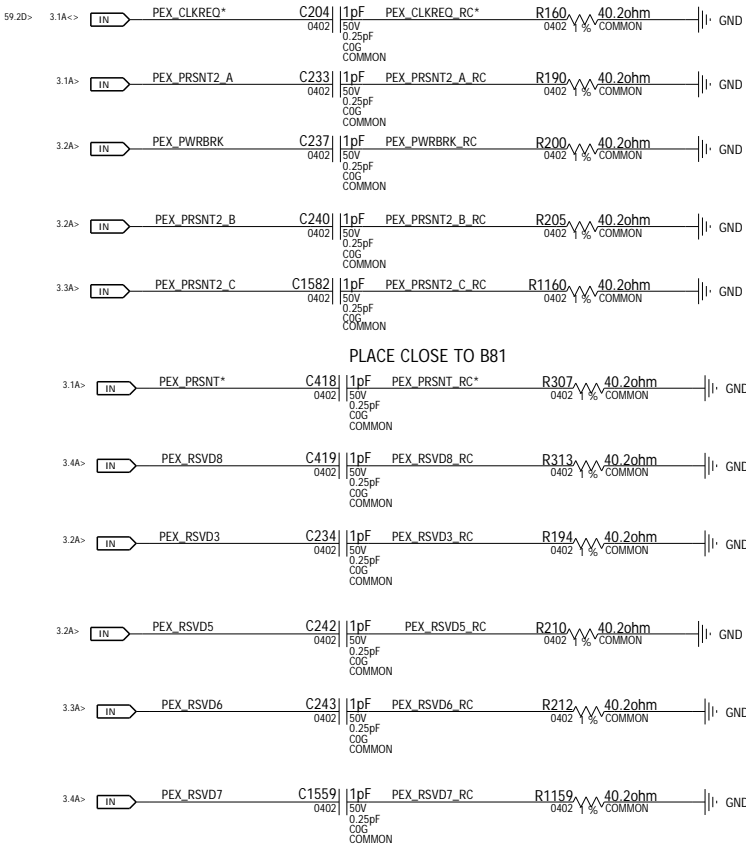
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