H11H4-AM V:1.1

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40	DC/DC VCORE PWM IC
41	DC/DC VCORE DRIVER IC
42	DC/DC VCCGT&VSA
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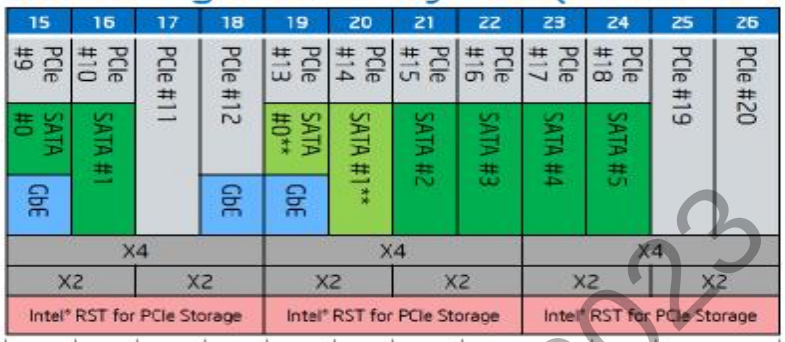
HSIO Lane Assignements by SKU (Lanes 1-14)

HSIO Lane Assignements by SKU (Lanes 15-26)



Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

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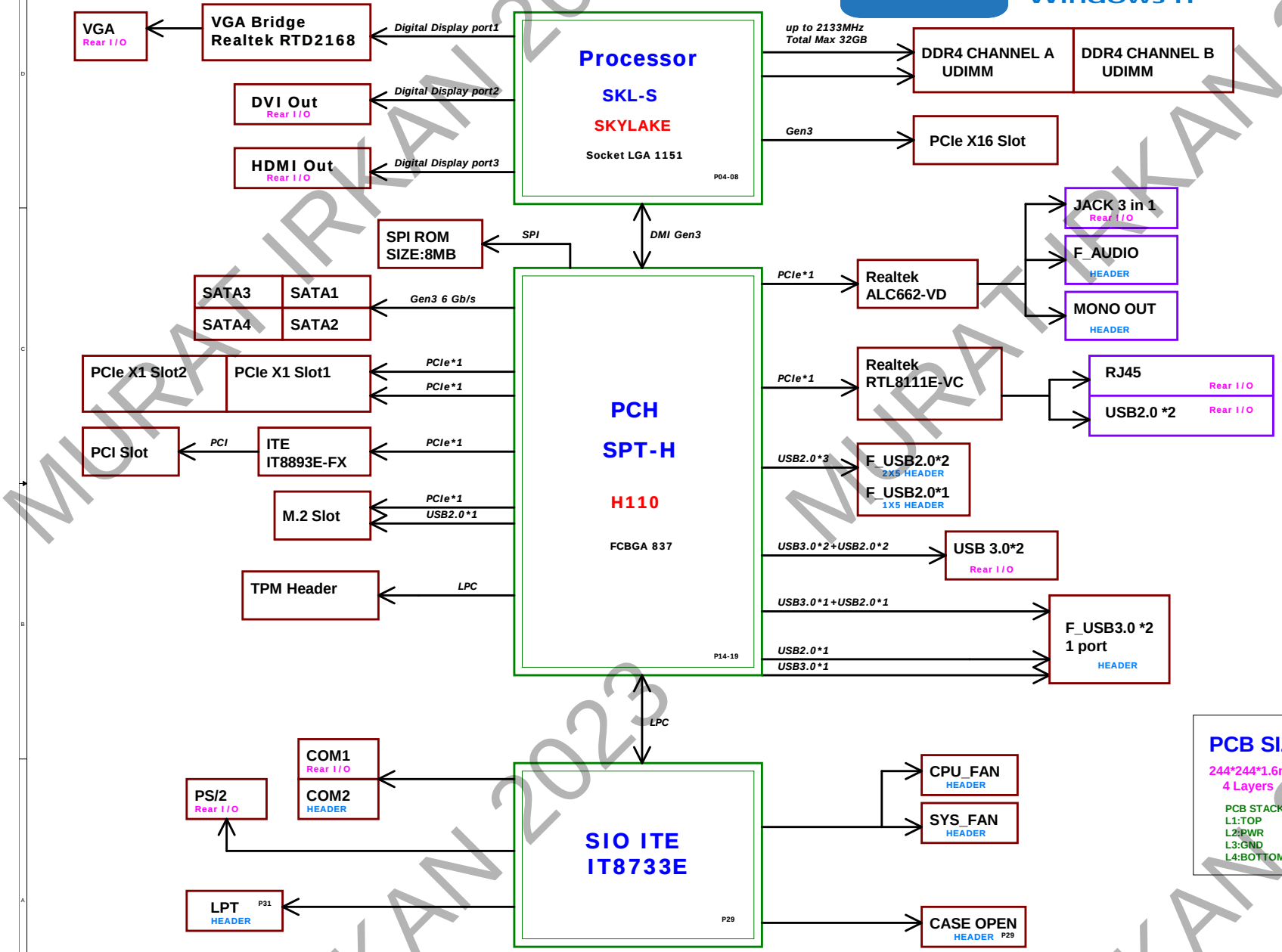
INTEL LGA1151 PLATFORM-ANAKART

Skylake-S Desktop Platform

Windows 10 Windows 11



PCB SIZE

244*244*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems		
Title: Block Diagram		
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PCH-GPIO function

Data:2014/10/02

Pin Name	Power Well	Usage	Default Status	Boot Set(BIOS Check)
GPP_A11	3VSB	PME_L	PME#	PME#
GPP_G13	VCC3	HDPANEL_DETECT	GPI	GPI
GPP_G14	VCC3	on-board TPM detect	GPI	GPI
GPP_E7	VCC3	THERMAL_SD	GPI	GPI
GPP_B3	3VSB	BT_DIS_L	GPI	GPO-->Hi
GPP_H15	3VSB	for ACER reserve	GPI	GPI
GPP_H14	3VSB	for ACER reserve	GPI	GPI
GPP_E9	3VSB	BIOS WP Jumper	GPI	GPI
GPP_F16	3VSB	USB_EN	GPI	GPO-->Hi
GPP_F17	3VSB	LPC_PME_L	GPI	GPI
GPP_E0	VCC3	OBR	GPI	GPI
GPD11	DSW	LAN_DIS_L	LANPHYPC	LANPHYPC
GPD9	DSW	PCH_RI_L	SLP_WLAN#	GPI
GPD10	DSW	ME Disable	SLP_S5#	GPO-->Low
GPD0	DSW	RLAN_PWR_EN	BATLOW#	GPO-->Hi
GPP_F22	VCC3	PCH_GPP_F22	GPI	PCH_GPP_F22
GPP_G22	VCC3	TP_VGA	GPI	TP_VGA
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPI	CLK_REQ1_M.2_WLAN_L
GPP_B17	3VSB	M.2_DIS_L_R	GPI	M.2_DIS_L_R

SIO-GPIO function

Data:2013/10/01

Pin Name	Power Well	Usage	Default SET

Interrupt mapping

Data:2014/11/10

Function	INT# port	PCIe*1 port	Device

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Title: GPIO Function/INT# Mapping

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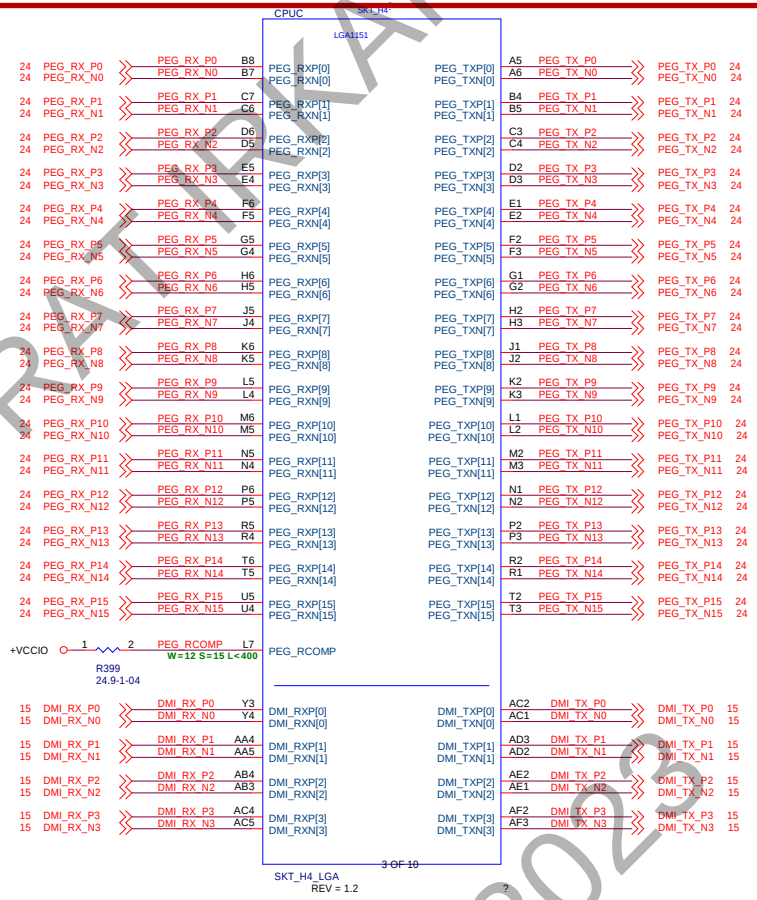
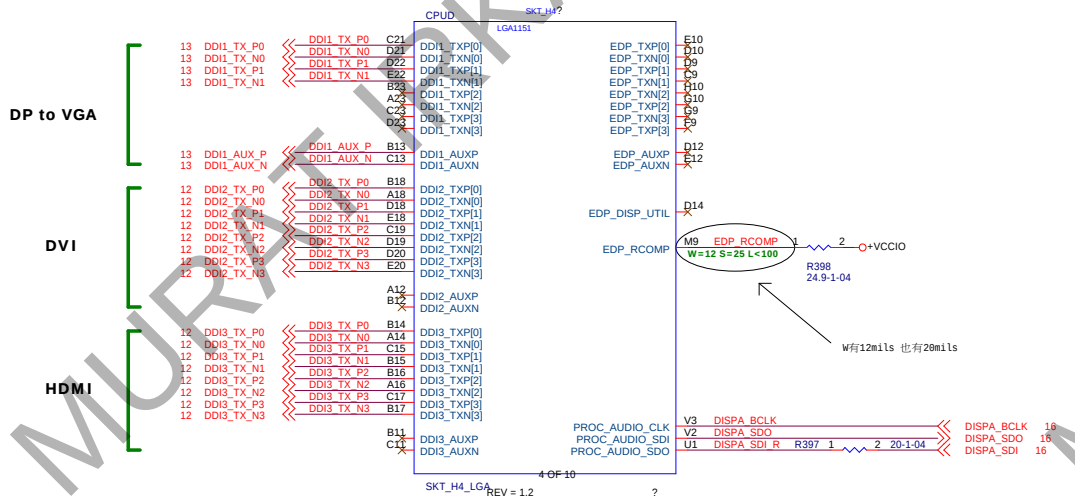
INTEL LGA1151 SOKET PLATFORM





Elitegroup Computer Systems	
Title	CPU-PEG/DMI/DDI/EDP
Size: Custom	Document Number: H11H4-AM
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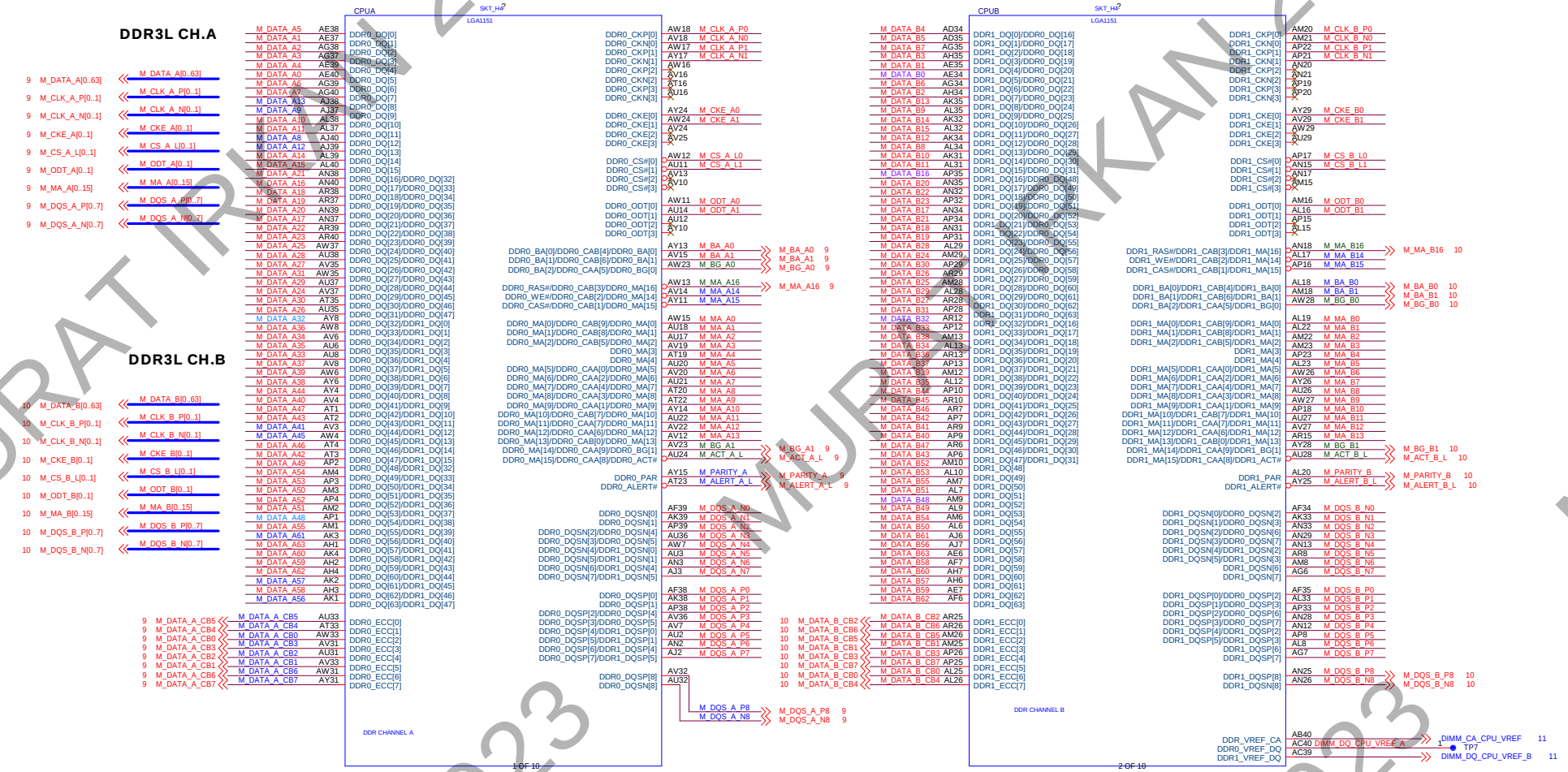
INTEL LGA1151 SOKET PLATFORM



Elitegroup Computer Systems	
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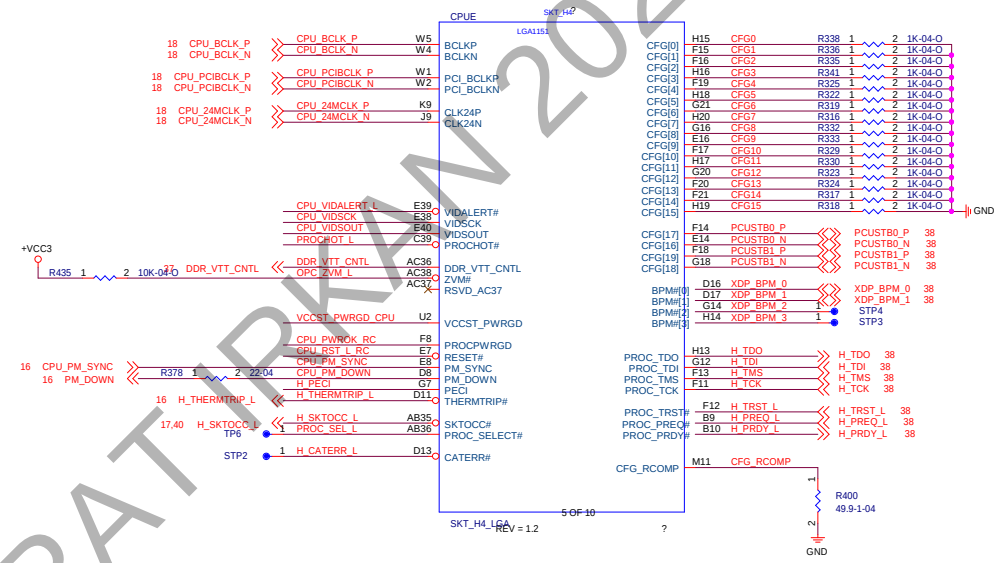
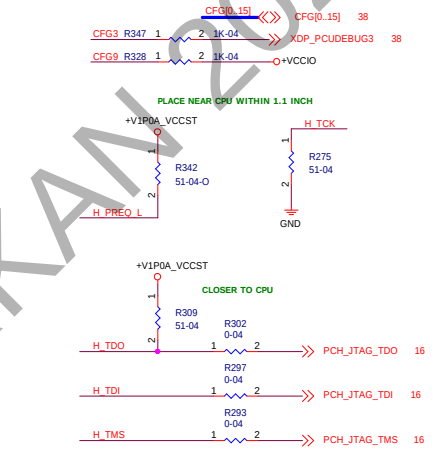
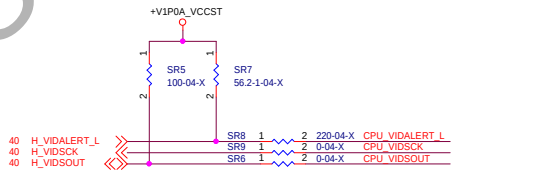


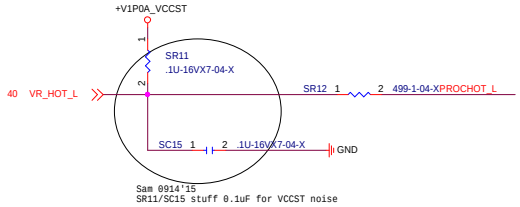
CFG[0:15] Configuration note

- **CFG[0]:** Strap value sampled after PCU PLL lock until de-asserted:
  - 0 = Test.
  - 1 = (Default) Normal Operation; No test.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 0 = Lane numbers reversed.
  - 1 = Normal operation.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 0 = Disabled.
  - 1 = (default) Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation:
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = Reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
  - 0 = PEG Wait for BIOS for training.
  - 1 = (default) PEG Train Immediately following RESET# de-assertion.
- **CFG[19:8]:** Reserved configuration lanes.

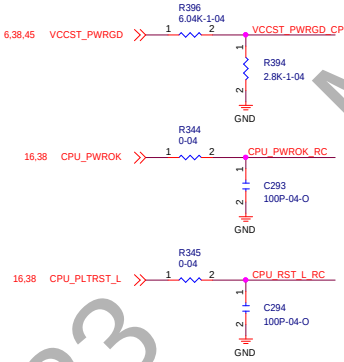


Asynchronous & Sideband Signal

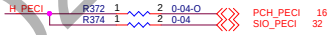




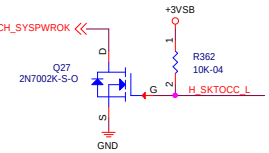
Processor Power Good



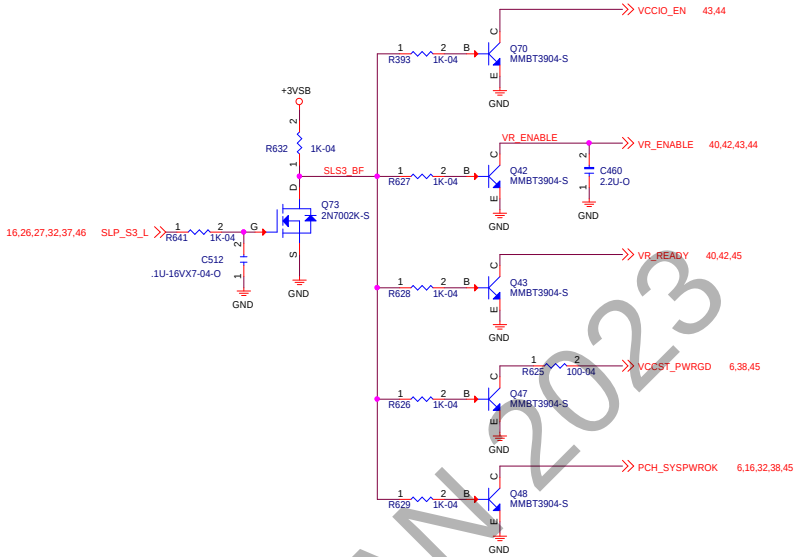
PECI



SKTOCC#



Sequencing Circuit



Elitegroup Computer Systems		
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Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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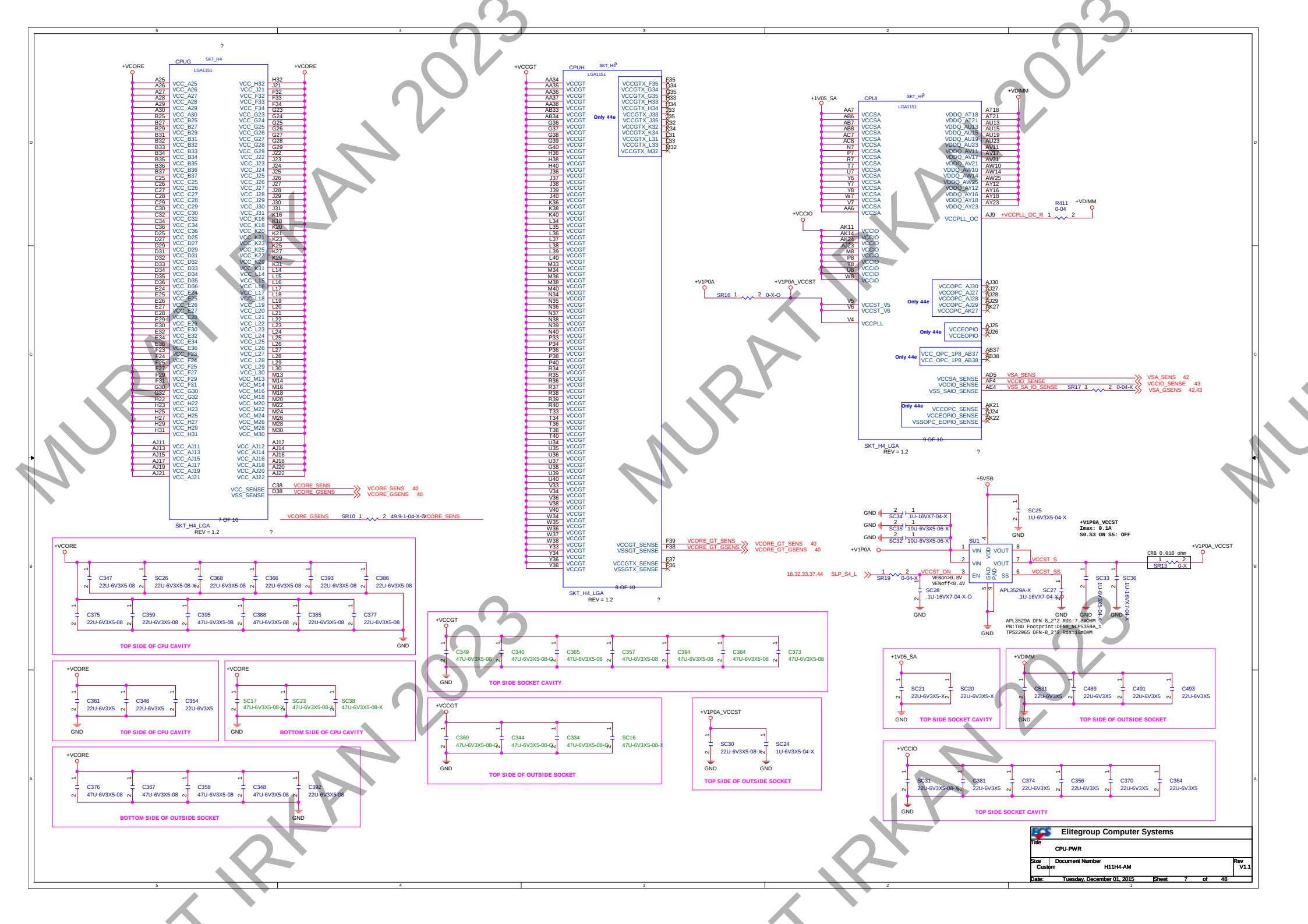
CPUG
SKT_H4
LGA1151
+VCORE
VCC_SENSE
VSS_SENSE
VCORE_SENS
VCORE_GSENS
7 OF 10
SKT_H4_LGA
REV = 1.2
CPUH
VCCGT
VCCGTX_SENSE
VSSGTX_SENSE
VCORE_GT_SENS
VCORE_GT_GSENS
8 OF 10
CPUI
+1V05_SA
+VDIMM
+VCCIO
+V1P0A
+V1P0A_VCCST
VCCPLL_OC
VCCIO_SENSE
VSA_SENSE
VSS_SA_IO_SENSE
9 OF 10
TOP SIDE OF CPU CAVITY
BOTTOM SIDE OF CPU CAVITY
TOP SIDE SOCKET CAVITY
TOP SIDE OF OUTSIDE SOCKET
BOTTOM SIDE OF OUTSIDE SOCKET
TOP SIDE SOCKET CAVITY
TOP SIDE OF OUTSIDE SOCKET
TOP SIDE SOCKET CAVITY
+5VSB
APL3529A-X
TPS22965
+V1P0A_VCCST
Imax: 0.1A
S0.S3 ON S5: OFF
Elitegroup Computer Systems
CPU-PWR
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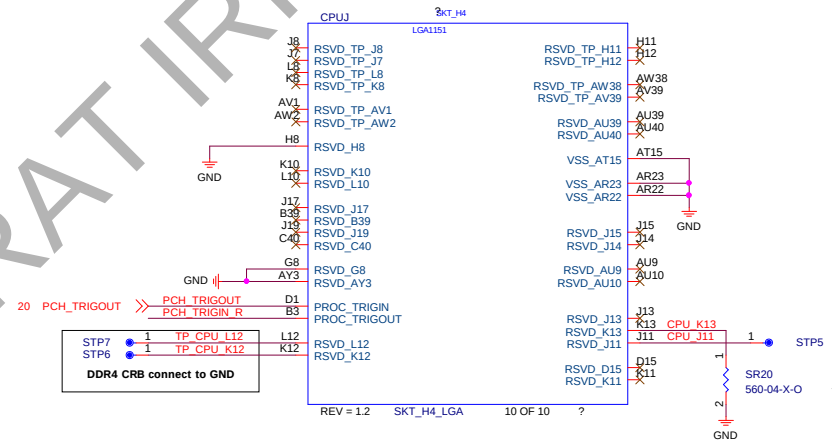

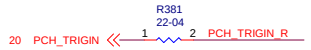

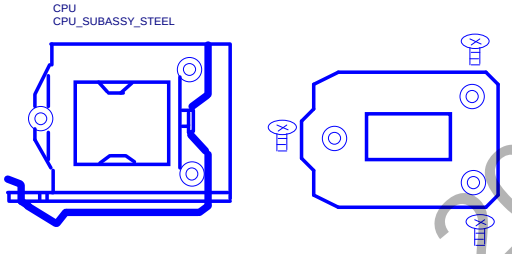

CPU steel (T/U pahse)
PN:20-800-005911
SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES
(替)20-800-007611

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Title: CPU-GND			
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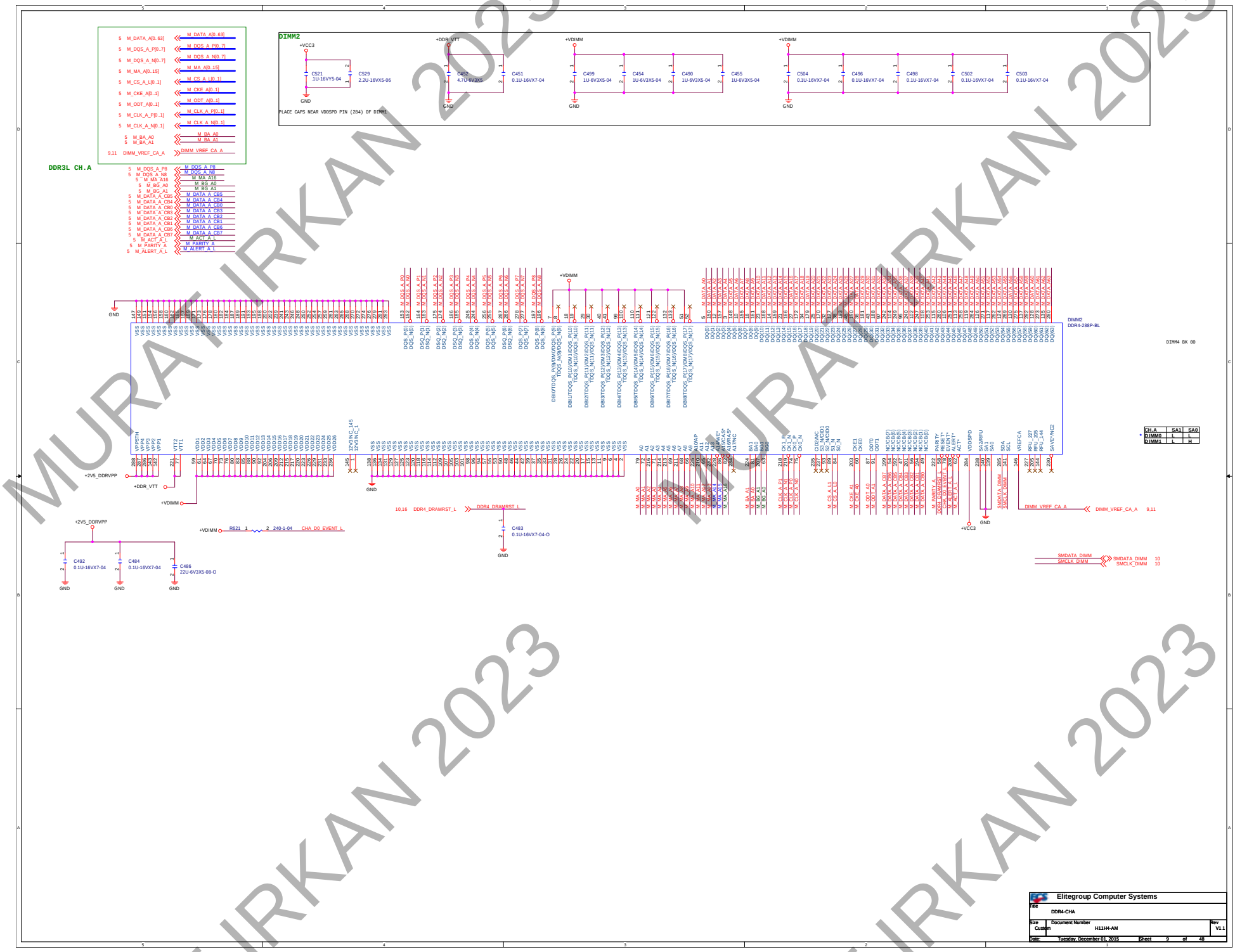

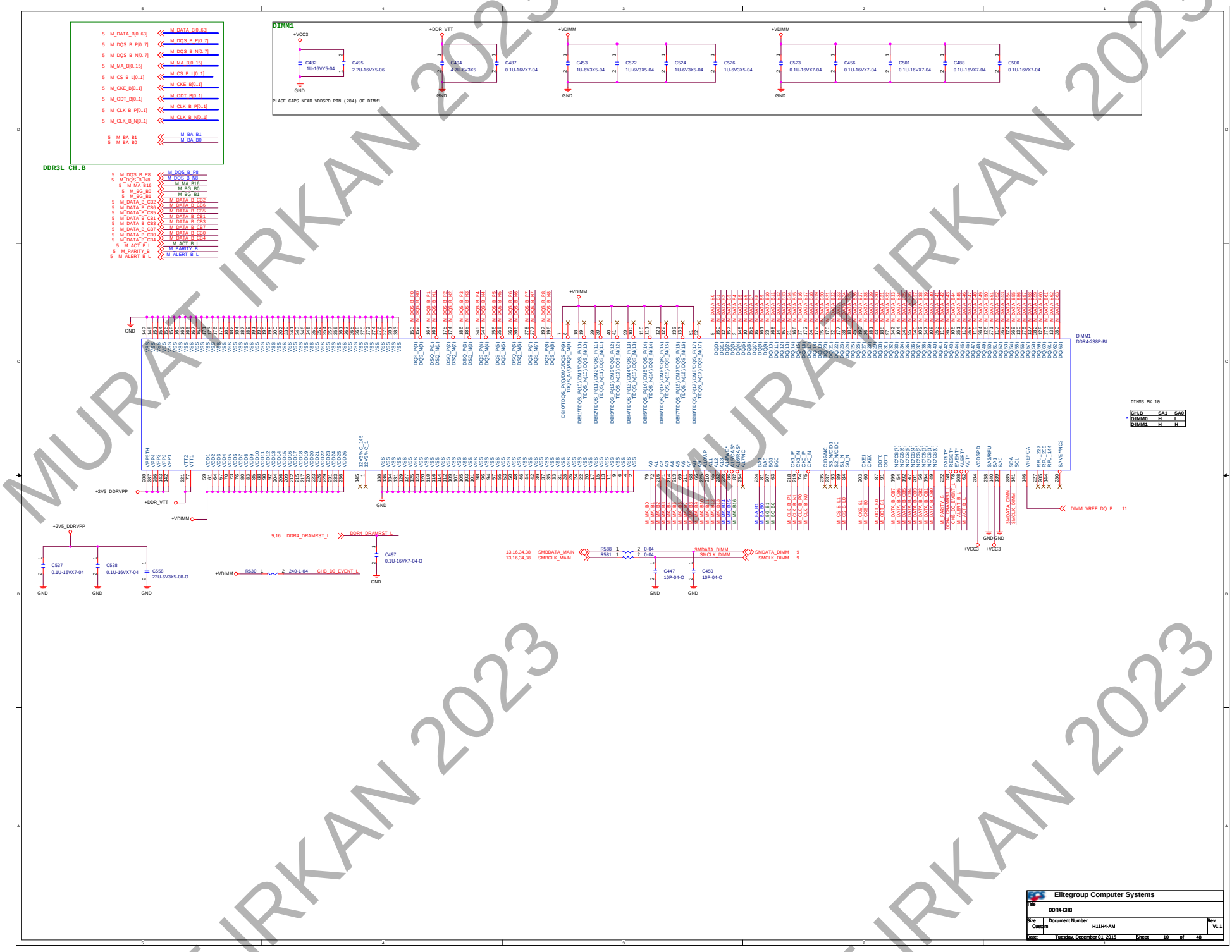

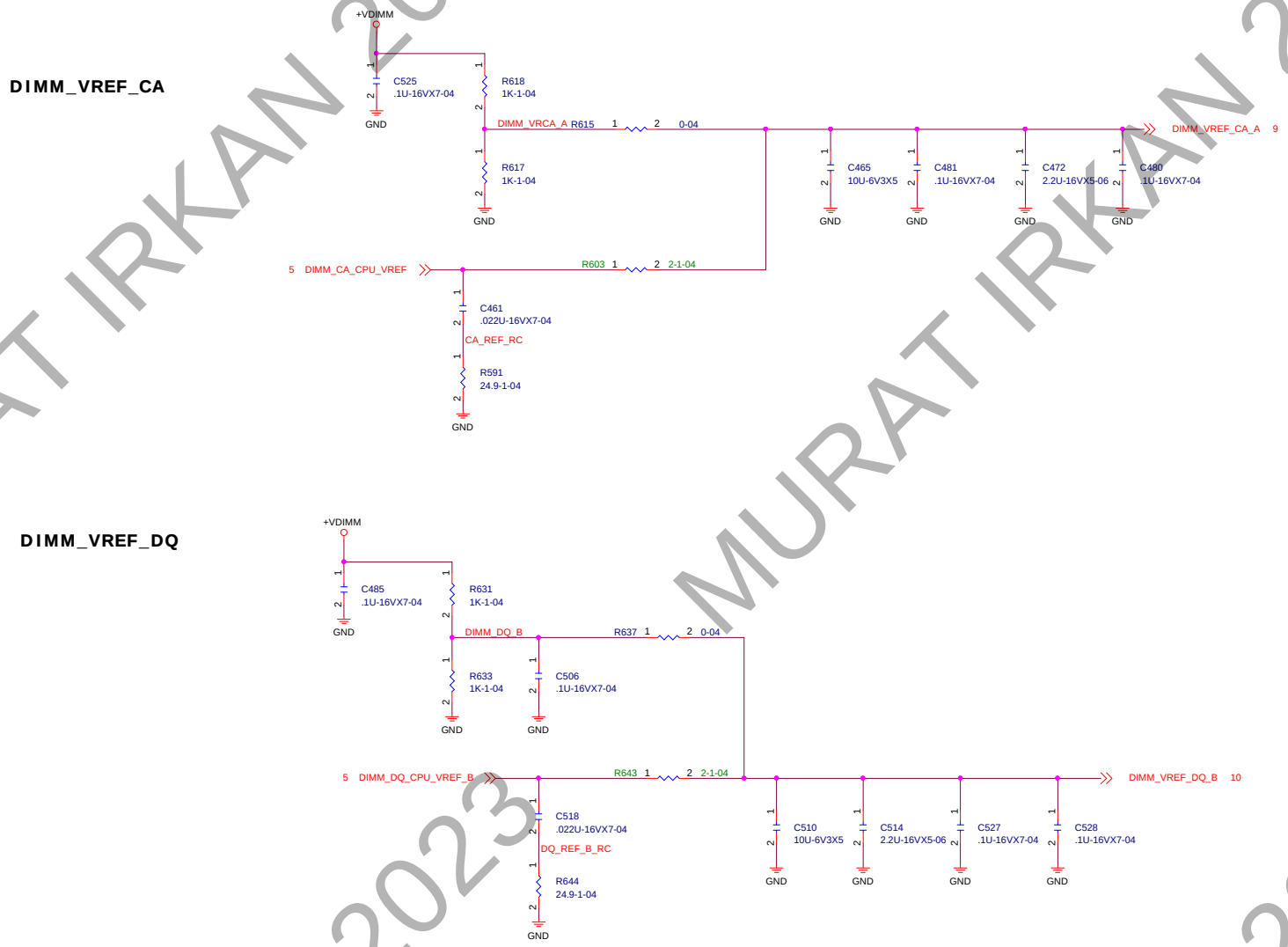

Elitegroup Computer Systems	
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Size: Custom	Document Number: H11H4-AM
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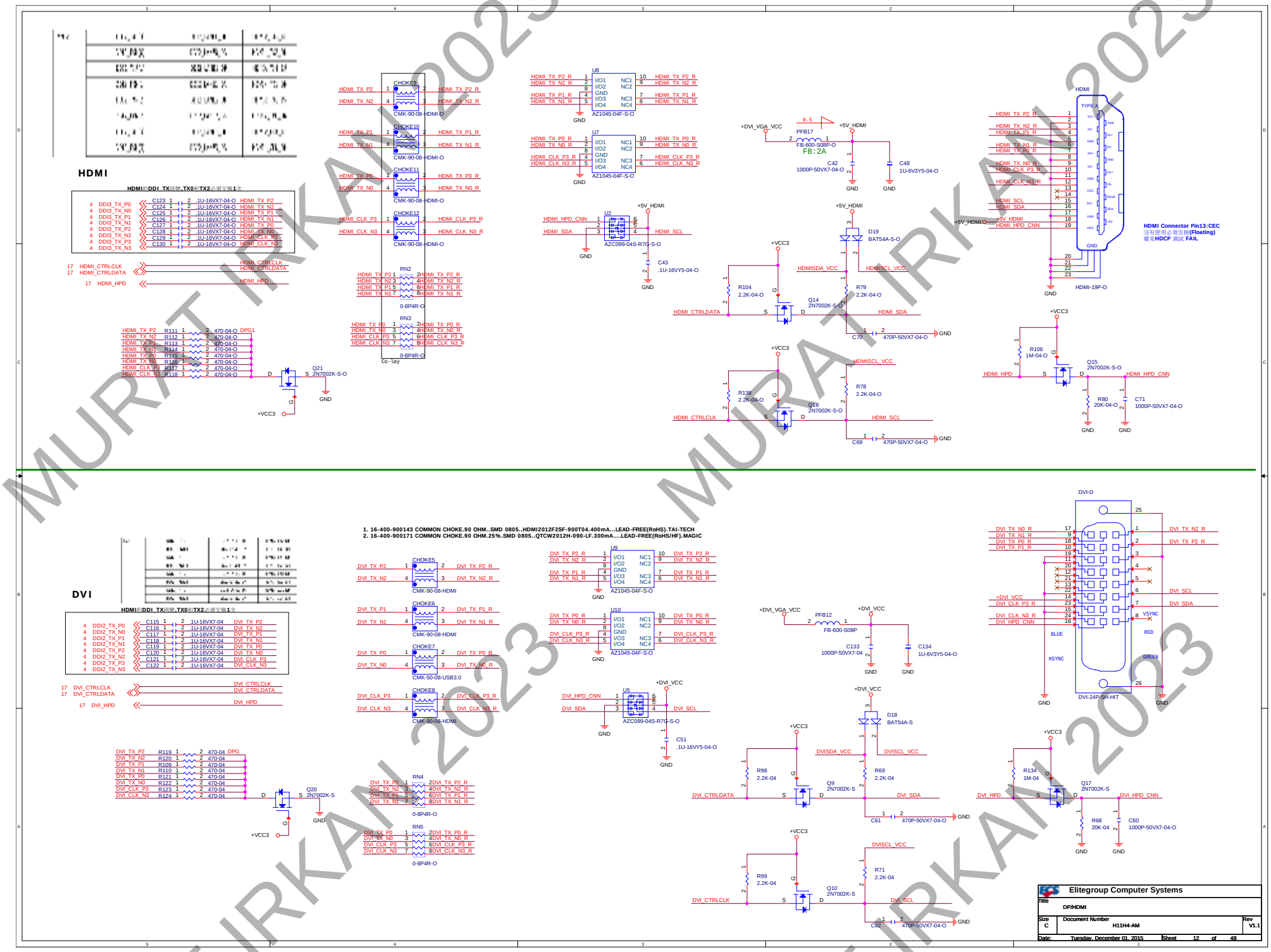
HDMI
HDMI的DDI_TX訊號,TX0和TX2必須交換1次
HDMI_TX_P2
HDMI_TX_N2
HDMI_TX_P1
HDMI_TX_N1
HDMI_TX_P0
HDMI_TX_N0
HDMI_CLK_P3
HDMI_CLK_N3
HDMI_CTRLCLK
HDMI_CTRLDATA
HDMI_HPD
CHOKE9
CHOKE10
CHOKE11
CHOKE12
CMK-90-08-HDMI-O
RN2
RN3
0-8P4R-O
Co-Lay
U8
U7
AZ1045-04F-S-O
U2
AZC099-04S-R7G-S-O
HDMI_HPD_CNN
HDMI_SDA
HDMI_SCL
+5V_HDMI
+VCC3
+DVI_VGA_VCC
PFB17
FB-600-S08P-O
FB:2A
C42
1000P-50VX7-04-O
C48
1U-6V3Y5-04-O
C43
.1U-16VY5-04-O
D19
BAT54A-S-O
HDMISDA_VCC
HDMISCL_VCC
R104
2.2K-04-O
R79
2.2K-04-O
Q14
2N7002K-S-O
C70
470P-50VX7-04-O
R138
2.2K-04-O
R78
2.2K-04-O
Q18
2N7002K-S-O
C69
470P-50VX7-04-O
HDMI
TYPE A
HDMI-19P-O
HDMI Connector Pin13:CEC
沒有使用此選空接(Floating)
避免HDCP 測試 FAIL
R106
1M-04-O
Q15
2N7002K-S-O
R80
20K-04-O
C71
1000P-50VX7-04-O
R111
R112
R113
R114
R115
R116
R117
R118
470-04-O
DPG1
Q21
2N7002K-S-O
DVI
HDMI的DDI_TX訊號,TX0和TX2必須交換1次
DVI_TX_P2
DVI_TX_N2
DVI_TX_P1
DVI_TX_N1
DVI_TX_P0
DVI_TX_N0
DVI_CLK_P3
DVI_CLK_N3
DVI_CTRLCLK
DVI_CTRLDATA
DVI_HPD
CHOKE5
CHOKE6
CHOKE7
CHOKE8
CMK-90-08-HDMI
CMK-50-08-USB3.0
RN4
RN5
U9
U10
AZ1045-04F-S-O
U5
AZC099-04S-R7G-S-O
DVI_HPD_CNN
DVI_SDA
DVI_SCL
+DVI_VCC
PFB12
FB-600-S08P
C133
1000P-50VX7-04
C134
1U-6V3Y5-04-O
C51
.1U-16VY5-04-O
D18
BAT54A-S
DVISDA_VCC
DVISCL_VCC
R98
2.2K-04
R69
2.2K-04
Q9
2N7002K-S
C61
470P-50VX7-04-O
R99
2.2K-04
R71
2.2K-04
Q10
2N7002K-S
C62
470P-50VX7-04-O
DVI-D
DVI-24P-SH-HIT
BLUE
HSYNC
RED
GREEN
VSYNC
R134
1M-04
Q17
2N7002K-S
R68
20K-04
C60
1000P-50VX7-04-O
R119
R120
R109
R110
R121
R122
R123
R124
470-04
DPG
Q20
2N7002K-S
1. 16-400-900143 COMMON CHOKE.90 OHM..SMD 0805..HDMI2012F2SF-900T04.400mA...LEAD-FREE(RoHS).TAI-TECH
2. 16-400-900171 COMMON CHOKE.90 OHM.25%.SMD 0805..QTCW2012H-090-LF.300mA....LEAD-FREE(RoHS/HF).MAGIC
Elitegroup Computer Systems
Title
DP/HDMI
Size C
Document Number H11H4-AM
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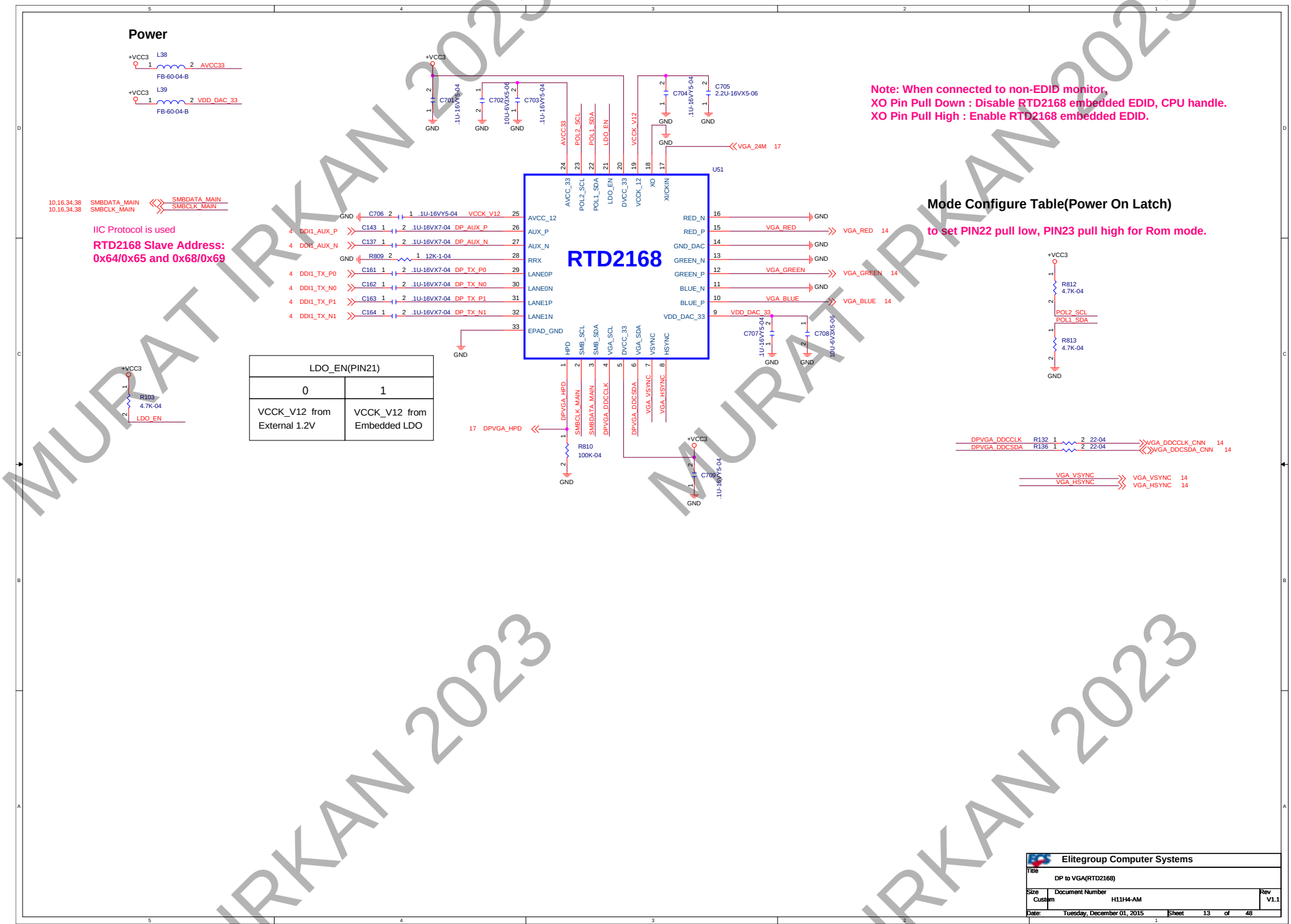
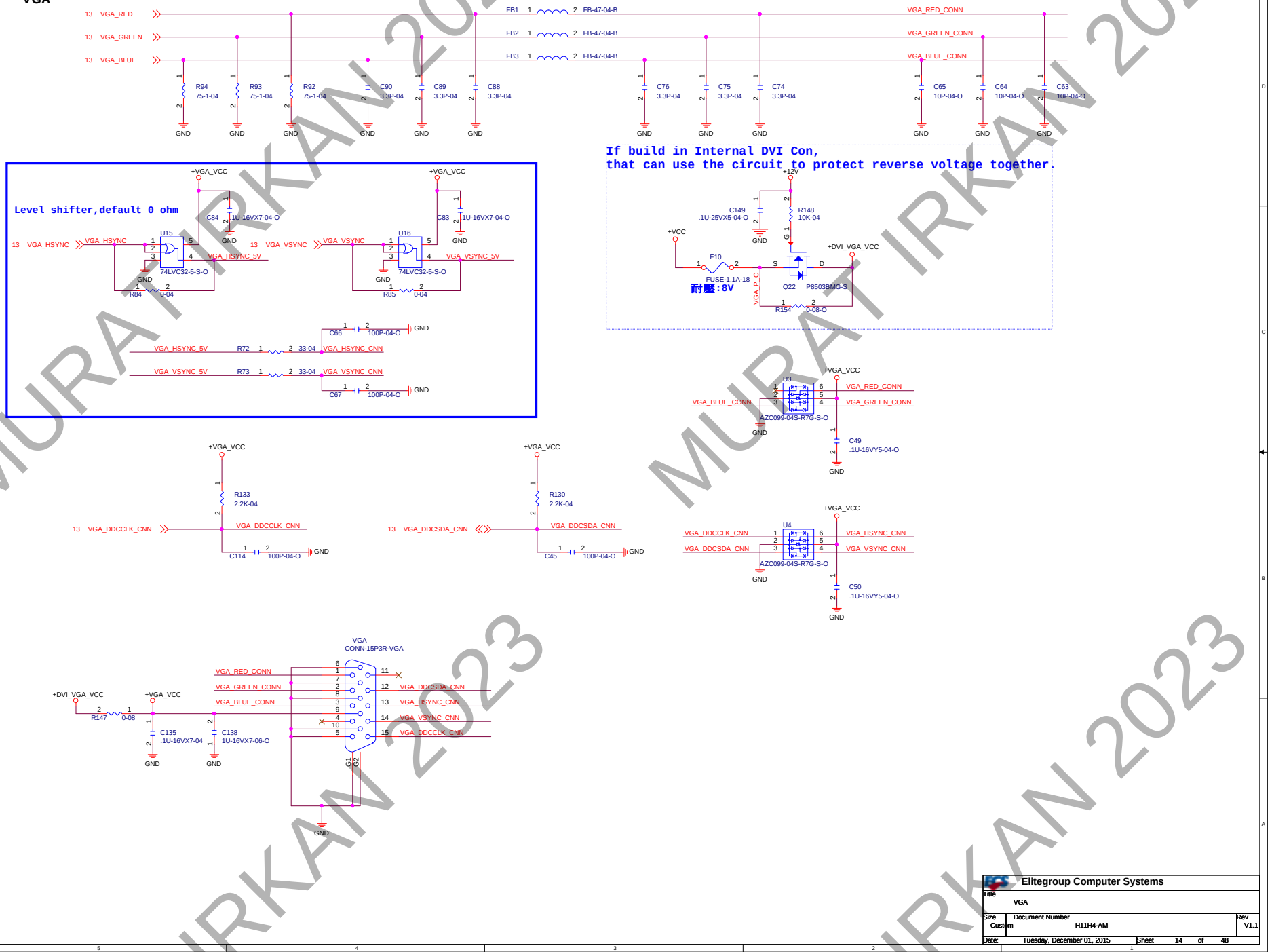


VGA



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Title: VGA		
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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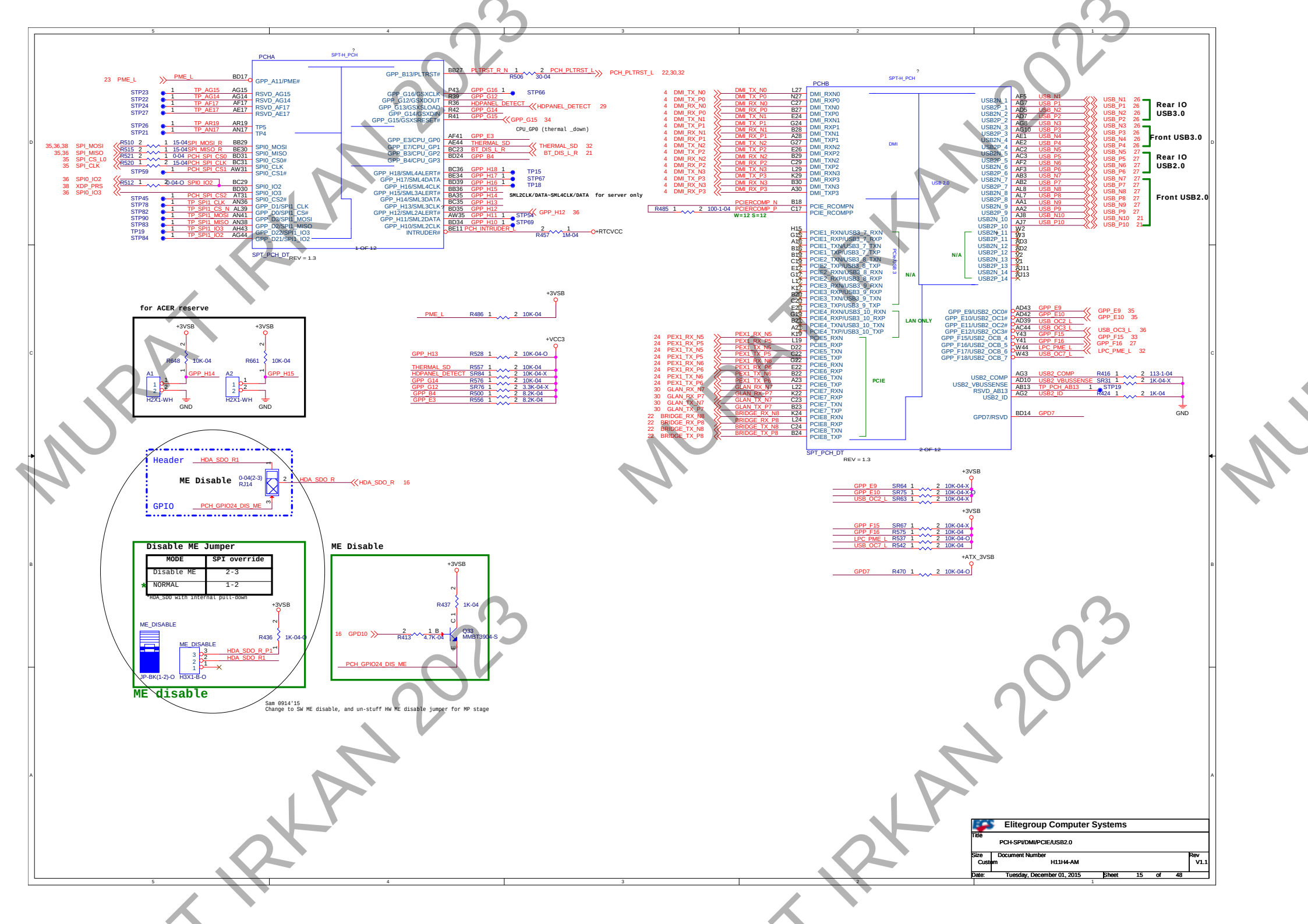

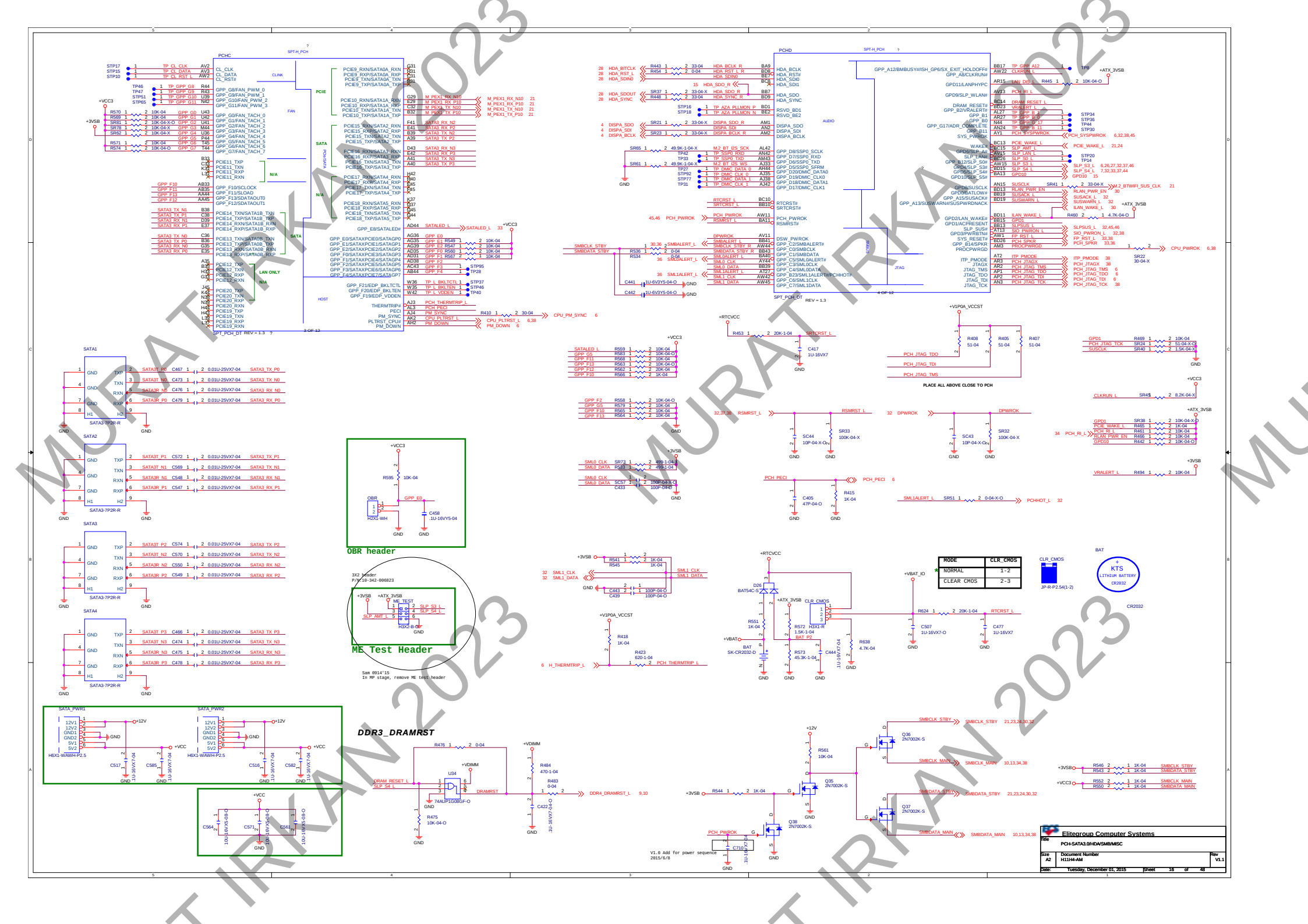

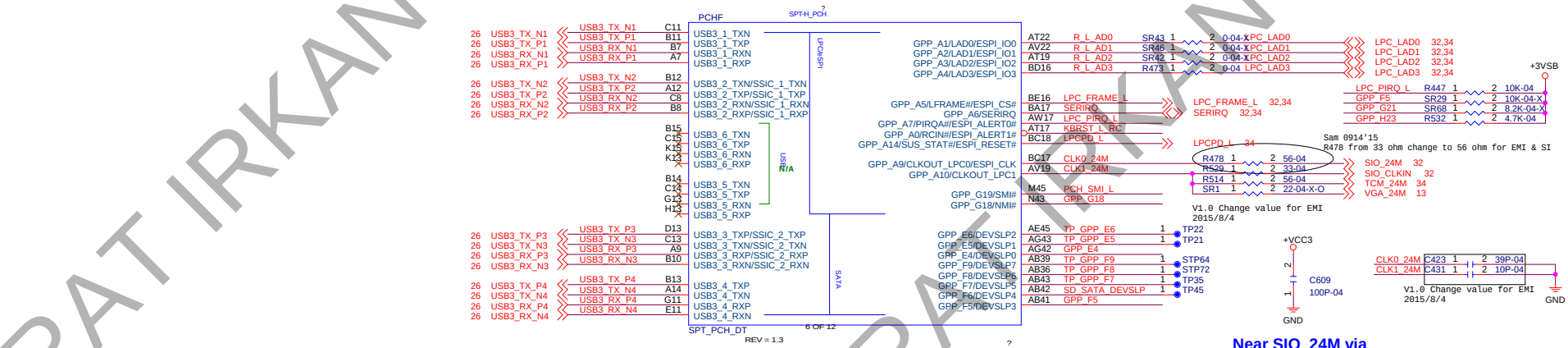

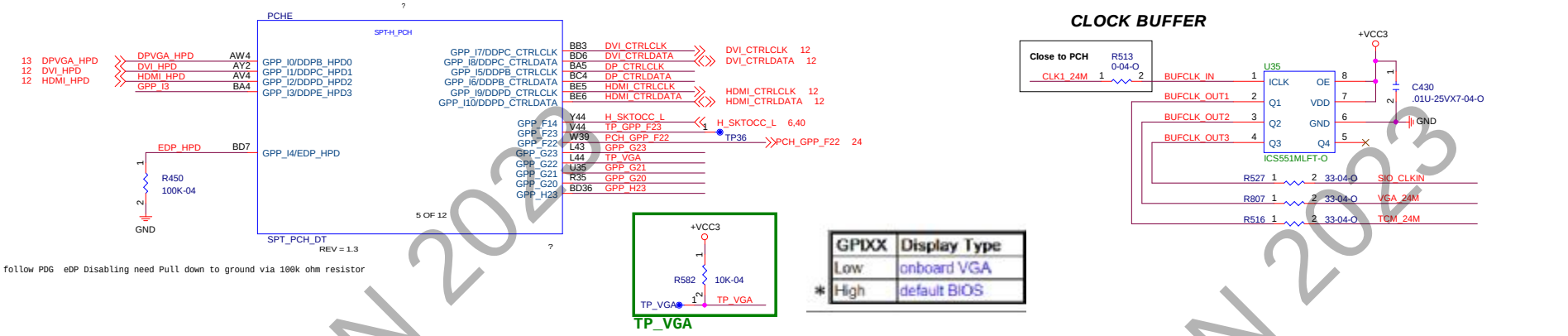

Elitegroup Computer Systems

Title	PCH-USB3.0/LPC		
Size	Document Number		Rev
Custom	H11H4-AM		V1.1
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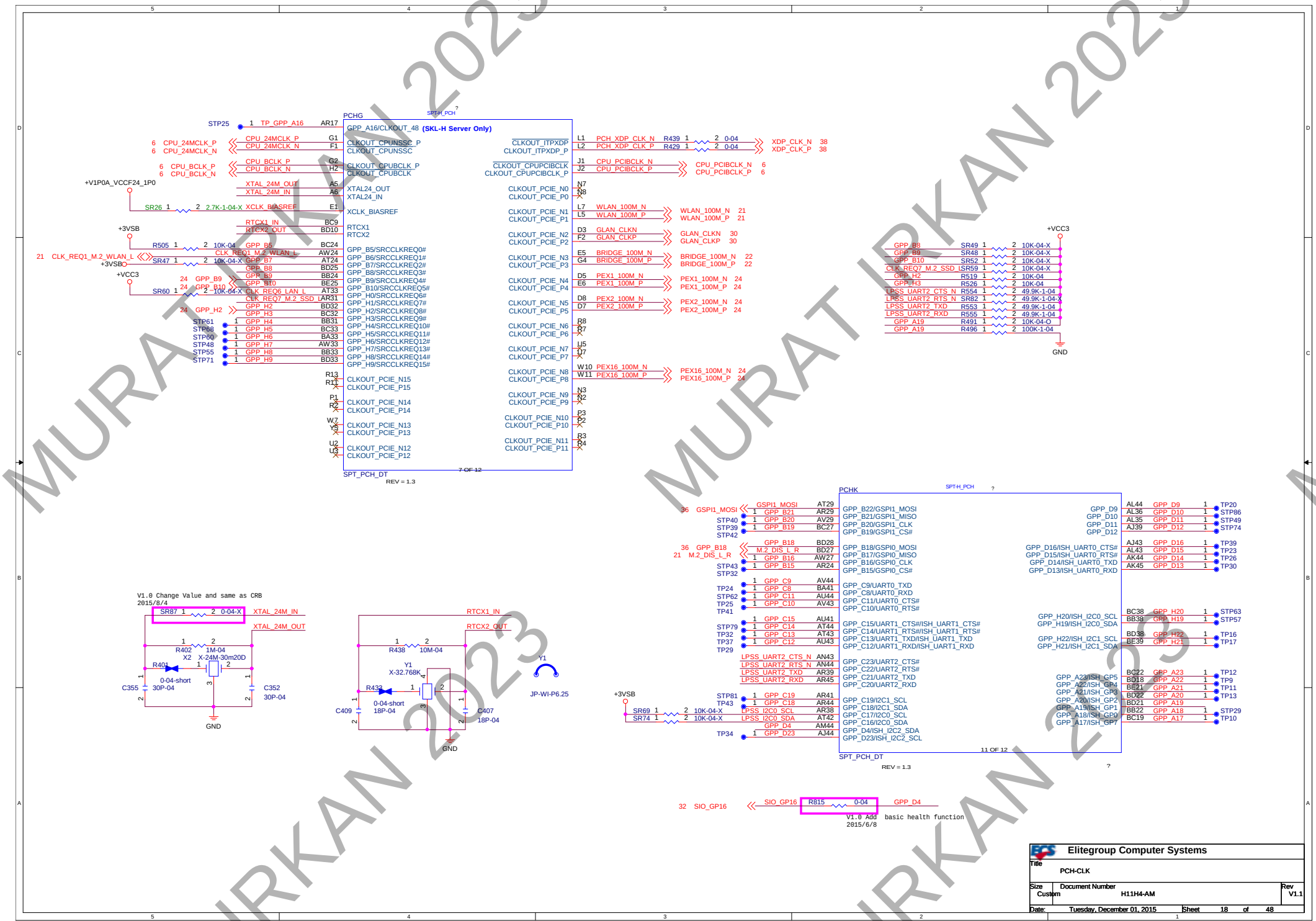
PCHG
SPT-H_PCH
GPP_A16/CLKOUT_48 (SKL-H Server Only)
CPU_24MCLK_P
CPU_24MCLK_N
CPU_BCLK_P
CPU_BCLK_N
XTAL_24M_OUT
XTAL_24M_IN
XCLK_BIASREF
RTCX1_IN
RTCX2_OUT
RTCX1
RTCX2
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
PCH_XDP_CLK_N
PCH_XDP_CLK_P
XDP_CLK_N
XDP_CLK_P
CPU_PCIBCLK_N
CPU_PCIBCLK_P
WLAN_100M_N
WLAN_100M_P
GLAN_CLKN
GLAN_CLKP
BRIDGE_100M_N
BRIDGE_100M_P
PEX1_100M_N
PEX1_100M_P
PEX2_100M_N
PEX2_100M_P
PEX16_100M_N
PEX16_100M_P
7 OF 12
SPT_PCH_DT
REV = 1.3
+V1P0A_VCCF24_1P0
+3VSB
+VCC3
CLK_REQ1_M.2_WLAN_L
CLK_REQ7_M.2_SSD_L
CLK_REQ6_LAN_L
M.2_DIS_L_R
M.2_DIS_L_R
GPP_B5
GPP_B6
GPP_B7
GPP_B8
GPP_B9
GPP_B10
GPP_H2
GPP_H3
GPP_H4
GPP_H5
GPP_H6
GPP_H7
GPP_H8
GPP_H9
STP25
STP61
STP68
STP60
STP48
STP55
STP71
SR26
SR47
SR60
R505
R13
R11
P1
R2
W7
Y5
U2
U3
V1.0 Change Value and same as CRB
2015/8/4
SR87
R402
1M-04
X2
X-24M-30m20D
R401
0-04-short
30P-04
C355
C352
GND
RTCX1_IN
RTCX2_OUT
R438
10M-04
Y1
X-32.768K
R432
0-04-short
18P-04
C409
C407
JP-WI-P6.25
PCHK
SPT-H_PCH
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA
GPP_D23/ISH_I2C2_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
11 OF 12
SPT_PCH_DT
REV = 1.3
GSPI1_MOSI
M.2_DIS_L_R
SR69
SR74
SIO_GP16
R815
0-04
V1.0 Add basic health function
2015/6/8
Elitegroup Computer Systems
Title
PCH-CLK
Size
Custom
Document Number
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18
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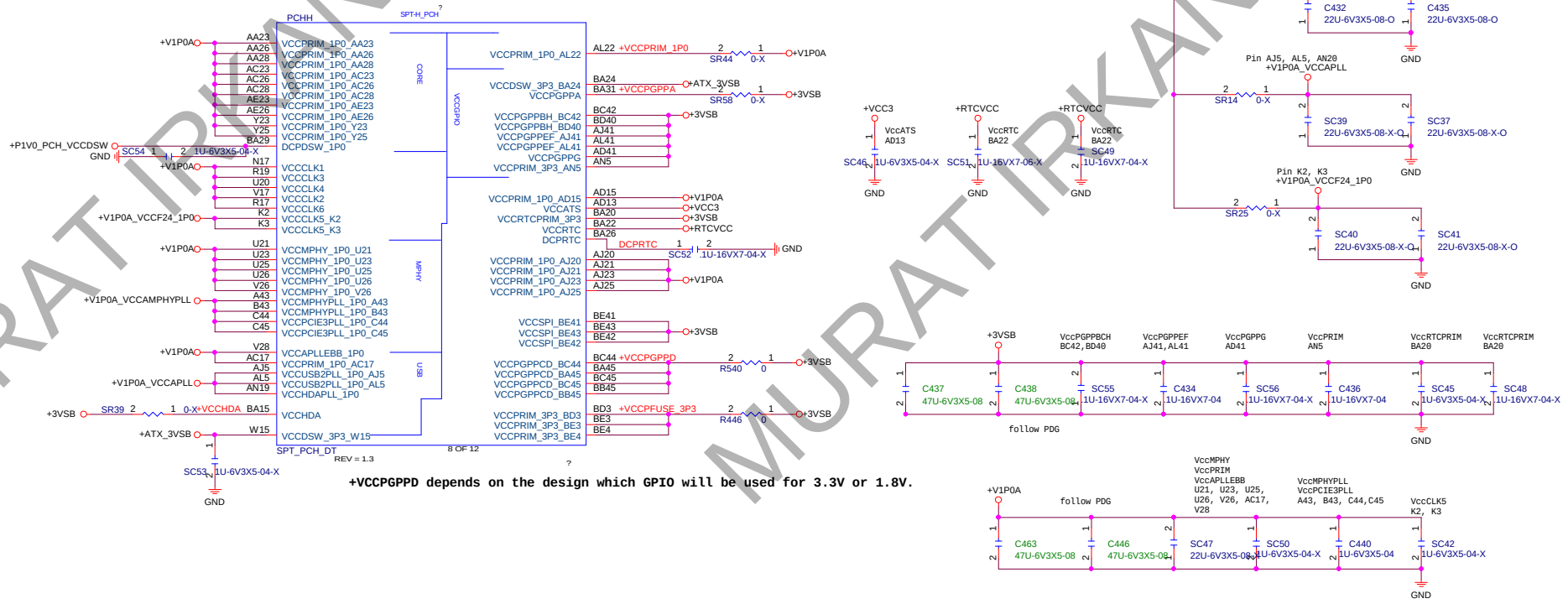
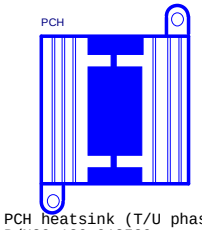
48



+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.



PCH heatsink (T/U phase)
P/N20-120-013580
20-120-013581
V1.0 Change
2015/6/8

Elitegroup Computer Systems			
Title: PCH-PWR			
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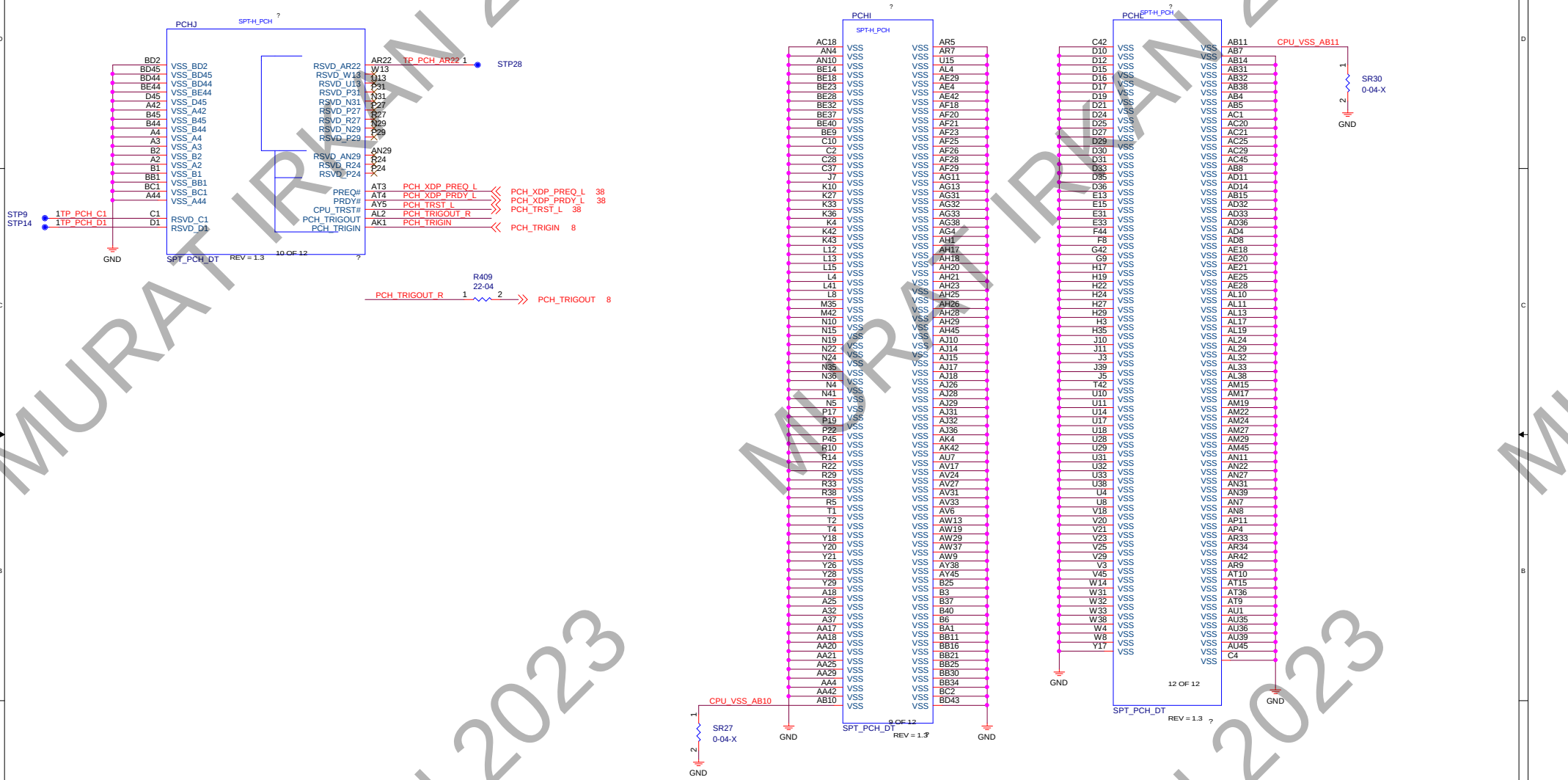

Elitegroup Computer Systems	
Title	PCH-GND
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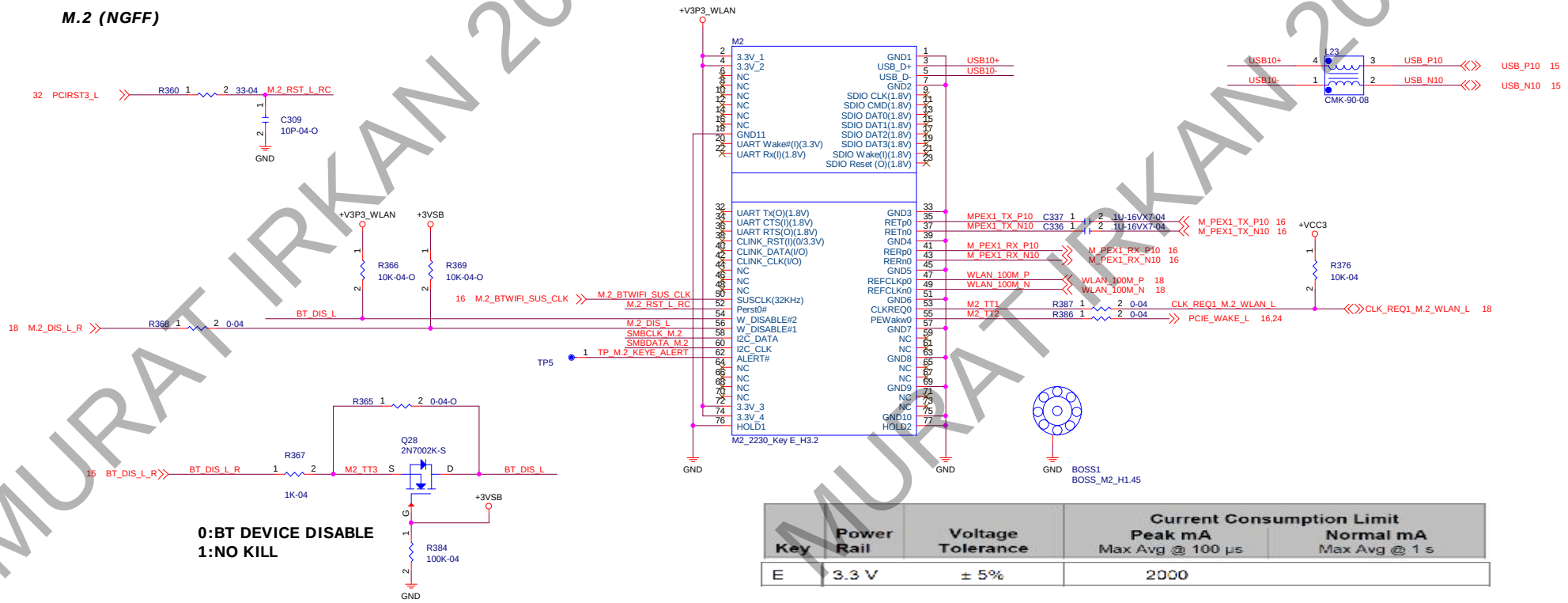
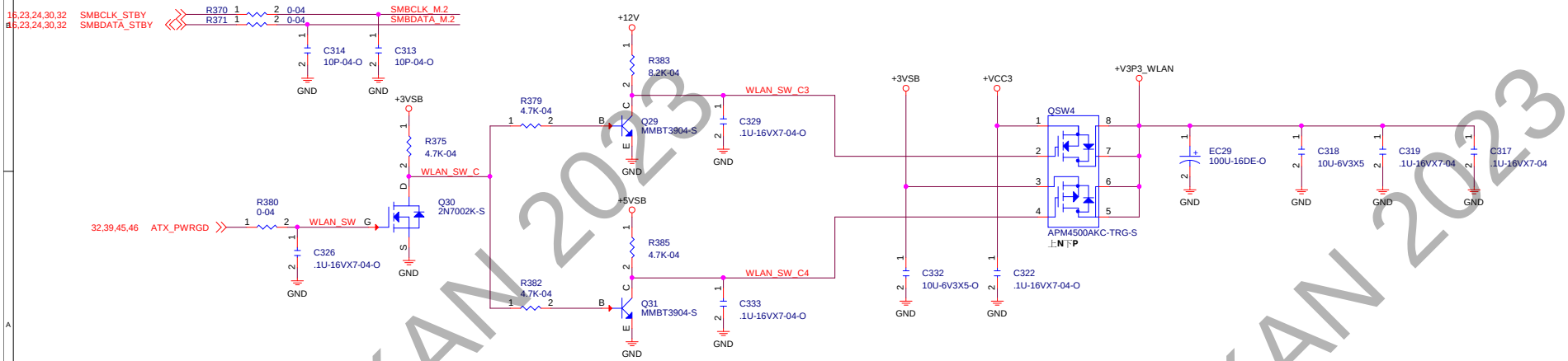
M.2 (NGFF)



Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak mA Max Avg @ 100 µs	Normal mA Max Avg @ 1 s
E	3.3 V	± 5%	2000	



	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB

Elitegroup Computer Systems

Title: M.2 Slot

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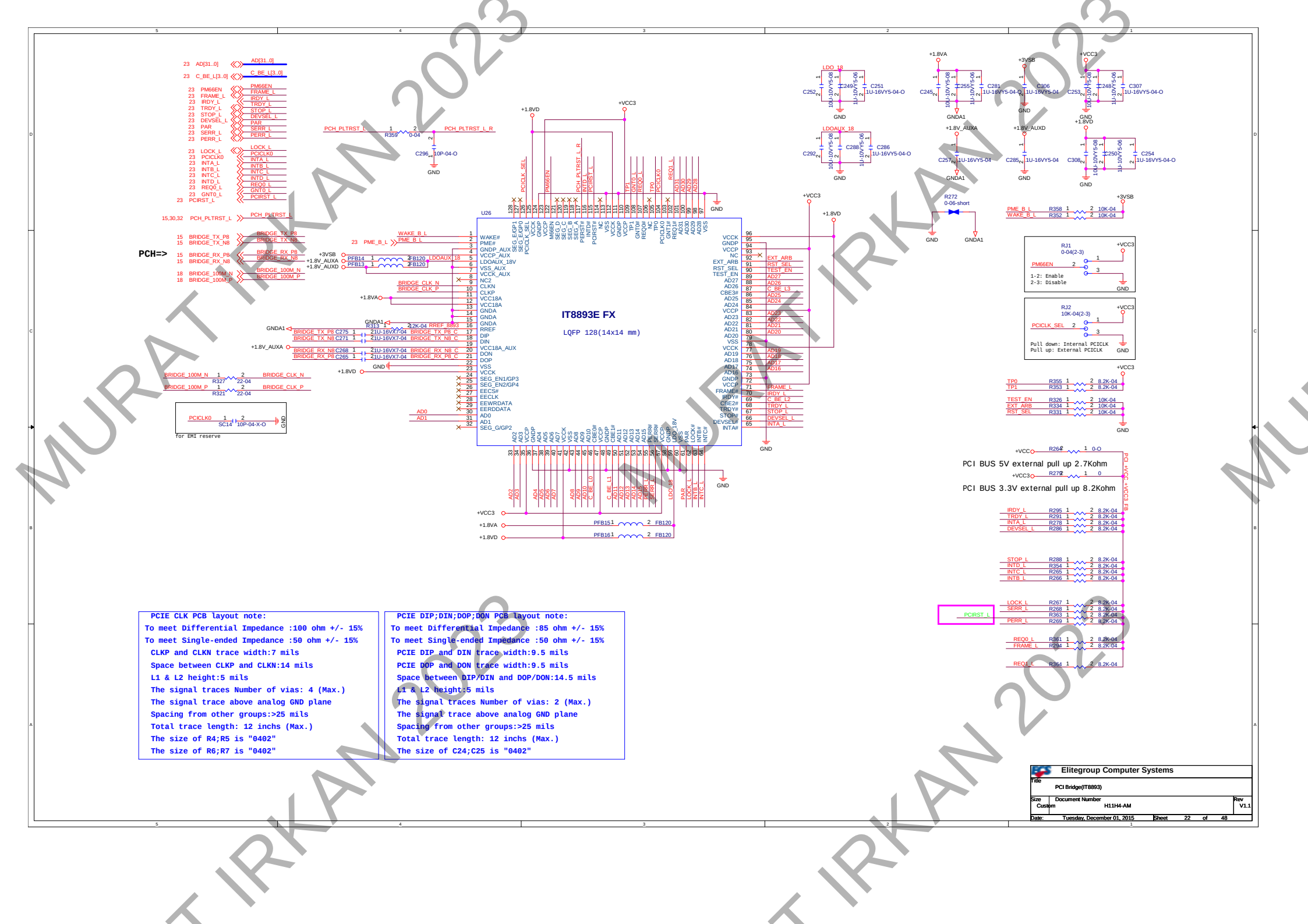
IT8893E FX
LQFP 128(14x14 mm)
PCH=>
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C24;C25 is "0402"
PCI BUS 5V external pull up 2.7Kohm
PCI BUS 3.3V external pull up 8.2Kohm
Elitegroup Computer Systems
PCI Bridge(IT8893)
H11H4-AM
Tuesday, December 01, 2015
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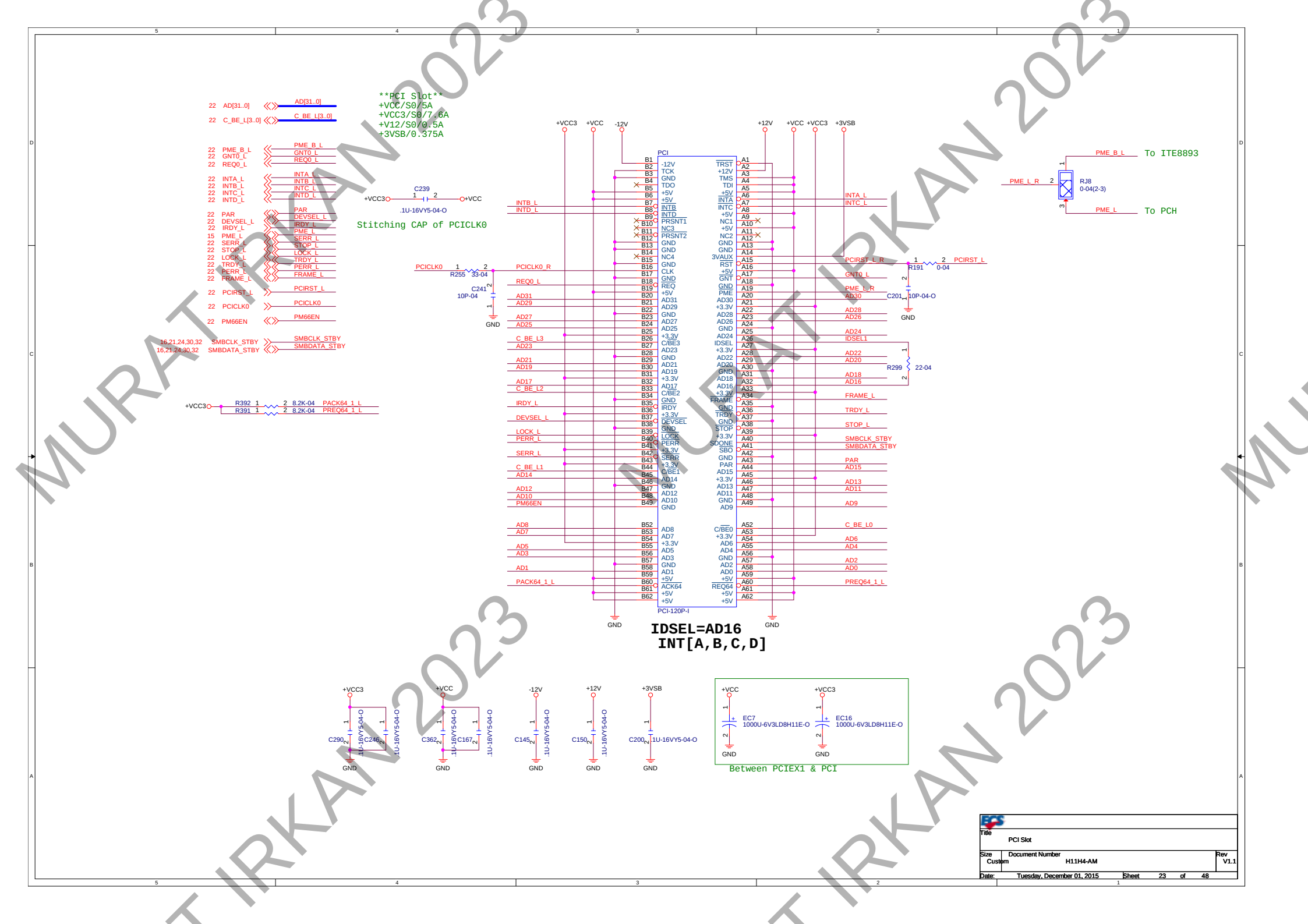

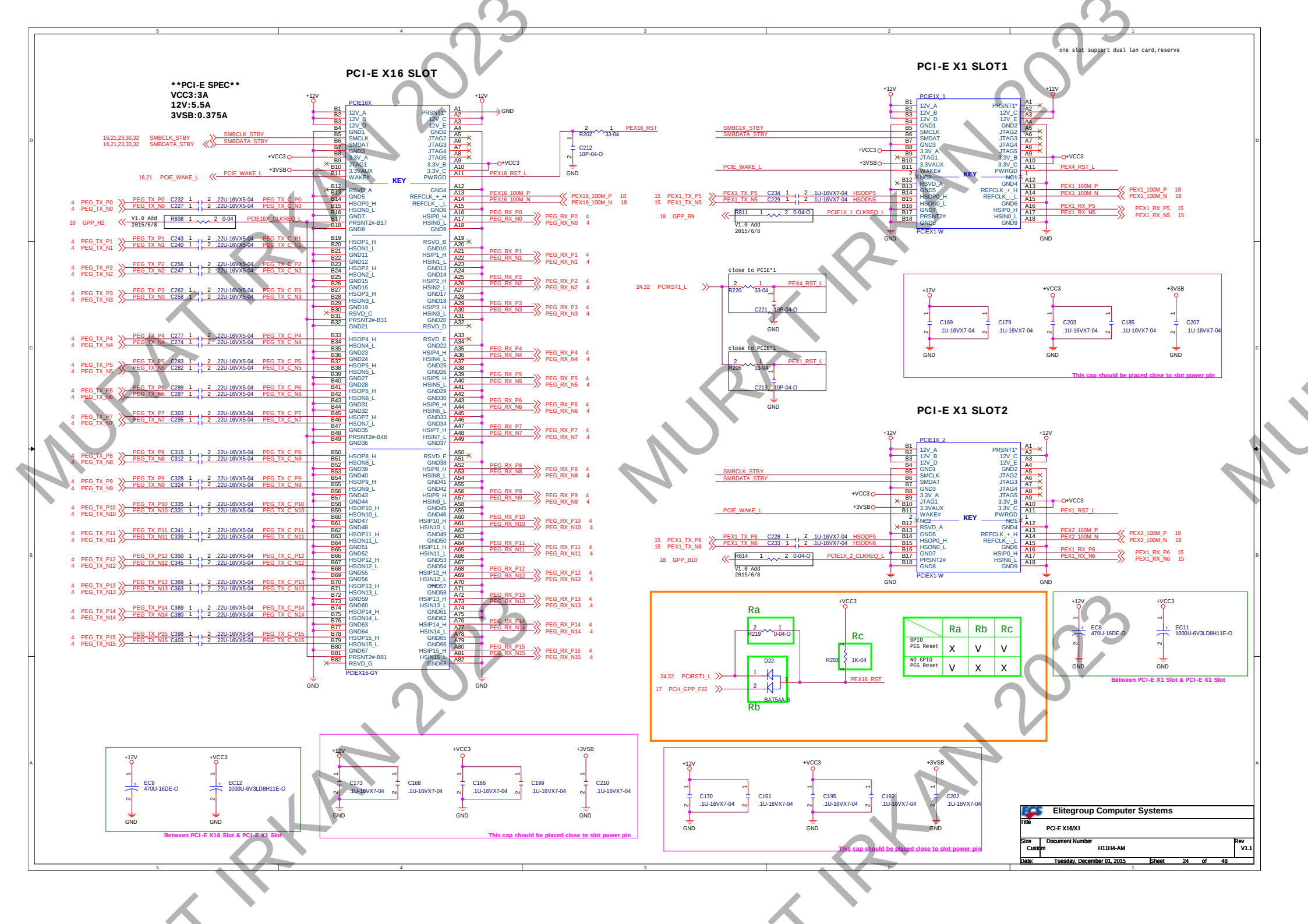
PCI-E X16 SLOT
PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A
PCIE16X
PCIEX16-GY
KEY
PCI-E X1 SLOT1
PCIE1X_1
PCIEX1-W
PCI-E X1 SLOT2
PCIE1X_2
one slot support dual lan card,reserve
close to PCIE*1
This cap should be placed close to slot power pin
Between PCI-E X16 Slot & PCI-E X1 Slot
Between PCI-E X1 Slot & PCI-E X1 Slot
Ra
Rb
Rc
GPIO PEG Reset
NO GPIO PEG Reset
Elitegroup Computer Systems
PCI-E X16/X1
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Title	Reserved		
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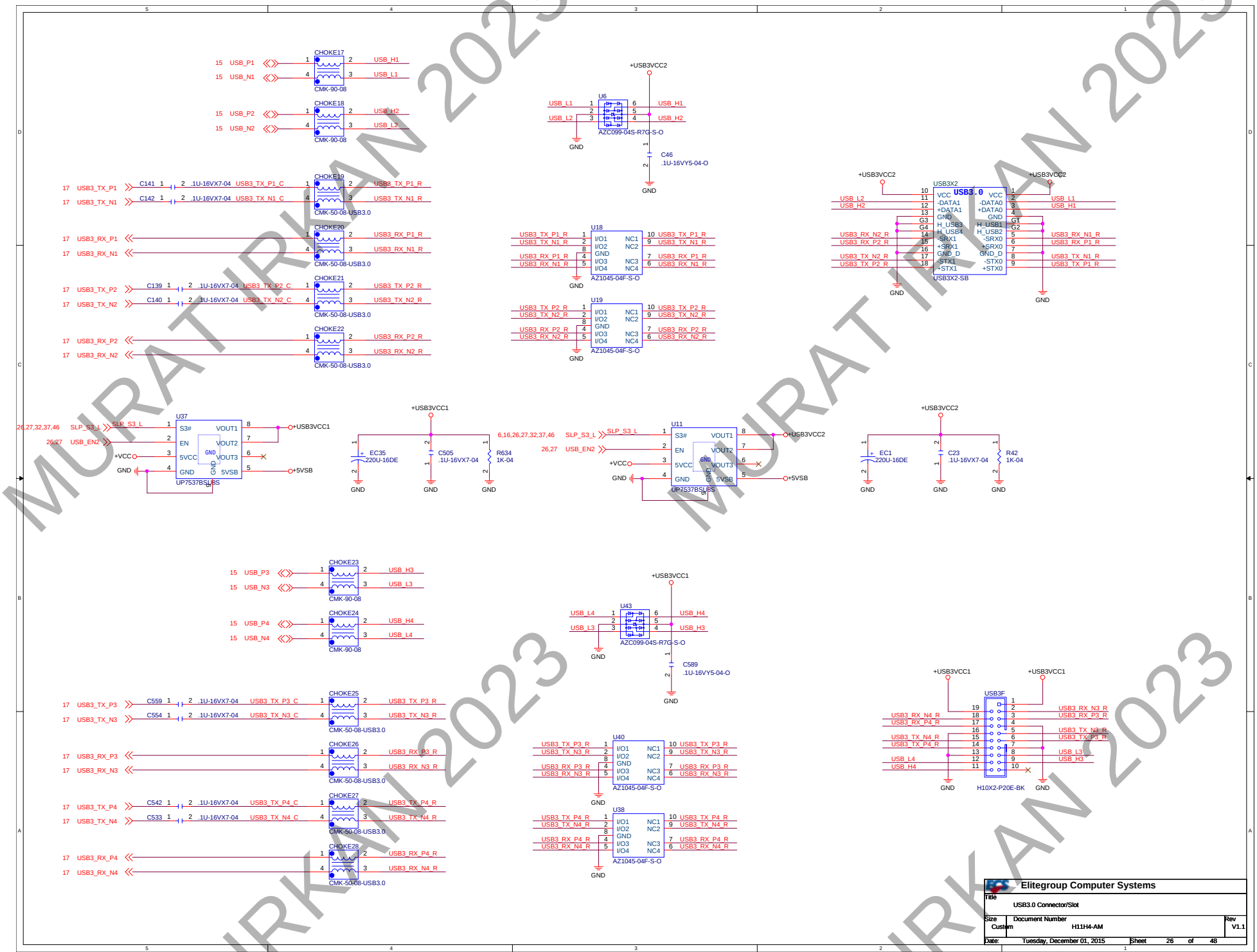
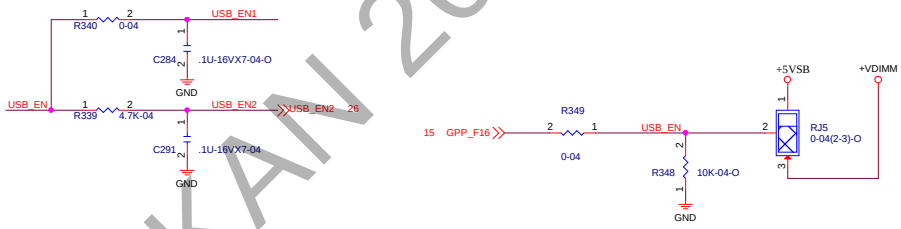
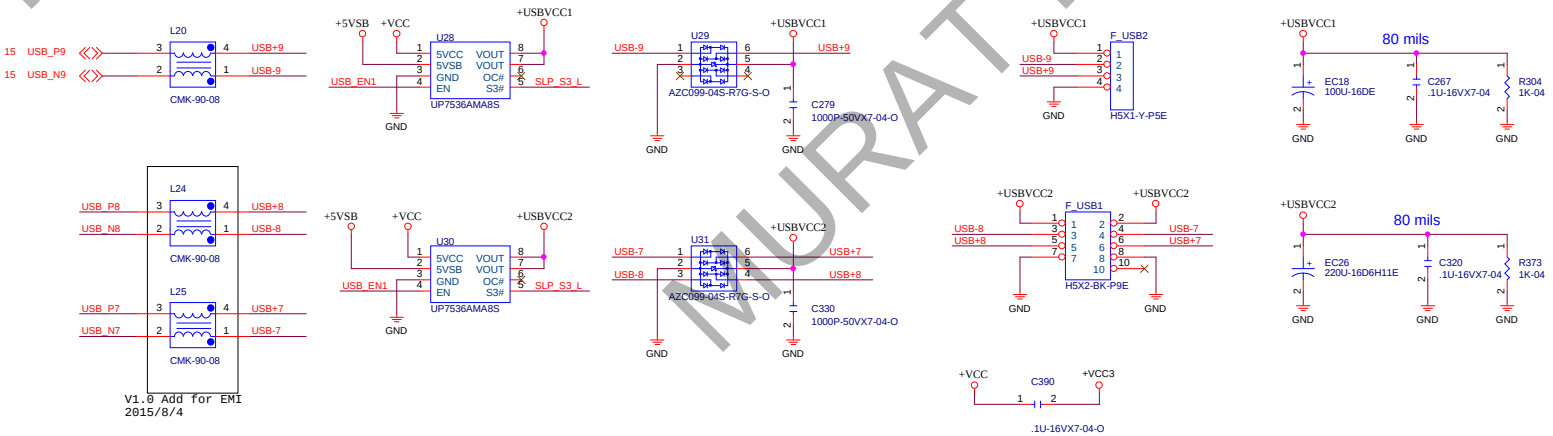


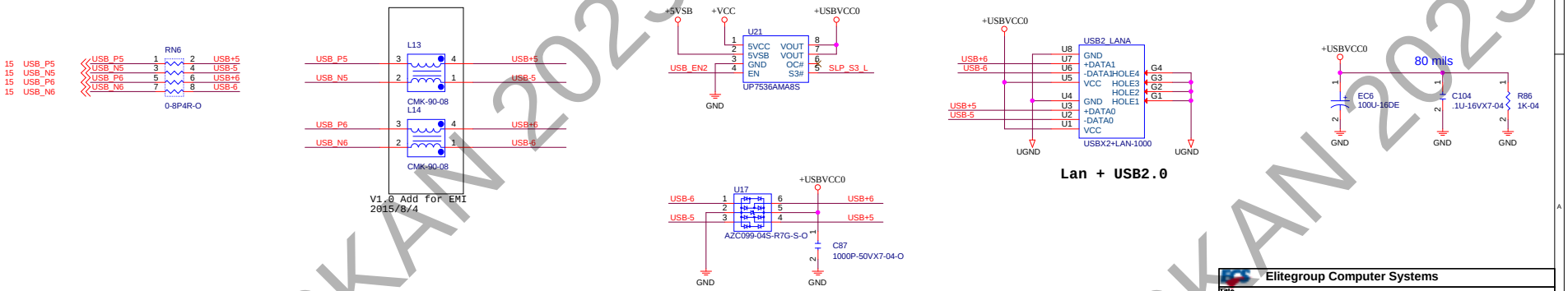


	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	



USB2.0 header

USB2.0 connecter



Elitegroup Computer Systems	
Title	USB2.0 Connector/Header
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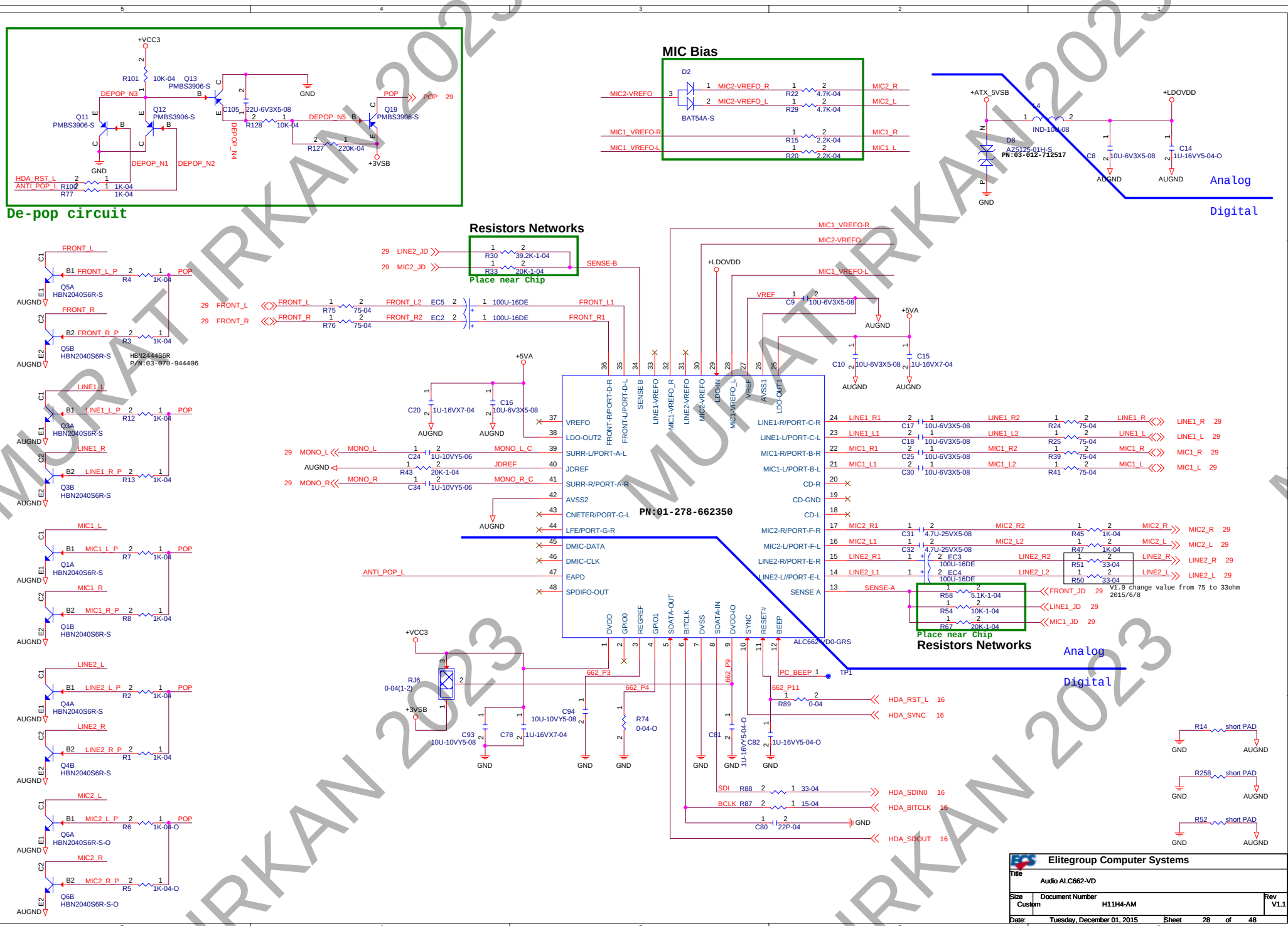

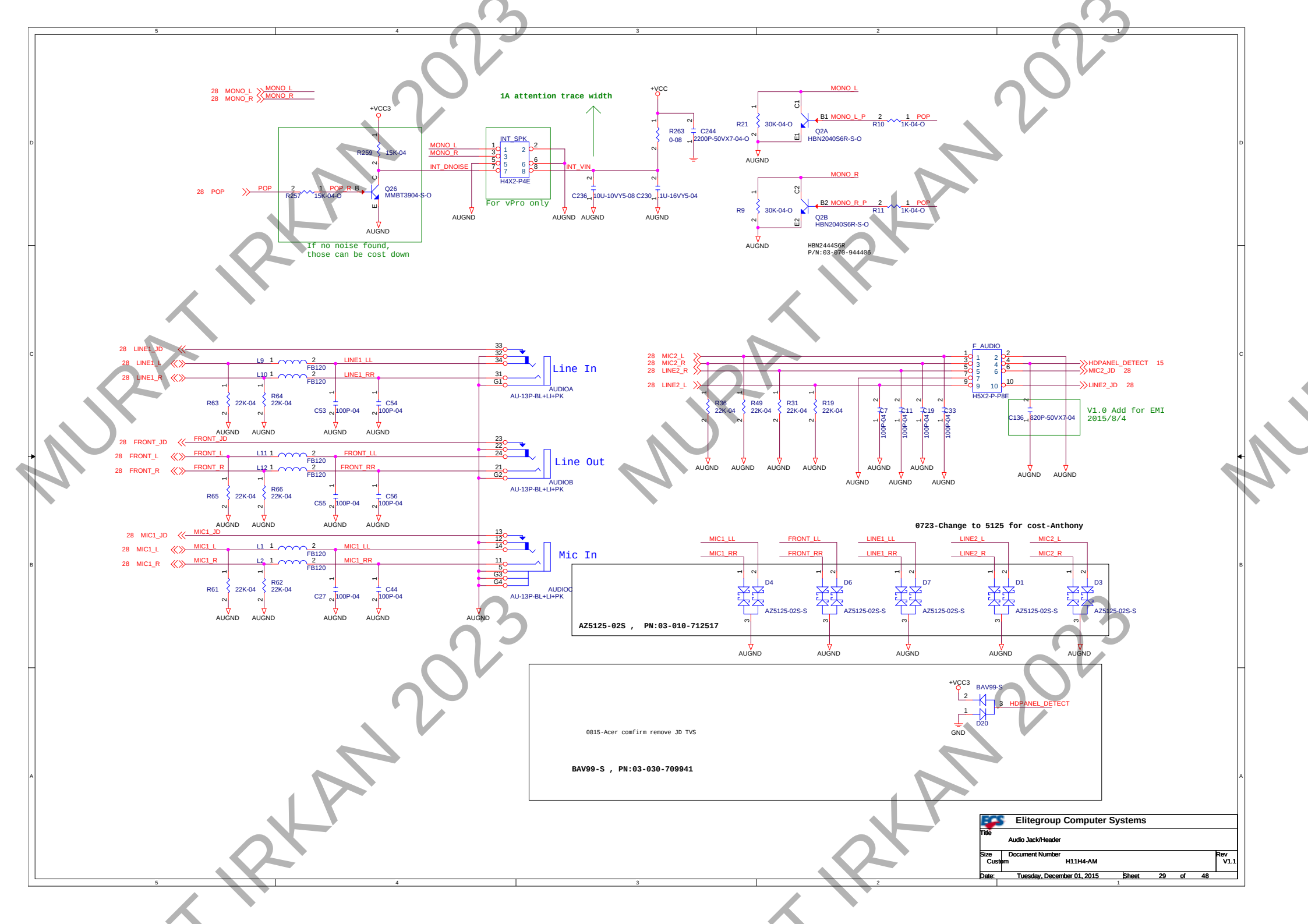

Elitegroup Computer Systems

Title	Audio Jack/Header		
Size	Document Number		Rev
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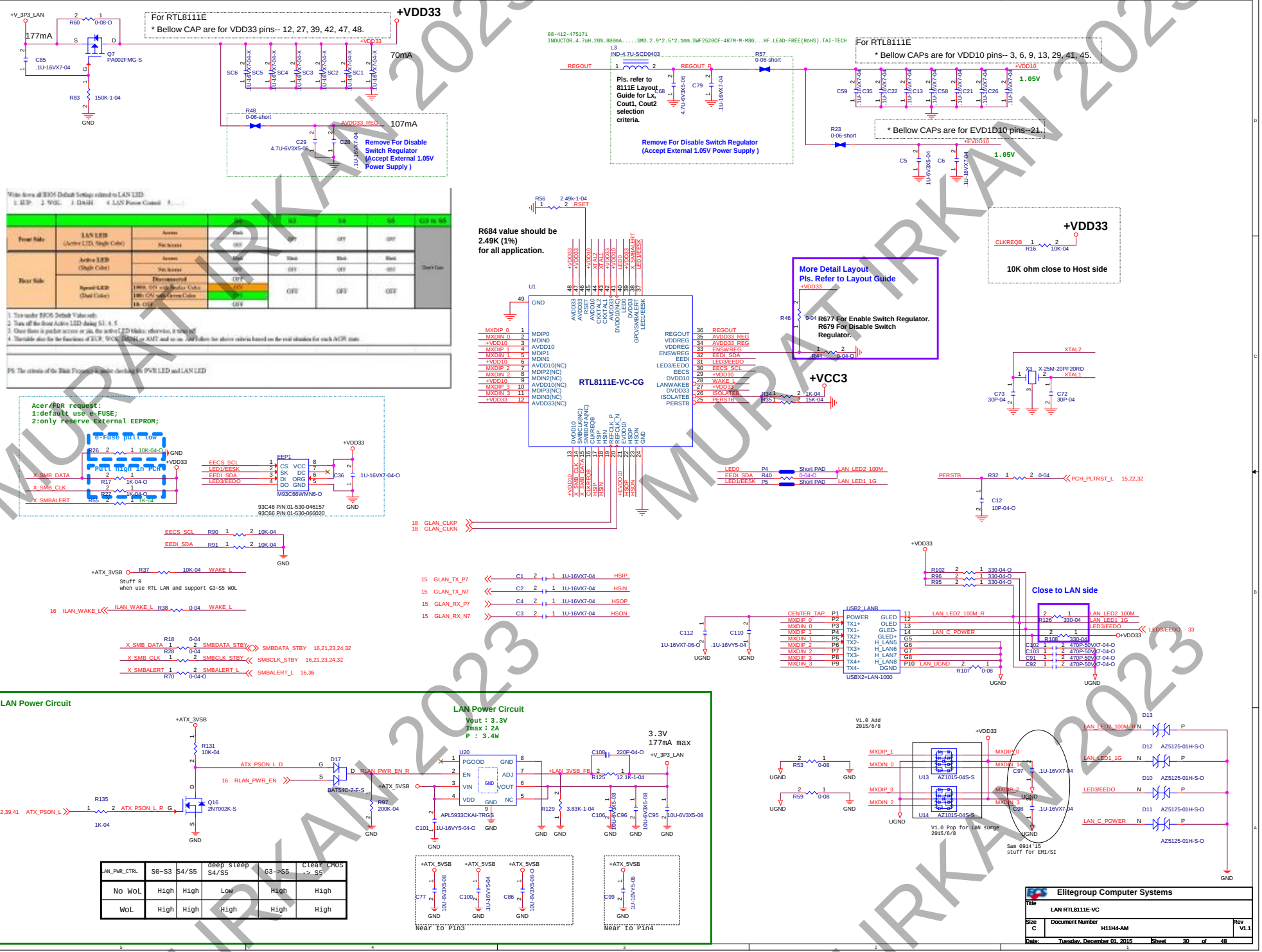

Elitegroup Computer Systems			
Title: Reserved			
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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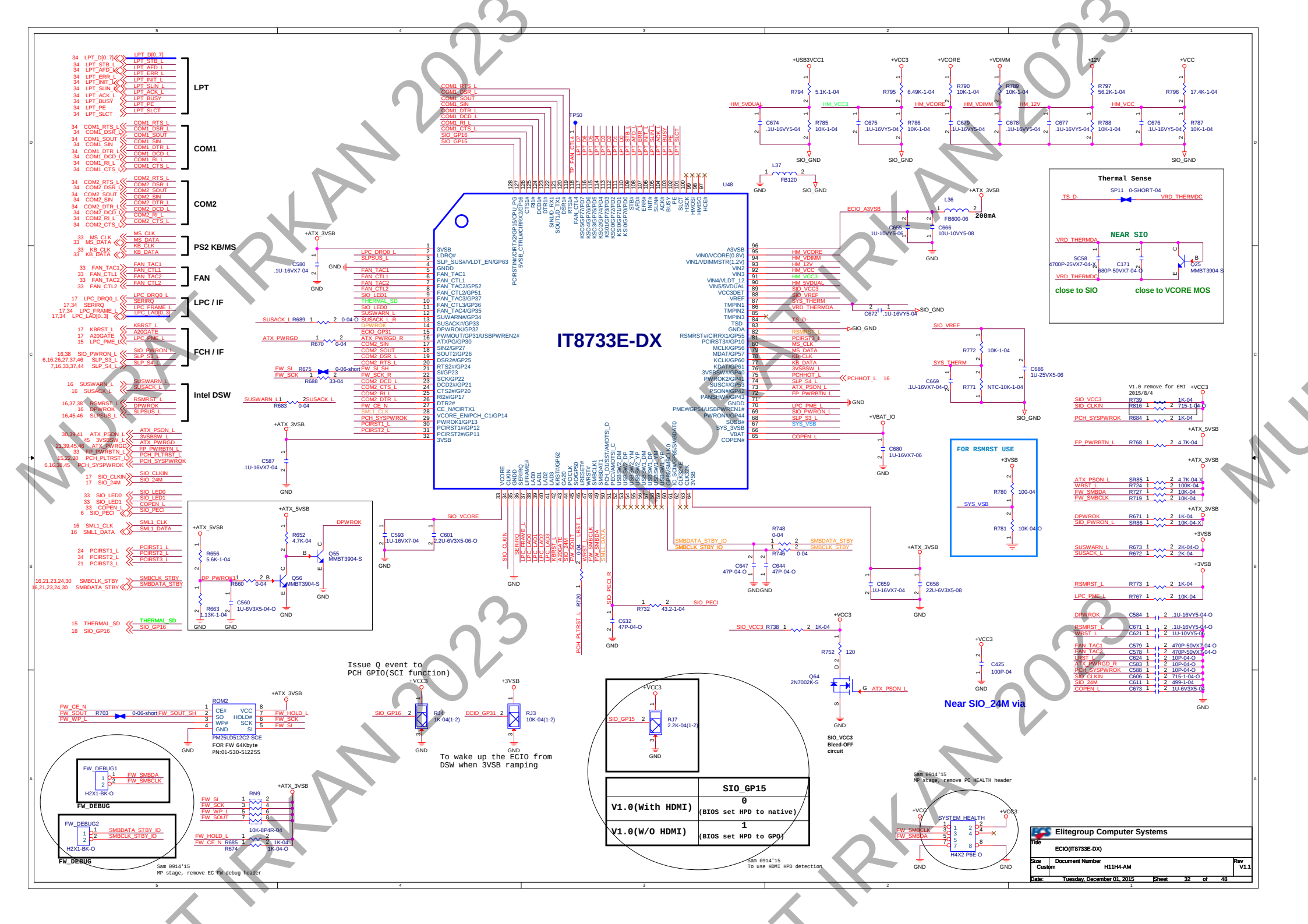
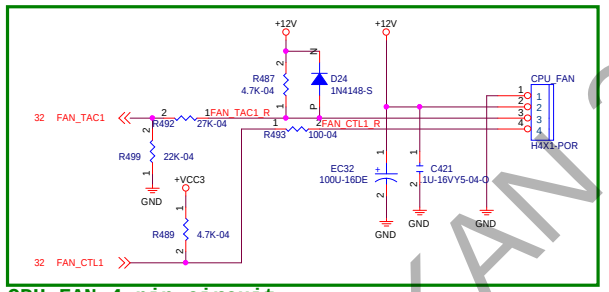
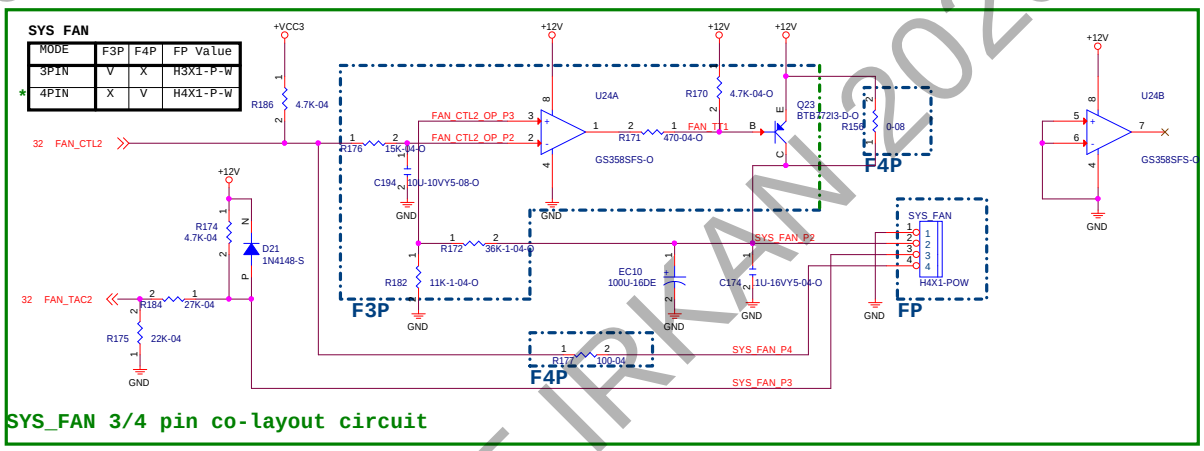


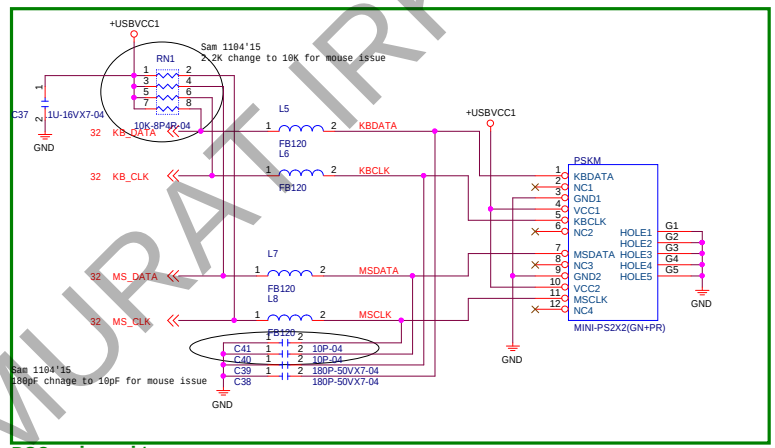
	SIO_GP15
V1.0(With HDMI)	0 (BIOS set HPD to native)
V1.0(W/O HDMI)	1 (BIOS set HPD to GPO)



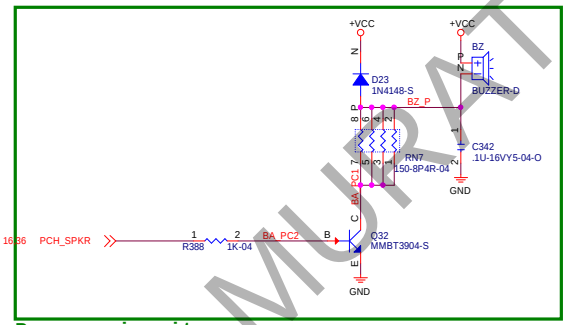
CPU_FAN 4 pin circuit



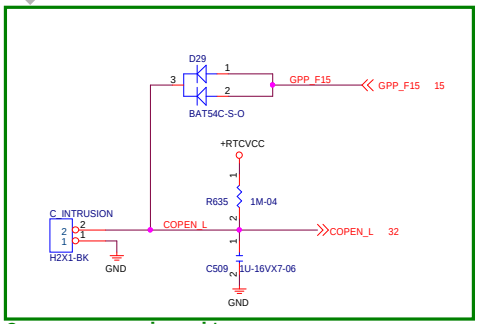
SYS_FAN 3/4 pin co-layout circuit



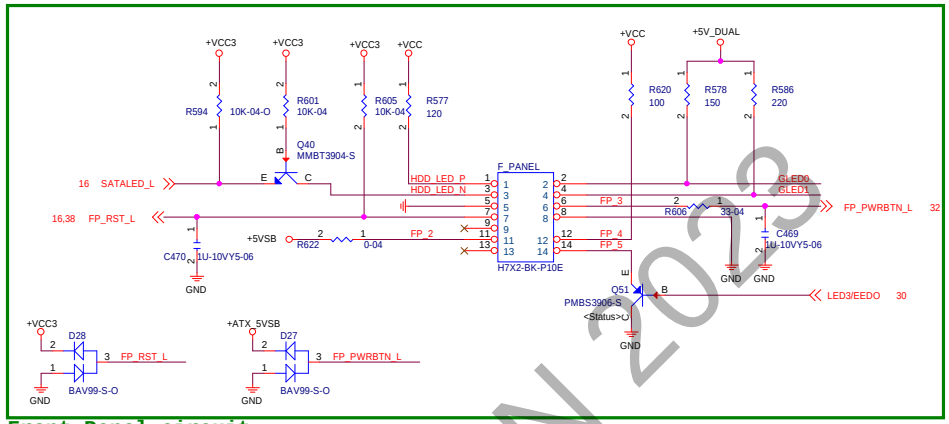
PS2 circuit



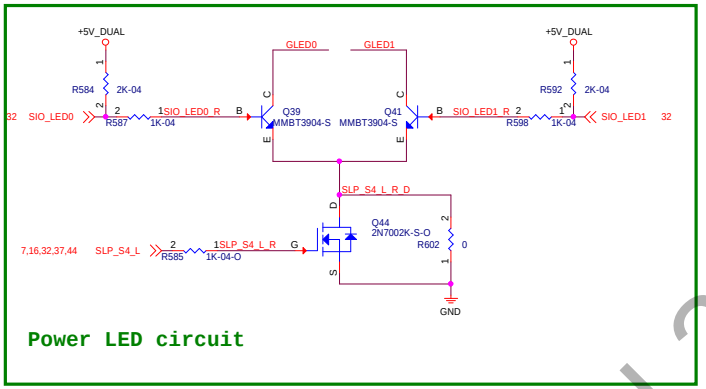
Buzzer circuit



Case open circuit



Front Panel circuit



Power LED circuit

Elitegroup Computer Systems			
Title: FAN/Buzzer/PS2/Front Panel			
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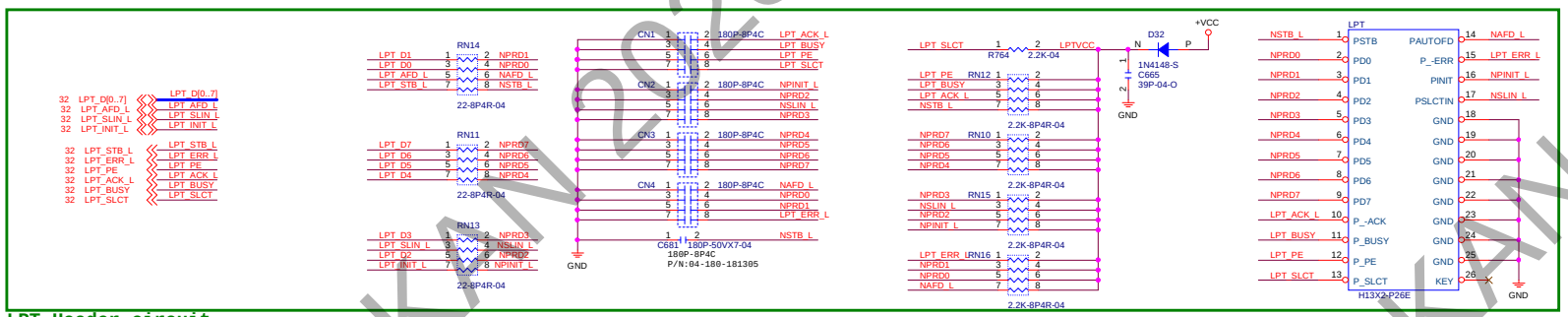
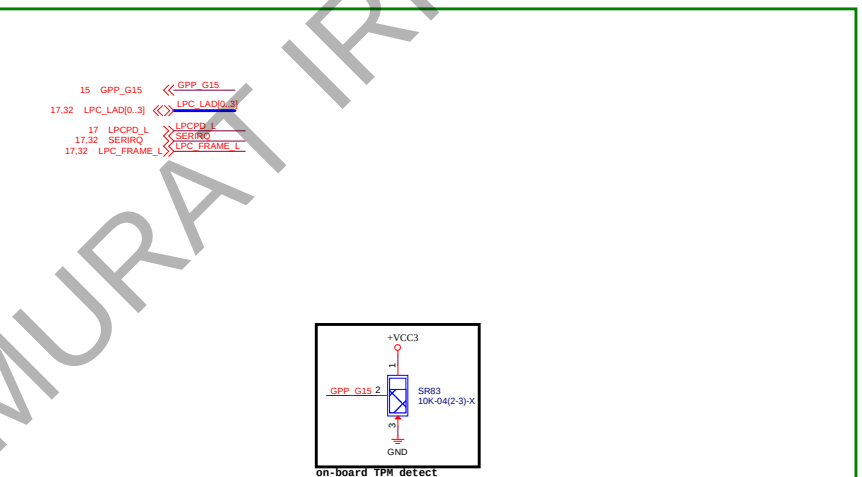
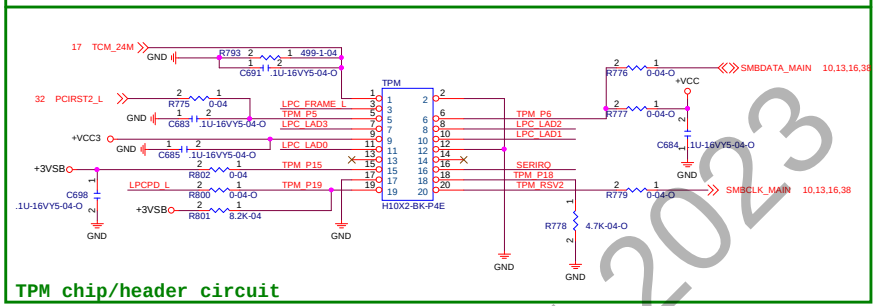
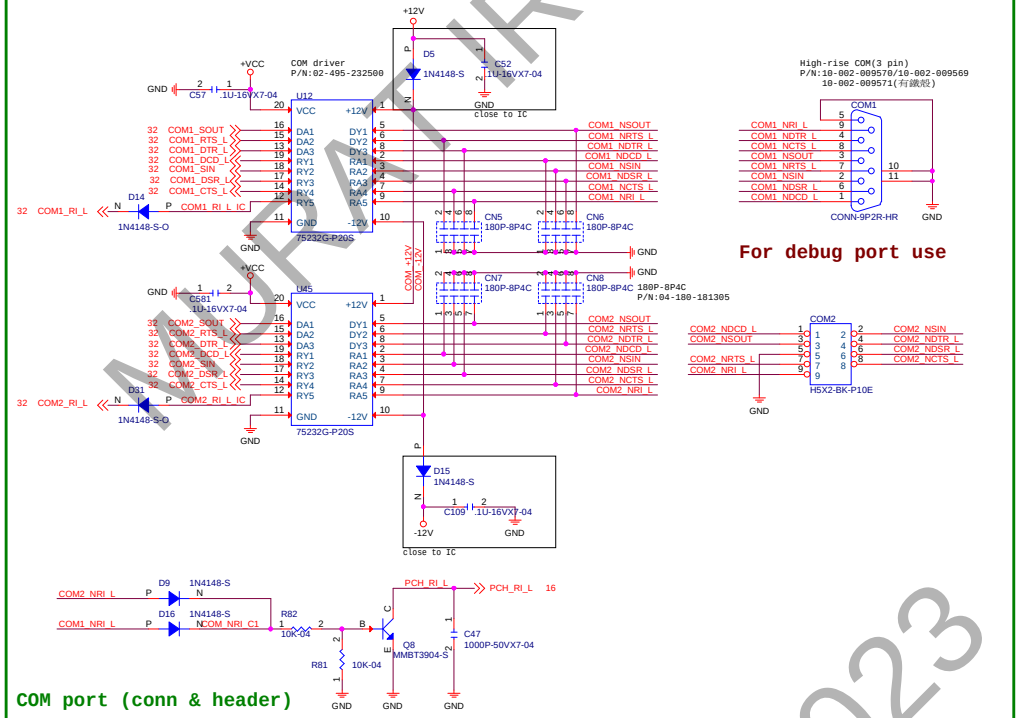


LPT Header circuit





TPM chip/header circuit



COM port (conn & header)

Elitegroup Computer Systems		
Title: TPM/TCM/LPT/COM/Asset ID		
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15,36,38 SPI_MOSI
15,36 SPI_MISO
SPI_MOSI R474 2 1 0-04 SPI_MOSI0
SPI_MISO R451 2 1 0-04 SPI_MISO0

15 SPI_CLK
SPI_CLK R455 2 1 0-04 SPI_CLK0

15 SPI_CS_L0
SPI_CS_L0 1 2 ROM_CS_L0
R463 0-04

Re

Sam 0914'15
In MP stage, remove SPI debug header

SPI_MOSI0 C419 2 12P-04-O
SPI_MISO0 C418 2 12P-04-O
ROM_CS_L0 C414 2 12P-04-O
C420 12P-04-O
GND

SPIROM1
ROM_CS_L0 1 CS# VCC 8
SPI_MISO0 2 SO HOLD# 7
SPI_IO2_0 3 WP# SCK 6
4 GND SI 5
SPI-64M-WINBOND
GND

+SPI_3P3V
SPI_IO3_0
SPI_CLK0
SPI_MOSI0

C426 2 10U-10VY5-08 C427 2 1U-16VX7-04
GND GND

close
ROM1

+SPI_3P3V
SPI_IO3_0 R462 2 1 1K-04
SPI_IO2_0 R472 2 1 0-04 SPI_WP

+3VSB
R501 short PAD
D25
BAT54C-S-O

+SPI_3P3V

A3 stuff BAT54C for debug and reserve 0 ohm
A4 0 ohm change to SH

SPI ROM

BIOS_WP JP-R(2-3)
BIOS_WP H3X1-R
GPP_E9 15
GND

BIOS WP Jumper:

MODE / WP	
BIOS WP	1-2
* NORMAL	2-3

+SPI_3P3V
R495 10K-04
SPI_WP
R504 0-04
Q34 PMBS3906-S-O
<Status>
GPP_E10 15
GND

A

BIOS WP

Sam 0914'15
In MP stage, remove SPI debug header

Ra
Rc
Rb
Rd

SPI_MISO0 R456 2 1 0-04-O

SPI_DEBUG
ROM_CS_L0
SPI_CS_L0
SPI_MISO0_R
SPI_WP
+SPI_3P3V
SPI_IO3_0_R
SPI_CLK0
SPI_MOSI0_R
H6X2-BK-P2E-P1.27-O
GND
6*2 SMD header
PN:10-382-012820

R458 2 1 0-04-O
R449 2 1 0-04-O
SPI_IO3_0
SPI_MOSI0

SPI_DEBUG
JP-P1.27(1-3)-O
1.27mm jumper
PN:10-611-002144

	Ra	Rb	Rc	Rd	Re
A3~A5	0	0	0	0	X
MP	X	X	X	X	0

Title	SPI ROM		
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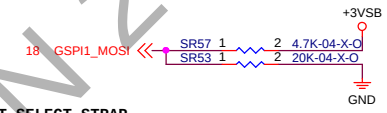
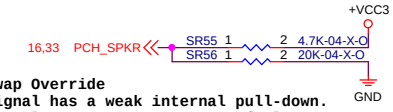
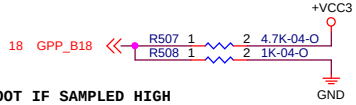


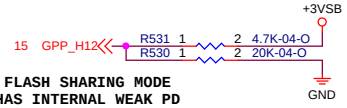
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



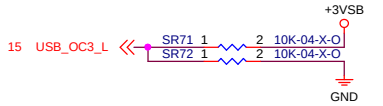
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



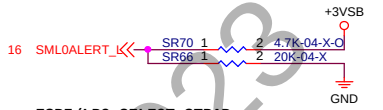
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING

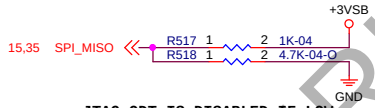


DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL

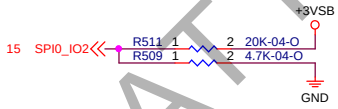


ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

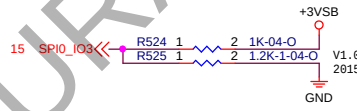
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



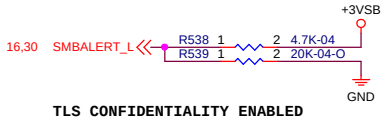
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



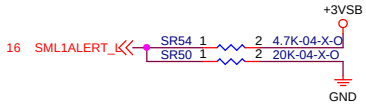
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1/ES2 only)



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD



EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

Title: Strap Pin		
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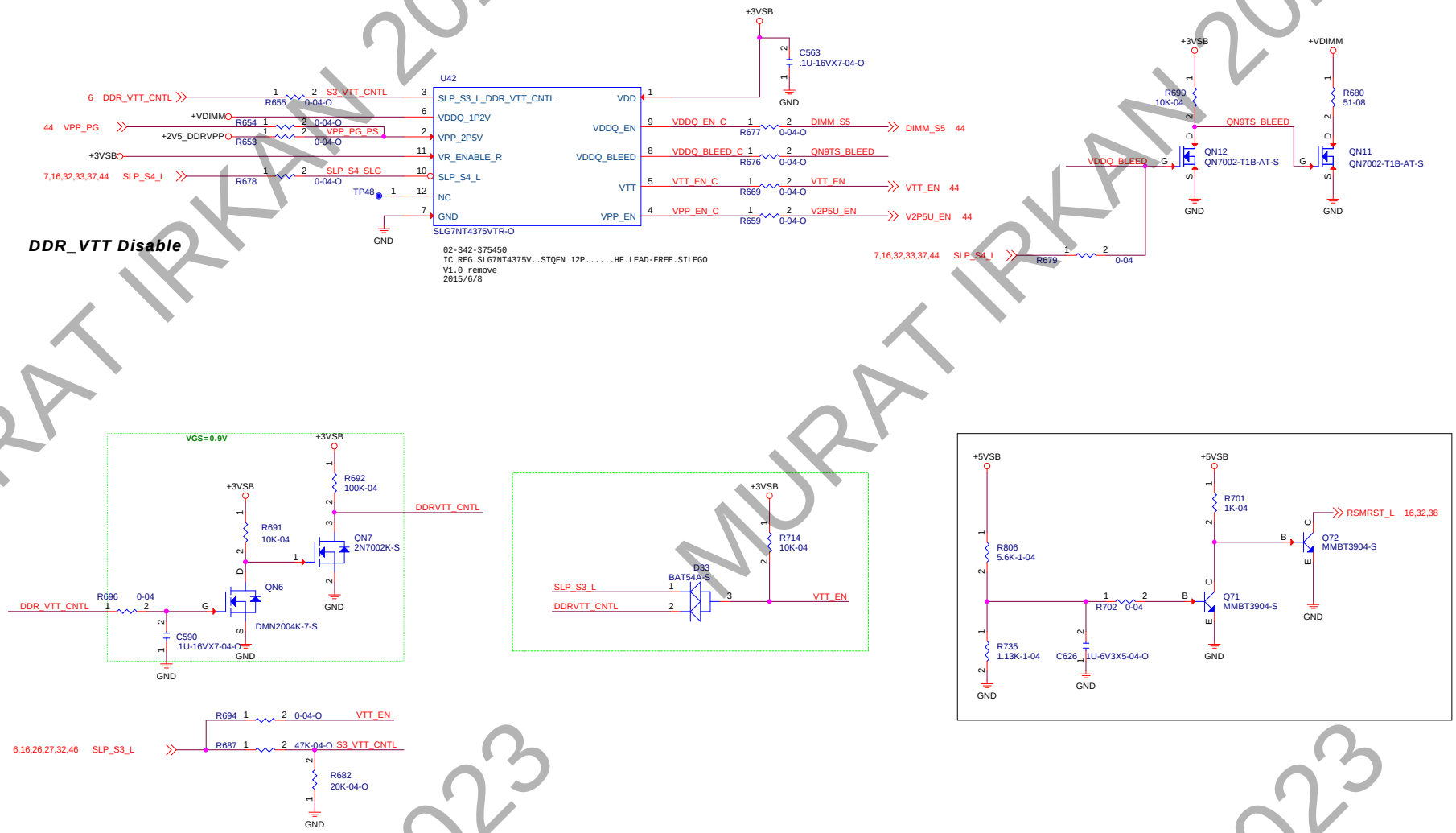
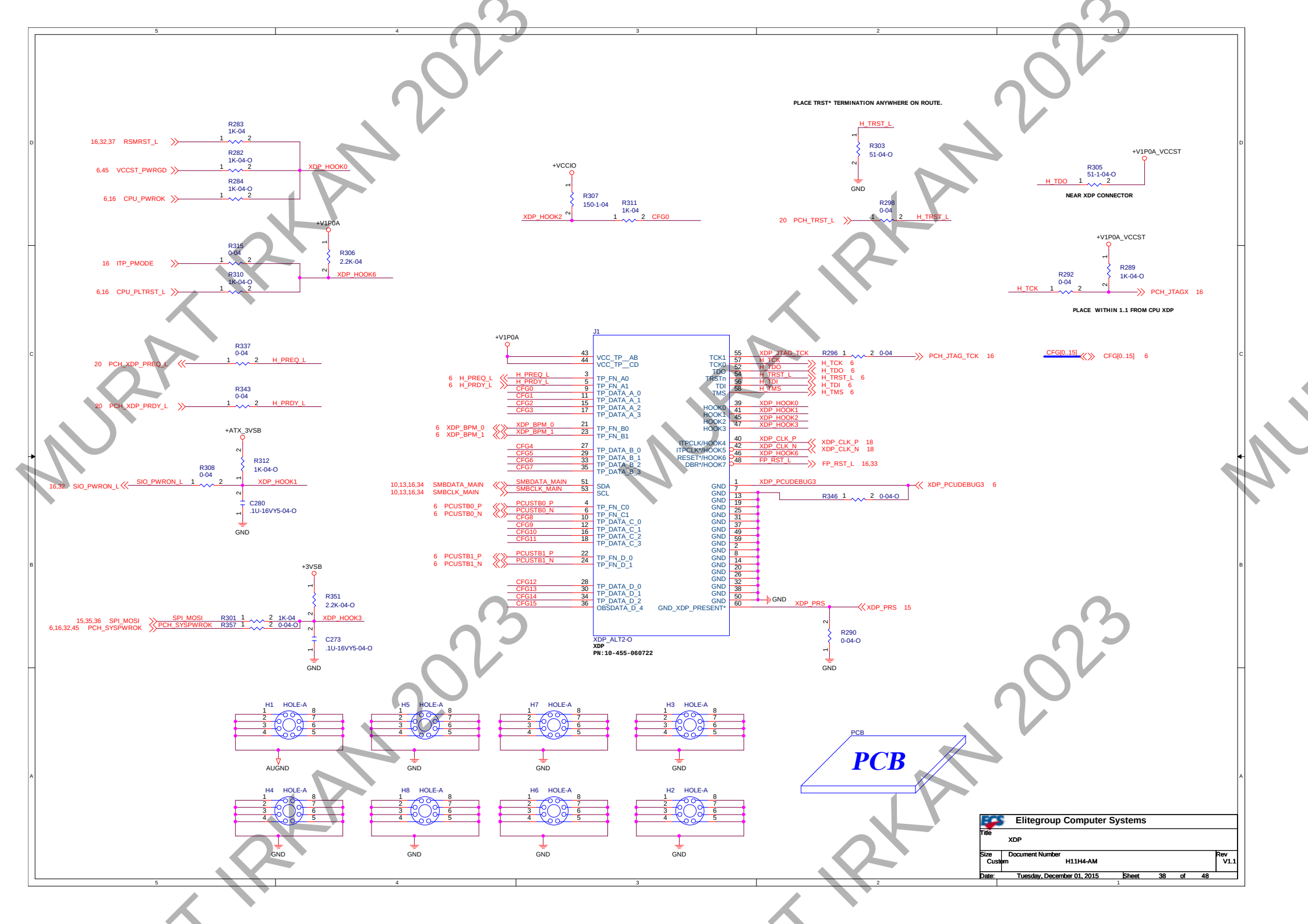
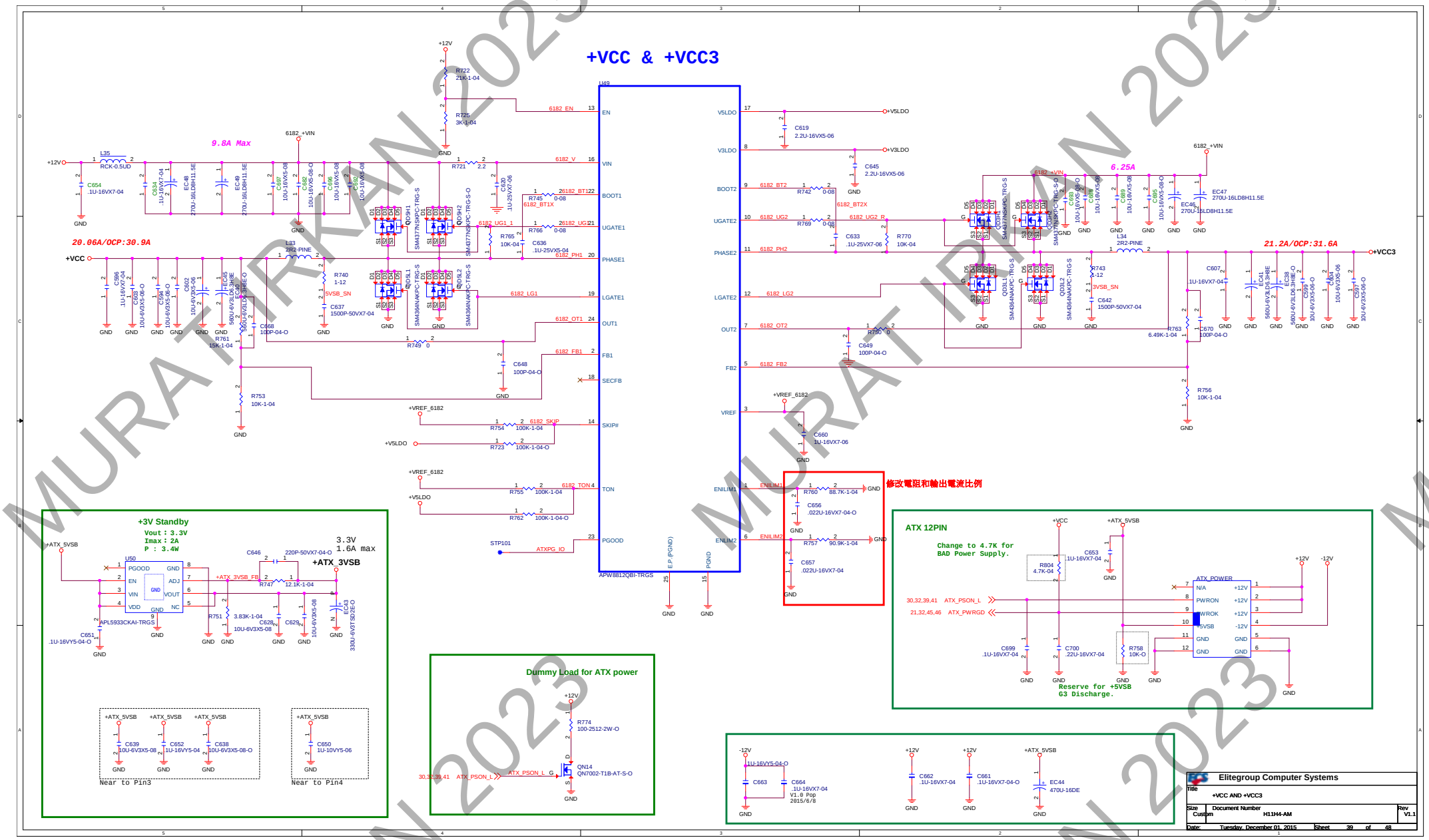
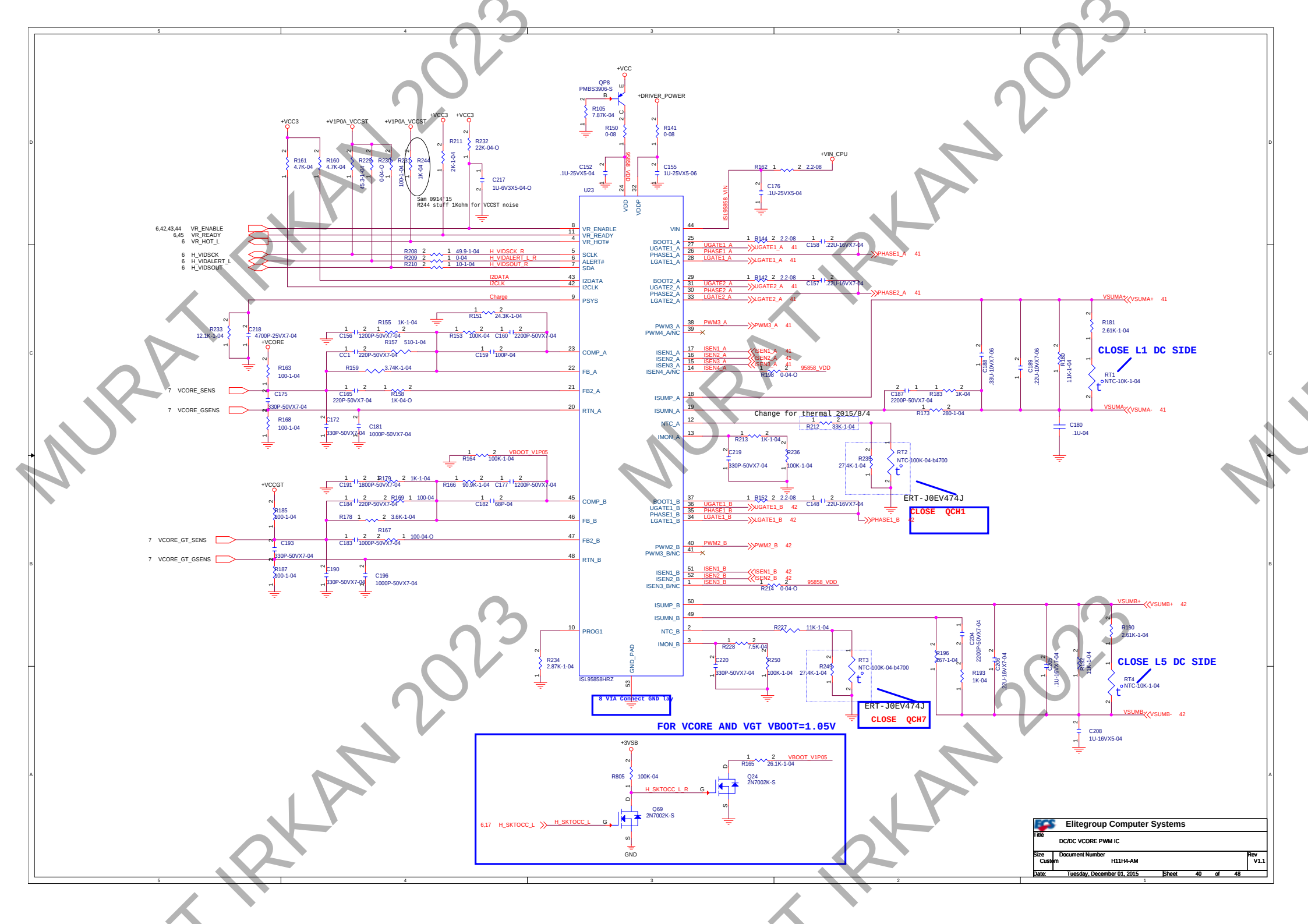
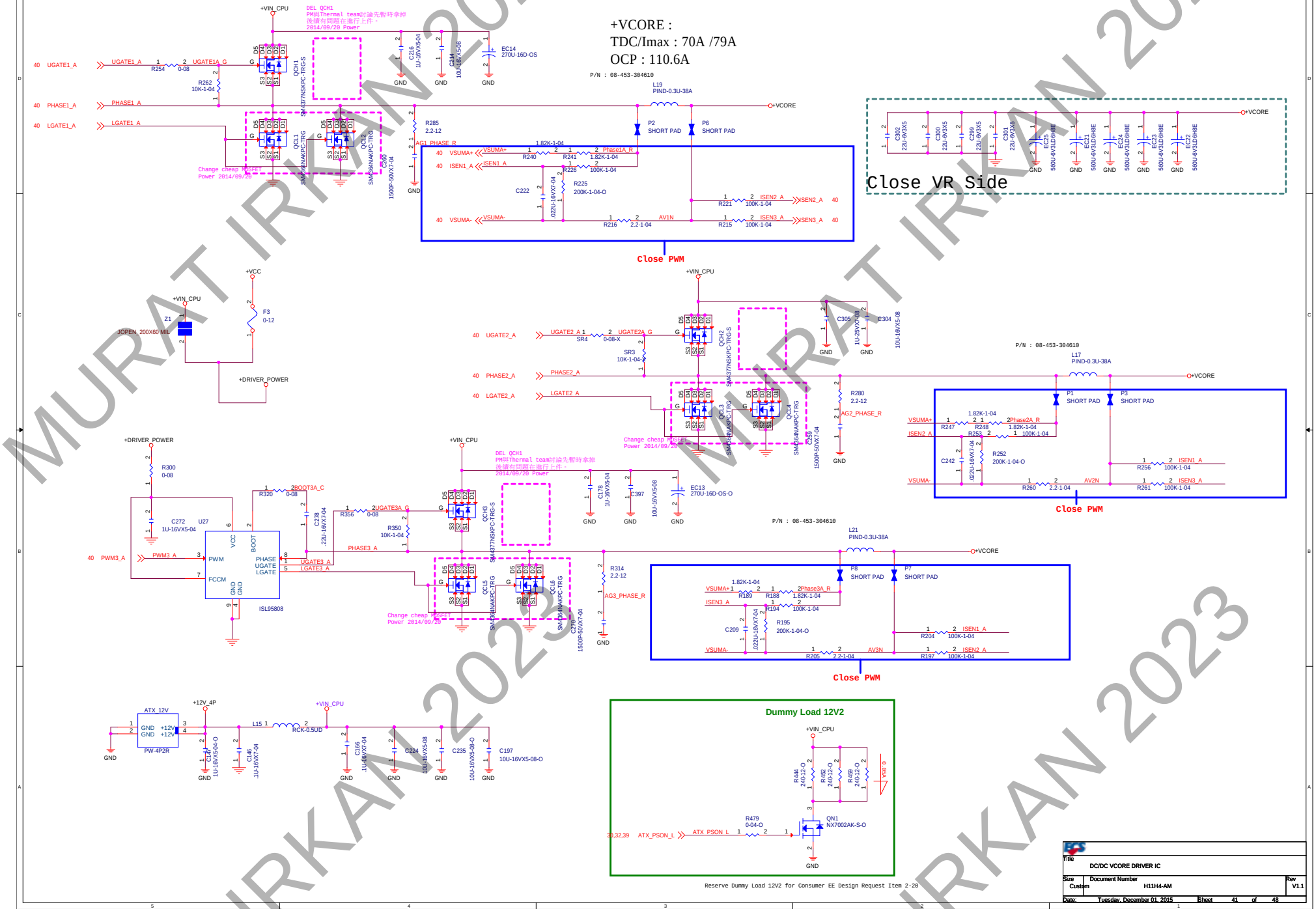
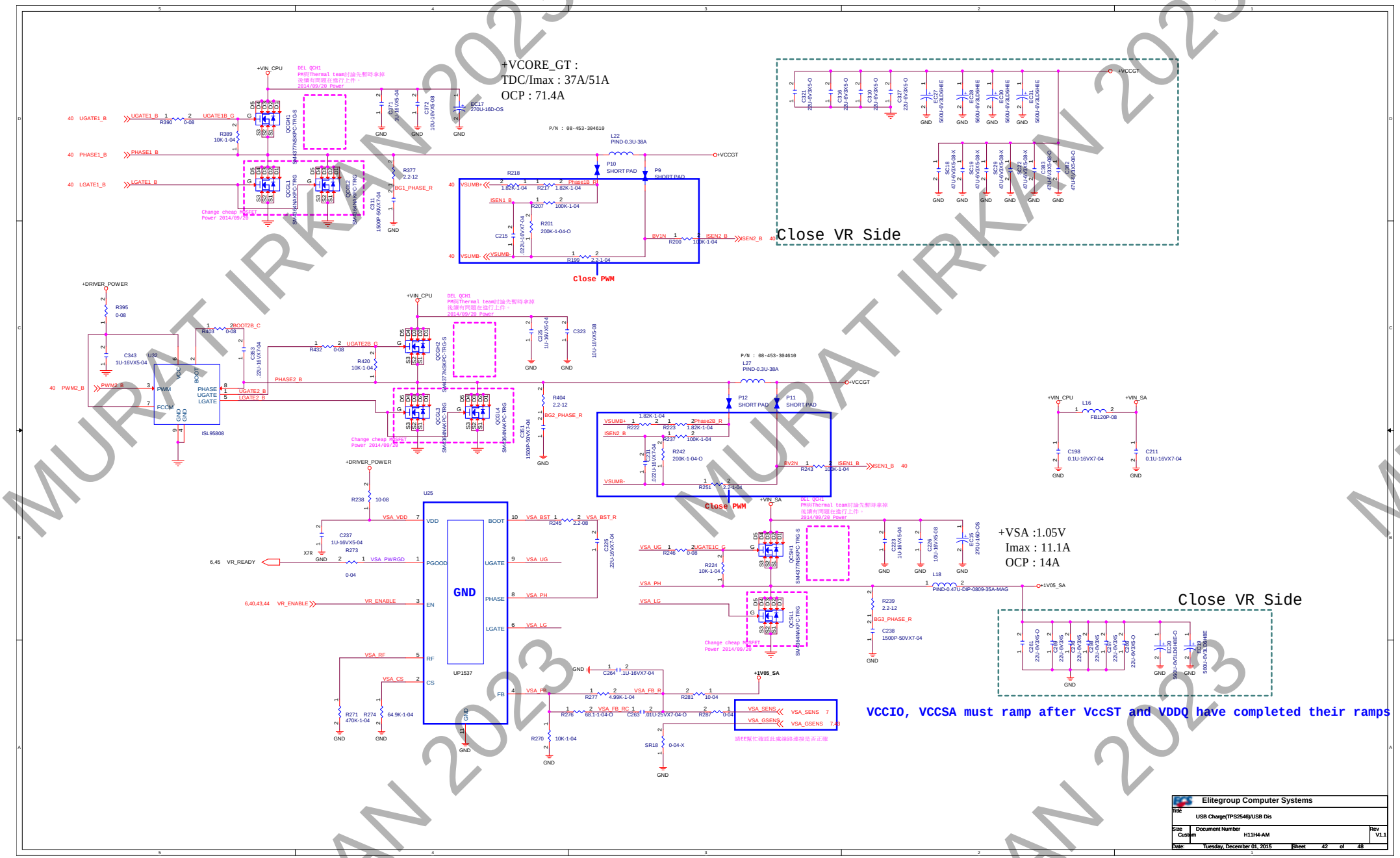


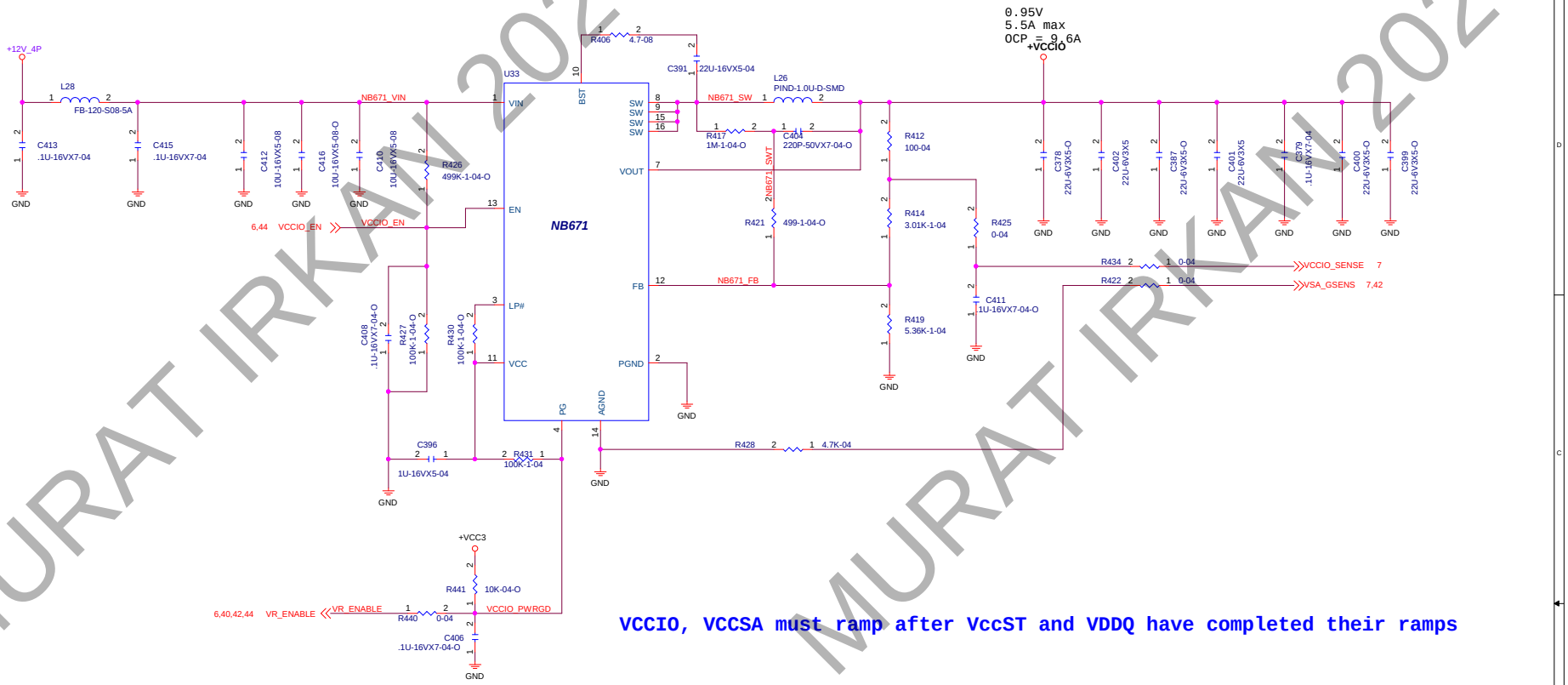






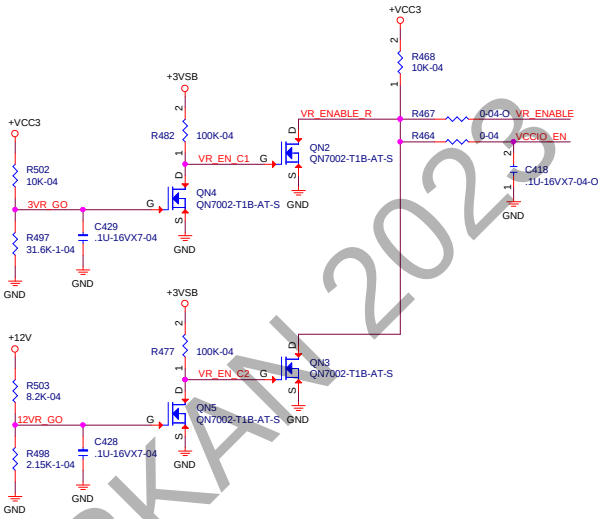






VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

VCCIO & VR ENABLE



Title	DC/DC VCCIO	
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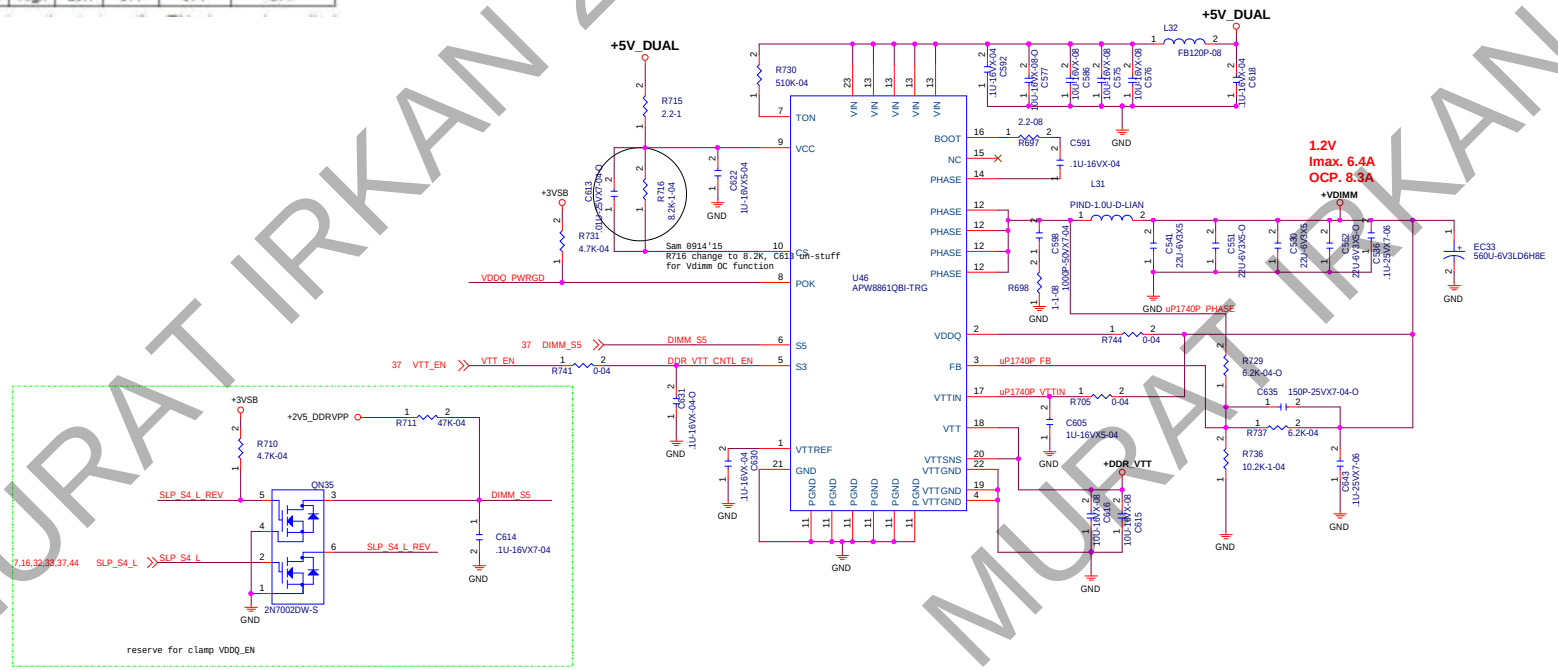
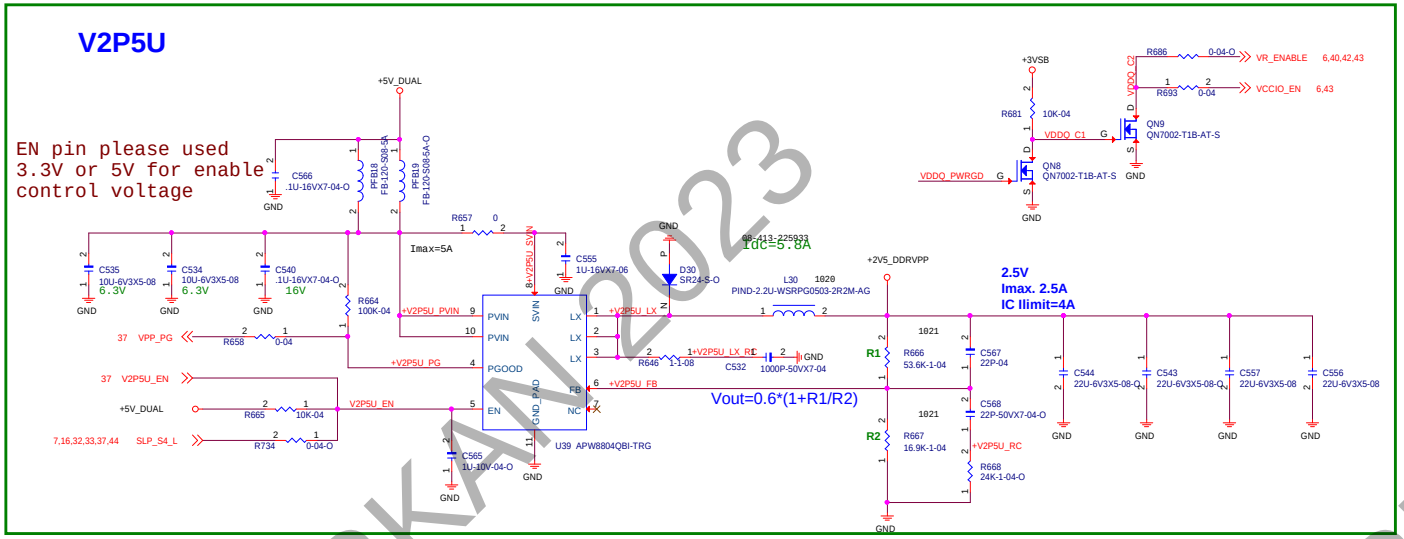
VDIMM Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



V2P5U

EN pin please used
3.3V or 5V for enable
control voltage



Title	DC/DC VDIMM & DDRVTT	
Size: Custom	Document Number: H11H4-AM	Rev: V1.1
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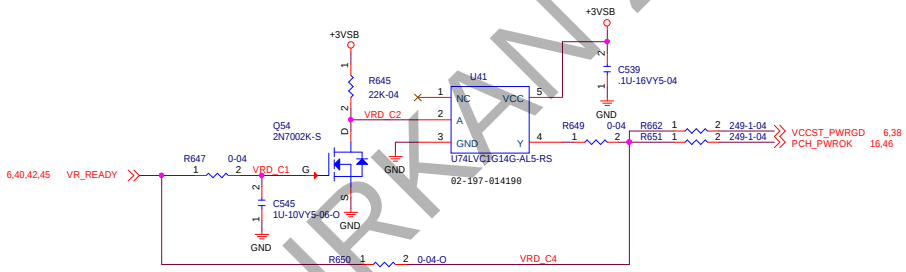
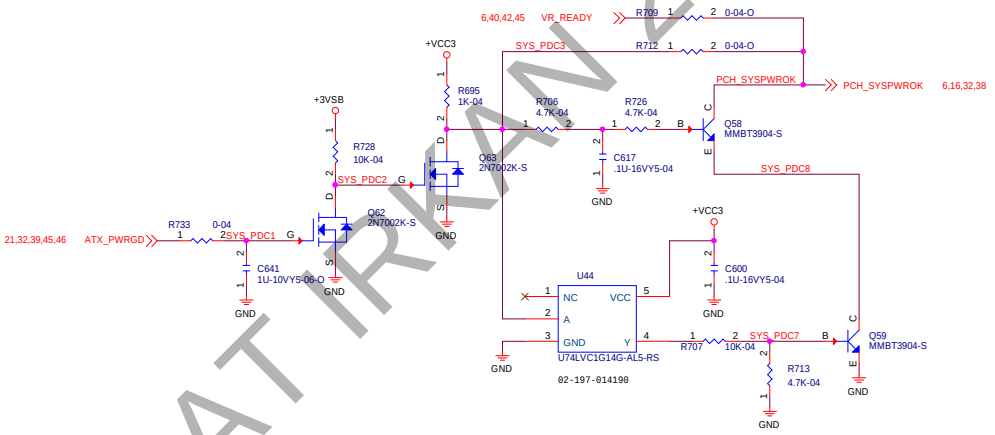
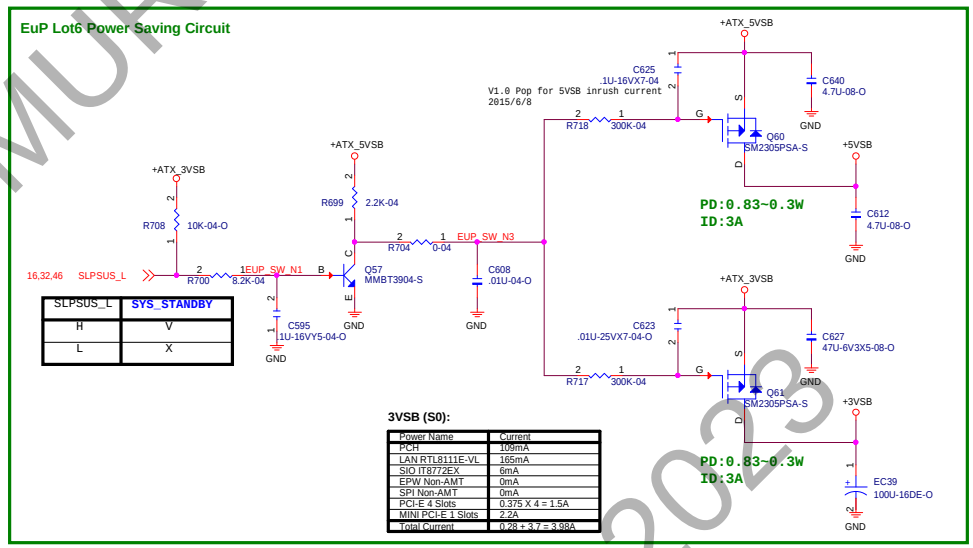
PCH & VCCST PWROK



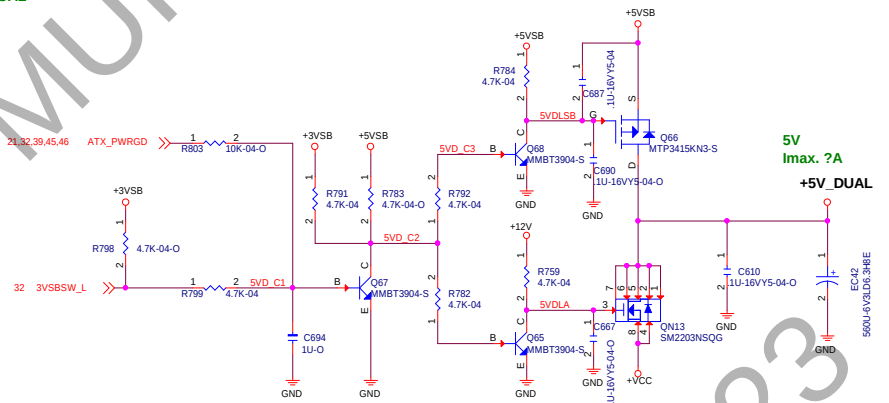
SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit



5VDUAL



Title	DC/DC DDRVPP & 5VDUAL
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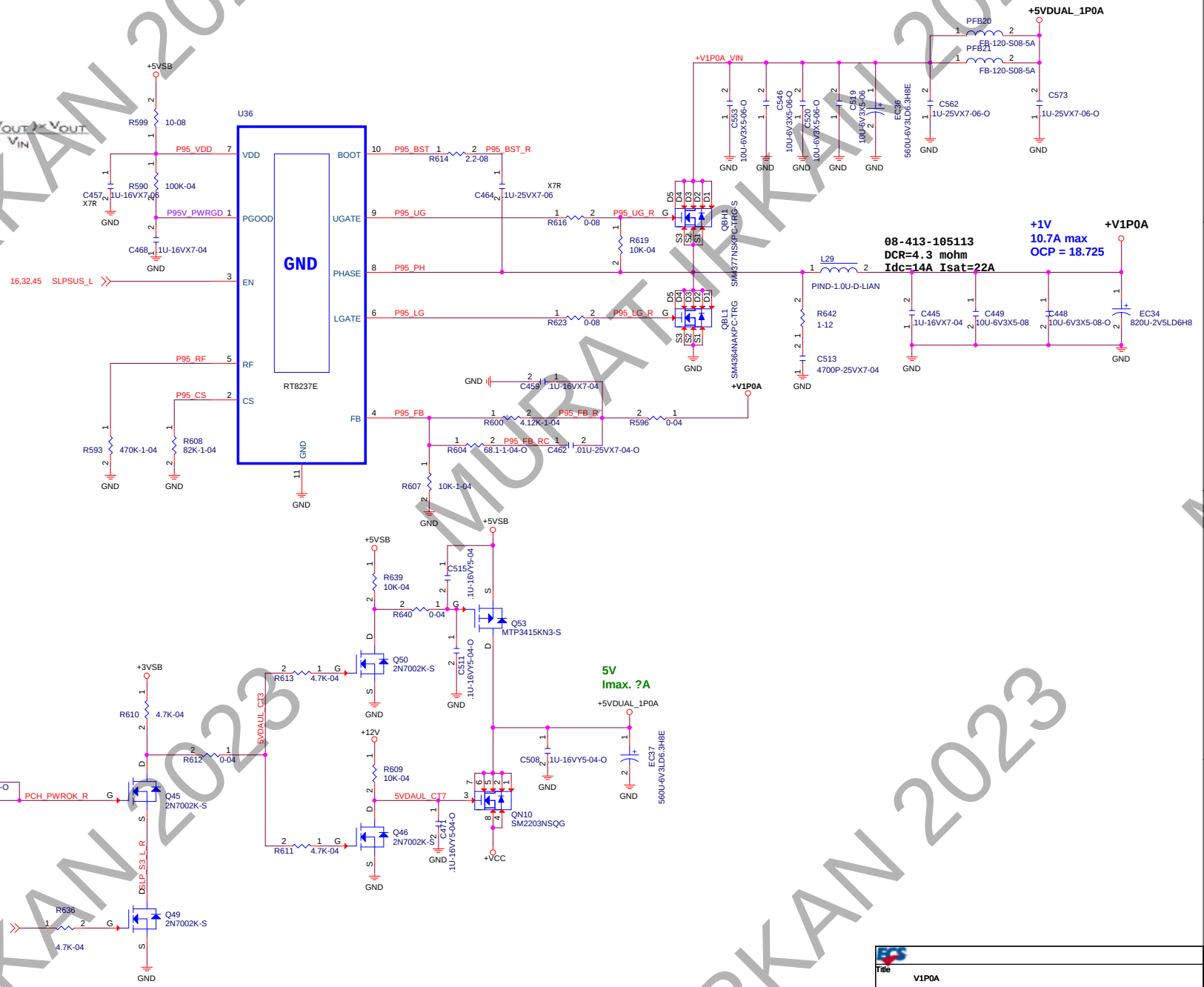
V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



Title	V1P0A		
Size: Custom	Document Number: H11H4-AM		Rev: V1.1
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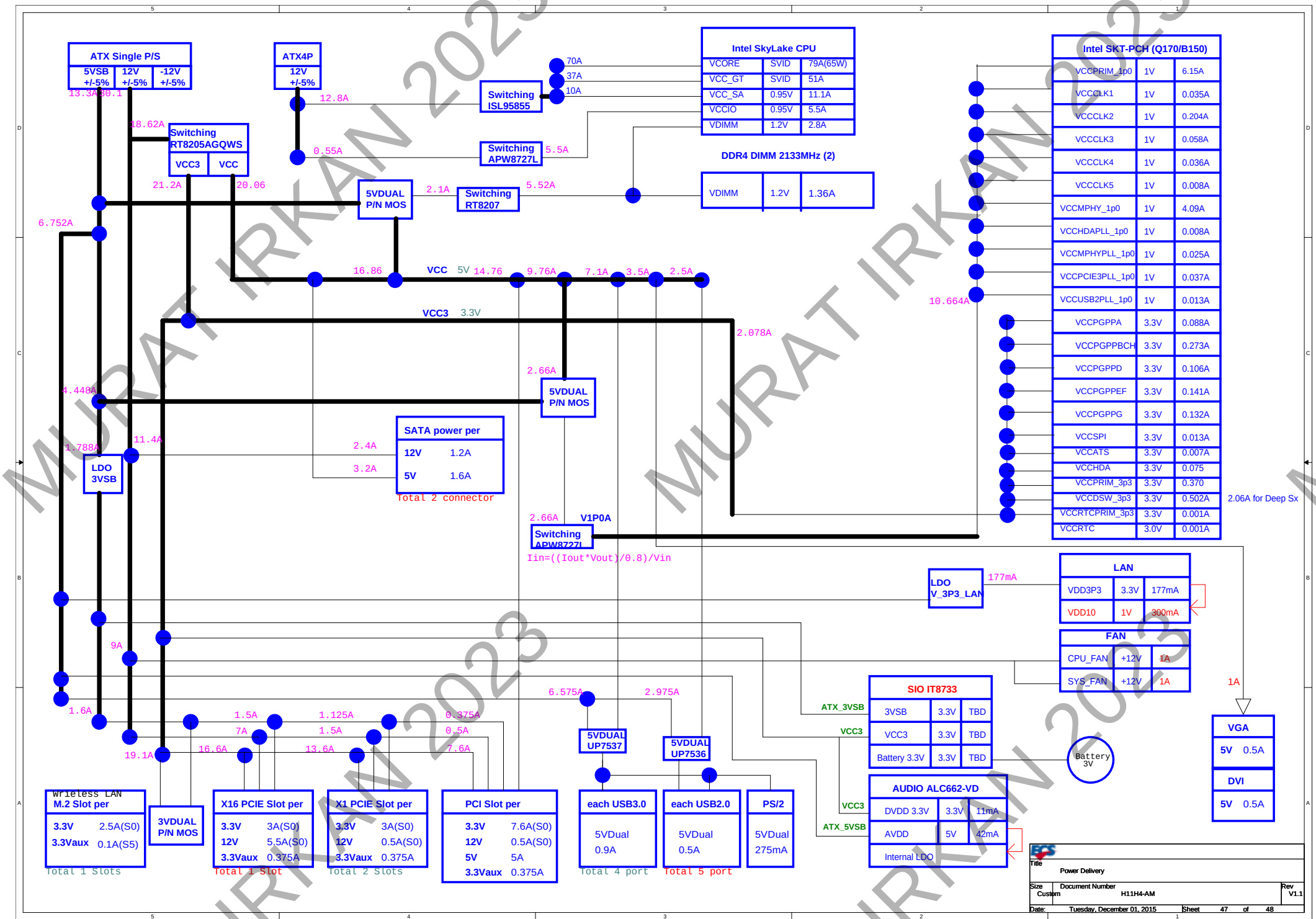


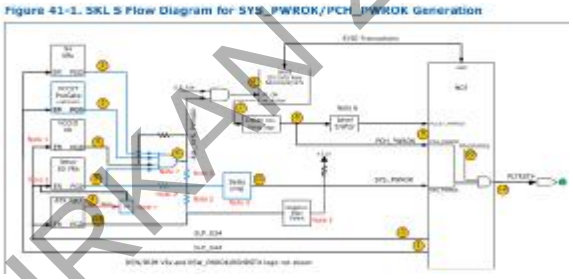
5 SLP4_L → +V1P0A_VCCST
+VDIMM

8.2 +VCC3 → +VCCIO
PGOOD[10]
9 → +1V05_SA
ISL95855HRTZ
VRDY[6]
10

PCIe X1 Slot_2
PCIe X16 Slot
PCIe X1 Slot_1
NGFF (For SSD)
NGFF (For WLAN & BT module)
TCM HEADER TPM module

13 SIO_PCIRST1_L
13 SIO_PCIRST2_L
13 SIO_PCIRST2_L

Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation



30 PCIRST1# | 31 PCIRST3# | 81 PCIRST2#
PANSHW#[72] | LRESET#[34]
RSMRST#[82]
SUSB#[68]
3VSB[32] | PWRON#[69]
ATXPG[16] | VIN[2:3] [92],[93] | PWROK1[29] | PSON#[73]

Super I/O IT8733E-DX

3 FP_PWRBTN_L
POWER BUTTON

1 +3VSB
9 ATX_PWRGD

13 PCH_PLTRST_L
RSMRST# de-actives delay 75ms from SYS_3VSB
2 RSMRST_L
5 SLP3_L
4 SIO_PWRBTN_L
11 PWROK1
Delay Logic 150ms

PCH_PWROK[AW11]
PLTRST#[BB27]
RSMRST#[BA11]
SLP_S3#[AW15]
PWRBTN#[AT13]
SYS_PWROK[AY1]
PLTRST_CPU#[AK2]
PROCPWRGD[AM3]
PCH-H

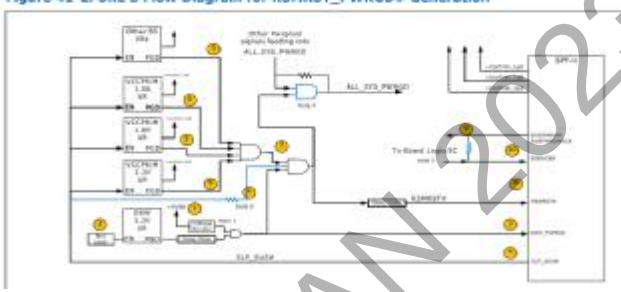
CPU_PLTRST_L
12 PROCPWRGD

RESET#[E7]
PROCPWRGD
S-processor

7.1 +12V
8.1 +VCC
7.2 +12V
6 PSON_L
8.2 +VCC3

MOS SWITCH
ATX Power 12V
5VSB to +3VSB LDO

Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



Title: Power Sequence MAP		
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