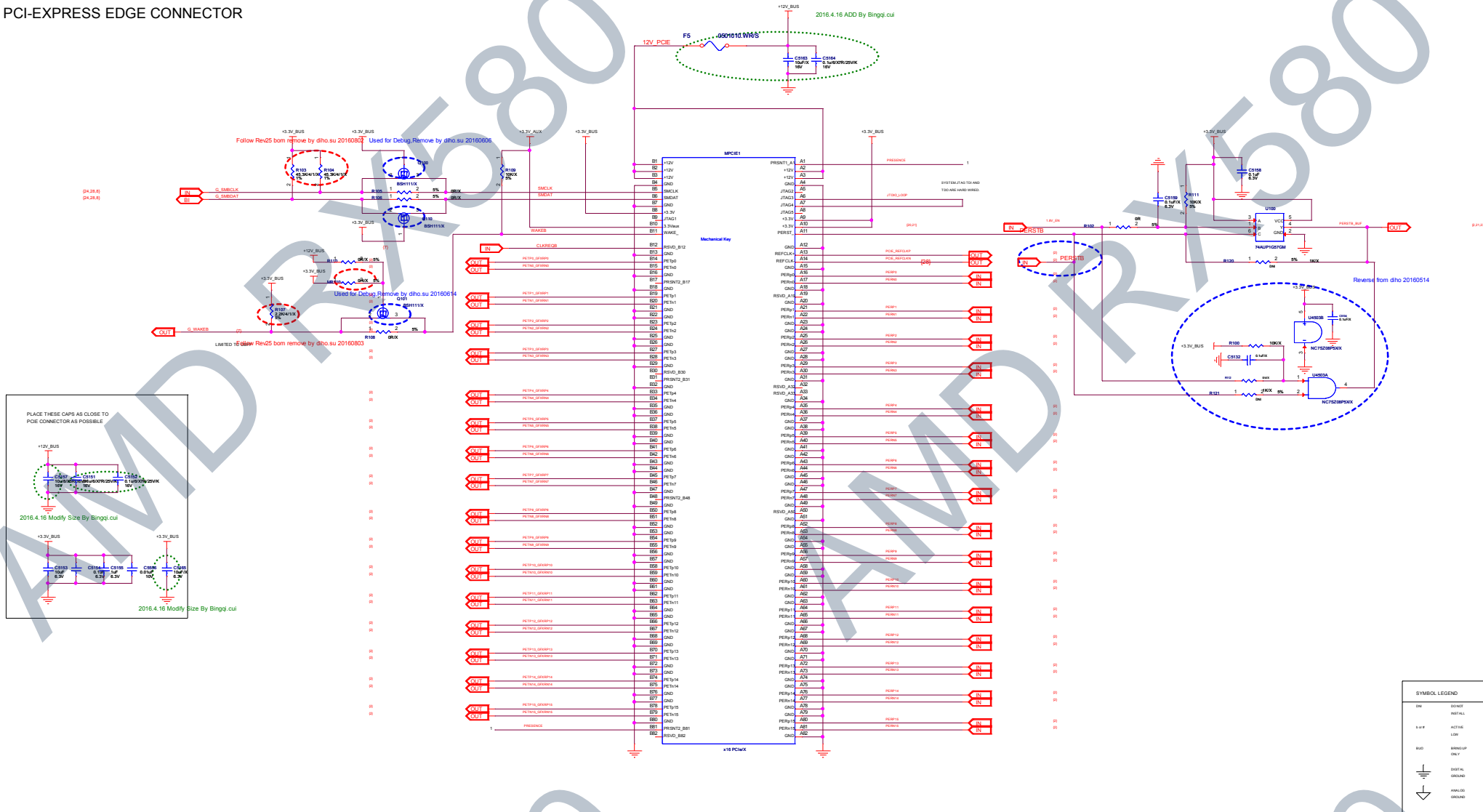


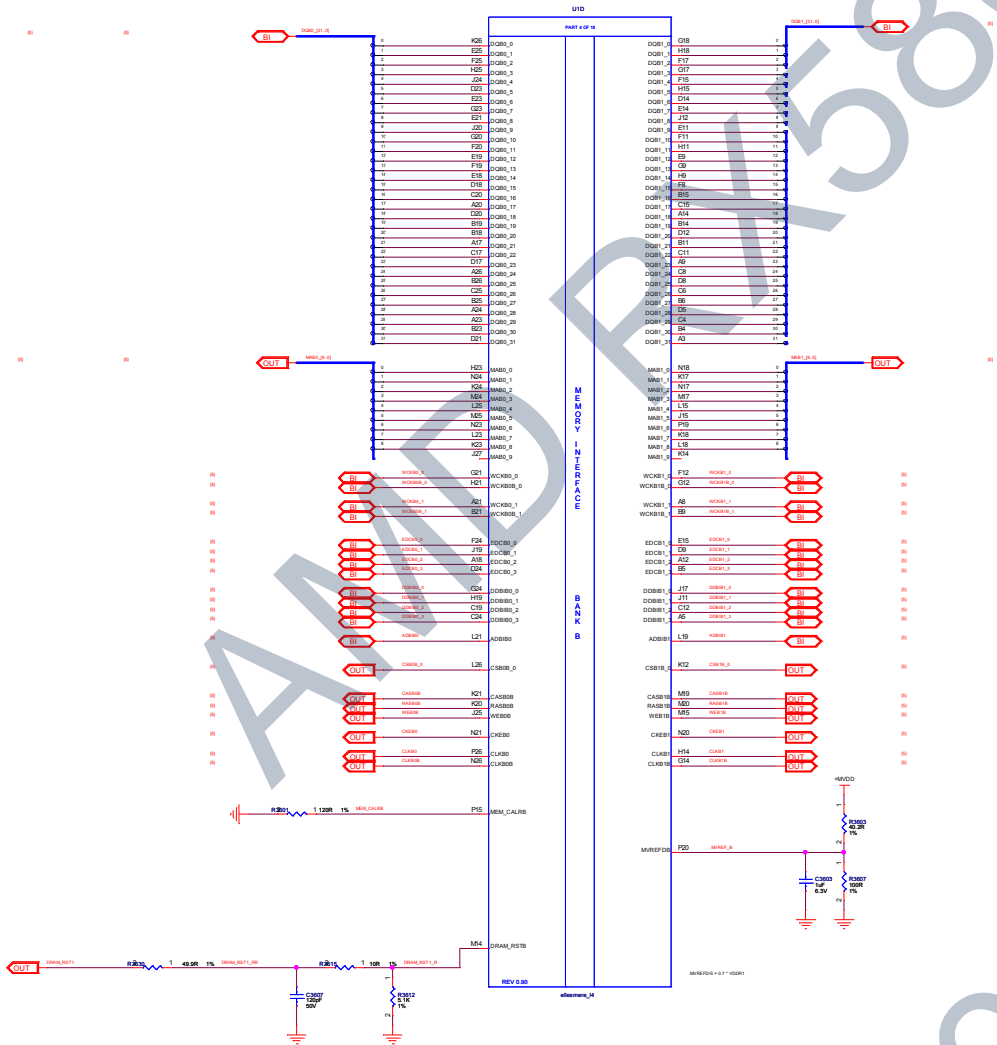
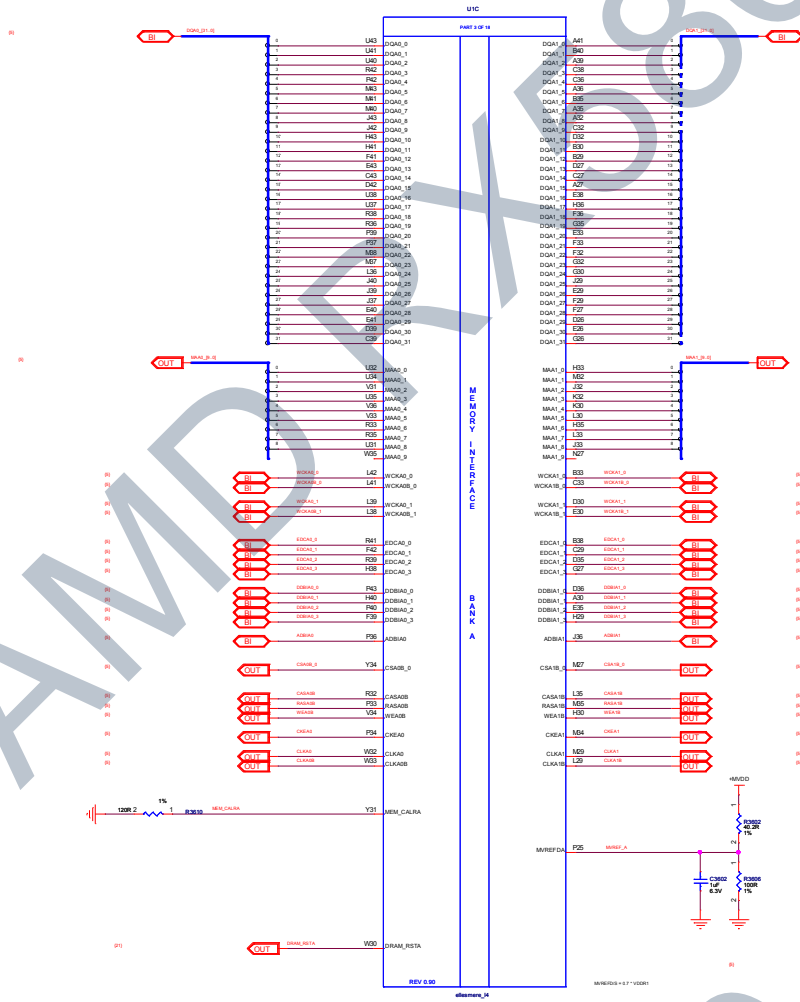
(1) PCI-EXPRESS EDGE CONNECTOR



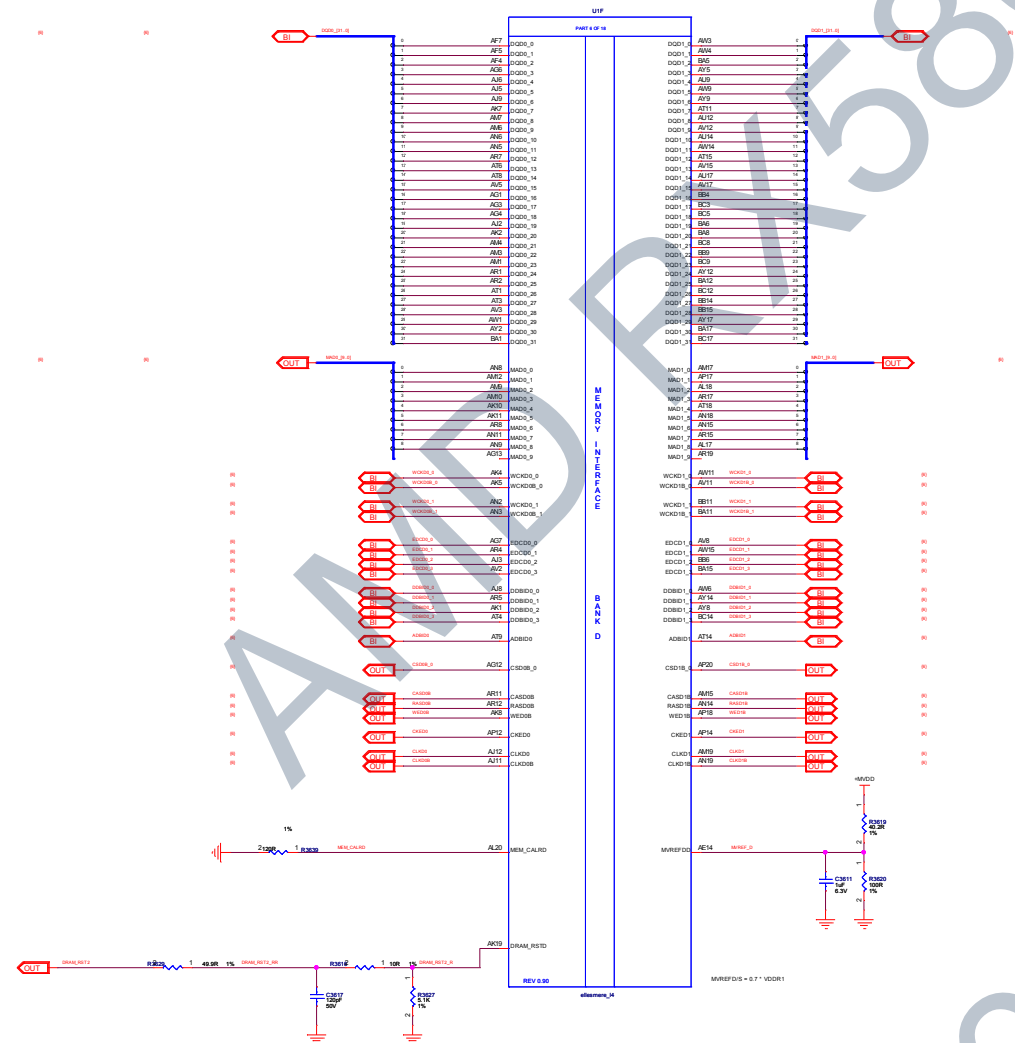
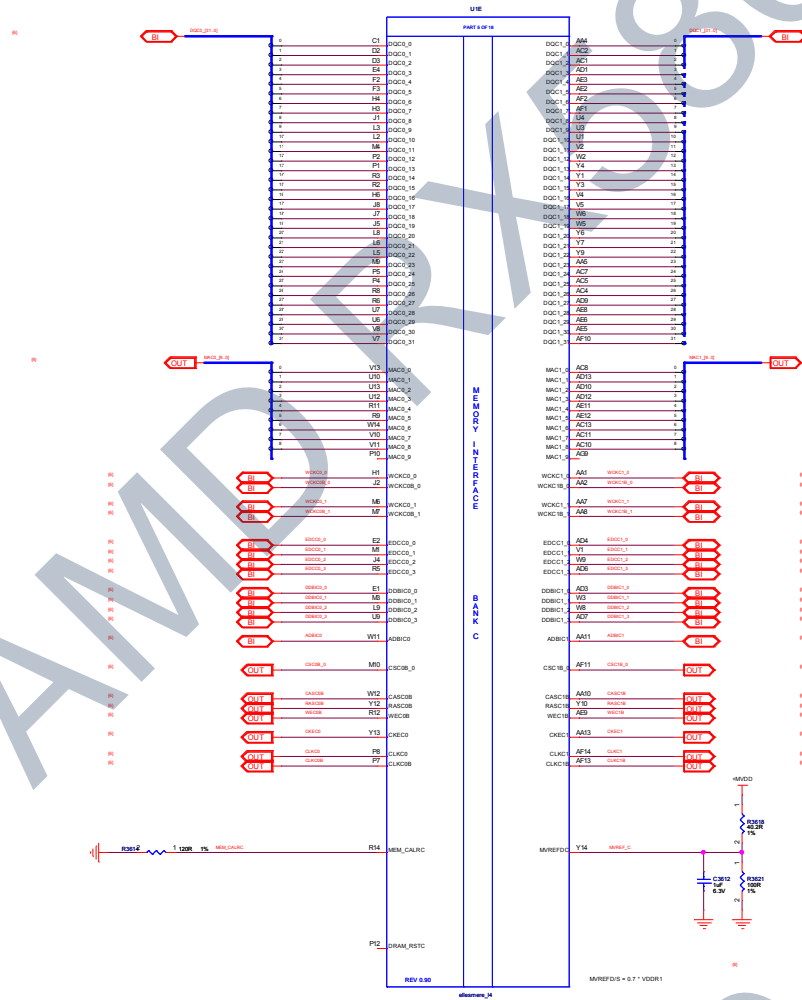
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Title <b>PCI Express</b>			
Size	Custom	Document Number	Rev
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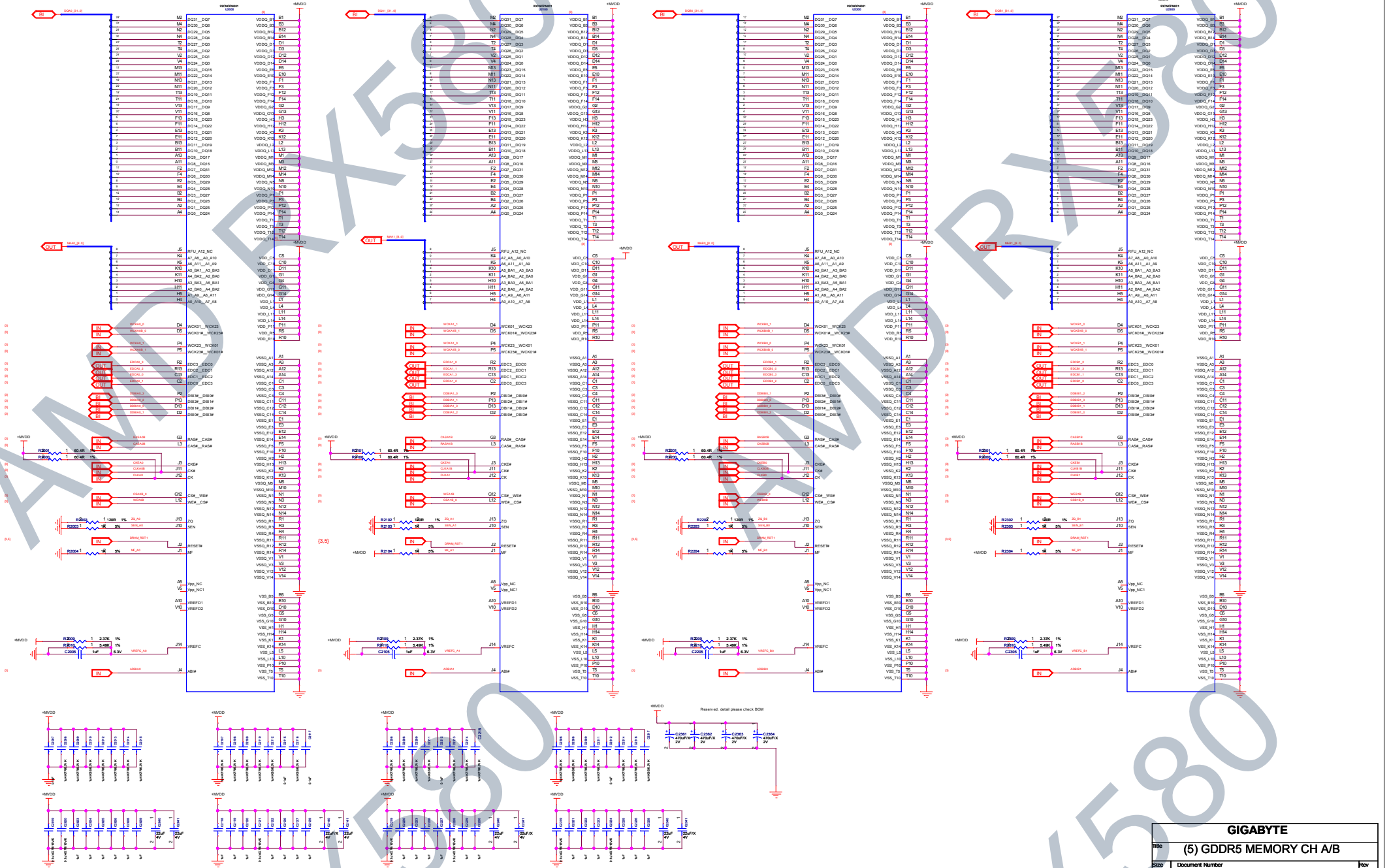
(3) ELLESMERE MEM INTERFACE CH A/B



## (4) ELLESMERE MEM INTERFACE CH C/D

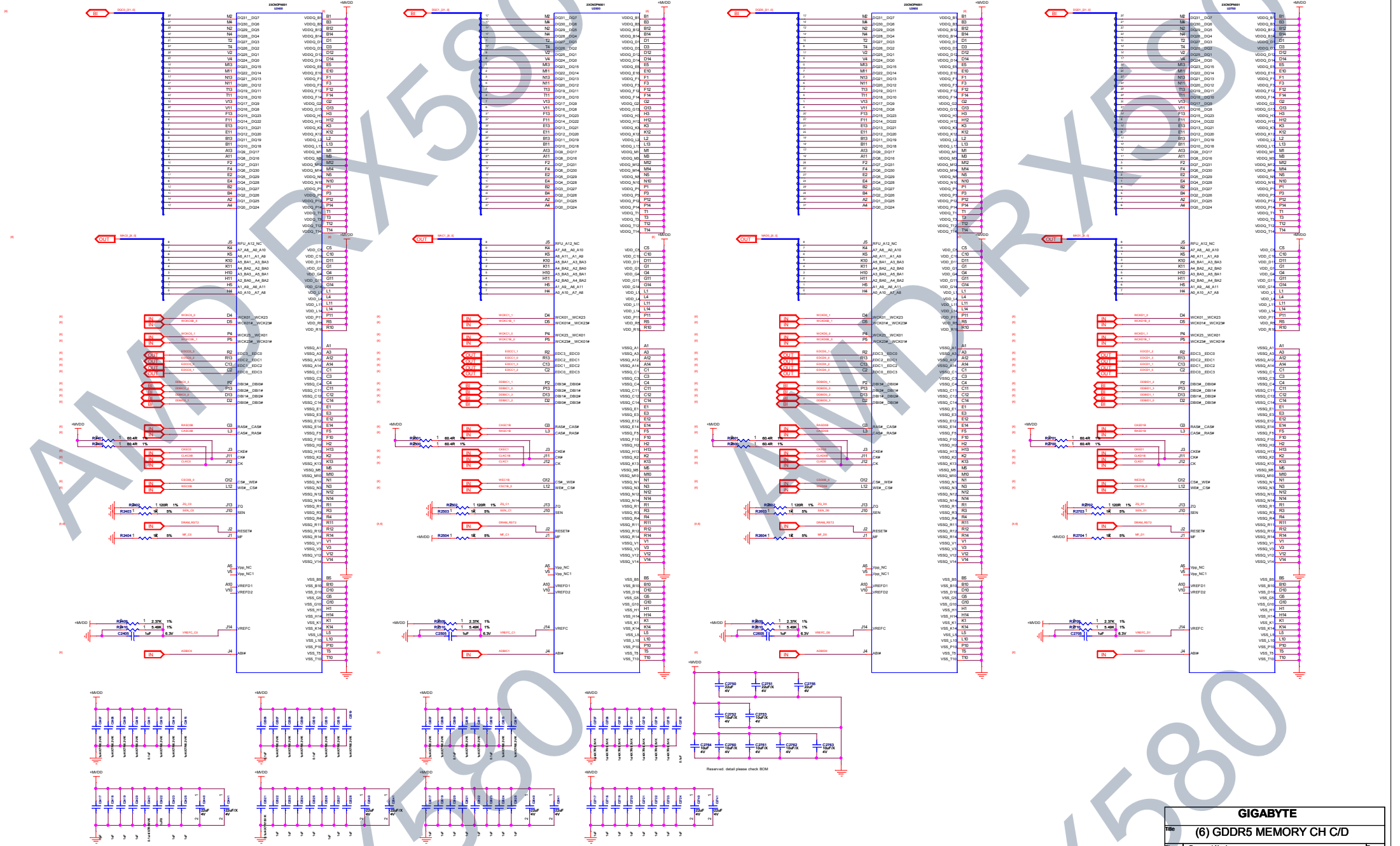


## (5) GDDR5 MEMORY CH A/B



GIGABYTE			
(5) GDDR5 MEMORY CH A/B			
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(6) GDDR5 MEMORY CH C/D



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(6) GDDR5 MEMORY CH C/D

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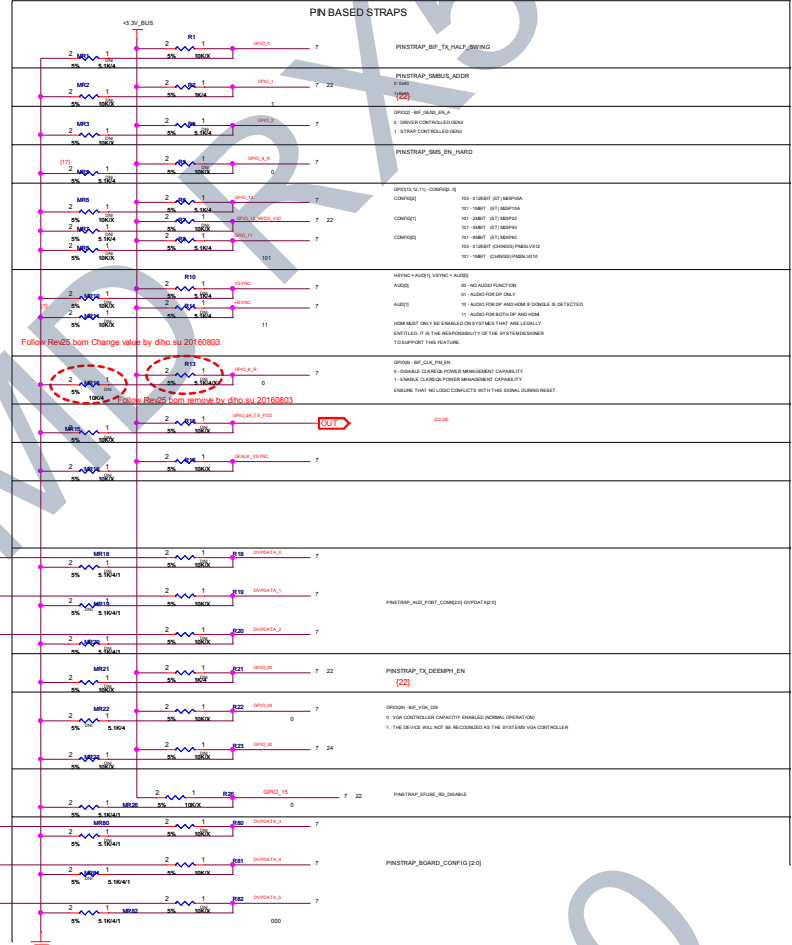
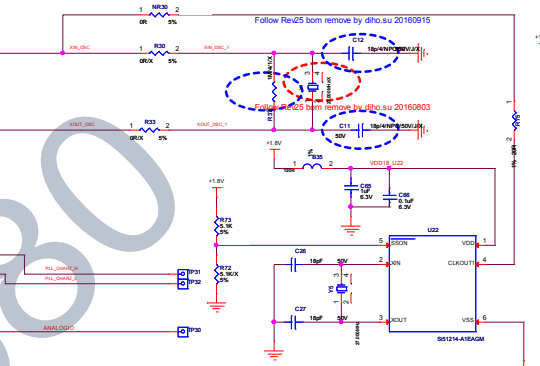
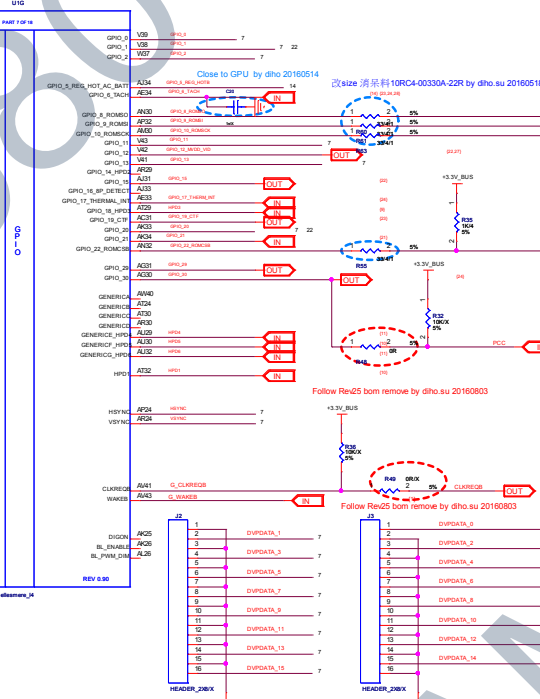
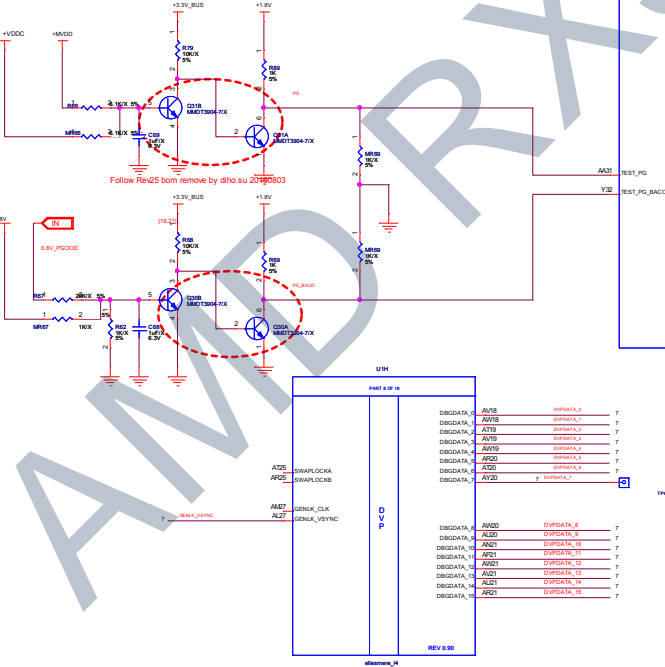
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(7) ELLESMERE GPIO STRAP CF XTAL

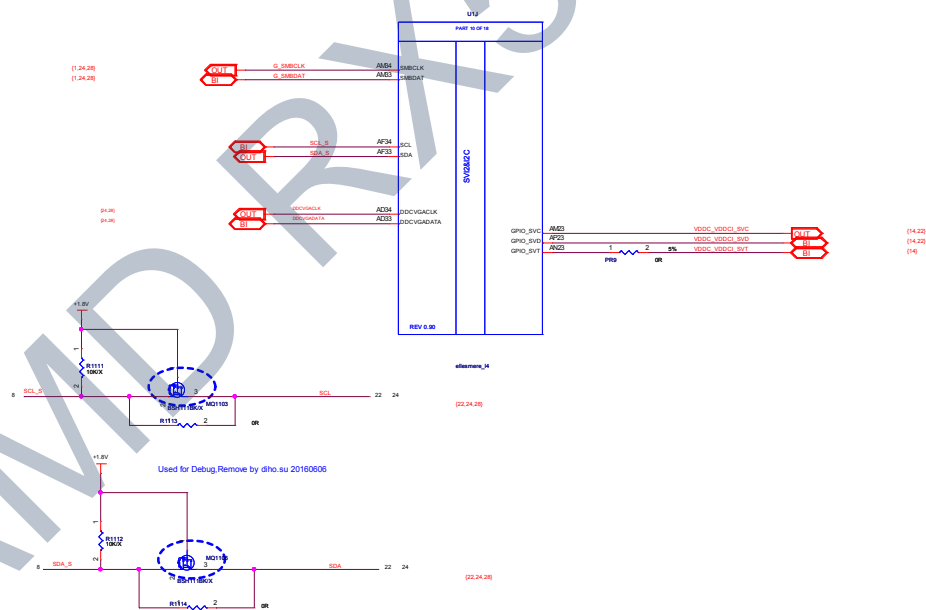
SCUDBG BUS		
IO ADDRESS	FUNCTION	DEVICE
DDCVGA BUS		
IO ADDRESS	FUNCTION	DEVICE
0x00	EXT TEMP SENSOR	LM8903



<b>GIGABYTE</b>			
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(8) ELLESMERE DAC1 LOCK

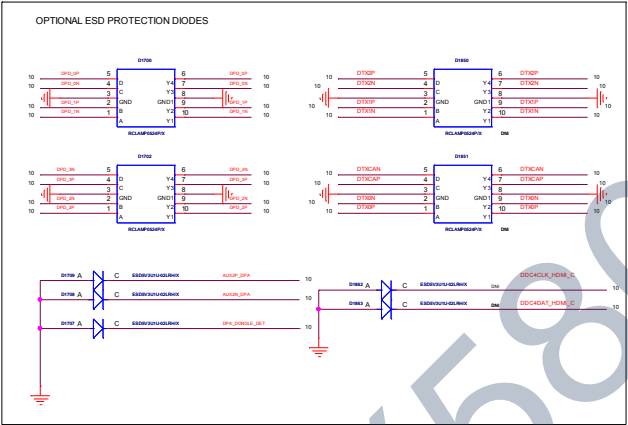
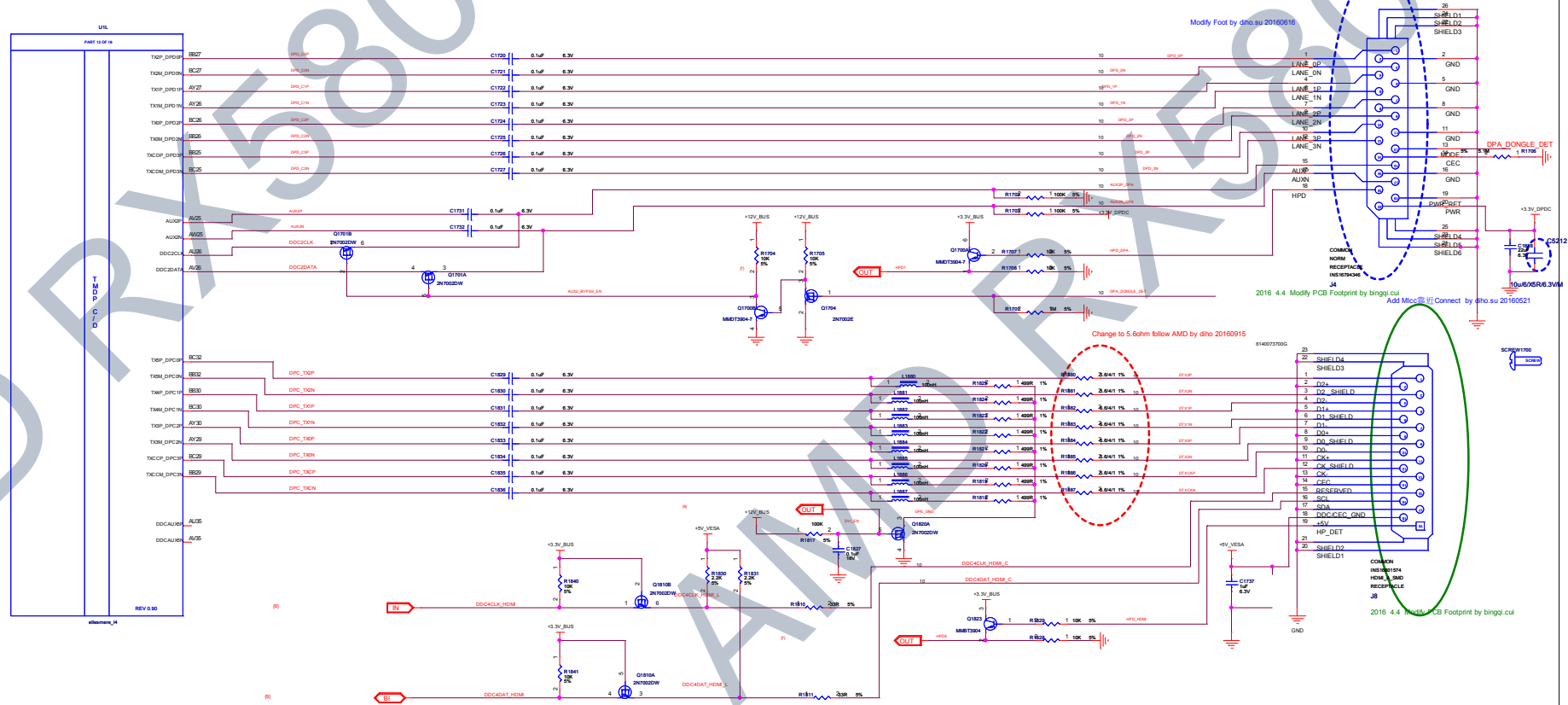


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ELLESMERE DAC1 LOCK			
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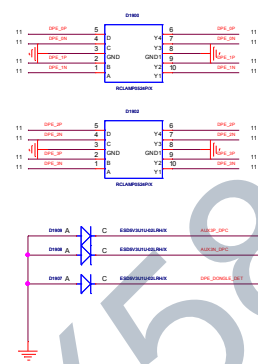
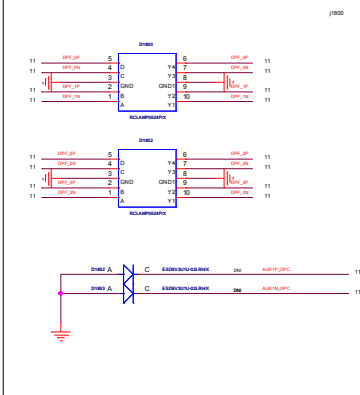




DeviceDB VIP + XinZhiZao 1 Year: [www.devedb.xyz/dev/subscriptions/](http://www.devedb.xyz/dev/subscriptions/)

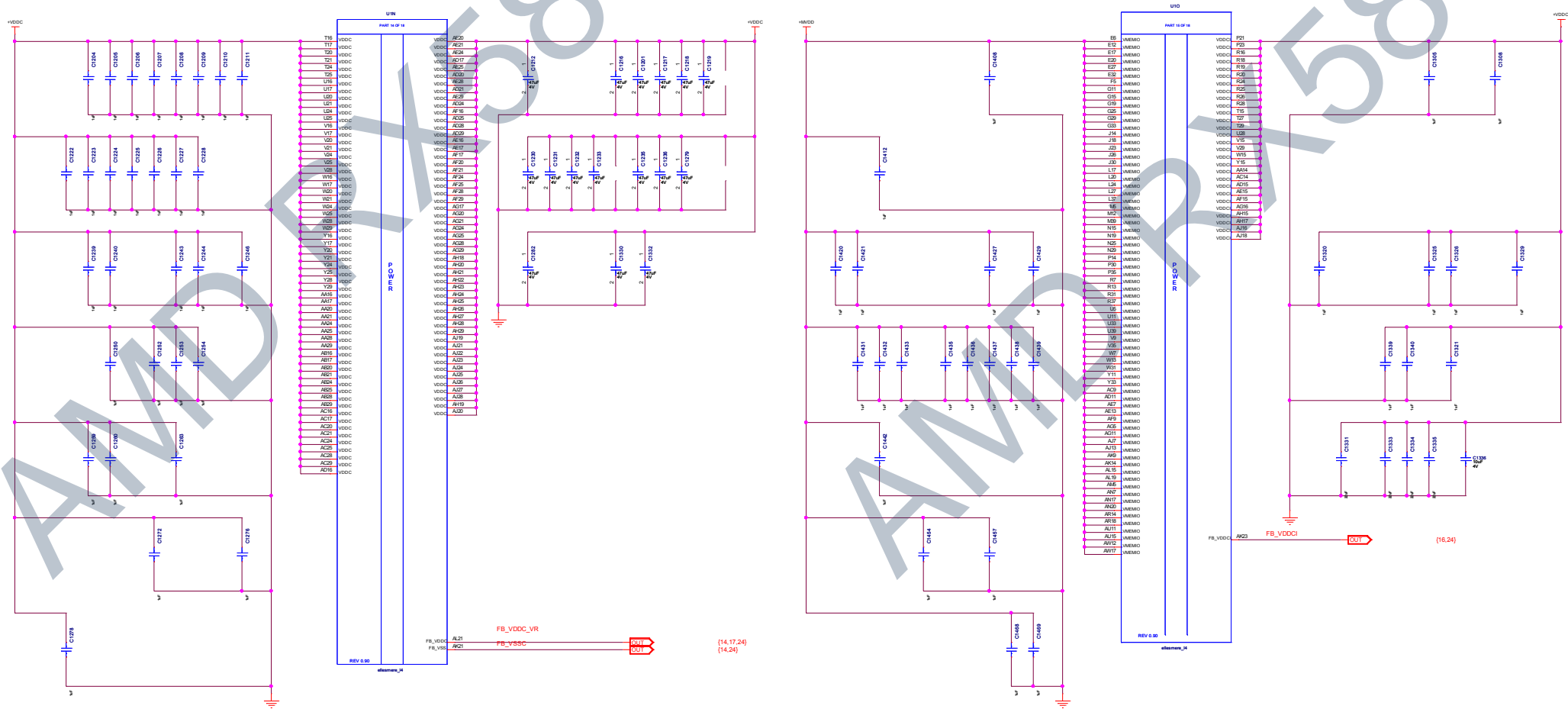


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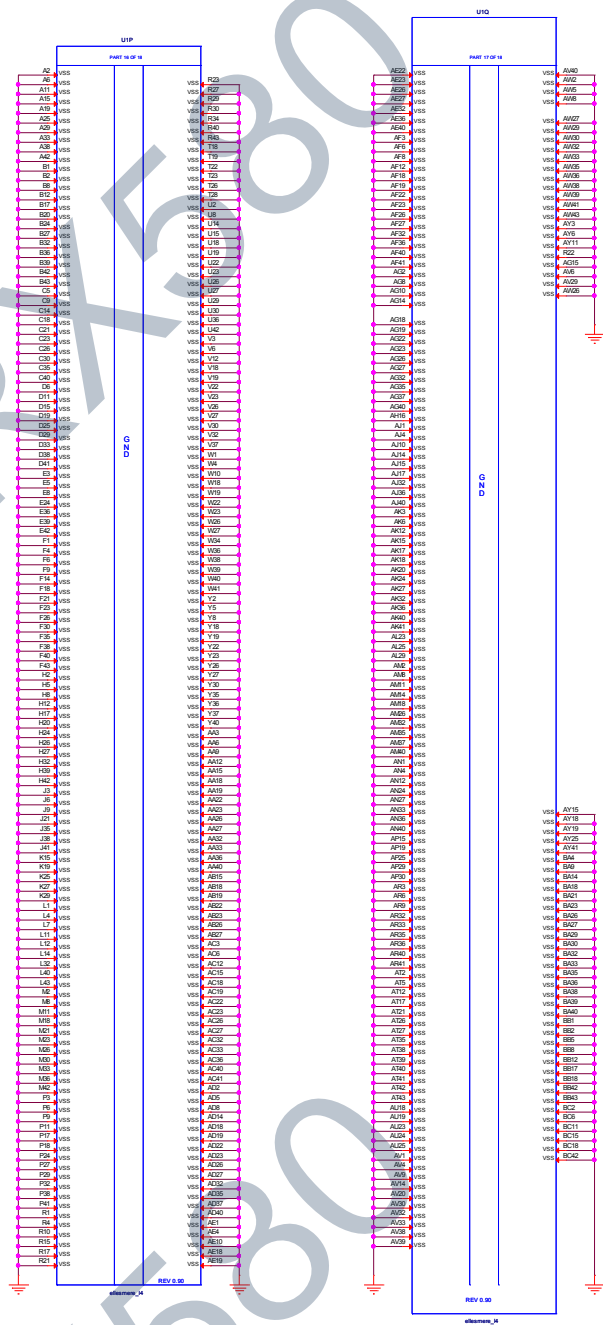


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Title <b>ELLESMERE LVTMDP E/F</b>			
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(12) ELLESMERE POWER



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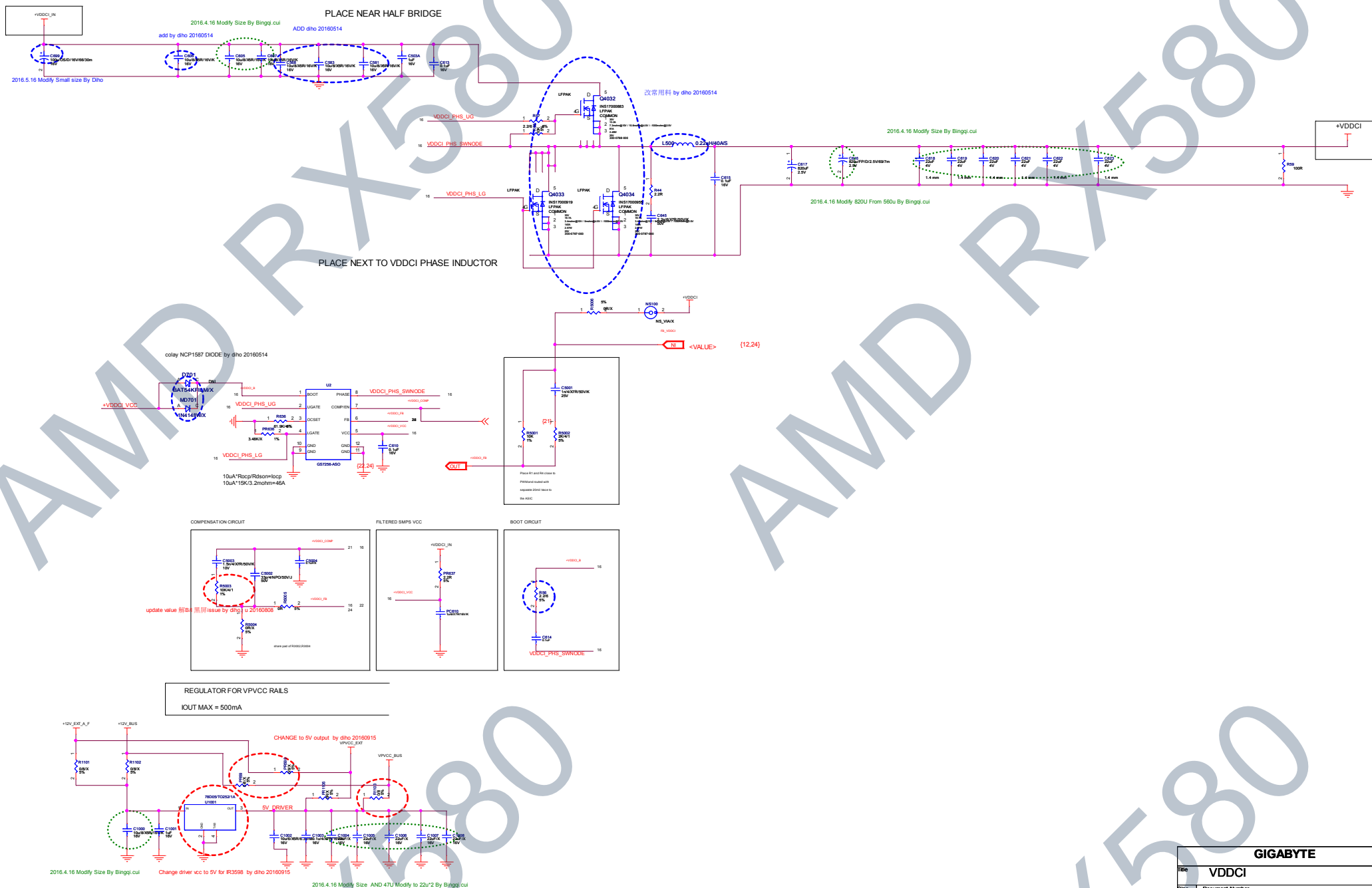


GIGABYTE			
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Site	Document Number	Rev	
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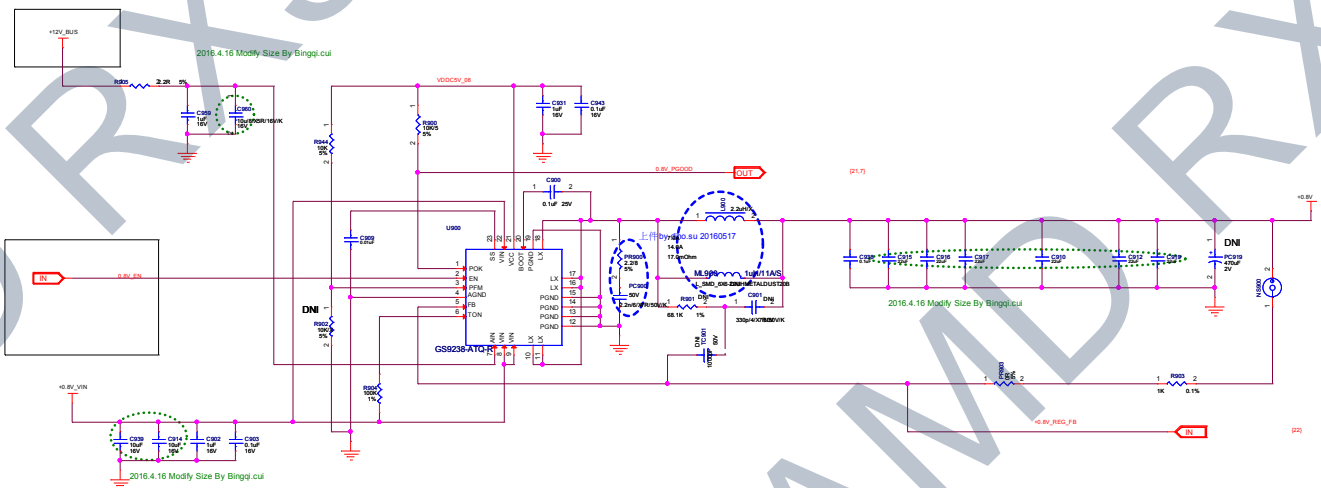
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Checksum	GV-RX580GAMING-8GD	1.0	
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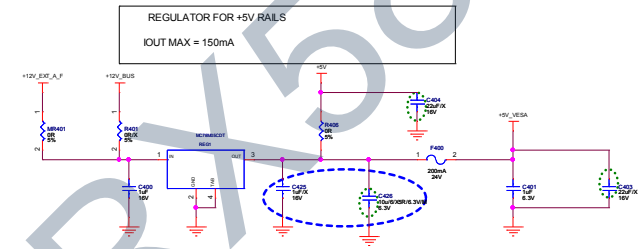
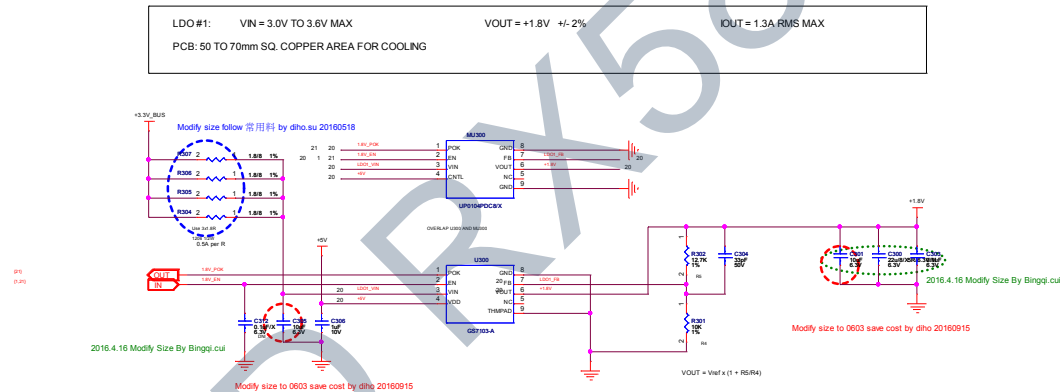
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(17) 0.95V



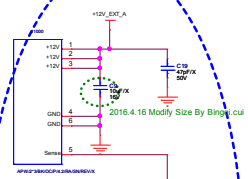
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Size	Document Number		Rev
Custom	GV-RX580GAMING-8GD		1.0
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(18) SMALL RAIL REGULATORS

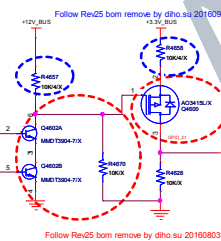
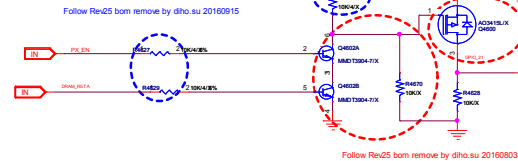
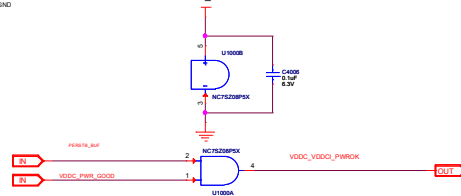
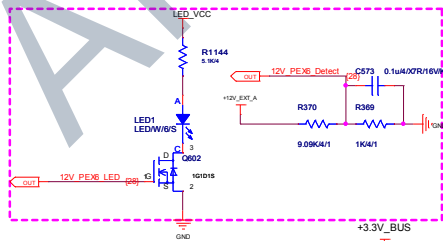
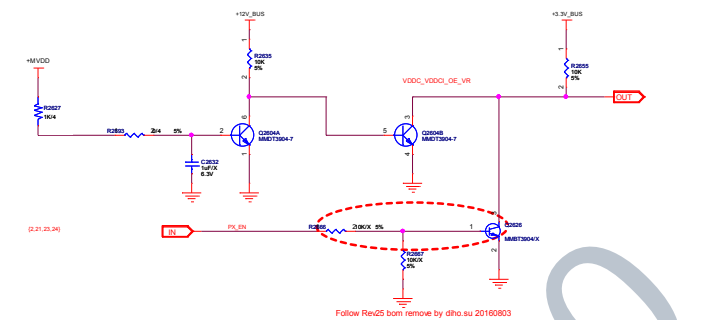
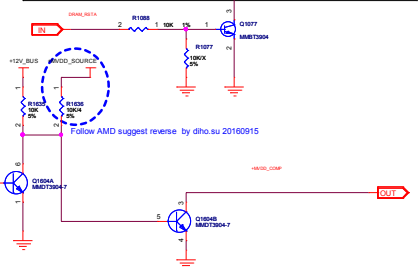
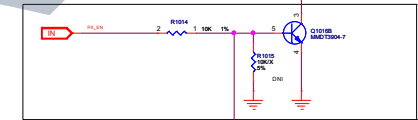
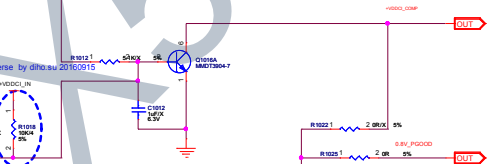
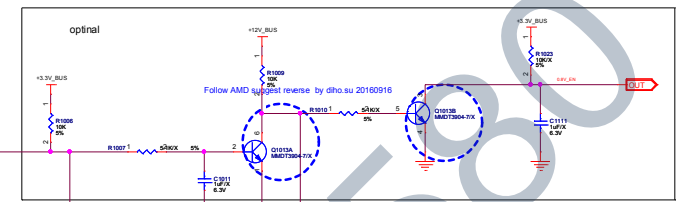
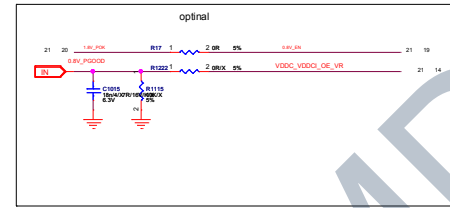
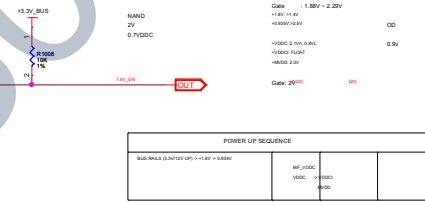
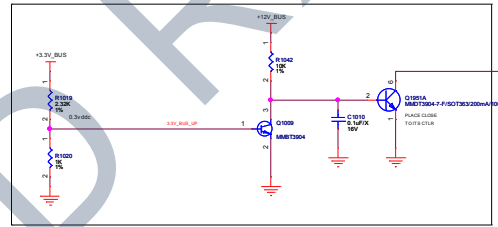
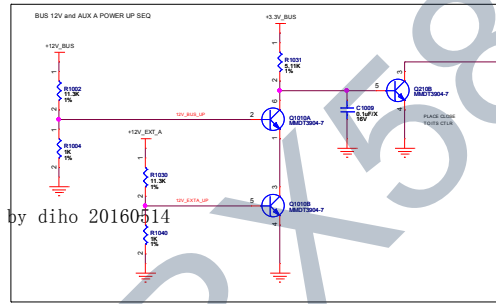
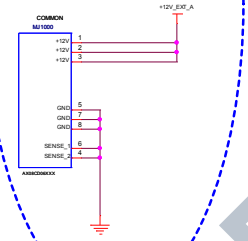


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(19) POWER MANAGEMENT



6PIN&amp;8PIN CONNECT COLAY by diho 20160514

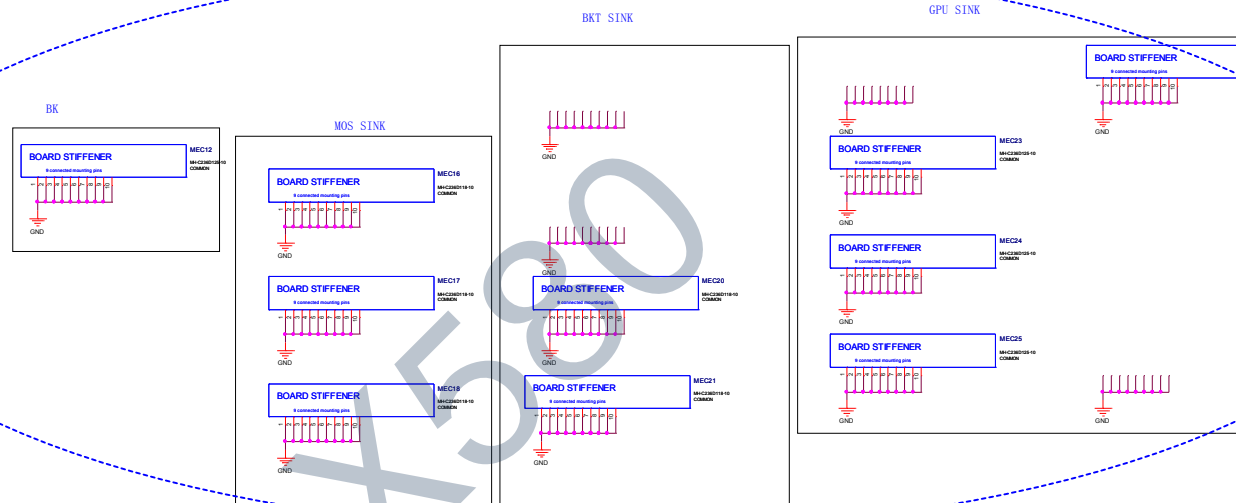
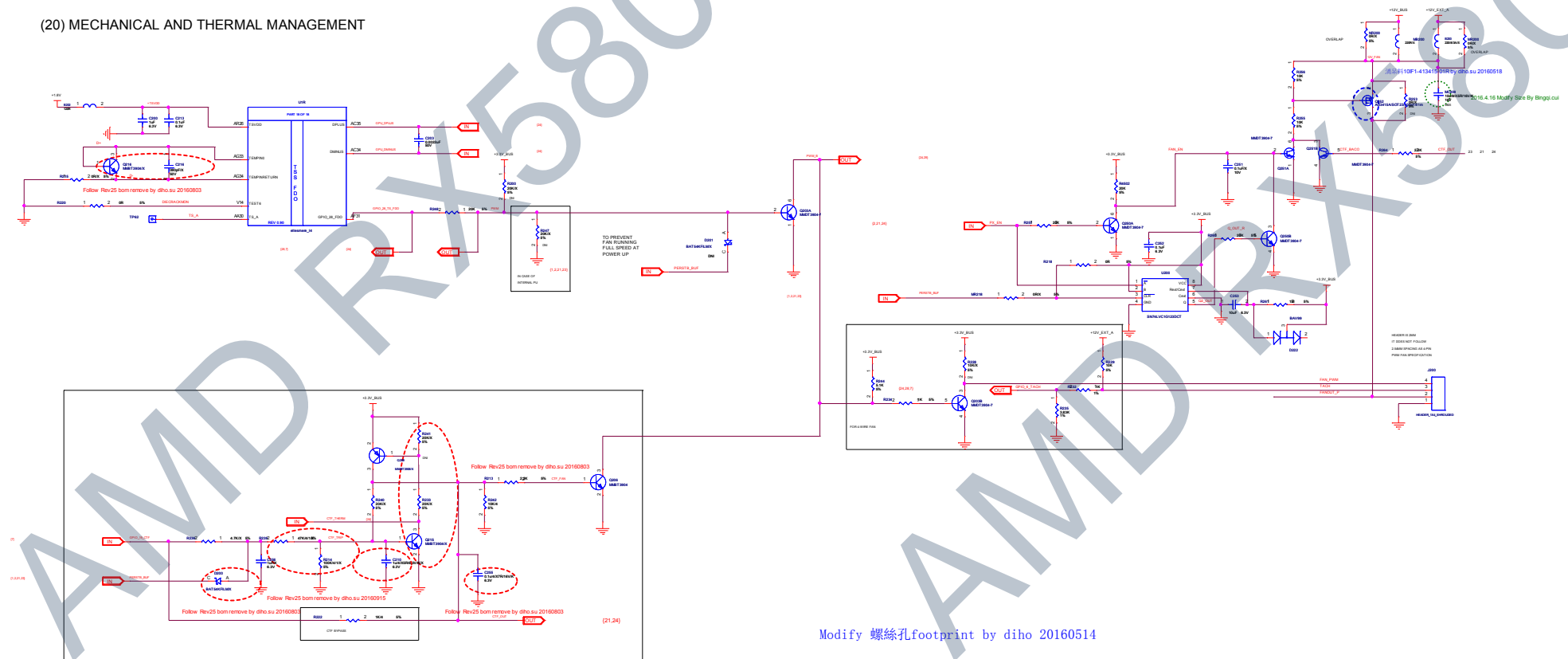


<b>GIGABYTE</b>			
<b>POWER MANAGEMENT1</b>			
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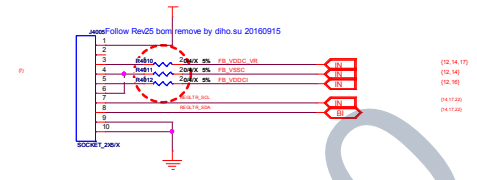
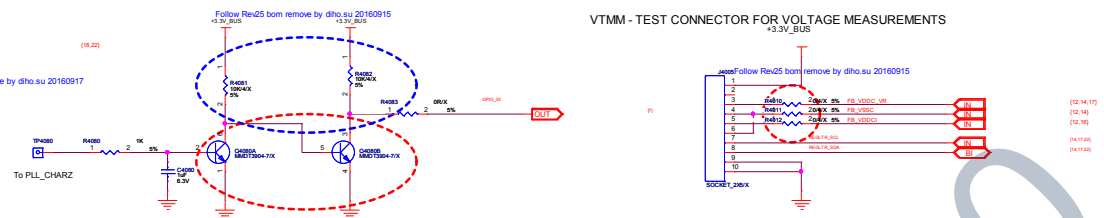
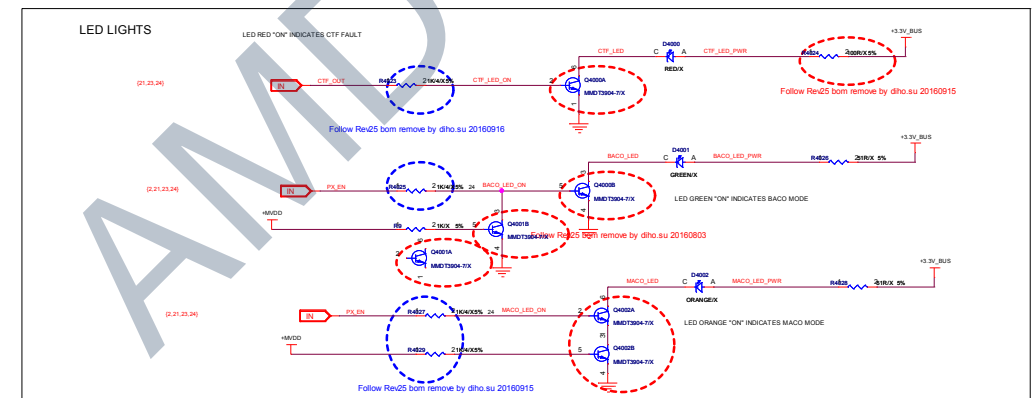
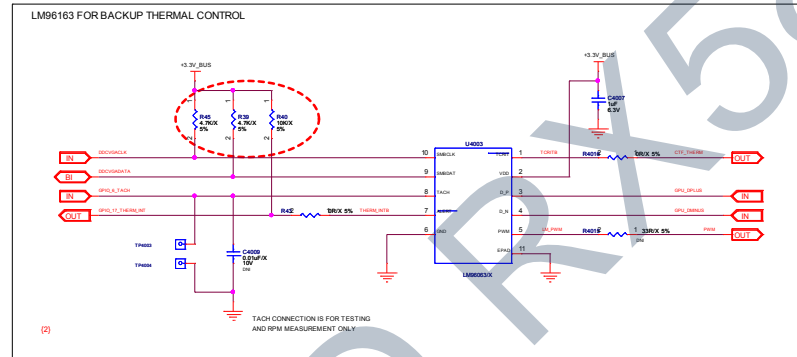
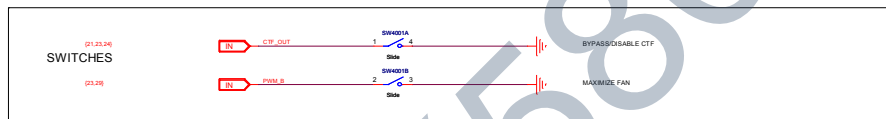
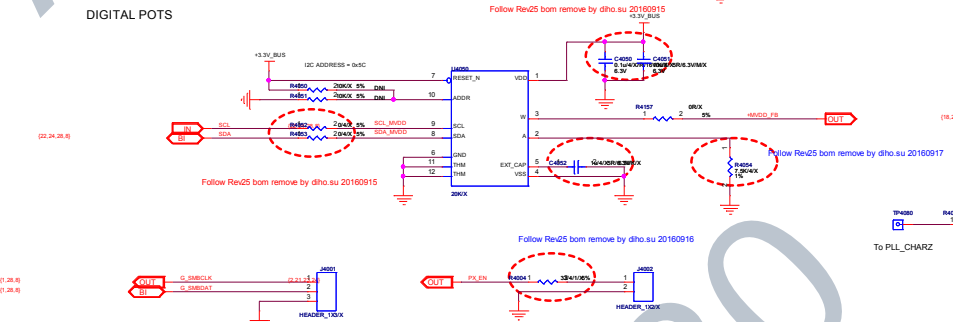
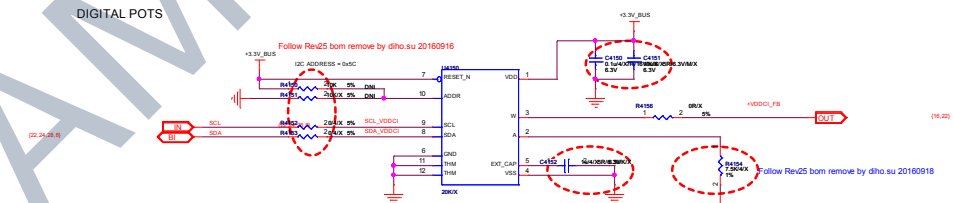
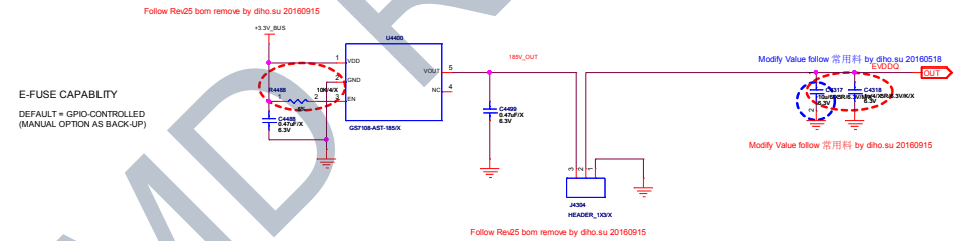
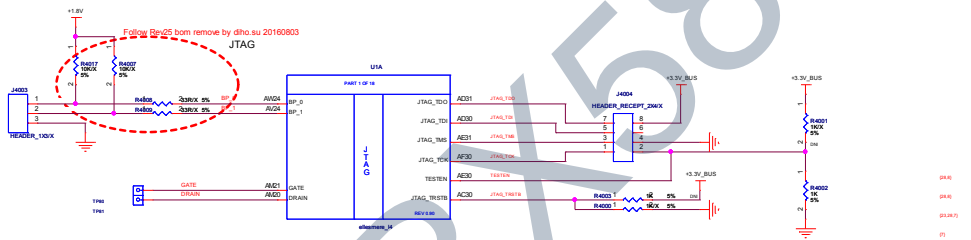


## (20) MECHANICAL AND THERMAL MANAGEMENT

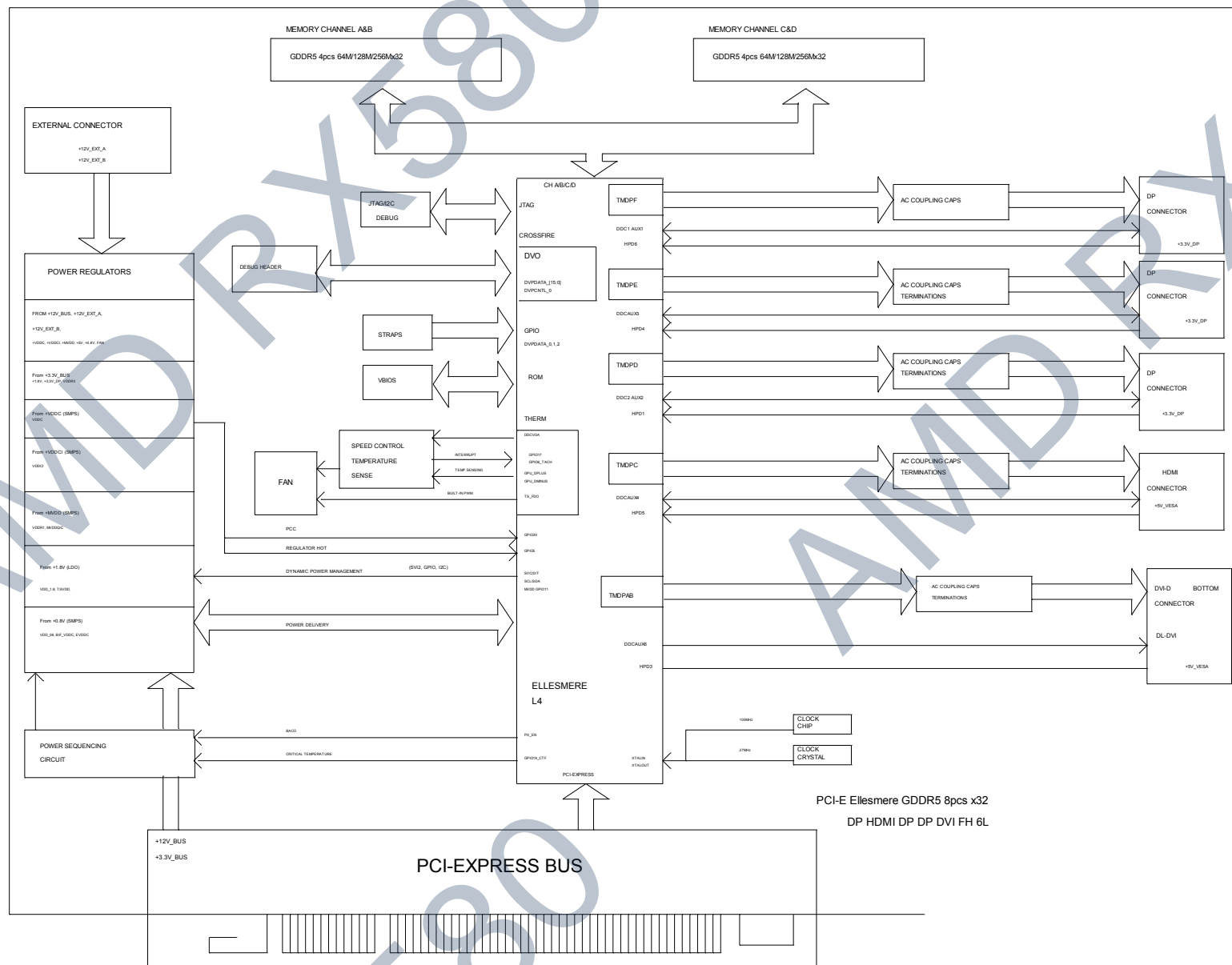


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## (21) DEBUG CIRCUITS



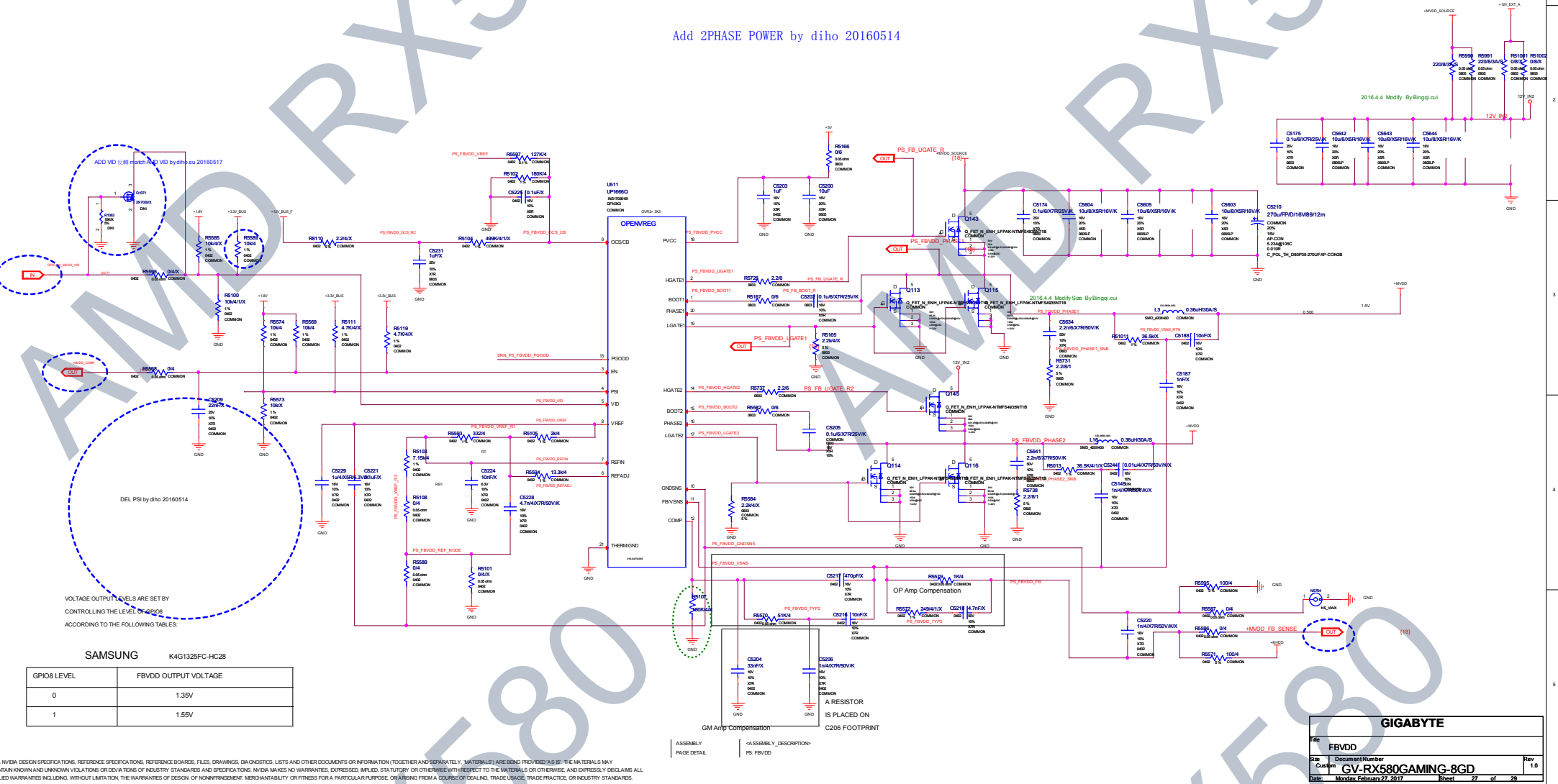
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Title <b>DEBUG CIRCUITS</b>			
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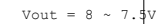


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BLOCK DIAGRAM			
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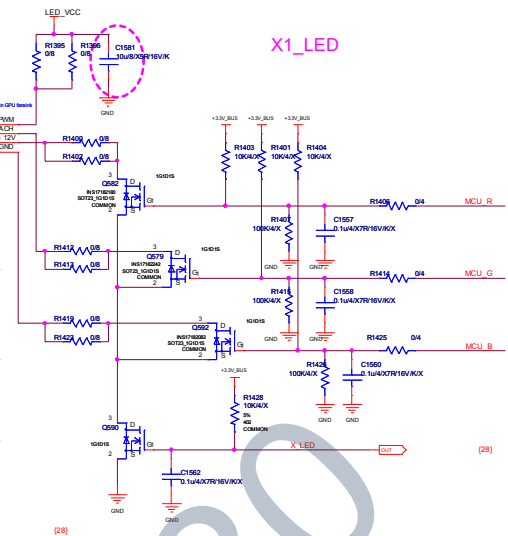
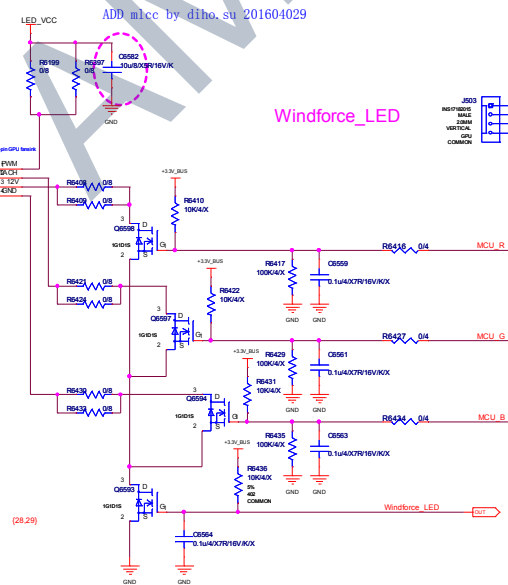
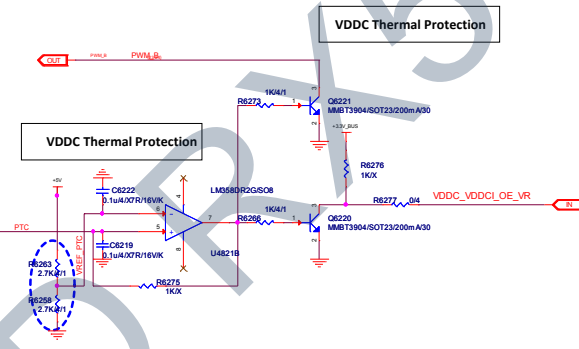
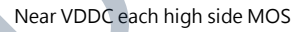
0	00A	000000	
1	00B	000000	1. Add SPI0 to SPI000 10000 2. Update SPI000 driver response
2	00C	000000	PCIE0: - add series resistor R1000 - R1007 - add pull-down inductor L1000 - L1007 Remove C400, C403, V0400, C410, C414, R400
3	00D	000000	Modify G007 Design

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