NVIDIA RTX3070

03/13/2024 04:11 PM

PG142-B00

DP + DP + DP + HDMI/DP

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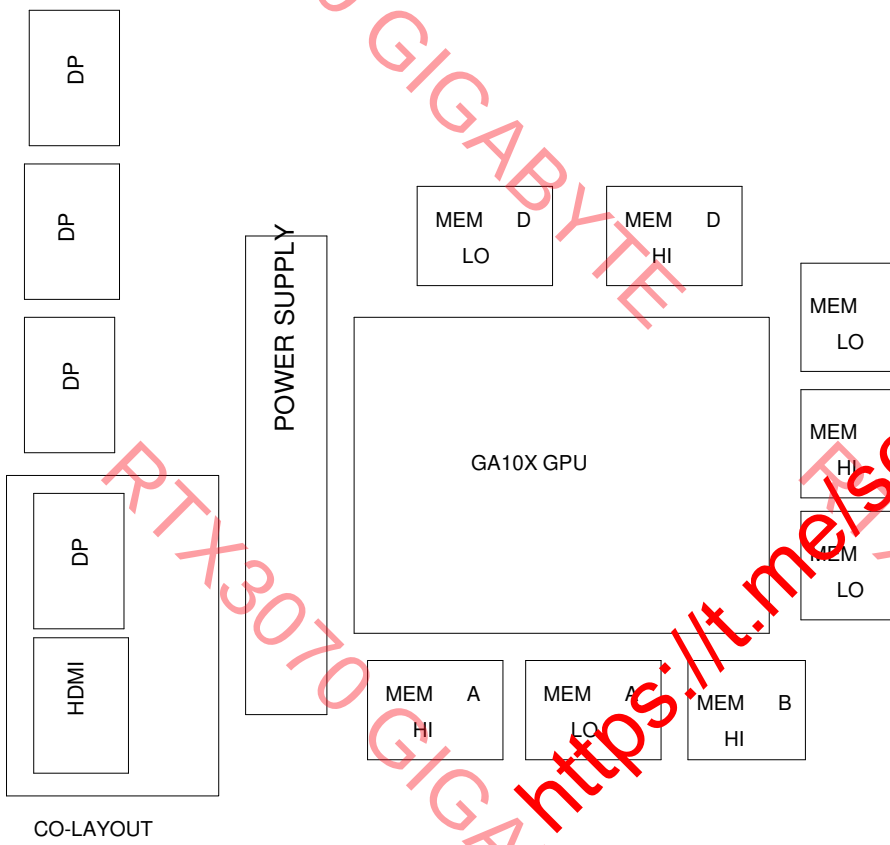

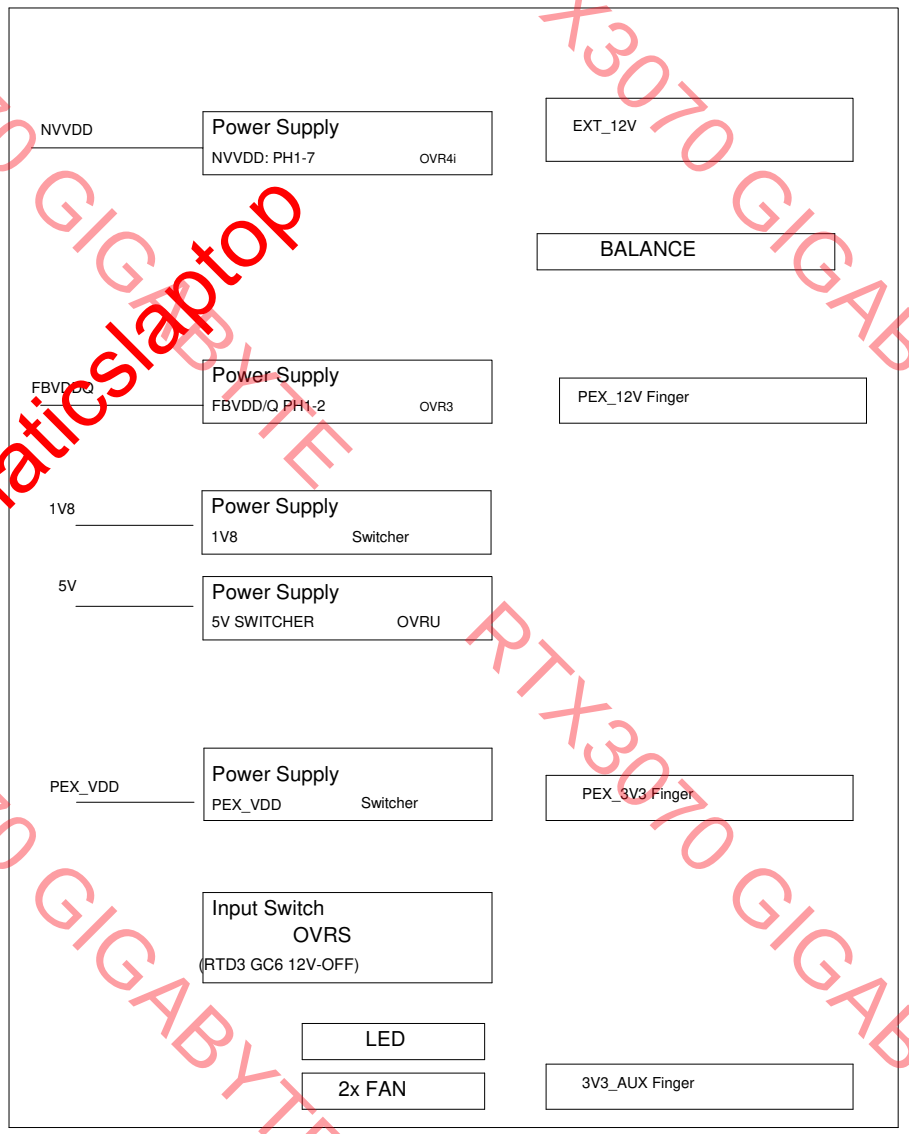

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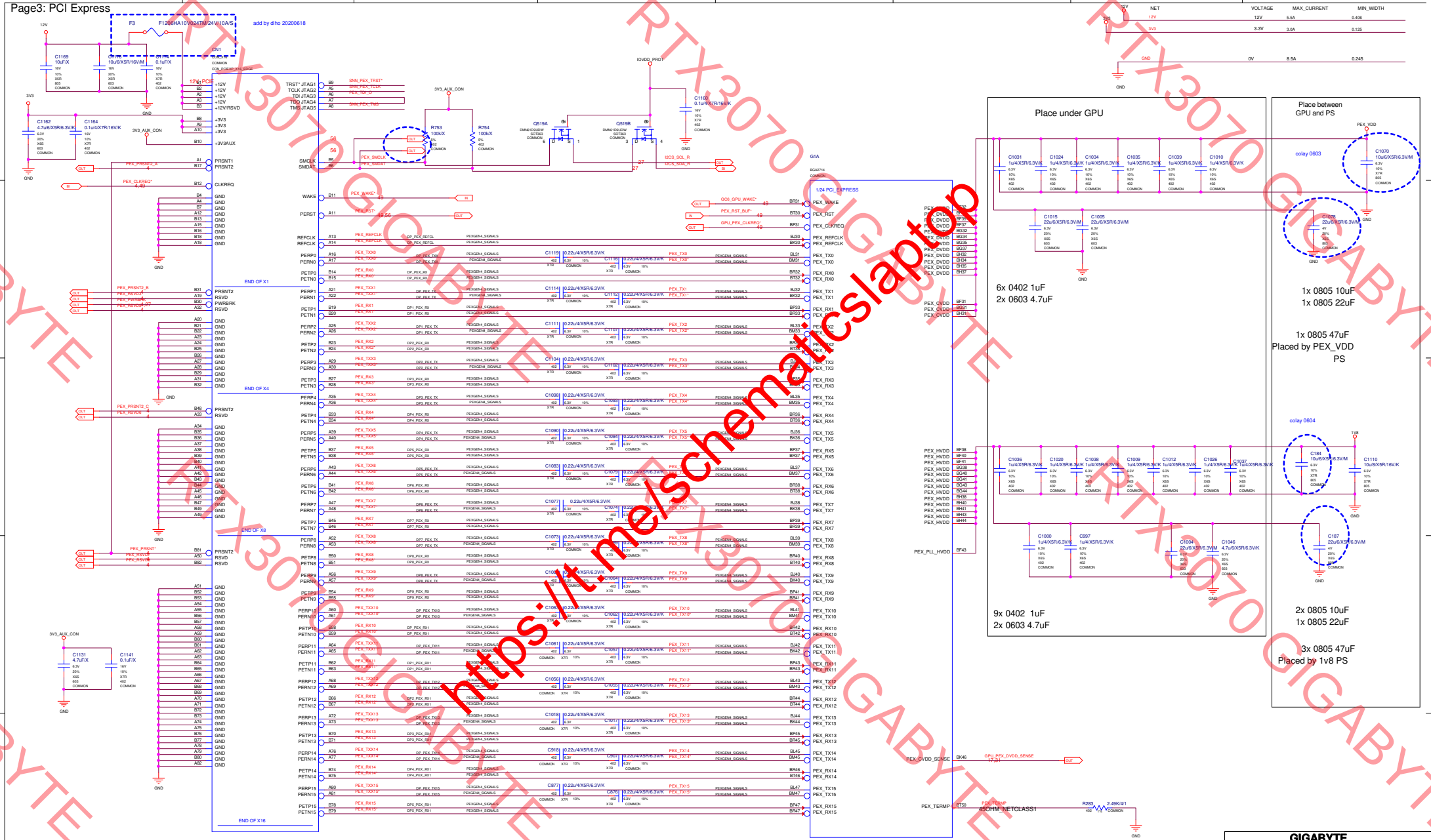

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Page4: PCIE GEN4 RC TERMINATIONS

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Page5: MEMORY: GPU Partition A/B

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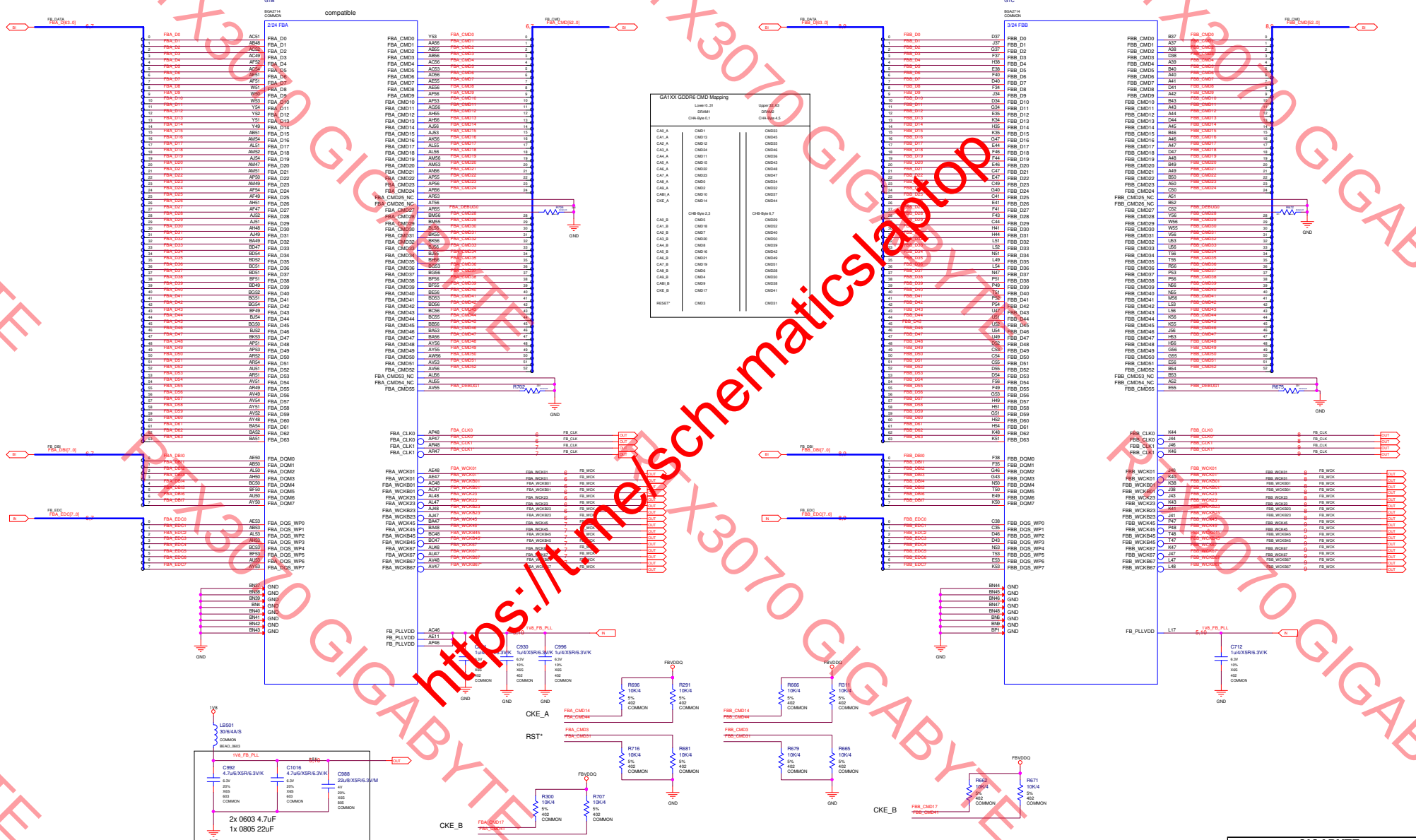

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MEMORY: GPU FB_AB

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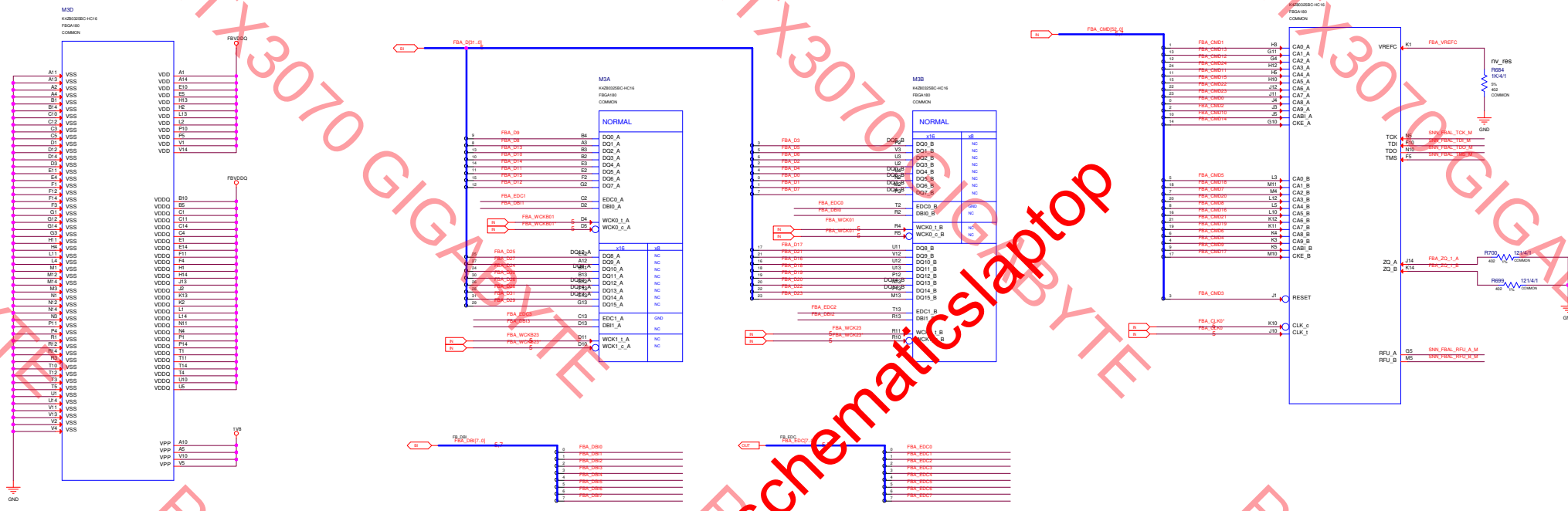
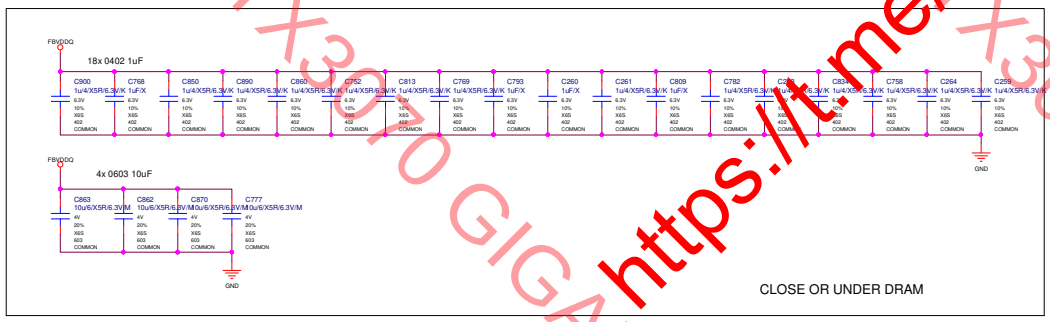
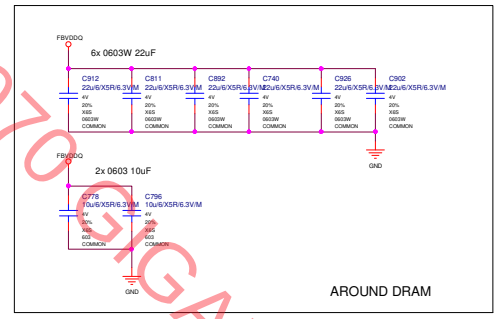
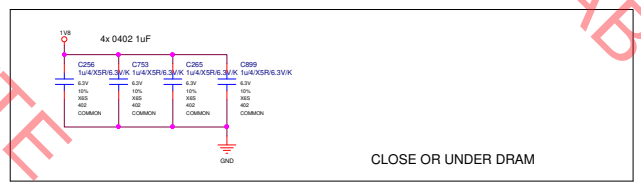


decap via : at least 2 gnd vias and 2 power vias for each cap







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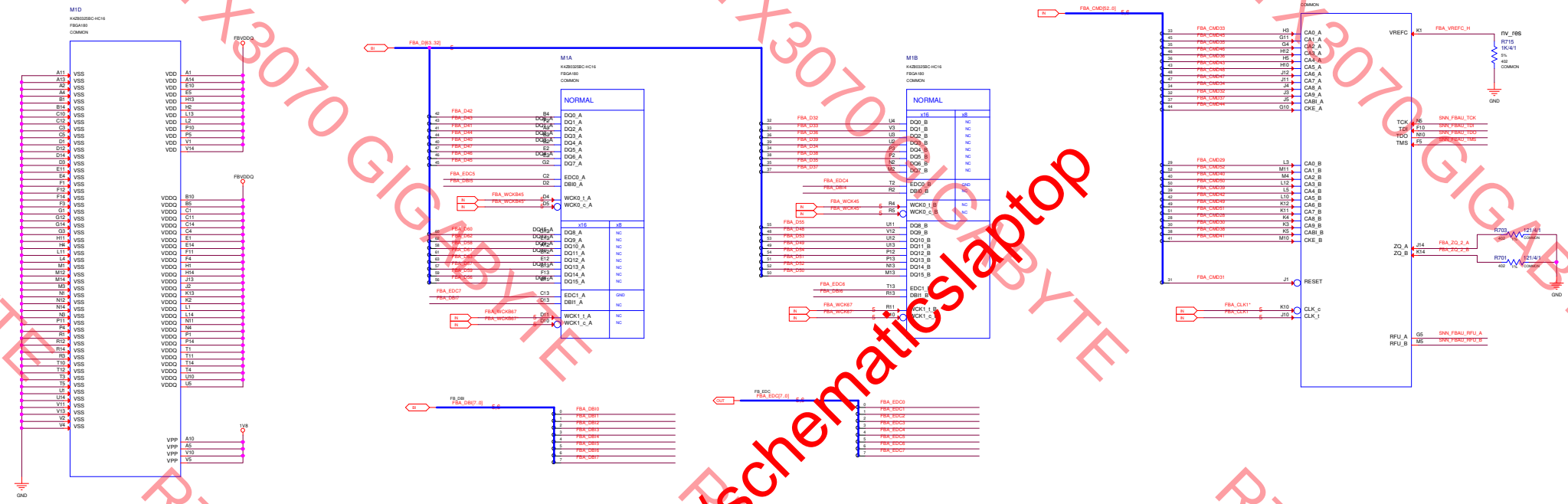

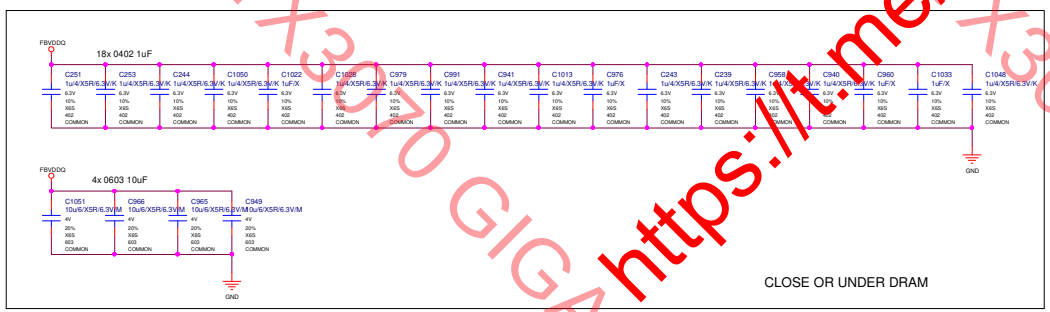

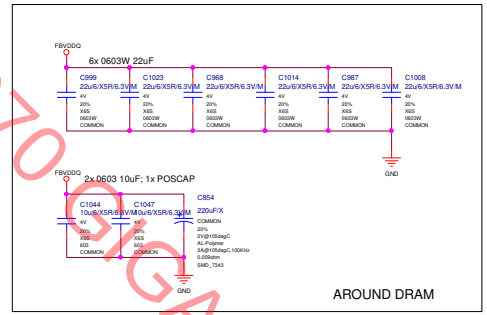

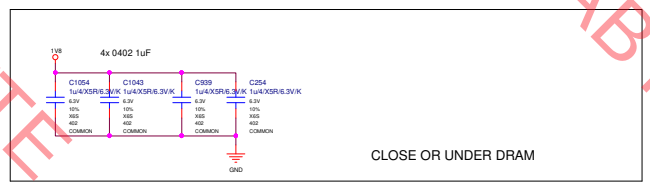

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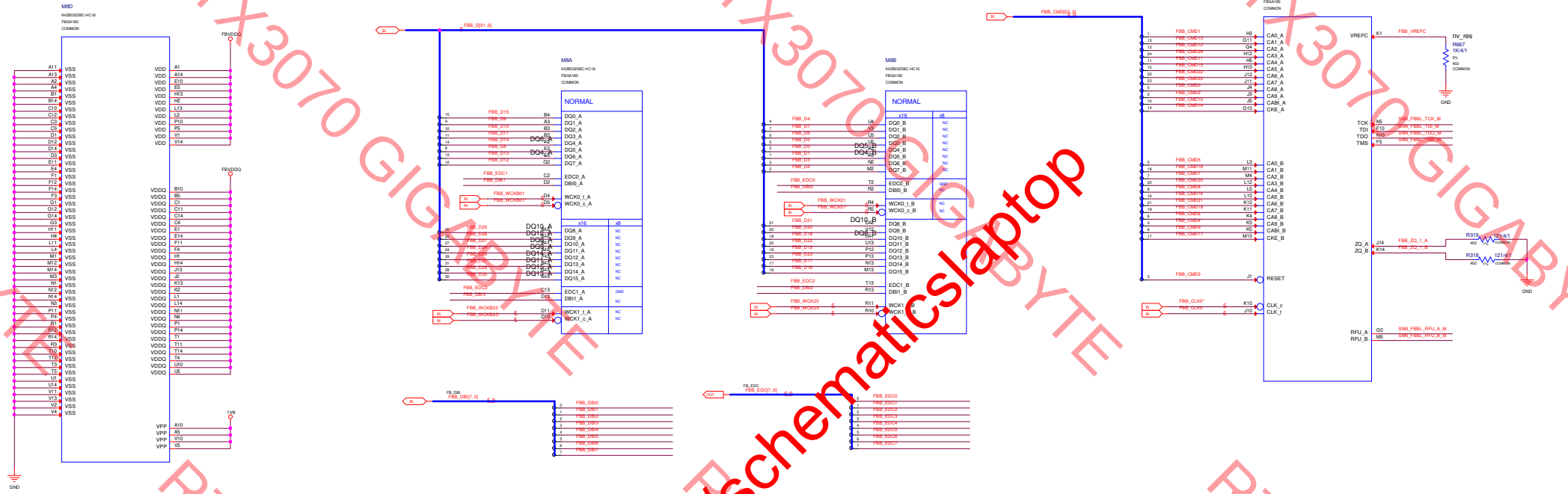

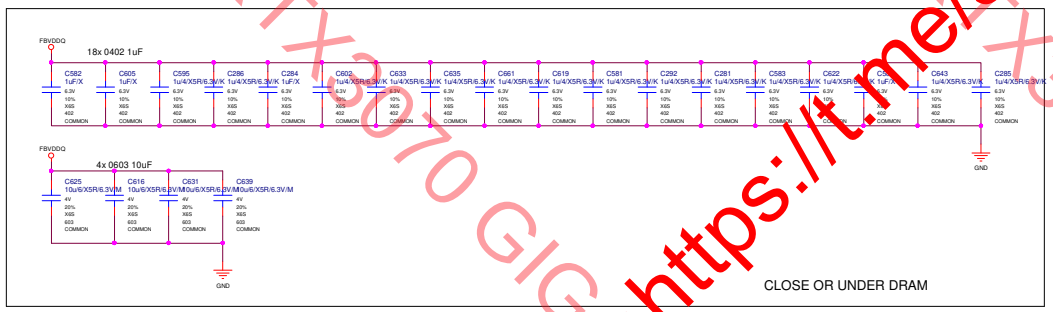

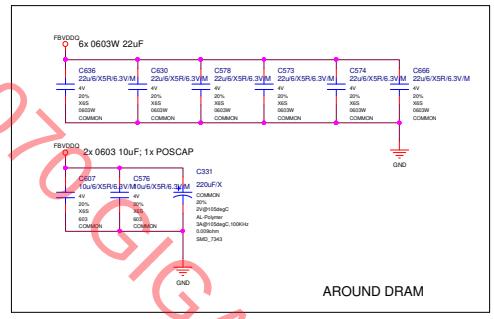

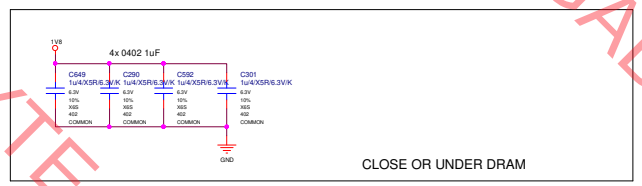

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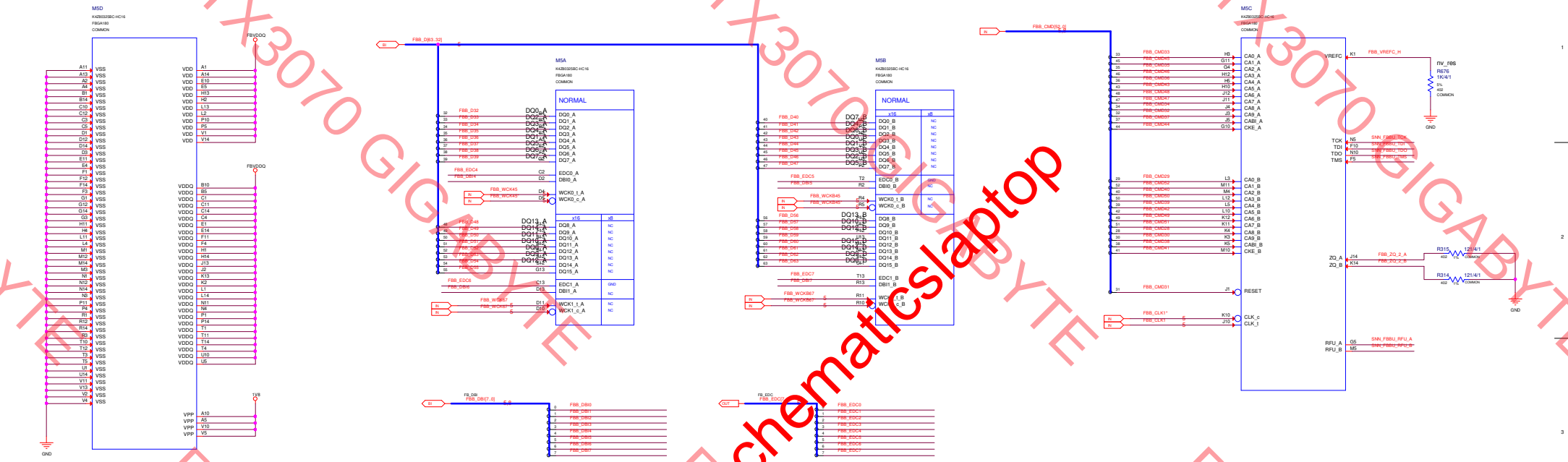

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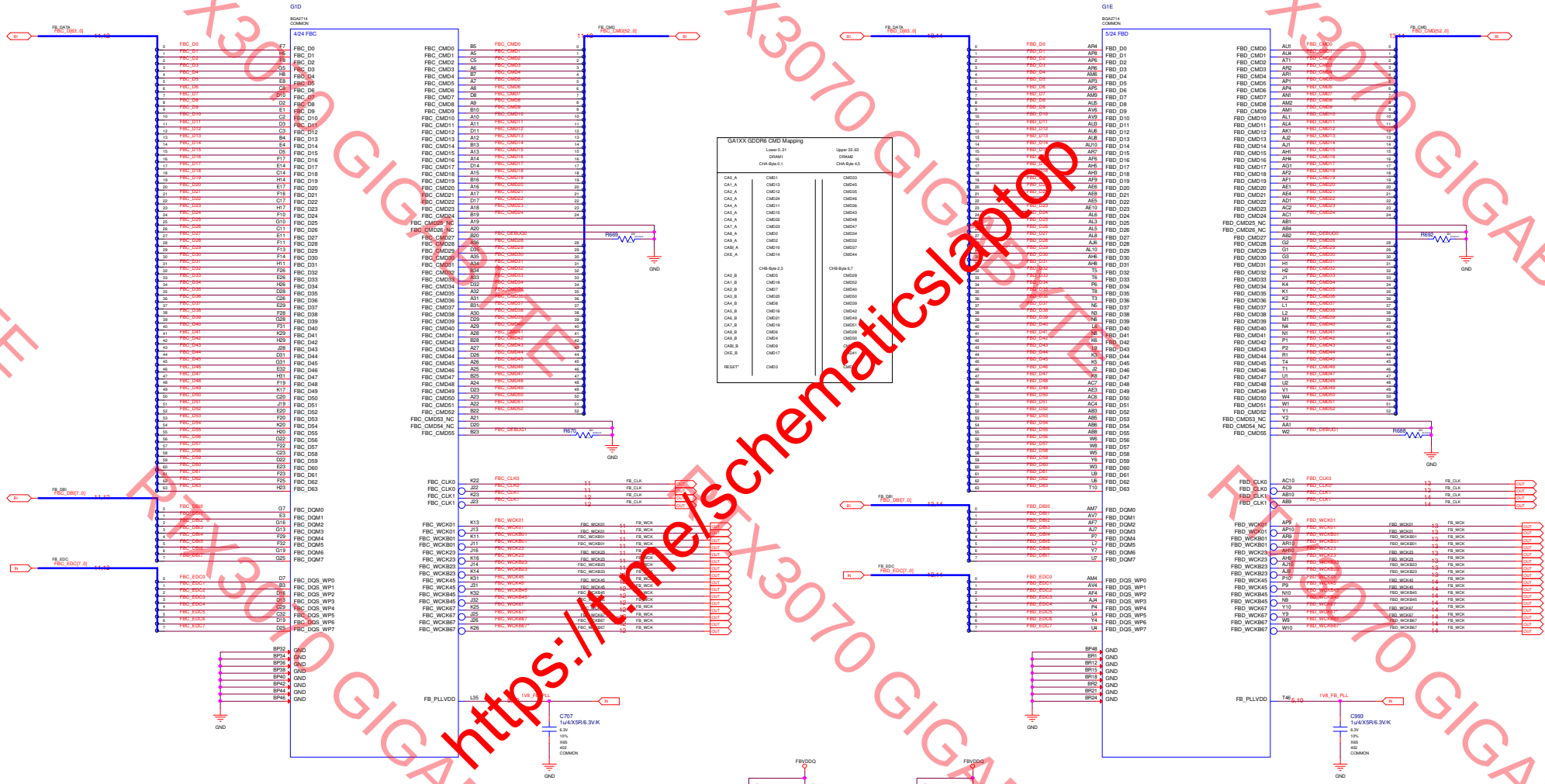

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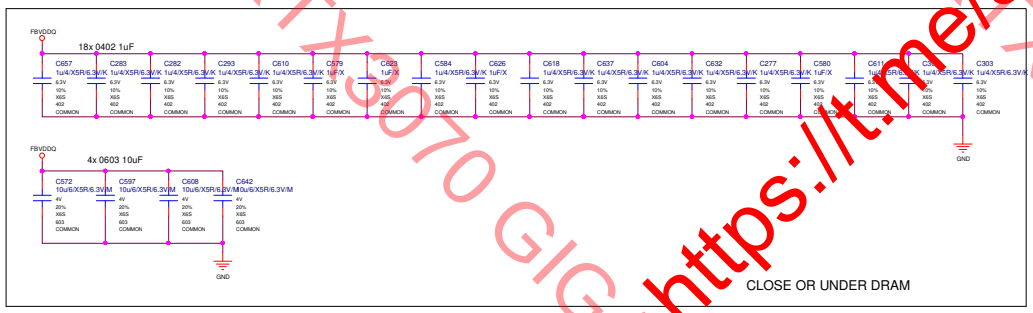

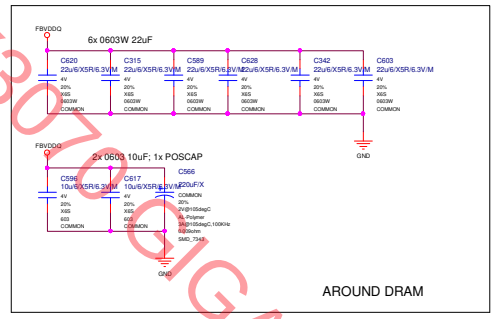

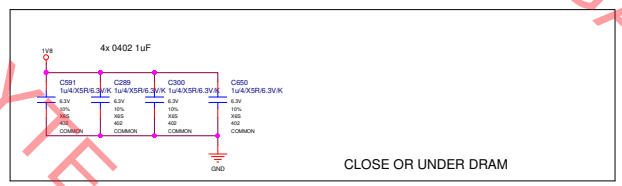

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Title: Page11: MEMORY: FBC Partition 31..0

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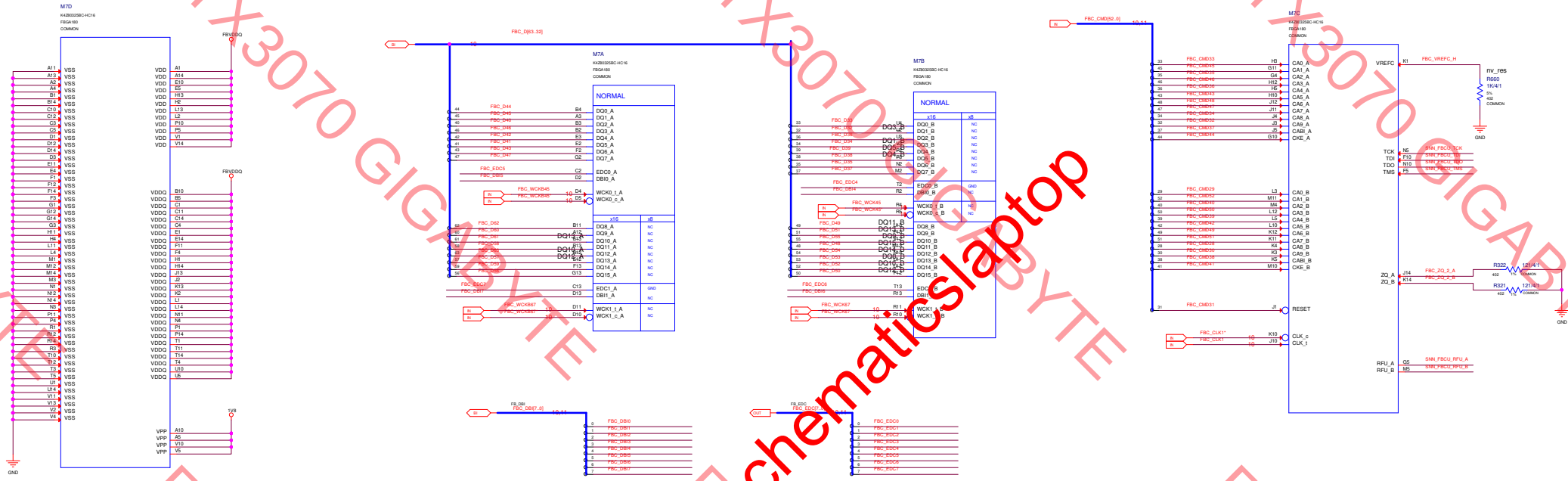

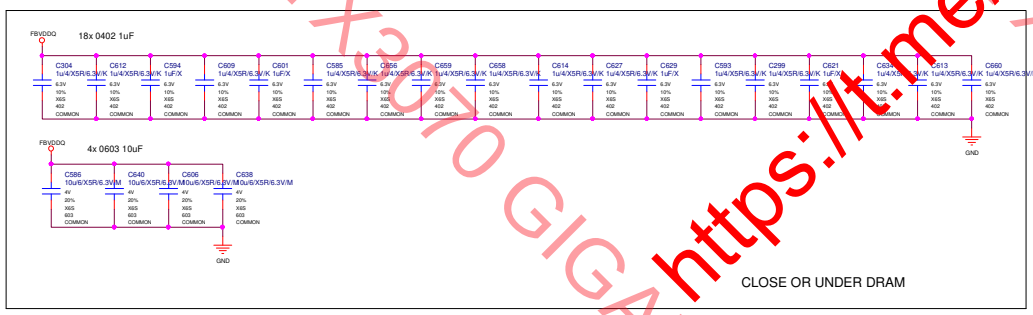

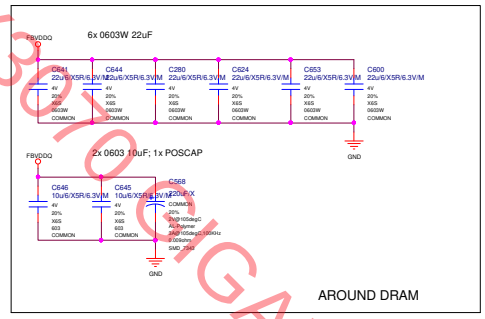

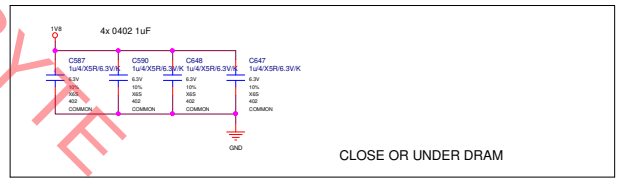

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Title: Page12: MEMORY: FBC Partition 63..32

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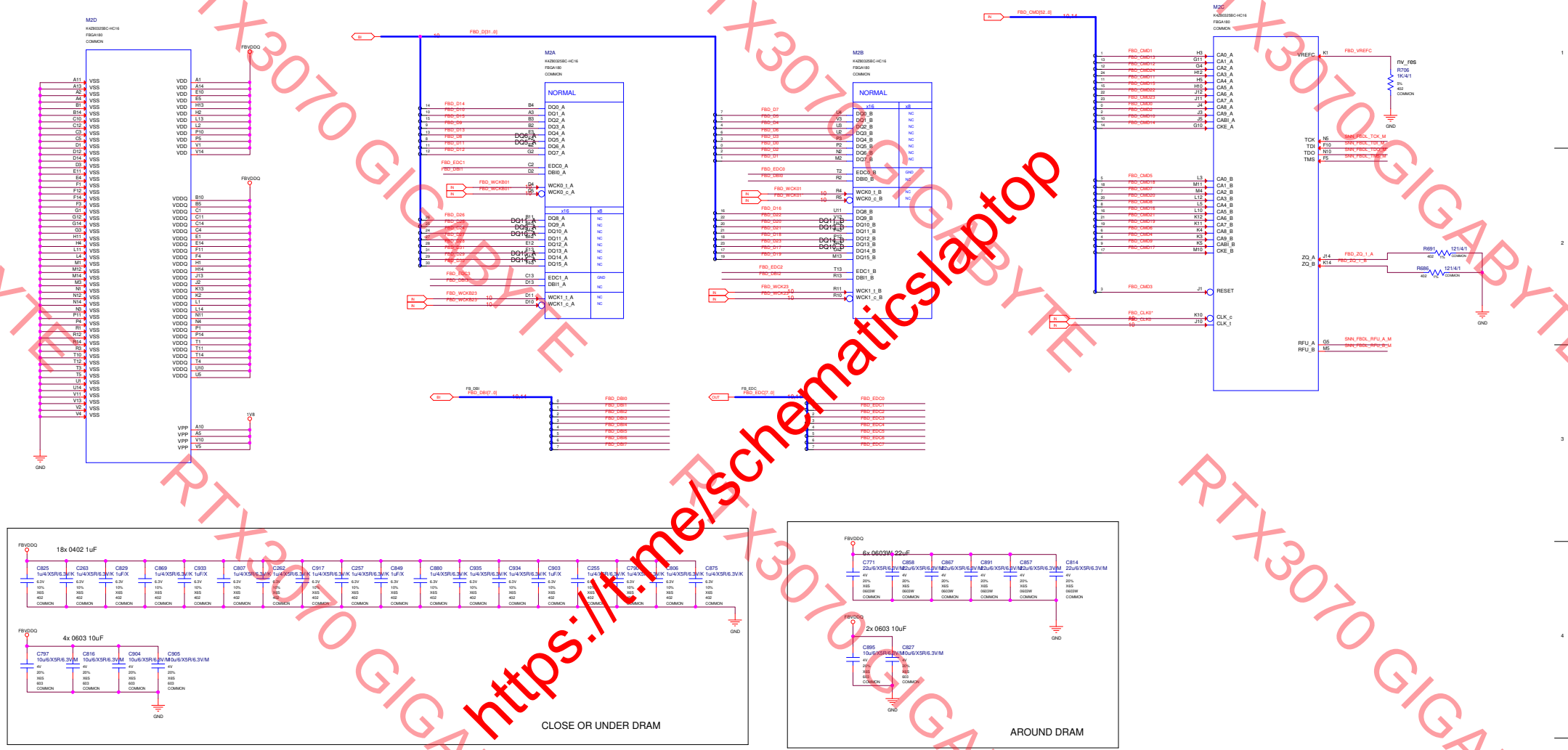

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MEMORY: FBD[31:0]

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Title	Page13: MEMORY: FBD Partition 31..0
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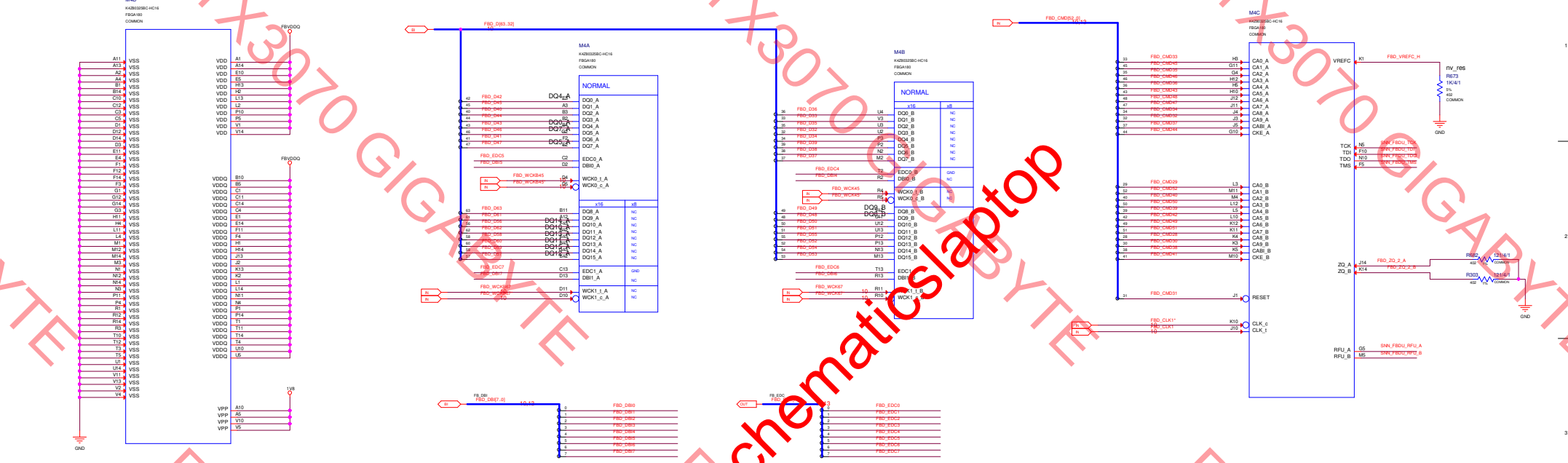

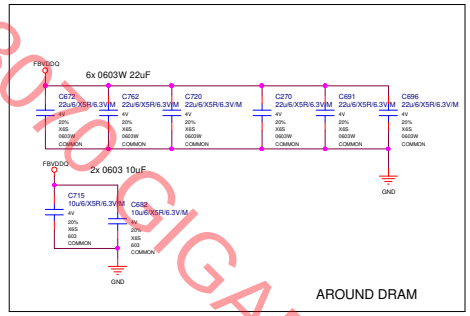

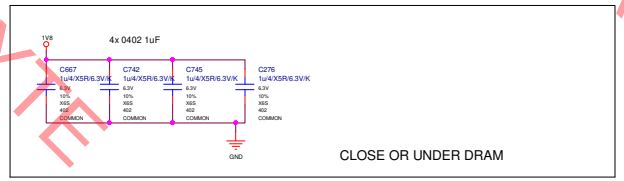

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[63:32]

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Title: Page14: MEMORY: FBD Partition 63..32

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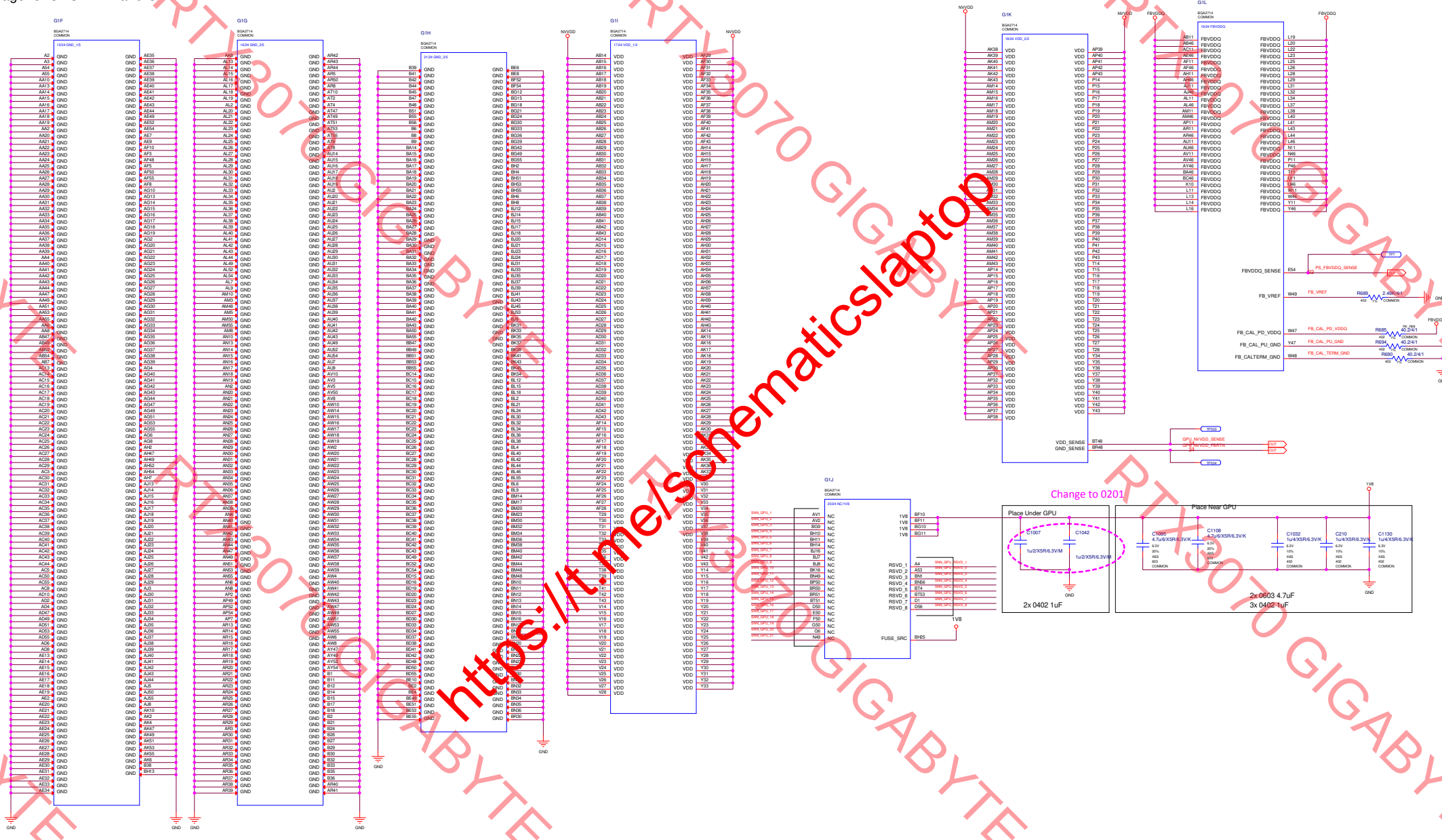
Page15: GPU PWR and GND



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU PWR & GND
1

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Title: Page15: GPU PWR and GND

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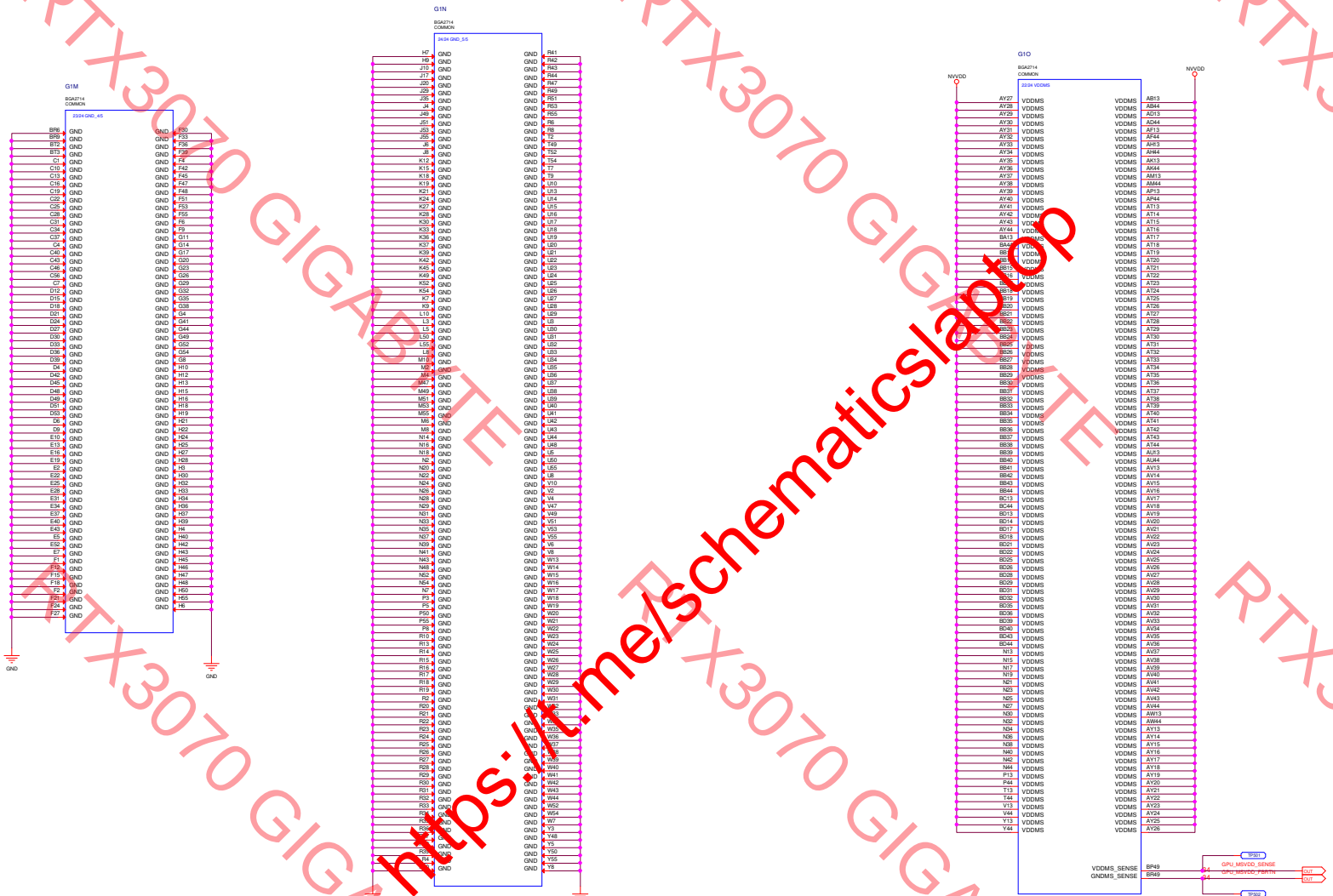
Page16: GPU PWR and GND 2



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU PWR & GND 2

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Title: Page16: GPU PWR and GND 2

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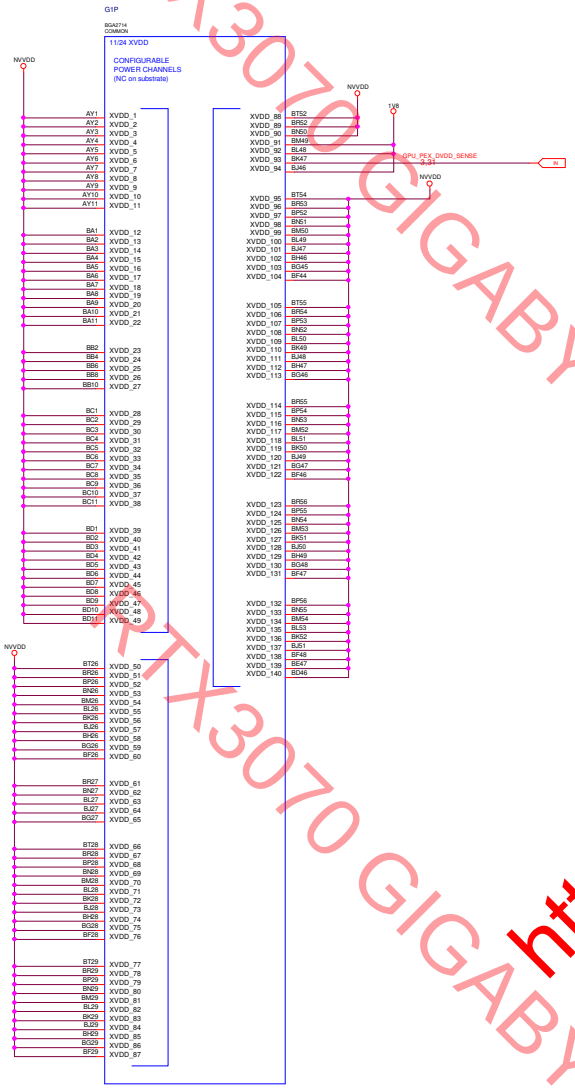

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU PWR & GND 3 (XVDD)

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GIGABYTE		
Title: Page17: XVDD		
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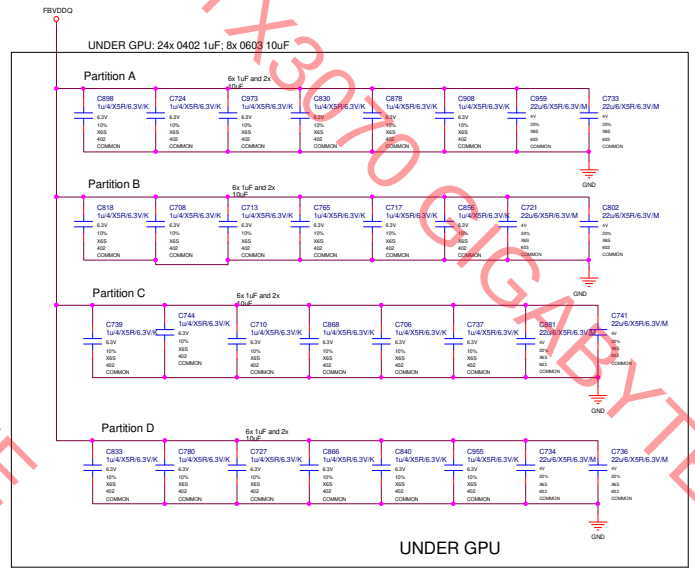
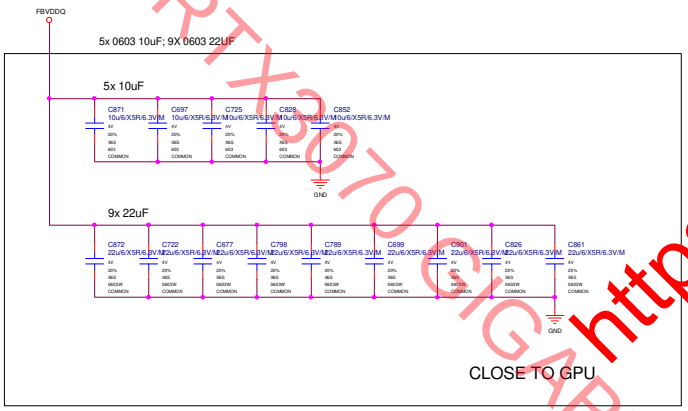
Page18: GPU DECOUPLING FBVDDQ

FBVDDQ





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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU DECOUPLING FBVDDQ

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GIGABYTE		
Title: Page18: GPU DECOUPLING FBVDDQ		
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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU DECOUPLING NVVDD

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GIGABYTE			
Title	Page19: GPU DECOUPLING NVVDD		
Size	Document Number		Rev
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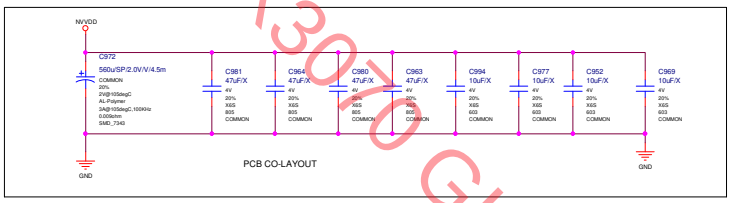
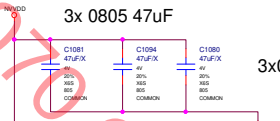


3x 0805 47uF



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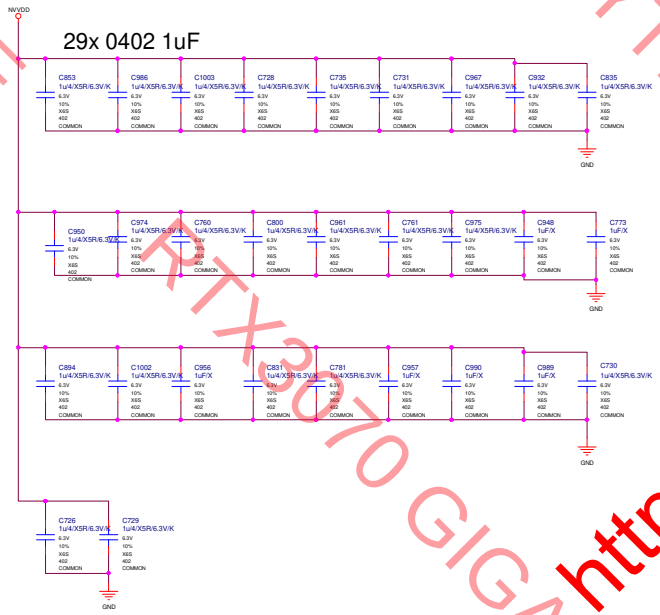
29x 0402 1uF



UNDER GPU

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU DECOUPLING NVVDD

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GIGABYTE		
Title: Page20: GPU DECOUPLING NVVDD		
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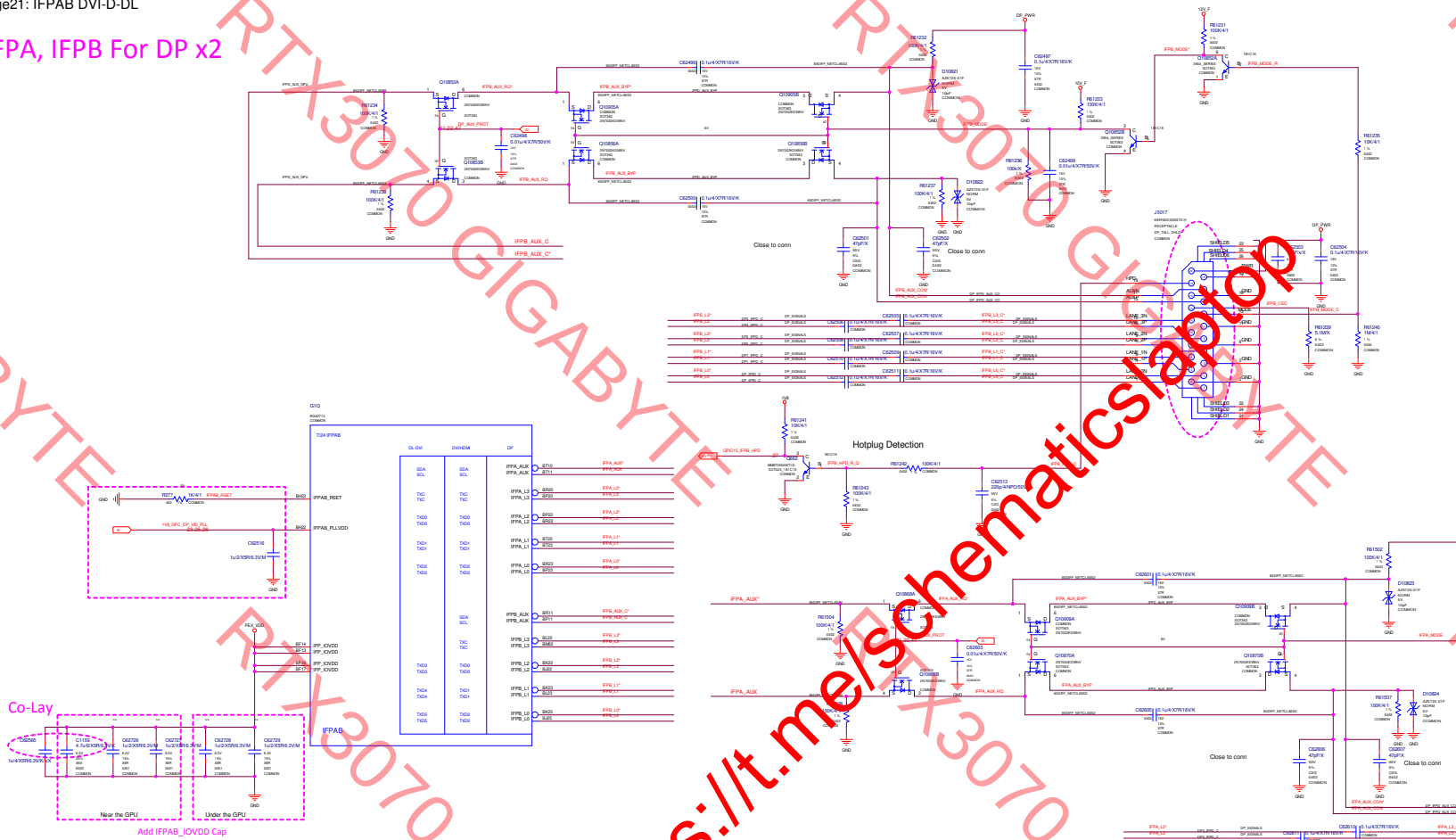
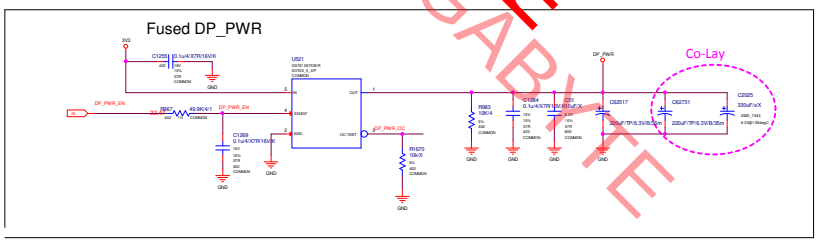
Page21: IFPAB DVI-D-DL

IFPA, IFPB For DP x2





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GIGABYTE			
Title	Page21: IFPAB DVI-D-DL		
Size: D	Document Number: GV-N3070AORUS M-8GD		Rev: 1.0
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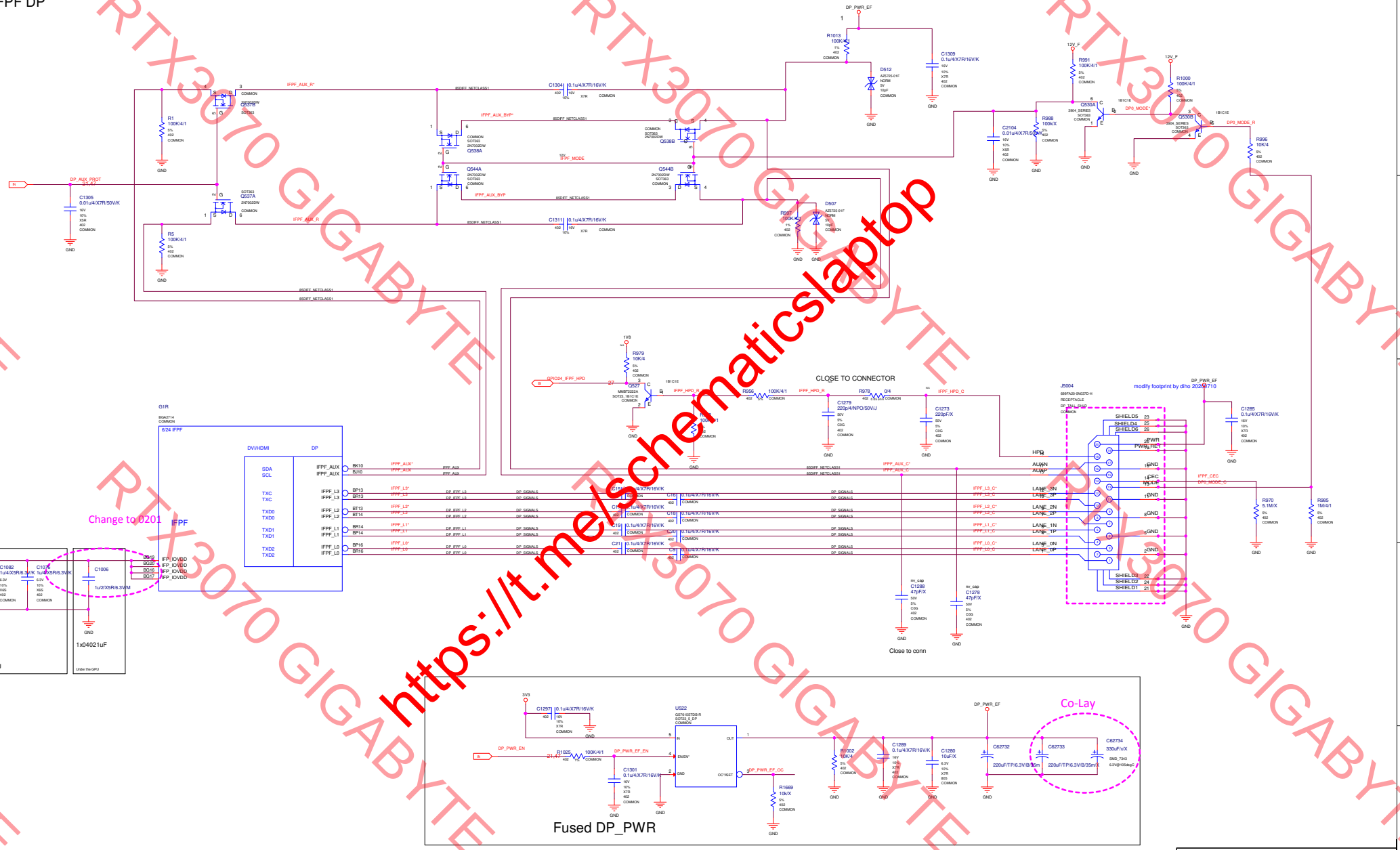

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Title	Page22: IFPF DP
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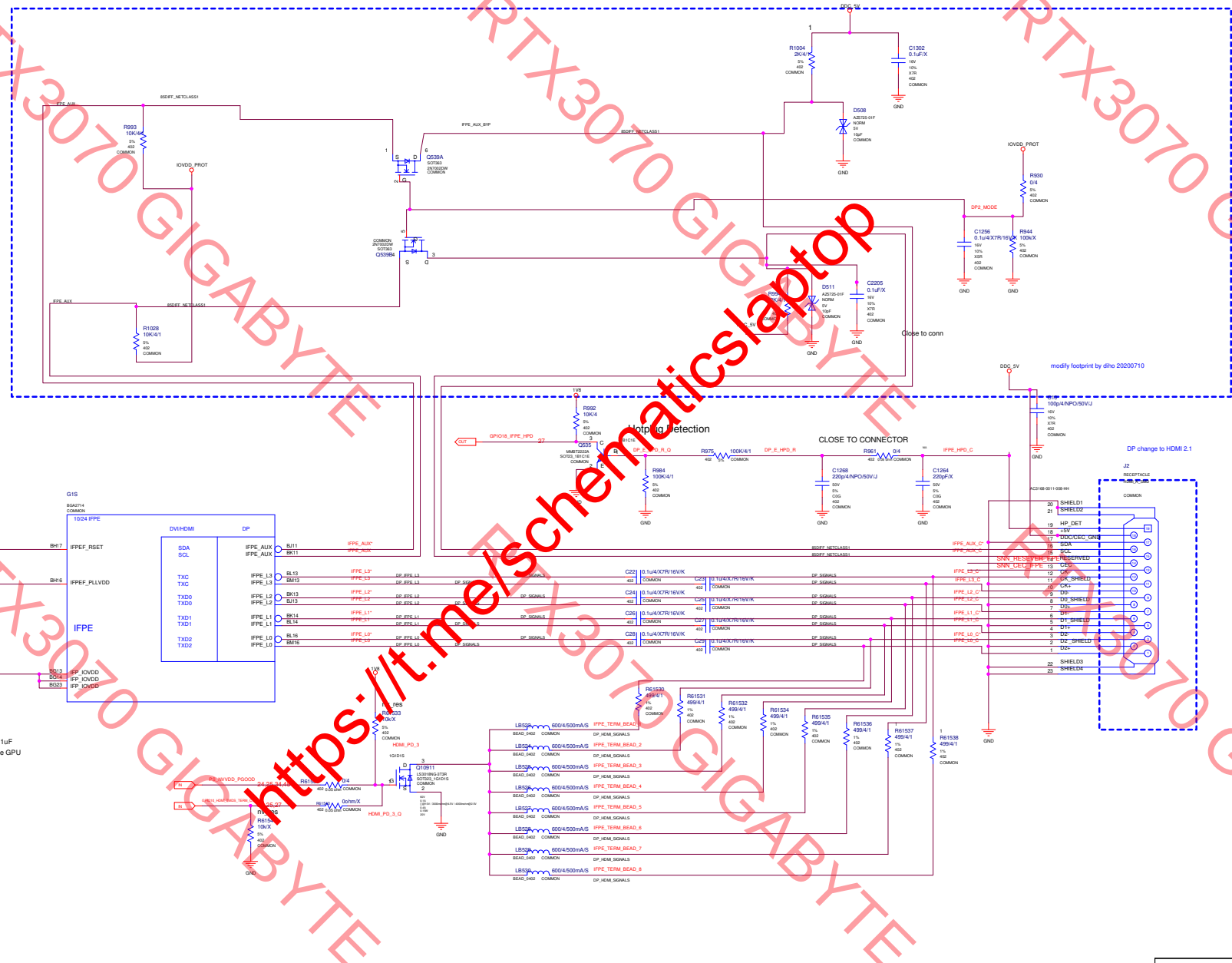
Page23: IFPE DP


IFPE_AUX
IOVDD_PROT
R993 10K/4
R1028 10K/4/1
Q539A
Q539B4
IFPE_AUX_BYP
DDC_5V
R1004 2K/4/1
C1302 0.1uF/X
D508
IOVDD_PROT
R930 0/4
DP2_MODE
C1256 0.1u/4/X7R/16V/K
R944 100K/X
D511
C2205 0.1uF/X
Close to conn
modify footprint by dlho 20200710
1V8
R992 10K/4
Q535
GPIO18_IFPE_HPD
Hotplug Detection
R984 100K/4/1
R975 100K/4/1
DP_E_HPD_R
CLOSE TO CONNECTOR
R961 0/4
IFPE_HPD_C
C1268 220p/4/NPO/50V/J
C1264 220pF/X
C1 100p/4/NPO/50V/J
DP change to HDMI 2.1
J2
RECEPTACLE
SHIELD1
SHIELD2
HP_DET
+3V
DDC/CEC_GND
SDA
SCL
RESERVED
CEC
DP_SHIELD
CK+
CK-
D0_SHIELD
D0+
D0-
D1_SHIELD
D1+
D1-
D2_SHIELD
D2+
SHIELD3
SHIELD4
SNN_RESEVED
SNN_CEC_IFPE
G1S
10/24 IFPE
DVI/HDMI
DP
IFPE_RSET
IFPE_PLLVDD
IFPE
SDA
SCL
TXC
TXC
TXD0
TXD0
TXD1
TXD1
TXD2
TXD2
IFPE_AUX
IFPE_L3
IFPE_L2
IFPE_L1
IFPE_L0
R272 1K/4/1
1V8_GPC_DP_VID_PLL
C1030 1u/2/X5R/6.3V/M
C1021 1u/2/X5R/6.3V/M
PEX_VDD
1x 0402 1uF Under the GPU
1x 0402 1uF Under the GPU
Change to 0201
IFP_IOVDD
IFP_IOVDD
IFP_IOVDD
R1533 0k/X
HDMI_PD_3
Q10911
R1534 0/4
R1535 0ohm/X
HDMI_PD_3_Q
R1536 10k/X
R1537 10K/4/1
R1538 10K/4/1
R1539 10K/4/1
R1540 10K/4/1
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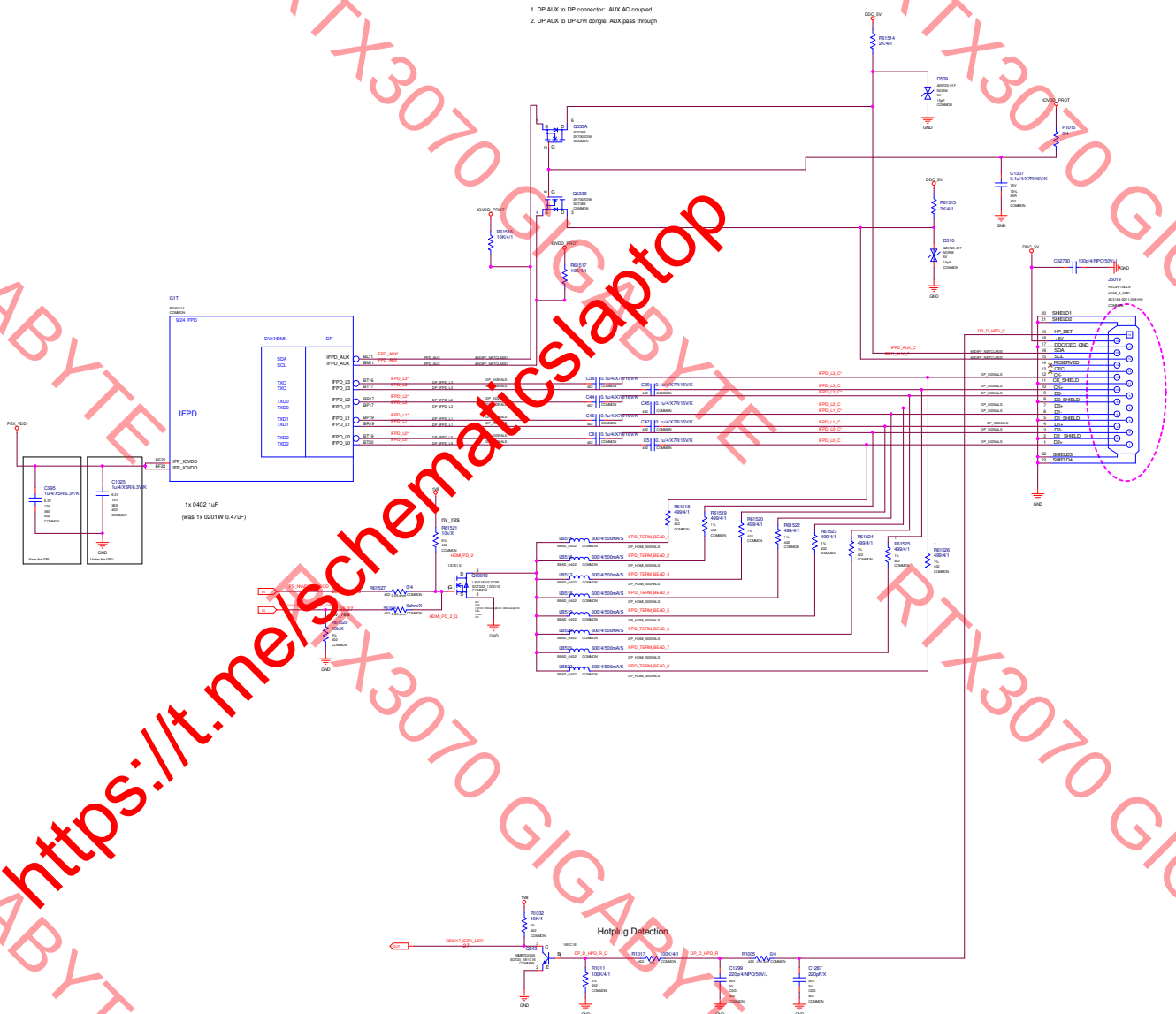

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GIGABYTE			
Title: Page24: IFPD DP			
Size: D	Document Number: GV-N3070AORUS M-8GD		Rev: 1.0
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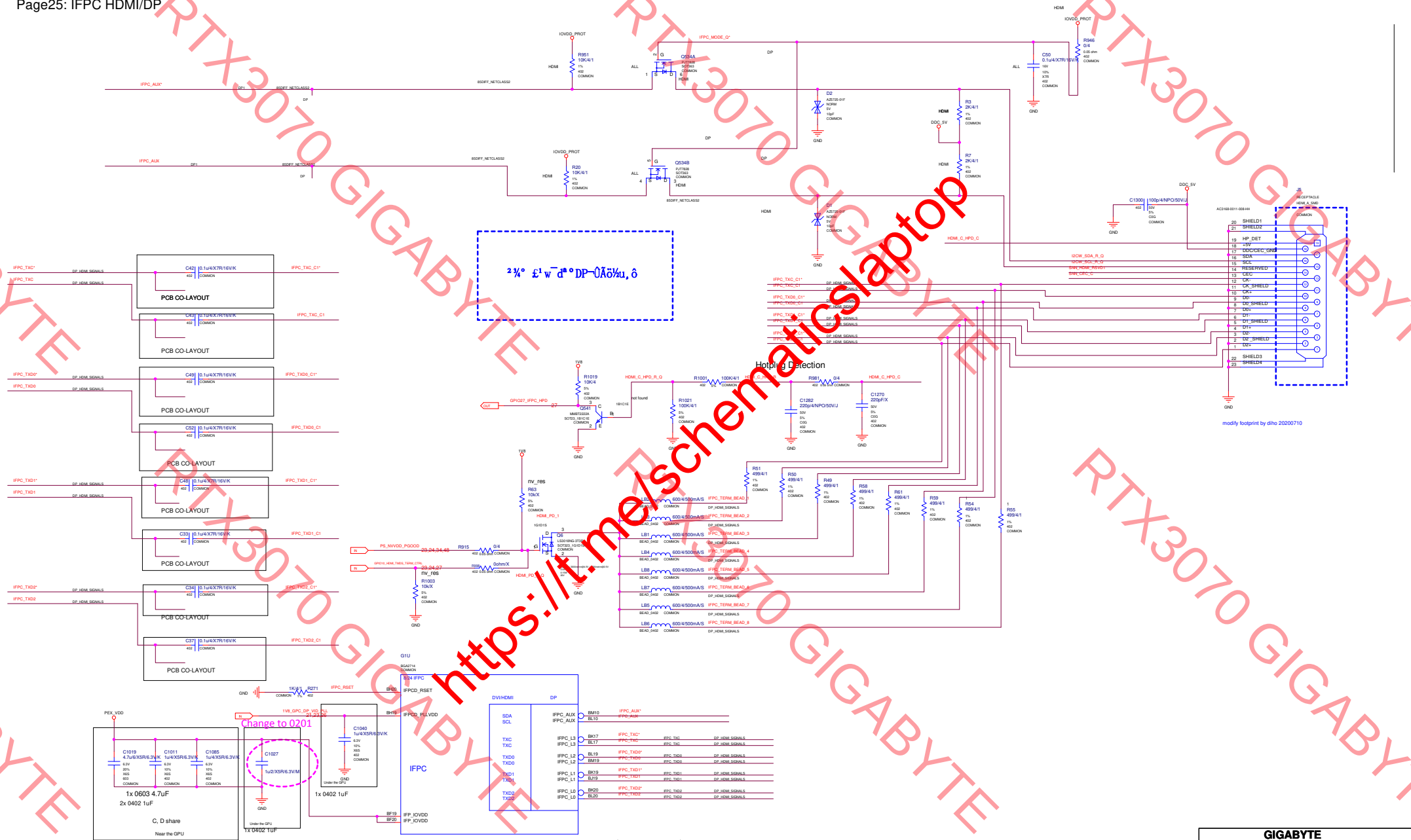

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Title	Page25: IFPC HDMI/DP
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Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
H	H	M	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

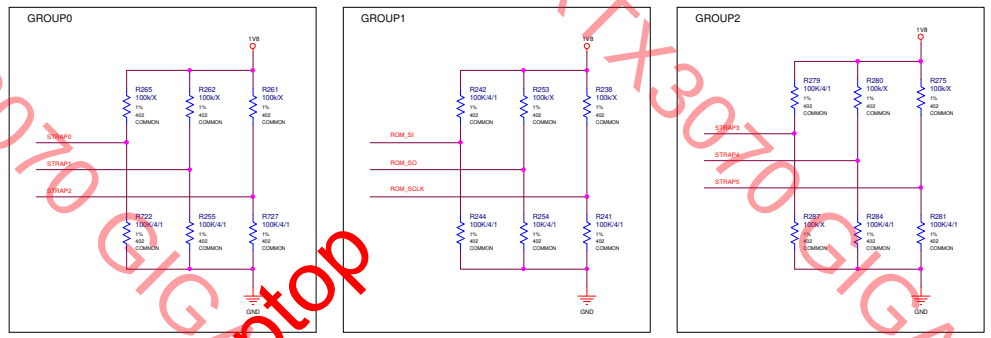
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

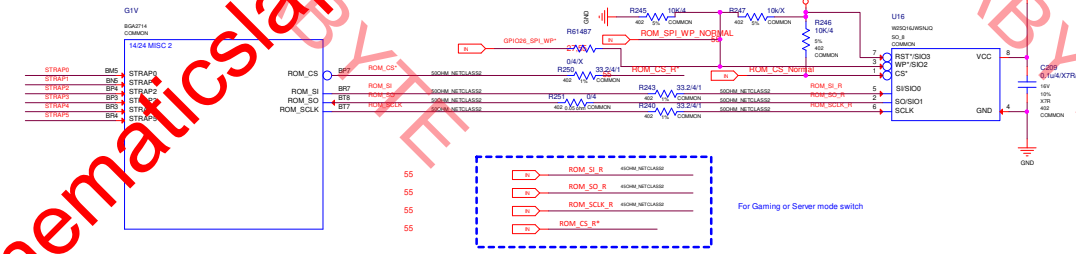
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

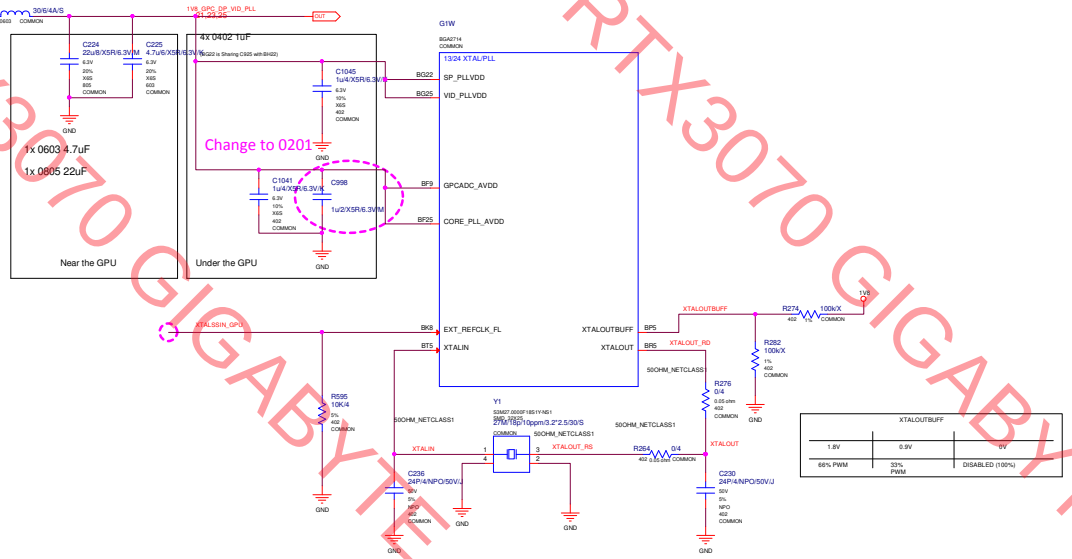
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: ROM, XTAL,STRAPS

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Title	Page26: MISC2: ROM, XTAL, Straps	
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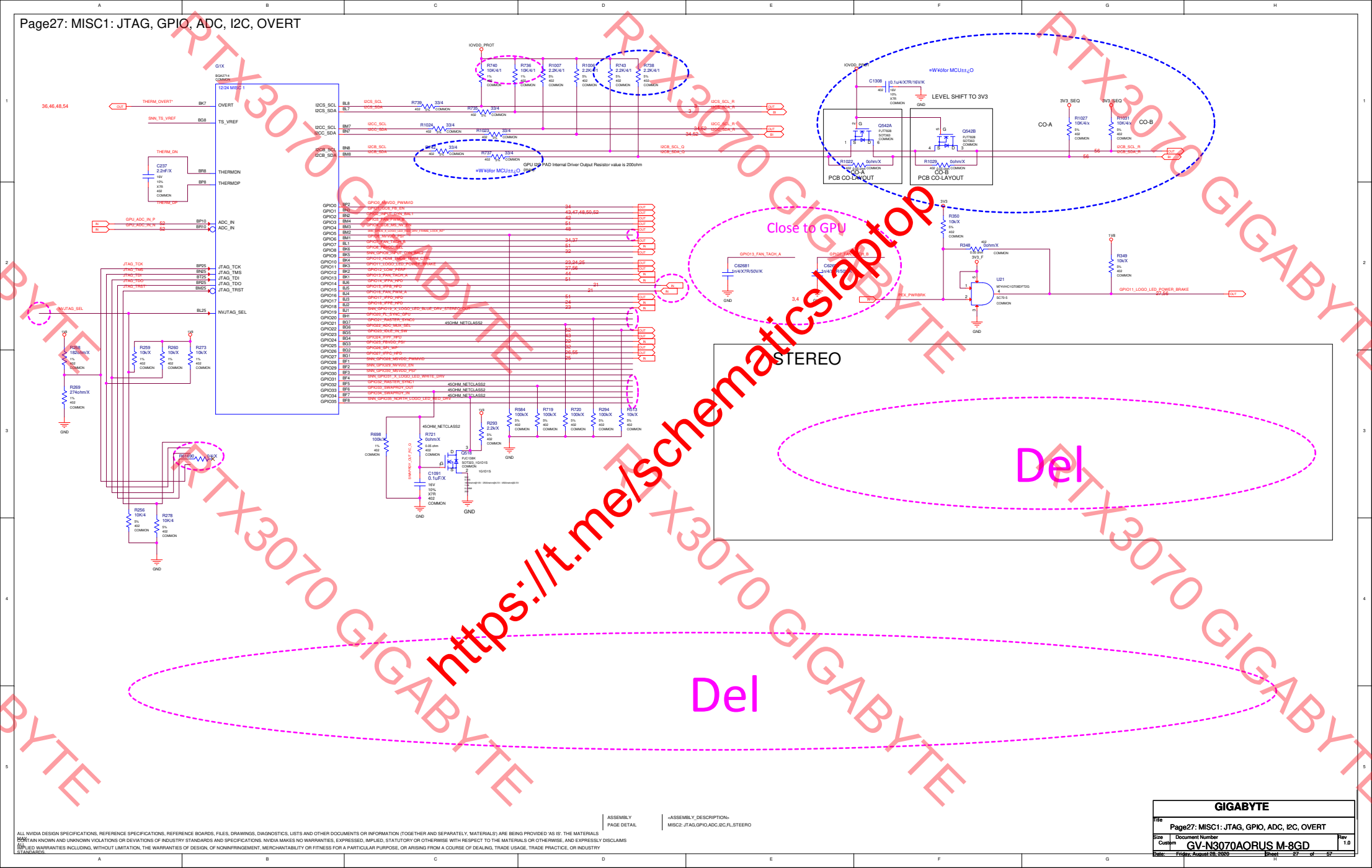

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PAGE DETAIL	MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO

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Page28: RGB

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WHITE DRIVE

LOGO LED WHITE

LOGO LED RED

RED DRIVE

GREEN DRIVE

BLUE DRIVE

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PAGE DETAIL MISC3: RGB

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Title: Page28: RGB		
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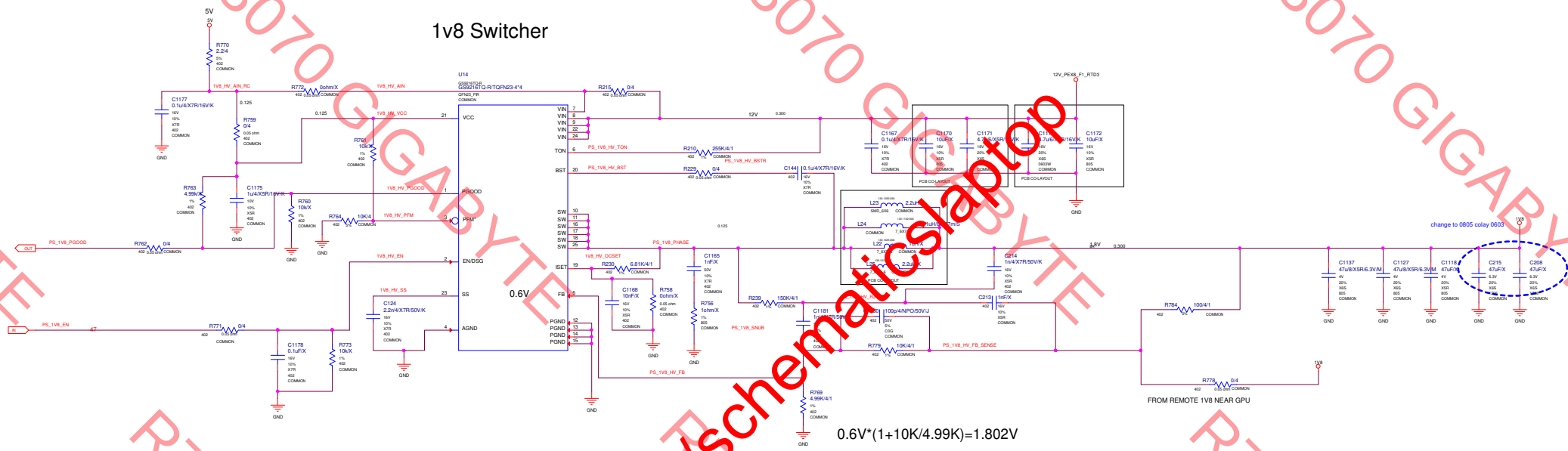

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PAGE DETAIL PS: 1V8

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Title: Page29: PS: 1V8

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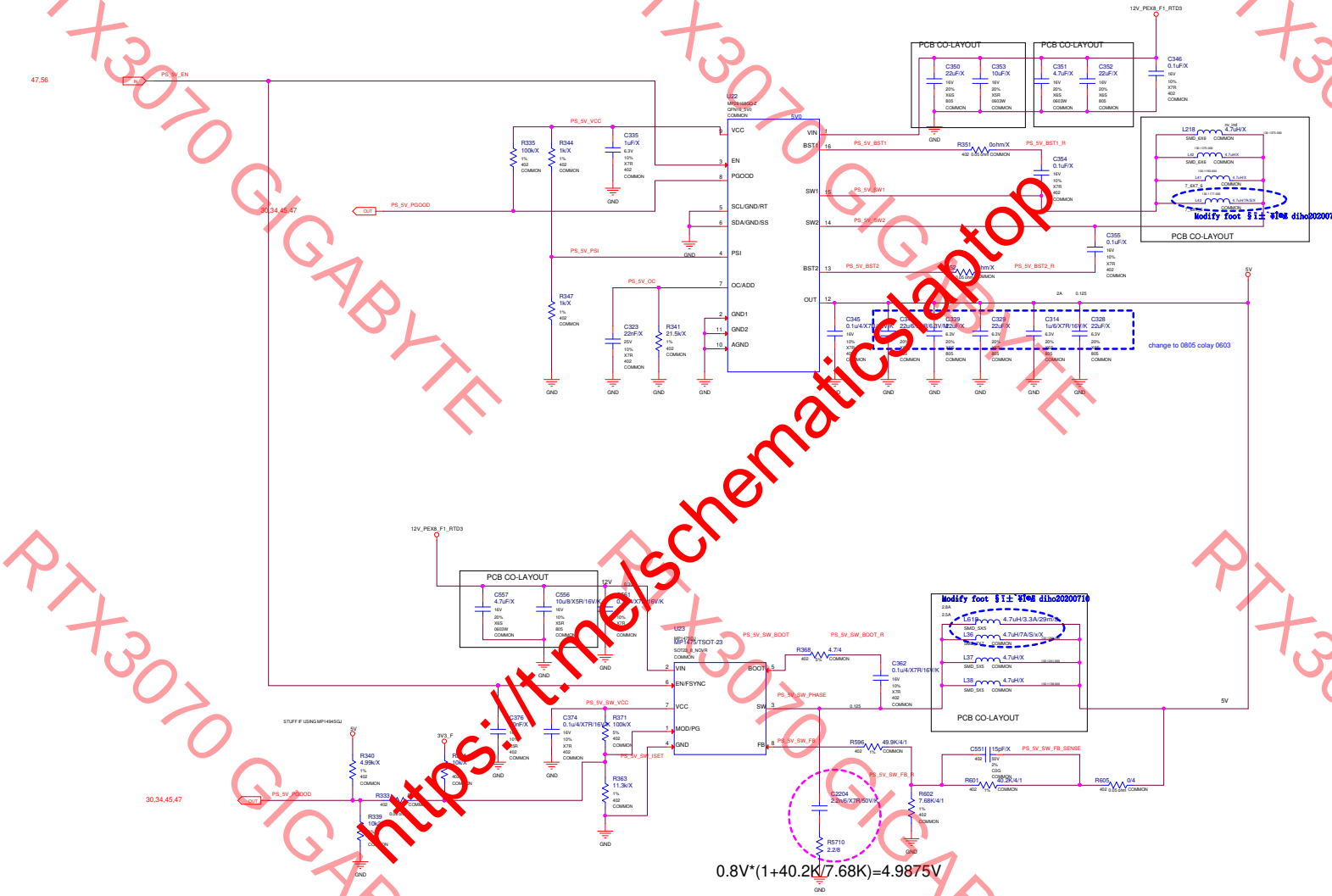

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
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Title: Page30: PS: 5V		
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
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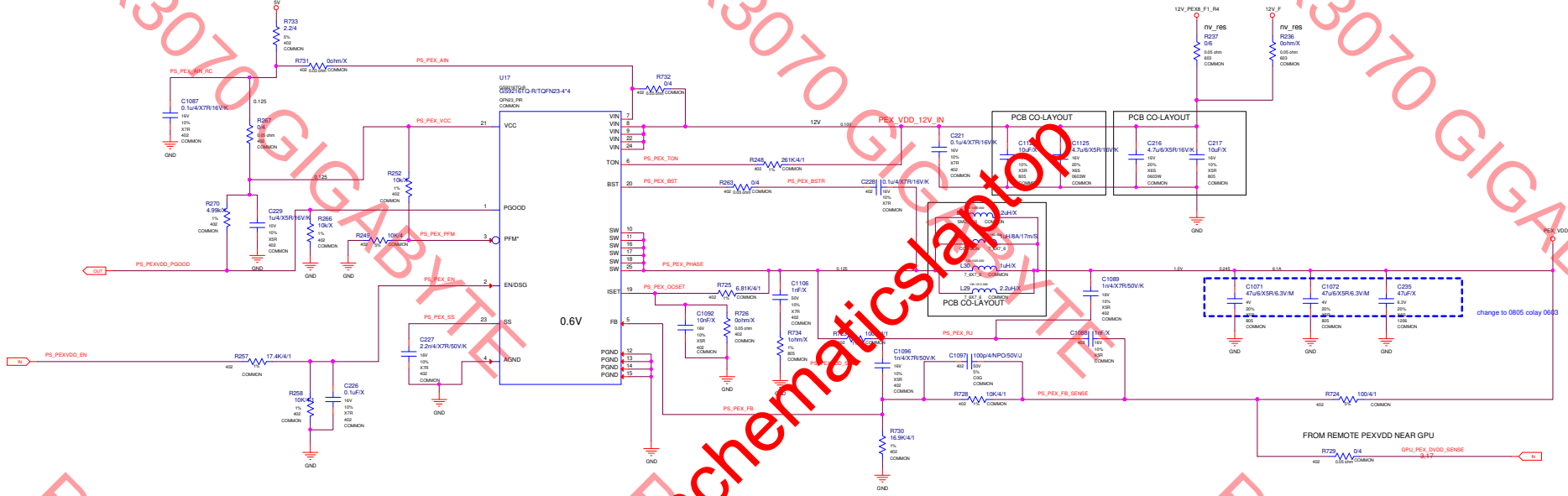
PEX Switcher



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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Title	Page31: PS: PEXVDD	
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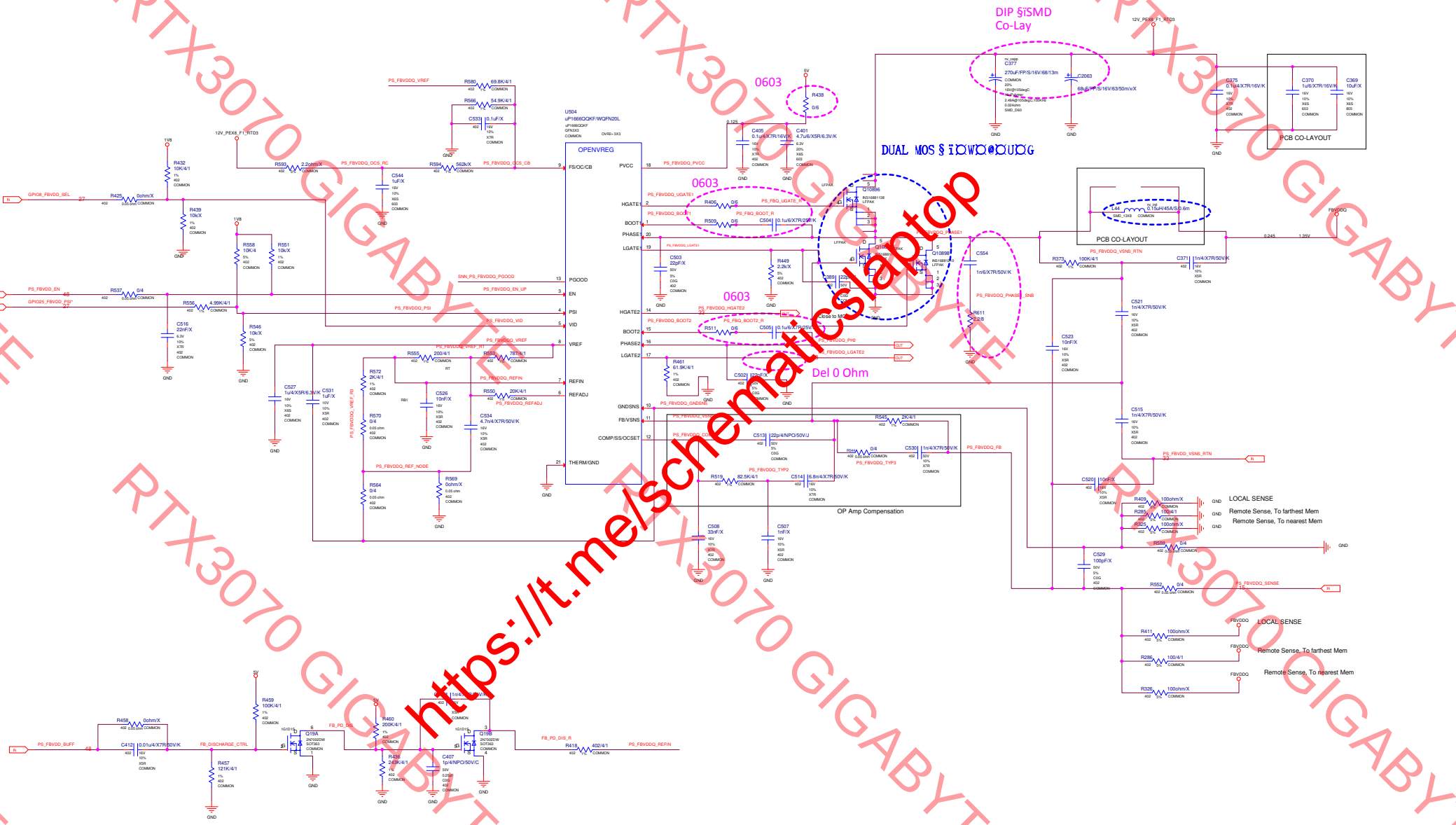

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: FBVDDQ

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Title: Page32: PS: FBVDDQ

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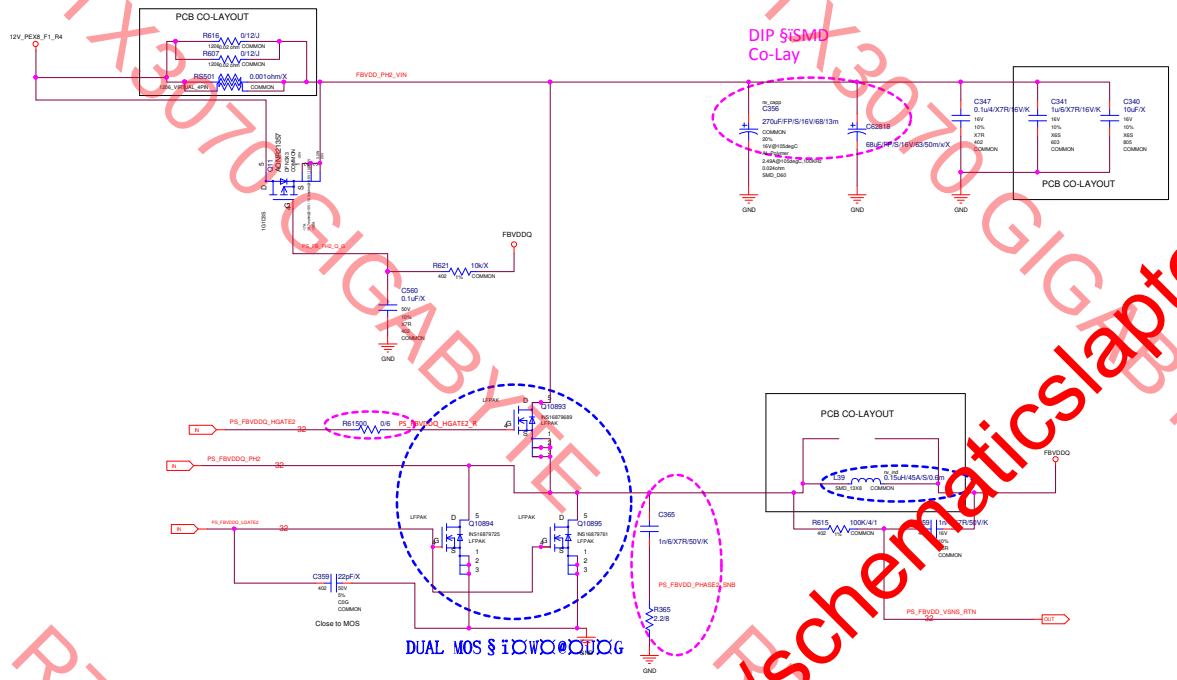
FBVDD PH2 INPUT ANTI-BACKDRIVE



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: FBVDDQ PH2

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Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
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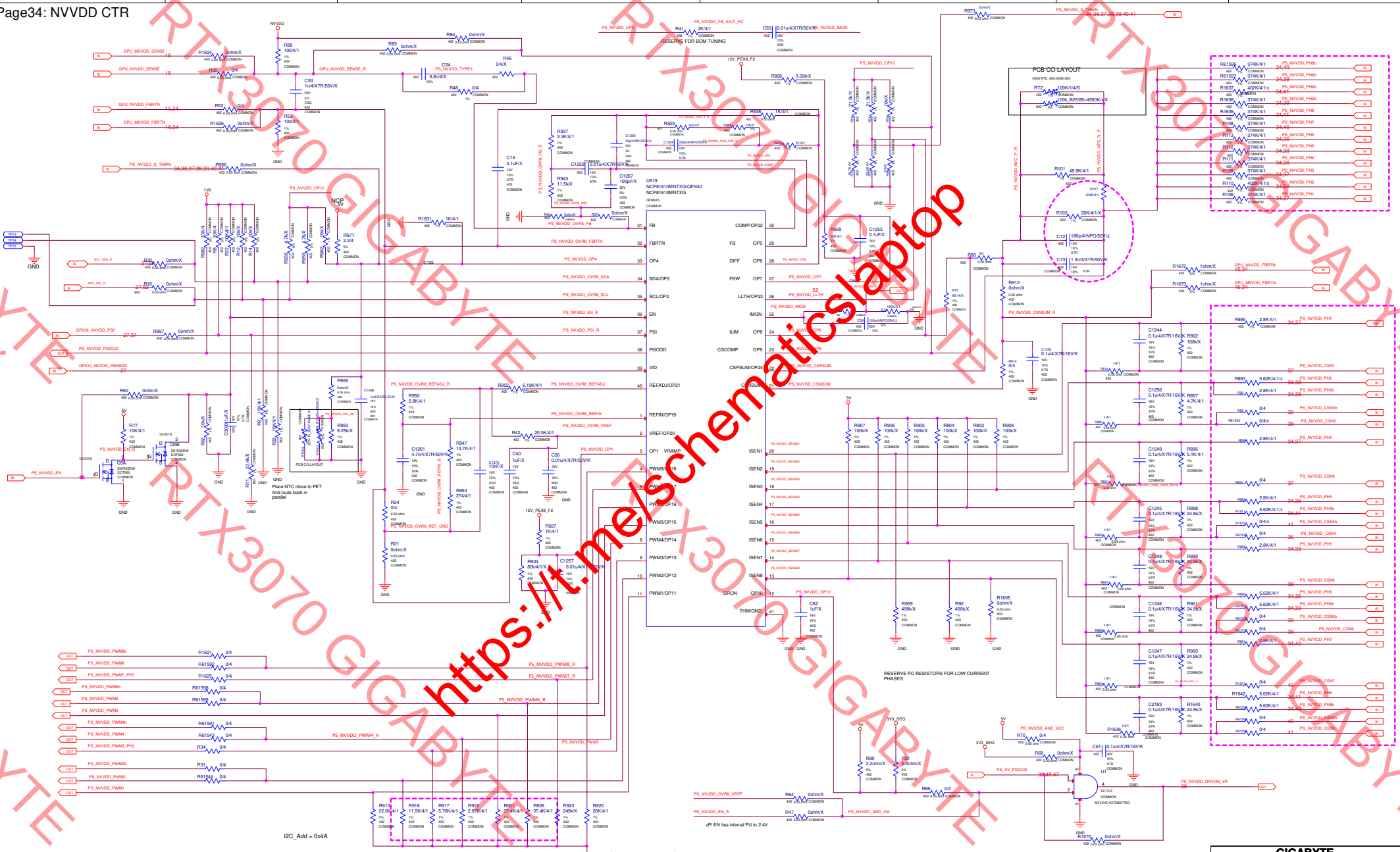

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Title: Page34: NVVDD CTR

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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	BLANK PAGE

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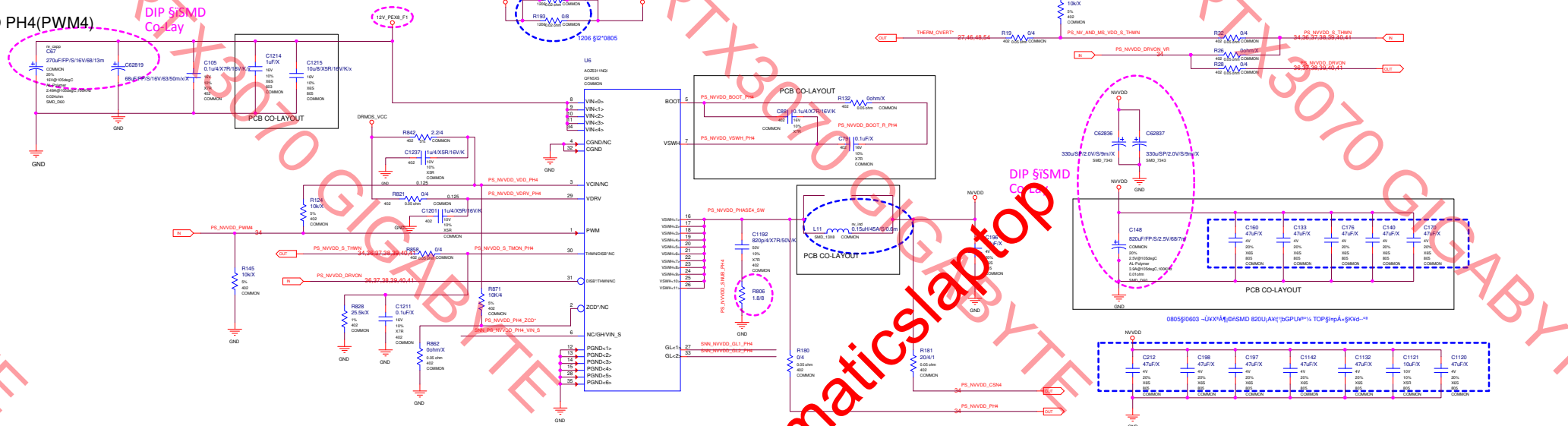
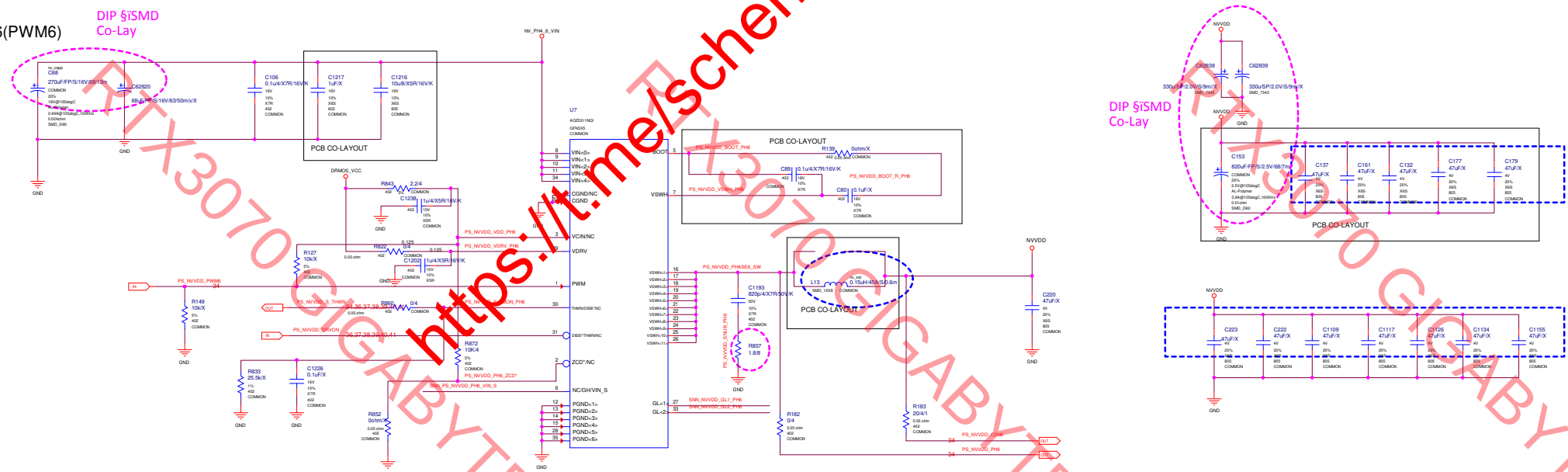
NVVDD PH4(PWM4)



NVVDD PH6(PWM6)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH4, PH6

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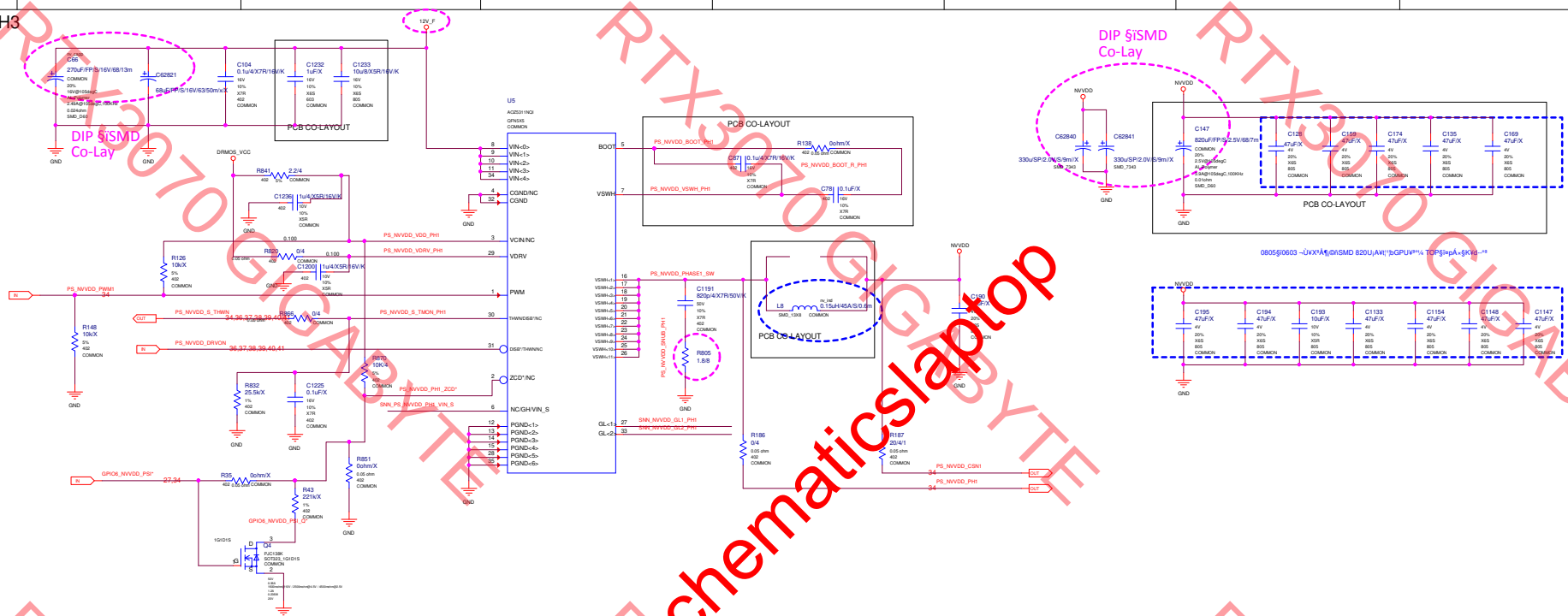
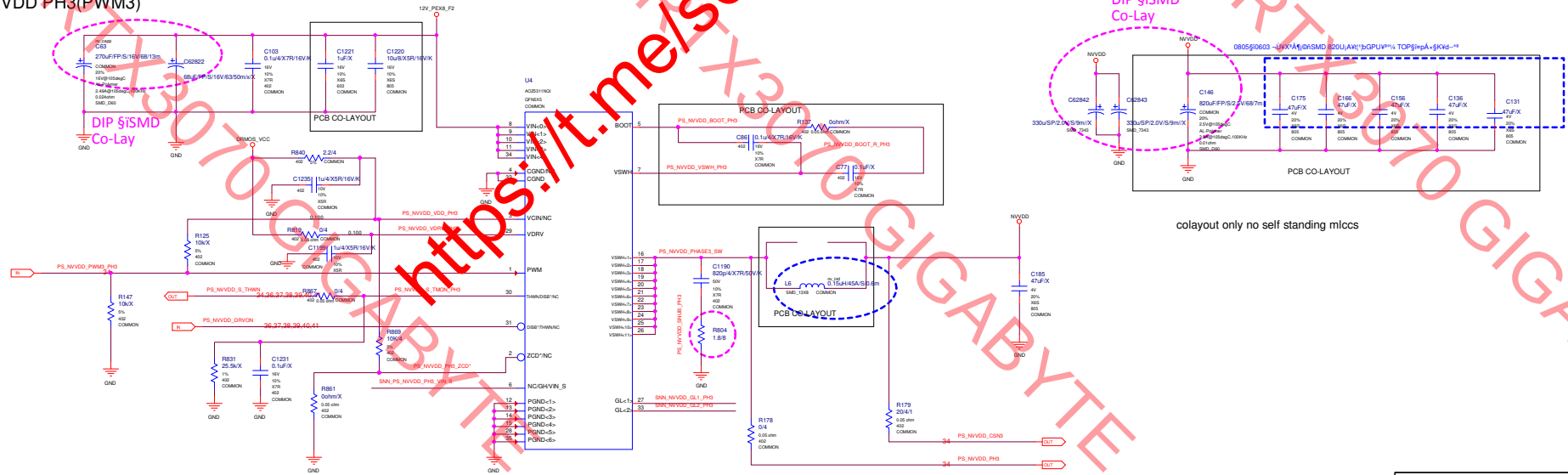
Page37: NVVDD PH1 & PH3

NVVDD PH1(PWM1)



NVVDD PH3(PWM3)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH1, PH3

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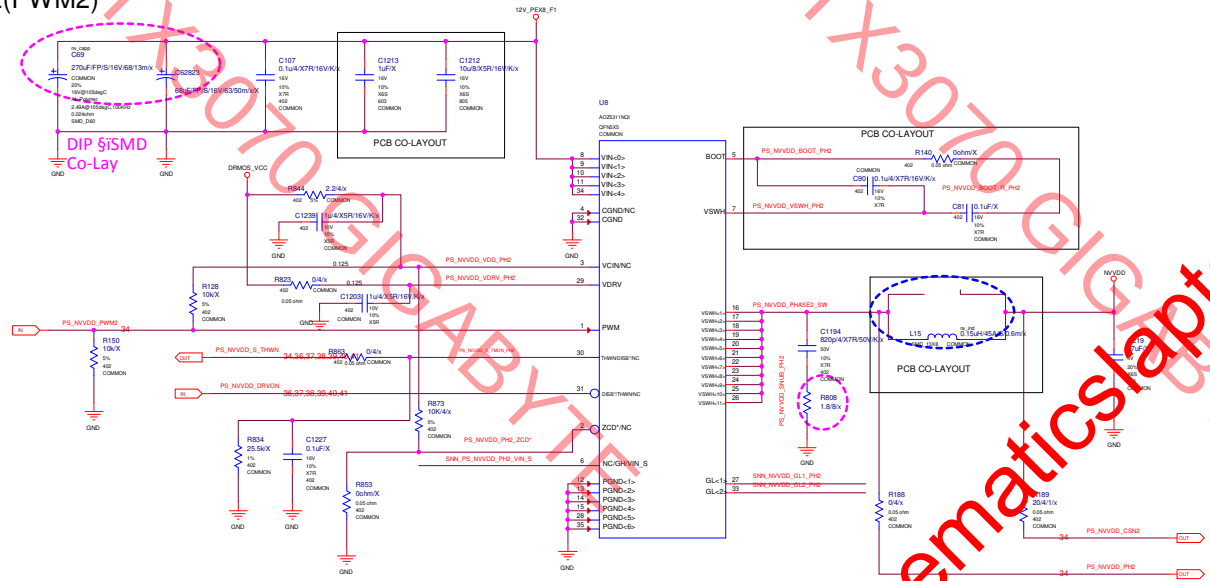
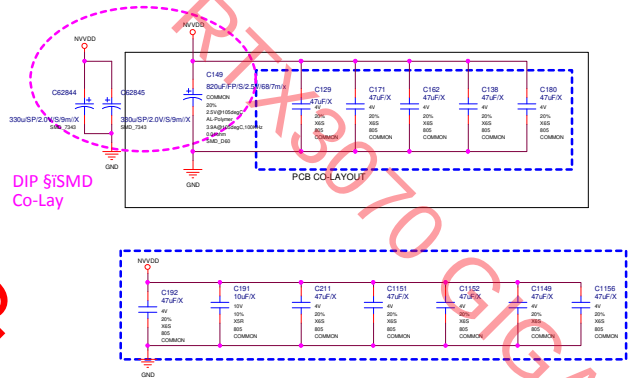
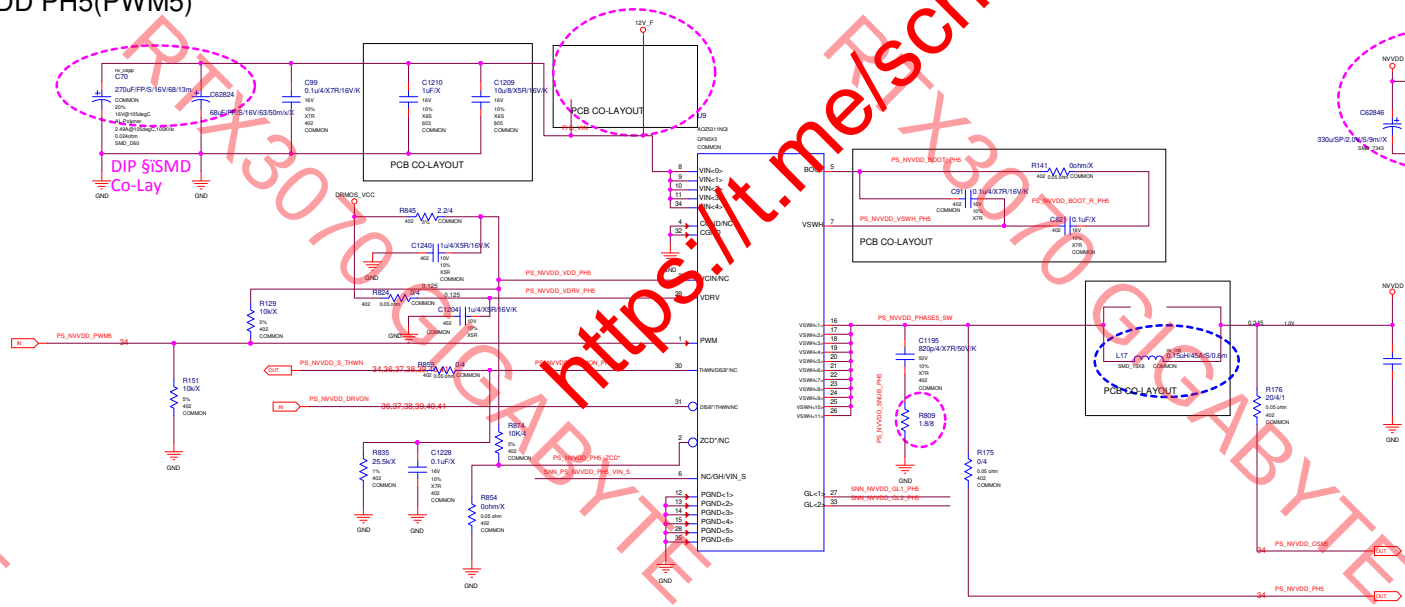
Page38: NVVDD PH2 & PH5

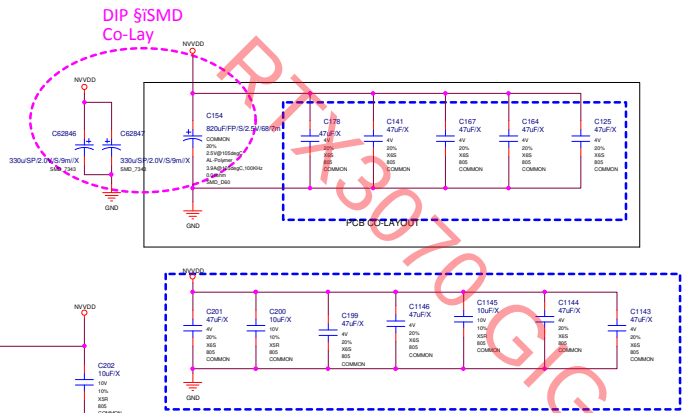
NVVDD PH2(PWM2)





NVVDD PH5(PWM5)





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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: NVVDD PH2, PH5

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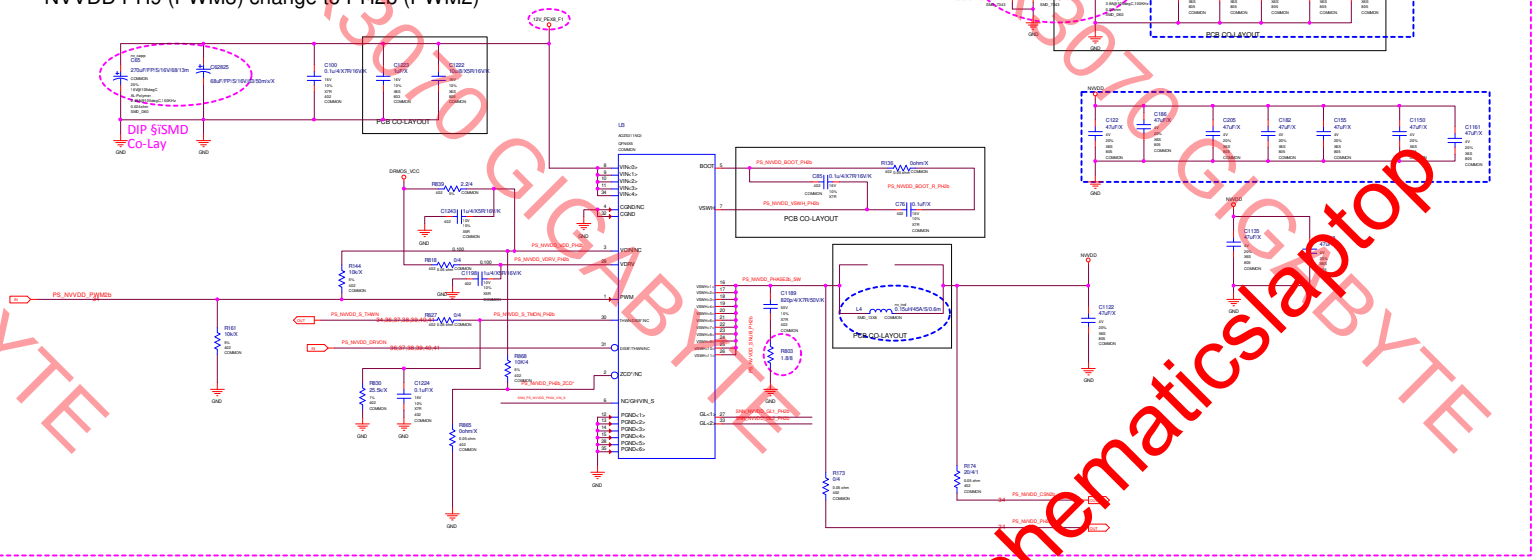
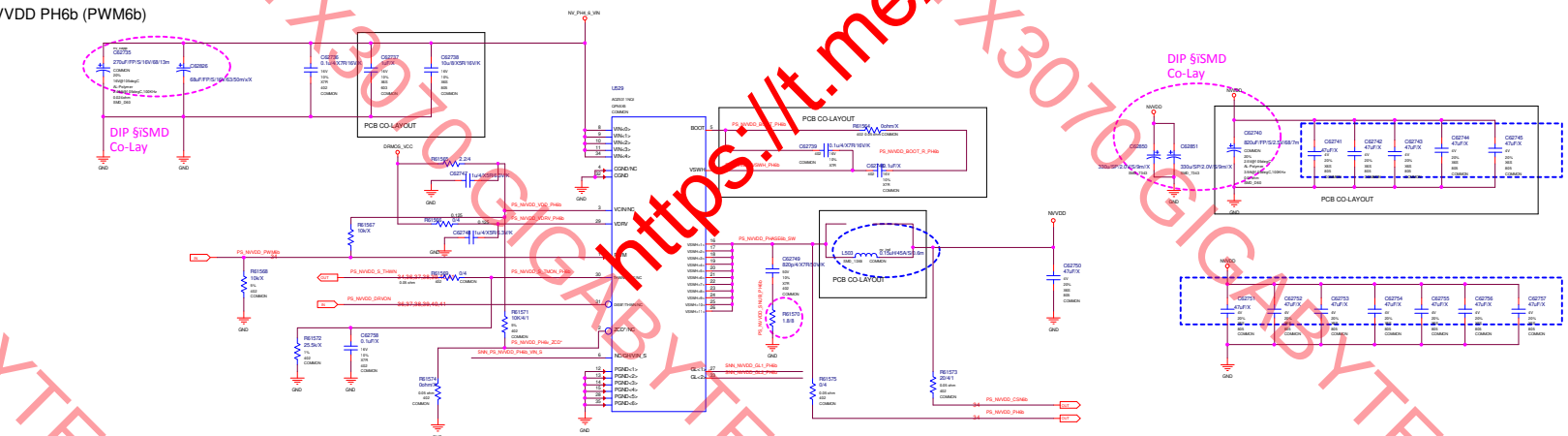
Page39: NVVDD PH2b

NVVDD PH9 (PWM3) change to PH2b (PWM2)



NVVDD PH6b (PWM6b)



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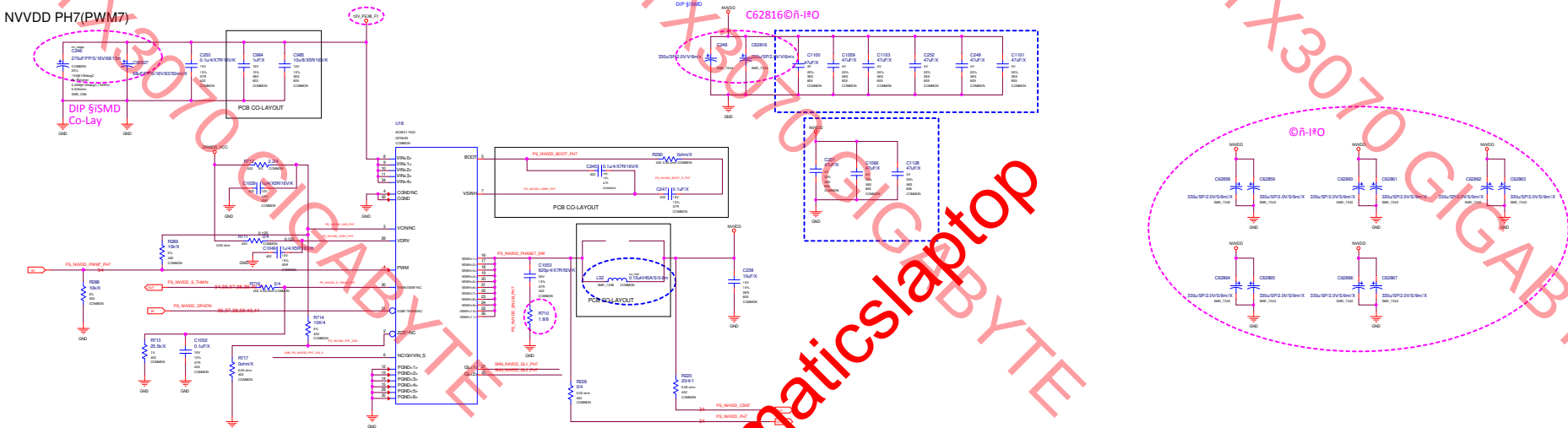
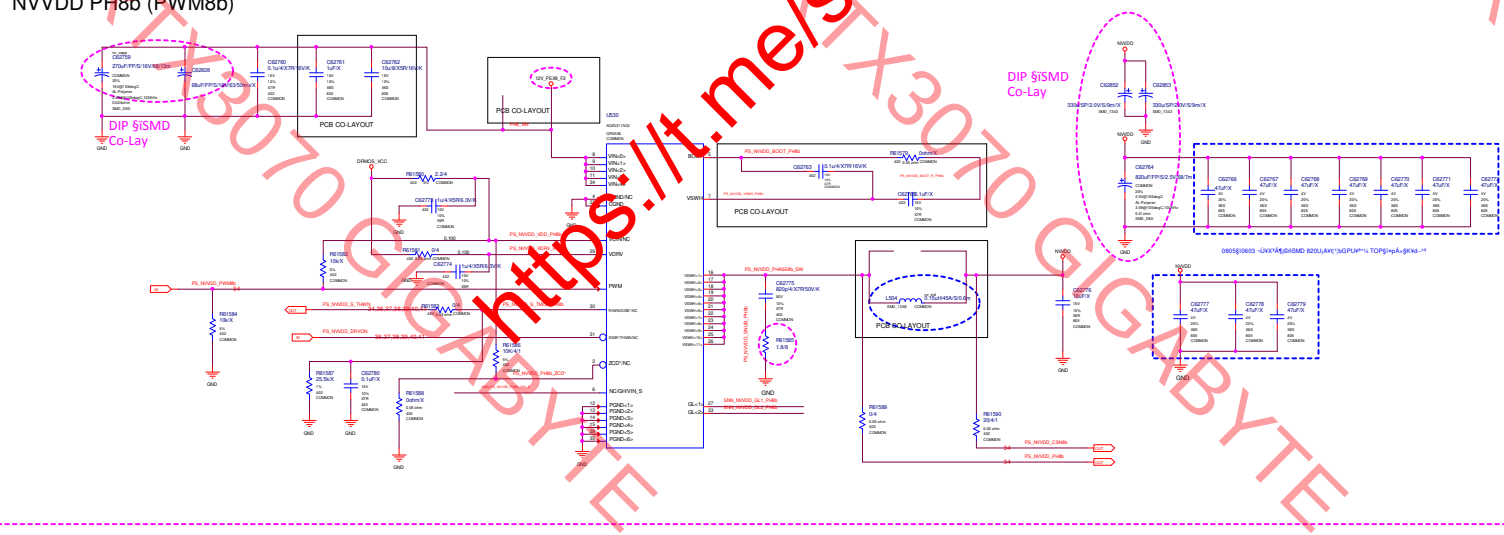
NVVDD PH7(PWM7)



NVVDD PH8b (PWM8b)



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Title	Page40: NVVDD PH7
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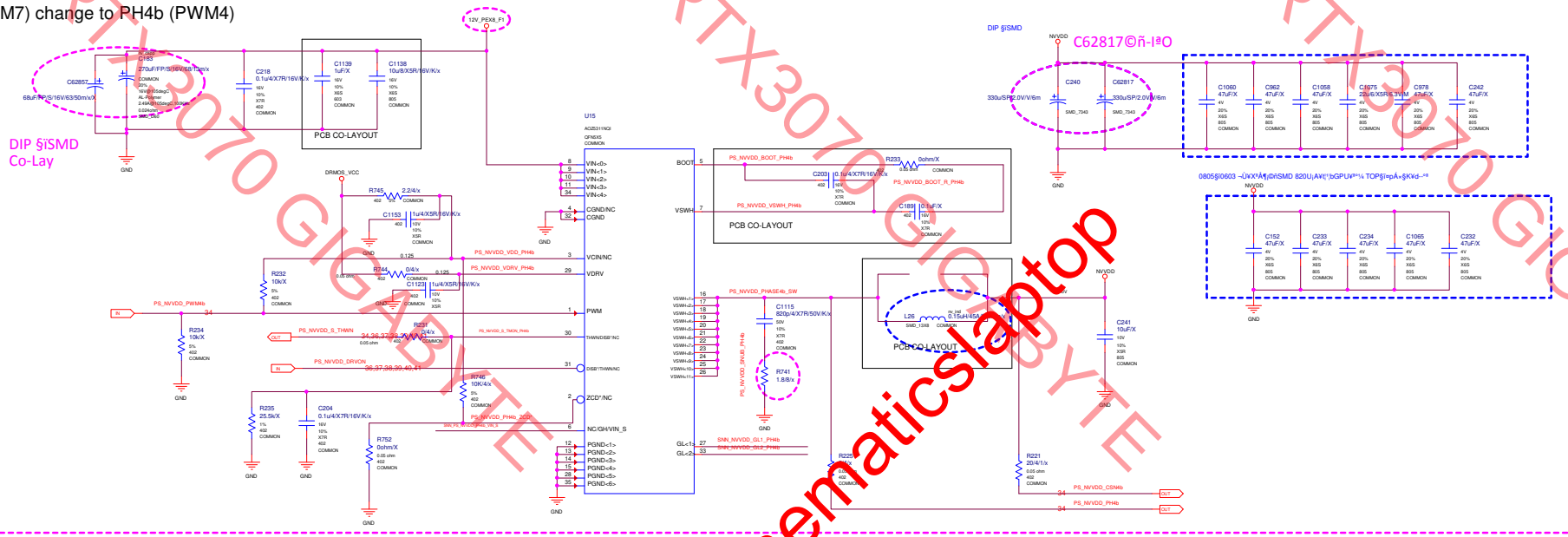
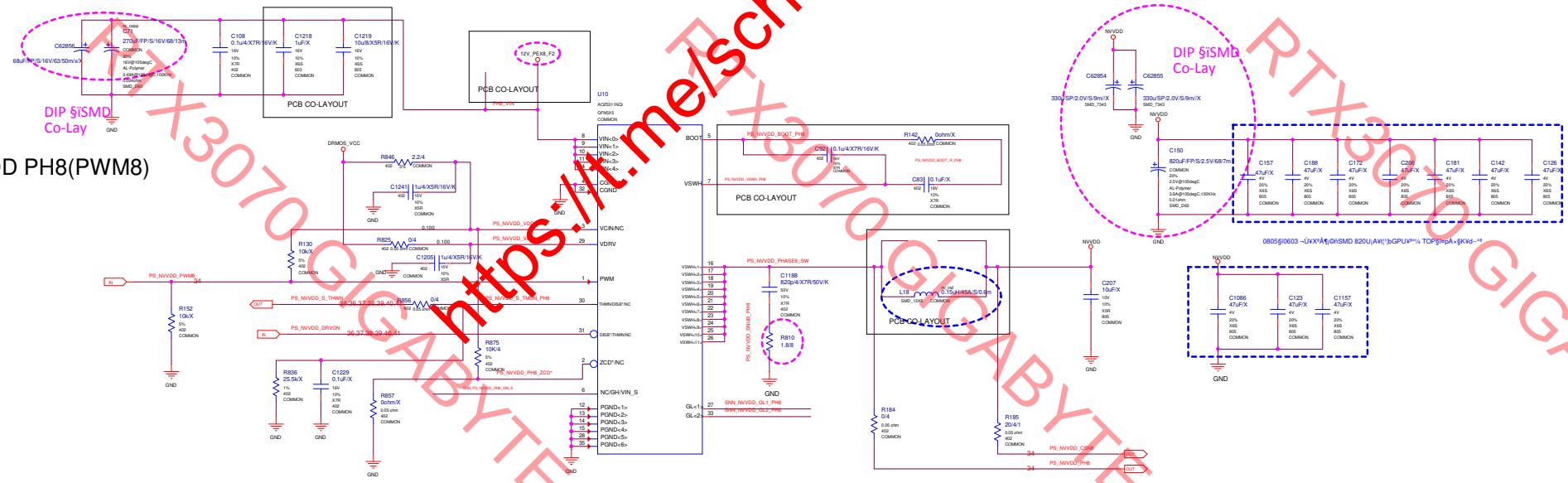
Page41: NVVDD PH4b & 8

NVVDD PH10(PWM7) change to PH4b (PWM4)



NVVDD PH8(PWM8)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH10, PH8

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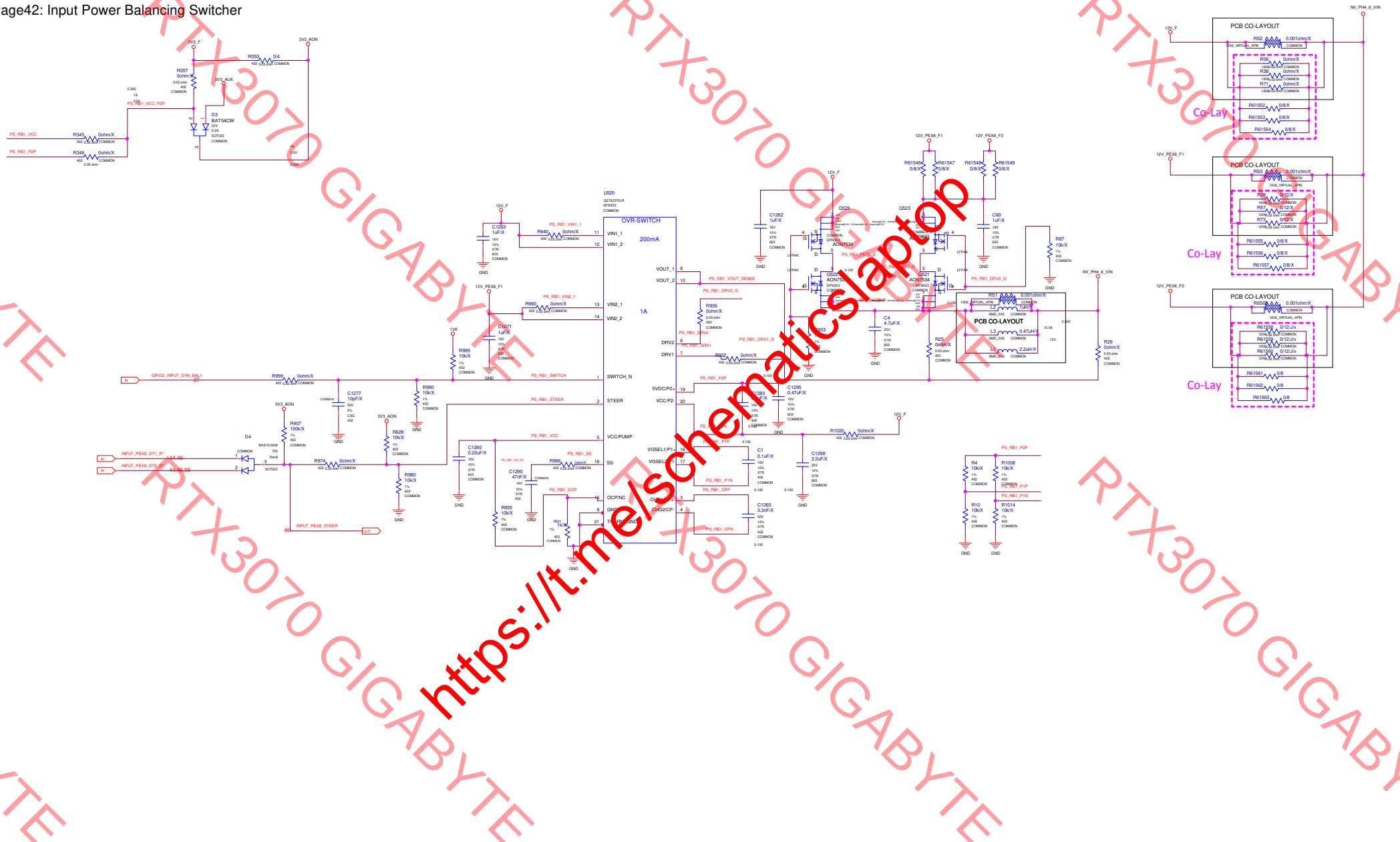
Page42: Input Power Balancing Switcher



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: OVRS_INPUT POWER BALANCE

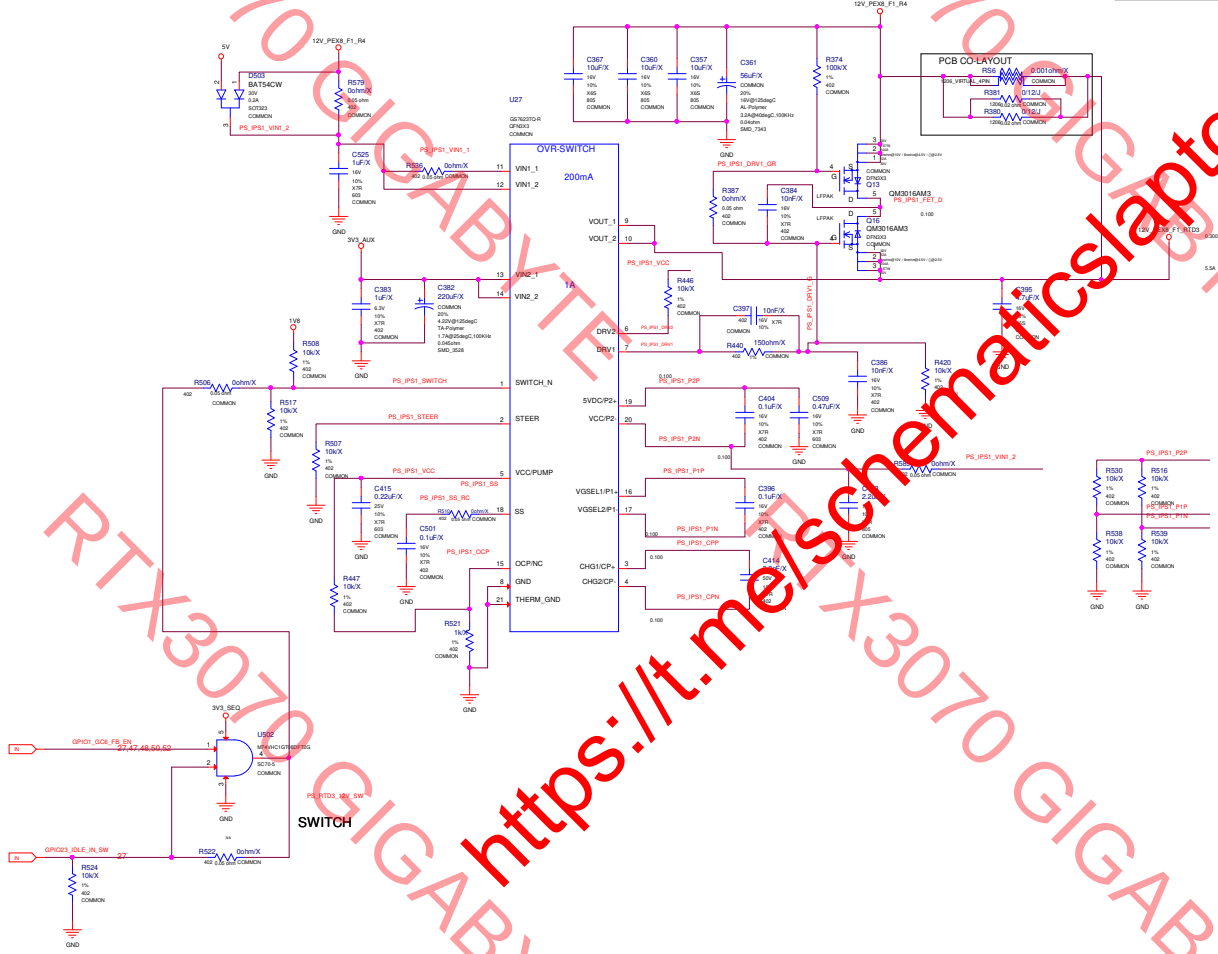
GIGABYTE		
Title: Page42: Input Power Balancing Switcher		
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Thursday, August 06, 2020	Sheet 42 of 57	

Page43: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: RDT3_12V & 3V3_A Switcher

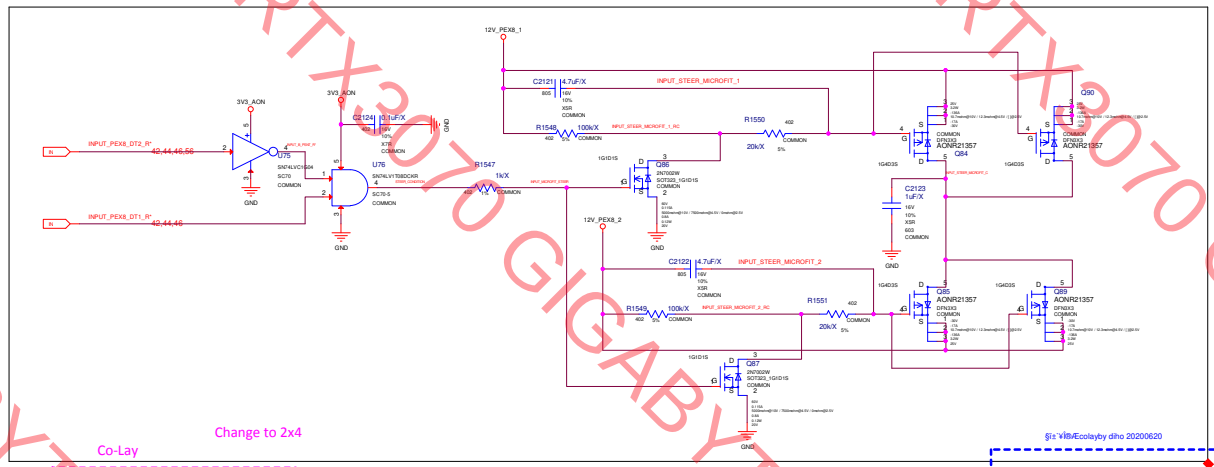
GIGABYTE

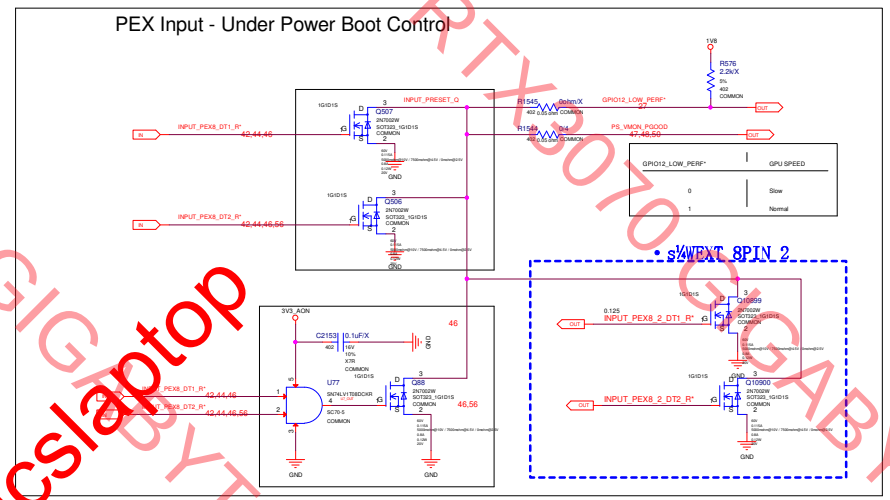
Title: Page42: Input Power Balancing Switcher

Size: Custom | Document Number: GV-N3070AORUS M-8GD | Rev: 1.0

Date: Tuesday, August 04, 2020 | Sheet 43 of 57

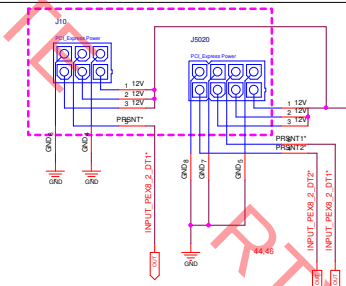
Page44: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT

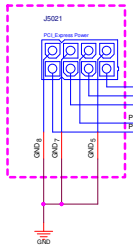


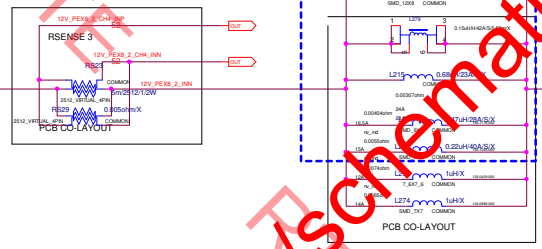


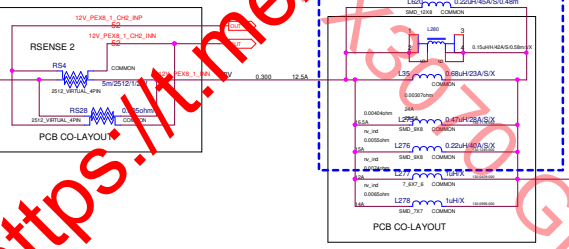
Co-Lay

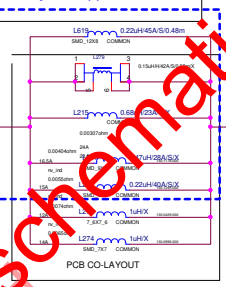
Change to 2x4

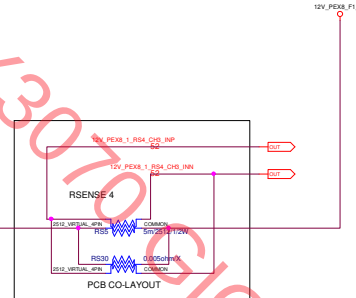


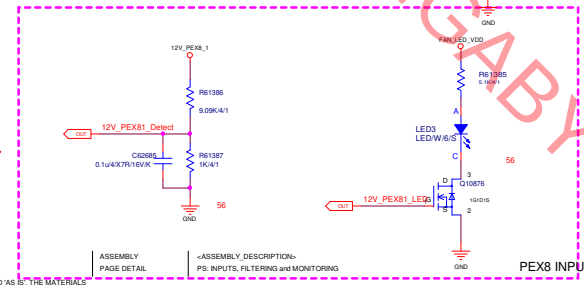


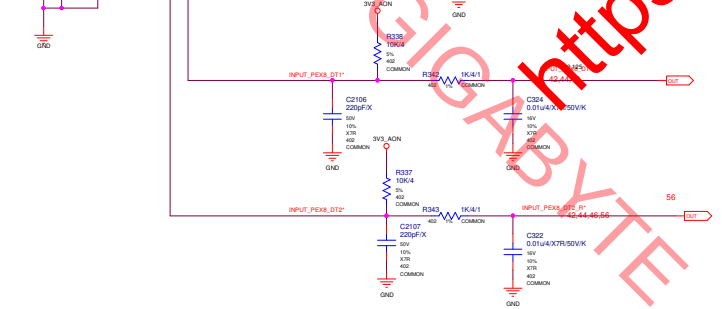












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ASSEMBLY
PAGE DETAIL
<ASSEMBLY_DESCRIPTION>
PS: INPUTS, FILTERING and MONITORING

PEX8 INPUT 2 - 2x4 PCIE CON 150W

GIGABYTE

Title	12V_EXT_INPUT, FILTERING & UNDER POWER BOOT	
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Thursday, August 06, 2020	Sheet 44 of 57	

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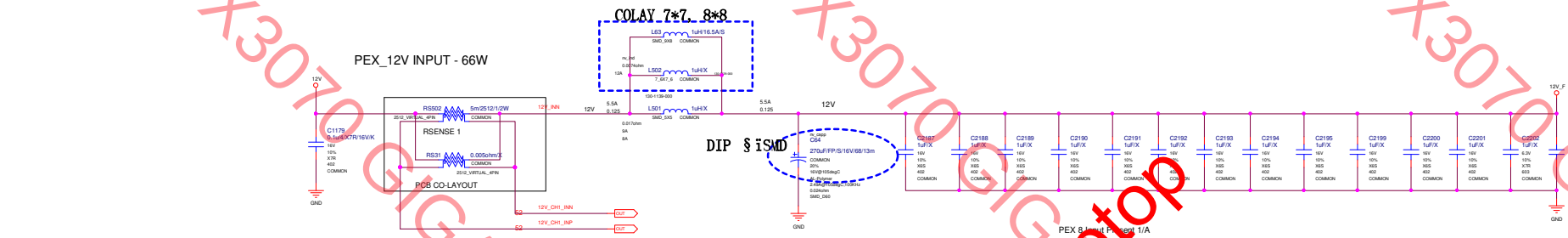

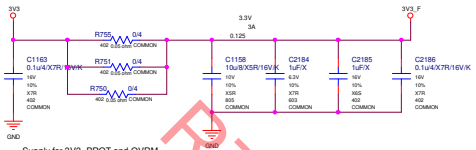

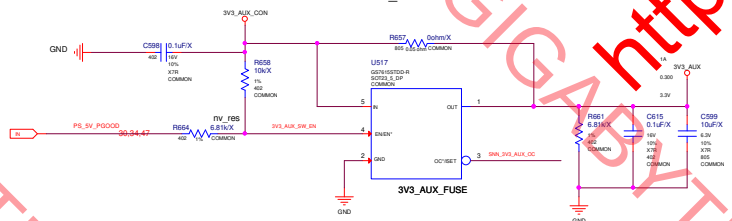

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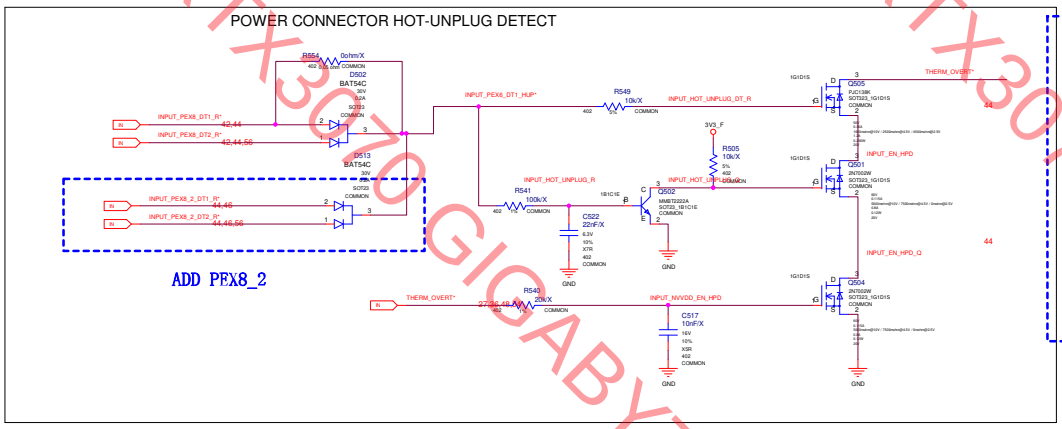
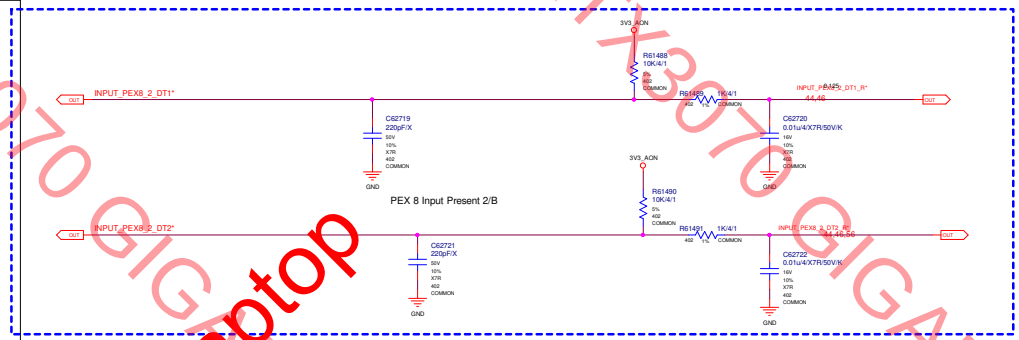
ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: PEX_12V, PEX_3V3 AND A3V3_AUX

GIGABYTE		
Title: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX		
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 45 of 57	

Page46: STEERING, UPB, HOT UNPLUG

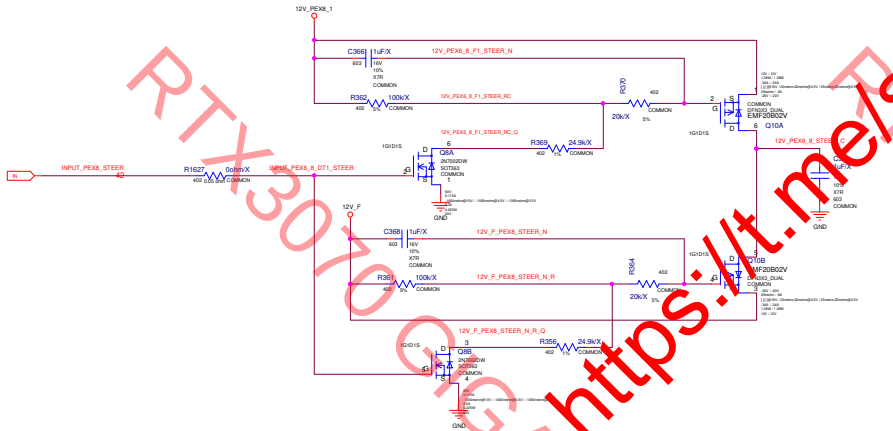
POWER CONNECTOR HOT-UNPLUG DETECT





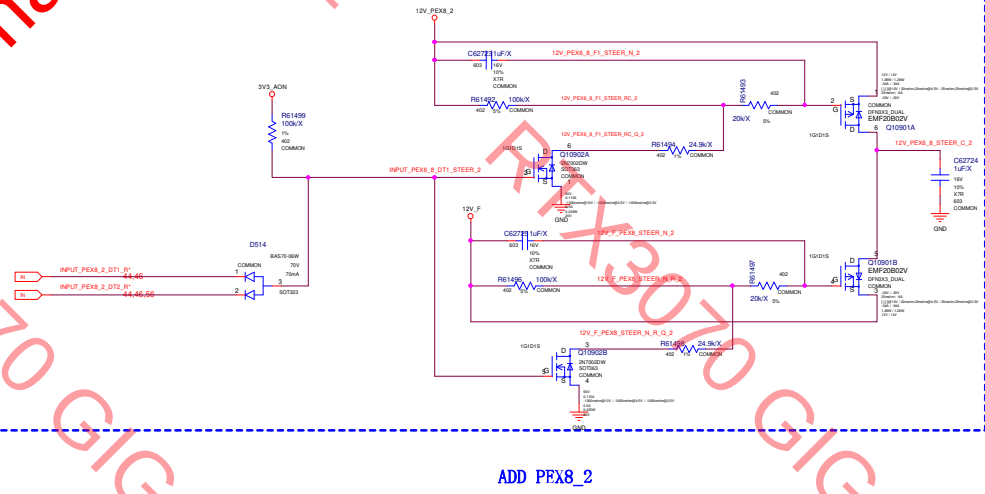
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



ADD PEX8_2

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: STEERING, UPB, HOT UNPLUG

GIGABYTE

Title: STEERING, UPB, HOT UNPLUG

Size: Custom | Document Number: GV-N3070AORUS M-8GD | Rev: 1.0

Date: Tuesday, August 04, 2020 | Sheet 46 of 57

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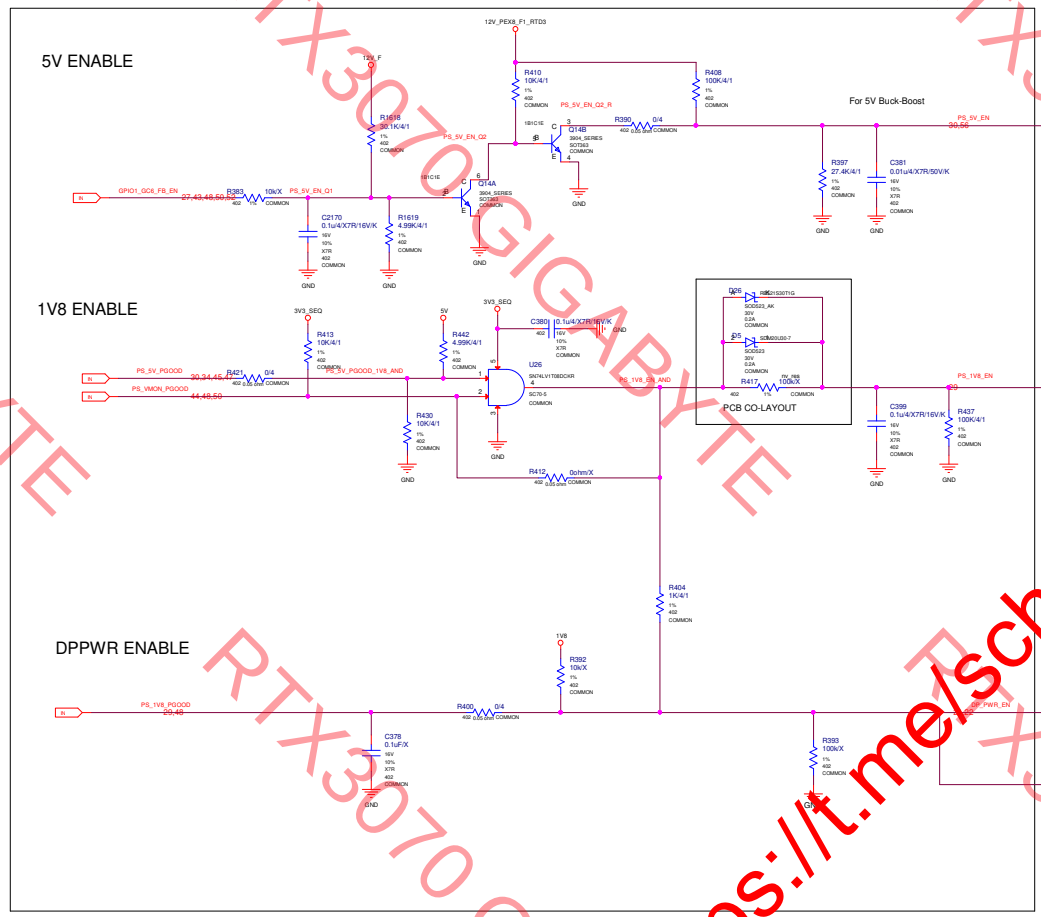

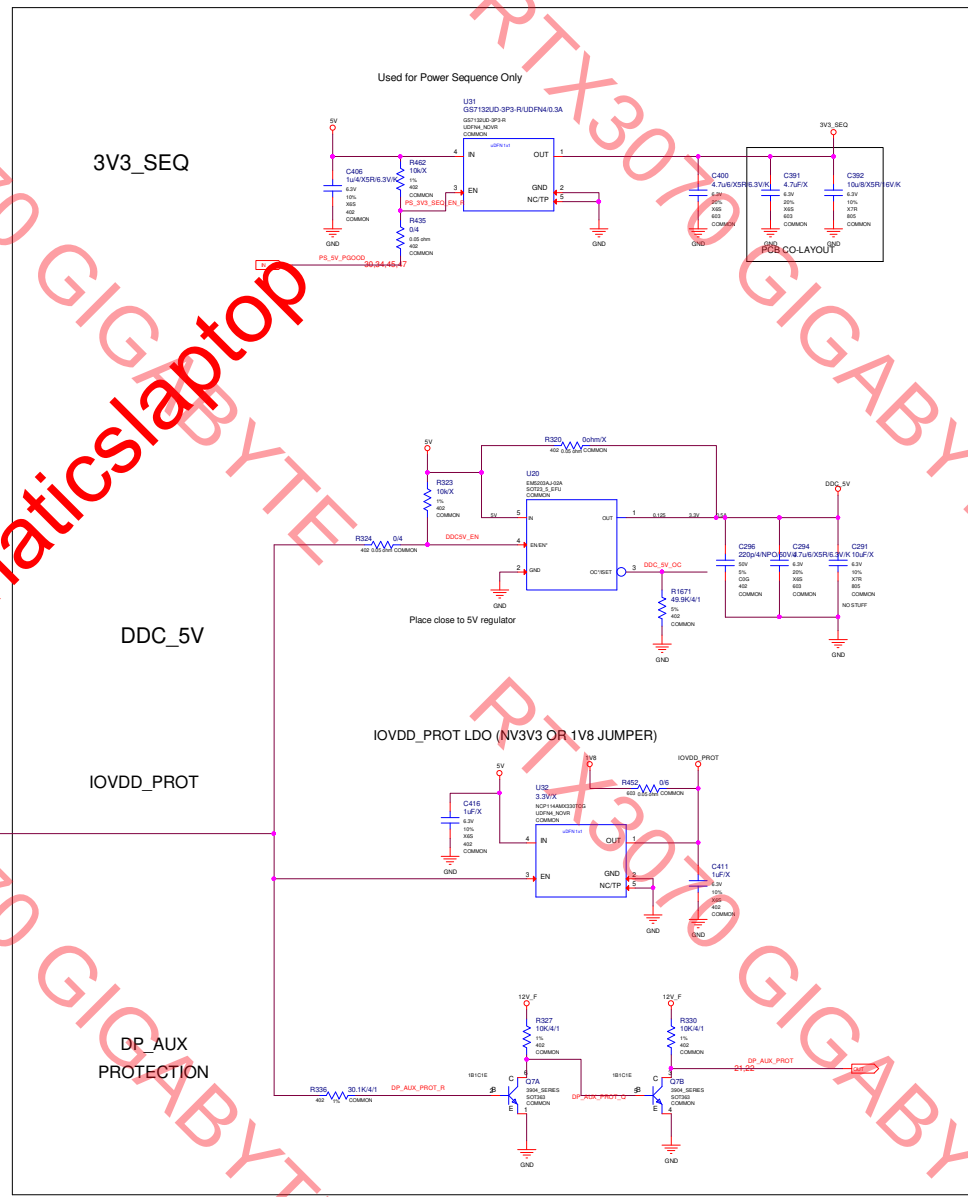

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL SEQ: 5V, 1V8, 3V3_SEQ

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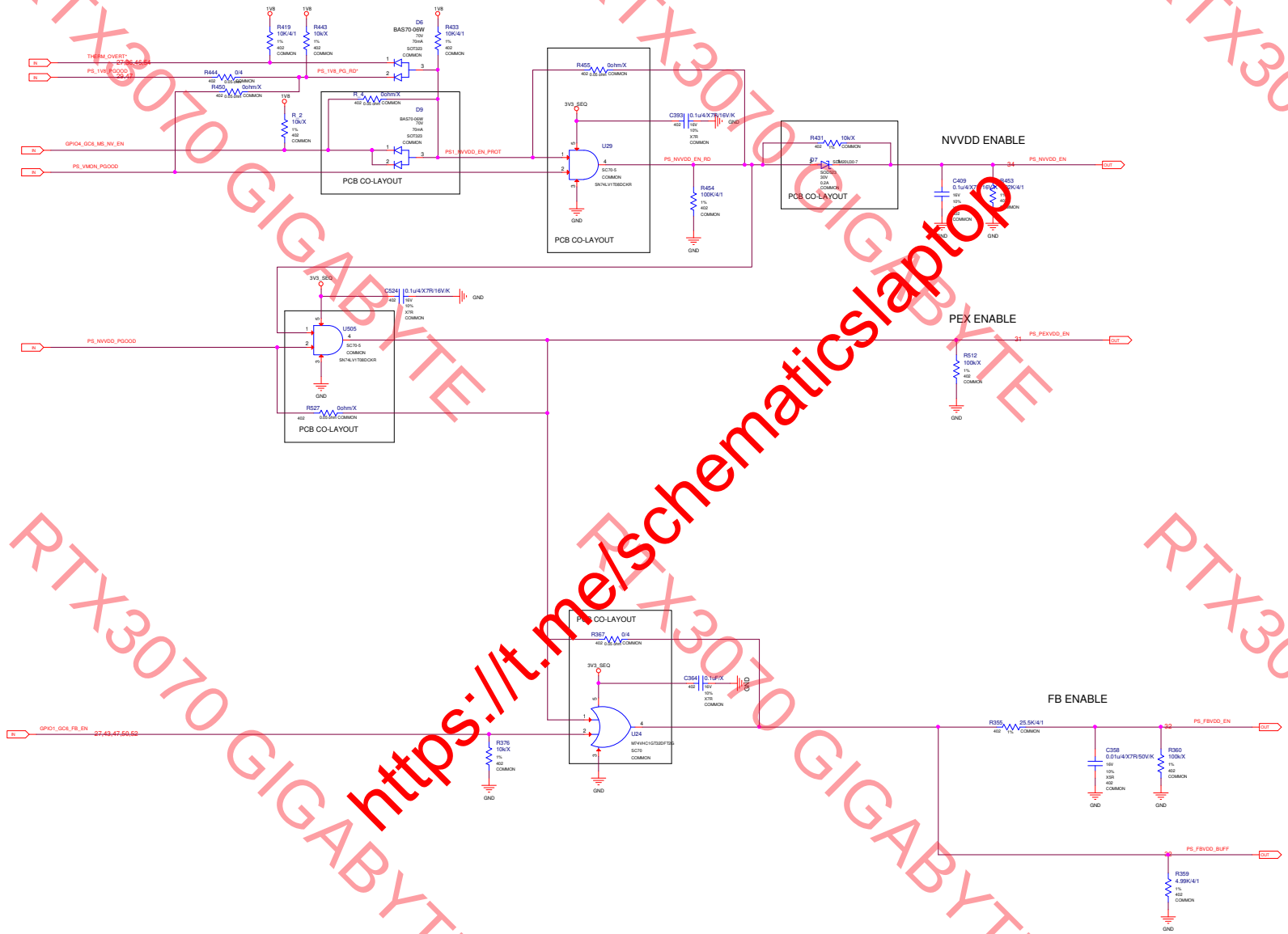
GIGABYTE

Title	SEQ: 5V, 1V8, 3V3_SEQ, DDC_5V, DP_AUX_PROT	
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Tuesday, September 08, 2020	Sheet 47 of 57	



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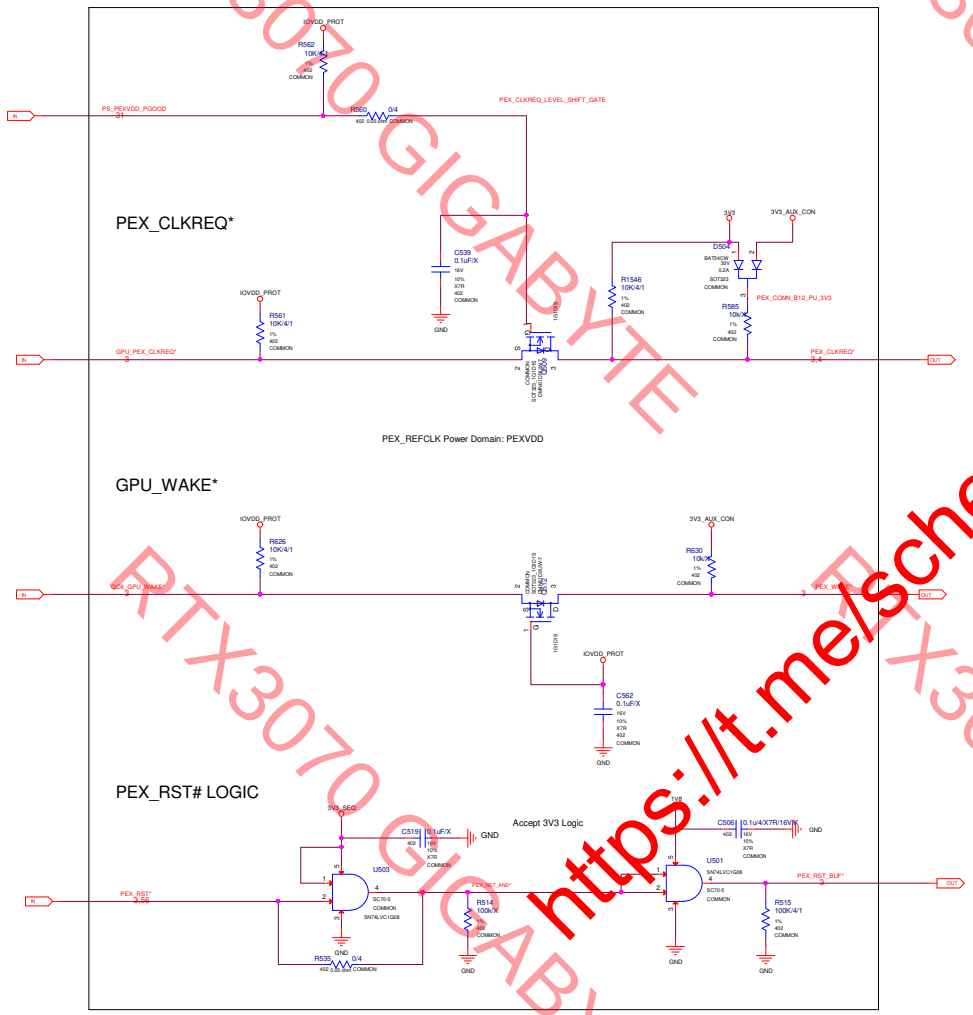
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

GIGABYTE		
Title: SEQ:NVVDD, PEX, FBVDDQ ENABLE		
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Tuesday, September 08, 2020	Sheet 48 of 57	



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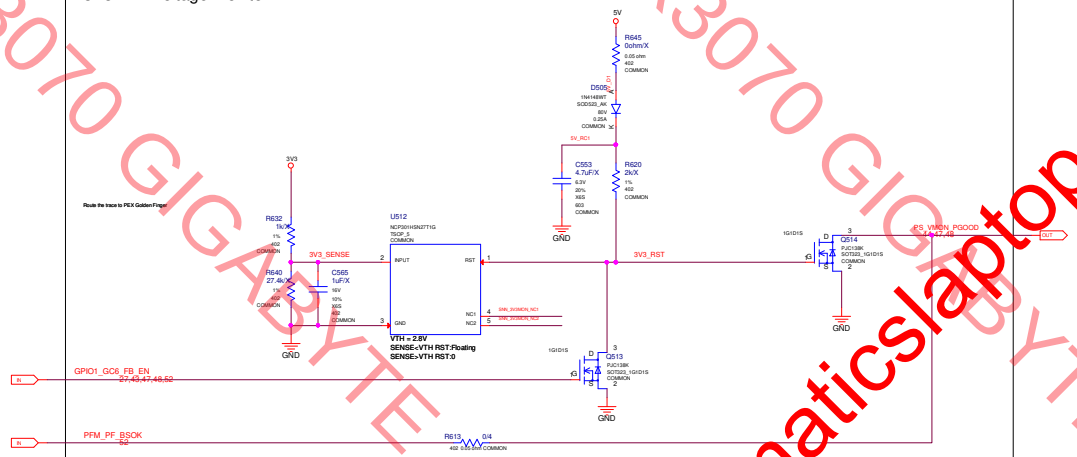
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: MISC

GIGABYTE		
Title: SEQ:MISC		
Size: Custom	Document Number: GV-N3070AORUS M-8GD	Rev: 1.0
Date: Tuesday, September 08, 2020	Sheet 49 of 57	

3V3PEX Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL SEQ: VOLTAGE MONITOR

GIGABYTE
Title SEQUENCE:Voltage Monitor
Size Custom | Document Number GV-N3070AORUS M-8GD | Rev 1.0
Date: Tuesday, August 04, 2020 | Sheet 50 of 57

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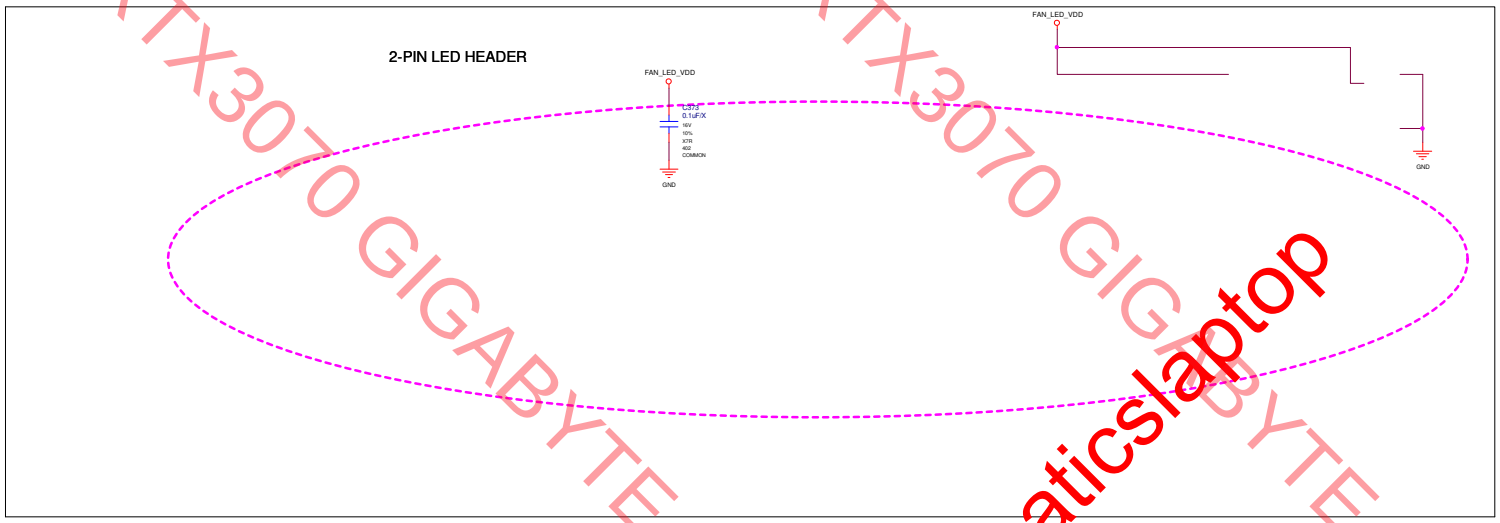

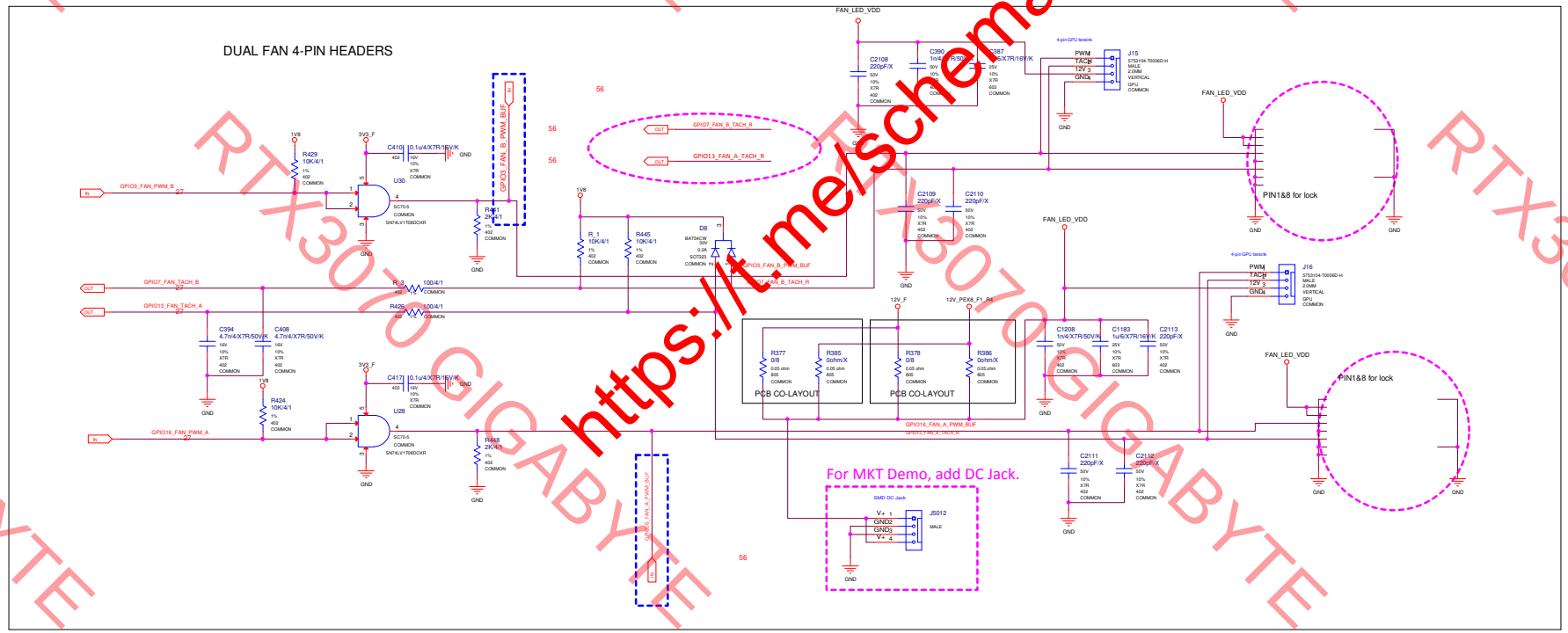

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN & LED

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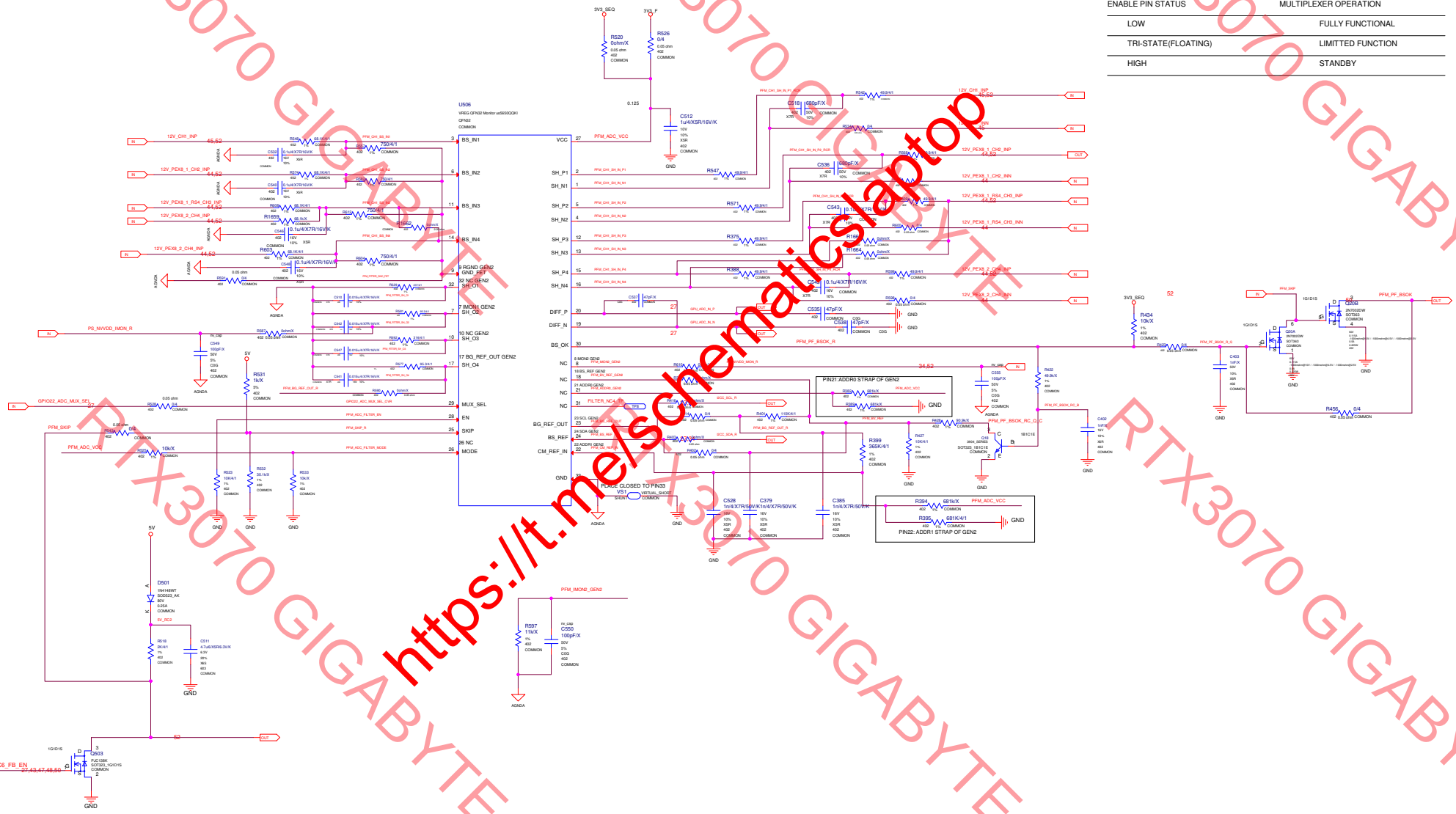
GIGABYTE	
Title	FAN&LED
Size: Custom	Document Number: GV-N3070AORUS M-8GD
Rev	1.0
Date: Tuesday, September 08, 2020	Sheet 51 of 57

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS:OVRM_PWR SENSE

GIGABYTE

Title: OVRM_PWR SENSE

Size: Custom | Document Number: GV-N3070AORUS M-8GD | Rev: 1.0

Date: Tuesday, September 08, 2020 | Sheet 52 of 57

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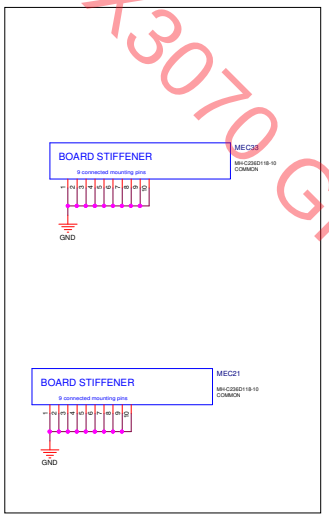
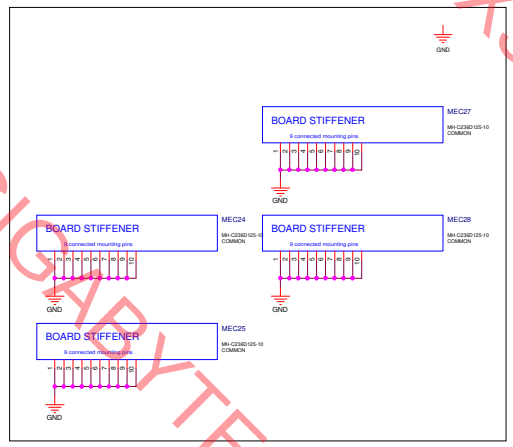
Page53: MECH

BKT SINK



GPU SINK



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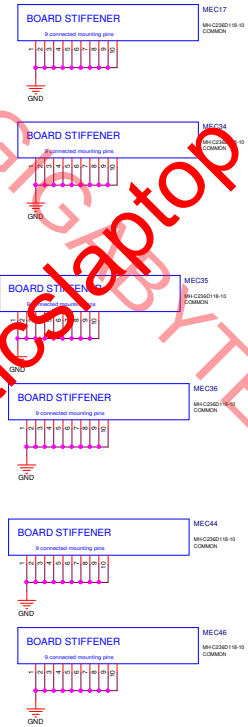

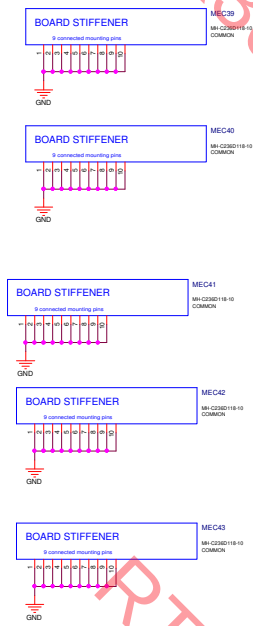

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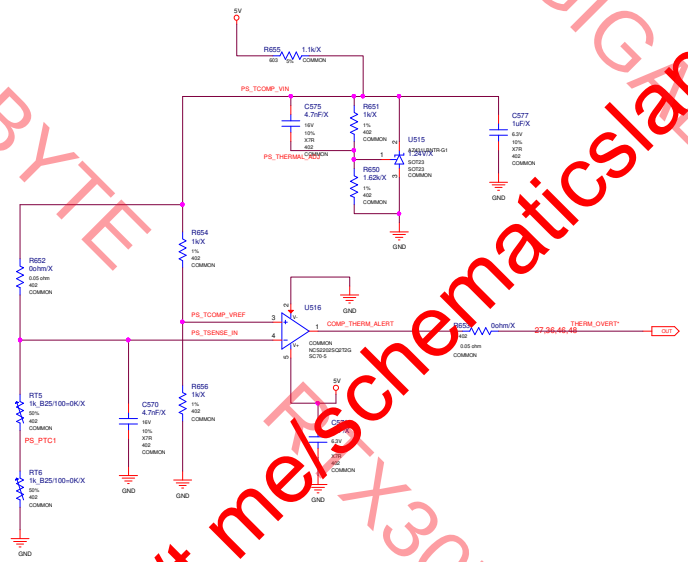

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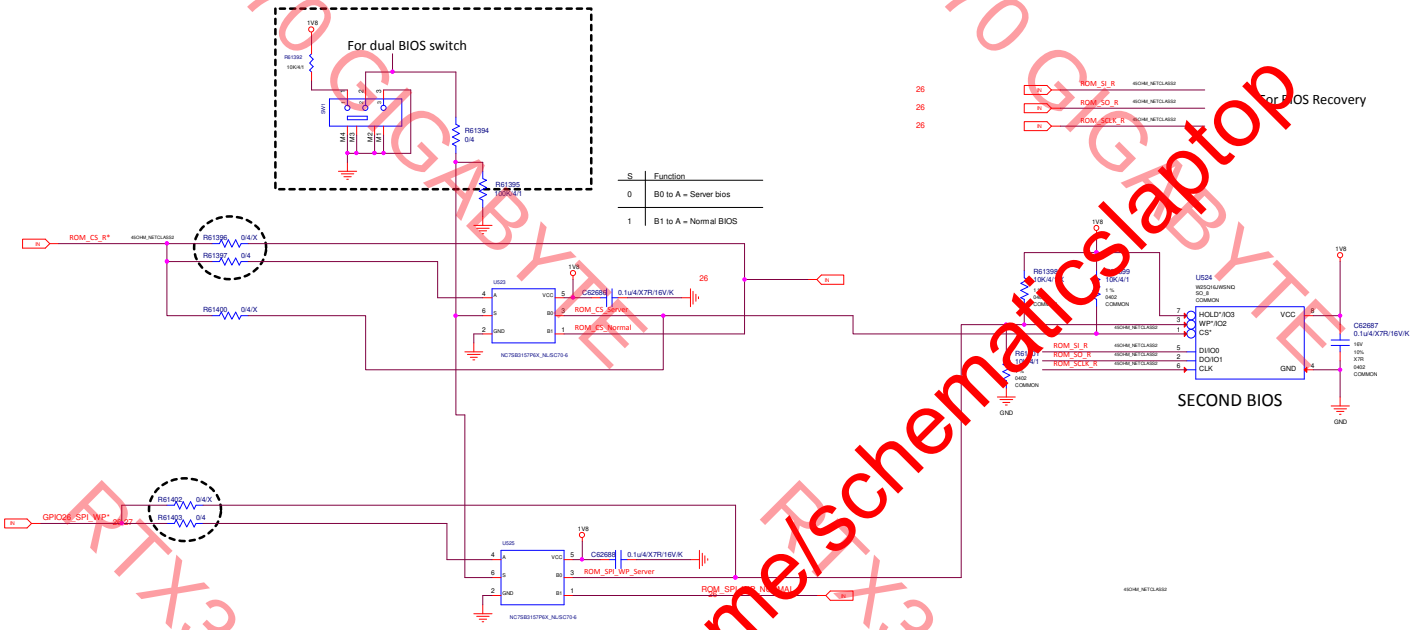

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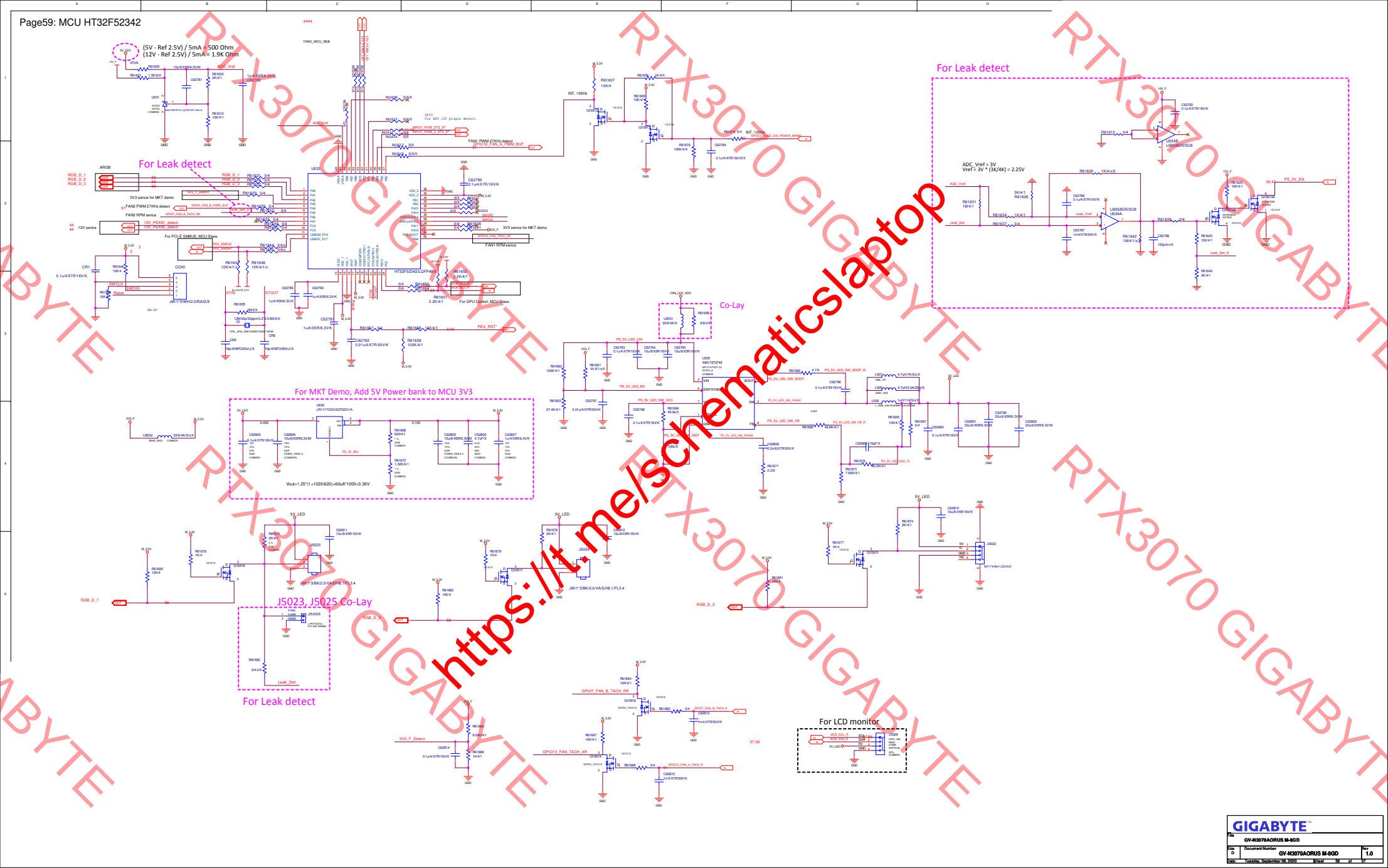

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History

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2018.07.21	First version

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