

4G bits DDR3L SDRAM

D2516ECMDXGGB-U

D2516ECMDXGJD-U

D2516ECMDXGJDI-U

D2516ECMDXGME-U

D2516ECMDXGMEI-U

D2516ECMDXGMEY-U

(256M words x 16 bits)

Specifications

- · Density: 4G bits
- Organization
- 32M words x 16 bits x 8 banks
- Package
- 96-ball FBGA <
- Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.35V (Typ)
- VDD, VDDQ = 1.283V to 1.45V
- Backward compatible for VDD, VDDQ=1.5V \pm 0.075V
- Data rate
 - 2133Mbps/1866Mbps/1600Mbps/1333Mbps (max.)
- Backward compatible
- · 2KB page size
- Row address: A0 to A14
- Column address: A0 to A9
- · Eight internal banks for concurrent operation
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
- Sequential (8, 4 with BC)
- Interleave (8, 4 with BC)
- Programmable /CAS (Read) Latency (CL)
- Programmable /CAS Write Latency (CWL)
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- · Refresh: auto-refresh, self-refresh
- · Refresh cycles
- Average refresh period
- 7.8μs at -40°C ≤ Temperature ≤ +85°C
- 3.9μs at +85°C ≤ Temperature ≤ +105°C
- Operating Case temperature range
- 0°C to +95°C (Commercial Temperature)
- 240°C to +95°C (Industrial Temperature)
 - -40°C to +105°C (Automotive Temperature)

Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- · Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the
- · DQS is edge-aligned with data for READs; centeraligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- . DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- · Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
- Synchronous ODT
- Dynamic ODT
- Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- · ZQ calibration for DQ drive and ODT
- Automatic self refresh (ASR)
- /RESET pin for Power-up sequence and reset function
- · SRT range:
- Normal/extended
- Programmable Output driver impedance control



	LINITRE		LINUTPO		
Revision History		W3352 DEBIAN			
Revision No.	History	Release date Editor	Approved by		
1.0	Initial release	Mar 2020			
1.1	Add P/N D2516ECMDXGGB-U	Apr 2020			
2 1.2	Add P/N D2516ECMDXGMEI-U	May 2022			
1.3	Add Automotive Temperature	Jan 2024 Jona Lee			

*Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by without notice.

All information discussed herein is provided on an "as is" basis, without warranties of any kind.

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MILRATIRWAN 2023-04 AND 3552 DEBIAN LINUX PC

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Ordering Information

	, LINUT	₹		LIMITAPE	
Ordering Info	mation Die revision	Organization (words x bits)	Internal Banks	JEDEC speed bin (CL-tRCD-tRP)	Package
D2516ECMDXGGB-U D2516ECMDXGJD-U D2516ECMDXGJDI-U D2516ECMDXGME-U D2516ECMDXGMEI-U D2516ECMDXGMEY-U	D D D D	256M x 16 256M x 16 256M x 16 256M x 16 256M x 16 256M x 16 256M x 16	8 8 8 7 3 . O.K	DDR3L-1600 (11-11-11) DDR3L-1866 (13-13-13) DDR3L-1866 (13-13-13) DDR3L-2133 (14-14-14) DDR3L-2133 (14-14-14) DDR3L-2133 (14-14-14)	96-ball FBGA 96-ball FBGA 96-ball FBGA 96-ball FBGA 96-ball FBGA 96-ball FBGA

Part Number

D 2516 E CM D X G JD I -U Internal code Type D : Packaged Device It is not marked on IC package. Temperature Organization Blank : Commercial Temperature(0°C to +95°C) 2516: 256M x 16 I Industrial Temperature(-40° to +95°) Y: Automotive Temperature (-40° to +105°) **Product Family** E: DDR3L, 1.35V GB: 1600 (11-11-11) NUPAT IRVAN 2023 OF ANS JD: 1866 (13-13-13) Manufacturer () ME: 2133 (14-14-14) Die Revision Kingston **Environment Code** G: Green, RoHS compliant and Halogen Free Package type X:FBGA96

MURATIRHAM 2023-04 AM3352 DEBIAM-LIMUX PC

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AM3352 DEBIAN LINUX MINI PC

Pin Configurations Pin Configurations

Pin Configurations (x16 configuration)

MIRATIRYAN 2023 /xxx indicates active low signal

96-ball FBGA

(RXA)		1	2	3	PY	7	8	9
MIRATIRKA	Α,	VDDQ	O DQU5	QQ DQU7		\circ	VDDQ	O VSS
S.	В	VSSQ	VDD	VSS		/DOSU	DQU6	VSSO
	С	VDDQ	\bigcirc	DQU1		\bigcirc	DQU2	
	D	VSSQ	\bigcirc	OMU		O DQU0	VSSQ	VDD
	EQU.	VSS	VSSQ	DQL0		DML	VSSQ	_
MURATIRKAN 2023.04 AM33552 DEBIAN LIMUS	F,	VDDQ	DQL2	DQSL		DQL1	DQL3	VSSQ
	G	VSSQ	DQL6	/DQSL		VDD	VSS	VSSQ
SEB.	H	() REFDO	VDDQ	O DQL4		O DQL7	O DQL5	VDDQ
	J	O NC	O vss	O /RAS		CK	O VSS	NCOS
1/3/55	К	\bigcirc	\bigcirc	\bigcirc		\bigcirc	\bigcirc	NC25
CARI	L	ODT	VDD	/CAS		/CK	\bigcirc	CKE
23.0	М	NC	/CS	WE		A10(AP	0	NC O
2420	N	VSS	BA0	BA2		40	VREFCA	
,2XX	Р	VDD	A3	A0 A2	, p.y	A12(/BC) BA1	VDD
	R	vss	A5	A2	7,,	A1	Ã4	○ vss
W.	_	VDD	A7	A9		A11	A6	VDD
h.	'	VSS	RESET	A13		O A14	O A8	VSS
				(7	Top view))		

Pin	Function	Pin name	Function
A0 to A14 ^{*2}	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET ^{*2}	Active low asynchronous reset
BA0 to BA2*2	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	Data input/output	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS*2	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE*2	Command input	VREFDQ	Reference voltage for DQ
CKE*2	Clock enable	VREFCA	Reference voltage for CA
CK,/CK	Differential clock input	ZQ 1	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC*1	No connection
ODT*2	ODT control	, RY	

Notes: 1. Not internally connected with die.

2. Input only pins (address, command, CKE,ODT and /RESET) do not supply termination.



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		ball FBGA	MIRATIRKAN 2023-04 AMS	IMO
		24.1		4.
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		OFF		OK
	a ^s	in the second se		ASP .
	133)-)3"
	V KIN		Pla	
	3.Ok		2.0k	
	2023		223	
	7,1		7,10	
4	P.		12	
X IR.			K.	
2A			2A	
NUP			NINE	
4.			4.	

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MIRATIRAM 2023 OA AM3352 DEBIAMILIMUX PC



	F.			LIMIT		
. Electrical Conditions All voltages are referenced to VSS (GND) Execute power-up and Initialization sequence before proper device operation is achieved. 1.1 Absolute Maximum Ratings						
9 ,	ns	18430.				
ole 1: Absolute Maximum Rating	gs Symbol	Rating	Unit	Notes		
ole 1: Absolute Maximum Rating	-	, extend	Unit V	Notes 1, 3		
ole 1: Absolute Maximum Rating	Symbol	Rating				
ole 1: Absolute Maximum Rating Parameter Power supply voltage	Symbol VDD	Rating -0.4 to +1.80	V	1, 3		
Parameter Power supply voltage Power supply voltage for output	Symbol VDD VDDQ	Rating -0.4 to +1.80 -0.4 to +1.80	V	1, 3 1, 3		
Parameter Power supply voltage Power supply voltage for output Input voltage	Symbol VDD VDDQ VIN	Rating 0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80	V V V	1, 3 1, 3 1		
Parameter Power supply voltage Power supply voltage for output Input voltage Output voltage	Symbol VDD VDDQ VIN VOUT	Rating -0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80	V V V	1, 3 1, 3 1		
Parameter Power supply voltage Power supply voltage for output Input voltage Output voltage Reference voltage	Symbol VDD VDDQ VIN VOUT VREFCA	Rating -0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80 0.49 to 0.51 × VDD	V V V V	1, 3 1, 3 1 1 1 3		
Parameter Power supply voltage Power supply voltage for output Input voltage Output voltage Reference voltage for DQ	Symbol VDD VDDQ VIN VOUT VREFCA VREFDQ	Rating 0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80 -0.4 to +1.80 0.49 to 0.51 × VDD 0.49 to 0.51 × VDDQ	V V V V V V	1, 3 1, 3 1 1 1 3		

- Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - Storage temperature is the case surface temperature on the center/top side of the DRAM.
 - VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Rating	Unit	Notes	
Commercial temperature	0 to +95	°C	1, 2, 3	
Industrial temperature	-40 to +95	°C	1, 2, 3	, R
Automotive temperature	-40 to +105	°C	1, 2, 3	Tu.

- Notes: 1. Commercial & Industrial & Automotive temperature is the case surface temperature on the center/top side of the DRAM.
 - 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM temperature must be maintained between 0°C to +85°C for commercial temperature and -40°C to +85°C for industrial and automotive temperature under all operating conditions.
 - 3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C or +85°C and +105°C operating temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a) Refresh commands must be doubled in frequency, therefore reducing the tefresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)
 - b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).



Recommended DC Operating Conditions 1.3

Table 3-a: Recommended DC Operating Conditions, DDR3L Operation.

Parameter	Symbol	min	typ max	Unit	Notes
Supply voltage	VDD	1.283	1.35 1.45	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.283	1.35 1.45	V	1, 2, 3

Notes:1.

- 2.
- Commercial temperature is 0°C to +95°C, Industrial temperature is -40°C to +95°C and Automotive temperature is -40°C to +105°C 3.

Table 3-b: Recommended DC Operating Conditions, DDR3 Operation.

Table 3-b. Recommended DC Operating Conditions, DDR3 Operation.						
Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	v 2	1, 2, 3

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.

- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together. 2.
- MIRATIRYAN 2023 OA AMS NURAT RYAN 2023-04 ANS. Commercial temperature is 0°C to +95°C, Industrial temperature is -40°C to +95°C and Automotive temperature is -40°C to +105°C

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1.4 IDD and IDDQ Measurement Conditions

In this chapter DD and IDDQ measurement conditions such as test load and patterns are defined.

The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2R1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC)max
- H and 1: VIN ≥ VIH(AC)min
- MID-LEVEL: defined as inputs are VREF = VDDQ / 2
- · FLOATING: don't care or floating around VREF.
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.

Note: The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting. RON = RZQ/7 (34Ω in MR1);

```
Qoff = 0B (Output Buffer enabled in MR1);
RTT Nom = RZQ/6 (40\Omega in MR1);
```

RTT WR = RZQ/2 (120 Ω in MR2);

TDQS Feature disabled in MR1

- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} := {H, H, H, H}

 Define /D = {/CS, /RAS, /CAS, /WE} := {H, H, H, H}



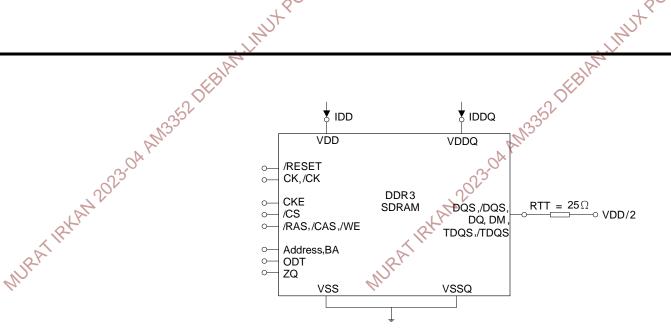


Figure 1: Measurement Setup and Test Load for IDD and IDDQ Measurements

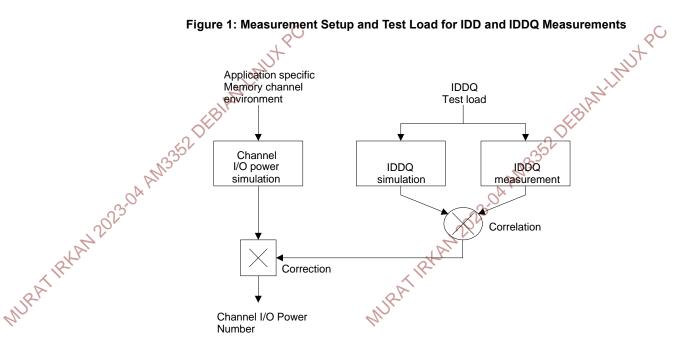


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power

rom Simulated Channel I/O Power to A Supported by IDDQ Measurement Supported by IDDQ Measurement Annual Report Reported by IDDQ Measurement Report Re MIRATIRAN 2023 OA ANS 352 DEBIANLINUX PC

Timings Used for IDD and IDDQ Measurement-Loop Patterns 1.4.1

Table 4 : Timings Used for IDD and IDDQ Measurement-Loop Patterns

		, LIMIT P			, >	INITP
		gs Used for IDD and IE		.oop Patterns	DDB31-2433	
	Table 4 : Timin	gs Used for IDD and II	DDQ Measurement-l	_oop Patterns	1333	
	OA AIT	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	_
	Parameter	9-9-9	11-11-11	13-13-13	14-14-14	Unit
MIRATIRA	CL	9	11	13 LAT	14	nCK
MILE	tCK(min)	1.5	1.25	1.071	0.938	ns
NIRI	nRCD(min)	9	11 NP	13	14	nCK
H.	nRC(min)	33	39	45	50	nCK
	nRAS(min)	24	28	32	36	nCK
	nRP(min)	9	11	13	14	nCK
	nFAW	30	32	33	38	nCK Q
	nRRD	5 10	6	6	7	nCK
	nRFC	174	208	243	279	nCK
MRATIRY	nRFC	352 DEBIT	MIRE	243 XIRXAN 2023-04 P	M3352 DEBIT	

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1.4.2 Basic IDD and IDDQ Measurement Conditions Table 5: Basic IDD and IDDQ Measurement Conditions

_	Parameter 1055	Symbol	Description
MURATIRKAN	Operating one bank active precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 6; Data I/O: MD-LEVEL; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2, (see Table 6); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 6
	Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 7; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2, (see Table 7); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 7
	Precharge standby current	IDD2N UT PC	CKE: H; External clock: on; tCK, CL: see Table 4 BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed, output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see Table 8
	Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 9; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 9; pattern details: see Table 9
-	Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
	Precharge power-down current slow exit Precharge power-down current fast exit	IDD2P0	CKE: L; External clock: on; tCK, CL; see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
MIRATIRIE	Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
	Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
	Active standby current	IDD3NUTPC	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 8
	Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
,RYAT	Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to Table 11; data I/O: seamless read data burst with different data between one burst and the next one according to Table 11; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2, (see Table 11); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 11



Table 5: Basic IDD and IDDQ Measurement Conditions (cont'd)

	Parameter 1997	Symbol	Description
MIRATIRYAS	Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to Table 12; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2, (see Table 12); Output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 12
	Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 4; BL: 8*1; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to Table 13; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC (Table 12); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 13
	Self-refresh current: normal temperature range	IDD8/117	Commercial temperature: 0 to 85°C and Industrial temperature -40 to 85°C; ASR: disabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: see Table 4; BL: 8*1;AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
	Self-refresh current: extended temperature range	IDD6ET	Commercial temperature: 0 to 95°C, Industrial temperature: -40 to 95°C and Automotive temperature: -40 to 105°C; ASR: Disabled*4; SRT: Extended*5; CKE: L; External clock: off; CK and /CK: L; CL: Table 4; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
,URAT IRVAT	Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 4; BL: 8*1, *6; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to Table 15; data I/O: read data bursts with different data between one burst and the next one according to Table 15; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, ···7) with different addressing, see Table 15; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 15
4.	RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].

2. MR: Mode Register

Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];

RTT_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT_WR enable: set MR2 bits [10, 9] = [1,0].

3. Precharge power down mode: set MR0 bit A12= 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.

4. Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.

emper in the second sec 5. Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.

6. Read burst type: nibble sequential, set MR0 bit A3 = 0



Table 6: IDD0 Measurement-Loop Pattern

				stp										LINI	t Po	
	Table 6: II	DD0 Meas	rement-Loo	p Patte	ern						C	552 DK	BIAR			
	CK, /CK	Su CKE -Lo	b Cycle oop number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
	0,0		0	ACT	0	0	1	1	0	·0,0	0	0	0	0	0	
	2022		1, 2	D, D	1	0	0	0	0 0	0	0	0	0	0	0	
	4		3, 4	/D, /D	1	1	1	1 ,	0	0	0	0	0	0	0	
2X				Repea	t patter	n 14 ı	until nR	AŞ-1	, trunca	te if ne	cessary	/				
1 lks			nRAS	PRE	0	0	1 /	0	0	0	0	0	0	0	0	
IPA			•••	Repea	t patter	n 14 ເ	until nR	C - 1, t	runcate	if nece	essary					
MIRATIRA		٥	1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	
	H	0	1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	
	Toggling Static H		1 x nRC + 3,4	/D?/D	1	1	1	1	0	0	0	0	0	F	+ QC	
	ggli		12	Repea	t patter	n nRC	+ 1,,4	until 1	*nRC +	nRAS	- 1, tru	ncate if	f neces	sary) '	
	5		1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	0	SAN	F	0	
		<	5 ¹	Repea	t nRC +	⊦ 1,,4	until 2	x nRC	- 1, trun	cate if	necess	ary	·			
		2	2 x nRC	Repea	t Sub-L	oop 0,	use BA	= 1 ins	tead			SV.				
	X 2023.01	232	4 x nRC	Repea	t Sub-L	oop 0,	use BA	= 2 ins	tead		10°)~				
		AM 3	6 x nRC	Repea	t Sub-L	oop 0,	use BA	= 3 ins	tead		DL.					
	2.0	<u>4</u>	8 x nRC			oop 0,				2.Oh						
	20,5	_ 5	10 x nRC			oop 0,				j ²						
	72	_ 6	12 x nRC			.oop 0,			100	,						
Z,	<u> </u>	7	14 x nRC	Repea	t Sub-L	oop 0,	use BA	= 7 ins	tead							

DM must be driven low all the time. DQS, /DQS are FLOATING.

DQ signals are FLOATING.

BA: BA0 to BA2.

Am: m means Most Significant Bit (MSB) of Row address.

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Table 7: IDD1 Measurement-Loop Pattern

					NATE.											test	2
	Table 7:	IDD1 M	easure	ment-Lo									3520	BIA			
	CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/cs	/RAS	/CAS	/WE	ODT	BA*³	A11 Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*²
MIRATIRY	~~~	S		0	ACT	0	0	1	1	0	05,0	0	0	0	0	0	_
	20/1			1, 2	D, D	1	0	0	0	0 0	0	0	0	0	0	0	_
6	4			3, 4	/D, /D	1	1	1	1	9	0	0	0	0	0	0	_
2×					Repeat	patter	n 14 uı	ntil nR0	CD - 1	truncate	e if nece	essary					
1/1/2				nRCD	RD	0	1	0	1/1/	0	0	0	0	0	0	0	00000000
,RA					Repeat	patter	n 14 uı	ntil nR	(S - 1, 1	truncate	if nece	essary					
W.				nRAS	PRE	0	0	W.	0	0	0	0	0	0	0	0	_
					Repeat	patter	n 14 uı	ntil nR0	C - 1, tru	uncate i	f neces	sary					
			0	1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	_
	I	•	Ū	1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	
	Toggling Static H			1 x nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	9	2
	<u>.</u>	ח		1	Repeat	patter	n nRC +	1,, 4	until nl	RC + nF	RCD - 1	, trunc	ate if ne	cessa	ıry T	70	
	Todal	, , ,		1 x nRC + nRCD	RD	0	1	0	1	0	0	0	0	0 0	¥	0	00110011
			A C	<u> </u>	Repeat	patter	n nRC +	1,, 4	until nl	RC + nF	RAS - 1	, trunca	ate if ne	cessa	ry		
		.0	357	1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	8 V	0	F	0	_
		No			Repeat	patter	n nRC +	1,, 4	until 2	x nRC -	1, trun	cate if	necess	ary			
		- VE	1	$2\times nRC\\$	Repeat	Sub-L	.oop 0, u	se BA=	: 1 inste	ead		b.					
	-03 (0)	Or	2	$4\times nRC$	Repeat	Sub-L	.oop 0, u	se BA=	2 inste	ead	2,0						
	002	_	3	$6\times nRC$	Repeat	Sub-L	.oop 0, u	se BA=	: 3 inste	ead	32						
	4.1	_	4	$8\times nRC$	Repeat	Sub-L	.oop 0, u	se BA=	4 inste	ead\							
at 1		_	5	10 × nRC	Repeat	Sub-L	.oop 0, u	se BA=	5 inst	ead							
1/K		_	6	12 × nRC	Repeat	Sub-L	.oop 0, u	se BA=	6 inste	ead							
.DA			7	14 × nRC					1								
MURATIRY	Notes: 1. 2. 3.	DM mu Burst s BA: BA	ust be dri equence 40 to BA2	ven low al driven on 2.													

- Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
- 3. BA: BA0 to BA2.
- Am: m means Most Significant Bit (MSB) of Row address.

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Table 8: IDD2N and IDD3N Measurement-Loop Pattern

					STRE									4	LIN	str
	CK,	: IDD2N a	and IDE	3N Meas	sureme	nt-Loc	p Patt	ern				AM	552 DK	BIAT A7	A3	Α0
	/CK	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	Am	A10	-A9	-A6	-A2 Data*2
	ഹാ			0	D	1	0	0	0	0	0	0	0	0	0	0
	201		0	1	D	1	0	0	0	0 0	Ó	0	0	0	0	0
2	4		U	2	/D	1	1	1	1	67	0	0	0	0	F	0
OFY	=	E O		3	/D	1	1	1	104	0	0	0	0	0	F	0
1/1/	,		1	4 to 7	Repeat	Sub-Lo	oop 0, u	se BA=	1 inste	ead						
.QA	Ċ	ົກ <u> </u>	2	8 to 11	Repeat	Sub-Lo	oop 0, u	se BA=	2 inste	ead						
MURATIRYA			3	12 to 15	Repeat	Sub-Lo	oop 0, u	se BA=	3 inste	ead						
12	,	l ogginng Static H	4	16 to 19	Repeat	Sub-Lo	oop 0, u	se BA=	4 inste	ead						
		_	5	20 to 23	Repeat	Sub-Lo	oop 0, u	se BA=	5 inste	ead						
		_	6	24 to 27	Repeat	Sub-Lo	oop 0, u	se BA=	6 inste	ead						
		_	7	28 to 31	Repeat	Sub-Lo	oop 0, u	se BA=	7 inste	ead						C

- DQ signals are FLOATING. 2.
- 3. BA: BA0 to BA2.
- Am: m means Most Significant Bit (MSB) of Row address.

Table 9: IDD2NT and IDDQ2NT Measurement-Loop Pattern

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.				_	6	24 to 27	Repeat	t Sub-Lo	oop 0, u	ise BA=	= 6 inst	ead							
1					7	28 to 31	Repeat	Sub-Lo	oop 0, u	se BA=	7 inst	ead							<i>C</i> .
1							1 7	e. DQS,	,/DQS a	are FLC	DATING	€.						. (
1							357											5	
1								(140D)	, D								11	7	
1			4.	Am: m ı	means N	lost Signif	icant Bit	(MSB)	of Row	addres	S.					~	7.		
1						3/12										BIL	,*		
1					06	,*									O'	/			
1		Table	9: I	DD2NT	and ID	DQ2NT	Measur	ement	-Loop	Patte	rn				52				
1				1/3	5									10	5				
1		CK,		Du.		-							4	A11		Α7	А3	A0	
Total 1st Repeat Sub-Loop 0, but ODT = 0 and BA= 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA= 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA= 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.		/CK	0	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA*	-Am	A10	-A9	-A6	-A2	Data*2
Total 1s Repeat Sub-Loop 0, but ODT = 0 and BA = 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA = 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA = 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.		2	رن.			0	D	1	0	0	0	0	\leftarrow	0	0	0	0	0	
Total 19 Repeat Sub-Loop 0, but ODT = 0 and BA = 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA = 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA = 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.		120			0	1	D	1	0	0	0	0,7	0	0	0	0	0	0	
Total 19 Repeat Sub-Loop 0, but ODT = 0 and BA = 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA = 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA = 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.	۰۲۷	25			O	2	/D	1	1	1	1	10	0	0	0	0	F	0	
Total 19 Repeat Sub-Loop 0, but ODT = 0 and BA = 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA = 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA = 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.	PK	*	C H	_		3	/D	1	1	1	1,2	0	0	0	0	0	F	0	
Total 19 Repeat Sub-Loop 0, but ODT = 0 and BA = 5 6 24 to 27 Repeat Sub-Loop 0, but ODT = 1 and BA = 6 7 28 to 31 Repeat Sub-Loop 0, but ODT = 1 and BA = 7 Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.	D.		tati	_	1	4 to 7	Repeat	t Sub-Lo	oop 0, b	ut ODI	= 0 ar	nd BA=	1						
Total 15	P.		ng S	_	2	8 to 11	Repeat	t Sub-Lo	oop 0, b	ut ODT	¯=1 ar	nd BA=	2						
Total 15			glir		3	12 to 15	Repeat	t Sub-Lo	oop 0, b	ut ODT	= 1 ar	nd BA=	3						
Solution			Tog	_	4	16 to 19	Repeat	t Sub-Lo	oop 0, b	ut ODT	= 0 ar	nd BA=	4						
Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most Significant Bit (MSB) of Row address.			•	_	5	20 to 23	Repeat	t Sub-Lo	oop 0, b	ut ODT	= 0 ar	nd BA=	5						
Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most Significant Bit (MSB) of Row address.				_	6	24 to 27	Repeat	t Sub-Lo	oop 0, b	ut ODT	= 1 ar	nd BA=	6						
Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING. 2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most significant Bit (MSB) of Row address.				_	7	28 to 31	Repeat	Sub-Lo	oop 0, b	ut ODT	= 1 ar	nd BA=	7						C_{1}
2. DQ signals are FLOATING. 3. BA: BA0 to BA2. 4. Am: m means Most Significant Bit (MSB) of Row address. PARTIRARM 2023-04 AMS 352 HELDER LINE AND AM		Notes:	: 1.	DM mu	ust be dri	iven low al	I the time	e. DQS,	,/DQS a	are FLC	DATING	€.						+	
3. BA: BA0 to BA2. 4. Am: m means Most Significant Bit (MSB) of Row address. RAT REAR RATE REAR RATE RATE RATE RATE R			2.				<i>3</i> 2'										1	7,	
4. Am: m means Most Significant Bit (MSB) of Row address. RATIRAAN 2023 04 AM 2023 04 A				BA: BA	0 to BA2														
JRAT IRVAN 2023-04 AM3352 THEBY. MIRAT IRVAN 2023-04 AM3352 THEBY. MIRAT IRVAN 2023-04 AM3352 THEBY.			4.	Am: m ı	means N	lost Signif	icant Bit	(MSB)	of Row	addres	S.					, D	, ,		
JRAT IRVAN 2023-04 AM3352 DV WILEAT IRVAN 2023-04 AM3352 DV WILEAT IRVAN 2023-04 AM3352 DV					4	9,,									<	BI.			
JRAT IRKAN 2023-04 AM33501 MURAT IRKAN 2023-04 AM33501																~			
JRAT IRVAN 2023-04 ARMS MURAT IRVAN 2023-04 ARMS 15				0	50										350				
JRAT IRKAN 2023-04 IN WILLIAM 20				N.S.										M,S					
JRAT IRVAN 2013-10 MURAT IRVAN 2013-10 15			~	× /×.										ib.					
JRAT IRVAN 2013 NILPAT IRVAN 2013			J.O.										3.O.						
JRAT IRKAN I		905	,									00	3/2						
JRAT IRVAN		7.1										4							
JRATIFE MIRATIFE 15	at 1	P .									N	B.							
JRA NIJRA 15	1/4										X IF								
	2P									28									
15	The									NIF									
15										4.									
										15									

- 2. DQ signals are FLOATING
- BA: BA0 to BA2.
- Am: m means Most Significant Bit (MSB) of Row address.

Table 10: IDD2P0, IDD2P1, IDD2Q and IDD3P Measurement-Loop Pattern

						tu	?										4	LINI	5+ Po		
	Table 10	: IDD2P0, IDD)2P1,	DD2	Q and	i IDD	3P M	easuı	reme	ent-L	_oop	Patter	n			,n.	EBIA	Burst length			
	External Clock	Name	CK	CKE	RC	RAS	RCD	RRD	CL	AL	СЅВ	Comm and	Am	ВА	DM	ODT	DQ, DQS	Burst length	Active banks	ldle banks	Data
		IDD2P0 Precharge Power-Down Current (Slow Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	202	3.0A	0		Acted		None	All	Midlevel
X	Toggling	IDD2P1 Precharge Power-Down Current (Fast Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	RYA	0	0	0	Acted, off	Acted	8	None	All	Midlevel
WILL.	P P	IDD2Q Precharge Quiet Standby Current	CK (MIN) IDD	1	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
		IDD3P Active Power-Down Current	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	All	None	Midlevel
	Notes: 1.	MR0[12] defin DLL on (fast e "Acted, off" me	exit. MF	20[12]	= 1) a	and bl	L off	(slow e	arge exit, N sign	MRO[12] = LOW.	PKAS	202	3.04	AN CONTRACTOR OF THE PROPERTY	3520	EBIAS	Y-LIMI.	All		n de la company

Notes: 1. MR0[12] defines DLL on/off behavior during precharge power-down only; # 1)

"R bits a

"REPART IRVAN 2023 OA AN 3352 DE BIANTI DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).

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^{2. &}quot;Acted, off" means the MR bits are enabled, but the signal is LOW.

Table 11: IDD4R and Measurement-Loop Pattern

					ites										11	st	2
		11: IDD4R			ent-Lo	op Pat	tern					No.	520 ^K	BIAN			
	CK, /CK	CKE	Sub	Cycle number	Com- mand	/CS	/D A S	/CAS	/ME	ODT	BA**	A11 -Am	A10	A7 -A9	A3 -A6	A0	Data*²
MRATIRY	70K	S CKE	-Loop	0	RD	0	1	0	1		200	0	0	0	0	0	00000000
	1200			1	D	1	0	0	0	0,1	0	0	0	0	0	0	_
18	7			2,3	/D, /D	1	1	1	1 1	0	0	0	0	0	0	0	
PY	•		0	4	RD	0	1	0	1,2	0	0	0	0	0	F	0	00110011
A		I		5	D	1	0	0 0	0	0	0	0	0	0	F	0	_
"IR"		Toggling Static H		6,7	/D, /D	1	1	10P	1	0	0	0	0	0	F	0	
M		S D	1	8 to 15	Repeat	Sub-Lo	oop 0, b	ut BA=	1								
		iglin _	2	16 to 23	Repeat	Sub-Lo	oop 0, b	ut BA=	2								
			3	24 to 31	Repeat	Sub-Lo	oop 0, b	ut BA=	3								
			4	32 to 39	Repeat	Sub-Lo	oop 0, b	ut BA=	4								
		_	5	40 to 47	Repeat	Sub-Lo	oop 0, b	ut BA=	5								SC
		_	6	48 to 55	Repeat	Sub-Lo	oop 0, b	ut BA=	6							4	
			7	56 to 63	Repeat	Sub-Lo	oop 0, b	ut BA=	7	·					1/2		

erv. A sign, and Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.

Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

BA: BA0 to BA2

Am: m means Most Significant Bit (MSB) of Row address.

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Table 12: IDD4W Measurement-Loop Pattern

	CK, /CK	CKE	Sub	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11	A10	A7 -A9	A3 -A6	A0 -A2	Data*²
	207	Or.		0	WR	0	1	0	0	1	0,0	0	0	0	0	0	00000000
	00/12			1	D	1	0	0	0	1 0	Ø	0	0	0	0	0	_
2	4		0	23	/D, /D	1	1	1	1	4	0	0	0	0	0	0	_
2/Y			0	4	RD	0	1	0	0	-1	0	0	0	0	F	0	00110011
1 / Ille	Ξ.	E		5	D	1	0	0	0	1	0	0	0	0	F	0	_
MIRATIRA	:			6,7	/D, /D	1	1	1,28	1	1	0	0	0	0	F	0	_
W,	9	ე ე	1	8 to 15	Repeat	Sub-Lo	op 0, b	ut BA=	1								
\	<u>:</u>		2	16 to 23	Repeat	Sub-Lo	op 0, b	ut BA=	2								
	Š	5 5 6 6 7	3	24 to 31	Repeat	Sub-Lo	op 0, b	ut BA=	3								
		_	4	32 to 39	Repeat	Sub-Lo	op 0, b	ut BA=	4								
		_	5	40 to 47	Repeat	Sub-Lo	op 0, b	ut BA=	5								<i>C</i> .
		_	6	48 to 55	Repeat	Sub-Lo	op 0, b	ut BA=	6							, <	20
		_	7	56 to 63	Repeat	Sub-Lo	op 0, b	ut BA=	7						1	5	

DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING. Notes: 1.

- Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
- BA: BA0 to BA2.
- Am: m means Most Significant Bit (MSB) of Row address.

Table 13: IDD5B Measurement-Loop Pattern

CK,	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
70		0	0	REF	0	0	0	1	67	0	0	0	0	0	0	_
			1, 2	D	1	0	0	0	0	0	0	0	0	0	0	_
			3,4	/D, /D	1	1	1	1/4	0	0	0	0	0	F	0	_
I			5 to 8	Repeat	cycles	14, b	ut BA	1								
Toggling Static H			9 to 12	Repeat	cycles	14, b	ut BA=	2								
St		1	13 to 16	Repeat	cycles	14, b	out BA=	3								
iii G			17 to 20	Repeat	cycles	14, b	ut BA=	4								
5 6 6			21 to 24	Repeat	cycles	14, b	ut BA=	5								
F			25 to 28	Repeat	cycles	14, b	ut BA=	6								
			29 to 32	Repeat	cycles	14, b	ut BA=	7							4	00
		2	33 to nRFC - 1	Ranga		οορ 1, ι	until nR	FC - 1.	Trunca	te, if ne	ecessa	ıry			tu	
3. 4.		AO to BA	Wost Signif	icant Bit	(MSB)	of Row	addres	DATING	BH 22	323:O	× RN.	357	SEB!			
		4	- (R)				18	3								

- DQ signals are FLOATING.
- BA: BA0 to BA2.
- Am: m means Most Significant Bit (MSB) of Row address

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					ST											LINI	St PC			
Table	e 14: IDD6, IDD6ET a	nd II	DD8 N	leasure	emen	nt-L	оор Р	atter	n					March C	EBIAN					
External Clock	Name AM	СК	CKE	RC RA	SRC	D	RRDC	LAL	/CS	Comm	n A0- Am	ВА	SRT	ASR	ODT	DQ, DQS		Active banks		Data
Off, CK and JCK = Low	IDD6: Self Refresh Current Normal Temperature Range 0°C to +85°C	N/A	0		ļ	N/A				Midle	evelo	77	Disabled (normal)	Disabled	Acted, Midlev el	Acted	N/A	None	All	Midlevel
Off, CK and	IDD6ET: Self Refresh Current Extended Temperature Range 0°C to +105°C	N/A	0		7	N/A		4	N	Midle	evel		Enabled (extended)	Disabled	Acted, Midlev el	Acted	N/A	None	All	Midlevel I
Midlevel	IDD8: Reset	N/A	Midle vel	N.LIN	7	N/A				Midle	evel		N/A	N/A	Midleve	Midle vel	N/A	None	All	Midlevel I

"Acted, midlevel" means the MR command is enabled, but the signal is midlevel. Notes: 1.

During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; MIRATIRKAN 2023-OA AN During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + tRFC.

MIRATIRAM 2023 OA AM3352 DEBIAMILIMUX PC MURATIRHAM 2023-04 AM3352 DEBIAM-LIMUX PC

Table 15: IDD7 Measurement-Loop Pattern

			50									~	3				
	CK, /CK	CKE	Sub	Cycle number	Com- mand	/cs	/RAS	/CAS	/WE	ODT	BA*3	A11	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
		OR,		0	ACT	0	0	1	1	0	00	0	0	0	0	0	_
	റ്	5	0	1	RDA	0	1	0	1	0	90	0	1	0	0	0	00000000
	201		0	2	D	1	0	0	0	201	0	0	0	0	0	0	_
~ 5	7	_			Repeat	above	D Comr	nand u	ıntil nR	RD = 1							
1/2				nRRD	ACT	0	0	1	UP	0	1	0	0	0	F	0	_
P			1	nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			1	nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	_
ile'		_			Repeat			11		nRRD -	- 1						
M		_	2	2 x RRD	Repeat		1.01										
		_	3	3 x RRD	Repeat	Sub-Lo		ut BA=									
			4	4 x nRRD	D Assert a	1 and rep	0 eat abo	0 ve D C	0 ommar	0 nd until	3 nFAW	0 – 1, if	0 neces	0 sary	F	0	
		_	5	nFAW	Repeat	Sub-Lo	op 0, bi	ut BA=	4					-			
		_	6	nFAW + nRRD	Repeat	Sub-Lo	oop 1, bi	ut BA=	5								² C
		_	7	nFAW + 2 x nRRD	Repeat	Sub-Lo	oop 0, bi	ut BA=	6						17	102	,
		_	8	nFAW + 3 x nRRD	Repeat	Sub-Lo	oop 1, bi	ut BA=	7					, A	7.		
		_	C	nFAW + 4 x	D	1	0	0	0	0	7	0	0 4	6	F	0	_
	_	_	90	nRRD	Assert a	and rep	eat abo	ve D C	ommar	nd until	2 x nF	AW – 1	.if ne	cessa	rv		
		iatic r	55/	2 x nFAW + 0	ACT	0	0	1	1	0	0	0,05	-	0	F	0	_
	č	is but Alles	10	2 x nFAW +	RDA	0	1	0	1	0	D-	Sha	1	0	F	0	00110011
	C	50		2 x nFAW +	D	1	0	0	0	0 0	0	0	0	0	F	0	_
	- Wi	<u>o</u>		2	Repeat	above	D Comr	nand ເ	ıntil 2 x	nFAW	nRR	D – 1					
MIRATIRYA	420	_		2 x nFAW + nRRD	ACT	0	0	1	1,5	4	1	0	0	0	0	0	_
1 RX			11	2 x nFAW + nRRD + 1	RDA	0	1	0 <	R	0	1	0	1	0	0	0	00000000
NIRA				2 x nFAW + nRRD + 2	D Repeat	1 above	0 D Comr	nand u	0 Intil 2 x	0 nFAW	1 + 2 x n	0 RRD –	0	0	0	0	_
M.		_	12	2 x nFAW + 2 x nRRD	Repeat		M,										
		_	13	2 x nFAW + 3 x nRRD	Repeat	Sub-Lo	oop 11, I	out BA	= 3								
		_	4.4	2 x nFAW +	D	1	0	0	0	0	3	0	0	0	0	0	_
			14	4 x nRRD	Assert a	and rep	eat abo	ve D C	ommar	nd until	3 x nF	AW – 1	, if ne	cessa	ry		20
		_	15	3 x nFAW	Repeat	Sub-Lo	op 10, l	out BA	= 4							+,	
		_	16	3 x nFAW + nRRD	Repeat	Sub-Lo	oop 11, I	out BA	= 5						, 15	70,	
		_	17	3 x nFAW + 2 + nRRD	Repeat	Sub-Lo	oop 10, I	out BA	= 6					SIR	7.		
		_	18)	3 x nFAW + 3 + nRRD	Repeat	Sub-Lo	oop 11, l	out BA	= 7					×,			
		_	5	3 x nFAW +	D	1	0	0	0	0	7	0 0	20	0	0	0	_
		3	19	4 + nRRD	Assert a	and ren											
							0.0	0		,		411	,	500	,		

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.



^{2.} Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

BA: BA0 to BA2.

^{4.} Am: m means Most Significant Bit (MSB) of Row address

2. Electrical Specifications

2.1 DC Characteristics

Table 16: DC Characteristics 1 (VDD, VDDQ = 1.283V to 1.45V)

	Parameter	Symbol	Data rate	x16(max)	unit	Notes
			(Mbps)			
,			1333	55		
of h	Operating current	IDD0	1600	LP57	mA	
IK.	(ACT-PRE)		1866 2133	59 61		
MRATIRXA						
IR'	Operating current		1333 1600	78 81		
M	(ACT-RD-PRE)	IDD1	1866	84	mA	
V	(ACT-RD-FRE)		2133	87		
			1333	8		
			1600	8		
		IDD2P0	1866	8	mA	SlowPD Exit
	Precharge power-down	C,	2133	8		C
	standby current	. 80	1333	12		, 80
		IDD2P1	1600	14	mA	FastPD Exit
		IDDZĘ	1866	16	IIIA	ASIF D EXIL
			2133	18		
		DT'	1333	22		al a
	Precharge standby current	IDD2N	1600	24	mA 💸	7
			1866	26	OK.	
			2133		-2V	
	December of the August of the		1333	29 31 33 35	SO'	
	Precharge standby ODT current	IDD2NT	1600 1866	31 33	mA	
	ODT current		2133	35		
	- O _{IX}		1333	22		
	Precharge quiet standby		1600	24		
	current	IDD2Q	1866	26)	mA	
	4		2133	26) 28		
4	~		1333	24		
IR.	Active power-down current	IDD3P	1600	26	A	
	(Always fast exit)	וטטטף	1866	28	mA	
MRATIRA			2133	30		
all?			1333	36		
/-	Active standby current	IDD3N	1600	38	mA	
			1866	40		
			2133	42		
	Operating ourrest		1333	145 155		
	Operating current (Burst read operating)	IDD4R	1600 1866	155 165	mA	<i>C</i> .
	(Durot read operating)	, 80	2133	175		, 80
		.+;-	1333	145		1
	Operating current	-120	1600	155		"AD
	(Burst write operating)	IDD4W	1866	165	mA	
	(DT.	2133	175	, (al l
	, P)		1333	228	18)	7
	Burst refresh current	IDD5B	1600	235		
	Durst refresh current	סטטטו	1866	242	2 Inex	
	255		2133	249	22.	
	Mo		1333	180		
	All bank interleave read	IDD7	1600	190	mA	
	current ON	.551	1866	200		
	-0 ²	_	2133	210		
	200		1333	100		
	RESET low current	IDD8	1600 1866	10	mA	
1/2	~		1866 2133	10		
121			2133	10		

	,	LIKUTP			LINITPO
	Table 17: Self-Refresh Curre	ent (VDD, VDDQ :	= 1.283V to 1.45V)	(2) DEB	, p.T
	Parameter 2	Symbol	max	unit	Notes
	Self-refresh current normal temperature range	IDD6	12	OA ATTH	Max
	Self-refresh current extended temperature range	IDD6ET	16	mA	Max@95°C
MRATIRY			MIRATIRXANT		

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2.2 Pin Capacitance

Table 18: Pin Capacitance [DDR3L-1333 to 2133] (Operating Temperature = 25°C, VDD, VDDQ = 1.283V to 1.45V)

OA F				DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133			
Parameter	3	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes	
Input/output		CIO	1.4	2.4	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2	
Input capacitar	nce,	ССК	0.8	1.4	0.8	2/1.4	0.8	1.3	0.8	1.3	pF	2	
Input capacitar	nce delta,	CDCK	0	0.15	SPI	0.15	0	0.15	0	0.15	pF	2, 3	<
Input/output ca delta, DQS and /DQS		CDDQS	0	0.15		0.15	0	0.15	0	0.15	pF	2, 4	8
Input capacitar (control, addre command, inpu pins)	SS,	CI	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	Ç ^{pF}	2, 5	
Input capacitar (All control input pins)		CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	V 0.2	pF	2, 6, 7	
Input capacitar (All address/co	mmand	CDI_ADD_ CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9	
Input/output ca delta, DQ,DM, /DQS, TDQS,	DQS, PAR	CDIO	-0.5	0.3	-0.5	0.3	-0.5 P	0.3	-0.5	0.3	pF	2, 10	
Input/output ca	0-1	CZQ	-	3	_	3 ,	101,5	3	-	3	pF	2, 11	
MIRATI RAP Notes	 VDD, VDD necessary) Absolute value Absolute value 	ne DM, TDQS and Q, VSS, VSSQ ap . VDD = VDDQ = alue of CCK-C/Ck alue of CIO(DQS)	oplied and 1.5V, VB (. -CIO(/DQ	d all other IAS=VDE	r pins floating 0/2 and on-di	(except t e termina	he pin under tion off.				OT as	12	
12		to ODT, /CS, CKE . applies to ODT, /			∆2,∛RAS, /CA	.S and /W	Æ.						•

- VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.5V, VBIAS=VDD/2 and on-die termination off.
- Absolute value of CCK-C/CK.
- Absolute value of CIO(DQS)-CIO(/DQS).
- CI applies to ODT, /CS, CKE, A0-A14, BA0-BA2, /RAS, /CAS and /WE.
- CDI_CTRL applies to ODT, /CS and CKE. 6.
- 7. $CDI_CTRL = CI(CTRL) - 0.5 \times (CI(CLK) + CI(/CLK)).$
- MURAT IRKAN 2023-04 ANS 352 DEBIANLINUX PC CDI_ADD_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.
- $CDI_ADD_CMD = CI(ADD_CMD) 0.5 \times (CI(CLK) + CI(/CLK)).$ 9.
- 10. $CDIO=CIO(DQ,DM) 0.5 \times (CIO(DQS)+CIO(/DQS))$.
- 11. Maximum external load capacitance on ZQ pin: 5pF.



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2.3 Standard SpeedBins

		LIMITAR				MUTPO
	2.3 Standard Sp	Y			EBIAM	
	Table 19: DDR3 Speed Bin CL-tRCD-tRP	L-1333 Speed Bins –	DDR3L-1333 9-9-9			
		/CAS write latency	min	max O	— Unit	Notes
MRATIRY	tAASI	,	13.5 (13.125)	20015	ns	10
PX	tRCD		13.5 (13.125)	HAT-	ns	10
NRA	tRP		13.5 (13.125)		ns	10
M	tRC		49.5 (49.125)		ns	10
	tRAS		36	9 x tREFI	ns	5
	tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 5, 9
		CWL=6, 7,	Reserved	Reserved	ns	4
		CWL=5	2.5	3.3	ns	1, 2, 3, 5
	tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 5
		CWL=7,	Reserved	Reserved	ns	4
		CWL=5	Reserved	Reserved	ns	4
	tCK(avg)@CL=7	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 5
		CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
	Syl.	CWL=5	Reserved	Reserved	ns	4
	tCK(avg)@CL=8	CWL=6	1.875	<2.5	ns	1, 2, 3, 5
	N.	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
	tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
		CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 5
	tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
, 5	7	CWL=7	1.5	<1.875	ns	1, 2, 3, 5
24	Supported CL settings		5, 6	, (7) , 8, (9), 10,	nCK	

5, 6, 7,

nCK

MURAT IRVAN 2023-04 ANS 352 DEBIANLINUX PC MURAT IRWAN 2023-04 AND 3552 DEBIANLIMUX PC

Supported CWL settings

		LIKUTPE				AUTRE
	Table 20: DDR3L-1600	BIAI			EBIALL	<u>></u>
	252	opeeu bilis		357) *	
	Speed Bin	_	DDR3L-1600			
	CL-tRCD-tRP	-	11-11-11			
I	Symbol	/CAS write latency	min	max	Unit	Notes
I	tAA		13.75	—200 l	ns	11
1			(13.125) 13.75	4		
at	tRCD		(13.125)		ns	11
NURATIRY			13.75			
PA	tRP		(13.125)	_	ns	11
W.	tRC		48.75		20	11
	IRC		(48.125)		ns	11
	tRAS		35	9 x tREFI	ns	10
	tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 6, 9
		CWL=6, 7, 8	Reserved	Reserved	ns	4
	.01//	CWL=5	2.5	3.3	ns	1, 2, 3, 6
	tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 6
	-	CWL=7, 8	Reserved Reserved	Reserved Reserved	ns	4
		CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 6
	tCK(avg)@CL=7	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
		CWL=8	Reserved	Reserved	ns	4
	3	CWL=5	Reserved	Reserved	ns	4
	1011 1001/135	CWL=6	1.875	<2.5	ns	1, 2, 3, 6
	tCK(avg)@CL=8	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
		CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	023	CWL=5, 6	Reserved	Reserved	ns	4
	tCK(avg)@CL=9	CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 6
MIRATIRY	<u> </u>	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
1/K	101// \0.01 10	CWL=5, 6	Reserved		ns	4
.DA	tCK(avg)@CL=10	CWL=7	1.5	<1.875	ns	1, 2, 3, 6
N)	-	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
19	tCK(avg)@CL=11	CWL=5, 6, 7 CWL=8	Reserved 1.25	Reserved <1.5	ns ns	1, 2, 3
	Supported CL settings		5.6 (7)	8 (9) 10 11	nCK	
	Supported CWL settings		5, 5, (1)	, 6, 7, 8	nCK	
	Supported CWL settings Annual State of the settings of the setting of the set	EBAN-LINUX PC		AN 2023 OK AN 3352 O	EBIANLI	Nut PC
MURATIRY	A 201		NIRATIRY 25	A 201		
T	nototo	®				

		LIMITAPO				MITPE
	Table 21: DDR3L-186	Speed Bins		,	DEBIAN	
	Speed Bin	_	DDR3L-1866		, ,	
	CL-tRCD-tRP Symbol	/CAS write latency	13-13-13 min	max OA	 Unit	Notes
	-0 ⁵	7CAS WITTE TALEFICY	13.91	20073	ns	Notes
.01	tRCD		(13.125) 13.91 (13.125)	axan-	ns	
MRATIRY!	tRP		13.91 (13.125)	_	ns	
and a	tRC		47.91 (47.125)	_	ns	
	tRAS		34	9 x tREFI	ns	
	tCK(avg)@CL=5	CWL=5	Reserved	Reserved	ns	1, 2, 3, 4, 7
		CWL=6, 7, 8, 9	Reserved	Reserved	ns	4,
	101// \@01 0	CWL=5	2.5	3.3	ns	1, 2, 3, 7
	tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 7
	-	CWL=7, 8, 9 CWL=5	Reserved Reserved	Reserved Reserved	ns	4
	tCK(avg)@CL=7	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	ick(avg)@cL=1	CWL=7, 8, 9	Reserved	Reserved	ns	4
		CWL=5	Reserved	Reserved	ns	4
	350	CWL=6	1.875	< 2.5	ns	1, 2, 3, 7
	tCK(avg)@CL=8	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 7
	V Bla	CWL=8,9	Reserved	Reserved	ns	4
	- OK	CWL=5, 6	Reserved	Reserved	ns	4
	2,2	CWL=7	1.5	< 1.875	ns	1, 2, 3, 4, 7
	tCK(avg)@CL=9	CWL=8	Reserved	Reserved	ns	4
, _ 5		CWL=9	Reserved	Reserved	ns	1, 2, 3, 4, 7
PK	tCK(avg)@CL=10	CWL=5, 6		Reserved	ns	4
NURATIRY		CWL=7	1.5	< 1.875	ns	1, 2, 3, 7
Pr		CWL=8	Reserved	Reserved	ns	1, 2, 3, 4, 7
M		CWL=5, 6, 7	Reserved	Reserved	ns	4
	tCK(avg)@CL=11	CWL=8	1.25	< 1.5	ns	1, 2, 3, 4, 7
		CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
		CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	tCK(avg)@CL=12	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
		CWL=5, 6, 7, 8	Reserved	Reserved	ns	4, 8
	tCK(avg)@CL=13	CWL=9	1.07	< 1.25	ns	12,3
	Supported CL settings	14	0.0	10 10 (7) (0) (11)	014	IL.
	Supported CWL settings	4.		5, 6, 7, 8, 9	nCK	<i>*</i>
MRATIRX	Supported CL settings Supported CWL settings	į į į į į į į į į į į į į į į į į į į	MIRAT	10, 13, (7), (9), (11) 5, 6, 7, 8, 9	DEBI	
	naeto		26			



		180				180
		INITRO				AUT PO
		LIK				
		, al			Ja.	
	Table 22: DDR3L-213	3 Speed Bins			BI	
		opeca ziiic				
	Speed Bin	_	DDR3L-2133	_		
	CL-tRCD-tRR	_	14-14-14	1133	_	
	Symbol	/CAS write latency	min	max	Unit	Notes
	tAA 02		13.09	20 00	ns	11
	tRCD		13.09	-01/2	ns	
	tRP		13.09	7.1	ns	
NRATIRY!	tRC		46.09	<u> </u>	ns	
X IK.	tRAS		33.0	9 x tREFI	ns	9
2A	tCK(avg)@CL=5	CWL=5,6,7, 8, 9,10	Reserved	Reserved	ns	1, 2, 3, 4, 8
NUP		CWL=5	2.5	3.3	ns	1, 2, 3, 8
b.	tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 8
	-	CWL=7, 8, 9,10	Reserved	Reserved	ns	4
	tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
		CWL=6	1.875	< 2.5	ns	1, 2, 3, 8
		CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 8
	tCK(avg)@CL=8	CWL=8, 9,10	Reserved	Reserved	ns	4 ×
		CWL=5	Reserved	Reserved	ns	4
		CWL=6 CWL=7	1.875	< 2.5	ns	1, 2, 3, 8
		CWL=8, 9,10	Reserved Reserved	Reserved Reserved	ns	1, 2, 3, 4, 8
		CWL=5, 6	Reserved	Reserved	ns	4
	tCK(avg)@CL=9	CWL=7	1.5	< 1.875	ns	1, 2, 3, 8
		CWL=8	Reserved	Reserved 25	ns	1, 2, 3, 4, 8
		CWL=9,10	Reserved	Reserved Reserved	ns	4
		CWL=5, 6	Reserved	Reserved	ns	4
	tCK(avg)@CL=10	CWL=7	1.5	< 1.875	ns	1, 2, 3, 8
		CWL=8, 9	Reserved	Reserved	ns	1, 2, 3, 4, 8
		CWL=10	Reserved	Reserved	ns	4
MIRATIRYS		CWL=5, 6, 7	Reserved	Reserved	ns	4
Y III	101(/) @ 01 - 44	CWL=8	1.25	< 1.5	ns	1, 2, 3, 8
.QA	tCK(avg)@CL=11	CWL=9	Reserved A	Reserved	ns	1, 2, 3, 4, 8
NUM		CWL=10	Reserved	Reserved	ns	1, 2, 3, 4
H.		CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	tCK(avg)@CL=12	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4, 8
		CWL=10	Reserved	Reserved	ns	1, 2, 3, 4
	tCK(avg)@CL=13	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
		CWL=9	1.07	< 1.25	ns	1, 2, 3, 8
		CWL=10	Reserved	Reserved	ns	1, 2, 3, 4
	tCK(avg)@CL=14	CWL=5, 6, 7, 8,9	Reserved	Reserved	ns	4
		CWL=10	0.938	< 1.07	ns	1, 2, 3
	Supported CL settings	SIRT	5,6,7,8,9,1	0,11,12,13,14	nCK	

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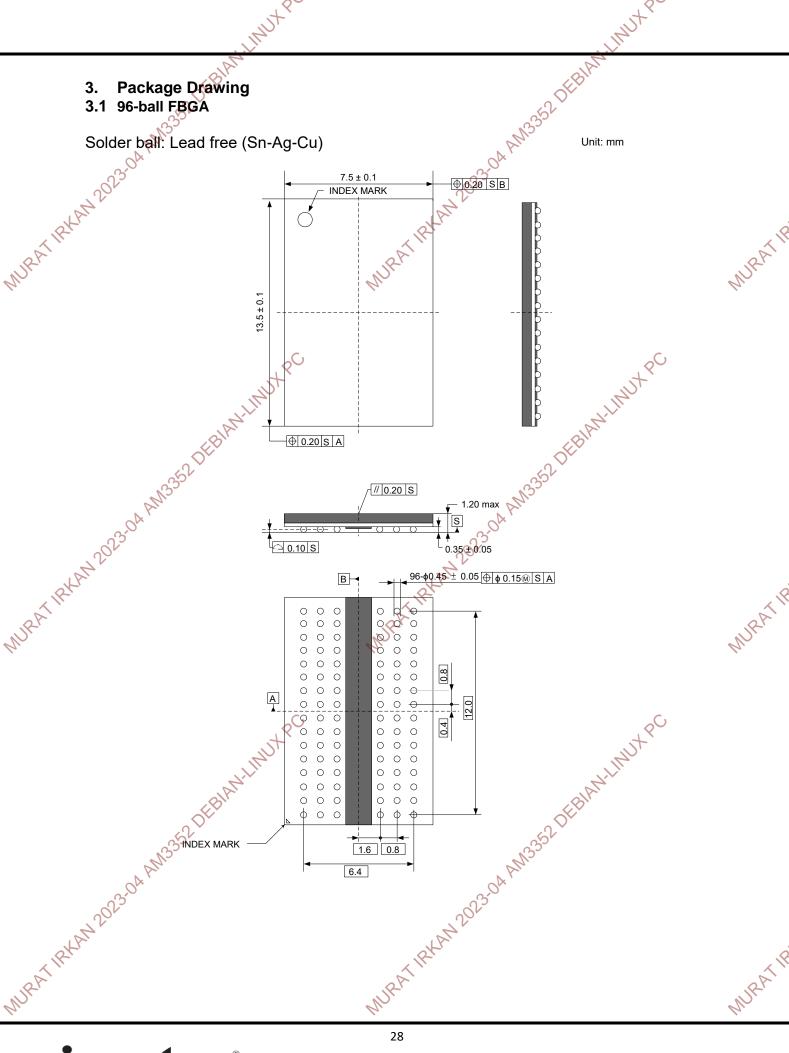
Supported CWL settings

Electrical Characteristics & AC Timing for DDR3L-1600 to DDR3L-2133 (Cont'd) Standard Speed Bins (Cont'd)

- NOTE 1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- tCK(AVG).MIN limits: Since CAS Latency is not purely analog data and strobe output are synchronized by the DLL all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
- NOTE 3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
- NOTE 4. 'Reserved' settings are not allowed. User must program a different value.
- NOTE 5. Any DDR3L-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 6. Any DDR3L-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 7. Any DDR3L 1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR3L-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- NOTE 9. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD
- NOTE 10 tREFI depends on operating commercial temperature and industrial temperature.
- NOTE 11. For devices supporting optional down binning to CL=11 and CL=9, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match.

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NOTES FOR CMOS DEVICES

1) PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function. <

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2) Usage in exposure to direct suplight or the outdoors, or in dusty places.

- 3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CQ2, H2S, NH3, SO2, and NOx.
- Usage in environments with static electricity, or strong electromagnetic waves or radiation.

5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.

7) Usage near heating elements, igniters, or flammable items.

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