

# DDR4 SDRAM LRDIMM

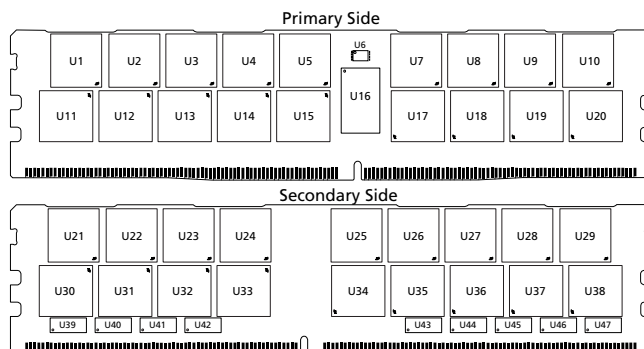
## Addendum

### MTA72ASS8G72LZ – 64GB

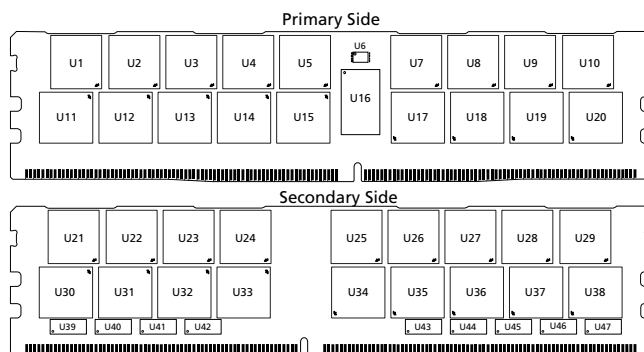
#### Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 LRDIMM Core data sheet
- 288-pin, command/address/control-registered, data-buffered, load-reduced dual in-line memory module (LRDIMM)
- Fast data transfer rates: PC4-3200, PC4-2933, PC4-2666, PC4-2400
- 64GB (8 Gig x 72)
- Quad-rank, using 16Gb TwinDie DDR4
- On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each

**Figure 1: 288-Pin LRDIMM (R/C-D3)**



**Figure 2: 288-Pin LRDIMM (R/C-E2)**



#### Options

- Operating temperature
  - Commercial (0°C ≤ T<sub>OPER</sub> ≤ 95°C)
- Package
  - 288-pin DIMM (Green)
- Frequency/CAS latency
  - 0.625ns @ CL = 22 (DDR4-3200)
  - 0.682ns @ CL = 21 (DDR4-2933)
  - 0.75ns @ CL = 19 (DDR4-2666)
  - 0.83ns @ CL = 17 (DDR4-2400)

#### Marking

None

Z

-3G2

-2G9

-2G6

-2G3



## 64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM Features

**Table 1: Addressing**

Parameter	64GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb TwinDie (4 Gig x 4), 16 banks
Module rank address	4 CS <sub>n</sub> [3:0]

**Table 2: Part Numbers and Timing Parameters – 64GB Modules**

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL <sub>n</sub> RCD <sub>n</sub> RP)
MTA72ASS8G72LZ-3G2__	64GB	8 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA72ASS8G72LZ-2G9__	64GB	8 Gig x 72	23.47 GB/s	0.682ns/2933 MT/s	21-21-21
MTA72ASS8G72LZ-2G6__	64GB	8 Gig x 72	21.3 GB/s	0.75ns/2666 MT/s	19-19-19
MTA72ASS8G72LZ-2G3__	64GB	8 Gig x 72	19.2 GB/s	0.83ns/2400 MT/s	17-17-17

- Notes: 1. Base device: MT40A4G4, 16Gb TwinDie DDR4 SDRAM. The data sheet for the base device can be found on [micron.com](http://micron.com).
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA72ASS8G72LZ-3G2R2.

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## DQ Map: R/C-E2

Table 3: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	7	155	U2	0	15	166
	1	5	148		1	13	159
	2	6	10		2	14	21
	3	4	3		3	12	14
U3	0	23	177	U4	0	31	188
	1	21	170		1	29	181
	2	22	32		2	30	43
	3	20	25		3	28	36
U5	0	CB7	199	U7	0	39	247
	1	CB5	192		1	37	240
	2	CB6	54		2	38	102
	3	CB4	47		3	36	95
U8	0	47	258	U9	0	55	269
	1	45	251		1	53	262
	2	46	113		2	54	124
	3	44	106		3	52	117
U10	0	63	280	U12	0	2	12
	1	61	273		1	1	150
	2	62	135		2	3	157
	3	60	128		3	0	5
U13	0	8	16	U14	0	16	27
	1	10	23		1	18	34
	2	9	161		2	17	172
	3	11	168		3	19	179
U15	0	26	45	U16	0	CB2	56
	1	25	183		1	CB1	194
	2	27	190		2	CB3	201
	3	24	38		3	CB0	49
U17	0	34	104	U18	0	42	115
	1	32	97		1	40	108
	2	35	249		2	43	260
	3	33	242		3	41	253
U19	0	50	126	U20	0	56	130
	1	48	119		1	58	137
	2	51	271		2	57	275
	3	49	264		3	59	282



**Table 4: Component-to-Module DQ Map, Back**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	61	273	U22	0	53	262
	1	63	280		1	55	269
	2	60	128		2	52	117
	3	62	135		3	54	124
U23	0	45	251	U24	0	37	240
	1	47	258		1	39	247
	2	44	106		2	36	95
	3	46	113		3	38	102
U25	0	CB5	192	U26	0	29	181
	1	CB7	199		1	31	188
	2	CB4	47		2	28	36
	3	CB6	54		3	30	43
U27	0	21	170	U28	0	13	159
	1	23	177		1	15	166
	2	20	25		2	12	14
	3	22	32		3	14	21
U29	0	5	148	U30	0	58	137
	1	7	155		1	56	130
	2	4	3		2	59	282
	3	6	10		3	57	275
U31	0	48	119	U32	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
U33	0	32	97	U34	0	CB1	194
	1	34	104		1	CB2	56
	2	33	242		2	CB0	49
	3	35	249		3	CB3	201
U35	0	25	183	U36	0	18	34
	1	26	45		1	16	27
	2	24	38		2	19	179
	3	27	190		3	17	172
U37	0	10	23	U38	0	1	150
	1	8	16		1	2	12
	2	11	168		2	0	5
	3	9	161		3	3	157



## DQ Map: R/C-D3

Table 5: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	6	10	U2	0	14	21
	1	4	3		1	12	14
	2	7	155		2	15	166
	3	5	148		3	13	159
U3	0	22	32	U4	0	30	43
	1	20	25		1	28	36
	2	23	177		2	31	188
	3	21	170		3	29	181
U5	0	CB6	54	U7	0	38	102
	1	CB4	47		1	36	95
	2	CB7	199		2	39	247
	3	CB5	192		3	37	240
U8	0	46	113	U9	0	54	124
	1	44	106		1	52	117
	2	47	258		2	55	269
	3	45	251		3	53	262
U10	0	62	135	U11	0	2	12
	1	60	128		1	0	5
	2	63	280		2	3	157
	3	61	273		3	1	150
U12	0	10	23	U13	0	18	34
	1	8	16		1	16	27
	2	11	168		2	19	179
	3	9	161		3	17	172
U14	0	26	45	U15	0	CB2	56
	1	24	38		1	CB0	49
	2	27	190		2	CB3	201
	3	25	183		3	CB1	194
U17	0	34	104	U18	0	42	115
	1	32	97		1	40	108
	2	35	249		2	43	260
	3	33	242		3	41	253
U19	0	50	126	U20	0	58	137
	1	48	119		1	56	130
	2	51	271		2	59	282
	3	49	264		3	57	275



**Table 6: Component-to-Module DQ Map, Back**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	60	128	U22	0	52	117
	1	62	135		1	54	124
	2	61	273		2	53	262
	3	63	280		3	55	269
U23	0	44	106	U24	0	36	95
	1	46	113		1	38	102
	2	45	251		2	37	240
	3	47	258		3	39	247
U25	0	CB4	47	U26	0	28	36
	1	CB6	54		1	30	43
	2	CB5	192		2	29	181
	3	CB7	199		3	31	188
U27	0	20	25	U28	0	12	14
	1	22	32		1	14	21
	2	21	170		2	13	159
	3	23	177		3	15	166
U29	0	4	3	U30	0	56	130
	1	6	10		1	58	137
	2	5	148		2	57	275
	3	7	155		3	59	282
U31	0	48	119	U32	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
U33	0	32	97	U34	0	CB0	49
	1	34	104		1	CB2	56
	2	33	242		2	CB1	194
	3	35	249		3	CB3	201
U35	0	24	38	U36	0	16	27
	1	26	45		1	18	34
	2	25	183		2	17	172
	3	27	190		3	19	179
U37	0	8	16	U38	0	0	5
	1	10	23		1	2	12
	2	9	161		2	1	150
	3	11	168		3	3	157

## I<sub>DD</sub> Specifications

**Table 7: DDR4 I<sub>DD</sub> Specifications and Conditions (0° ≤ T<sub>C</sub> ≤ 85°) – 64GB (Die Revision B)**

Values are for the MT40A4G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	2666	2400	Units
One bank ACTIVATE-PRECHARGE current	I <sub>CDD0</sub>	2232	2178	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>pp</sub> current	I <sub>CPP0</sub>	216	216	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>CDD1</sub>	2448	2394	mA
Precharge standby current	I <sub>CDD2N</sub>	1980	1962	mA
Precharge standby ODT current	I <sub>CDD2NT</sub>	2250	2250	mA
Precharge power-down current	I <sub>CDD2P</sub>	1800	1800	mA
Precharge quite standby current	I <sub>CDD2Q</sub>	1890	1890	mA
Active standby current	I <sub>CDD3N</sub>	2088	2034	mA
Active standby I <sub>pp</sub> current	I <sub>CPP3N</sub>	216	216	mA
Active power-down current	I <sub>CDD3P</sub>	1962	1926	mA
Burst read current	I <sub>CDD4R</sub>	3582	3384	mA
Burst write current	I <sub>CDD4W</sub>	3420	3258	mA
Burst refresh current (1x REF)	I <sub>CDD5R</sub>	2358	2304	mA
Burst refresh I <sub>pp</sub> current (1x REF)	I <sub>CPP5R</sub>	252	252	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I <sub>CDD6N</sub>	1980	1980	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I <sub>CDD6E</sub>	2160	2160	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I <sub>CDD6R</sub>	1620	1620	mA
Auto self refresh current (25°C)	I <sub>CDD6A</sub>	1209.6	1209.6	mA
Auto self refresh current (45°C)	I <sub>CDD6A</sub>	1620	1620	mA
Auto self refresh current (75°C)	I <sub>CDD6A</sub>	1980	1980	mA
Auto self refresh current I <sub>pp</sub> current	I <sub>CPP6X</sub>	288	288	mA
Bank interleave read current	I <sub>CDD7</sub>	8100	7560	mA
Bank interleave read I <sub>pp</sub> current	I <sub>CPP7</sub>	486	468	mA
Maximum power-down current	I <sub>CDD8</sub>	1800	1800	mA

Notes: 1. When T<sub>C</sub> > 85°C, the I<sub>DD</sub> and I<sub>pp</sub> values must be derated. Refer to the base device data sheet I<sub>DD</sub> and I<sub>pp</sub> specification tables for derating values for the applicable die-revision.





## 64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM I<sub>DD</sub> Specifications

**Table 8: DDR4 I<sub>DD</sub> Specifications and Conditions (0° ≤ T<sub>C</sub> ≤ 85°) – 64GB (Die Revision D)**

Values are for the MT40A4G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	2933	2666	Units
One bank ACTIVATE-PRECHARGE current	I <sub>CDD0</sub>	2286	2232	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>pp</sub> current	I <sub>CPP0</sub>	216	216	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>CDD1</sub>	2502	2448	mA
Precharge standby current	I <sub>CDD2N</sub>	1998	1980	mA
Precharge standby ODT current	I <sub>CDD2NT</sub>	2340	2250	mA
Precharge power-down current	I <sub>CDD2P</sub>	1800	1800	mA
Precharge quite standby current	I <sub>CDD2Q</sub>	1890	1890	mA
Active standby current	I <sub>CDD3N</sub>	2232	2178	mA
Active standby I <sub>pp</sub> current	I <sub>CPP3N</sub>	216	216	mA
Active power-down current	I <sub>CDD3P</sub>	1998	1962	mA
Burst read current	I <sub>CDD4R</sub>	3780	3582	mA
Burst write current	I <sub>CDD4W</sub>	3744	3600	mA
Burst refresh current (1x REF)	I <sub>CDD5R</sub>	2502	2448	mA
Burst refresh I <sub>pp</sub> current (1x REF)	I <sub>CPP5R</sub>	252	252	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I <sub>CDD6N</sub>	2016	2016	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I <sub>CDD6E</sub>	2196	2196	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I <sub>CDD6R</sub>	1656	1656	mA
Auto self refresh current (25°C)	I <sub>CDD6A</sub>	1209.6	1209.6	mA
Auto self refresh current (45°C)	I <sub>CDD6A</sub>	1656	1656	mA
Auto self refresh current (75°C)	I <sub>CDD6A</sub>	2016	2016	mA
Auto self refresh current I <sub>pp</sub> current	I <sub>CPP6X</sub>	288	288	mA
Bank interleave read current	I <sub>CDD7</sub>	5274	5004	mA
Bank interleave read I <sub>pp</sub> current	I <sub>CPP7</sub>	504	486	mA
Maximum power-down current	I <sub>CDD8</sub>	1800	1800	mA

Notes: 1. When T<sub>C</sub> > 85°C, the I<sub>DD</sub> and I<sub>pp</sub> values must be derated. Refer to the base device data sheet I<sub>DD</sub> and I<sub>pp</sub> specification tables for derating values for the applicable die-revision.



## 64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM I<sub>DD</sub> Specifications

**Table 9: DDR4 I<sub>DD</sub> Specifications and Conditions (0° ≤ T<sub>C</sub> ≤ 85°) – 64GB (Die Revision R)**

Values are for the MT40A4G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

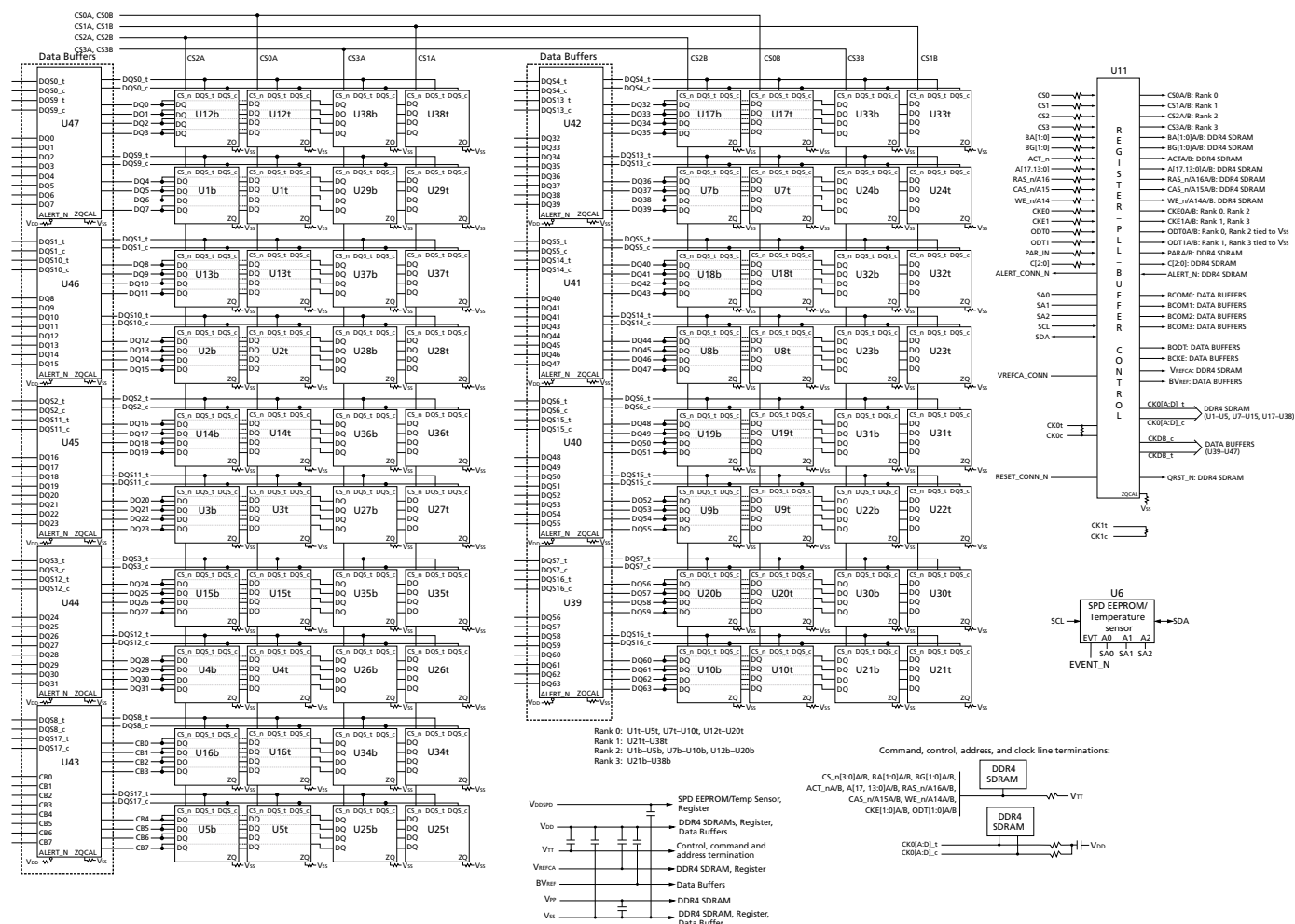
Parameter	Symbol	3200	2933	2666	Units
One bank ACTIVATE-PRECHARGE current	I <sub>CDD0</sub>	2448	2412	2376	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>pp</sub> current	I <sub>CPP0</sub>	234	234	234	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>CDD1</sub>	2538	2502	2466	mA
Precharge standby current	I <sub>CDD2N</sub>	2304	2286	2268	mA
Precharge standby ODT current	I <sub>CDD2NT</sub>	2358	2322	2286	mA
Precharge power-down current	I <sub>CDD2P</sub>	2160	2160	2160	mA
Precharge quite standby current	I <sub>CDD2Q</sub>	2232	2232	2232	mA
Active standby current	I <sub>CDD3N</sub>	2376	2340	2304	mA
Active standby I <sub>pp</sub> current	I <sub>CPP3N</sub>	144	144	144	mA
Active power-down current	I <sub>CDD3P</sub>	2196	2178	2160	mA
Burst read current	I <sub>CDD4R</sub>	3474	3330	3204	mA
Burst write current	I <sub>CDD4W</sub>	3096	2988	2880	mA
Distributed refresh current (1x REF)	I <sub>CDD5R</sub>	2466	2448	2430	mA
Distributed refresh I <sub>pp</sub> current (1x REF)	I <sub>CPP5R</sub>	252	252	252	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I <sub>CDD6N</sub>	2232	2232	2232	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I <sub>CDD6E</sub>	2952	2952	2952	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I <sub>CDD6R</sub>	1764	1764	1764	mA
Auto self refresh current (25°C)	I <sub>CDD6A</sub>	1368	1368	1368	mA
Auto self refresh current (45°C)	I <sub>CDD6A</sub>	1764	1764	1764	mA
Auto self refresh current (75°C)	I <sub>CDD6A</sub>	2124	2124	2124	mA
Auto self refresh current (95°C)	I <sub>CDD6A</sub>	2952	2952	2952	mA
Auto self refresh current I <sub>pp</sub> current	I <sub>CPP6X</sub>	288	288	288	mA
Bank interleave read current	I <sub>CDD7</sub>	5490	5490	4968	mA
Bank interleave read I <sub>pp</sub> current	I <sub>CPP7</sub>	576	576	576	mA
Maximum power-down current	I <sub>CDD8</sub>	1728	1728	1728	mA

Notes: 1. When T<sub>C</sub> > 85°C, the I<sub>DD</sub> and I<sub>pp</sub> values must be derated. Refer to the base device data sheet I<sub>DD</sub> and I<sub>pp</sub> specification tables for derating values for the applicable die-revision.

## 64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM Functional Block Diagram

## Functional Block Diagram

### Figure 3: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external  $240\Omega \pm 1\%$  resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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