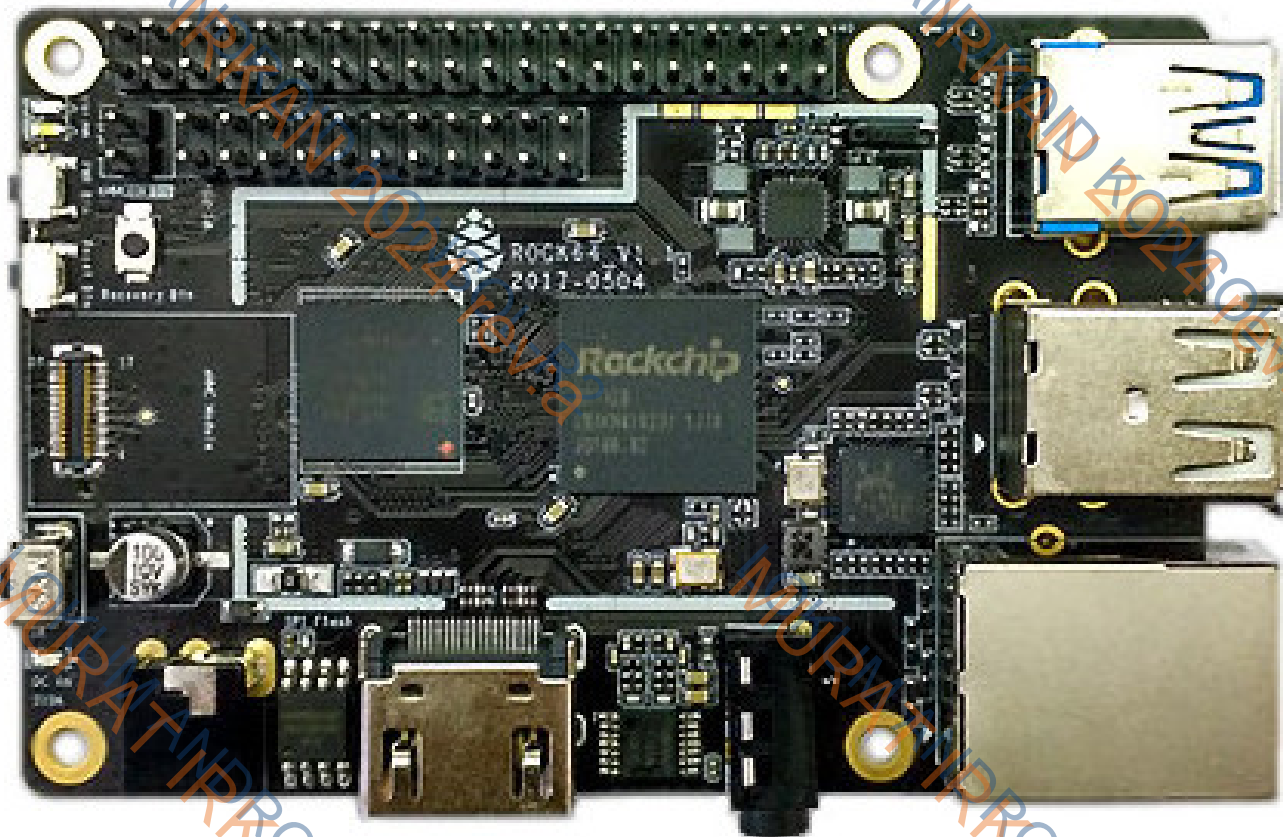


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07.System Power-PMIC RK805-1		-----5
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RK3328 BOX Ref



Bill

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

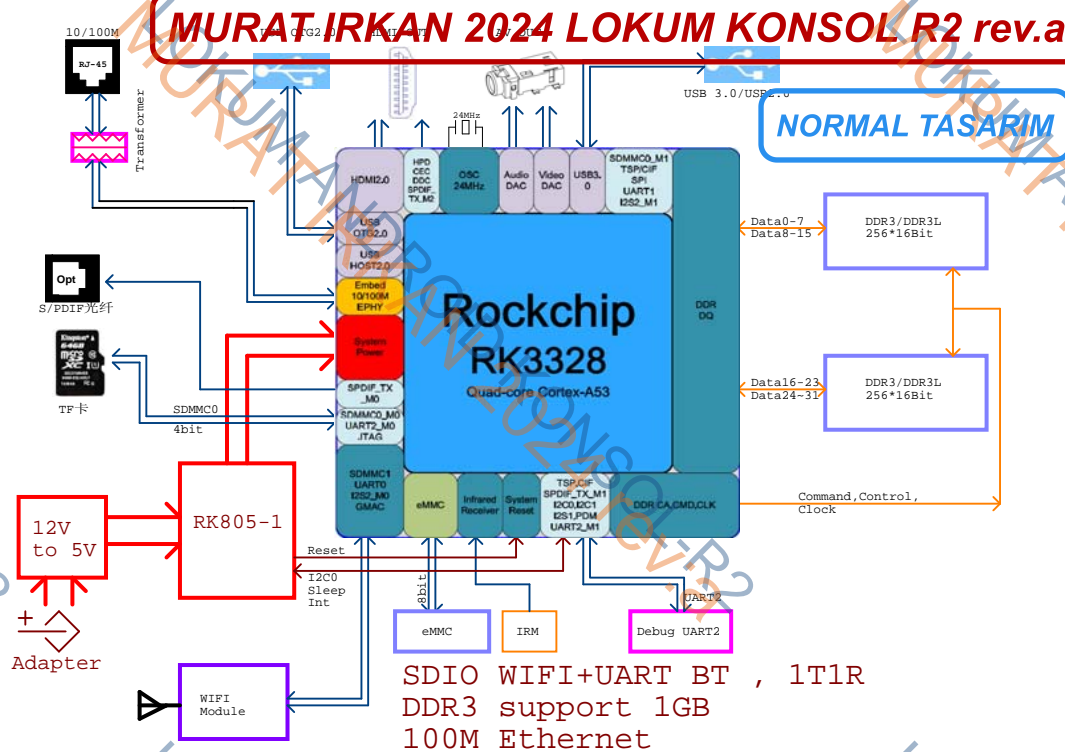
Note:

Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

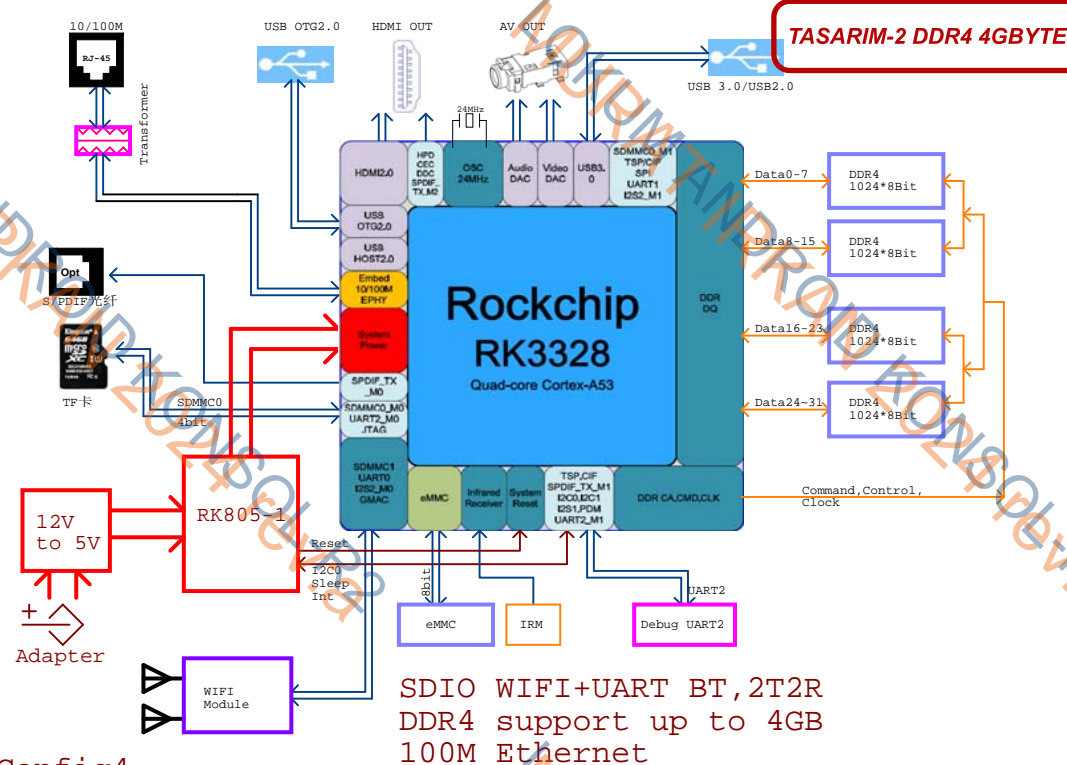
MURAT IRKAN 2024 LOKUM KONSOL R2 rev.a

NORMAL TASARIM



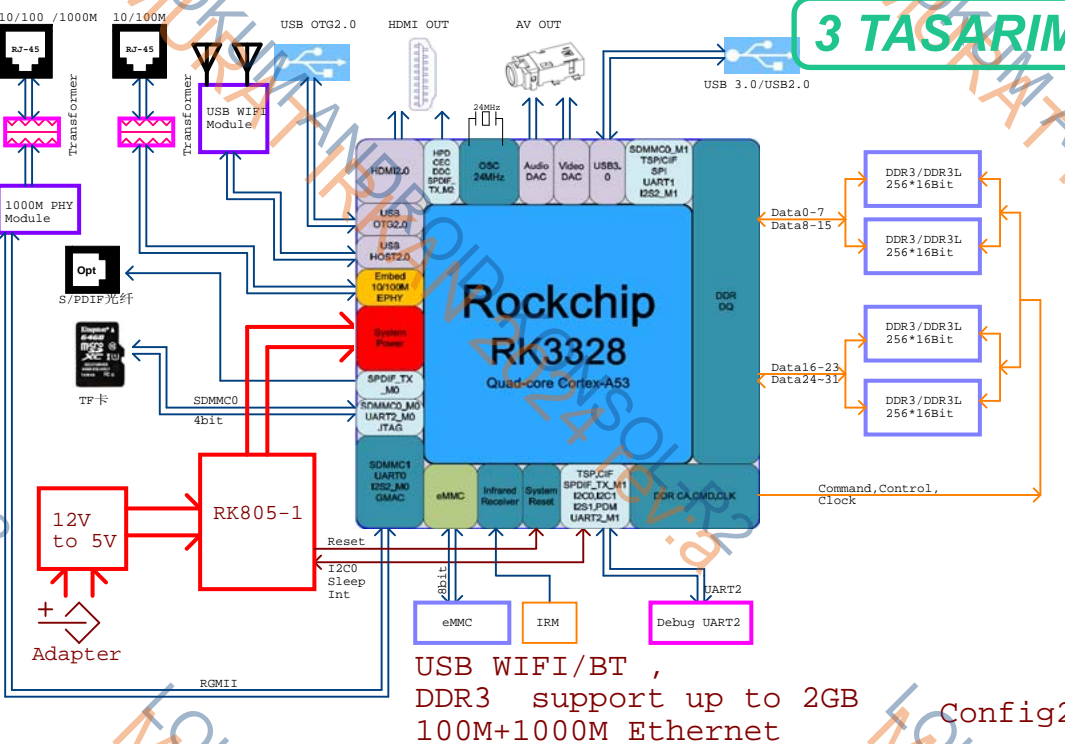
Default config

TASARIM-2 DDR4 4GBYTE

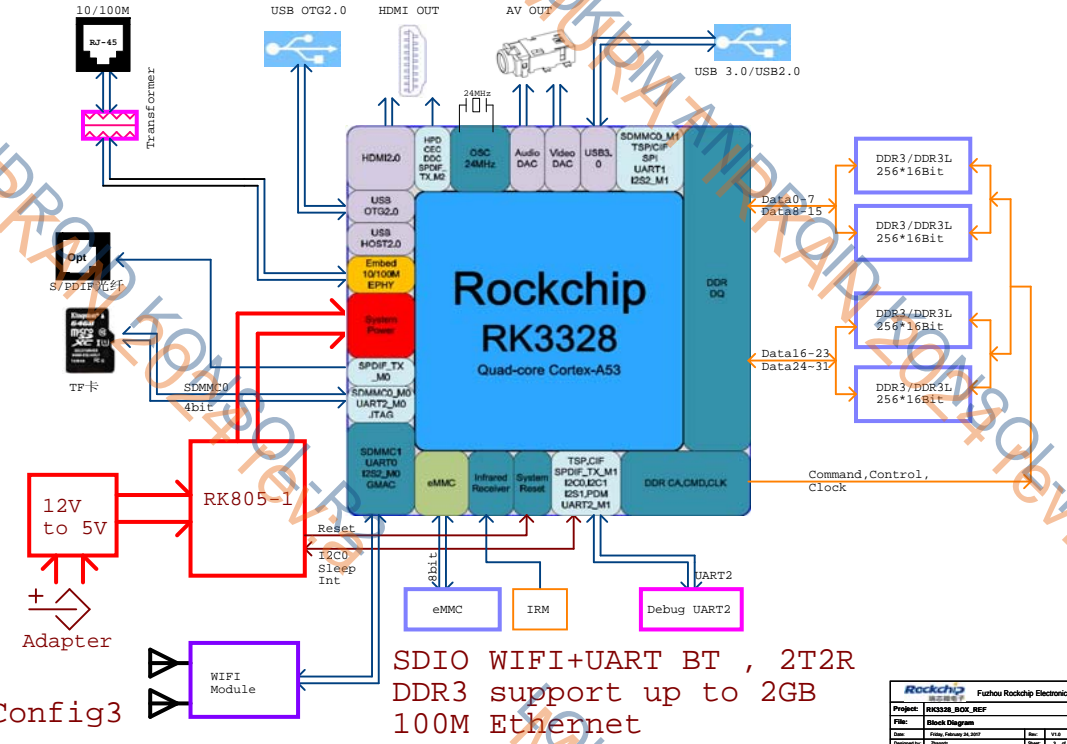


Config4

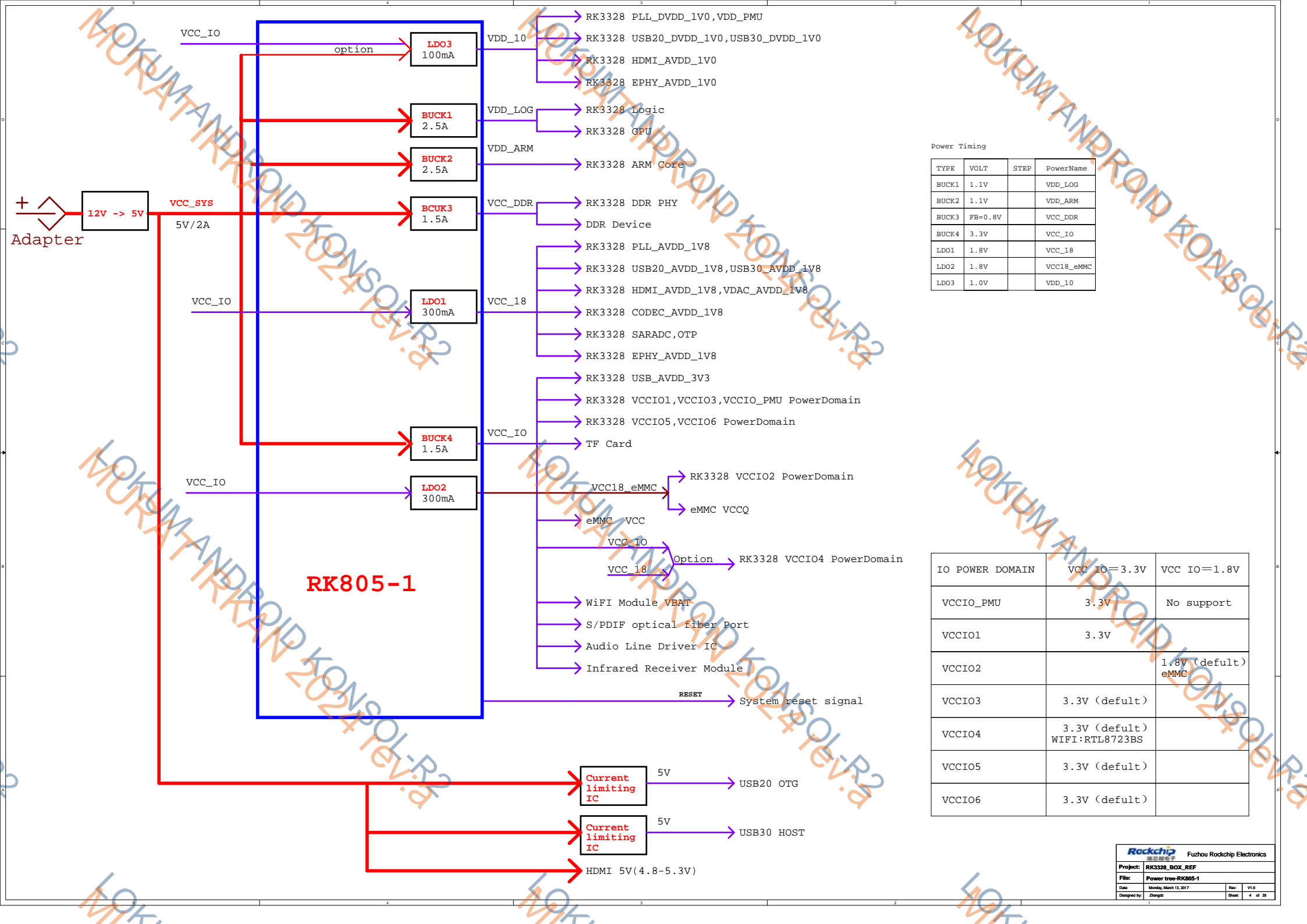
3 TASARIM



Config2



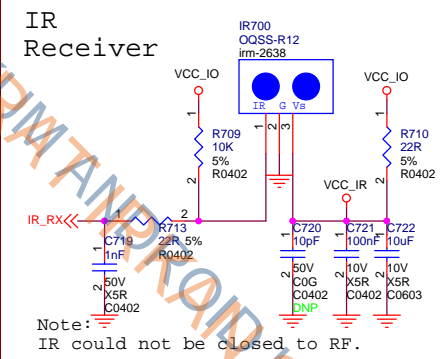
Config3



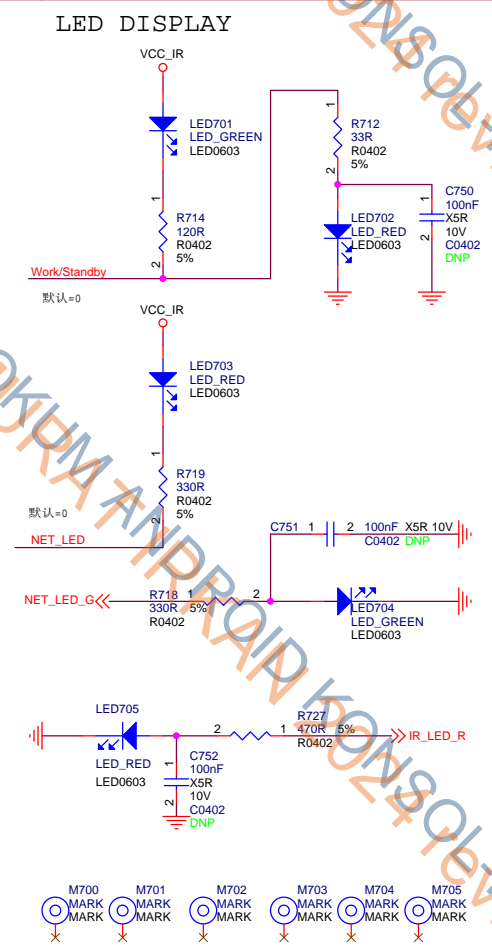
Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

IO POWER DOMAIN	VCC IO=3.3V	VCC IO=1.8V
VCCIO_PMU	3.3V	No support
VCCIO1	3.3V	
VCCIO2		1.8V (default) eMMC
VCCIO3	3.3V (default)	
VCCIO4	3.3V (default) WIFI:RTL8723BS	
VCCIO5	3.3V (default)	
VCCIO6	3.3V (default)	



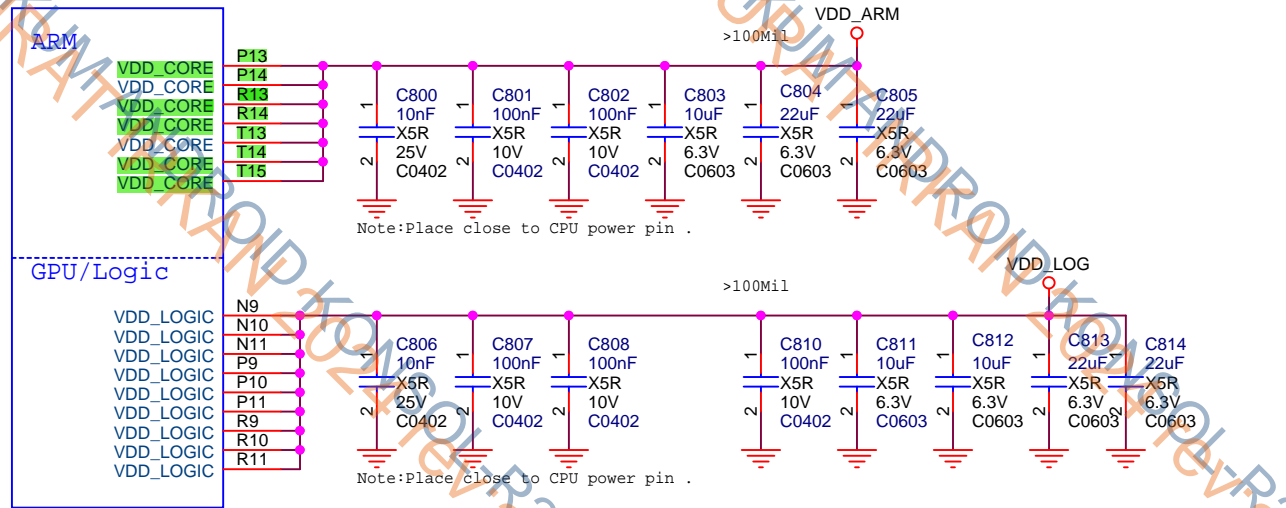
VCC_SYS



	DDR3	DDR3L	DDR4
VCC_DDR	1.527V	1.353V	1.2V
R725	100K 1%	47K 1%	51K 1%
R726	110K 1%	68K 1%	100K 1%

ARM GUC VE GPU GUC

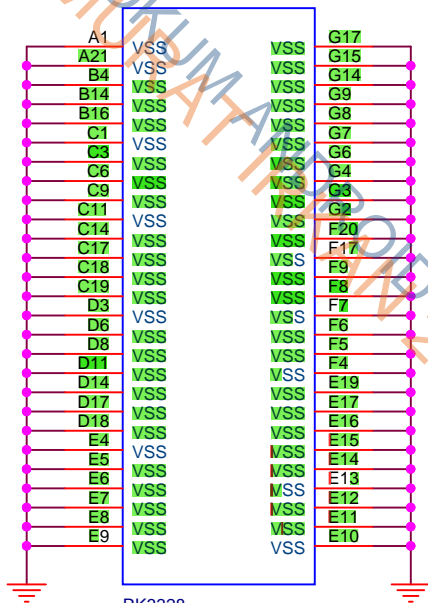
U800N



RK3328

BGA395_14R00X14R00X1R24

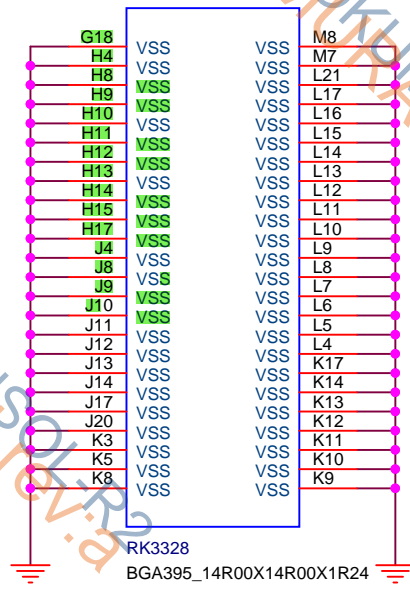
U800O



RK3328

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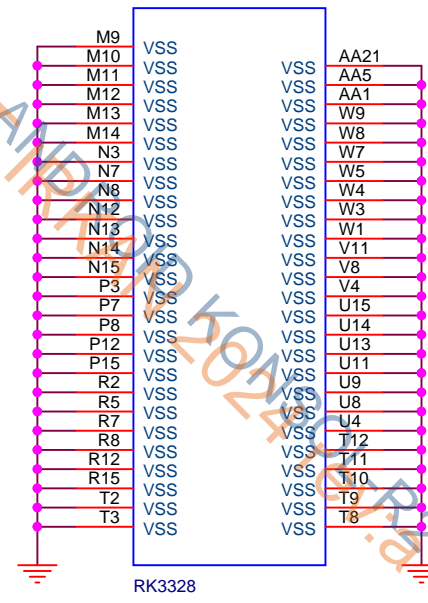
U800P



RK3328

BGA395_14R00X14R00X1R24

U800Q



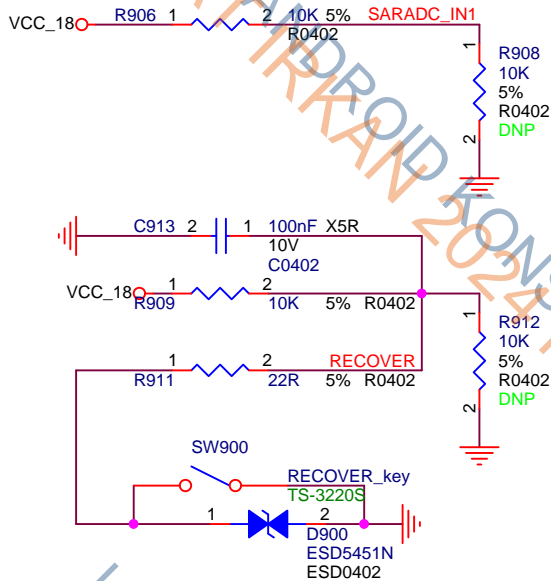
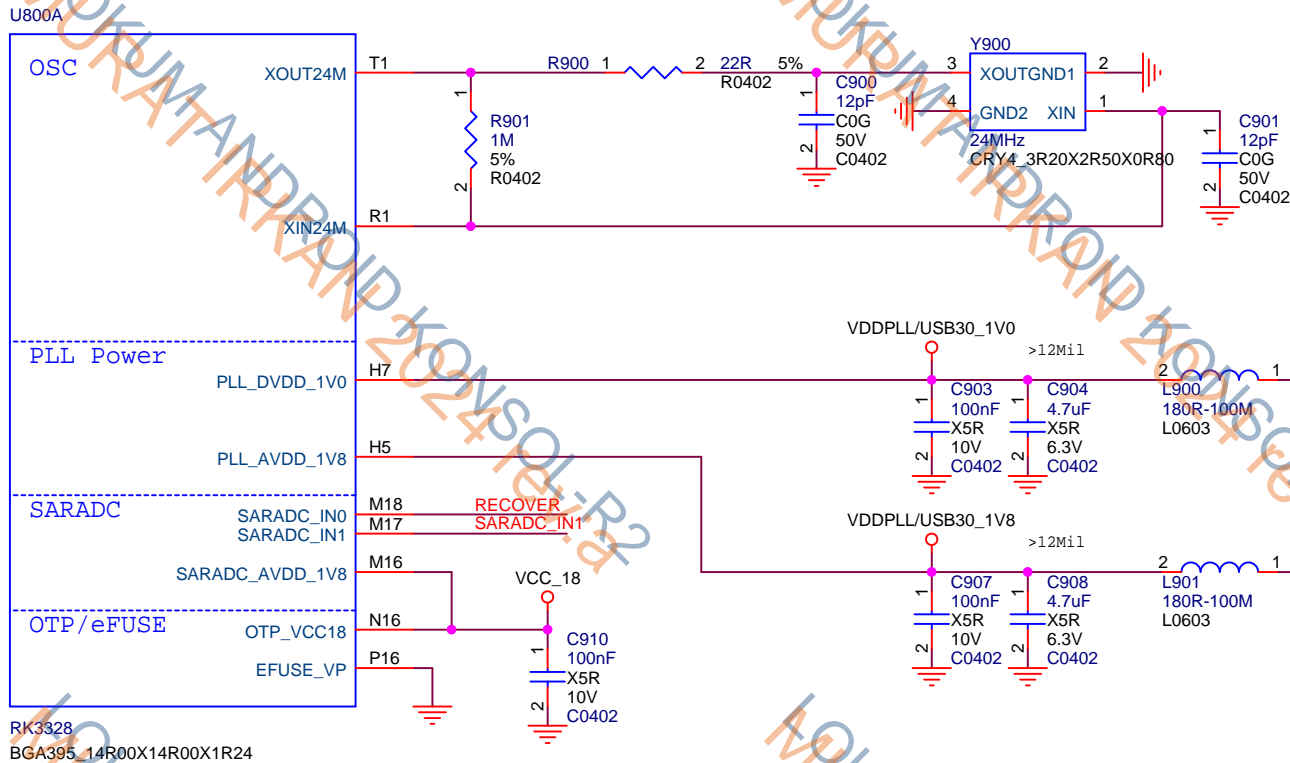
RK3328

BGA395_14R00X14R00X1R24

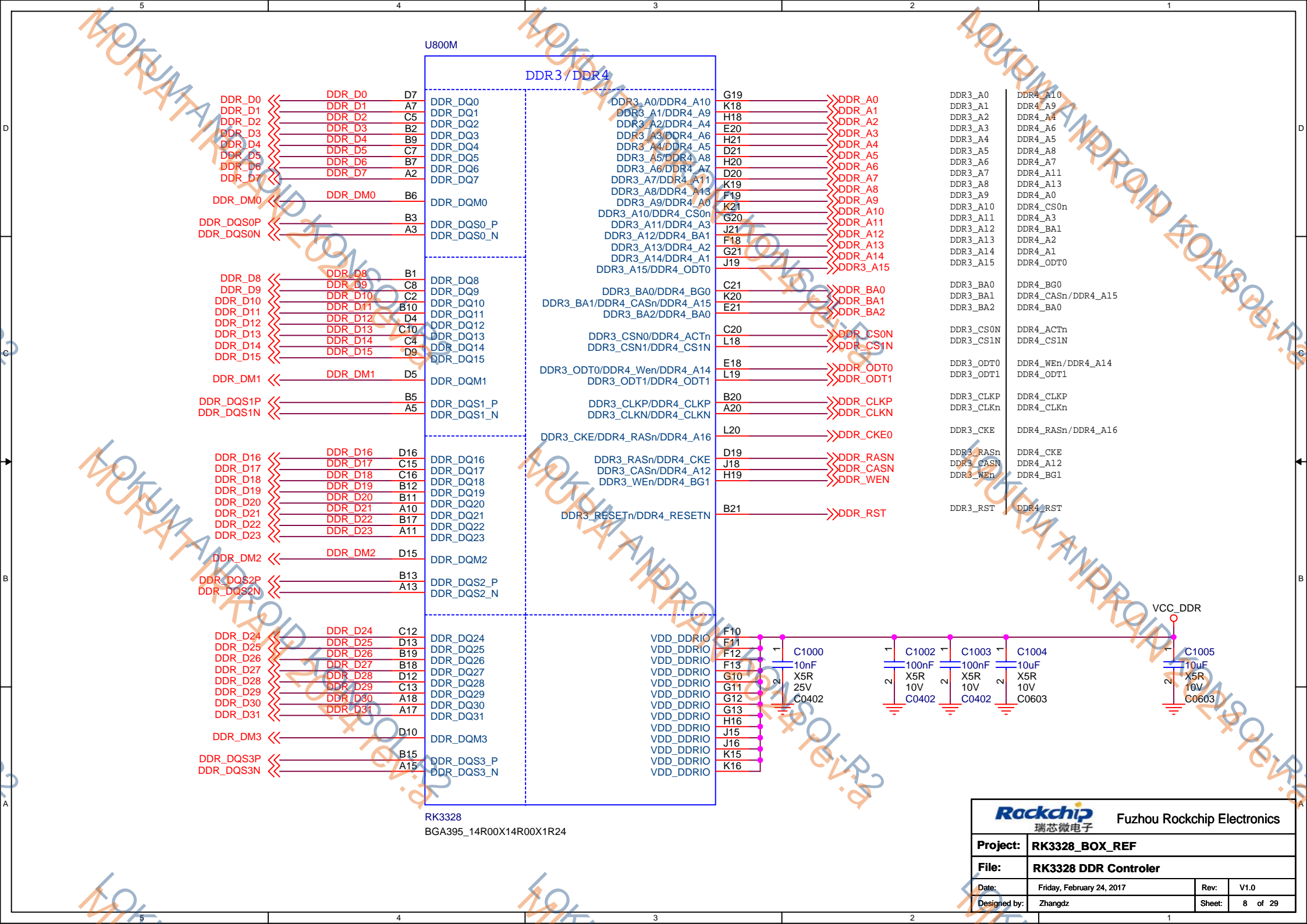


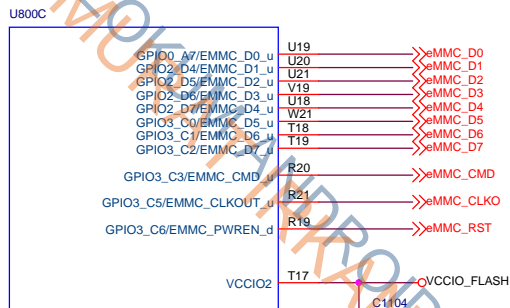
Fuzhou Rockchip Electronics

Project: RK3328_BOX_REF	
File: RK3328 Power	
Date: Tuesday, March 07, 2017	Rev: V1.0
Designed by: Zhangdz	Sheet: 6 of 29

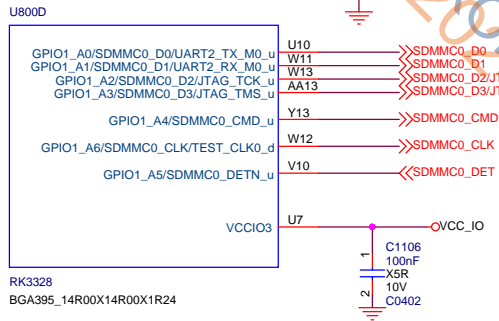


SARADC_IN0 BOM Ver...	SARADC_IN1 PCB Ver...	Pull up	Pull down
Recover		DNP	10K
BOM1		110K	10K
BOM2		100K	20K
BOM3		100K	33K
BOM4		36K	18K
BOM5		51K	36K
BOM6		51K	51K
BOM7		36K	51K
BOM8		18K	36K
BOM9		33K	100K
BOM10		20K	100K
BOM11		10K	110K
BOM12		10K	DNP

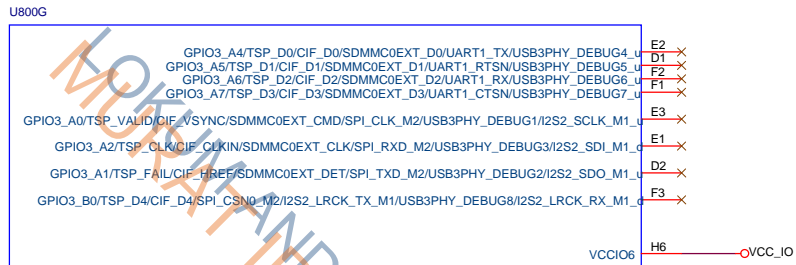




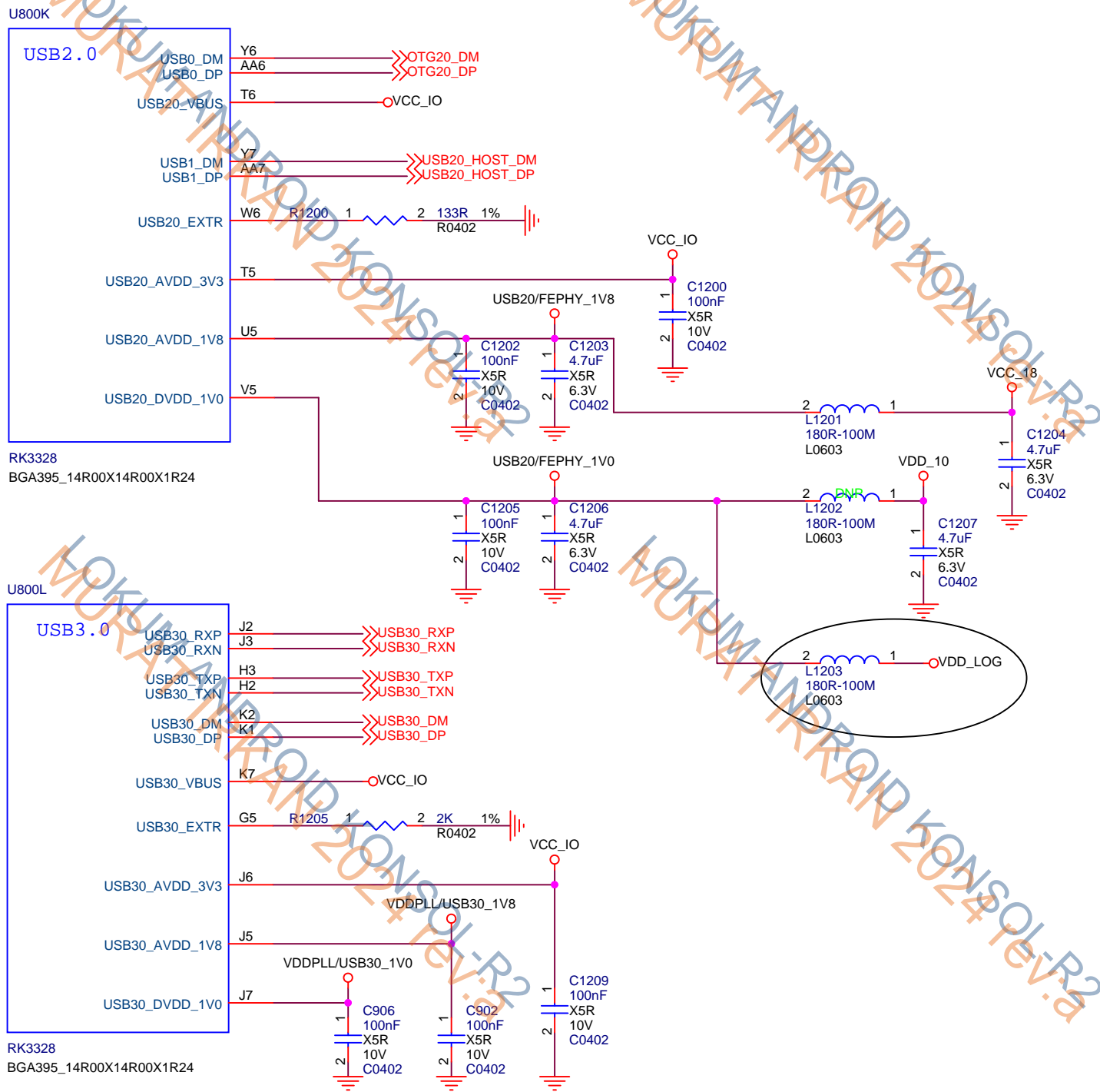
RK3328
BGA395_14R00X14R00X1R24



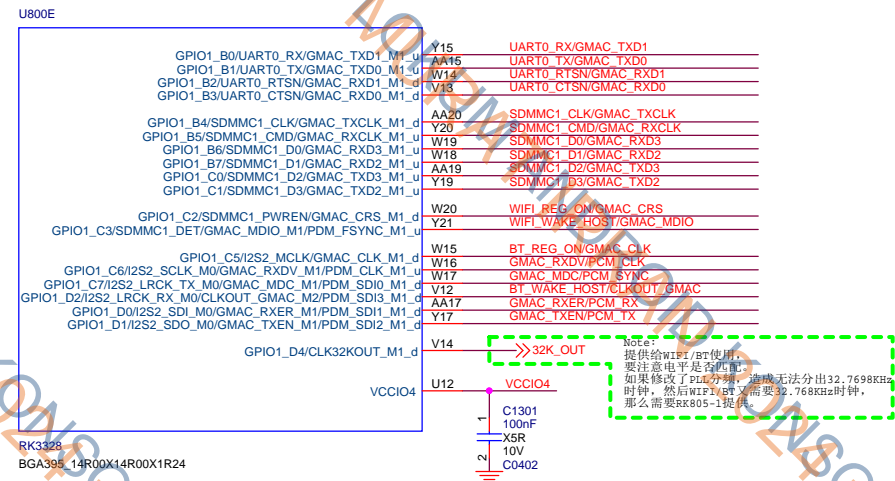
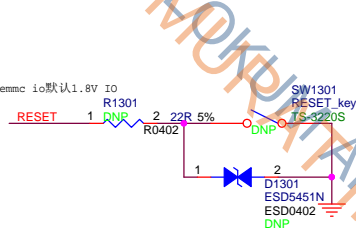
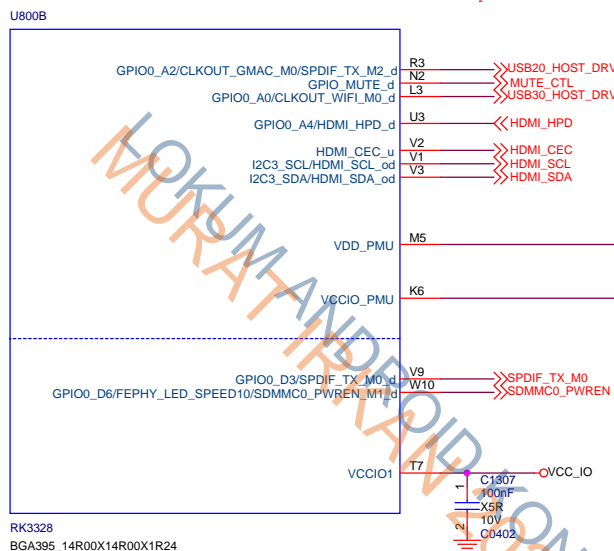
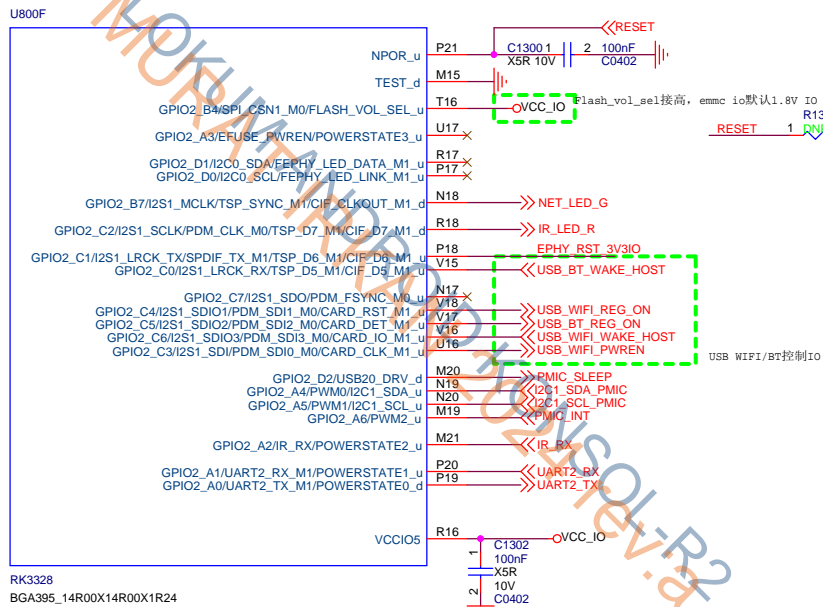
RK3328
BGA395_14R00X14R00X1R24



RK3328
BGA395_14R00X14R00X1R24



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Friday, February 24, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	10 of 29



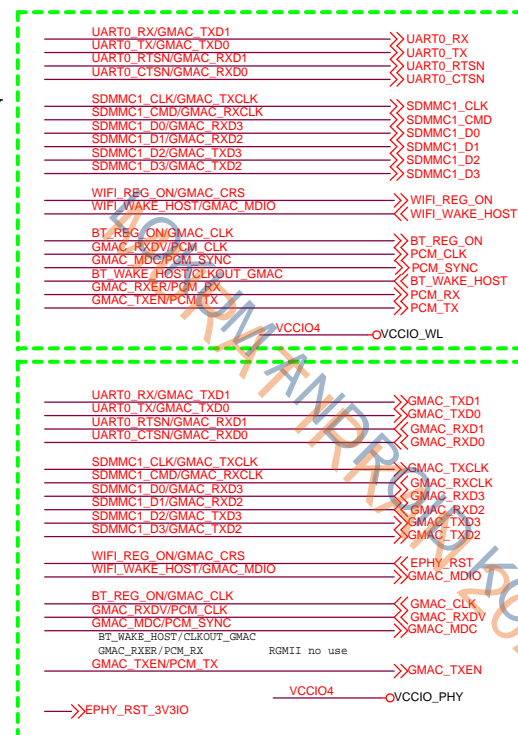
Note:
以太网配置选择和WIFI,BT配置选择

1: 只需100M以太网时, 使用内置的100M PHY
WIFI,BT可以选择
SDMMC1 WIFI和UART0 BT
或SDMMC1 WIFI和USB BT
或SDMMCOEXT WIFI和USB BT
或USB WIFI和USB BT。

2: 需要1000M以太网时, 需外接1000M PHY
WIFI,BT可以选择
USB WIFI和USB BT。
或SDMMCOEXT WIFI和USB BT
这个配置下, 可以支持双网口,
内置的100M以太网也可以同时用。

3: 需双100M以太网时,
一个用内置的100M PHY
另一个用外置的100M PHY (接GMAC IO上)
WIFI,BT可以选择
SDMMC1 WIFI和UART1 BT
或SDMMC1 WIFI和USB BT
或SDMMCOEXT WIFI和USB BT
或USB WIFI和USB BT。

Note:
SDIO1+UART0和GMAC的IO是复用的。
二选一



U800I

HDMI2.0 out

HDMI_TXCLKN
HDMI_TXCLKP

HDMI_TX0N
HDMI_TX0P

HDMI_TX1N
HDMI_TX1P

HDMI_TX2N
HDMI_TX2P

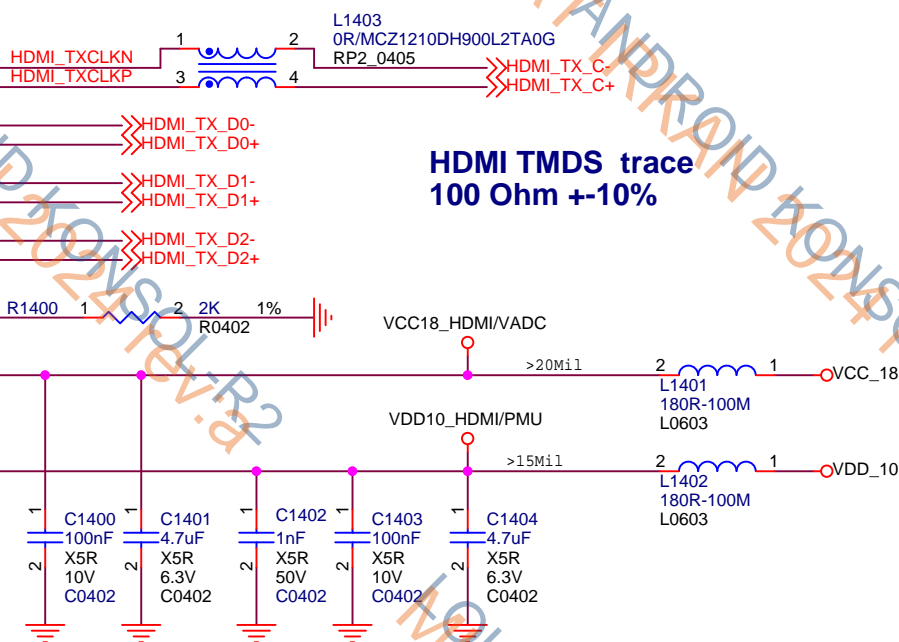
HDMI_EXTR

HDMI_AVDD_1V8

HDMI_AVDD_1V0

RK3328

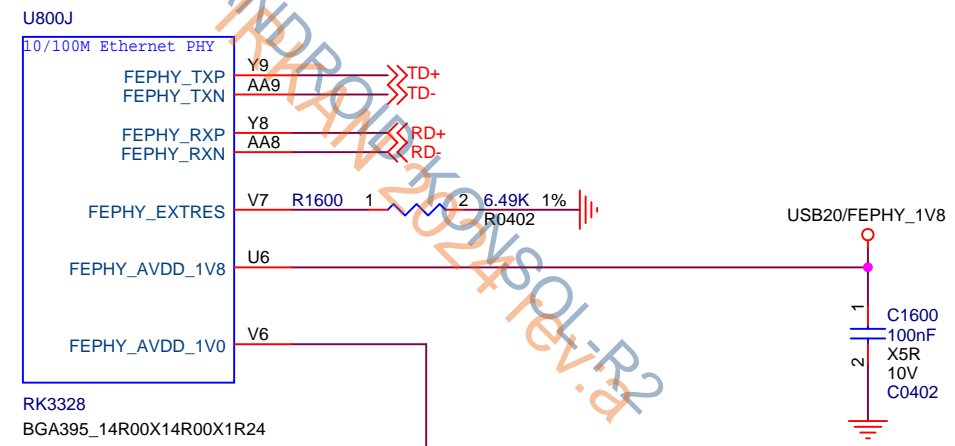
BGA395_14R00X14R00X1R24



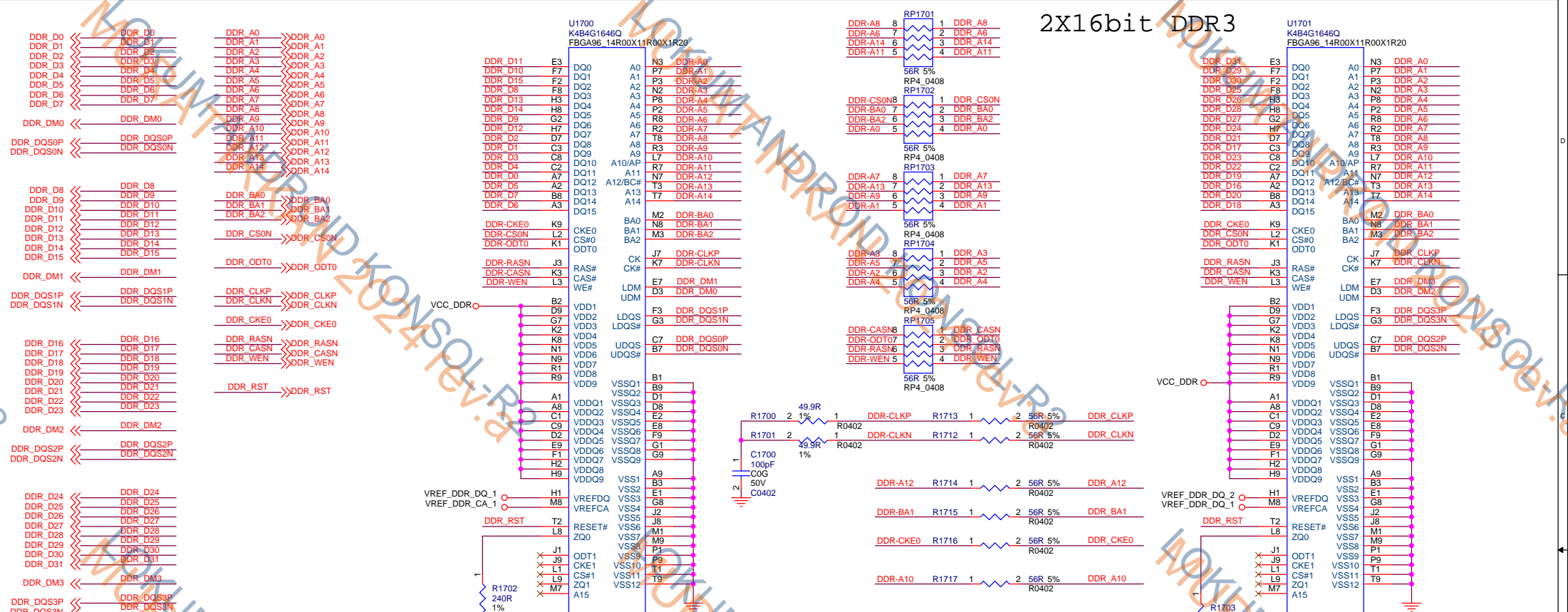
瑞芯微电子

Fuzhou Rockchip Electronics

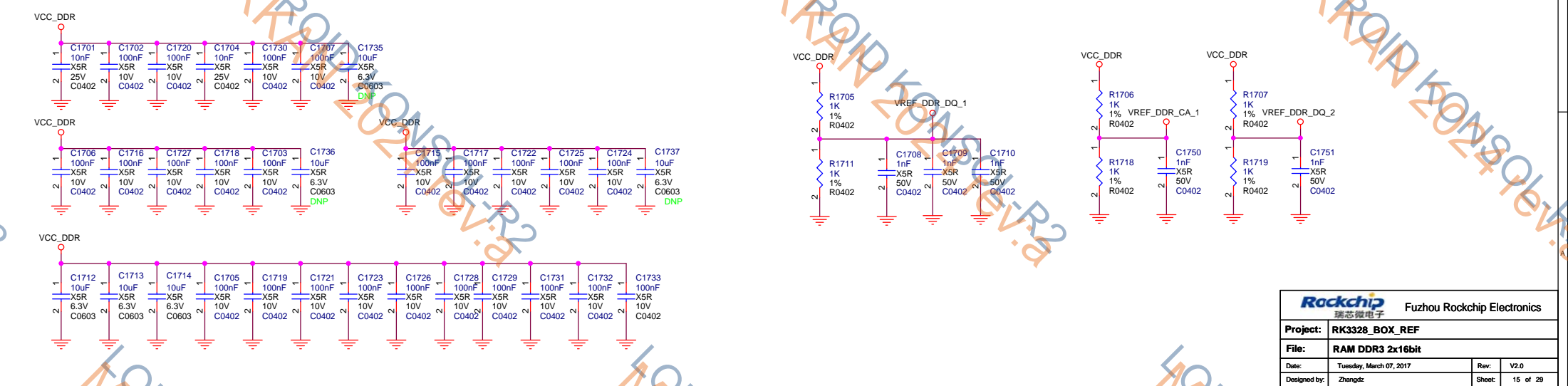
Project:	RK3328_BOX_REF		
File:	RK3328 HDMI PHY		
Date:	Friday, February 24, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	12 of 29



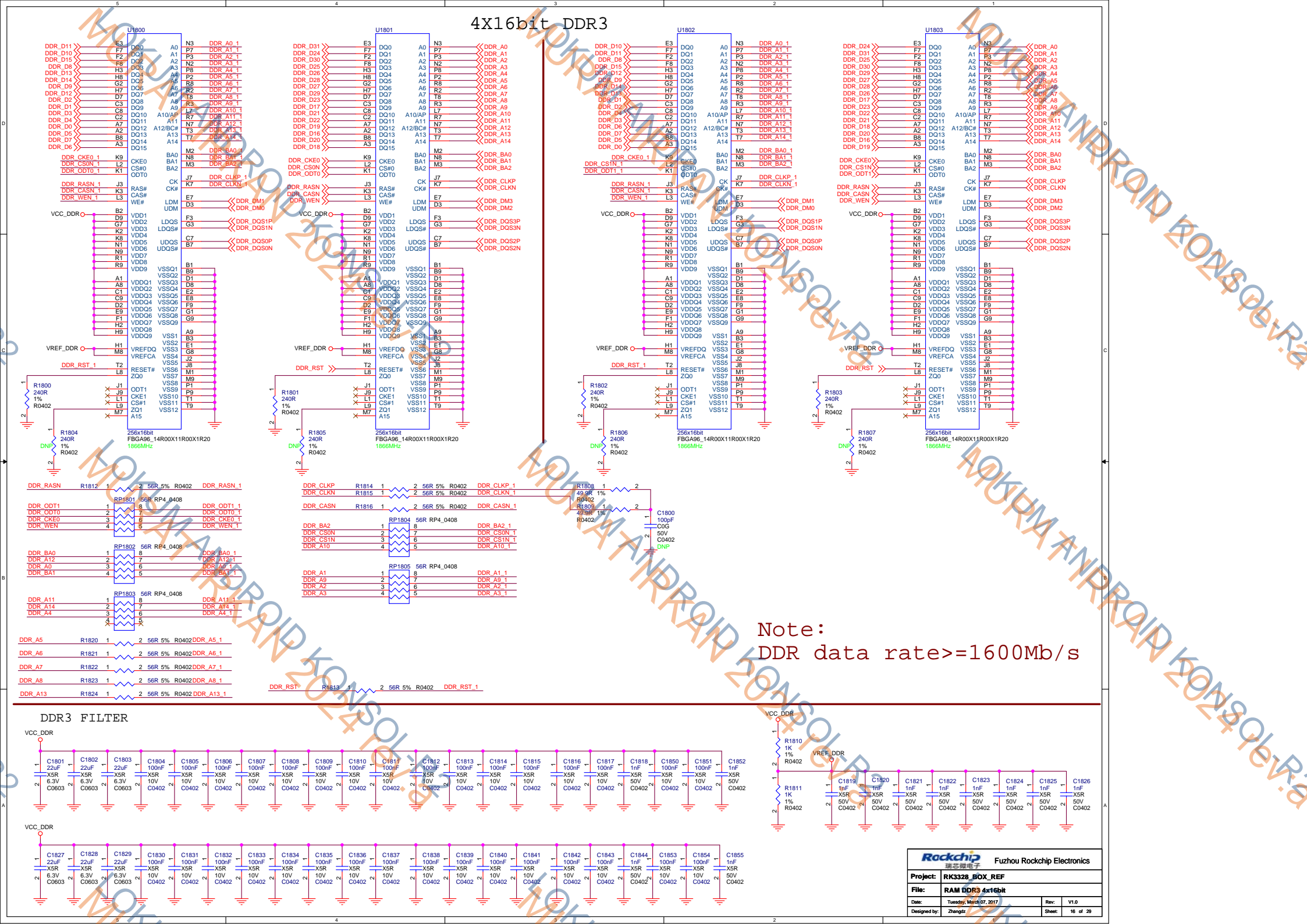
Embed FEPHY



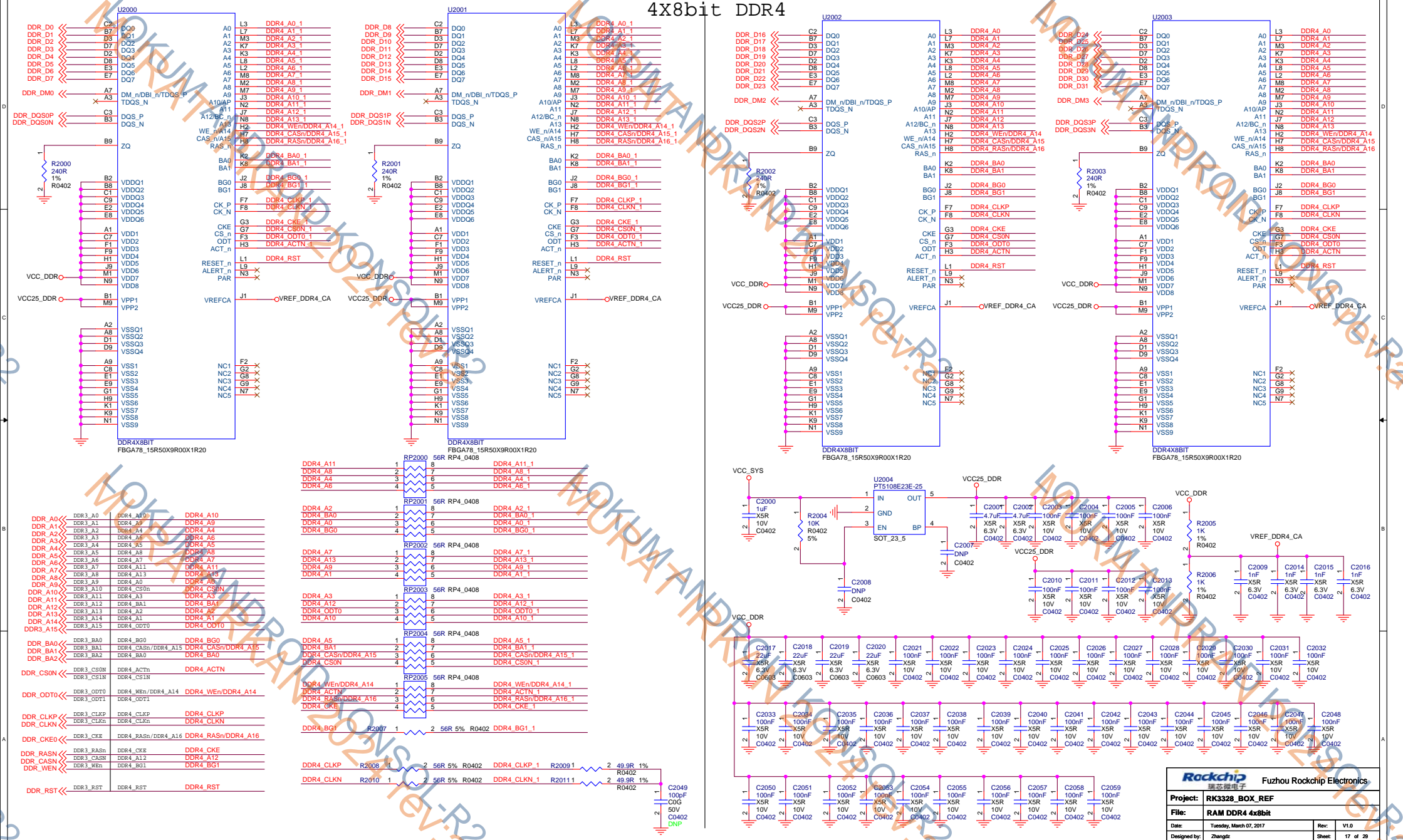
Note:
DDR data rate>=1600Mb/s



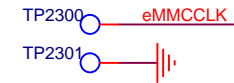
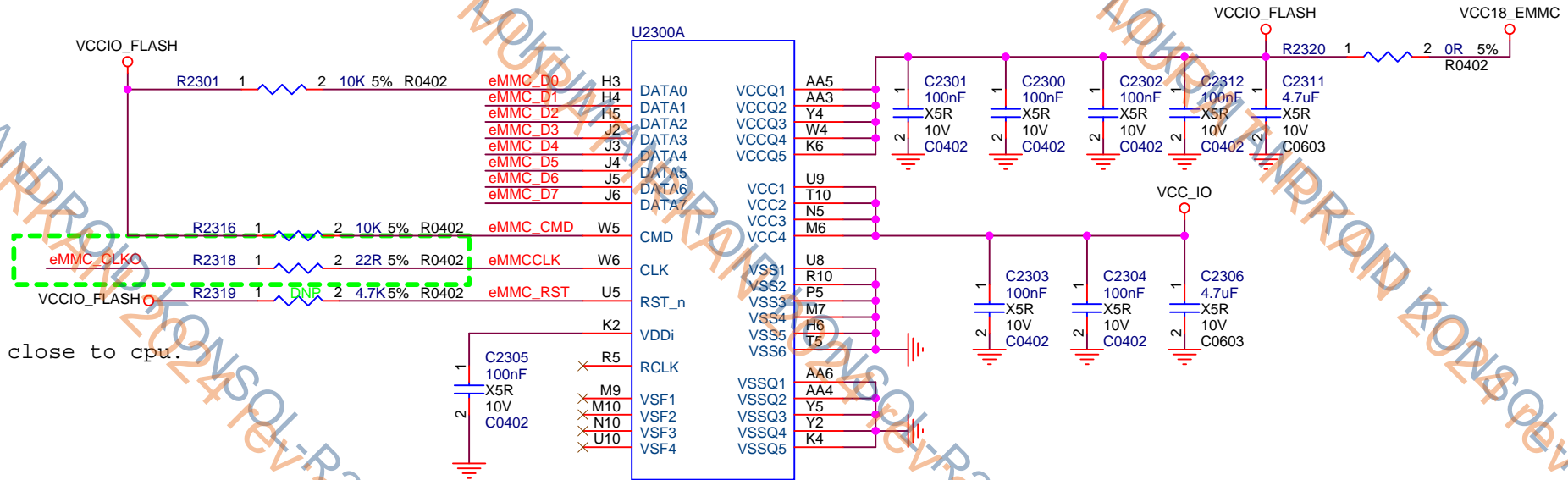
Note:
DDR data rate $\geq 1600\text{Mb/s}$



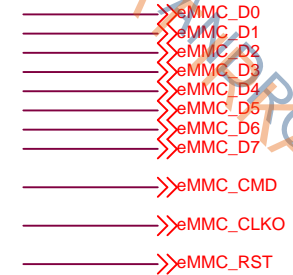
4x8bit DDR4




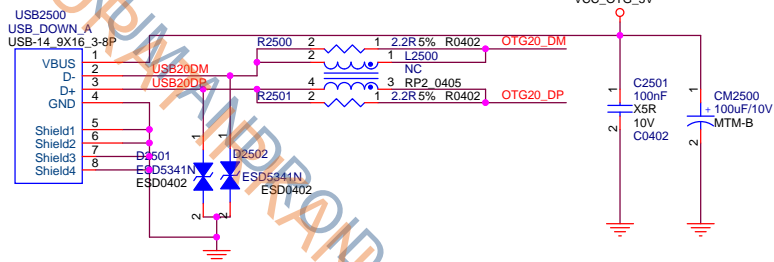
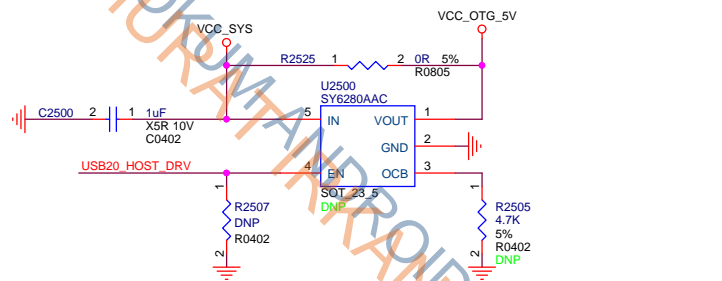
Note:
The 22ohm Res. close to cpu.



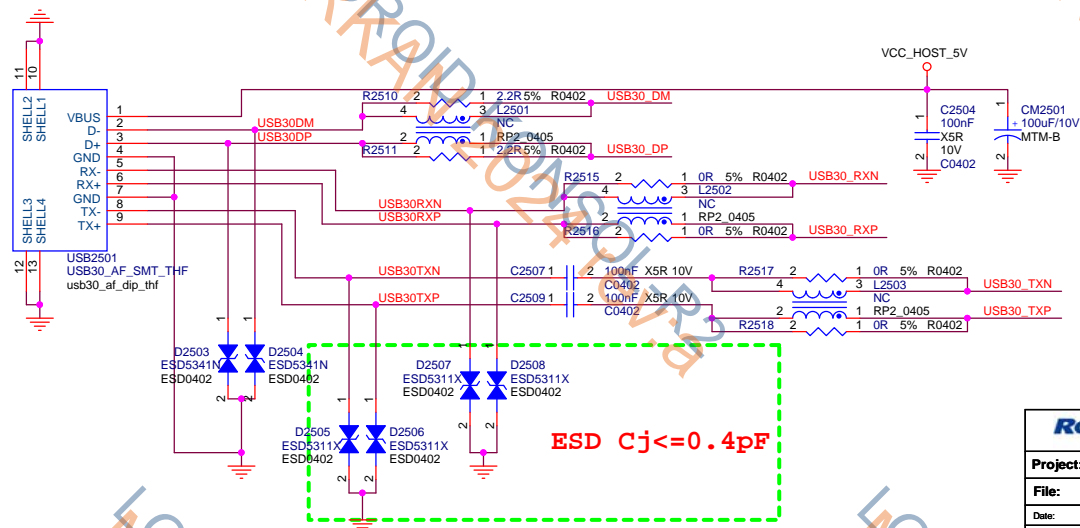
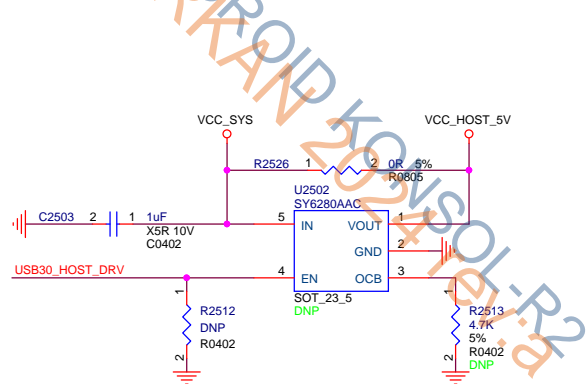
Note:
eMMC Update.



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	Flash-eMMC		
Date:	Tuesday, March 07, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	19 of 29



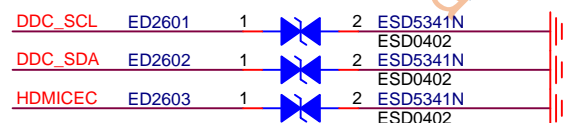
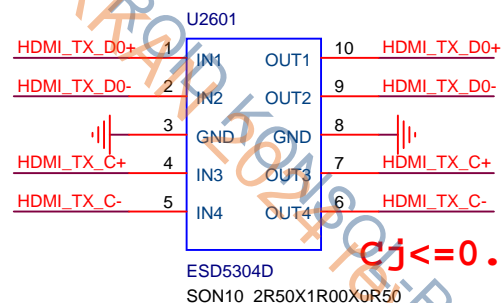
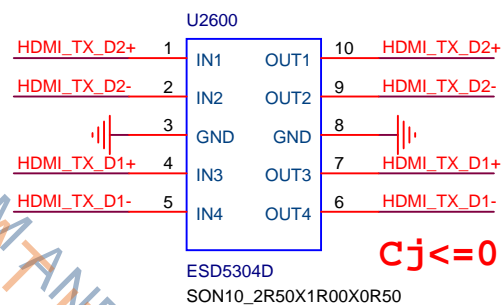
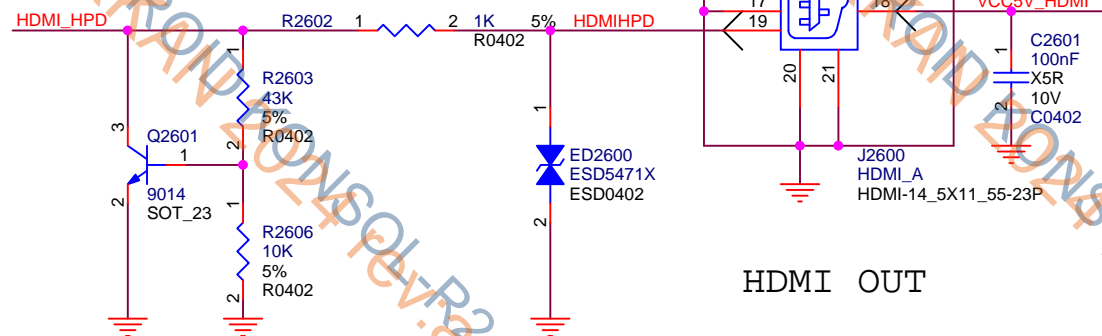
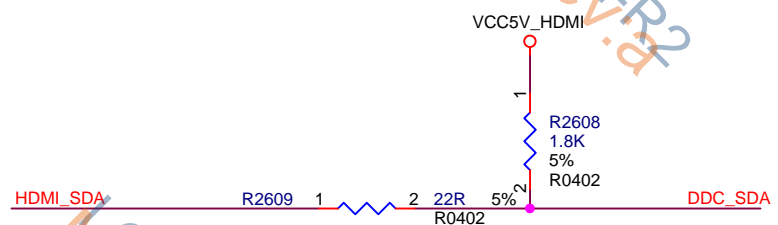
>>>OTG20_DM
 >>>OTG20_DP
 >>>USB20_HOST_DRV

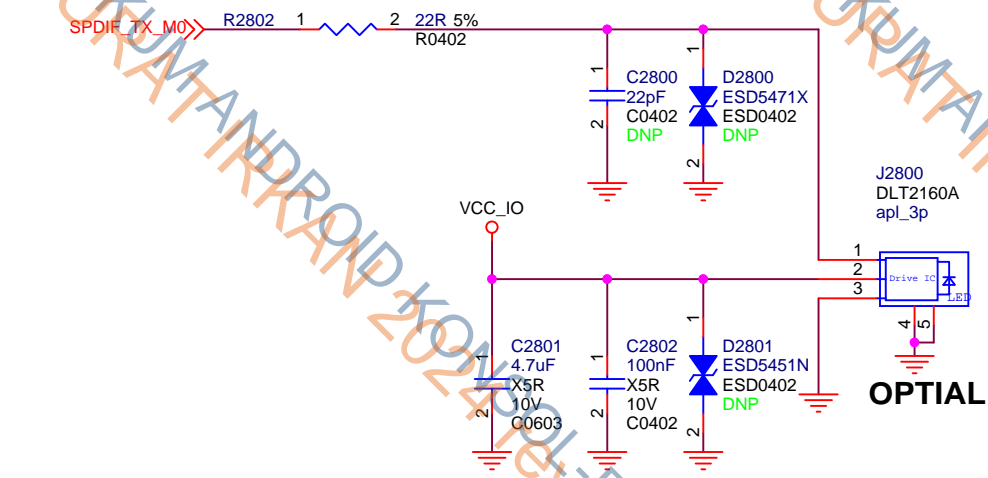


>>>USB30_RXP
 >>>USB30_RXN
 >>>USB30_TXP
 >>>USB30_TXN
 >>>USB30_DM
 >>>USB30_DP
 >>>USB30_HOST_DRV

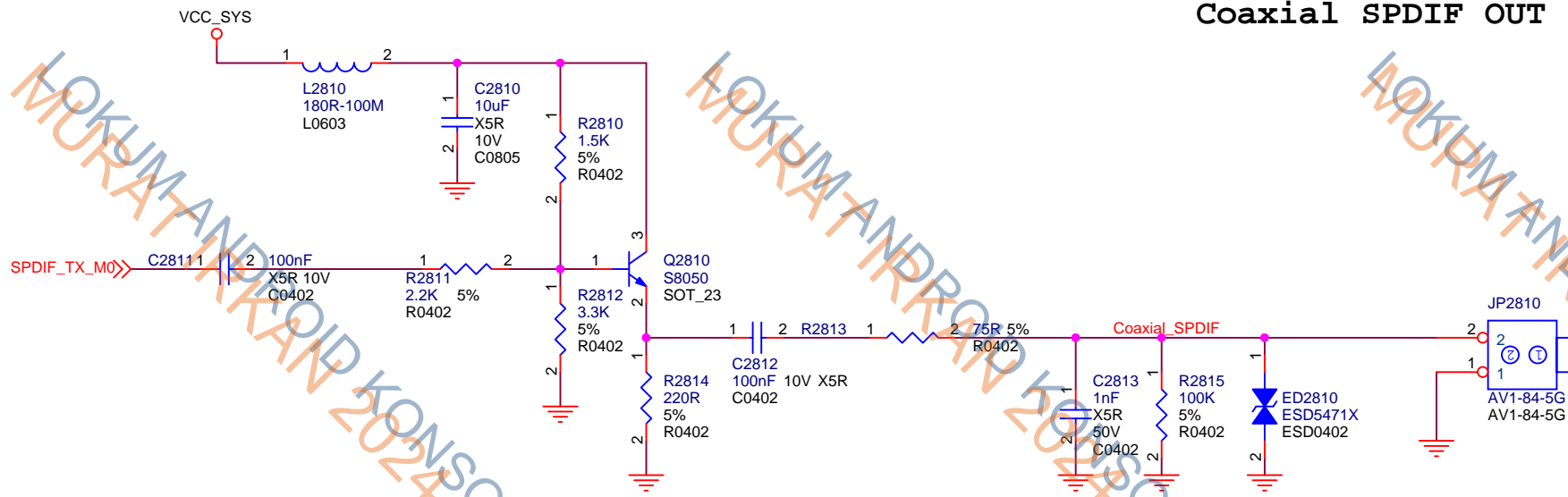
ESD Cj<=0.4pF

 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	USB Port		
Date:	Tuesday, March 07, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	20 of 29






Optical SPDIF OUT



Coaxial SPDIF OUT

 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	S/PDIF Port		
Date:	Friday, February 24, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	22 of 29

VDAC_OUT

VCC_IO
D2900
BAT54S
SOT_23

CVBS_OUT

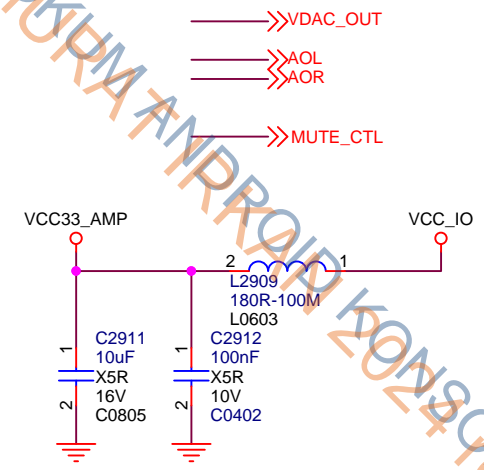
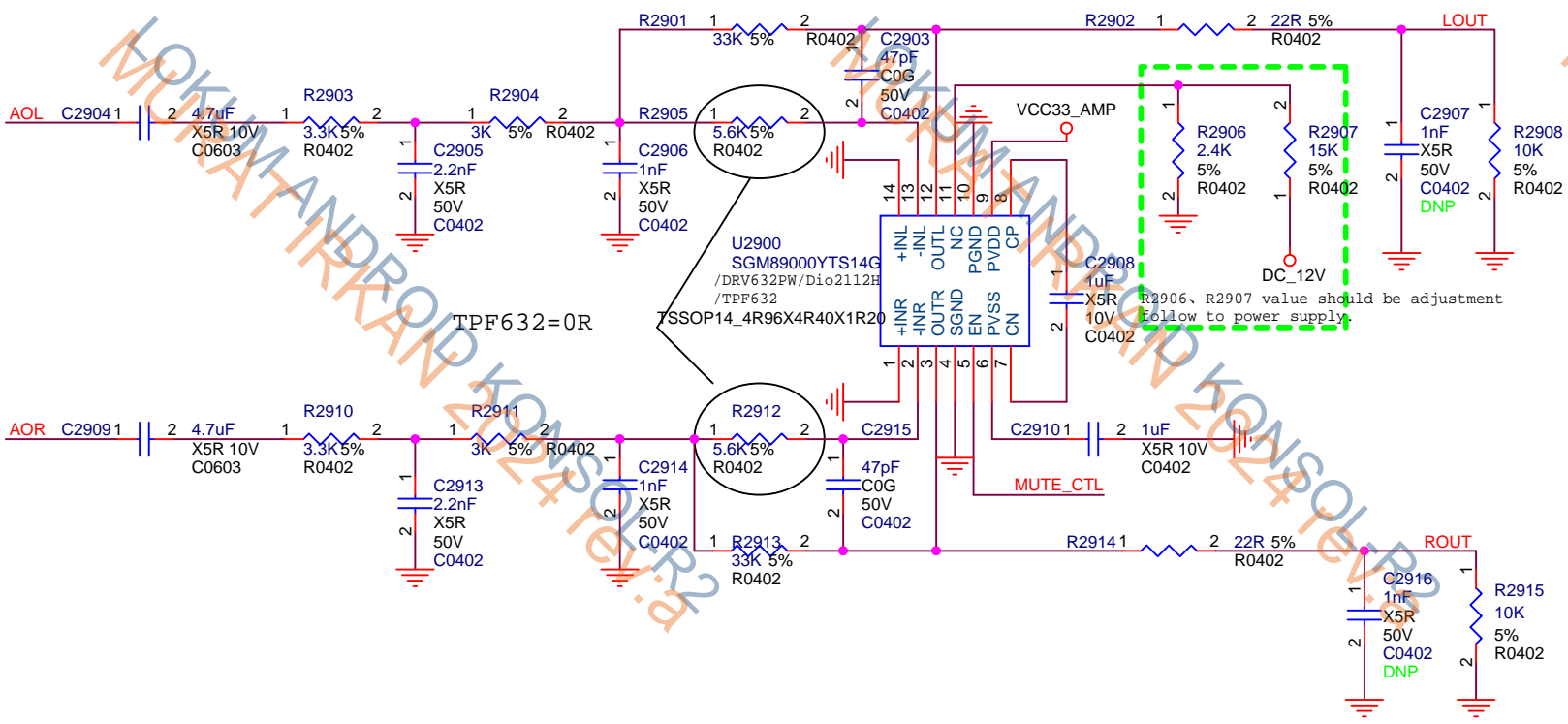
CVBS_OUT

ROUT
LOUT


J2900
SMT-PJ
PJ-320D-5_SMTa

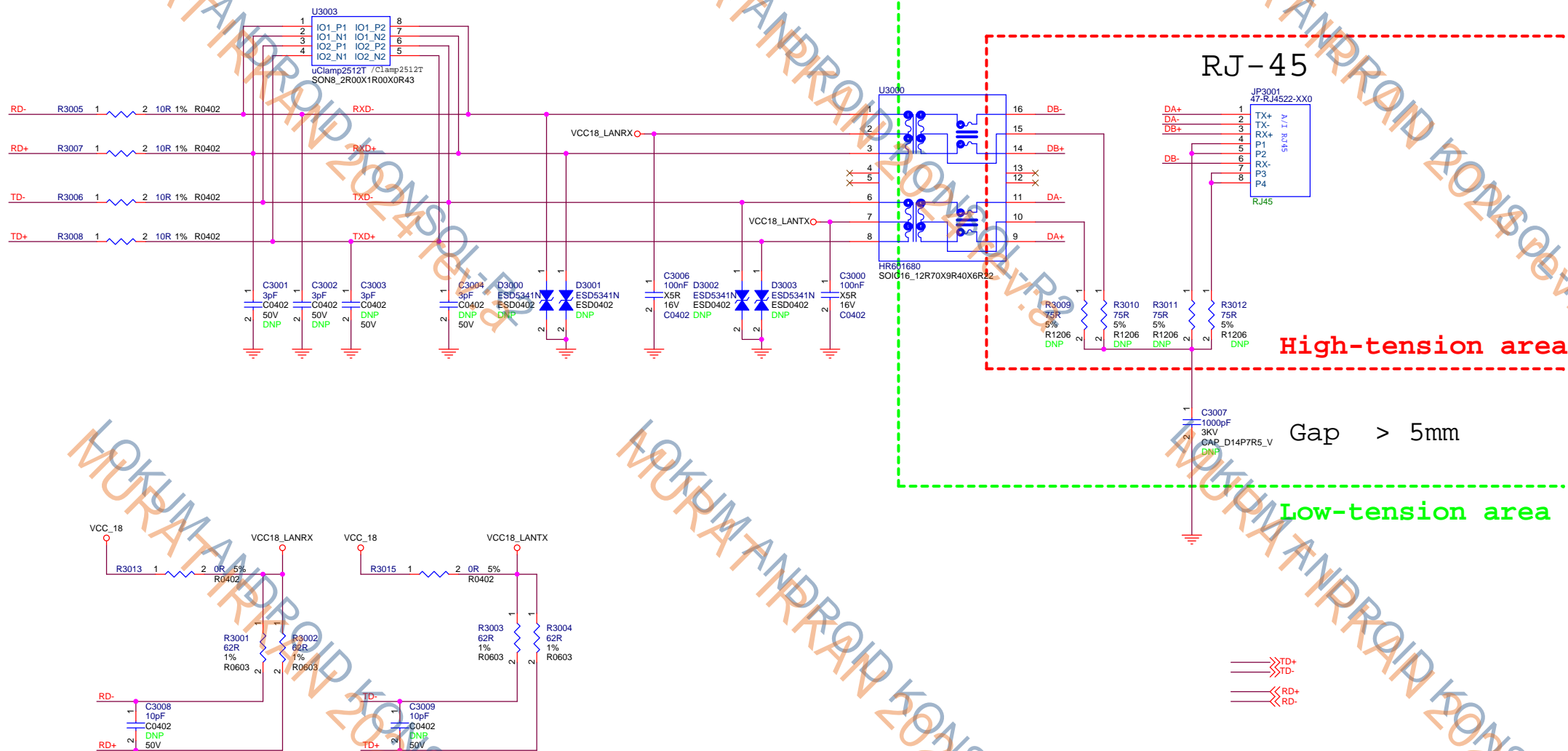
D2901 DNP
ESD5451N
ESD0402
D2902 DNP
ESD5451N
ESD0402
D2903 DNP
ESD5451N
ESD0402

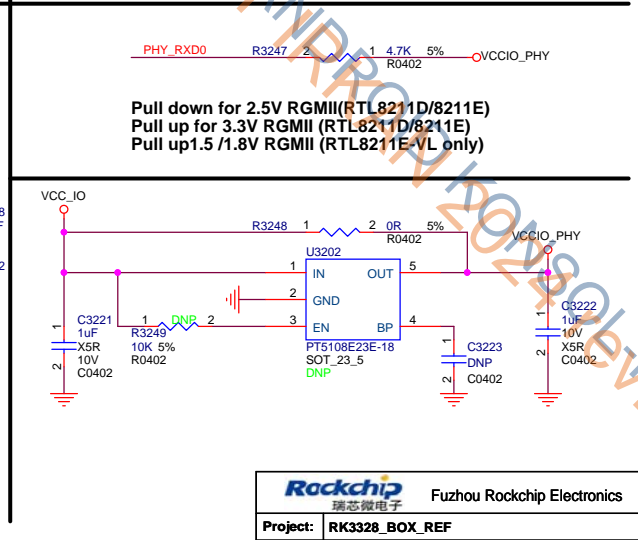
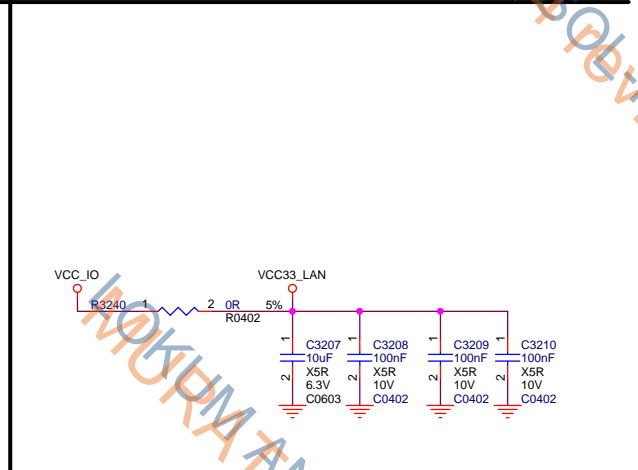
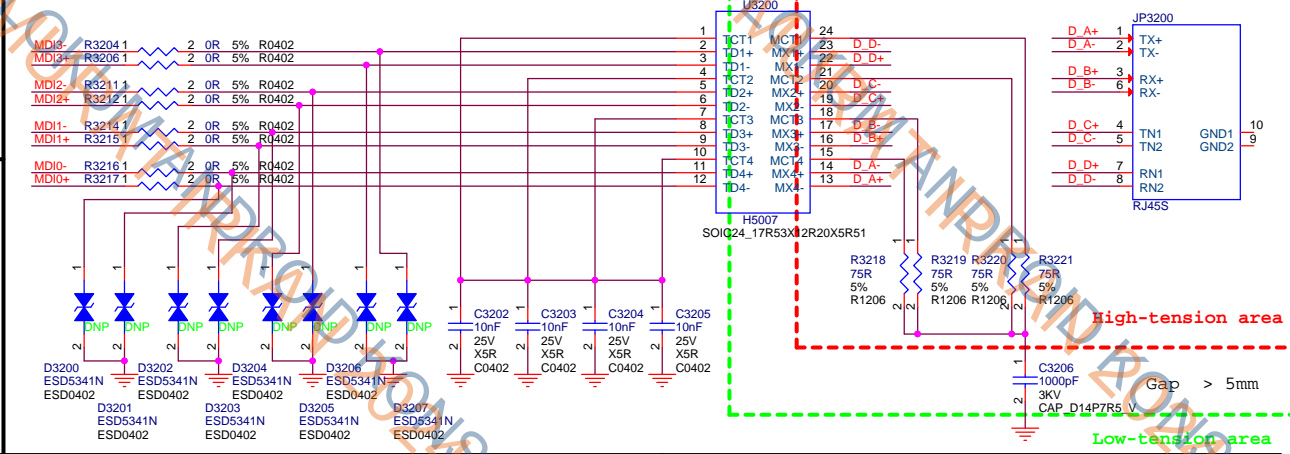
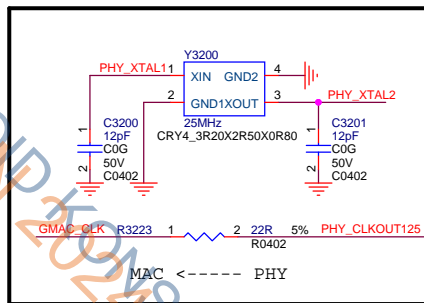
AV OUT



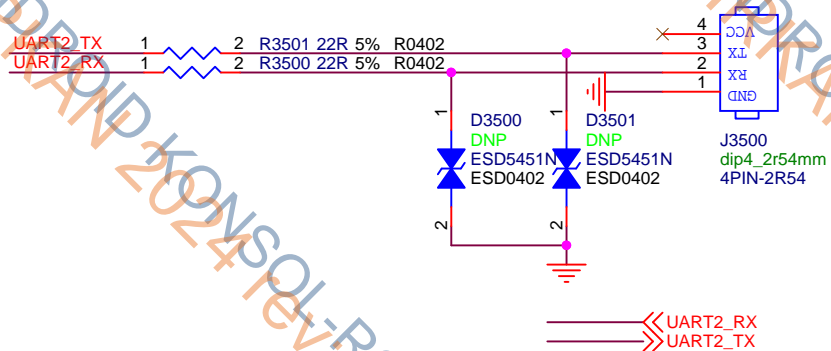
2-Vrms Audio Line Driver

 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	AV OUT Port		
Date:	Tuesday, March 07, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	23 of 29



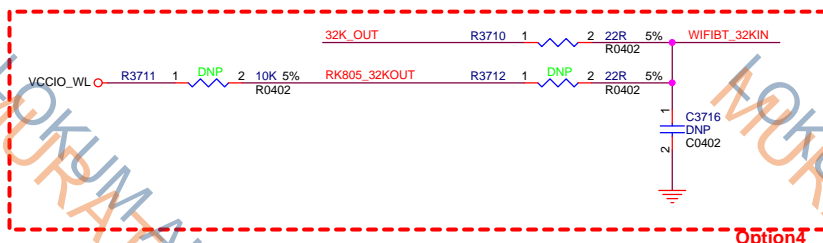
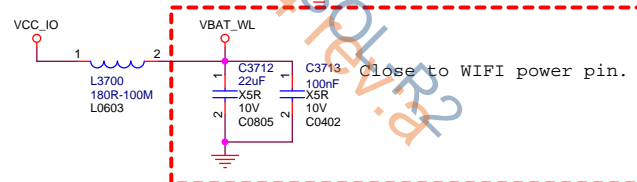
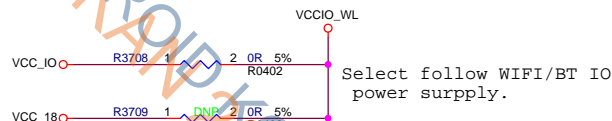
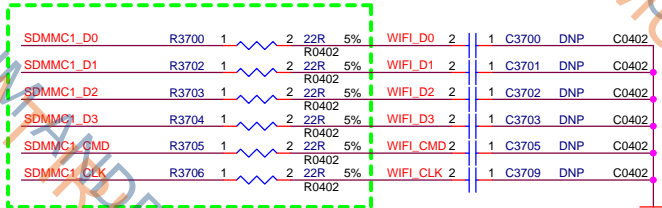


Debug UART2

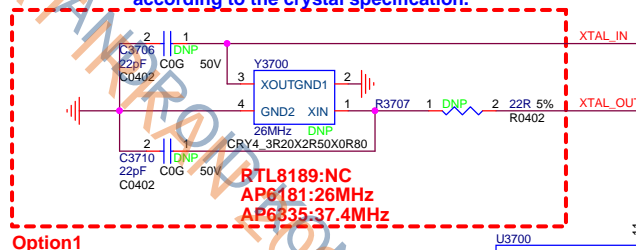


 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_REF		
File:	Debug UART2/JTAG		
Date:	Friday, February 24, 2017	Rev:	V1.0
Designed by:	<designer>	Sheet:	26 of 29

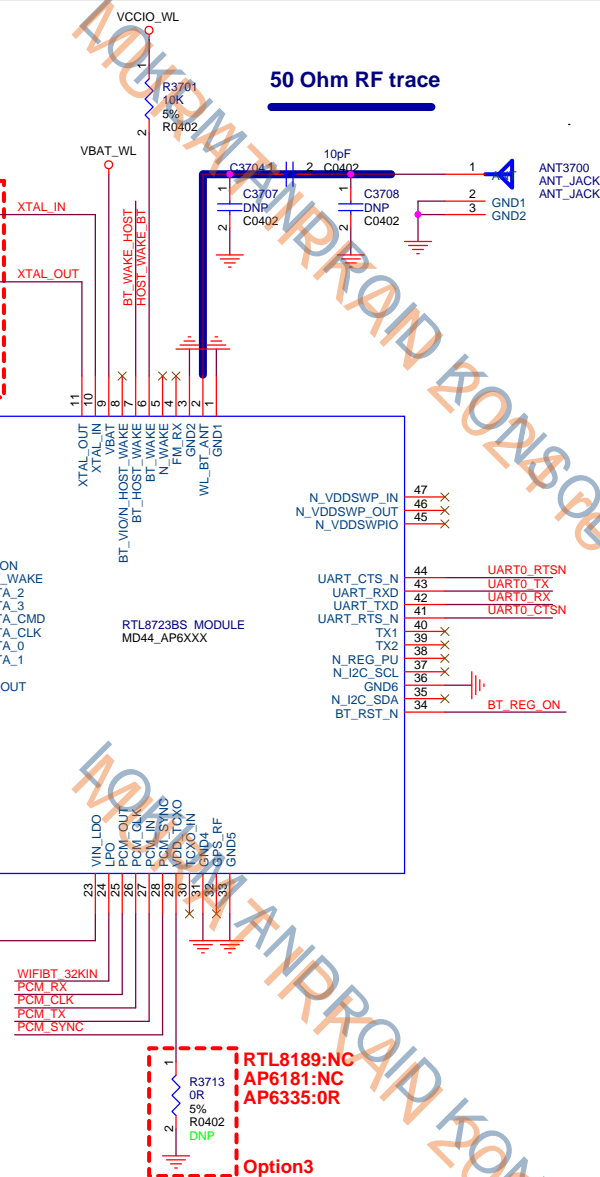
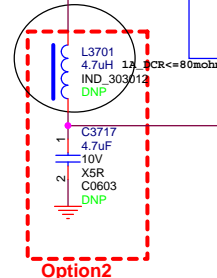
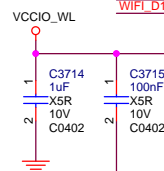
请靠近CPU放置。



Note:
Adjusted the load capacitance
according to the crystal specification.



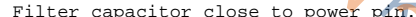
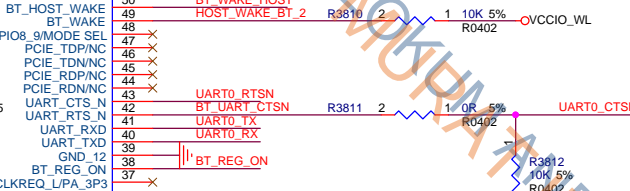
WIFI REG_ON
WIFI WAKE_HOST
WIFI D2
WIFI D3
WIFI CMD
WIFI CLK
WIFI D0
WIFI D1



1X1 WIFI
AP6181/AP6212/AP6330/AP6335/RTL8189FTV
RTL8723BS/XZ3538/XZ3660

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181	No	Yes	No	No	No	26MHz	1.71-3.6V
AP6212	No	Yes	No	No	Yes	26MHz	1.71-3.6V
XZ3538	No	Yes	No	No	Yes	26MHz	1.71-3.6V
AP6330	Yes	Yes	No	Yes	Yes	26MHz	1.2-2.9V
XZ3660	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V
RTL8189FTV	No	Yes	No	No	No	40MHz On the module	3.3V
RTL8723BS	No	Yes	No	No	Yes		1.71-3.63V

OPTION	1	2	3	4	5
AP6181	Yes	Yes	No	Yes	
AP6212	Yes	Yes	No	Yes	
AP6330	Yes	Yes	No	Yes	
AP6335	Yes	Yes	Yes	Yes	
RTL8189FTV	No	No	No	No	
RTL8723BS	No	No	No	Yes	



OPTION	1	2	3		
AP6356S	Paste	Paste			
QCA6174	DNP	DNP			
RTL8822	DNP	DNP			
RTL8192	DNP	DNP			