CE Schematics For RK3568

BEIQI_CE_RK3568_LDDR4P_V1.0

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项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	00.Cover Page		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	0 of 99

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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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图纸:	01.Index and Notes		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-06	CZA	1:Revision preliminary version	

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项目：	BEIQI_CE_RK3568		
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图纸：	02.Revision History		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
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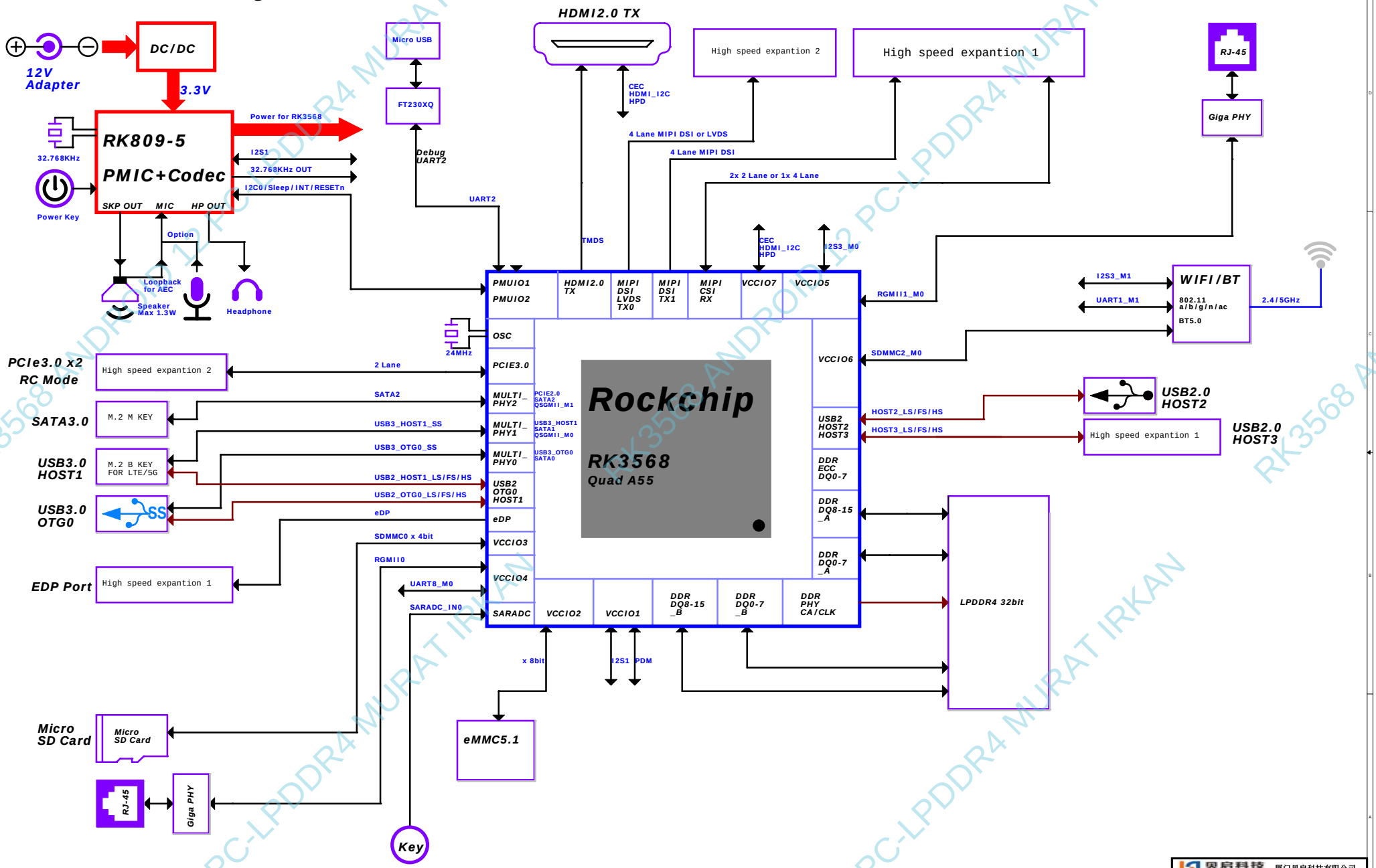
RK3568 Ref Block Diagram



项目：	BEIQI_CE_RK3568
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图纸：	03.Block Diagram
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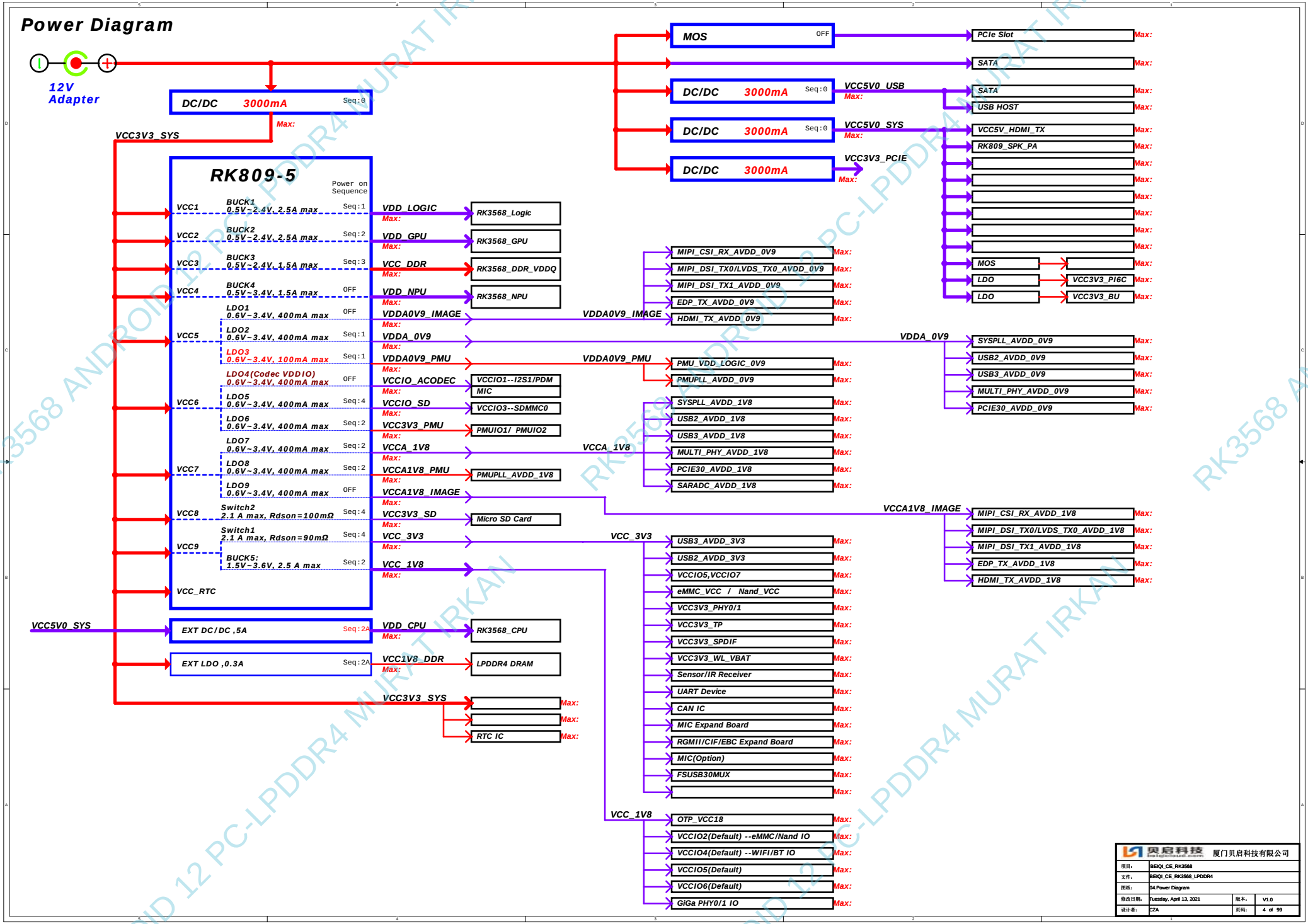
Power Diagram



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项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	04.Power Diagram		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
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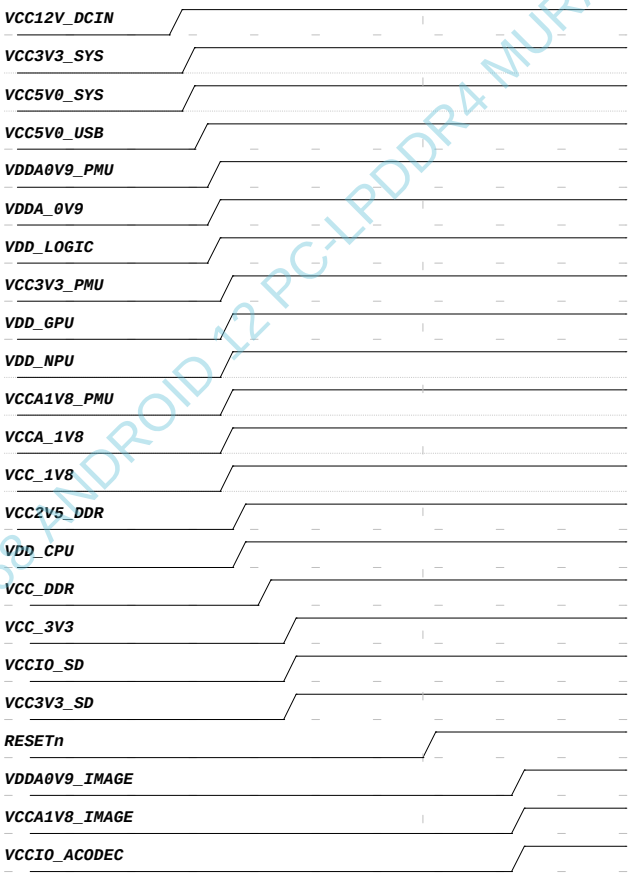
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

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项目：	BEIQI_CE_RK3568		
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图纸：	05.Power Sequence/IO Domain Map		
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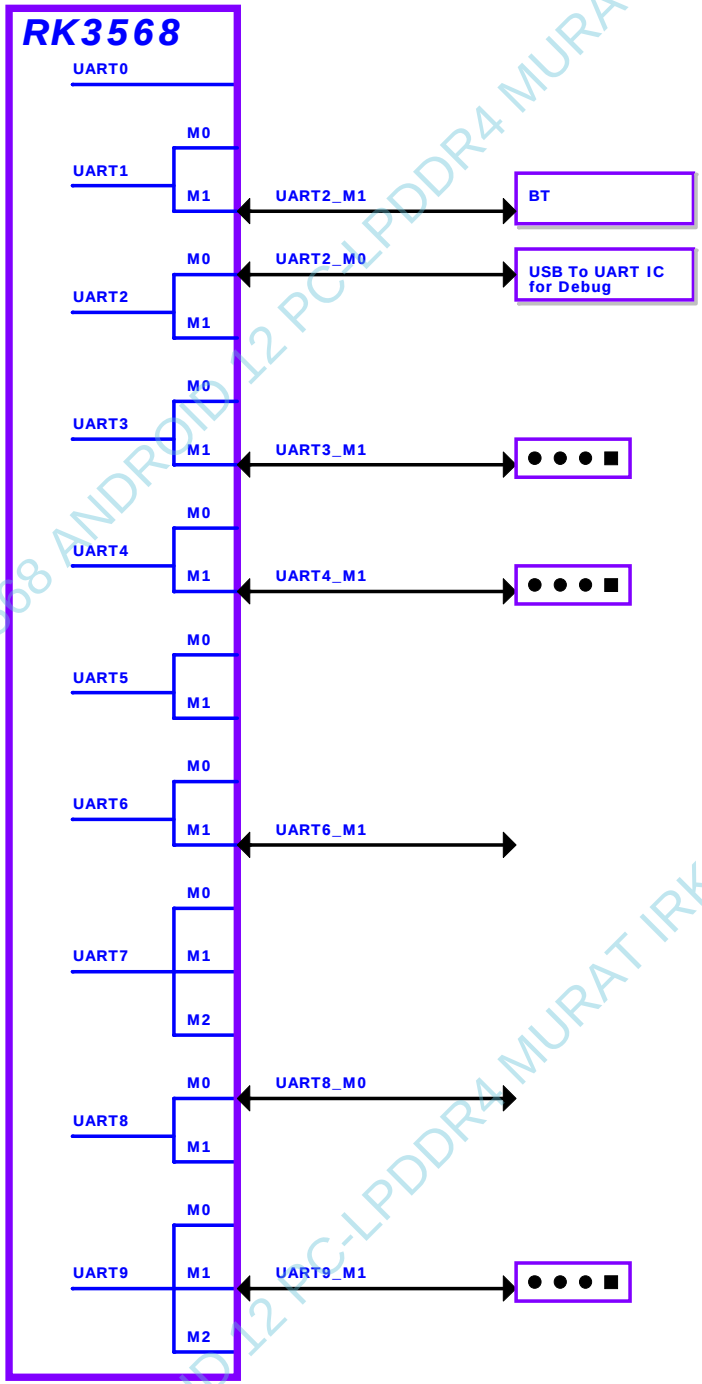
UART MAP



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项目：	BEIQI_CE_RK3568		
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图纸：	06.UART Map		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
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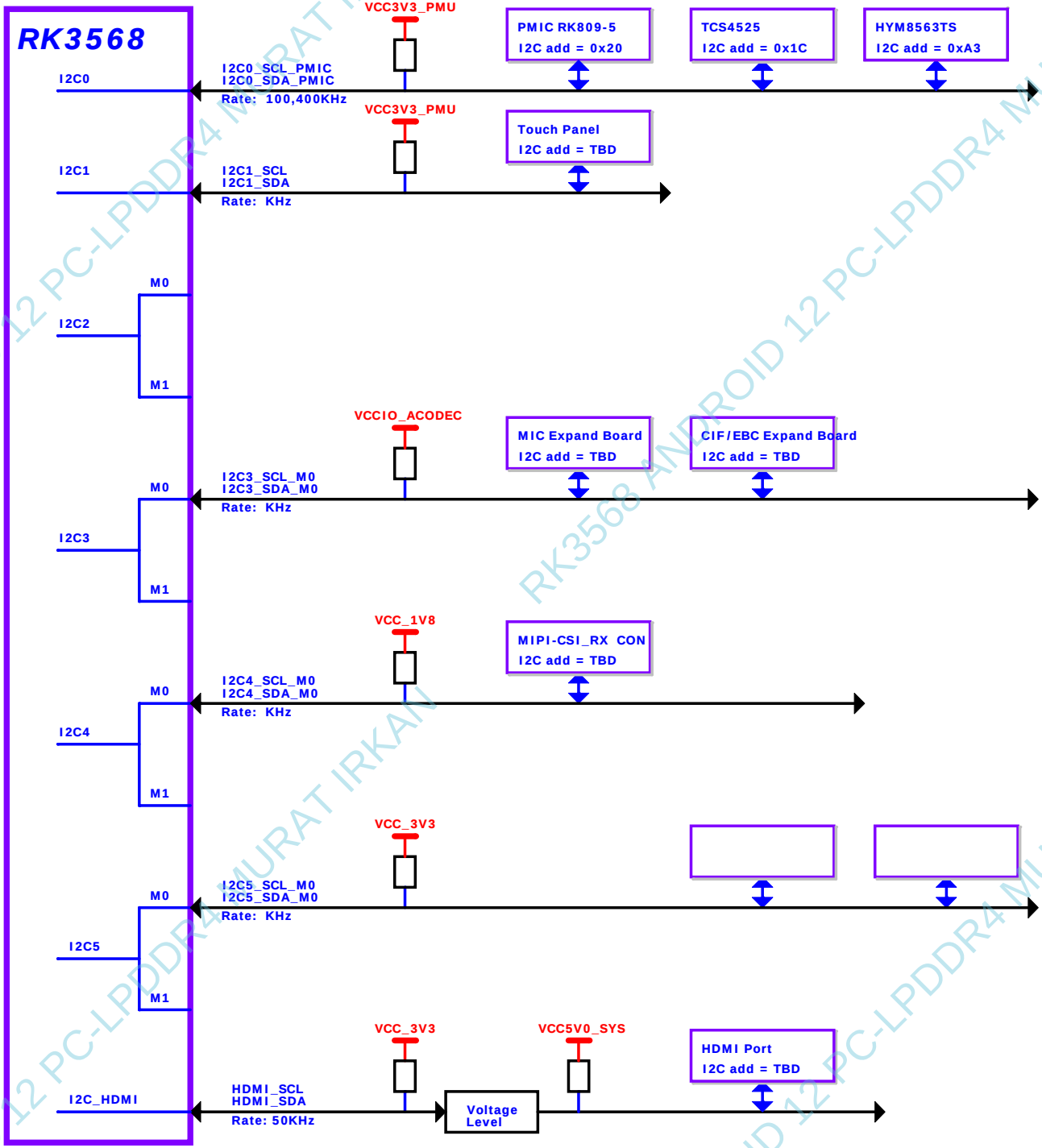
I2C MAP



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项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	07.I2C Bus Map		
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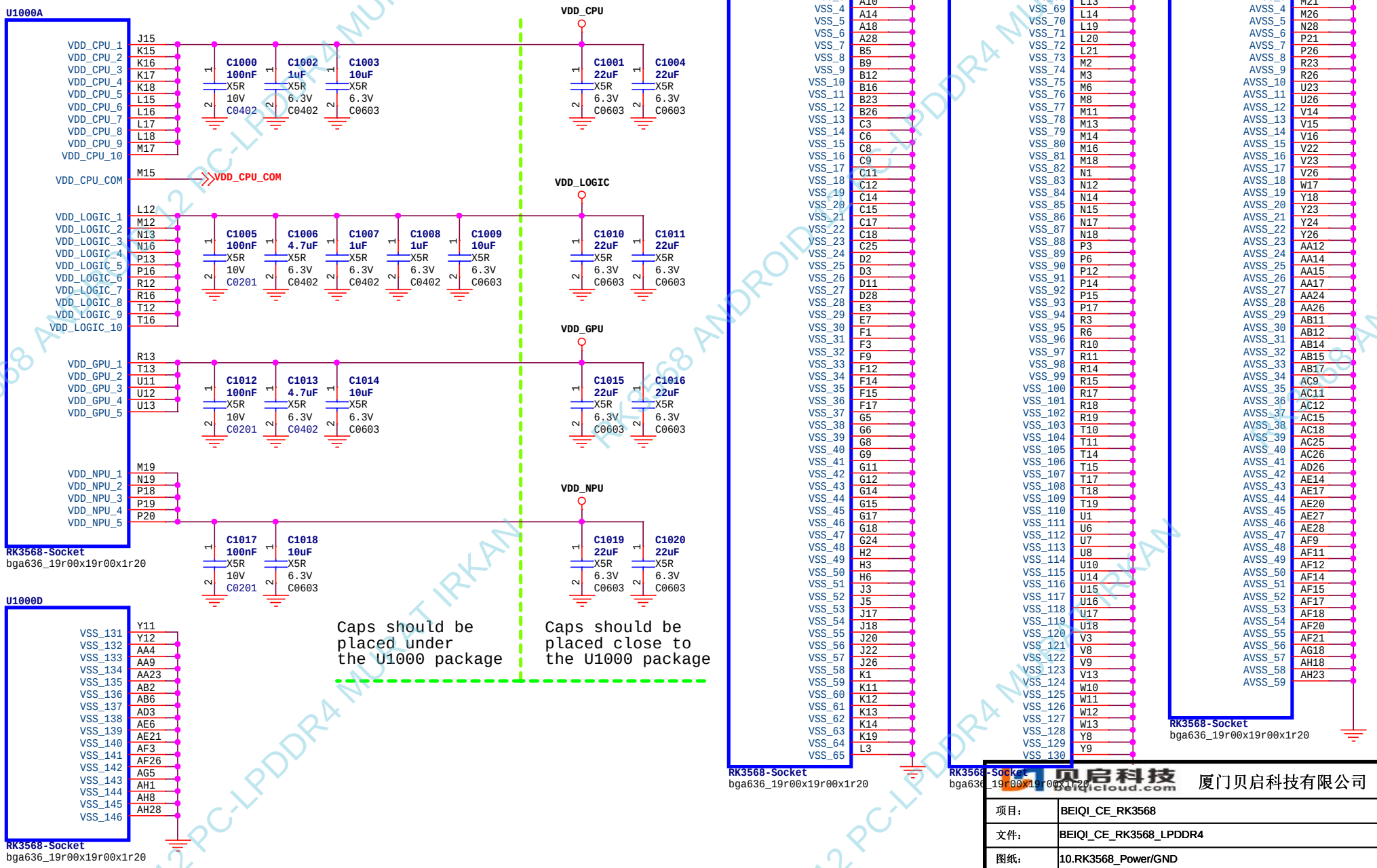
RK3568_ABCDE (Power&Gnd)



厦门贝启科技有限公司			
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	10.RK3568_Power/GND		
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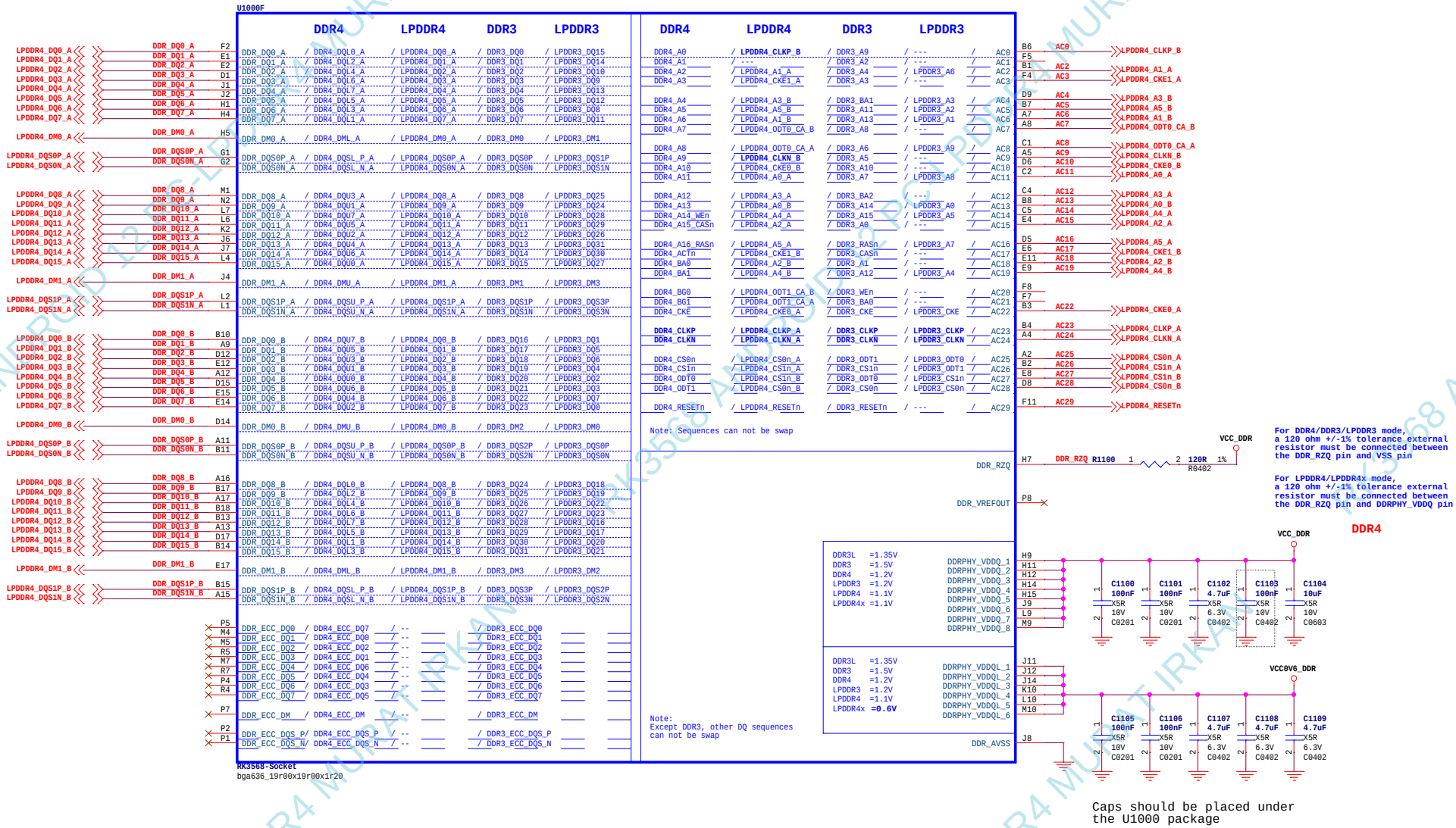
RK3568_F (DDR PHY)



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项目:	BEIQI_CE_RK3568		
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图纸:	11.RK3568_DDR PHY		
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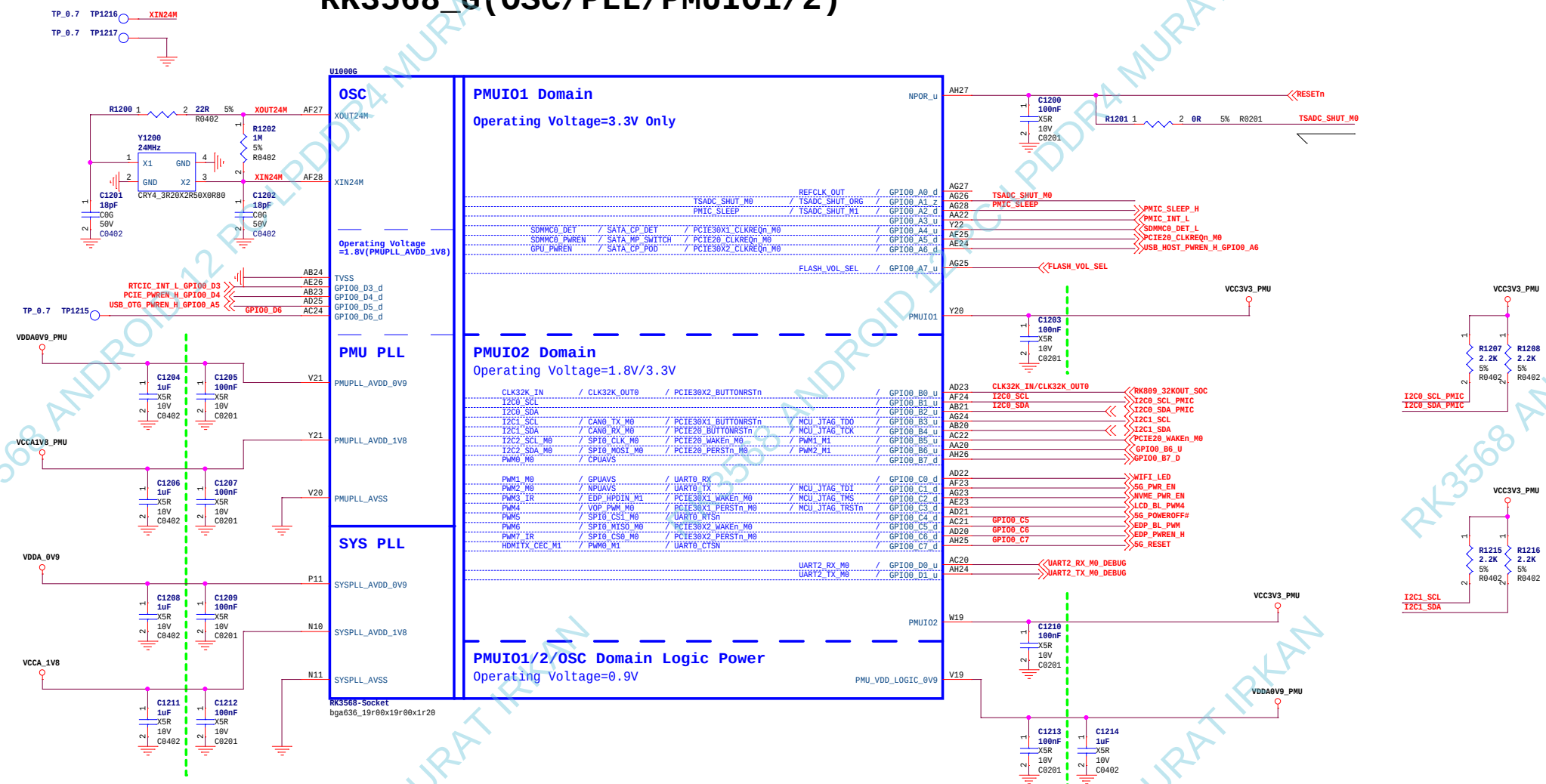
RK3568_G(OSC/PLL/PMUIO1/2)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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项目:	BEIQI_CE_RK3568		
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图纸:	12.RK3568_OSC/PLL/PMUIO		
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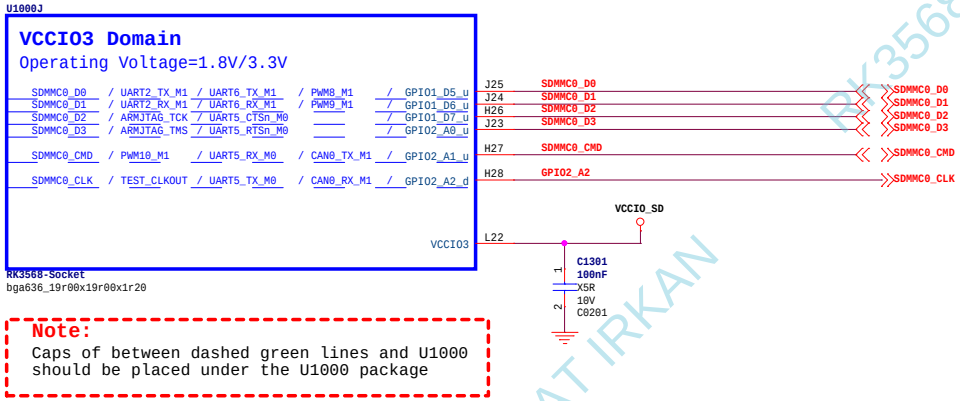
RK3568_I(VCCIO2 Domain)

RK3568_J(VCCIO3 Domain)



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项目：	BEIQI_CE_RK3568		
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图纸：	13.RK3568_Flash/SD Controller		
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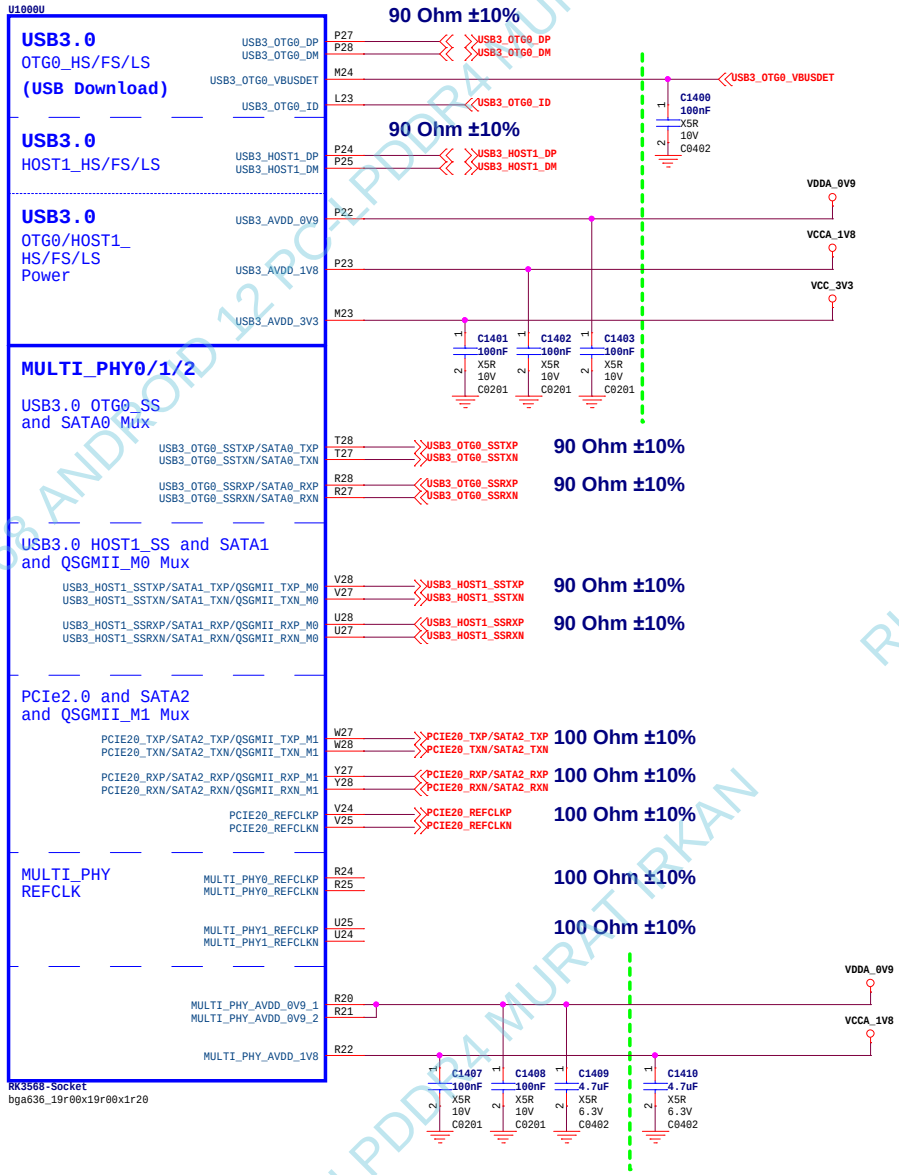
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



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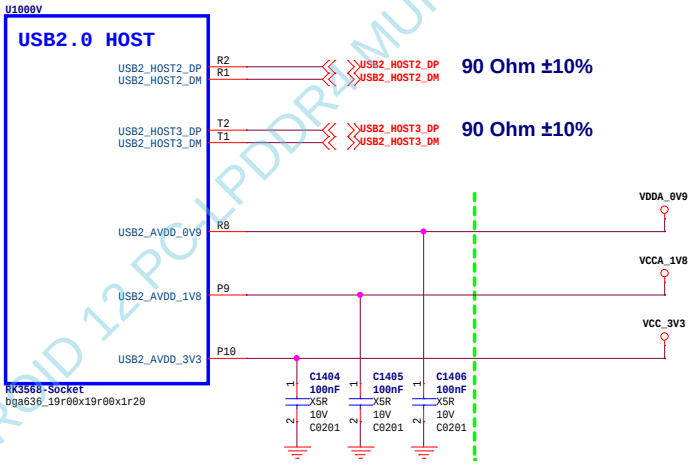
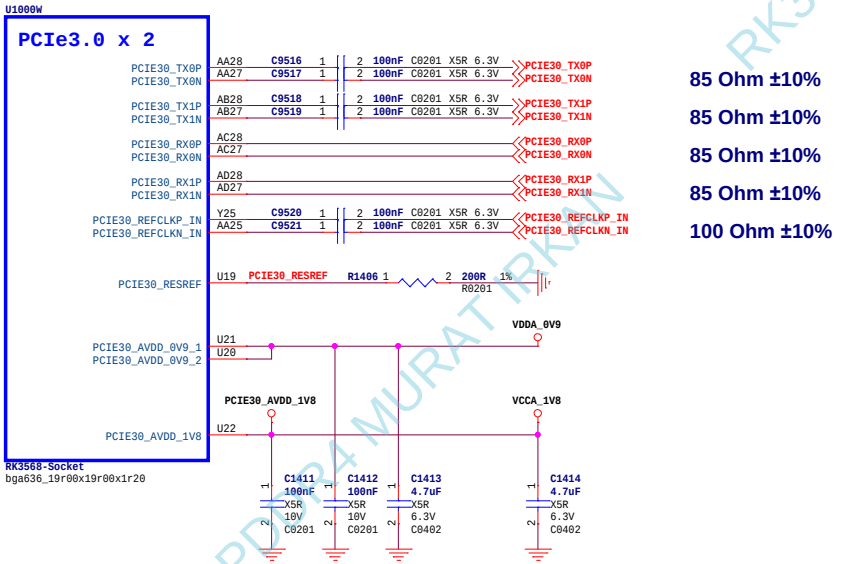
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



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项目：	BEIQI_CE_RK3568		
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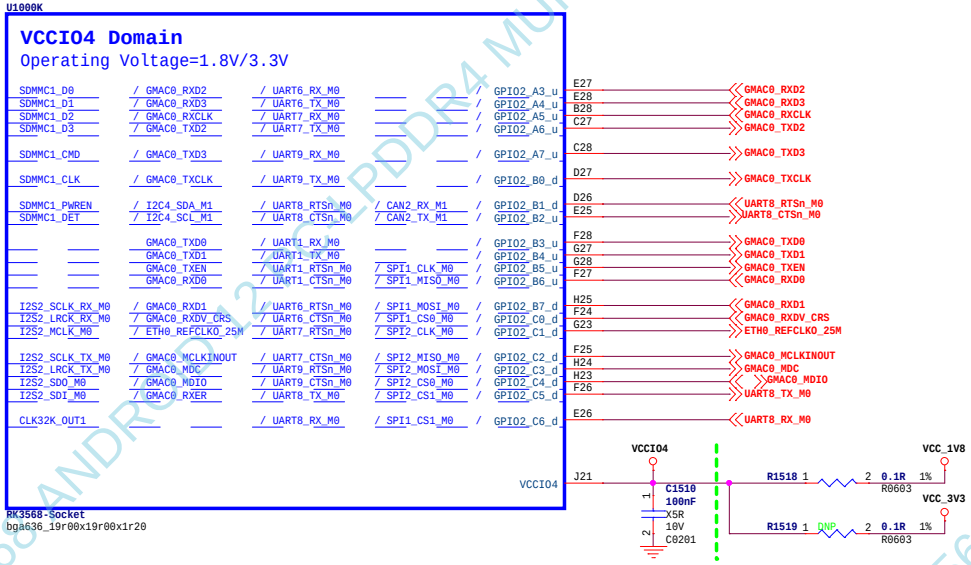
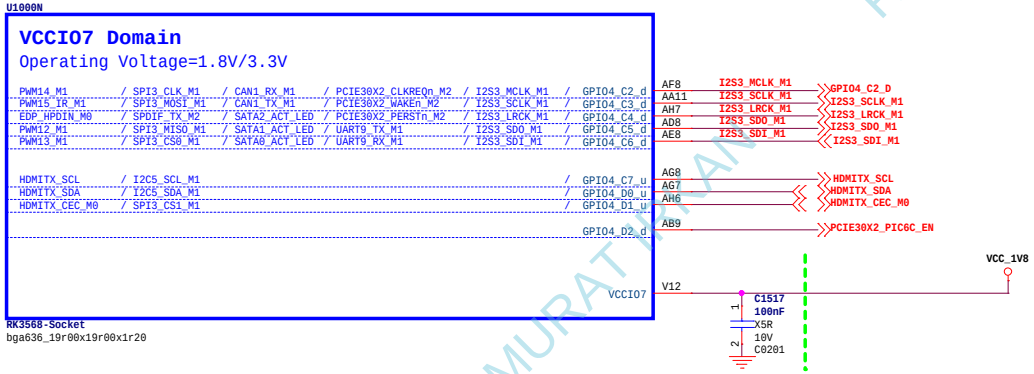
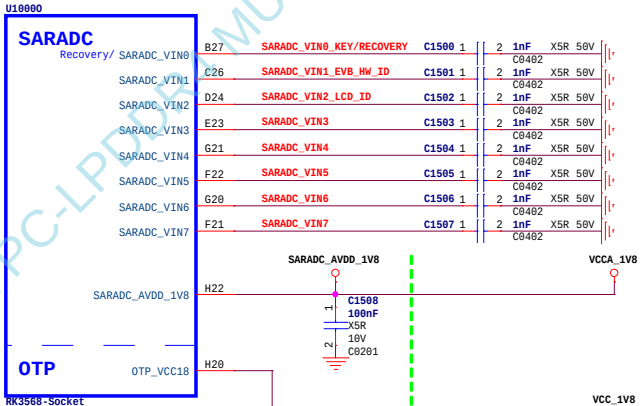
RK3568_K(VCCIO4 Domain)

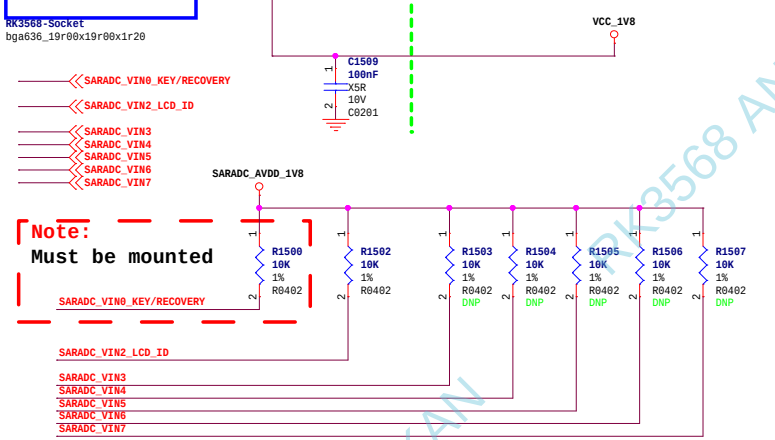


RK3568_N(VCCIO7 Domain)



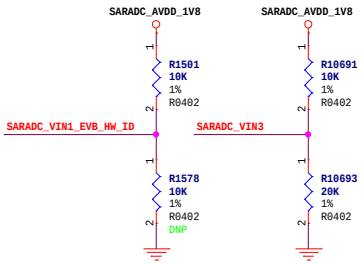
RK3568_O(SARADC/OTP)





Note:
Must be mounted

SARADC_VIN1_EVB_HW_ID	Rup	Rdown	ADC	
EVB1	10K	DNP	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	DNP	10K	0	0V
EVB8				



Note:
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项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	15.RK3568_SARADC/GPIO		
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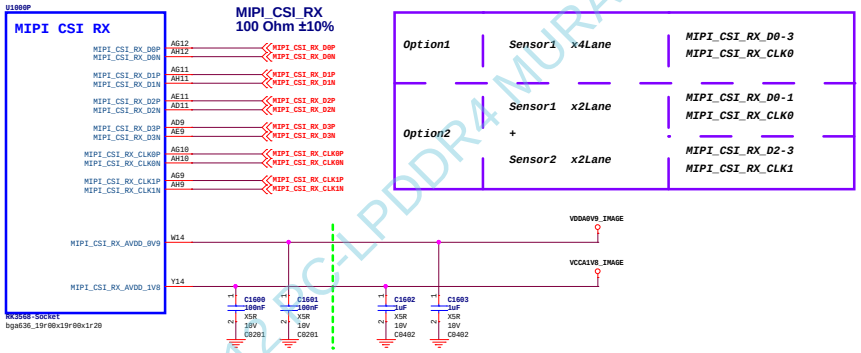
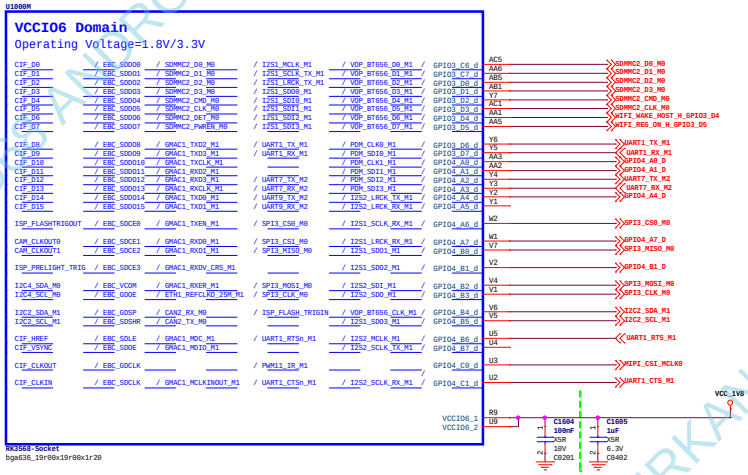
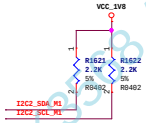
RK3568_P(MIPI_CSI_RX)



RK3568_M(VCCIO6 Domain)





Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
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项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	16.RK3568_VI Interface		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
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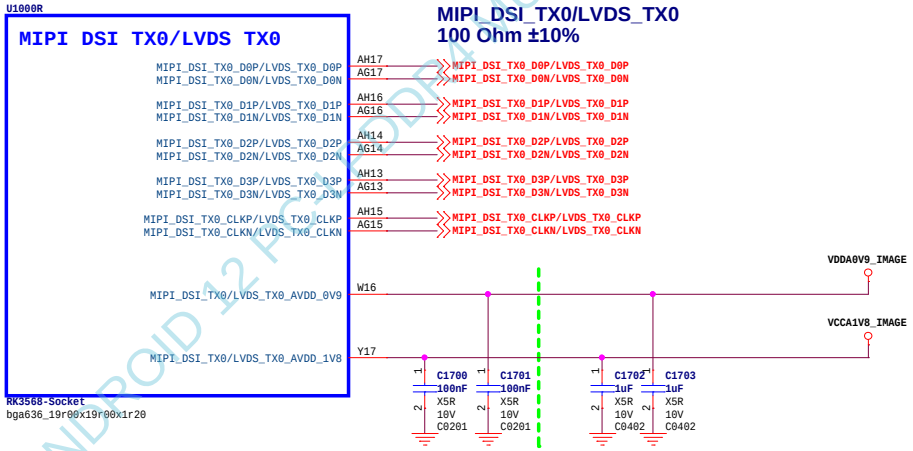
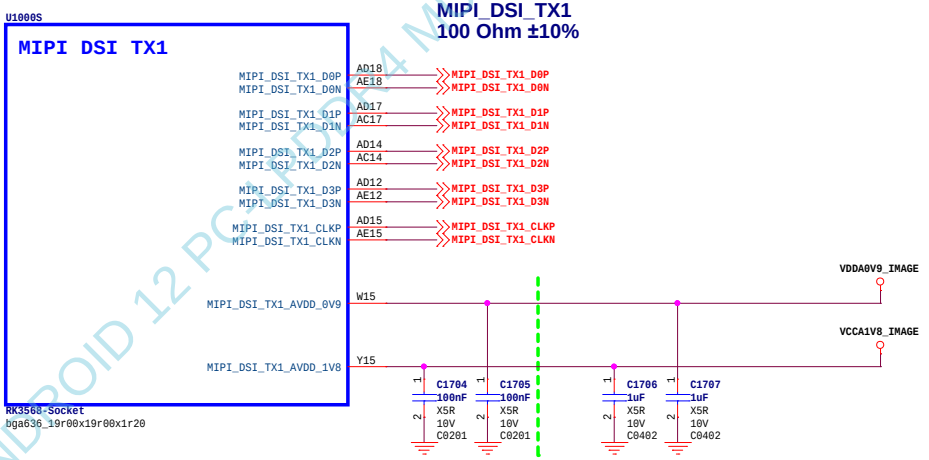
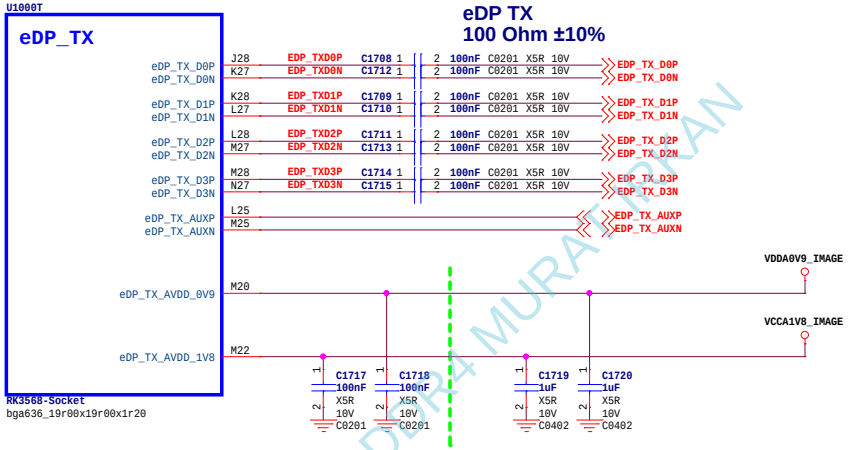
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



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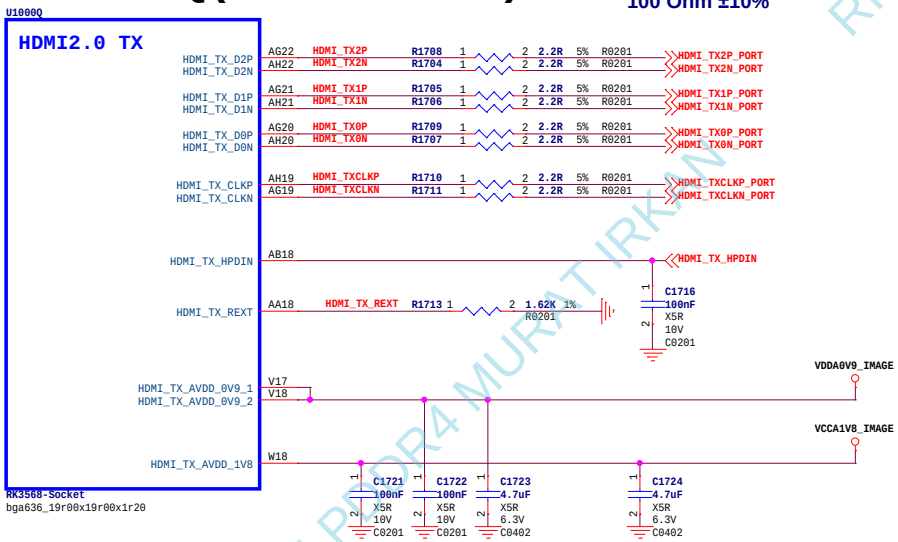
RK3568_Q(HDMI2.0 TX)



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项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	17.RK3568_VO Interface_1		
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RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568-Socket
bga636_19r00x19r00x1r20

AG6 GMAC1_INT/PMEB_GPIO2_D0
AD7 GMAC1_RSTn_GPIO2_D1
AC8 GMAC0_INT/PMEB_GPIO2_D2
AC7 GMAC0_RSTn_GPIO2_D3
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 BT_LED
AH4 BT_REG_ON_H_GPIO3_A0
AB8 BT_WAKE_HOST_H_GPIO3_A1
AE5 GMAC1_TXD2_M0
AG4 GMAC1_TXD3_M0
AF4 GMAC1_RXD2_M0
AH3 GMAC1_RXD3_M0
AG3 GMAC1_TXCLK_M0
AH2 GMAC1_RXCLK_M0
AG2 ETH1_REFCLKO_25M_M0
AG1 GMAC1_RXD0_M0
AF2 GMAC1_RXD1_M0
AF1 GMAC1_RXDV_CRS_M0
AE1 HOST_WAKE_BT_H_GPIO3_B4
AE2 GMAC1_TXD0_M0
AE3 GMAC1_TXD1_M0
AD4 GMAC1_TXEN_M0
AD2 GMAC1_MCLKINOUT_M0
AD1 PCIE20_PERSTn_M1
AA7 HP_DET_L_GPIO3_C2
AC4 FAN_CTRL
AC3 GMAC1_MDC_M0
AC2 GMAC1_MDIO_M0

VCCIO5
V10
V11
C1800 100nF X5R 10V C0201
C1801 1uF X5R 6.3V C0402 DNP
R10699 1 DNP 5% 2 R0402
R10700 1 0R 5% 2 R0402
VCC_3V3
VCC_1V8

VCCIO5
R1800 10K 5% R0402
R1801 10K 5% R0402
GMAC1_INT/PMEB_GPIO2_D0
GMAC0_INT/PMEB_GPIO2_D2
od

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	18.RK3568_VO Interface_2		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
设计者:	CZA	页码:	18of 99

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/	GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/	GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/	GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/	GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/	GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/	GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/	GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/	GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/	GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/	GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/	GPIO1_B3_d

VCCIO1

RK3568-Socket

bga636_19r00x19r00x1r20

D18 E18 A19 B19 F18 A20 C20 B20 D20 E20 A21 B21

I2C3_SDA_M0
I2C3_SCL_M0
I2S1_MCLK_M0
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0
I2S1_SCLK_TX_M0_RK809
I2S1_SCLK_RX_M0
GPIO1_A4_D
I2S1_LRCK_TX_M0
I2S1_LRCK_TX_M0_RK809
I2S1_LRCK_RX_M0
PDM_CLK0_M0_RK809
I2S1_SDO0_M0
I2S1_SDO0_M0_RK809
GPIO1_B0_D
GPIO1_B1_D
GPIO1_B2_D
I2S1_SDI0_M0
I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17

C1900
100nF
X5R
10V
C0201

Default:RK809+PDM MIC
S1900=ON
S1901=OFF

VCCIO_ACODEC

R1905
2.2K
5%
R0402

R1906
2.2K
5%
R0402

I2C3_SDA_M0
I2C3_SCL_M0

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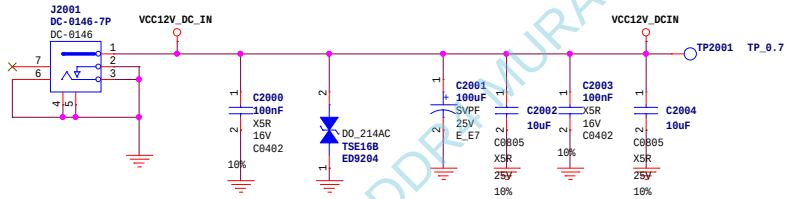
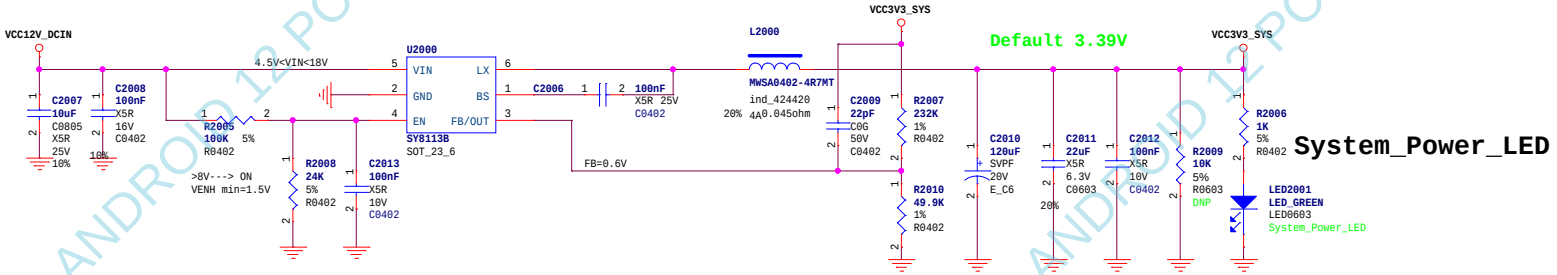
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	19.RK3568_Audio Interface		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	19 of 99

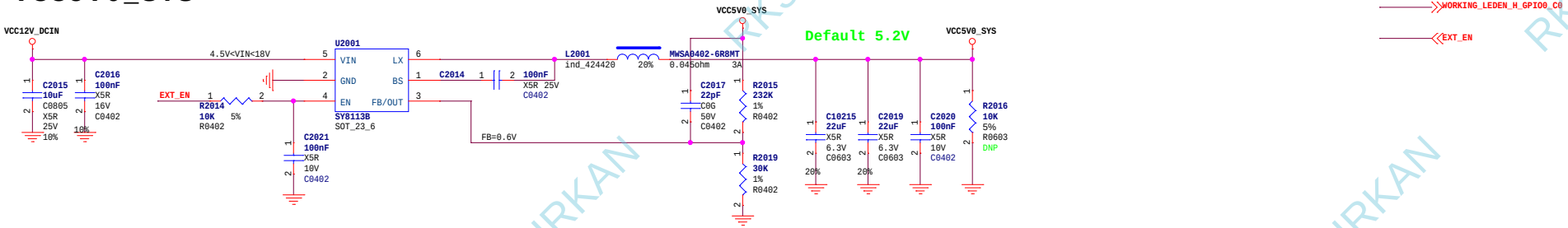
12V/3A DCIN



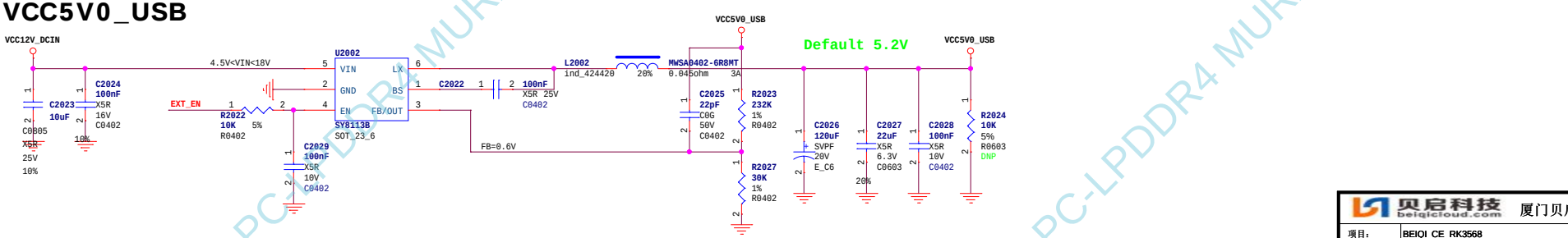
VCC3V3_SYS



VCC5V0_SYS



VCC5V0_USB



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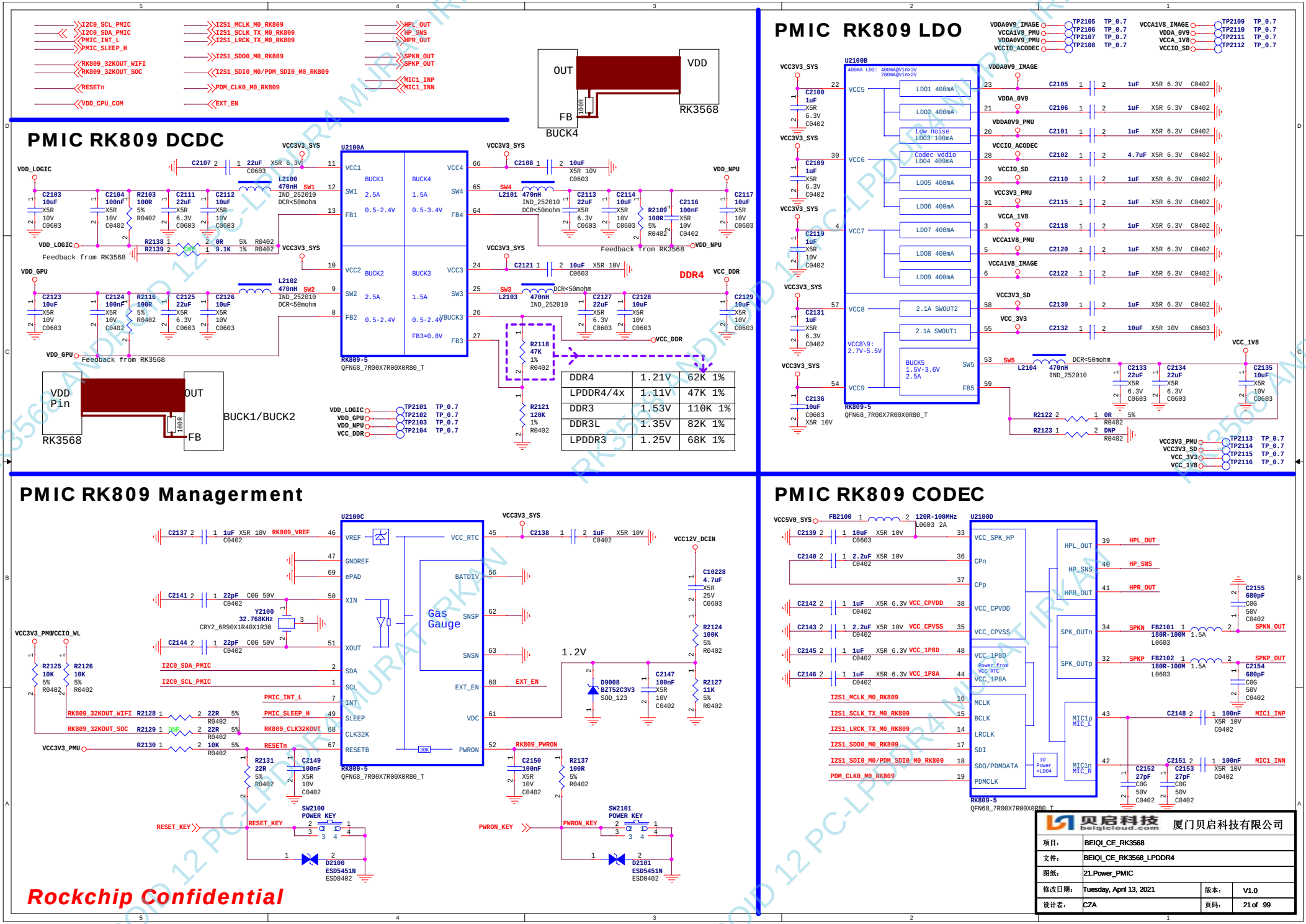
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	20.Power_DC IN		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	20 of 99


I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RK809_32KOUT_WIFI
RK809_32KOUT_SOC
RESETn
VDD_CPU_COM
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
EXT_EN
HPL_OUT
HP_SNS
HPR_OUT
SPKN_OUT
SPKP_OUT
MIC1_INP
MIC1_INN
OUT
VDD
FB
100R
RK3568
BUCK4
PMIC RK809 DCDC
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
VCC3V3_SYS
U2100A
RK809-5
QFN68_7R00X7R00X0R80_T
BUCK1
BUCK2
BUCK3
BUCK4
2.5A
1.5A
0.5-2.4V
0.5-3.4V
0.5-2.4V
FB3=0.8V
L2100 470nH SW1
L2102 470nH SW2
L2101 470nH
L2103 470nH
IND_252010
DCR<50mohm
Feedback from RK3568
DDR4
DDR4 1.21V 62K 1%
LPDDR4/4x 1.11V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.25V 68K 1%
BUCK1/BUCK2
TP2101 TP2102 TP2103 TP2104
PMIC RK809 LDO
U2100B
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V-3.6V 2.5A
VCC8\9: 2.7V-5.5V
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_3V3
VCC_1V8
VCCA1V8_PMU
VDDA0V9_PMU
VCCIO_ACODEC
TP2105 TP2106 TP2107 TP2108
TP2109 TP2110 TP2111 TP2112
VCC3V3_PMU
VCC3V3_SD
VCC_3V3
VCC_1V8
TP2113 TP2114 TP2115 TP2116
PMIC RK809 Management
U2100C
RK809-5
QFN68_7R00X7R00X0R80_T
Gas Gauge
Y2100 32.768KHz
CRY2_6R90X1R40X1R30
VCC3V3_PMU
VCCIO_WL
I2C0_SDA_PMIC
I2C0_SCL_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RK809_32KOUT_WIFI
RK809_32KOUT_SOC
RESETn
RK809_CLK32KOUT
RESET_KEY
PWRON_KEY
SW2100 POWER KEY
SW2101 POWER KEY
D2100 ESD5451N
D2101 ESD5451N
ESD0402
1.2V
D9008 BZT52C3V3
SOD_123
VCC12V_DCIN
RK809_PWRON
EXT_EN
Rockchip Confidential
PMIC RK809 CODEC
U2100D
RK809-5
QFN68_7R00X7R00X0R80_T
VCC5V0_SYS
FB2100 120R-100MHz
L0603 2A
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
HPL_OUT
HP_SNS
HPR_OUT
SPKN
SPKP
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
MIC1_INP
MIC1_INN
IO Power =LDO4
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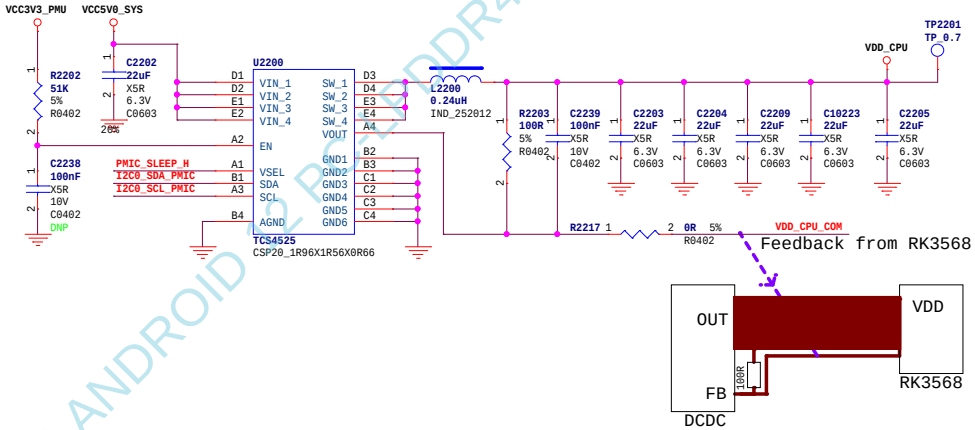
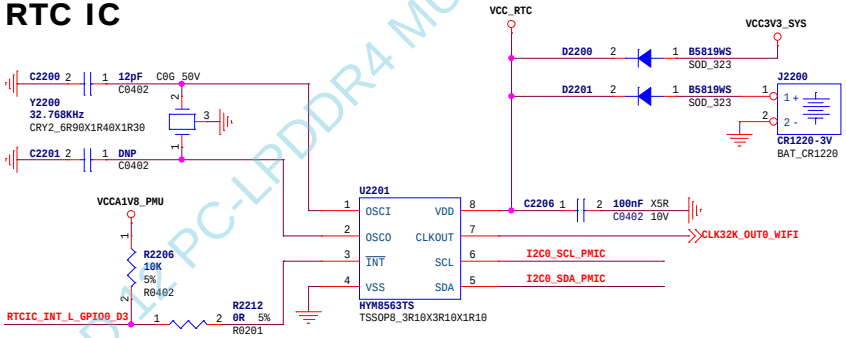
项目: BEIQI_CE_RK3568
文件: BEIQI_CE_RK3568_LPDDR4
图纸: 21.Power_PMIC
修改日期: Tuesday, April 13, 2021
版本: V1.0
设计者: CZA
页码: 21 of 99

CPU_AVS/CPU_DVS_PWM0_M0
PMIC_SLEEP_H
VDD_CPU_COM
I2C0_SCL_PMIC
I2C0_SDA_PMIC
RTCIC_INT_L_GPIO0_D3
I2C5_SCL_M0
I2C5_SDA_M0

VDD_CPU



RTC IC



Address:Read A3H,Write A2H

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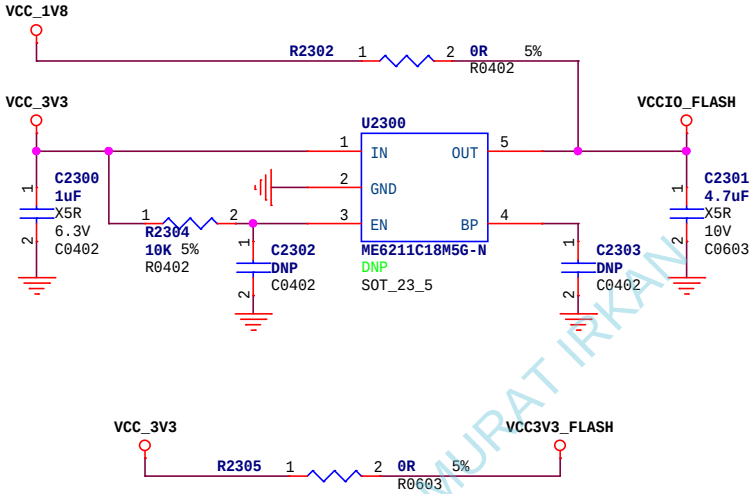
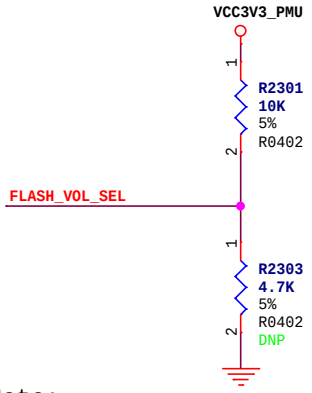
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	22.Power_other		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	22 of 99

FLASH_VOL_SEL

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

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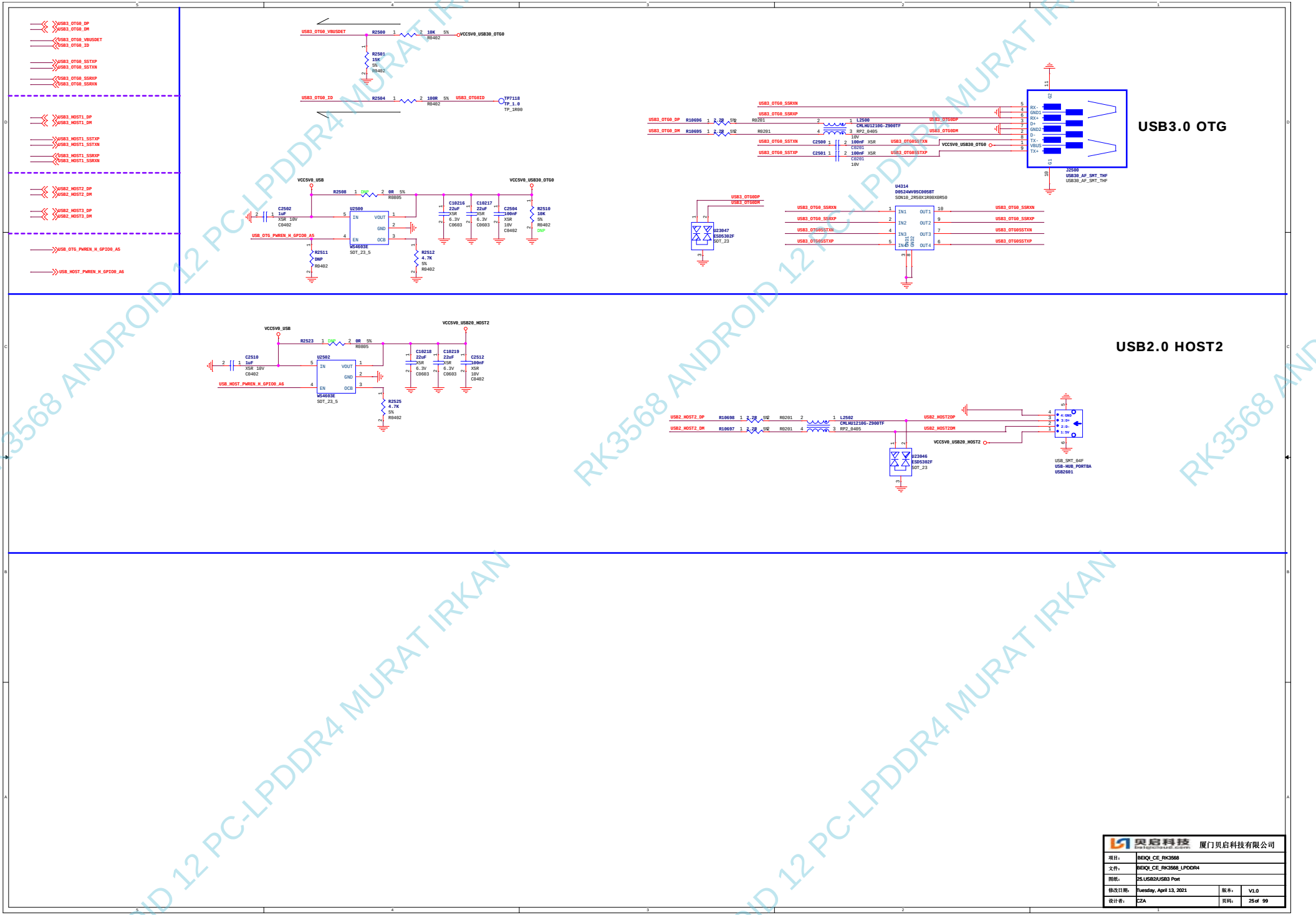
项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	23.Power_Flash Power Manage		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
设计者:	CZA	页码:	23of 99



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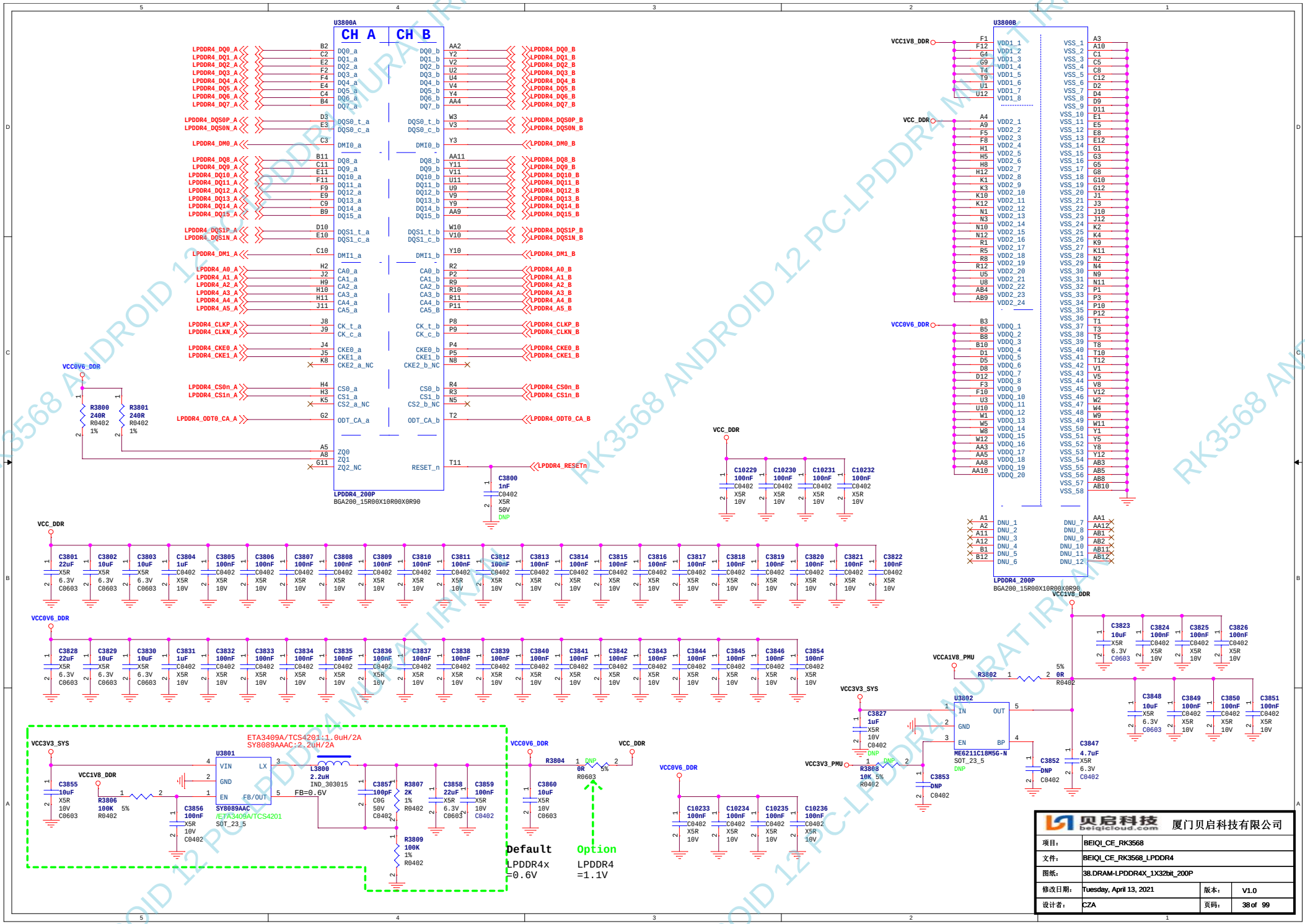
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	25.USB2/USB3 Port		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	25of 99


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC0V6_DDR
VCC_DDR
VCC1V8_DDR
VCC3V3_SYS
VCCA1V8_PMU
VCC3V3_PMU
U3801
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
ETA3409A/TCS4201:1.0uH/2A
SY8089AAC:2.2uH/2A
U3802
ME6211C18M5G-N
SOT_23_5
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
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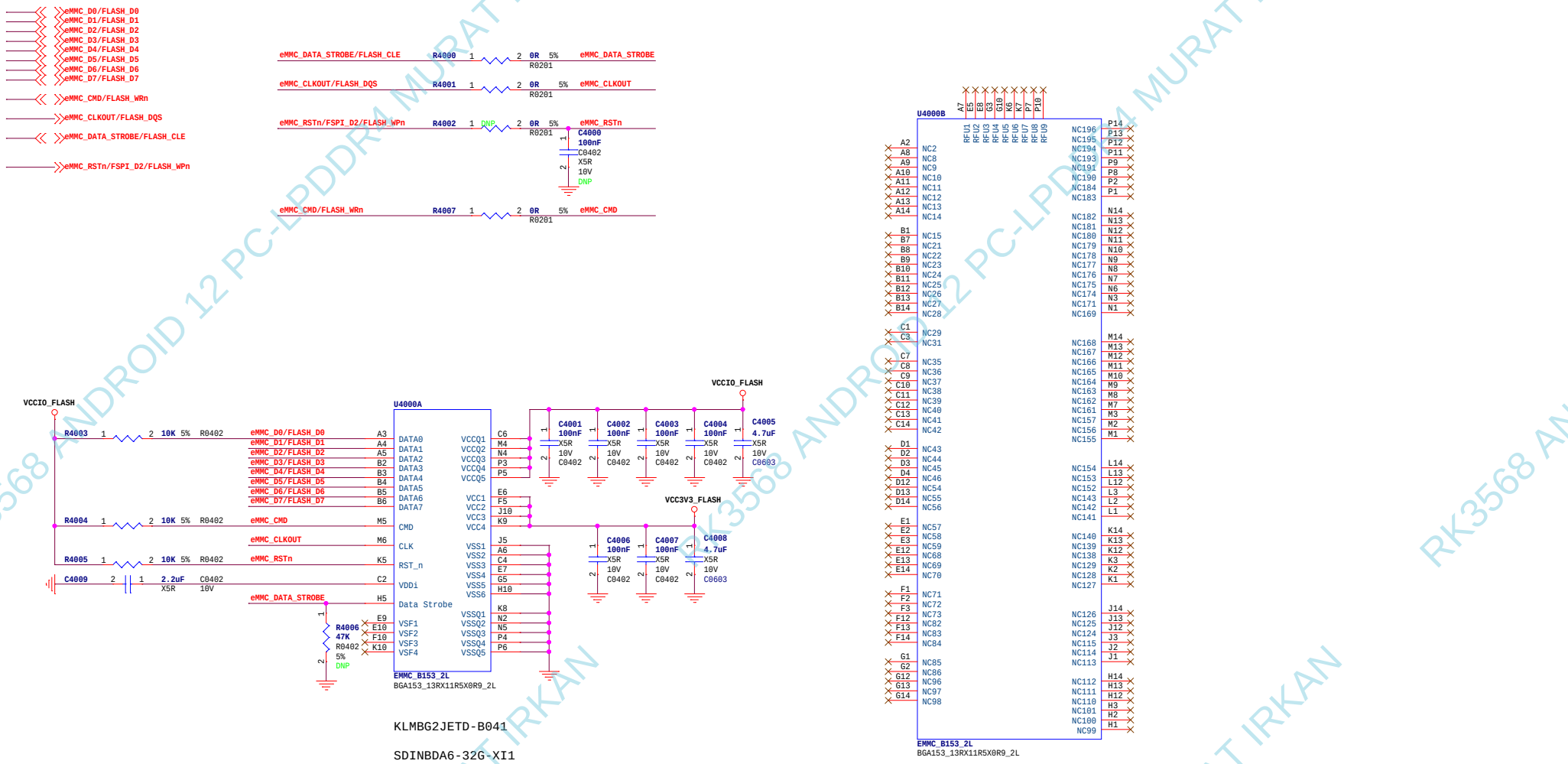
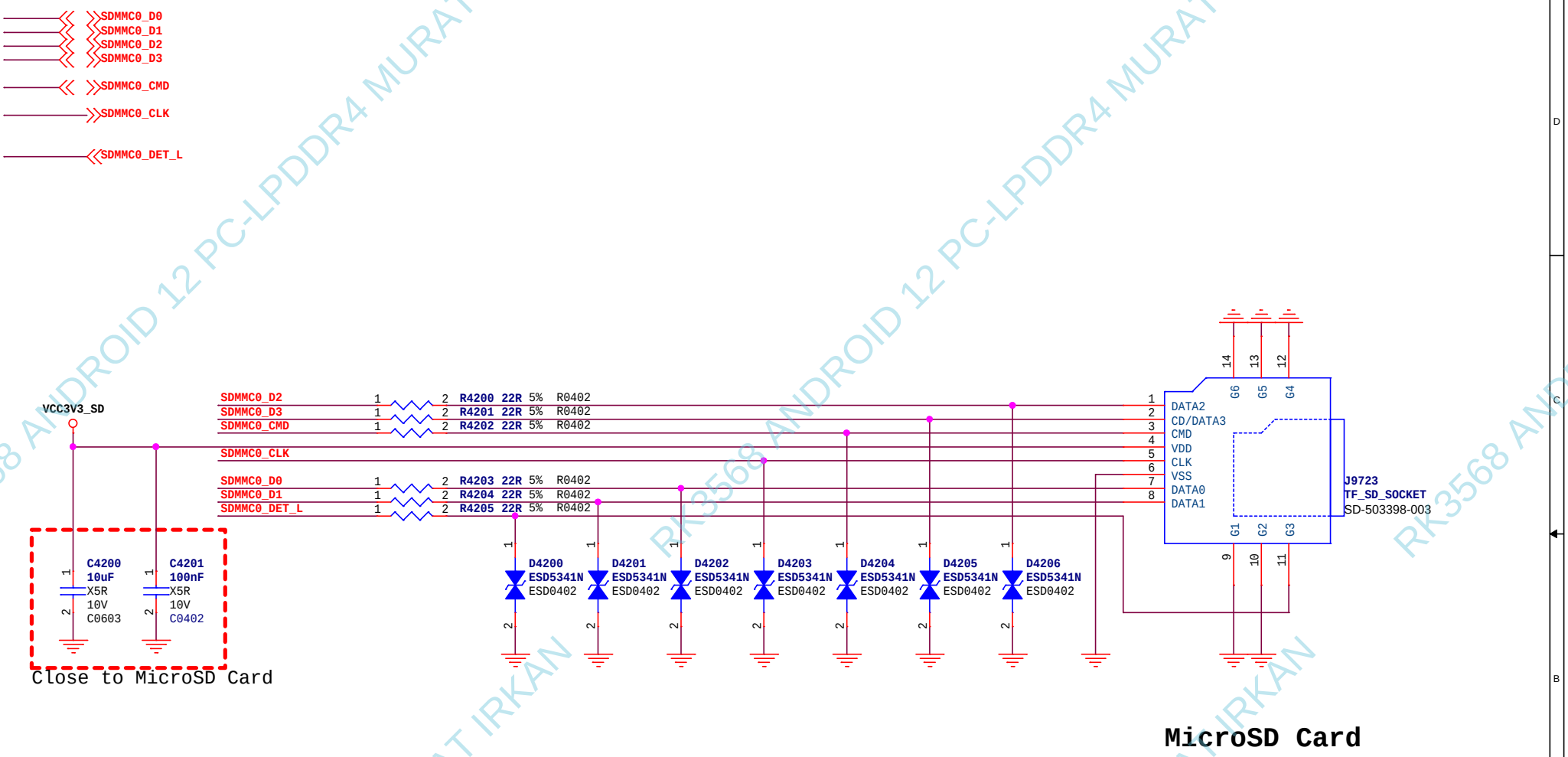
项目: BEIQI_CE_RK3568
文件: BEIQI_CE_RK3568_LPDDR4
图纸: 38.DRAM-LPDDR4X_1X32bit_200P
修改日期: Tuesday, April 13, 2021
版本: V1.0
设计者: CZA
页码: 38 of 99



贝启科技 beiqicloud.com	厦门贝启科技有限公司		
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	40.Flash-eMMC Flash		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	40 of 99



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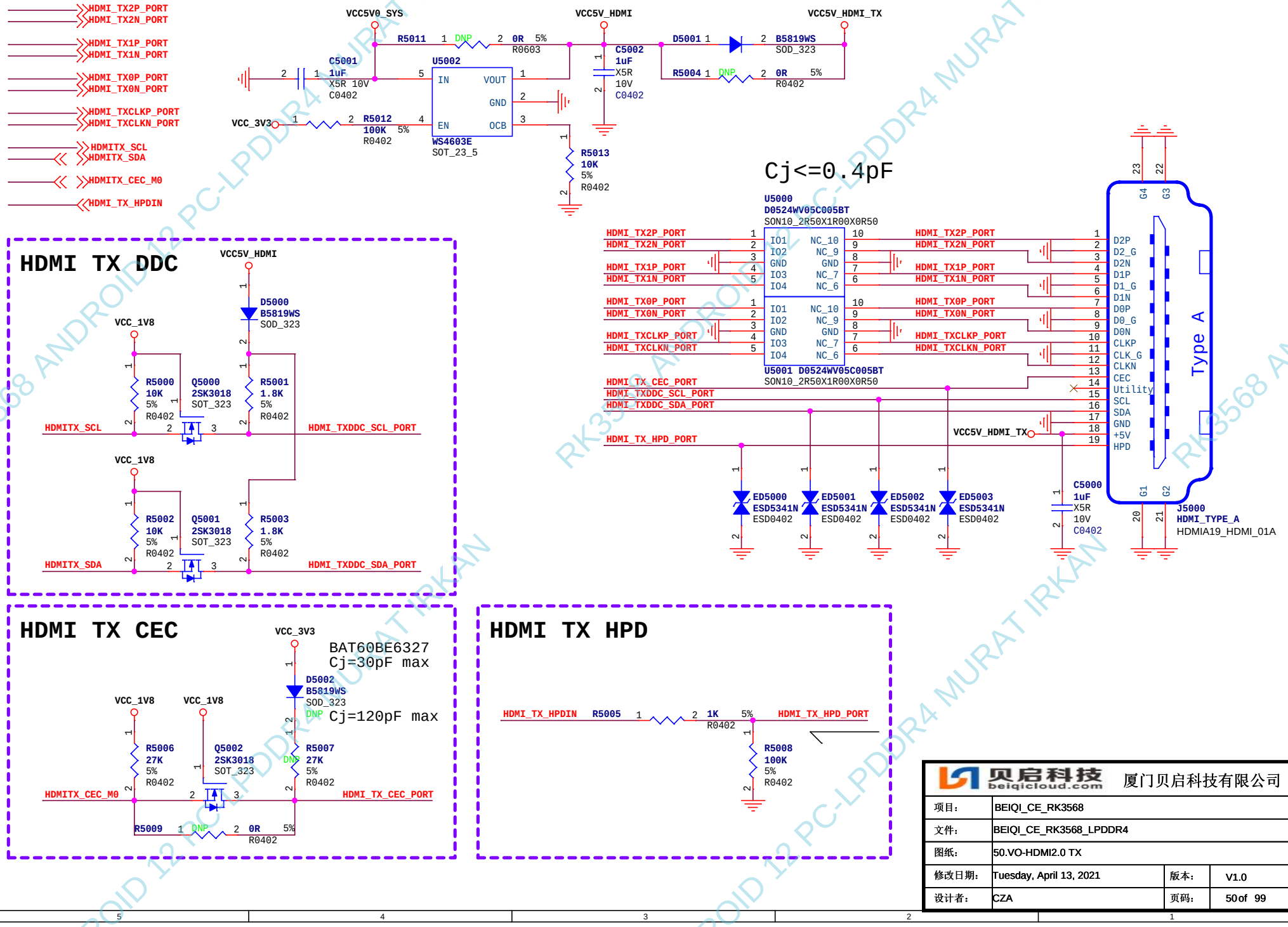
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	42.Flash-MicroSD Card		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	42 of 99



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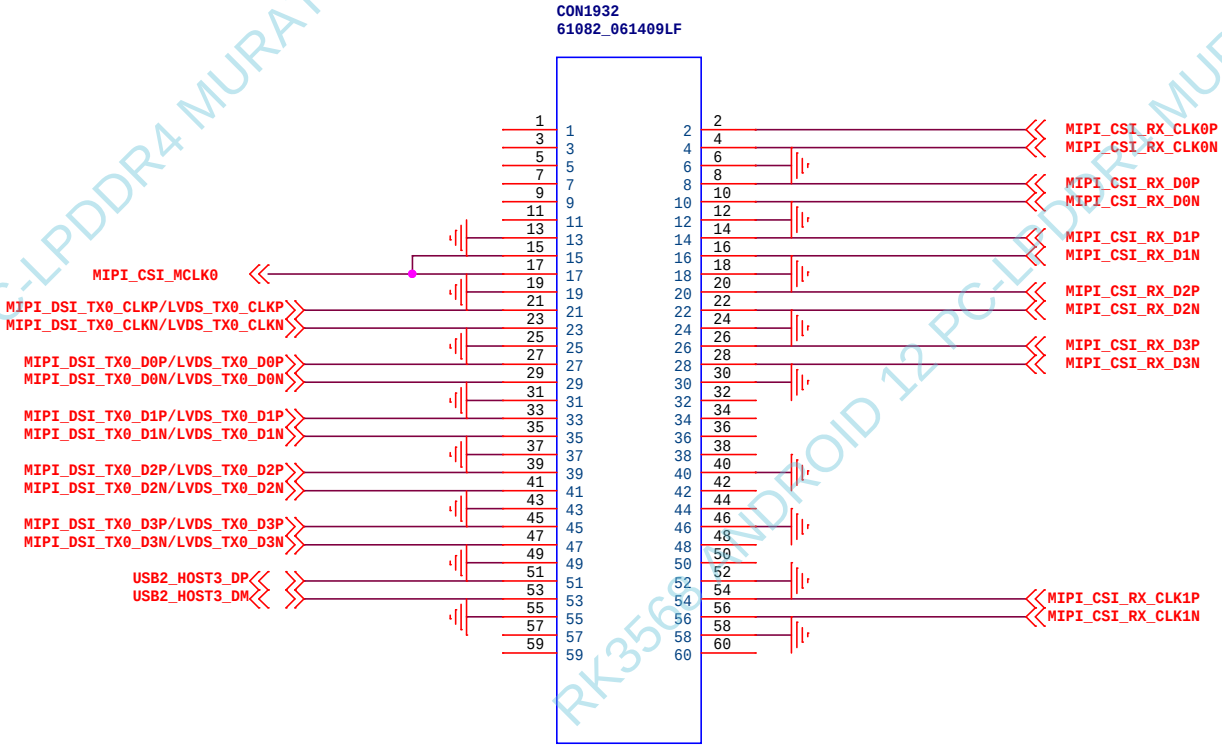
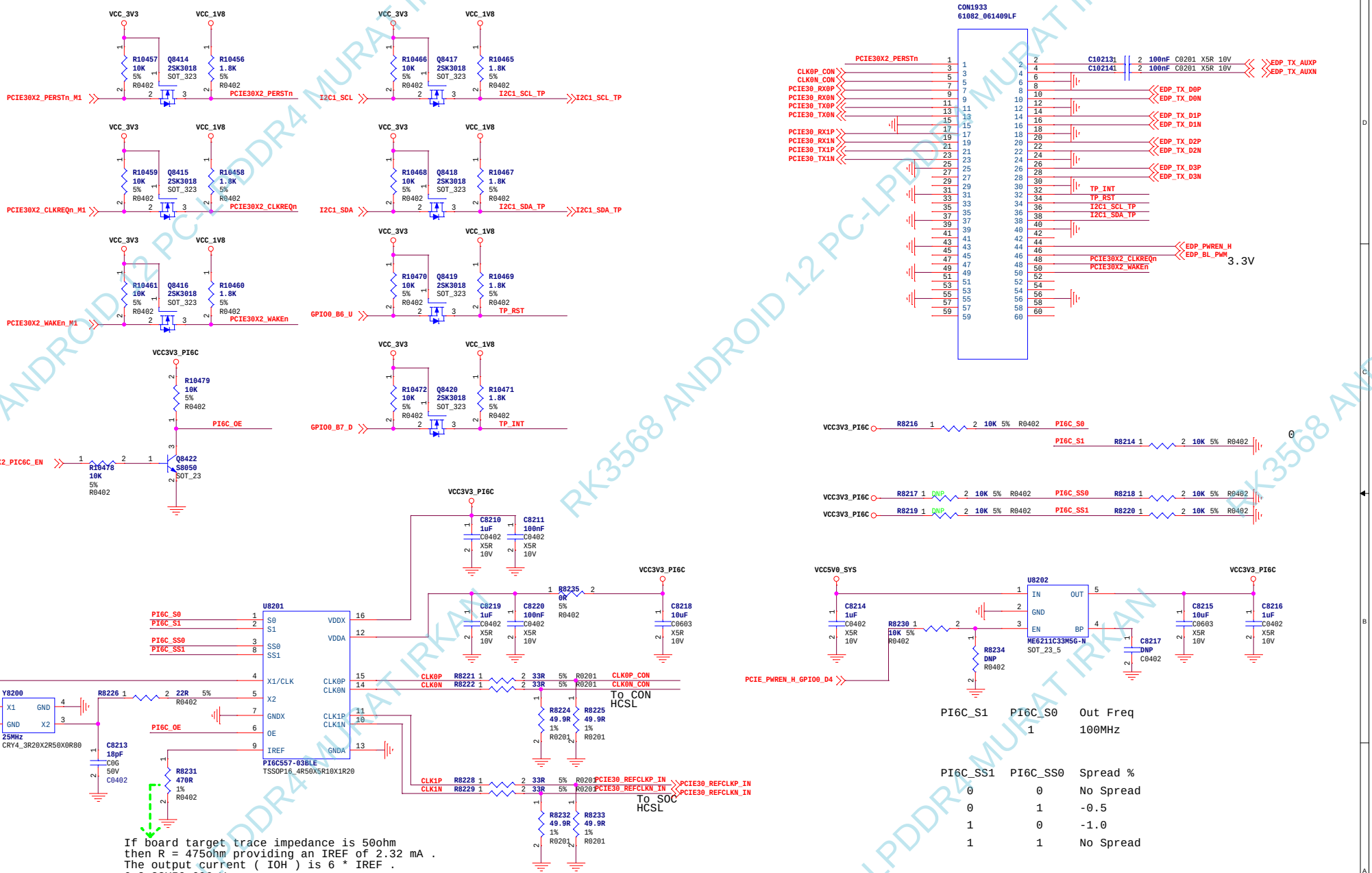
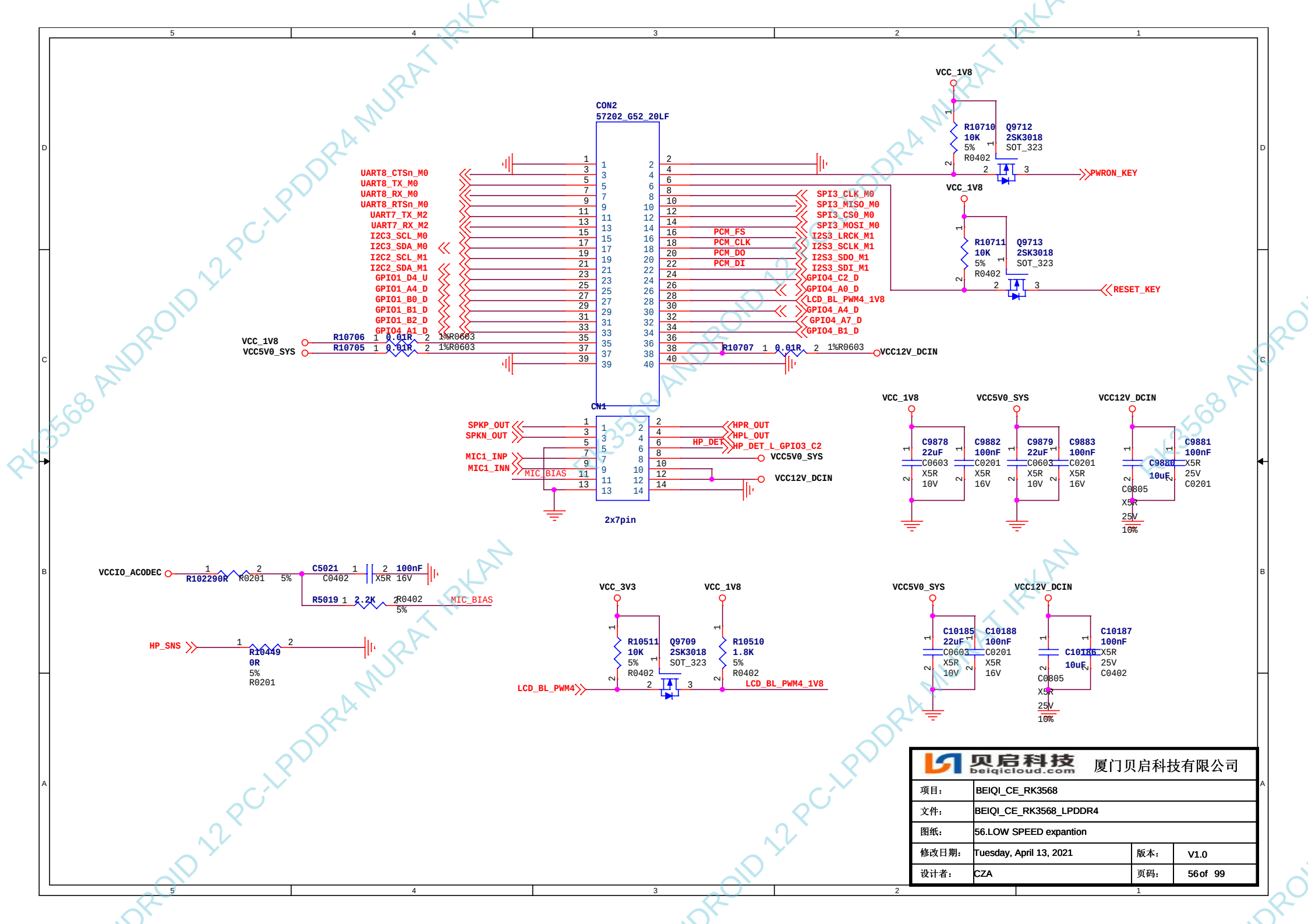
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	50.VO-HDMI2.0 TX		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	50 of 99



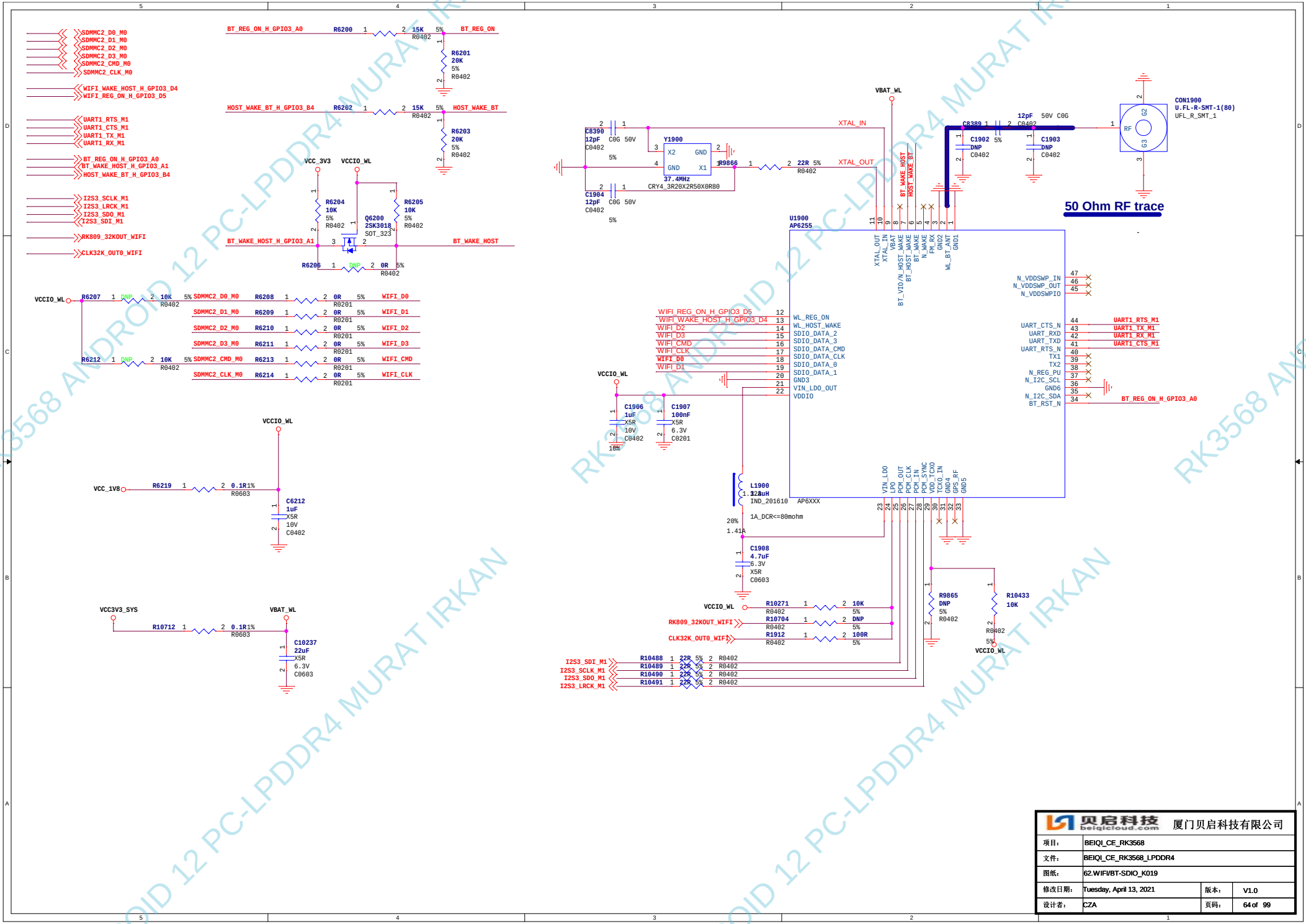
贝启科技 beiqicloud.com 厦门贝启科技有限公司			
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	52.High speed expantion 1		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	52 of 99



贝启科技 beiqicloud.com	厦门贝启科技有限公司		
项目:	BEIQI_CE_RK3568		
文件:	BEIQI_CE_RK3568_LPDDR4		
图纸:	54.High speed expantion 2		
修改日期:	Tuesday, April 13, 2021	版本:	V1.0
设计者:	CZA	页码:	54 of 99



贝启科技 beiqicloud.com 厦门贝启科技有限公司			
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	56.LOW SPEED expantion		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	56 of 99



项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	62.WIFI/BT-SDIO_K019		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	64 of 99

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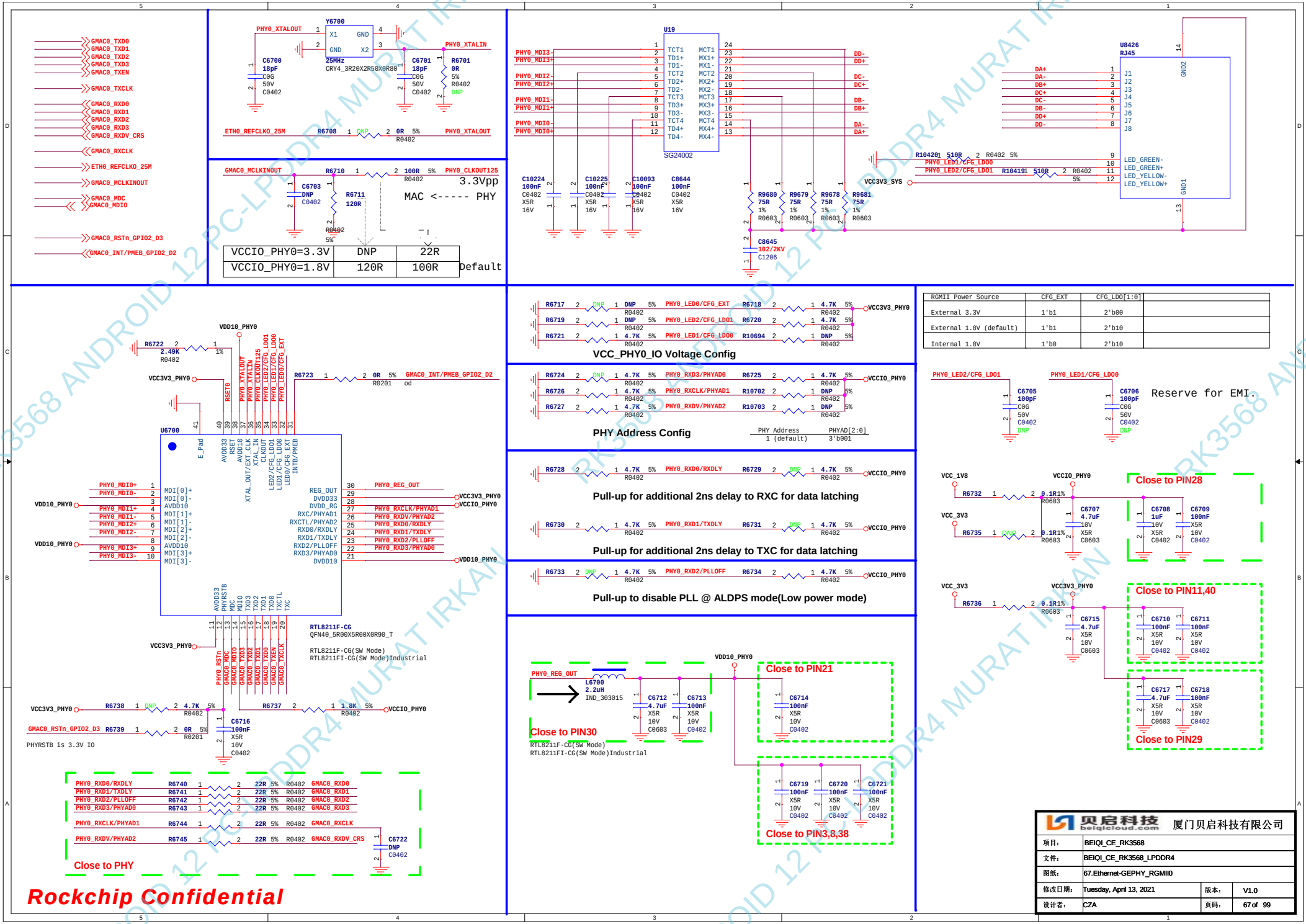
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO2_D3
GMAC0_INT/PMEB_GPIO2_D2
Y6700
25MHz
CRY4_3R20X2R50X0R80
PHY0_XTALOUT
PHY0_XTALIN
C6700 18pF C0G 50V C0402
C6701 18pF C0G 50V C0402
R6701 0R 5% R0402 DNP
ETH0_REFCLKO_25M
R6708 DNP 0R 5% R0402
GMAC0_MCLKINOUT
R6710 100R 5% R0402
PHY0_CLKOUT125
C6703 DNP C0402
R6711 120R R0402
3.3Vpp
MAC <----- PHY
VCCIO_PHY0=3.3V DNP 22R
VCCIO_PHY0=1.8V 120R 100R Default
U19
SG24002
PHY0_MDI3-
PHY0_MDI3+
PHY0_MDI2-
PHY0_MDI2+
PHY0_MDI1-
PHY0_MDI1+
PHY0_MDI0-
PHY0_MDI0+
DD-
DD+
DC-
DC+
DB-
DB+
DA-
DA+
C10224 100nF C0402 X5R 16V
C10225 100nF C0402 X5R 16V
C10093 100nF C0402 X5R 16V
C8644 100nF C0402 X5R 16V
R9680 75R 1% R0603
R9679 75R 1% R0603
R9678 75R 1% R0603
R9681 75R 1% R0603
C8645 102/2KV C1206
VCC3V3_SYS
U8426
RJ45
R104201 510R R0402 5%
R104191 510R R0402 5%
PHY0_LED1/CFG_LDO0
PHY0_LED2/CFG_LDO1
LED_GREEN-
LED_GREEN+
LED_YELLOW-
LED_YELLOW+
GND2
GND1
VDD10_PHY0
R6722 2.49K R0402
VCC3V3_PHY0
R6723 0R R0201 od
GMAC0_INT/PMEB_GPIO2_D2
U6700
E_Pad
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R6738 DNP 4.7K R0402
R6737 1.8K R0402
R6739 0R R0201
GMAC0_RSTn_GPIO2_D3
C6716 100nF X5R 10V C0402
PHYRSTB is 3.3V IO
PHY0_RXD0/RXDLY R6740 22R R0402 GMAC0_RXD0
PHY0_RXD1/TXDLY R6741 22R R0402 GMAC0_RXD1
PHY0_RXD2/PLLOFF R6742 22R R0402 GMAC0_RXD2
PHY0_RXD3/PHYAD0 R6743 22R R0402 GMAC0_RXD3
PHY0_RXCLK/PHYAD1 R6744 22R R0402 GMAC0_RXCLK
PHY0_RXDV/PHYAD2 R6745 22R R0402 GMAC0_RXDV_CRS
C6722 DNP C0402
Close to PHY
Rockchip Confidential
R6717 DNP
R6719 DNP
R6721 4.7K
PHY0_LED0/CFG_EXT
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
R6718 4.7K
R6720 4.7K
R10694 DNP
VCC3V3_PHY0
VCC_PHY0_IO Voltage Config
R6724 DNP
R6726 4.7K
R6727 4.7K
PHY0_RXD3/PHYAD0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
R6725 4.7K
R10702 DNP
R10703 DNP
VCCIO_PHY0
PHY Address Config
PHY Address 1 (default)
PHYAD[2:0] 3'b001
R6728 4.7K
PHY0_RXD0/RXDLY
R6729 DNP
Pull-up for additional 2ns delay to RXC for data latching
R6730 4.7K
PHY0_RXD1/TXDLY
R6731 DNP
Pull-up for additional 2ns delay to TXC for data latching
R6733 DNP
PHY0_RXD2/PLLOFF
R6734 4.7K
Pull-up to disable PLL @ ALDPS mode(Low power mode)
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V 1'b1 2'b00
External 1.8V (default) 1'b1 2'b10
Internal 1.8V 1'b0 2'b10
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
C6705 100pF C0G 50V C0402 DNP
C6706 100pF C0G 50V C0402 DNP
Reserve for EMI.
VCC_1V8
VCCIO_PHY0
VCC_3V3
R6732 0.1R1% R0603
R6735 DNP 0.1R1% R0603
C6707 4.7uF 10V X5R C0603
C6708 1uF 10V X5R C0402
C6709 100nF X5R 10V C0402
Close to PIN28
VCC3V3_PHY0
R6736 0.1R1% R0603
C6715 4.7uF 10V X5R C0603
C6710 100nF X5R 10V C0402
C6711 100nF X5R 10V C0402
Close to PIN11,40
C6717 4.7uF X5R 10V C0603
C6718 100nF X5R 10V C0402
Close to PIN29
PHY0_REG_OUT
L6700 2.2uH IND_303015
C6712 4.7uF X5R 10V C0603
C6713 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C6714 100nF X5R 10V C0402
Close to PIN21
C6719 100nF X5R 10V C0402
C6720 100nF X5R 10V C0402
C6721 100nF X5R 10V C0402
Close to PIN3,8,38
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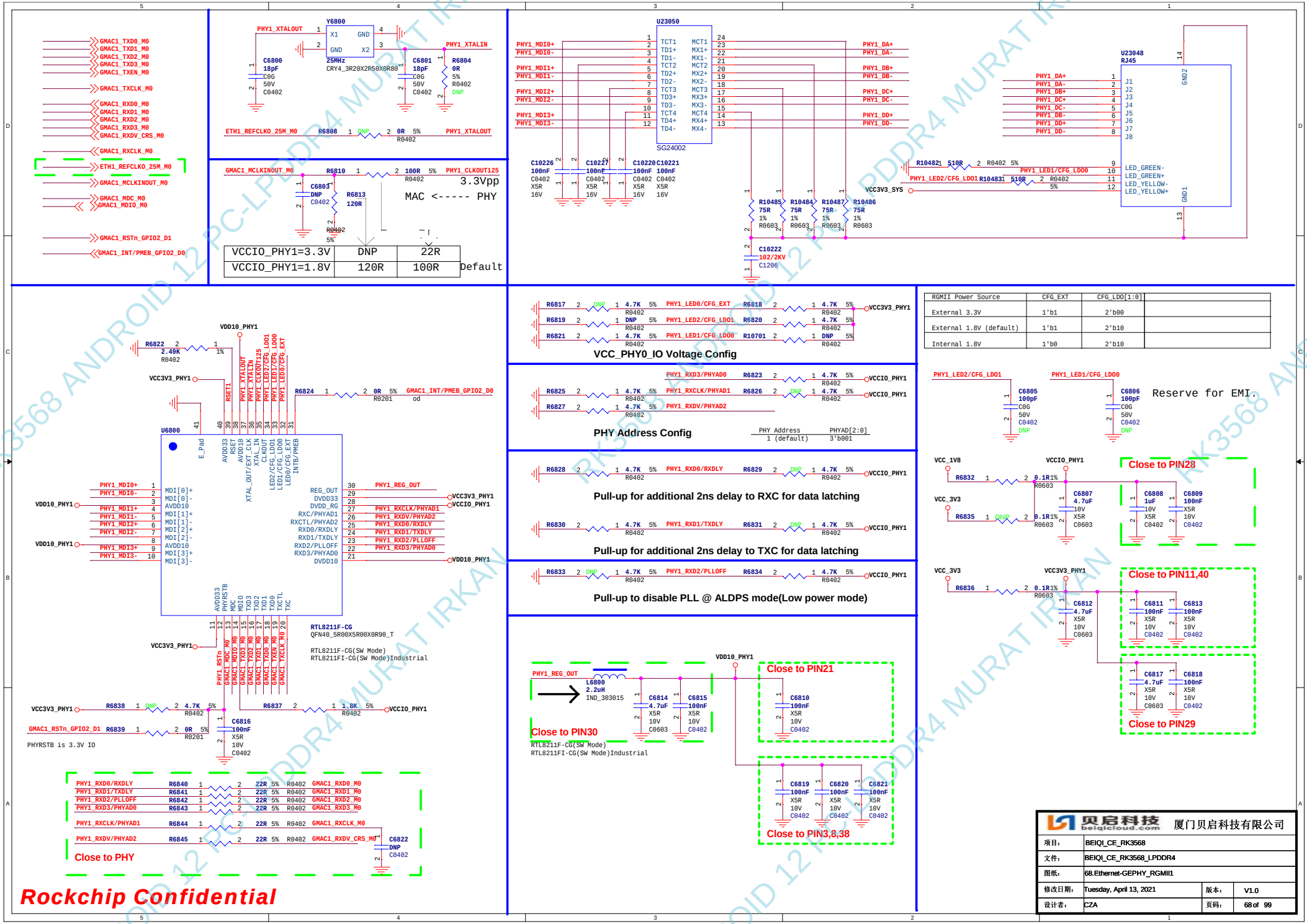
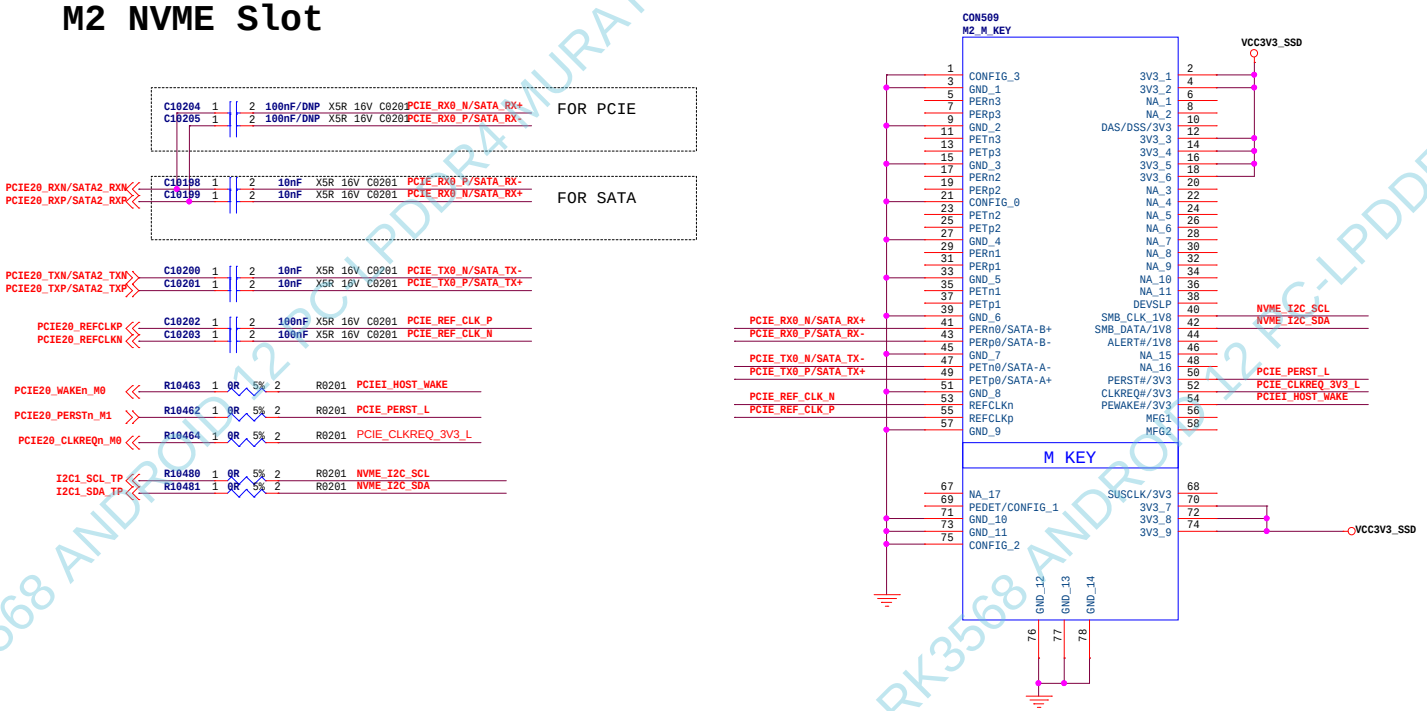
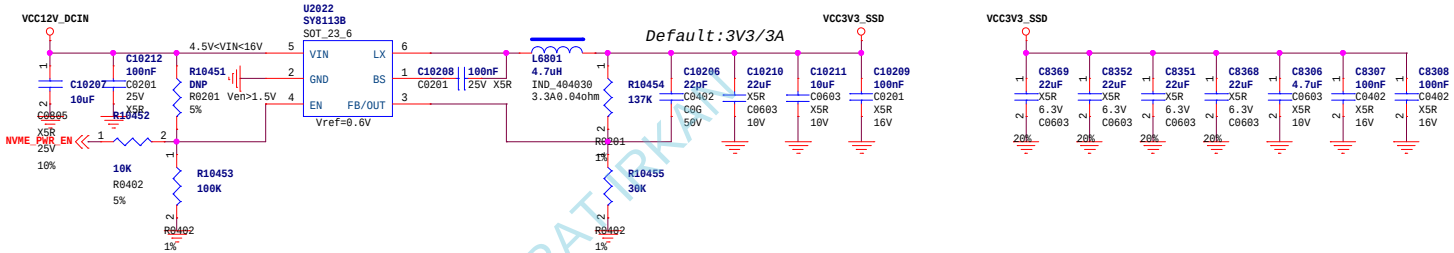
项目: BEIQI_CE_RK3568
文件: BEIQI_CE_RK3568_LPDDR4
图纸: 67.Ethernet-GEPHY_RGMII0
修改日期: Tuesday, April 13, 2021
版本: V1.0
设计者: CZA
页码: 67 of 99



M2 NVME Slot





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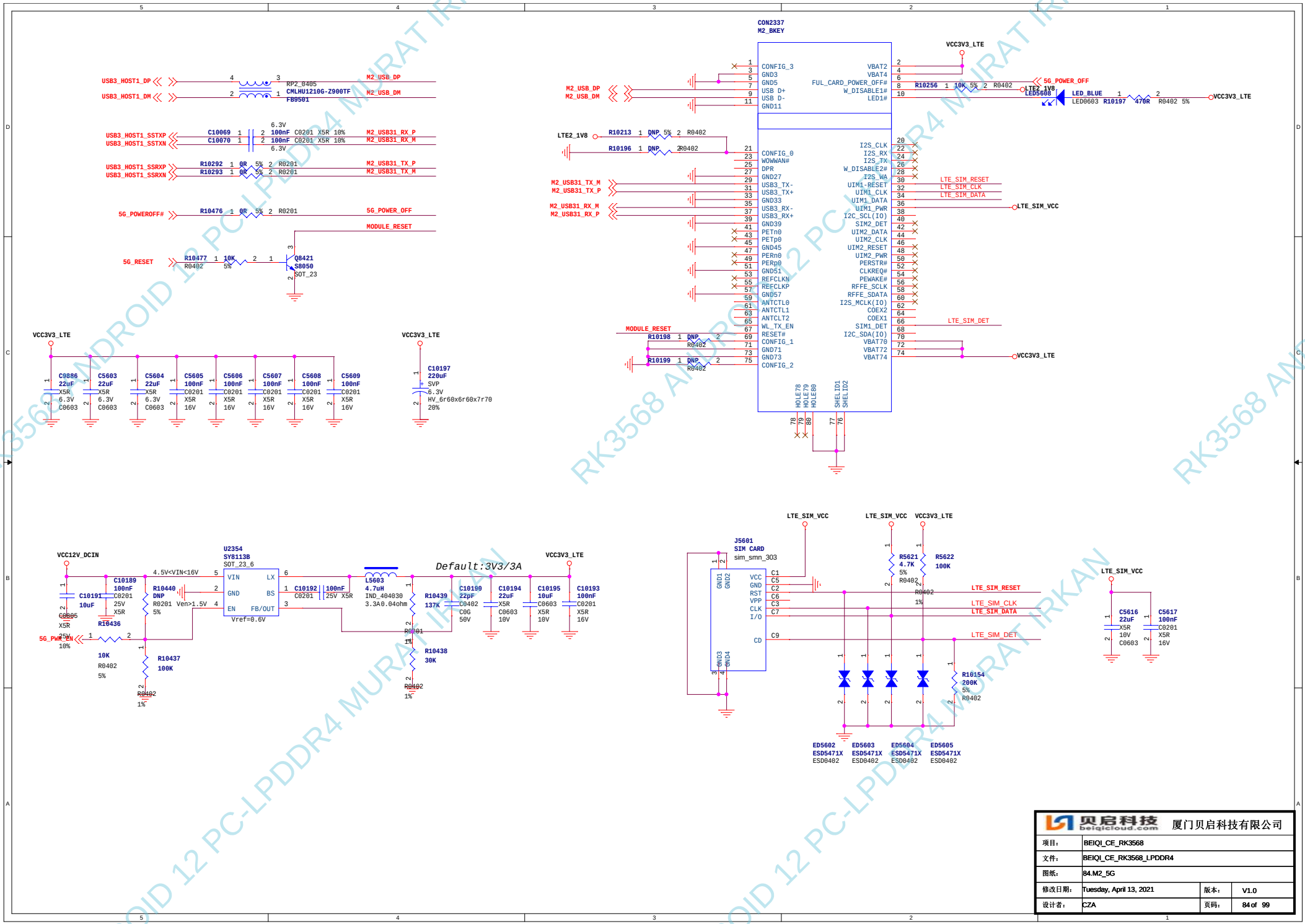
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	83.M.2 SSD		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	83 of 99



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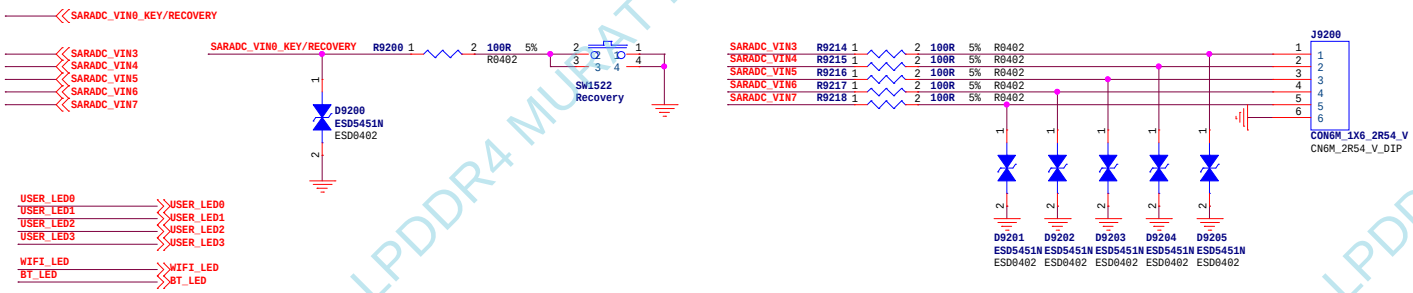
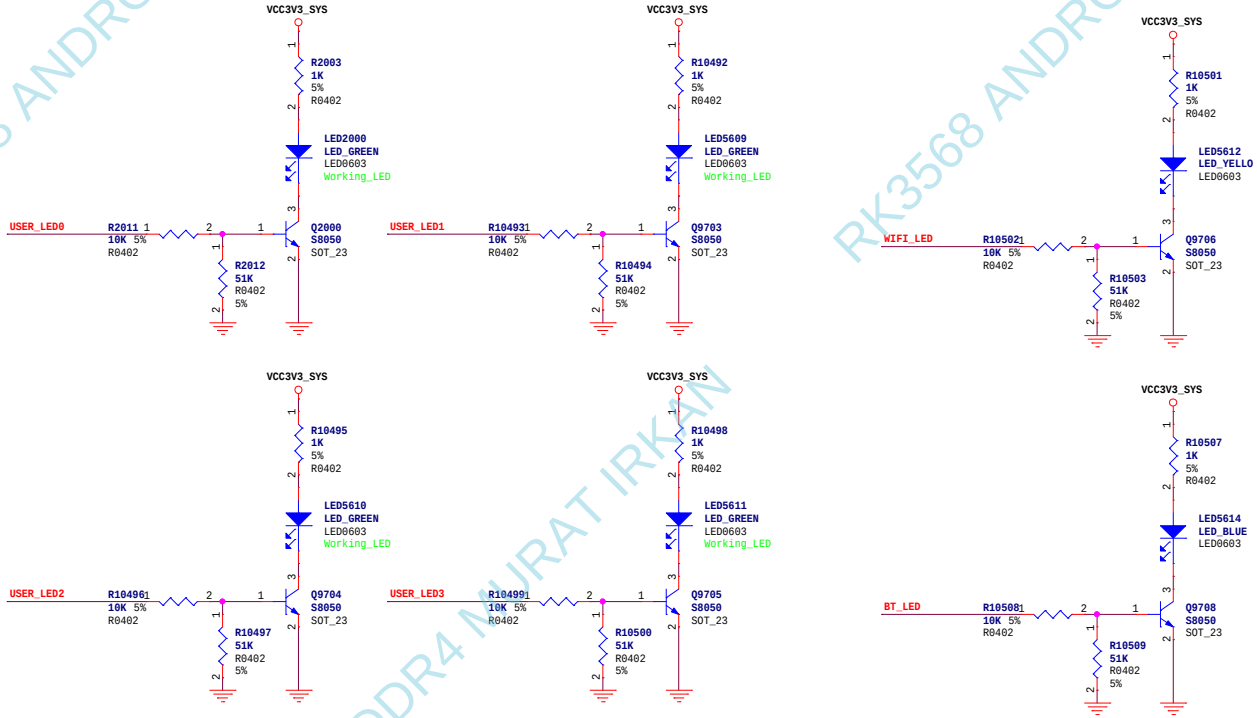
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	84.M2_5G		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	84 of 99



Working LED



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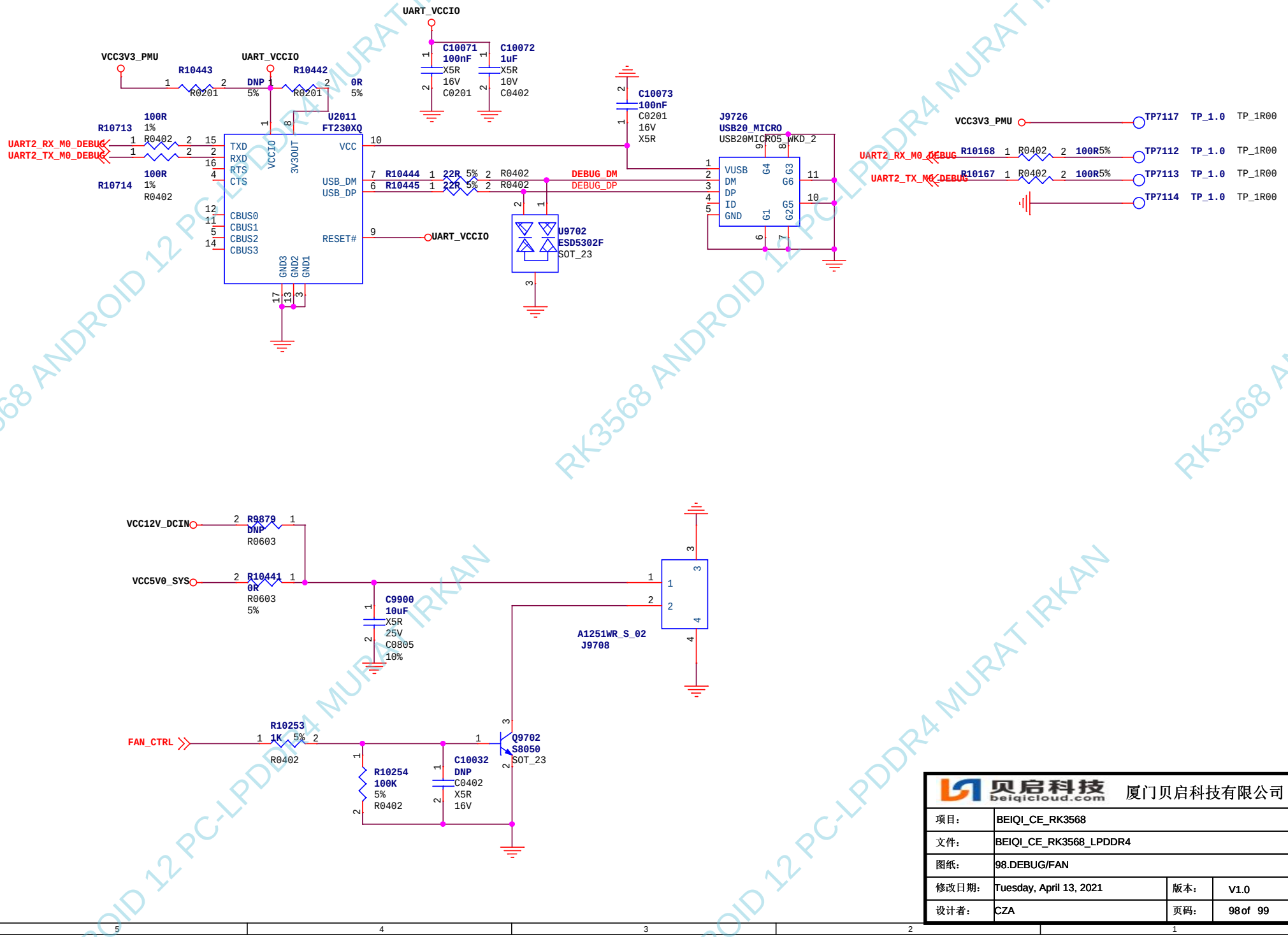
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	92.KEY Array		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	92 of 99



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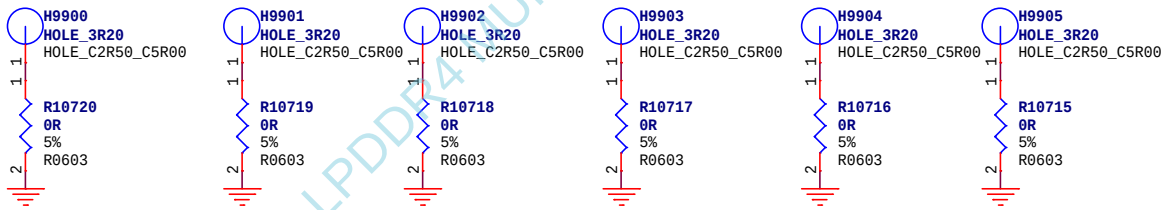
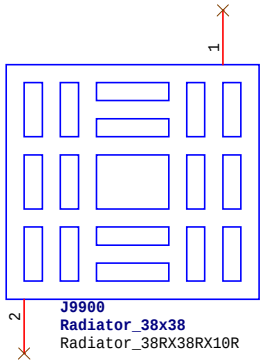
项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	98.DEBUG/FAN		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	98 of 99





TOP Mark

BOTTOM Mark

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项目：	BEIQI_CE_RK3568		
文件：	BEIQI_CE_RK3568_LPDDR4		
图纸：	99.Mark/Hole/Heatsink		
修改日期：	Tuesday, April 13, 2021	版本：	V1.0
设计者：	CZA	页码：	99 of 99