Reference Schematic For RK3308

RK3308_AI-VA_MB_REF_V11

20180703

PMIC: Discrete
RAM: DDR3
ROM: eMMC/Nand/SPI Nor + TF card
Interface: ACODEC/I2S/PDM/SPDIF/LCDC/MAC

	Fuzhou Rockchip Electronics
Project:	**RK3308_AI-VA_MB_REF**
File:	**00.Cover Page**
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Note

NOTE 1：

Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:

Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

ROCKCHIP 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3308_AI-VA_MB_REF		
File:	01.Index		
Date:	Wednesday, July 04, 2018	Rev:	1.1
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Revision History

Version	Date	Author	Change Note	Approved
V0.1	2018.03.07	Joseph.Wei	First edition	
V1.0	2018.05.11	Joseph.Wei	**1 Update VDD_CORE&VDD_LOG Power supply circuits, they are seperated by different power supply** **2 Update Analog MIC circurt,MIC1&MIC 2 as Loopback function, MIC3~MIC8 as MIC IN function.** 3 Update VDD_LOG Power supply circuit, Set VDD_LOG default voltage as 1.04V,modify R2208=110K%1 4 Update TF Card circuits. 5 Update RMII circuits. 6 Update WiFi circuits. 7 ADD LPDDR2&DDR2 design circuits. 8 Upadate Hardware ID circuits. Detailed change point please check published document: 《RK3308_AI-VA_REF_V10_20180511_SCH_Modify_Notes》.	
V1.1	2018.07.03	Joseph.Wei	1 ADD PMIC RK816-3 design circuits. 2 FLASH Default selecet Nand Flash. 3 ADD RTL8723DS design circuits. 4 Modify the ADC of Recovery to ADC_KEY_IN1. 5 Modify divider resistance of WIFI_REG_ON . 6 Modify divider resistance of CLK_32K_OUT . 7 ADD PowerAmp XA8872 design circuits. 8 VDD_1V0 Power Supply from VDD_LOG. 9 PDM MIC:PDM_CLK Unified modify to PIN T16 of RK3308. 10 Modify Loopback circuit parameter.	

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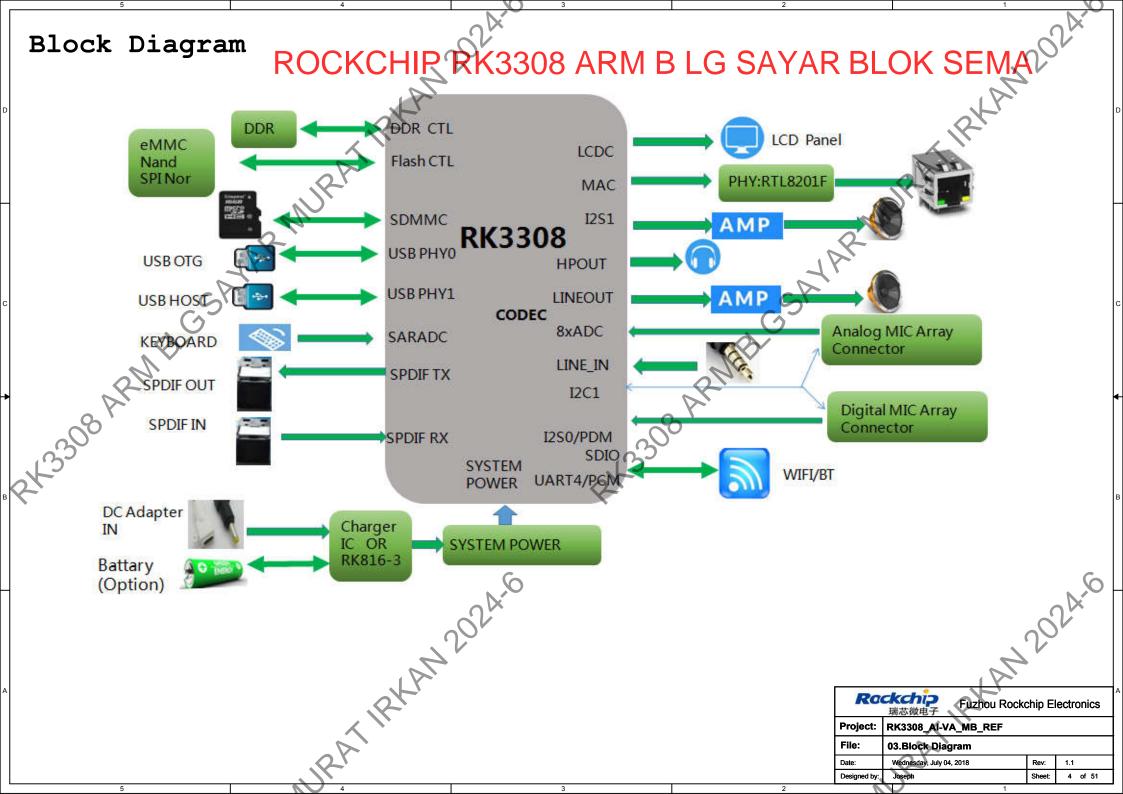
Project:	**RK3308_AI-VA_MB_REF**
File:	**02.Revision History**

Date:	Wednesday, July 04, 2018	Rev:	1.1
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Block Diagram

ROCKCHIP RK3308 ARM B LG SAYAR BLOK SEMA

RK3308 (CODEC) signals	
DDR CTL	DDR
Flash CTL	eMMC / Nand / SPI Nor
SDMMC	
USB PHY0	USB OTG
USB PHY1	USB HOST
SARADC	KEYBOARD
SPDIF TX	SPDIF OUT
SPDIF RX	SPDIF IN
SYSTEM POWER	
LCDC	LCD Panel
MAC	PHY:RTL8201F
I2S1	AMP
HPOUT	
LINEOUT	AMP
8xADC	Analog MIC Array Connector
LINE_IN	
I2C1	
I2S0/PDM	Digital MIC Array Connector
SDIO	WIFI/BT
UART4/PCM	

DC Adapter IN → Charger IC OR RK816-3 → SYSTEM POWER

Battary (Option)

I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0 GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK	VCCIO1	I2C0_SCL I2C0_SDA	VCC_IO	Reserve			
I2C1	GPIO0_B4/I2C1_SCL GPIO0_B3/I2C1_SDA	VCCIO0	I2C1_SCL I2C1_SDA	VCC_IO	IS31FL3236A	0x3C/0x3F	MIC Array Connector-Analog	
					ATSHA204A-SSHDA-T	0x64		
					XA8326	0x31/0x30		
					RK816-3	0x1A		
I2C2	GPIO2_A3/UART0_RTSN/SPI0_CSN0/I2C2_SCL GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA	VCCIO2	I2C2_SCL I2C2_SDA	APIO2_VDD	Reserve			

Power Diagram and Sequence

Scheme1:
12V IN without Battery
REF Select about <POWER&USB PORT>

20.12V IN Without BAT(OPT1)

22.Discrete Power(OPT1&OPT2)

25.USB Port(OPT1&OPT2)

Adapter
12V/2A

BUCK 3A — VCC5V0_SYS

BUCK1 1A — VDD_LOG — RK3308 Logic

LDO1 300mA — Default / Option — VDD_1V0 — RK3308 PLLAVDD_1V0, / RK3308 USB_DVDD_1V0

BUCK2 2A — VDD_CORE — RK3308 ARM Core

BUCK3 1A — VGC_DDR — RK3308 DDR PHY / DDR Device

BUCK4 1A — VCC_IO —
- RK3308 USB_AVDD_3V3
- RK3308 VCCIO0& VCCIO1& VCCIO5 PowerDomain
- TF Card
- SPDIF OUT/IN Port
- LCM 3.3V Supply
- WiFi Module VBAT
- RTL8201F
- PA:XA8326

LDO2 500mA — VCC_1V8 —
- RK3308 PLL_AVDD_1V8
- RK3308 USB_AVDD_1V8
- RK3308 SARADC_AVDD_1V8
- RK3308 OTP_AVDD_1V8
- RESET BYPASS:RESET IC
- 1.8V — RK3308 CODEC_AVDD_1V8

1.8V Default / 3.3V Option — RK3308 VCCIO2 PowerDomain / RK3308 VCCIO4 PowerDomain / VCCIO_WIFI

3.3V Option / 1.8V Option — RK3308 VCCIO3 PowerDomain

LDO4 300mA — 1.8V Default — eMMC or FLASH Nand VCCQ

RK3308 AVDD_CODEC_3V3

Current limiting IC — 5V — USB0 OTG

Current limiting IC — 5V — USB0 HOST

12V — PA:TPA3110&XA8326

Power up Timing

PowerName		timer	Default voltage	Normal voltage
VCC5V0_SYS	DCDC	Slot:1	5.0V	5.0V
VDD_LOG	DCDC	Slot:2	1.04V	1.04V
VDD_1V0	LDO/DCDC	Slot:2	1.0V	1.0V
VDD_CORE	DCDC	Slot:2	1.0V	DVFS
VCC_DDR	DCDC	Slot:4	DDR3=1.5V DDR3L=1.35V	DDR3=1.5V DDR3L=1.35V
VCC_1V8	LDO	Slot:4	1.8V	1.8V
VCCIO_FLASH	LDO(1.8V) or VCC_IO	Slot:4	1.8V	1.8V or 3.3V
VCCIO_SDIO	LDO(1.8V) or VCC_IO	Slot:4	1.8V	1.8V or 3.3V
VCC_IO	DCDC	Slot:4	3.3V	3.3V
Reset		50mS		

IO PowerDomain	Voltage=3.3V	Voltage=1.8V
VCCIO0	3.3V (Default) PMUIO	Support
VCCIO1	3.3V (Default) LCDC	Support
VCCIO2	Support	1.8V (Default) I2S0
VCCIO3	Support	1.8V (Default) eMMC
VCCIO4	Support	1.8V (Default) WiFi(SDIO)
VCCIO5	3.3V (Default) SDMMC	Support

Power Diagram and Sequence

Battery

Charger IC(PowerPath)

Adapter 12V/2A

Power Control

VCC5V0_SYS

12VOLT ADAPTOR

BUCK1 1A → VDD_LOG → RK3308 Logic

LDO1 300mA → VDD_1V0 Default / Option → RK3308 PLLAVDD_1V0, RK3308 USB_DVDD_1V0

BUCK2 2A → VDD_CORE → RK3308 ARM Core

BUCK3 1A → VCC_DDR → RK3308 DDR PHY / DDR Device

BUCK4 1A → VCC_IO →
- RK3308 USB_AVDD_3V3
- RK3308 VCCIO0& VCCIO1& VCCIO5 PowerDomain
- TF Card
- SPDIF OUT/IN Port
- LCM 3.3V Supply
- WiFi Module VBAT
- RTL8201F
- PA:XA8326

LDO2 500mA → VCC_1V8 →
- RK3308 PLL_AVDD_1V8
- RK3308 USB_AVDD_1V8
- RK3308 SARADC_AVDD_1V8
- RK3308 OTP_AVDD_1V8
- RESET BYPASS:RESET IC
- 1.8V → RK3308 CODEC_AVDD_1V8

1.8VDefault / 3.3VOption → RK3308 VCCIO2 PowerDomain / RK3308 VCCIO4 PowerDomain / VCCIO_WIFI

3.3VOption / 1.8VOption → RK3308 VCCIO3 PowerDomain

LDO4 300mA 1.8VDefault → eMMC or FLASH Nand VCCQ

RK3308 AVDD_CODEC_3V3

Current limiting IC → 5V → USB0 OTG

Current limiting IC → 5V → USB0 HOST

BOOST → PA:TPA3110&XA8326

Power up Timing

PowerName	timer	Default voltage	Normal voltage
VCC5V0_SYS	DCDC	Slot:1	5.0V	5.0V
VDD_LOG	DCDC	Slot:2	1.04V	1.04V
VDD_CORE	DCDC	Slot:2	1.0V	DVFS
VDD_1V0	LDO	Slot:3	1.0V	1.0V
VCC_DDR	DCDC	Slot:4	DDR3=1.5V DDR3L=1.35V	DDR3=1.5V DDR3L=1.35V
VCC_1V8	LDO	Slot:4	1.8V	1.8V
VCCIO_FLASH	LDO(1.8V) or VCC_IO	Slot:4	1.8V	1.8V or 3.3V
VCCIO_SDIO	LDO(1.8V) or VCC_IO	Slot:4	1.8V	1.8V or 3.3V
VCC_IO	DCDC	Slot:4	3.3V	3.3V
Reset		50mS		

IO PowerDomain	Voltage＝3.3V	Voltage＝1.8V
VCCIO0	3.3V (Default) PMUIO	Support
VCCIO1	3.3V (Default) LCDC	Support
VCCIO2	Support	1.8V (Default) I2S0
VCCIO3	Support	1.8V (Default) eMMC
VCCIO4	Support	1.8V (Default) WiFi(SDIO)
VCCIO5	3.3V (Default) SDMMC	Support

Power Diagram and Sequence

Scheme3:
5V IN With 1Cell Battery
REF Select about <POWER&USB PORT>

26.USB Port for RK816-3(OPT3)

27.RK816-3 With 1Cell BAT(OPT3)

RK816-3

5V 2AMPER

UAB Adapter

Input 5V/2A

5V/2A

Battery 3.7V

3.7V PIL

VCC1	BUCK1	→ VDD_ARM → RK3308 ARM Core
VCC2	BUCK2	→ VDD_LOG
VCC3	BUCK4	→ VCC_DDR
VCC4	BUCK3	→ VCC_IO

Default VDD_1V0 → RK3308 PLLAVDD_1V0,
RK3308 USB_DVDD_1V0

RK3308 Logic
RK3308 DDR PHY
DDR Device

RK3308 USB_AVDD_3V3
RK3308 VCCIO0& VCCIO1& VCCIO5 PowerDomain
TF Card
SPDIF OUT/IN Port
LCM 3.3V Supply
WiFI Module VBAT
RTL8201F
PA:XA8326

Power Manger VCC_SYS

LDO1 VCC_1V8_CODEC → RK3308 CODEC_AVDD_1V8

LDO2 VCC_1V8 → RK3308 PLL_AVDD_1V8
RK3308 USB_AVDD_1V8
RK3308 SARADC_AVDD_1V8
RK3308 OTP_AVDD_1V8

VCC5

1.8V Default → RK3308 VCCIO2 PowerDomain
3.3V Option → RK3308 VCCIO4 PowerDomain
VCCIO_WIFI
1.8V Option → RK3308 VCCIO3 PowerDomain
3.3V Default → eMMC or FLASH Nand VCCQ
RK3308 AVDD_CODEC_3V3

LDO3

Option VDD_10 → RK3308 C/DPLL_DVDD_1V0,A/GPLL_DVDD_1V0
RK3308 USB_DVDD_1V0

Gas Gauge

VCC6

LDO4 VCCIO_SD → Reserve for VCCIO_SDMMC
LDO5 VCCIO_3V3 → Reserve for VCC_3V3_CODEC
LDO6 → Reserve

Boost

Current limiting IC — 5V → USB0 OTG

BOOST → Current limiting IC — 5V → USB0 HOST

BOOST → PA:CS8509E

IO PowerDomain	Voltage=3.3V	Voltage=1.8V
VCCIO0	3.3V（Default）PMUIO	Support
VCCIO1	3.3V（Default）	Support
VCCIO2	Support	1.8V（Default）
VCCIO3	3.3V（Default）	Support
VCCIO4	Support	1.8V（Default）SDIO
VCCIO5	3.3V（Default）SDMMC	Support

RK3308 Part-L

RK3308 Part-N
RK3308 Part-M

RK3308 ARM CPU GUC

Part-L (U1000L)

ARM

VDD_CORE — Trace>60mil(Max 1.5A)

Signal	Pin
CORE_VDD_1	N6
CORE_VDD_2	N7
CORE_VDD_3	N8
CORE_VDD_4	P5
CORE_VDD_5	P6
CORE_VDD_6	P7
CORE_VDD_7	R5
CORE_VDD_8	R6
CORE_VDD_9	R8

Logic

VDD_LOG — Trace>30mil(Max 0.5A)

Signal	Pin
LOGIC_VDD_1	F10
LOGIC_VDD_2	F11
LOGIC_VDD_3	F12
LOGIC_VDD_4	G10
LOGIC_VDD_5	G11
LOGIC_VDD_6	G12

U1000L
RK3308
BGA355_52R00x52R00x44R00

VDD_CORE

C1000	C1002	C1003	C1004	C1001
22uF	100nF	100nF	100nF	DNP
X5R	X5R	X5R	X5R	4.7uF
6.3V	16V	16V	16V	X5R
C0603	C0402	C0402	C0402	10V
				C0402

VDD_LOG

C1006	C1007	C1008	C1009
10uF	100nF	100nF	DNP
X5R	X5R	X5R	4.7uF
6.3V	16V	16V	X5R
C0603	C0402	C0402	10V
			C0402

Note:All the Power filter capacitors should be placed close to the power pins of RK3308

Part-M (U1000M)

Pin	Signal	Signal	Pin
A1	VSS_1	VSS_26	F14
A4	VSS_2	VSS_27	F15
A9	VSS_3	VSS_28	F16
B8	VSS_4	VSS_29	G8
B11	VSS_5	VSS_30	G9
C4	VSS_6	VSS_31	G13
C6	VSS_7	VSS_32	G14
C7	VSS_8	VSS_33	E18
C11	VSS_9	VSS_34	H7
D2	VSS_10	VSS_35	H8
E1	VSS_11	VSS_36	H9
E5	VSS_12	VSS_37	H10
E9	VSS_13	VSS_38	H11
F2	VSS_14	VSS_39	H12
G3	VSS_15	VSS_40	H13
J5	VSS_16	VSS_41	J7
K1	VSS_17	VSS_42	J8
K3	VSS_18	VSS_43	J9
L5	VSS_19	VSS_44	J10
D11	VSS_20	VSS_45	J11
D12	VSS_21	VSS_46	J12
E11	VSS_22	VSS_47	J13
E12	VSS_23	VSS_48	K7
E13	VSS_24	VSS_49	K8
F13	VSS_25	VSS_50	K9

U1000M
RK3308
BGA355_52R00x52R00x44R00

Part-N (U1000N)

Pin	Signal	Signal	Pin
K10	VSS_51	VSS_79	M14
K11	VSS_52	VSS_80	M15
K12	VSS_53	VSS_81	N9
K13	VSS_54	VSS_82	N10
K14	VSS_55	VSS_83	N11
K15	VSS_56	VSS_84	N12
K16	VSS_57	VSS_85	N13
K17	VSS_58	VSS_86	N14
L7	VSS_59	VSS_87	N15
L8	VSS_60	VSS_88	P8
L9	VSS_61	VSS_89	P9
L10	VSS_62	VSS_90	P10
L11	VSS_63	VSS_91	P11
L12	VSS_64	VSS_92	P12
L13	VSS_65	VSS_93	P13
L14	VSS_66	VSS_94	P14
L15	VSS_67	VSS_95	P15
L16	VSS_68	VSS_96	A20
M4	VSS_69	VSS_97	C13
M5	VSS_70	VSS_98	C17
M6	VSS_71	VSS_99	D20
M7	VSS_72	VSS_100	H17
M8	VSS_73	VSS_101	N1
M9	VSS_74	VSS_102	R7
M10	VSS_75	VSS_103	R14
M11	VSS_76	VSS_104	T7
M12	VSS_77	VSS_105	U17
M13	VSS_78	VSS_106	Y1

U1000N
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-A

RK3308 ARM PC KRISTAL 24mHz

OSC

XOUT_24M — E20 — 1 R1100 2 22R 5% R0402

Y1100
3 X2 GND 2
4 GND X1 1
24MHz
CRY4_3R20X2R50X0R80

C1100 15pF C0G 50V C0402
C1101 15pF C0G 50V C0402

XIN_24M — E19

If share clk source with WiFi, Accuracy <= 10ppm. Otherwise <=20ppm for Independent crystal design

NPOR/WIFI CLK
Fix 1.8V

C1102 2 | 1 100nF C0402 16V X5R

NPOR_u — B20 — RESET

NPOR_BYPASS_d — C19

R1107 10K R0402 5%
1 2 VCC_1V8

REF_CLKOUT_d — C20 — REF_CLK_OUT

TVSS — D19

PLL

VDD_1V0

PLL_AVDD_1V0 — E15

C1104 100nF X5R 16V C0402

VCC_1V8

PLL_AVDD_1V8 — E17

C1105 100nF X5R 16V C0402

PLL_VSS — G15

U1000A
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-K
RK3308 ARM PC/TABLET

DDR

U1000K
RK3308
BGA355_52R00x52R00x44R00

Pin	Signal		Signal	Pin	Net
J4	DDR_DQ0		DDR_A0	B4	DDR_A0
G5	DDR_DQ1		DDR_A1	A5	DDR_A1
H4	DDR_DQ2		DDR_A2	A3	DDR_A2
L1	DDR_DQ3		DDR_A3	E6	DDR_A3
E2	DDR_DQ4		DDR_A4	B7	DDR_A4
F1	DDR_DQ5		DDR_A5	B3	DDR_A5
E3	DDR_DQ6		DDR_A6	A6	DDR_A6
K2	DDR_DQ7		DDR_A7	A2	DDR_A7

DDR_D0, DDR_D1, DDR_D2, DDR_D3, DDR_D4, DDR_D5, DDR_D6, DDR_D7

DDR_DM0 — G1 — DDR_DM0

DDR_DQS0P — J3 — DDR_DQS0P
DDR_DQS0N — K4 — DDR_DQS0N

Pin	Signal		Signal	Pin	Net
			DDR_A8	A10	DDR_A8
			DDR_A9	E7	DDR_A9
			DDR_A10	C9	DDR_A10
			DDR_A11	B5	DDR_A11
			DDR_A12	B6	DDR_A12
			DDR_A13	D7	DDR_A13
			DDR_A14	B10	DDR_A14

Pin	Signal		Signal	Pin	Net
F4	DDR_DQ8		DDR_BA0	B2	DDR_BA0
G2	DDR_DQ9		DDR_BA1	C8	DDR_BA1
L4	DDR_DQ10		DDR_BA2	D6	DDR_BA2
D3	DDR_DQ11				
L2	DDR_DQ12		DDR_CS0N	B1	DDR_CS0N
F3	DDR_DQ13				
M2	DDR_DQ14		DDR_ODT0	C5	DDR_ODT0
K5	DDR_DQ15				

DDR_D8, DDR_D9, DDR_D10, DDR_D11, DDR_D12, DDR_D13, DDR_D14, DDR_D15

DDR_DM1 — L3 — DDR_DM1

DDR_DQS1P — H2 — DDR_DQS1P
DDR_DQS1N — H3 — DDR_DQS1N

Signal	Pin	Net
DDR_CLK	C3	DDR_CLKP
DDR_CLKN	C2	DDR_CLKN
DDR_CKE	B9	DDR_CKE0
DDR_RASN	D5	DDR_RASN
DDR_CASN	D8	DDR_CASN
DDR_WEN	E8	DDR_WEN
DDR_RESET	E4	DDR_RESET

VCC_DDR — J6 — DDR_VDD_1
H6 — DDR_VDD_2
G6 — DDR_VDD_3
F7 — DDR_VDD_4
F8 — DDR_VDD_5
F9 — DDR_VDD_6
E10 — DDR_VDD_7

FP_1 — F5
FP_2 — F6
FP_3 — D10

Note: Reserver for RK3308G

VCC_DDR

R1200
DNP
1K
1%
R0402

C1215
DNP
1nF
C0402
X5R
50V

R1201
DNP
1K
1%
R0402

Power Filter

VCC_DDR

C1208	C1210	C1211	C1209	C1216
10uF	100nF	100nF	DNP	DNP
C0603	C0402	C0402	100nF	4.7uF
X5R	X5R	X5R	C0402	X5R
6.3V	16V	16V	X5R	10V
			16V	C0402

Note:All the Power filter capacitors should be
placed close to the power pins of RK3308

RK3308 Part-E

NAND FLASH/eMMC/SFC/SPI

Pin	Signal
U11	GPIO3_A0/FLASH_D0/EMMC_D0/SFC_SIO0_u → FLASH_D0
V12	GPIO3_A1/FLASH_D1/EMMC_D1/SFC_SIO1_u → FLASH_D1
Y12	GPIO3_A2/FLASH_D2/EMMC_D2/SFC_WP_SIO2_u → FLASH_D2
Y11	GPIO3_A3/FLASH_D3/EMMC_D3/SFC_HOLD_SIO3_u → FLASH_D3
W11	GPIO3_A4/FLASH_D4/EMMC_D4/SFC_CLK_u → FLASH_D4/SFC_CLK
V11	GPIO3_A5/FLASH_D5/EMMC_D5/SFC_CSN0_u → FLASH_D5/SFC_CS0
U10	GPIO3_A6/FLASH_D6/EMMC_D6_u → FLASH_D6
U12	GPIO3_A7/FLASH_D7/EMMC_D7_u → FLASH_D7
V13	GPIO3_B0/FLASH_WRN/EMMC_CMD_u → FLASH_WRN/EMMC_CMD
T13	GPIO3_B1/FLASH_CLE/EMMC_CLK_d → FLASH_CLE/EMMC_CLK
U13	GPIO3_B2/FLASH_RDN/SPI1_MISO_u → FLASH_RDN
R10	GPIO3_B3/FLASH_ALE/EMMC_PWREN/SPI1_CLK_d → FLASH_ALE/EMMC_RST
W12	GPIO3_B4/FLASH_RDY/I2C3_SDA_M1/SPI1_MOSI/UART3_RX_u → FLASH_RDY
T12	GPIO3_B5/FLASH_CSN0/I2C3_SCL_M1/SPI1_CSN0/UART3_TX_u → FLASH_CS0N

VCCIO_FLASH

R12 VCCIO3

C1300
100nF
X5R
16V
C0402

U1000E
RK3308
BGA355_52R00x52R00x44R00

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK3308_AI-VA_MB_REF
File:	13.RK3308 FLASH Controller
Date:	Wednesday, July 04, 2018
Designed by:	Joseph

Rev: 1.1

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RK3308 Part-I

USB2.0

USB0_DM	A13	USB_OTG_DM
USB0_DP	B13	USB_OTG_DP
USB_VBUS	C14	USB_DET
USB_ID	C12	USB_OTG_ID
USB1_DM	A12	USB_HOST_DM
USB1_DP	B12	USB_HOST_DP

USB_EXTR   C15   R1400 1   133R   2   1%   R0402

USB_AVDD_3V3_1   D13
USB_AVDD_3V3_2   E14

VCC_IO

C1400
100nF
X5R
16V
C0402

USB_AVDD_1V8   D16

USB_VDD_1V8   VCC_1V8

C1401
100nF
X5R
16V
C0402

R1401 1   1R   5%   2   R0402

USB_VDD_1V0   VDD_1V0

USB_VDD_1V0   D15

C1402
100nF
X5R
16V
C0402

R1403 1   1R   5%   2   R0402

U1000I
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-J

SARADC

ADC_IN0	A19 → TP6001 TP_0.7
ADC_IN1	B19 → ADC_KEY_IN1
ADC_IN2	C18 → BAT_DET
ADC_IN3	A18 → ADC_HW_ID1 TP1500 TP_0.7
ADC_IN4	B18
ADC_IN5	D18 → CHG_DET

SADC_AVDD_1V8 D17

VCC_1V8

C1500
100nF
X5R
16V
C0402

OTP

OTP_VCC_1V8 E16

U1000J
RK3308
BGA355_52R00x52R00x44R00

ADC_KEY_IN1

C1503
1nF
C0402
X5R
50V

Note:C1503 should be placed
close to the B19 pin of RK3308

HW ID

ADC_HW_ID	Pull-up Resistance	Pull-down Resistance	ADC Value
BOM0	51K	DNP	1024
BOM1	51K	51K	512
BOM2	51K	22K	308

VCC_1V8

R1501
51K
1%
R0402

ADC_HW_ID1

R1503
51K
1%
R0402

C1502
100nF
X5R
16V
C0402

RK3308 Part-C

LCDC/I2S1_8CH/PDM_8CH/MAC

GPIO1_A0/LCDC_DCLK_d	Y5	LCDC_CLK
GPIO1_A1/LCDC_HSYNC_d	V4	LCDC_HSYNC
GPIO1_A2/LCDC_VSYNC/I2S1_8CH_MCLK_M0_d	U4	LCDC_VSYNC
GPIO1_A3/LCDC_DEN/I2S1_8CH_SCLK_TX_M0_d	W4	LCDC_DEN/I2S1_SCLK_TX_M0
GPIO1_A4/LCDC_D0/I2S1_8CH_SCLK_RX_M0/PDM_8CH_CLK_M0_d	W5	LCDC_D0
GPIO1_A5/LCDC_D1/I2S1_8CH_LRCK_TX_M0_d	V5	LCDC_D1/I2S1_LRCK_TX_M0
GPIO1_A6/LCDC_D2/I2S1_8CH_LRCK_RX_M0_d	U5	LCDC_D2
GPIO1_A7/LCDC_D3/I2S1_8CH_SDO0_M0_d	W6	LCDC_D3/I2S1_SDO0_M0
GPIO1_B0/LCDC_D4/I2S1_8CH_SDO1_SDI3_M0/PDM_8CH_SDI3_M0_d	V6	LCDC_D4
GPIO1_B1/LCDC_D5/I2S1_8CH_SDO2_SDI2_M0/PDM_8CH_SDI2_M0_d	U6	LCDC_D5
GPIO1_B2/LCDC_D6/I2S1_8CH_SDO3_SDI1_M0/PDM_8CH_SDI1_M0_d	T6	LCDC_D6
GPIO1_B3/LCDC_D7/I2S1_8CH_SDI0_M0/PDM_8CH_SDI0_M0_d	U7	LCDC_D7/I2S1_SDI0_M0
GPIO1_B4/LCDC_D8/I2S1_8CH_MCLK_M1/MAC_CLK_d	V7	LCDC_D8/MAC_CLK
GPIO1_B5/LCDC_D9/I2S1_8CH_SCLK_TX_M1/MAC_MDC_d	T8	LCDC_D9/MAC_MDC
GPIO1_B6/LCDC_D10/I2S1_8CH_SCLK_RX_M1/PDM_8CH_CLK_M1/MAC_MDIO_d	W7	LCDC_D10/MAC_MDIO
GPIO1_B7/LCDC_D11/I2S1_8CH_LRCK_TX_M1/MAC_RXER_d	Y7	LCDC_D11/MAC_RXER
GPIO1_C0/LCDC_D12/I2S1_8CH_LRCK_RX_M1/MAC_RXDV_d	V9	LCDC_D12/MAC_RXDV
GPIO1_C1/LCDC_D13/I2S1_8CH_SDO0_M1/MAC_TXEN_d	V8	LCDC_D13/MAC_TXEN
GPIO1_C2/LCDC_D14/I2S1_8CH_SDO1_SDI3_M1/PDM_8CH_SDI3_M1/MAC_TXD0_d	U8	LCDC_D14/MAC_TXD0
GPIO1_C3/LCDC_D15/I2S1_8CH_SDO2_SDI2_M1/PDM_8CH_SDI2_M1/MAC_TXD1_d	U9	LCDC_D15/MAC_TXD1
GPIO1_C4/LCDC_D16/I2S1_8CH_SDO3_SDI1_M1/PDM_8CH_SDI1_M1/MAC_RXD0_d	R9	LCDC_D16/MAC_RXD0
GPIO1_C5/LCDC_D17/I2S1_8CH_SDI0_M1/PDM_8CH_SDI0_M1/MAC_RXD1_d	Y9	LCDC_D17/MAC_RXD1

TP1600
TP_0.7

TP1601
TP_0.7

Remind:
Reserve two point for Jtag Debug

UART/SPI2/JTAG/I2C0

GPIO1_C6/UART1_CTSN/UART2_RX_M0/SPI2_MISO/JTAG_TCK_u	W9	SPI2_RX/UART2_RX_M0
GPIO1_C7/UART1_RTSN/UART2_TX_M0/SPI2_MOSI/JTAG_TMS_u	T9	SPI2_TX/UART2_TX_M0
GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK_u	V10	SPI2_CLK
GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0_u	T10	SPI2_CS

VCC_IO

VCCIO1 R11

C1601
100nF
C0402
16V
X5R

U1000C
RK3308
BGA355_52R00x52R00x44R00

Correspondence between LCDC DATA and RGB

LCDC	18bit Panel	24bit Panel
LCDC_D0	B0	B2
LCDC_D1	B1	B3
LCDC_D2	B2	B4
LCDC_D3	B3	B5
LCDC_D4	B4	B6
LCDC_D5	B5	B7
LCDC_D6	G0	G2
LCDC_D7	G1	G3
LCDC_D8	G2	G4
LCDC_D9	G3	G5
LCDC_D10	G4	G6
LCDC_D11	G5	G7
LCDC_D12	R0	R2
LCDC_D13	R1	R3
LCDC_D14	R2	R4
LCDC_D15	R3	R5
LCDC_D16	R4	R6
LCDC_D17	R5	R7

RK3308 Part-F

SDIO

GPIO4_A0/SDIO_D0_u	J19	SDIO_D0
GPIO4_A1/SDIO_D1_u	J17	SDIO_D1
GPIO4_A2/SDIO_D2_u	G18	SDIO_D2
GPIO4_A3/SDIO_D3_u	G17	SDIO_D3
GPIO4_A4/SDIO_CMD_u	H18	SDIO_CMD

GPIO4_A5/SDIO_CLK_d J18 R1700 1 2 22R 5% R0402 SDIO_CLK

UART4

GPIO4_A6/UART4_CTSN_u	K19	UART4_CTS
GPIO4_A7/UART4_RTSN_u	K18	UART4_RTS
GPIO4_B0/UART4_RX_u	F17	UART4_RXD
GPIO4_B1/UART4_TX_u	J16	UART4_TXD
GPIO4_B2_d	G16	HOST_WAKE_BT
GPIO4_B3_d	F19	BT_REG_ON

I2S0_2CH

GPIO4_B4/I2S0_2CH_MCLK_d	H16	BT_WAKE_HOST
GPIO4_B5/I2S0_2CH_SCLK_d	F18	PCM_CLK
GPIO4_B6/I2S0_2CH_LRCK_TX_d	J15	PCM_SYNC
GPIO4_B7/I2S0_2CH_SDO_d	H15	PCM_OUT
GPIO4_C0/I2S0_2CH_SDI_d	H14	PCM_IN

VCCIO4 J14

VCCIO_SDIO

C1700
100nF
X5R
16V
C0402

U1000F
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-G

SDMMC/UART2

GPIO4_D0/SDMMC_D0_u	B17	SDMMC_D0
GPIO4_D1/SDMMC_D1_u	A17	SDMMC_D1
GPIO4_D2/SDMMC_D2/UART2_RX_M1_u	B15	SDMMC_D2/UART2_RX_M1
GPIO4_D3/SDMMC_D3/UART2_TX_M1_u	A15	SDMMC_D3/UART2_TX_M1
GPIO4_D4/SDMMC_CMD_u	C16	SDMMC_CMD

GPIO4_D5/SDMMC_CLK_d B16 R1712 1 22R 5% 2 R0402 SDMMC_CLK

GPIO4_D6/SDMMC_PWREN_d B14 SDMMC_PWREN

VCCIO5 D14

VCCIO_SDMMC

C1701
100nF
X5R
16V
C0402

U1000G
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-B

U1000B

Pin	Signal		Net
N3	GPIO0_A0/SDIO_INTN_d		WIFI_WAKE_HOST
N4	GPIO0_A1/SDIO_WRPT_d		PHONE_CTL
P3	GPIO0_A2/SDIO_PWREN_d		WIFI_REG_ON
P4	GPIO0_A3/SDMMC_DET_u		SDMMC_DET
R3	GPIO0_A4/TEST_CLKOUT_u		FLASH_SEL/LCD_PWREN

NOTE: PIN R3 Default   1:VCCIO_FLASH=1.8V
as FLASH_SEL Function   0:VCCIO_FLASH=3.3V

R1802 1   2.2K2   5%   R0402

VCCIO_FLASH	VCCIO_FLASH =1.8V	VCCIO_FLASH =3.3V
R1802	DNP	2.2K

Pin	Signal		Net
R4	GPIO0_A5_d		SPK_MUTE
T5	GPIO0_A6_d		PWR_KEY/PMIC_INT
T4	GPIO0_A7_d		PWR_HOLD
T3	GPIO0_B0_d		MIC_LED_EN
Y3	GPIO0_B1/PMIC_SLEEP_d		POWER_SLEEP
U3	GPIO0_B2/TSADC_SHUT_d		TSADC_SHUT/MAC_RST
V2	GPIO0_B3/I2C1_SDA_u		I2C1_SDA
V1	GPIO0_B4/I2C1_SCL_u		I2C1_SCL
V3	GPIO0_B5/PWM0_d		CORE_DVS
W2	GPIO0_B6/PWM1_d		LCD_BL
W1	GPIO0_B7/PWM2/I2C3_SDA_M0_d		SD_CTRL
U2	GPIO0_C0/PWM3/I2C3_SCL_M0_d		IR_RX/PA_DRV
Y2	GPIO0_C3/RTC_CLK		CLK_32K_OUT
T2	GPIO0_C4_d		LCD_RST
N2	GPIO0_C5/OTG_DRVBUS_d		USB_DRV

Remind:According to actual product application
Select a function.
if need both function,MAC_RSTselect other GPIO

Remind:According to actual product application
Select a function.
if need both function,PA_DRV select other GPIO

SPDIF

Pin	Signal		Net
T1	GPIO0_C1/SPDIF_TX_d		SPDIF_TX
W3	GPIO0_C2/SPDIF_RX_d		SPDIF_RX

VCCIO0   N5

VCC_IO
C1800
100nF
X5R
16V
C0402

U1000B
RK3308
BGA355_52R00x52R00x44R00

TSADC

VCC_IO

R1800   R1801
2.2K   2.2K
5%   5%
R0402   R0402

I2C1_SDA
I2C1_SCL

RESET

TSADC_SHUT/MAC_RST   2 R1807 1 DNP 5% 1   Q1800
                        47K R0402   DNP
                                               S8050
                                               SOT_23

As TSADC_SHUT Funtion

RK3308 Part-D

U1000D

UART0/SPI0/I2C2

Pin	Signal		Net
U14	GPIO2_A0/UART0_RX/SPI0_MISO_u		SPI0_RX
V16	GPIO2_A1/UART0_TX/SPI0_MOSI_u		SPI0_TX
Y16	GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA_u		SPI0_CLK/I2C2_SDA
W16	GPIO2_A3/UART0_RTSN/SPI0_CSN0/I2C2_SCL_u		SPI0_CS/I2C2_SCL

I2S0_8CH/PDM_8CH

Pin	Signal		Net
T15	GPIO2_A4/I2S0_8CH_MCLK/PDM_8CH_CLK_M_M2_d		I2S0_MCLK
R15	GPIO2_A5/I2S0_8CH_SCLK_TX_d		I2S0_SCLK_TX
T16	GPIO2_A6/I2S0_8CH_SCLK_RX/PDM_8CH_CLK_S_M2_d		I2S0_SCLK_RX/PDM_CLK
V17	GPIO2_A7/I2S0_8CH_LRCK_TX_d		I2S0_LRCK_TX
R16	GPIO2_B0/I2S0_8CH_LRCK_RX_d		I2S0_LRCK_RX
V14	GPIO2_B1/I2S0_8CH_SDO0_d		I2S0_SDO0
V15	GPIO2_B2/I2S0_8CH_SDO1_d		I2S0_SDO1
U16	GPIO2_B3/I2S0_8CH_SDO2_d		I2S0_SDO2
T17	GPIO2_B4/I2S0_8CH_SDO3_d		I2S0_SDO3
T14	GPIO2_B5/I2S0_8CH_SDI0/PDM_8CH_SDI0_M2_d		I2S0_SDI0/PDM_SDI0
U15	GPIO2_B6/I2S0_8CH_SDI1/PDM_8CH_SDI1_M2_d		I2S0_SDI1/PDM_SDI1
W14	GPIO2_B7/I2S0_8CH_SDI2/PDM_8CH_SDI2_M2_d		I2S0_SDI2/PDM_SDI2
Y14	GPIO2_C0/I2S0_8CH_SDI3/PDM_8CH_SDI3_M2_d		I2S0_SDI3/PDM_SDI3

APIO2_VDD

R1811   R1812
DNP   DNP
2.2K   2.2K
5%   5%
R0402   R0402

SPI0_CLK/I2C2_SDA
SPI0_CS/I2C2_SCL

VCCIO2   T11

APIO2_VDD
C1801
100nF
X5R
16V
C0402

2 R1805 1 0R 5%
R0402   VCC_1V8

2 R1806 1 DNP 5%
          0R R0402   VCC_IO

U1000D
RK3308
BGA355_52R00x52R00x44R00

RK3308 Part-H

ACODEC

U1000H
RK3308
BGA355_52R00x52R00x44R00

CODEC_HPOUT_R	W18	HPOUT_R
CODEC_HPOUT_L	Y19	HPOUT_L
CODEC_LINEOUT_R	W19	LINEOUT_R
CODEC_LINEOUT_L	W20	LINEOUT_L
CODEC_HPDET	V18	PHONE_DET

| CODEC_LINE1 | T20 | LINE_IN1 |
| CODEC_LINE2 | T19 | LINE_IN2 |

CODEC_MICN1	V19	CODEC_MICN1	C1917	1	2	470nF C0402 X5R 10V	SPKL1_N
CODEC_MICP1	V20	CODEC_MICP1	C1919	1	2	470nF C0402 X5R 10V	SPKL1_P
CODEC_MICN2	U19	CODEC_MICN2	C1921	1	2	470nF C0402 X5R 10V	SPKR1_N
CODEC_MICP2	U20	CODEC_MICP2	C1922	1	2	470nF C0402 X5R 10V	SPKR1_P
CODEC_MICN3	P17	CODEC_MICN3	C1925	1	2	470nF C0402 X5R 10V	MICN3
CODEC_MICP3	P18	CODEC_MICP3	C1926	1	2	470nF C0402 X5R 10V	MICP3
CODEC_MICN4	R19	CODEC_MICN4	C1927	1	2	470nF C0402 X5R 10V	MICN4
CODEC_MICP4	R20	CODEC_MICP4	C1928	1	2	470nF C0402 X5R 10V	MICP4
CODEC_MICN5	P19	CODEC_MICN5	C1929	1	2	470nF C0402 X5R 10V	MICN5
CODEC_MICP5	P20	CODEC_MICP5	C1930	1	2	470nF C0402 X5R 10V	MICP5
CODEC_MICN6	M18	CODEC_MICN6	C1931	1	2	470nF C0402 X5R 10V	MICN6
CODEC_MICP6	N18	CODEC_MICP6	C1932	1	2	470nF C0402 X5R 10V	MICP6
CODEC_MICN7	N19	CODEC_MICN7	C1933	1	2	470nF C0402 X5R 10V	MICN7
CODEC_MICP7	N20	CODEC_MICP7	C1934	1	2	470nF C0402 X5R 10V	MICP7
CODEC_MICN8	M19	CODEC_MICN8	C1935	1	2	470nF C0402 X5R 10V	MICN8
CODEC_MICP8	M20	CODEC_MICP8	C1936	1	2	470nF C0402 X5R 10V	MICP8

C1907 4.7uF C0603 X5R 10V — R18 CODEC_VCM
C1910 4.7uF C0603 X5R 10V — T18 CODEC_VCMH

VCC_3V3_CODEC — P16 CODEC_AVDD_3V3
C1913 100nF X5R 16V C0402

VCC_1V8_CODEC — M17 CODEC_AVDD_1V8_1 / N17 CODEC_AVDD_1V8_2
C1918 4.7uF X5R 6.3V C0402

CODEC_AVSS_1	L17
CODEC_AVSS_2	L18
CODEC_AVSS_3	L19
CODEC_AVSS_4	L20
CODEC_AVSS_5	M16
CODEC_AVSS_6	N16
CODEC_AVSS_7	R17
CODEC_AVSS_8	Y20

CODEC_MICBIAS1 — Y18 — MICBIAS1
C1923 1uF C0402 X5R 6.3V

CODEC_MICBIAS2 — U18 — MICBIAS2
C1924 1uF C0402 X5R 6.3V

Application scene	MIC IN Channel	Loopback Channel
6MIC IN+ 2Speaker OUT	MIC3～MIC8	MIC1～MIC2
6MIC IN+ 1Speaker OUT	MIC3～MIC8	MIC1
4MIC IN+ 2Speaker OUT	MIC5～MIC8	MIC3～MIC4
4MIC IN+ 1Speaker OUT	MIC5～MIC8	MIC3
2MIC IN+ 1Speaker OUT	MIC7～MIC8	MIC5

12V IN Without Battery

12V DC IN

12V DCIN

J2000
DC-0007-5P

F2000
JK-SMD200L
F8050

VCC12V_DCIN

DC3_DC_0007_5P

D2000
SS32
DO_214AC

R2000
2R
5%
R1206

C2000
10uF
C0805
X5R
25V

C2001
2.2uF
C0805
X5R
25V

PowerAmplifier Power Supply

VCC12V_DCIN

R2001
0R   5%
R0805

VCC12V_PA

R0805
0R   5%
R2002

Play Together

12V to 5V BUCK

VCC12V_DCIN

C2003
10uF
C0805
X5R
25V

C2004
100nF
C0402
X5R
25V

R2003
10K
5%
R0402

U2000
SY8113B
SOT_23_6

4.5V<VIN<18V

5 VIN	LX 6
2 GND	BS 1
4 EN	FB/OUT 3

C2002
100nF
X5R 16V
C0402

L2000
3.3uH
IND_404030
3.3A 0.04ohm

5.1V/3A

R2004
75K
1%
R0402

R2006
10K
1%
R0402

C2005
100pF
C0402
C0G
50V

C2006
22uF
C0805
X5R
16V

C2007
10uF
C0805
X5R
16V

C2008
100nF
C0402
X5R
16V

R2005
3.3K
5%
R0402

LED2000
LED_RED
LED0603

VCC5V0_SYS

12V IN With 2Cell Battery

12V DC IN

12V DCIN
J2100 DC-0007-5P
DC3_DC_0007_5P
F2100 JK-SMD200L F8050
VCC12V_DCIN
R2102 2R 5% R1206
D2100 SS32 DO_214AC
C2105 10uF C0805 X5R 25V
C2107 2.2uF C0805 X5R 25V

Battery

BT2100
BAT3_2R54
VCC_BAT
NTC
R2117 10K DNP 5% R0402
C2117 10uF C0805 16V X5R
R2115 390K 1% R0402
R2119 100K 1% R0402
C2118 100nF C0402
BAT_DET

PCB Note:
Double cell battery

POWER Control

VCC_IO
VCC_IN
VCC12V_DCIN
SW2100 Power ON SMT2_6R00X3R50X4R20
ED2100 ESD5451N ESD0402
R2126 10K 5% R0402
As PWR_KEY Funtion
PWR_KEY/PMIC_INT
Q2106 S8050 SOT_23
R2131 47K 5% R0402
R2133 47K 5% R0402
R2134 47K 5% R0402
PWR_HOLD
D2104 BAT54C SOT_23
R2132 10K 5% R0402
D2103 B5819WS SOD_323
R2130 150K 5% R0402
R2135 100K 5% R0402
VSYS_EN

Charger IC

VCC12V_DCIN
Q2100 WNM3003-3/TR SOT_23
Q2101 WNM3003-3/TR SOT_23
VDC
Rac R2100 0.01R 1% R1206
VCC_IN
C2101 22uF C0805 X5R 25V
C2100 1nF C0402 X5R 50V
R2101 1M R0402
R2105 4.7K 5% R0402
R2106 4.7K 5% R0402
C2102 100nF X5R 25V C0402
C2103 100nF C0402 X5R 25V
C2104 22uF C0805 X5R 16V
R2103 5% 22K R0402
R2104 5% 1K R0402
Q2102 WPM3407-3/TR SOT_23
D2101 SS32 DO_214AC
C2106 22uF C0805 X5R 16V
L2100 IND_606028 3.3uH 4.15A 0.025ohm
Rsr R2109 0.01R 1% R1206
VCC_BAT
C2109 10uF X5R 16V C0805
R2107 1M 5% R0402
VREF
R2110 220K R0402 5%
R2108 220K R0402 1%
C2110 1uF C0402 X5R 10V
C2108 47nF X5R 25V C0402
C2603 1uF X5R 16V
R2112 100K 5% R0402
R2113 27K 5% R0402
R2111 27K R0402 1%
C2112 100nF C0402 X5R 16V
C2111 100nF C0402 X5R 16V
VCC_1V8
R2114 10R 5% R0402
R2116 4.99K 1% R0402
VREF
C2115 100nF C0402 X5R 16V
C2116 1uF C0402 X5R 25V
C2113 100nF C0402 X5R 16V
C2114 100nF C0402 X5R 16V
R2118 10K 5% R0402
R2120 30K 5% R0402
NTC
CHG_DET

U2100 BQ24133 QFN24_5R65X3R65X1R00_T
ACP ACN CMSRC ACDRV VREF PVCC_1 PVCC_2 SW_1 SW_2 BATDRV BTST REGN ISET1 PGND_1 PGND_2 SRP SRN CELL VACSET AVCC OVPSET TTC TS STAT PWRPAD

VREF=3.3V
Idpm=Vacset/(20*Rac)
Icharge=Viset/(20*Rsr)
Iprecharge=Viset/(200*Rsr)
Iterm=Viset/(200*Rsr)
Tttc=Cttc*Kttc(Kttc=5.6min/nF)
If Vovpset above 1.6V or below 0.5V,charge is disabled.

VCC_IN to 5V BUCK

VCC_IN
4.5V<VIN<18V
U2103 SY8113B SOT_23_6
VIN LX GND BS EN FB/OUT
VSYS_EN
C2139 10uF C0805 X5R 25V
C2140 100nF C0402 X5R 25V
C2136 100nF X5R 16V C0402
L2103 3.3uH IND_404030 3.3A 0.04ohm
R2139 75K 1% R0402
C2141 100pF C0402 C0G 50V
C2142 22uF C0805 X5R 16V
C2143 10uF C0805 X5R 16V
C2144 100nF C0402 X5R 25V
R2140 3.3K 5% R0402
R2142 10K 5% R0402
VCC5V0_SYS
5.1V/3A
LED2100 LED_RED LED0603

PowerAmplifier Power Supply

VCC_IN
Q2107 WPM3401-3/TR SOT_23
L2102 4.7uH 2.35A IND_404200.075ohm
U2104 SY7203DBC DFN10_3R00X3R00X0R80_T
IN LX1 LX2 OVP NC1 NC2 NC3 NC4 EN GND2 FB
D2105 SS32 DO_214AC
VCC12V_PA
C2134 100nF X5R 16V C0402
R2136 100K 5% R0402
R2138 10K 5% R0402
R2135 47K 5% R0402
Q2108 S8050 SOT_23
C2145 10uF X5R 25V C0805
R2137 909K 1% R0402
C2137 22pF C0402 C0G 50V
C2135 10uF C0805 X5R 25V
C2138 100nF C0402 X5R 25V
R2143 15K 1% R0402
FB:0.2V
IR_RX/PA_DRV
PA_DRV

VDD_ARM

ETA3409A/CS4175-E:1.0uH/2A
SY8089AAAC:2.2uH/2A

V=Vmax-(Vmax-Vmin)*Duty
Default 1.015V
0.827-1.34V

VDD_CORE
Feedback from RK3308

Default down

VDD_LOG

ETA3409A/CS4175-E:1.0uH/2A
SY8089AAAC:2.2uH/2A

Default 1.04V

VDD_1V0

Note:
Default : VDD_1V0 Power Supply from VDD_LOG

VCC_DDR

Default 1.5V

DDR Type	VCC_DDR Voltage	R2217	R2218
DDR3	1.5V	150K	100K
DDR3L	1.35V	150K	120K
DDR2	1.8V	200K	100K
LPDDR2	1.2V	100K	100K

VCC_IO

Default 3.3V

VCC_1V8

Layout Note:The power of VCC_1V8
must be according to star topology to each load

VCCIO_FLASH

	FLASH_SEL (Pin R3 of RK3308)	VCCIO_FLASH
eMMC	H	1.8V
eMMC	L	3.3V
Nand Flash	H	1.8V
Nand Flash	L	3.3V (Default)

VCCIO_SDIO

SDIO2.0/3.0	SDIO2.0	SDIO3.0
VCCIO_SDIO	3.3V	1.8V

VCC_1V8_CODEC

Layout Note:
The power of VCC_1V8 must be according to star topology to each load.
VCC_1V8_CODEC should route from the source of VCC_18.

VCC_1V8_CODEC
(PIN MI7&NI7 of RK3308)
Output of LDO U2205:
The source of the power of VCC_1v8
Star topology to each load.
other loads

VCC_3V3_CODEC

Layout Note:
The power of VCC_IO must be according to star topology to each load.
VCC_3V3_CODEC should route from the source of VCC_IO.

VCC_3V3_CODEC
(PIN P16 of RK3308)
Output of DCDC U2204:
The source of the power of VCC_IO
Star topology to each load.
other loads

VCCIO_SDMMC

Option1(Default):
Only support SDMMC 2.0

Option2:
From Discrete LDO
Support SDMMC 3.0& SDMMC 2.0

SDIO2.0 H, 3.3V
SDIO3.0 L, 1.792V

ROCKCHIP 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3308_AI-VA_MB_REF
File: 22.Discrete Power(OPT1&OPT2)
Date: Wednesday, July 04, 2018
Designed by: Joseph
Rev: 1.1
Sheet: 21 of 51

USB OTG

USB_DET
USB_OTG_ID
USB_OTG_DM
USB_OTG_DP

VCC_IO
VCC5V0_SYS
VCC5V0_OTG

U2500
SY6280AAC
/TT9107/CW3031

R2500
100K
5%
R0402

IN VOUT
GND
EN OCB
SOT_23_5

R2504
4.7K
5%
R0402

USB_OTG_ID
R2511 5%
560K R0402
Q2500
S8050
SOT_23
C2501
1uF
C0402
X5R
10V

VCC5V0_OTG

U2500
USB20_micro
J2500
USB20Micro5_MU05_10MGF_T

VUSB
DM
DP
ID
GND

OTG_DM
OTG_DP

R2510 5%
100R R0402
USB_OTG_ID

R2502 1 2.2R 2 R0402 5% USB_OTG_DM

FB2500
90R-100M 4   3 DNP L0603D

R2505 1 2.2R 2 R0402 5% USB_OTG_DP

ED2502
ESD5451N
ESD0402

ED2500
ESD5451N
ESD0402

U2501
ESD5302F
SOT_23

Cj<3pF

2 R2501 5% 1 USB_DET
10K R0402

R2503
18K
1%
R0402

C2502
10uF
X5R
10V
C0603

C2500
100nF
X5R
16V
C0402

USB HOST

USB_HOST_DP
USB_HOST_DM

USB_DRV

VCC5V0_SYS

U2502
SY6280AAC
/TT9107/CW3031

VCC5V0_HOST

IN VOUT
GND
EN OCB
SOT_23_5

C2505
1uF
C0402
X5R
10V

USB_DRV

R2509
4.7K
5%
R0402

USB-HUB_PORTBA
USB2500
USB20A4_USB_AF_01_001

HOST_DM
HOST_DP

R2507 1 2.2R 2 5% R0402 USB_HOST_DM

FB2501 4   3 DNP L0603D
2   1 90R-100M

R2508 1 2.2R 2 5% R0402 USB_HOST_DP

U2503
ESD5302F
SOT_23

Cj<3pF

VCC5V0_HOST

ED2501
ESD5451N
ESD0402

C2504
22uF
C0805
X5R
16V

C2503
100nF
C0402
X5R
16V

USB OTG

USB_DET
USB_OTG_ID
USB_OTG_DM
USB_OTG_DP

VCC_RK816IN

VCC_RK816IN

USB20_micro
J2600
USB20Micro5_MU05_10MGF_T

VUSB
DM
DP
ID
GND

G3 G4
G2 G1

OTG_DM_1
OTG_DP_1
USB_OTG_ID

R2602 5%
100R R0402

R2601 2.2R R0402 5% USB_OTG_DM

FB2600 DNP
90R-100M L0603D

R2604 2.2R R0402 5% USB_OTG_DP

ED2600
ESD5451N
ESD0402

R2600 5%
10K R0402 USB_DET

C2601
10uF
X5R
10V
C0603

R2603
18K
1%
R0402

C2600
100nF
X5R
16V
C0402

R2611
3.3K
5%
R0402
LED2102
LED_RED
LED0603

ED2601
ESD5451N
ESD0402

U2600
ESD5302F
SOT_23

Cj<3pF

USB HOST

USB_HOST_DP
USB_HOST_DM
USB_DRV

BOOST+Limit Switch

VCC_SYS

L2600
2.2uH
IND_404026
2.10A
0.04ohm

D2600
SS32
DO_214AC

U2603
SY6280AAC
/TT9107/CW3031
SOT_23_5

VCC5V0_HOST

C2602
4.7uF
C0603
X5R
10V

R2605
10K
R0402
5%

U2601
SY7208/TCS9208
SOT_23_6

VIN LX
EN NC
GND FB

R2606
360K
R0402
1%

C2603
22pF
C0402
C0G
50V

C2604
10uF
C0603
X5R
10V

C2605
100nF
C0402
X7R
16V

IN VOUT
GND
EN OCB

USB_DRV

R2610
4.7K
5%
R0402

FB:0.6V

R2609
47K
R0402
1%

USB-HUB_PORTBA
USB2600
USB20A4_USB_AF_01_001

VCC5V0_HOST

HOST_DM_1
HOST_DP_1

R2607 2.2R 5% R0402 USB_HOST_DM

FB2601 DNP
90R-100M L0603D

R2608 2.2R 5% R0402 USB_HOST_DP

ED2602
ESD5451N
ESD0402

C2606
22uF
C0805
X5R
16V

C2607
100nF
C0402
X5R
16V

U2602
ESD5302F
SOT_23

Cj<3pF

	Fuzhou Rockchip Electronics	
Project:	RK3308_AI-VA_MB_REF	
File:	26.USB Port for RK816-3(OPT3)	
Date:	Wednesday, July 04, 2018	Rev: 1.1
Designed by:	Joseph	Sheet: 23 of 51

RK816-3 With 1Cell Battery

PWR_KEY/PMIC_INT
POWER_SLEEP
RESET
I2C1_SDA
I2C1_SCL

Notes

If adapter 5V direct connect to PMIC power pins.
DO NOT DELETE THE TVS PROTECTION!!!
Note that PMIC power pins supply voltage **< 6.5V**
Recommended TVS Partnumber: AZ5825-01F
Operating Supply Voltage: 5.5V
PeakPulse Current: >10A(tp=8/20us)
Surge Clamping Voltage: 6V
ESD Clamping Voltage: 6.5V
IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

VCC_RK816IN
ED2700 AZ5825-01F
ESD0402

DO NOT DELETE IT!
不得删除！
不得随意更换型号！

Feedback from RK3308 RK3308

USB没有用OTG功能可以不加
SW5 D2700 SS32 SOD_123

1.493V

RK816-3 U2700 QFN40 5R00X5R00X0R80_T

VDD_1V0

VDD_LOG FB2700 180R-100M VDD_1V0
L0603 1.5A 25%
VDD_1V0_LDO
R2709 0R R0402 5% DNP

Note:
Default : VDD_1V0 Power Supply from VDD_LOG

VCCIO_SDMMC

Option1(Default):
Only support SDMMC 2.0

VCC_IO R2708 5% 0R R0402 VCCIO_SDMMC

Option2:
VCCIO_SD from LDO of RK816-3
Support SDMMC 3.0& SDMMC 2.0

VCCIO_SD R2710 DNP5% 0R R0402

VCCIO_FLASH

VCC_1V8 R27111 DNP0R R0402 5% VCCIO_FLASH
VCC_IO R27141 0R R0402 5%

FLASH_SEL (Pin R3 of RK3308)		VCCIO_FLASH
eMMC	H	1.8V
	L	3.3V
Nand Flash	H	1.8V
	L	3.3V(Default)

VCCIO_SDIO

VCC_1V8 R27121 0R R0402 5% VCCIO_SDIO
VCC_IO R27151 DNP0R R0402 5%

SDIO2.0/3.0	SDIO2.0	SDIO3.0
VCCIO_SDIO	3.3V	1.8V

VCC_3V3_CODEC

VCCIO_3V3 R27131 0R R0402 5% VCC_3V3_CODEC
VCC_IO R27161 0R R0402 5%

Layout Note:
The power of VCC_IO must be according to star topology to each load.
VCC_3V3_CODEC should route from the source of VCC_IO.

VCC_3V3_CODEC (PIN P16 of RK3308)
Star topology to each load.

Output of BUCK4:
The source of the power of VCC_IO

other loads

PowerAmplifier Power Supply

VCC_SYS
Q2700 WPM3401-3/TR SOT_23
L2705 2.2uH IND 303015 1.6A 0.06ohm
D2701 B5819W SOD_123 VCC5V0_PA
U2701 SY7208/TCS9208 SOT_23_6
VIN LX
EN NC
GND FB
FB:0.6V

As PA_DRV Funtion
IR_RX/PA_DRV
Q2701 S8050 SOT_23

PCB Note:
Single cell battery

Note:
SNSP4SNSN按照差分要求走线：
R2306靠近R2305放置。

BT2700 BAT3_2R54

Key for Power Up
ED2701 ESD5451N ESD0402
SW2700 Power ON SMT2_6R00X3R50X4R20

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK3308_AI-VA_MB_REF
File:	27.RK816-3 With 1Cell BAT(OPT3)
Date:	Wednesday, July 04, 2018	Rev:	1.1
Designed by:	Joseph	Sheet:	24 of 51

DDR3 1x16bit

Remind: Refer to the latest AVL for parts selection.

U3000
K4B2G1646F-BYK0
FBGA96_14R00X11R00X1R20

Signal	Pin		Pin	Signal
DDR_D15	E3	DQ0	A0	N3	DDR_A0
DDR_D12	F7	DQ1	A1	P7	DDR_A1
DDR_D13	F2	DQ2	A2	P3	DDR_A2
DDR_D10	F8	DQ3	A3	N2	DDR_A3
DDR_D11	H3	DQ4	A4	P8	DDR_A4
DDR_D14	H8	DQ5	A5	P2	DDR_A5
DDR_D8	G2	DQ6	A6	R8	DDR_A6
DDR_D9	H7	DQ7	A7	R2	DDR_A7
DDR_D4	D7	DQ8	A8	T8	DDR_A8
DDR_D5	C3	DQ9	A9	R3	DDR_A9
DDR_D6	C8	DQ10	A10/AP	L7	DDR_A10
DDR_D2	C2	DQ11	A11	R7	DDR_A11
DDR_D3	A7	DQ12	A12/BC#	N7	DDR_A12
DDR_D0	A2	DQ13	A13	T3	DDR_A13
DDR_D7	B8	DQ14	A14	T7	DDR_A14
DDR_D1	A3	DQ15			

DDR_CKE0 K9 — CKE0 BA0 M2 DDR_BA0
DDR_CS0N L2 — CS#0 BA1 N8 DDR_BA1
DDR_ODT0 K1 — ODT0 BA2 M3 DDR_BA2

DDR_RASN J3 — RAS# CK J7 DDR_CLKP
DDR_CASN K3 — CAS# CK# K7 DDR_CLKN
DDR_WEN L3 — WE#

LDM E7 DDR_DM1
UDM D3 DDR_DM0

VCC_DDR —
B2 VDD1
D9 VDD2
G7 VDD3
K2 VDD4   LDQS F3 DDR_DQS1P
K8 VDD5   LDQS# G3 DDR_DQS1N
N1 VDD6
N9 VDD7   UDQS C7 DDR_DQS0P
R1 VDD8   UDQS# B7 DDR_DQS0N
R9 VDD9

A1 VDDQ1   VSSQ1 B1
A8 VDDQ2   VSSQ2 B9
C1 VDDQ3   VSSQ3 D1
C9 VDDQ4   VSSQ4 D8
D2 VDDQ5   VSSQ5 E2
E9 VDDQ6   VSSQ6 E8
F1 VDDQ7   VSSQ7 F9
H2 VDDQ8   VSSQ8 G1
H9 VDDQ9   VSSQ9 G9

VREF_DDR —
H1 VREFDQ   VSS1 A9
M8 VREFCA   VSS2 B3
            VSS3 E1
DDR_RESET —
T2 RESET#   VSS4 G8
L8 ZQ0   VSS5 J2
            VSS6 J8
J1 ODT1   VSS7 M1
J9 CKE1   VSS8 M9
L1 CS#1   VSS9 P1
L9 ZQ1   VSS10 P9
M7 A15   VSS11 T1
            VSS12 T9

R3000 49.9R 1% R0402
DDR_CLKP —1—/\/\—2—
DDR_CLKN —1—/\/\—2—
R3001 49.9R 1% R0402
C3000 100pF C0G 50V C0402

C3001 DNP 100nF C0402 X5R 16V
R3002 240R 1% R0402

Left signal list

DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DQS0P
DDR_DQS0N
DDR_DQS1P
DDR_DQS1N

DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14

DDR_DM0
DDR_DM1

DDR_BA0
DDR_BA1
DDR_BA2
DDR_CS0N
DDR_ODT0
DDR_CKE0
DDR_RASN
DDR_CASN
DDR_WEN
DDR_RESET

DDR_CLKP
DDR_CLKN

Power filter capacitors

VCC_DDR

C3002	C3003	C3004	C3005	C3006	C3007	C3008	C3009
10uF	100nF	100nF	100nF	100nF	100nF	DNP	DNP
X5R	X5R	X5R	X5R	X5R	X5R	100nF	100nF
6.3V	16V	16V	16V	16V	16V	C0402	C0402
C0603	C0402	C0402	C0402	C0402	C0402	X5R	X5R
						16V	16V

Note:All the Power filter capacitors should be placed close to the power pins of DDR3

VCC_DDR

R3003 1K 1% R0402
VREF_DDR
R3004 1K 1% R0402
C3010 1nF 50V C0402 X5R
C3011 DNP 1nF X5R 50V C0402

LPDDR2 1x16bit

Remind: Refer to the latest AVL for parts selection.

DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DQS0P
DDR_DQS0N
DDR_DQS1P
DDR_DQS1N

DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9

DDR_DM0
DDR_DM1

DDR_CS0N

DDR_CKE0

DDR_CLKP
DDR_CLKN

DDR_CLKP / DDR_CLKN — R3100 49.9R 1% R0402 — R3101 49.9R 1% R0402 — C3100 100pF C0G 50V C0402

VCC_DDR — R3102 1K 1% R0402 — VREFCA_DDR — R3103 1K 1% R0402 — C3101 1nF X5R 50V C0402 — C3102 1nF X5R 50V C0402

VCC_DDR — R3104 1K 1% R0402 — VREFDQ_DDR — R3106 1K 1% R0402 — C3103 1nF X5R 50V C0402 — C3104 1nF X5R 50V C0402

VCC_1V8 — R3107 0R R0402 5% — VDD1_1V8

VCC_DDR — C3105 10uF X5R 6.3V C0603 — C3106 1uF X5R 6.3V C0402 — C3107 100nF X5R 16V C0402 — C3108 100nF X5R 16V C0402 — C3109 100nF X5R 16V C0402 — C3110 100nF X5R 16V C0402 — C3111 100nF X5R 16V C0402 — C3112 1nF X5R 50V C0402

VDD1_1V8 — C3119 10uF X5R 6.3V C0603 — C3120 100nF X5R 16V C0402 — C3121 100nF X5R 16V C0402

Note:All the Power filter capacitors should be placed close to the power pins of LPDDR2

U3100

DDR_D11 N8 DQ0 CA0 P3 DDR_A0
DDR_D9 M8 DQ1 CA1 N3 DDR_A1
DDR_D10 M7 DQ2 CA2 M3 DDR_A2
DDR_D13 M9 DQ3 CA3 M2 DDR_A3
DDR_D12 M6 DQ4 CA4 M1 DDR_A4
DDR_D8 L7 DQ5 CA5 G2 DDR_A5
DDR_D14 L8 DQ6 CA6 F2 DDR_A6
DDR_D15 L9 DQ7 CA7 F3 DDR_A7
DDR_D3 G9 DQ8 CA8 E3 DDR_A8
DDR_D7 G8 DQ9 CA9 E2 DDR_A9
DDR_D0 G7 DQ10
DDR_D4 F6 DQ11 CK J3 DDR_CLKP
DDR_D2 F9 DQ12 CK# H3 DDR_CLKN
DDR_D6 F7 DQ13
DDR_D1 F8 DQ14 DM0 K5 DDR_DM1
DDR_D5 E8 DQ15 DM1 H5 DDR_DM0

DDR_CKE0 K1 CKE DQS0 L6 DDR_DQS1P
DDR_CS0N L1 CS# DQS0# L5 DDR_DQS1N
DQS1 G6 DDR_DQS0P
DQS1# G5 DDR_DQS0N

VCC_DDR N2 VDDCA_N2
H1 VDDCA_H1
F1 VDDCA_F1 C2 VSS0
VDD1_1V8 T6 VDD1_T6 D1 VSS1
B6 VDD1_B6 E1 VSS2
R1 VDD1_R1 H2 VSS3
C1 VDD1_C1 J1 VSS4
N1 VSS5
VCC_DDR D2 VDD2_D2 P1 VSS6
T5 VDD2_T5 R2 VSS7
J7 VDD2_J7 C5 VSS8
B5 VDD2_B5 C6 VSS9
P2 VDD2_P2 C9 VSS10
G1 VDD2_G1 D10 VSS11
E10 VSS12
C7 VDDQ_C7 F5 VSS13
C10 VDDQ_C10 G10 VSS14
D5 VDDQ_D5 J5 VSS15
E9 VDDQ_E9 J8 VSS16
F10 VDDQ_F10 L10 VSS17
H6 VDDQ_H6 M5 VSS18
J6 VDDQ_J6 N10 VSS19
K6 VDDQ_K6 P10 VSS20
M10 VDDQ_M10 R5 VSS21
N9 VDDQ_N9 R6 VSS22
P5 VDDQ_P5 R9 VSS23
R7 VDDQ_R7
R10 VDDQ_R10 NC_B2 B2
NC_B3 B3
VREFCA_DDR G3 VREFCA NC_C3 C3
VREFDQ_DDR J9 VREFDQ NC_J2 J2
NC_K2 K2
D3 ZQ NC_K3 K3
NC_L2 L2
NC_L3 L3
R3105 NC_R3 R3
240R NC_T2 T2
1% NC_T3 T3
R0402 NC_B7 B7

NC_B8 B8
A1 DNU_A1 NC_B9 B9
A2 DNU_A2 NC_C8 C8
B1 DNU_B1 NC_D6 D6
T1 DNU_T1 NC_D7 D7
U1 DUN_U1 NC_D8 D8
U2 DNU_U2 NC_D9 D9
A9 DNU_A9 NC_E5 E5
A10 DNU_A10 NC_E6 E6
B10 DNU_B10 NC_E7 E7
T10 DNU_T10 NC_N5 N5
U10 DNU_U10 NC_N6 N6
U9 DNU_U9 NC_N7 N7

NC_P6 P6
NC_P7 P7
NC_P8 P8
NC_P9 P9
NC_R8 R8
NC_T7 T7
NC_T8 T8
NC_T9 T9

128X16bit,533M

DDR2 1x16bit

Remind: Refer to the latest AVL for parts selection.

DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DQS0P
DDR_DQS0N
DDR_DQS1P
DDR_DQS1N

DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13

DDR_DM0
DDR_DM1

DDR_BA0
DDR_BA1
DDR_BA2
DDR_CS0N
DDR_ODT0
DDR_CKE0
DDR_RASN
DDR_CASN
DDR_WEN

DDR_CLKP
DDR_CLKN

U3200 DDRII-128M*16bit

Pin	Signal		Signal	Pin
G8	DQ0	A0		M8 DDR_A0
G2	DQ1	A1		M3 DDR_A1
H7	DQ2	A2		M7 DDR_A2
H3	DQ3	A3		N2 DDR_A3
H1	DQ4	A4		N8 DDR_A4
H9	DQ5	A5		N3 DDR_A5
F1	DQ6	A6		N7 DDR_A6
F9	DQ7	A7		P2 DDR_A7
C8	DQ8	A8		P8 DDR_A8
C2	DQ9	A9		P3 DDR_A9
D7	DQ10	A10		M2 DDR_A10
D3	DQ11	A11		P7 DDR_A11
D1	DQ12	A12		R2 DDR_A12
D9	DQ13	RFU/A13		R8 DDR_A13
B1	DQ14			
B9	DQ15	BA0		L2 DDR_BA0
		BA1		L3 DDR_BA1
K2	CKE	RFU/BA2		L1 DDR_BA2
L8	CS#			
K9	ODT	CK		J8 DDR_CLKP
		CK#		K8 DDR_CLKN
K7	RAS#			
L7	CAS#	LDM		F3 DDR_DM1
K3	WE#	UDM		B3 DDR_DM0
A1	VDD1	LDQS		F7 DDR_DQS1P
E1	VDD2	LDQS#		E8 DDR_DQS1N
J9	VDD3			
M9	VDD4	UDQS		B7 DDR_DQS0P
R1	VDD5	UDQS#		A8 DDR_DQS0N

DDR_CKE0 — CKE
DDR_CS0N — CS#
DDR_ODT0 — ODT
DDR_RASN — RAS#
DDR_CASN — CAS#
DDR_WEN — WE#

VDDQ1 / VSSQ ... (power/ground pins)

VCC_DDR

VREF_DDR — VREF

R3200 / R3201
DDR_CLKP — 1 — R3200 49.9R 1% R0402 — 2
DDR_CLKN — 1 — R3201 49.9R 1% R0402 — 2

C3200 100pF C0G 50V C0402

VCC_DDR

C3201	C3202	C3203	C3204	C3205	C3206	C3207	C3208
10uF	1uF	100nF	100nF	100nF	100nF	100nF	1nF
X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R
6.3V	6.3V	16V	16V	16V	16V	16V	50V
C0603	C0402	C0402	C0402	C0402	C0402	C0402	C0402

VCC_DDR

R3202 1K 1% R0402
VREF_DDR
R3203 1K 1% R0402

C3209 1nF X5R 50V C0402
C3210 1nF X5R 50V C0402

Note: All the Power filter capacitors should be placed close to the power pins of DDR2.

eMMC Flash

Remind: Refer to the latest AVL for parts selection.

Note:For Nand Flash + eMMC dual layout,
The D0-D7,CMD,CLK traces should pass through the pin of Nand Flash first,
and then connect to eMMC.

FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4/SFC_CLK
FLASH_D5/SFC_CS0
FLASH_D6
FLASH_D7
FLASH_WRN/EMMC_CMD
FLASH_CLE/EMMC_CLK
FLASH_ALE/EMMC_RST

VCCIO_FLASH

R4000   1 10K 2 5% R0402

FLASH_D0   H3
FLASH_D1   H4
FLASH_D2   H5
FLASH_D3   J2
FLASH_D4/SFC_CLK   J3
FLASH_D5/SFC_CS0   J4
FLASH_D6   J5
FLASH_D7   J6

U4000A
KLM8G1GEAC-B031

DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7

VCCQ1 AA5
VCCQ2 AA3
VCCQ3 Y4
VCCQ4 W4
VCCQ5 K6

VCCIO_FLASH

C4000   C4001   C4002   C4003   C4004
100nF   100nF   100nF   100nF   4.7uF
X5R   X5R   X5R   X5R   X5R
16V   16V   16V   16V   6.3V
C0402   C0402   C0402   C0402   C0603

R4001 1 10K 2 5% R0402

FLASH_WRN/EMMC_CMD   W5

CMD

VCC1 U9   T10
VCC2 N5
VCC3 M6
VCC4

VCC_IO

FLASH_CLE/EMMC_CLK   R4004 1 2 22R 5% R0402

FLASH_CLE/EMMC_CLK   W6

CLK

VSS1 U8 R10
VSS2 P5
VSS3 M7
VSS4 H6
VSS5 T5
VSS6

C4005   C4006   C4007
100nF   100nF   4.7uF
X5R   X5R   X5R
16V   16V   6.3V
C0402   C0402   C0603

VCCIO_FLASH   R4003 1 DNP 2 4.7K 5% R0402   FLASH_ALE/EMMC_RST   U5

RST_n

VDDi   K2

C4008
1uF
X5R
6.3V
C0402

RCLK R5

VSF1 M9
VSF2 M10
VSF3 N10
VSF4 U10

VSSQ1 AA6
VSSQ2 AA4
VSSQ3 Y5
VSSQ4 Y2
VSSQ5 K4

BGA169_18R00X14R00_2L

A4   A6   A9   A11   B2   B13   D1   D14   H1   H2   H7   H8   H9   H10   H11   H12   H13   H14   J1   J7   J8   J9   J10   J11   J12   J13   J14   K1   K3   K5   K7   K8   K9   K10

NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC9
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
NC20
NC21
NC22
NC23
NC24
NC25
NC26
NC27
NC28
NC29
NC31
NC32
NC33
NC34

NC138 NC137 NC136 NC135 NC134 NC133 NC132 NC131 NC130 NC129 NC128 NC127 NC126 NC125 NC124 NC123 NC122 NC121 NC120 NC119 NC118 NC117 NC116 NC115 NC114 NC113 NC112 NC111 NC110 NC109 NC108 NC107 NC106 NC105 NC104

NC103 W8
NC102 W7
NC101 W3
NC100 W2
NC99   W1
NC98   V14
NC97   V13
NC96   V12
NC95   V3
NC94   V2
NC93   V1
NC92   U14
NC91   U13
NC90   U12
NC88   U7
NC87   U6
NC85   U3
NC84   U2
NC83   U1
NC82   T14
NC81   T13
NC80   T12
NC78   T3
NC77   T2
NC76   T1
NC75   R14
NC74   R13
NC73   R12
NC71   R3
NC70   R2
NC69   R1

Remind:Short two TP points to Enter MaskRom.

TP4000 TP_0.7   FLASH_D0

TP4001 TP_0.7

Layout Note:As soon as possible
reduce the branch of FLASH_D0

U4000B
KLM8G1GEAC-B031
BGA169_18R00X14R00_2L

NC35 NC36 NC37 NC38 NC39 NC40 NC41 NC42 NC43 NC44 NC45 NC46 NC47 NC48 NC49   NC86 NC52 NC53 NC54 NC55 NC56 NC57   NC59 NC60 NC61 NC62 NC63 NC64 NC65 NC66 NC67 NC68

Nand Flash

Remind: Refer to the latest AVL for parts selection.

FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4/SFC_CLK
FLASH_D5/SFC_CS0
FLASH_D6
FLASH_D7
FLASH_WRN/EMMC_CMD
FLASH_CLE/EMMC_CLK
FLASH_RDN
FLASH_ALE/EMMC_RST
FLASH_RDY
FLASH_CS0N

VCCIO_FLASH

R4100
4.7K
5%
R0402

VCC_IO

FLASH_RDY

FLASH_RDN
FLASH_CS0N

VCCIO_FLASH

R4103
4.7K
5%
R0402

VCC_IO

FLASH_CLE/EMMC_CLK
FLASH_ALE/EMMC_RST
FLASH_WRN/EMMC_CMD
FLASH_WP

VCC_IO

U4100
GD9FU1G8F2AMG
TSOP48_18R40X12R10X1R20

Pin	Name	Name	Pin
1	VCC1	VSS5	48
2	VSS1	NC13	47
3	NC1	VSSQ4	46
4	R/B1	VCCQ4	45
5	R/B2	I/O7	44
6	R/B3	I/O6	43
7	R/B4	I/O5	42
8	RE	I/O4	41
9	CE0	VSSQ3	40
10	CE1	VCCQ3	39
11	NC2	VCCQ5	38
12	VCC2	VCC4	37
13	VSS2	VSS4	36
14	CE2	DQS	35
15	CE3	VCCQ2	34
16	CLE	VSSQ2	33
17	ALE	I/O3	32
18	WE	I/O2	31
19	WP	I/O1	30
20	NC3	I/O0	29
21	NC4	VCCQ1	28
22	NC5	VSSQ1	27
23	VSS3	NC6	26
24	VCC3	VSS6	25

R4101 DNP 2 R0402 VCCIO_FLASH
FLASH_D7
FLASH_D6
FLASH_D5/SFC_CS0
FLASH_D4/SFC_CLK

R4102 1 DNP 2 0R 5% VCCIO_FLASH
R0402 VCC_IO

VCCIO_FLASH

FLASH_D3
FLASH_D2
FLASH_D1
FLASH_D0

R4104 1 DNP 2 R0402 VCCIO_FLASH

Type of Flash	R4102
128MB SLC (Default)	DNP
else	0R

Note: if use toshiba and sandisk DDR mode,
VCCQ1 and VCCQ4 must be connected to VCCIO_FLASH.

Remind:Short two TP points to Enter MaskRom.

TP4100 TP_0.7 FLASH_D0

TP4101 TP_0.7

Layout Note:As soon as possible
reduce the branch of FLASH_D0

VCC_IO

C4100
4.7uF
X5R
6.3V
C0402

C4101
100nF
X5R
16V
C0402

VCCIO_FLASH

C4102
4.7uF
X5R
6.3V
C0402

C4103
100nF
X5R
16V
C0402

SPI Nor Flash

Remind: Refer to the latest AVL for parts selection.

U4200

Pin	Name		Name	Pin
1	HOLD/DQ3		CLK	16
2	VCC		DQ0	15
3	RESET/DNU		DNU8	14
4	DNU2		DNU7	13
5	DNU3		DNU6	12
6	DNU4		DNU5	11
7	SEL		VSS	10
8	DQ1		W/VPP/DQ2	9

GD25Q256D
SOP16_10R50X7R60X2R75

FLASH_D3 → 1
FLASH_D4/SFC_CLK ← 16
FLASH_D0 ← 15
FLASH_D5/SFC_CS0 → 7
FLASH_D1 → 8
FLASH_D2 ← 9

VCC_IO

C4200
100nF
X5R
16V
C0402

R4200 1 10K 2 R0402 5%

FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4/SFC_CLK
FLASH_D5/SFC_CS0

U4201
DNP
EN25Q32B-104HIP
SOP8_5R40X5R40X2R20

Pin	Name		Name	Pin
1	CS		VCC	8
2	DO(D1)		HOLD(D3)	7
3	WP(D2)		CLK	6
4	VSS		DI(D0)	5

FLASH_D5/SFC_CS0 → 1
FLASH_D1 → 2
FLASH_D2 → 3
FLASH_D3 ← 7
FLASH_D4/SFC_CLK ← 6
FLASH_D0 ← 5

VCC_IO

C4201
100nF
X5R
16V
C0402

Remind:Short two TP points to Enter MaskRom.

TP4200 TP_0.7 FLASH_D4/SFC_CLK

TP4201 TP_0.7

Layout Note:As soon as possible
reduce the branch of FLASH_D4/SFC_CLK

Rockchip
瑞芯微电子
Fuzhou Rockchip Electronics

Project:	RK3308_AI-VA_MB_REF
File:	42.Flash-SPI Nor Flash
Date:	Wednesday, July 04, 2018
Designed by:	Joseph

Rev:	1.1
Sheet:	30 of 51

RGB Panel

LCDC_CLK — R5001 1 22R 5% 2 R0402 — LCD_CLK_1

C5000
DNP
8pF
C0402
C0G
50V

LCDC_HSYNC — LCD_HSYNC
LCDC_DEN/I2S1_SCLK_TX_M0 — LCD_DEN
LCDC_VSYNC — LCD_VSYNC
LCDC_D0 — LCD_D0
LCDC_D1/I2S1_LRCK_TX_M0 — LCD_D1
LCDC_D2 — LCD_D2
LCDC_D3/I2S1_SDO0_M0 — LCD_D3
LCDC_D4 — LCD_D4
LCDC_D5 — LCD_D5
LCDC_D6 — LCD_D6
LCDC_D7/I2S1_SDI0_M0 — LCD_D7
LCDC_D8/MAC_CLK — LCD_D8
LCDC_D9/MAC_MDC — LCD_D9
LCDC_D10/MAC_MDIO — LCD_D10
LCDC_D11/MAC_RXER — LCD_D11
LCDC_D12/MAC_RXDV — LCD_D12
LCDC_D13/MAC_TXEN — LCD_D13
LCDC_D14/MAC_TXD0 — LCD_D14
LCDC_D15/MAC_TXD1 — LCD_D15
LCDC_D16/MAC_RXD0 — LCD_D16
LCDC_D17/MAC_RXD1 — LCD_D17

LCD_BL
FLASH_SEL/LCD_PWREN — LCD_PWREN
LCD_RST

SPI2_CLK
SPI2_CS
SPI2_TX/UART2_TX_M0 — SPI2_TX
SPI2_RX/UART2_RX_M0 — SPI2_RX

VCC_LCD
R5000
DNP
10K
R0402
5%

LCD_RST — R5002 1 0R 5% 2 R0603 — LCD_RST_1

C5001
DNP
1uF
C0402
X5R
6.3V

VCC_LCD
R5003 10K 5% R0402 — D/CX
R5004 10K 5% R0402 — RDX

U5000

Pin	Name
46	GND6
45	YU
44	XL
43	YD
42	XR
41	TE
40	CS
39	D/CX
38	WRX/SCL
37	RDX
36	SDI/SDA
35	SDO
34	DB0
33	DB1
32	DB2
31	DB3
30	DB4
29	DB5
28	DB6
27	DB7
26	DB8
25	DB9
24	DB10
23	DB11
22	DB12
21	DB13
20	DB14
19	DB15
18	DB16
17	DB17
16	DE
15	GND5
14	DOTCLK
13	GND4
12	HSYNC
11	VSYNC
10	RESET
9	IOVCC
8	VCC
7	GND3
6	GND2
5	VLED1-
4	VLED2-
3	VLED1+
2	VLED2+
1	GND1
47	GND7

SPI2_CS — CS
D/CX — D/CX
SPI2_CLK — WRX/SCL
RDX — RDX
SPI2_TX — SDI/SDA
SPI2_RX — SDO
LCD_D0 — DB0
LCD_D1 — DB1
LCD_D2 — DB2
LCD_D3 — DB3
LCD_D4 — DB4
LCD_D5 — DB5
LCD_D6 — DB6
LCD_D7 — DB7
LCD_D8 — DB8
LCD_D9 — DB9
LCD_D10 — DB10
LCD_D11 — DB11
LCD_D12 — DB12
LCD_D13 — DB13
LCD_D14 — DB14
LCD_D15 — DB15
LCD_D16 — DB16
LCD_D17 — DB17
LCD_DEN — DE
LCD_CLK_1 — DOTCLK
LCD_HSYNC — HSYNC
LCD_VSYNC — VSYNC
LCD_RST_1 — RESET

VCC_LCD — IOVCC
VCC — VCC
LED- — VLED1-
LED- — VLED2-
LED+ — VLED1+
LED+ — VLED2+

VCC_LCD

C5008
10uF
C0805
X5R
6.3V
DNP

C5009
100nF
C0402
X5R
16V

LCDK35C4S16T

Backlight / Power (bottom left)

VCC5V0_SYS

L5000
10uH
IND_303015
0.72A 0.25ohm

D5000
B5819W
SOD_123

LED+

C5002
4.7uF
10V
X5R
C0603

U5001
UP6003AMT6 /SY7201
SOT_23_6

Pin	Name
6	IN
2	—
4	EN
1	SW
5	OV
3	FB
—	GND

uP6003AMT6_FB=300mV
SY7201_FB=200mV

C5003
1uF
C0603
X5R 35V

LED-

LCD_BL

R5007
100K
5%
R0402

R5008
20R
1%
R0603

Center bottom

VCC_IO

R5005 1 0R 5% 2 R0603 DNP

VCC_LCD

C5004
1uF
C0402
X5R
10V

C5005
100nF
X5R
16V
C0402

R5006
1M
5%
R0402

Q5000
WPM2026
SOT23

C5006
4.7uF
C0603
6.3V
X5R

C5007
100nF
X5R
16V
C0402

R5009
100K
5%
R0402

LCD_PWREN

Project: RK3308_AI-VA_MB_REF
File: 50.LCM-RGB Panel
Date: Wednesday, July 04, 2018
Designed by: Joseph
Rev: 1.1
Sheet: 31 of 51

Note:
U5001 EN pin must support PWM brightness dimming control,
Otherwise,it needs to be increased PWM circuit at FB pin.

MCU Panel

LCDC_CLK >> R5100 1 22R 5% 2 R0402 LCD_CLK_2

C5100
DNP
8pF
C0402
C0G
50V

LCDC_HSYNC >> LCD_HSYNC
LCDC_DEN/I2S1_SCLK_TX_M0 LCD_DEN
LCDC_VSYNC LCD_VSYNC
LCDC_D0 LCD_D0
LCDC_D1/I2S1_LRCK_TX_M0 LCD_D1
LCDC_D2 LCD_D2
LCDC_D3/I2S1_SDO0_M0 LCD_D3
LCDC_D4 LCD_D4
LCDC_D5 LCD_D5
LCDC_D6 LCD_D6
LCDC_D7/I2S1_SDI0_M0 LCD_D7
LCDC_D8/MAC_CLK LCD_D8
LCDC_D9/MAC_MDC LCD_D9
LCDC_D10/MAC_MDIO LCD_D10
LCDC_D11/MAC_RXER LCD_D11
LCDC_D12/MAC_RXDV LCD_D12
LCDC_D13/MAC_TXEN LCD_D13
LCDC_D14/MAC_TXD0 LCD_D14
LCDC_D15/MAC_TXD1 LCD_D15
LCD_BL
FLASH_SEL/LCD_PWREN LCD_PWREN
LCD_RST

VCC_LCD

R5101
DNP
10K
5%
R0402

LCD_RST >> R5102 1 0R 5% 2 R0603 LCD_RST_2

C5101
DNP
1uF
C0402
X5R
6.3V

LCDC_HSYNC >> R5103 1 22R 5% 2 R0402 MCU_WRX
LCDC_VSYNC >> R5104 1 22R 5% 2 R0402 MCU_CS
LCDC_CLK >> R5105 1 22R 5% 2 R0402 MCU_DCX
LCDC_DEN/I2S1_SCLK_TX_M0 >> R5106 1 22R 5% 2 R0402 MCU_RDX

U5100
GND6 46

45 YU
44 XL
43 YD
42 XR
41 TE
MCU_CS 40 CS
MCU_DCX 39 D/CX
MCU_WRX 38 WRX/SCL
MCU_RDX 37 RDX
36 SDI/SDA
35 SDO
LCD_D0 34 DB0
LCD_D1 33 DB1
LCD_D2 32 DB2
LCD_D3 31 DB3
LCD_D4 30 DB4
LCD_D5 29 DB5
LCD_D6 28 DB6
LCD_D7 27 DB7
LCD_D8 26 DB8
LCD_D9 25 DB9
LCD_D10 24 DB10
LCD_D11 23 DB11
LCD_D12 22 DB12
LCD_D13 21 DB13
LCD_D14 20 DB14
LCD_D15 19 DB15
18 DB16
17 DB17
LCD_DEN 16 DE
15 GND5
LCD_CLK_2 14 DOTCLK
13 GND4
LCD_HSYNC 12 HSYNC
LCD_VSYNC 11 VSYNC
LCD_RST_2 10 RESET
VCC_LCD 9 IOVCC
8 VCC
7 GND3
6 GND2
LED- 5 VLED1-
4 VLED2-
LED+ 3 VLED1+
2 VLED2+
1 GND1

LCDK35C4S16T
GND7 47

Power Section

VCC5V0_SYS

L5100
10uH
IND_303015
0.72A 0.25ohm

D5100
B5819W
SOD_123

LED+

U5101
UP6003AMT6 /SY7201
SOT_23_6

6 IN SW 1
2 GND OV 5
4 EN FB 3

C5102
4.7uF
10V
X5R
C0603

C5103
1uF
C0603
X5R 35V

LED-

LCD_BL

R5109
100K
5%
R0402

R5110
20R
1%
R0603

uP6003AMT6_FB=300mV
SY7201_FB=200mV

VCC_IO

R5107 1 0R 5% 2 R0603 DNP

VCC_LCD

C5104
1uF
C0402
X5R
10V

C5105
100nF
X5R
16V
C0402

R5108
1M
5%
R0402

Q5100
WPM2026
SOT23

C5106
4.7uF
C0603
6.3V
X5R

C5107
100nF
X5R
16V
C0402

R5111
100K
5%
R0402

LCD_PWREN

VCC_LCD

C5108
10uF
C0805
X5R
6.3V
DNP

C5109
100nF
C0402
X5R
16V

Note:
U5101 EN pin must support PWM brightness dimming control,
Otherwise,it needs to be increased PWM circuit at FB pin.

SPI Panel

SPI2_CLK

SPI2_CS

SPI2_TX/UART2_TX_M0 — SPI2_TX

LCD_BL

FLASH_SEL/LCD_PWREN — LCD_PWREN

LCD_RST

VCC_LCD

R5200
DNP
10K
5%
R0402

LCD_RST — R5201 1 0R 5% 2 R0603 — LCD_RST_3

C5200
DNP
1uF
C0402
X5R
6.3V

VCC_LCD

C5201
10uF
C0805
X5R
6.3V
DNP

C5202
100nF
C0402
X5R
16V

U5200
LCDK280I1810T

- 18 GND5
- 17 GND4
- 16 XR
- 15 YU
- 14 XL
- 13 YD
- 12 GND3
- 11 CS
- 10 IOVCC
- 9 VCC
- 8 SCK
- 7 SDA
- 6 NC
- 5 RESET
- 4 GND2
- 3 LED+
- 2 LED-
- 1 GND1

SPI2_CS

VCC_LCD

SPI2_CLK

SPI2_TX

LCD_RST_3

LED+

R5202
0R
5%
R0603

Lower left circuit

VCC_IO

R5203 1 0R 5% 2 R0603 DNP

VCC_LCD

C5207
1uF
C0402
X5R
10V

C5208
100nF
C0402
X5R
16V

R5205
1M
5%
R0402

Q5201
WPM2026
SOT23

C5209
4.7uF
C0402
6.3V
X5R

C5210
100nF
C0402
X5R
16V

R5207
100K
5%
R0402

LCD_PWREN

Lower right circuit

VCC_IO

R5204
1M
5%
R0402

Q5200
WPM2026
SOT23

LED+

C5203
1uF
C0402
X5R
10V

C5204
100nF
C0402
X5R
16V

C5205
4.7uF
C0402
6.3V
X5R

C5206
100nF
C0402
X5R
16V

R5206
100K
5%
R0402

LCD_BL — R5208 1 2 1 Q5202 S8050 SOT_23

R5208
47K
5%
R0402

WIFI/BT Module-1T1R

Module Power

Level Shift

OPTION 1

37.4MHz: +-10ppm

OPTION 2

up to 700mA

OPTION 3

RF Microstrip Z0= 50 ohm

U6000 AW-CM256SM

OPTION	WIFI				BT	Crystals	VCCIO_SDIO
	a	b/g/n	ac	5GHz			
AW-CM256SM (Default)	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.6V
AP6255	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.6V
RTL8723BS	No	Yes	No	No	Yes	No the Moudle	1.62-3.6V
RTL8723DS	No	Yes	No	No	Yes	No the Moudle	1.62-3.6V
RTL8189ETV MODULE	No	Yes	No	No	No	No the Moudle	1.8V/3.3V

OPTION	1	2	3
AW-CM256SM (Default)	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6255	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
RTL8723BS	No	No	No
RTL8723DS	No	No	No
RTL8189ETV MODULE	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

WIFI/BT Module-2T2R

SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3
SDIO_CMD
SDIO_CLK

SDIO_D0 — R6100 1 2 22R 5% R0402 — WIFI_2X2_D0 2 1 C6100 DNP C0402
SDIO_D1 — R6101 1 2 22R 5% R0402 — WIFI_2X2_D1 2 1 C6101 DNP C0402
SDIO_D2 — R6102 1 2 22R 5% R0402 — WIFI_2X2_D2 2 1 C6102 DNP C0402
SDIO_D3 — R6103 1 2 22R 5% R0402 — WIFI_2X2_D3 2 1 C6103 DNP C0402
SDIO_CMD — R6104 1 2 22R 5% R0402 — WIFI_2X2_CMD 2 1 C6104 DNP C0402
SDIO_CLK — WIFI_2X2_CLK 2 1 C6105 DNP C0402

Level Shift

WIFI_REG_ON — R6106 1 15K 5% 2 R0402 — WIFI_REG_ON_2
R6107 1 20K 5% 2 R0402
R6111 1 0R 5% 2 R0402 DNP
WIFI_WAKE_HOST — R6140 47K R0402 5%
Q6100 S8050 SOT_23
WIFI_WAKE_HOST_2

Module Power

VCC_IO
VCC_WL
R6115 1 0R 2 R0603 5%

2T2R

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6356S	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.7-3.6V
AP62X2	Yes	Yes	No	Yes	Yes	37.4MHz	1.8-3.3V
8274B-SR	Yes	Yes	Yes	Yes	Yes	No the Moudle	1.7-3.6V
6222B-SR	Yes	Yes	Yes	Yes	Yes	No the Moudle	1.7-3.6V
6192B-SE	No	Yes	No	No	No	No the Moudle	1.7-3.6V

OPTION	1	2	3
AP6356S	Yes	Yes	No
AP62X2	Yes	Yes	Yes
8274B-SR	No	No	No
6222B-SR	No	No	No
6192B-SE	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Note:
Adjusted the load capacitance according to the crystal specification.

REF_CLK_OUT

R6109 DNP 33R R0402 5%

C6106 C0G 50V DNP 100pF C0402

R6130 DNP 680R 5% R0402
L6104 DNP 330nH 5% R0805
C6130 DNP 47pF 50V C0402 C0G

Layout Note:
Crystal away from antenna

C6112 22pF C0G 50V C0402
R6114 1 22R 5% 2 R0402
Y6100 X2 GND / GND X1 37.4MHz CRY4_3R20X2R50X0R80
C6115 22pF C0G 50V C0402

Option1

Option2
C6120 4.7uF 6.3V X5R C0603
L6101 4.7uH IND_303012

U6100 AP6356S

GND_11 / GND_10 / WL_ANT1 / GND_8 / GND_7 / GND_6 / GND_5 / GND_4 / GND_3 / WL_BT_ANT0 / GND_1

PA_PU — 12 NC_12
13 XTAL_OUT
14 XTAL_IN
WIFI_REG_ON_2 — 15 WL_REG_ON
WIFI_WAKE_HOST_2 — 16 WL_HOST_WAKE
WIFI_2X2_CMD — 17 SDIO_DATA_CMD
WIFI_2X2_CLK — 18 SDIO_DATA_CLK
WIFI_2X2_D3 — 19 SDIO_DATA_3
WIFI_2X2_D2 — 20 SDIO_DATA_2
WIFI_2X2_D0 — 21 SDIO_DATA_0
WIFI_2X2_D1 — 22 SDIO_DATA_1
23 GND_23
24 NC_24
25 VIN_LDO

BT_HOST_WAKE 50 — BT_WAKE_HOST
BT_WAKE 49 — HOST_WAKE_BT
NC_48 48
NC_47 47
NC_46 46
NC_45 45
NC_44 44
UART4_RTS 43 — UART4_RTS
UART_RTS_N 42 — UART4_CTS
UART_RXD 41 — UART4_TXD
UART_TXD 40 — UART4_RXD
GND_39 39
BT_REG_ON 38 — BT_REG_ON
NC_37 37

VIN_LDO_OUT / PCM_SYNC / PCM_IN / PCM_OUT / PCM_CLK / LPO / GND_32 / NC_33 / NC_35 / VDDIO / VBAT

26 27 28 29 30 31 32 34 35 36

VCCIO_SDIO

VCC_WL
>50mil

C6121 1uF X5R 6.3V C0402
C6124 100nF X5R 16V C0402
C6122 22uF X5R 10V C0805
C6123 100nF X5R 16V C0402

PCM_SYNC
PCM_OUT
PCM_IN
PCM_CLK

CLK_32K_OUT — R6119 1 10K 5% 2 R0402 — WIFIBT_32KIN
R6120 12K 5% R0402

ANT6100 ANT4411DR ANTPCB_44R00X11R00_DSR

R6108 1 2 0R 5% R0402 — ANT6100

C6107 1 10pF C0G 50V 2 C0402
R6110 DNP 2 0R 5% R0402 — ANT6101 ANT_JACK
C6108 DNP C0402
C6110 DNP C0402
GND1 GND2

R6112 1 2 0R 5% R0402 — ANT6102 ANT4411DR ANTPCB_44R00X11R00_DSR

C6111 1 10pF C0G 50V 2 C0402
R6113 DNP 2 0R 5% R0402 — ANT6103 ANT_JACK
C6113 DNP C0402
C6114 DNP C0402
GND1 GND2

PA_3V3
Q6101 WPM2015-3/TR SOT_23 DNP
VCC_IO

C6116 100nF X5R 16V C0402 DNP
C6117 4.7uF 6.3V C0603 DNP
C6118 100nF X5R 16V C0402 DNP
R6116 100K 5% R0402 DNP
C6119 4.7uF 6.3V X5R C0603 DNP

R6117 10K 5% R0402 DNP
Q6102 S8050 SOT_23 DNP
R6118 10K 5% R0402 — PA_PU

Option3

SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3
SDIO_CMD
SDIO_CLK

UART4_RXD
UART4_TXD
UART4_RTS

PCM_CLK
PCM_SYNC
PCM_OUT
PCM_IN

BT_REG_ON
BT_WAKE_HOST
WIFI_WAKE_HOST
HOST_WAKE_BT

SDIO_D0   R6200   1   22R   5%   RTL8723DS_D0
                           R0402
SDIO_D1   R6201   1   22R   5%   RTL8723DS_D1
                           R0402
SDIO_D2   R6202   1   22R   5%   RTL8723DS_D2
                           R0402
SDIO_D3   R6203   1   22R   5%   RTL8723DS_D3
                           R0402
SDIO_CMD   R6204   1   22R   5%   RTL8723DS_CMD
                           R0402
SDIO_CLK

VCC_IO

C6201   C6202   C6200 4.7uF C0402 X5R 6.3V
100nF   100nF
C0402   C0402
X5R   X5R
16V   16V

R6206
0R
R0402
5%

C6203
10uF
C0603
X5R
6.3V

VCC_IO

R6205
10K
R0402
5%
DNP

VBAT_EN

R6208
10K
R0402
5%

BT_REG_ON

CLK_32K_OUT   R6207
               0R
               R0402
               5%

L6200 2.2uH
IND_252010
0.225ohm

VDD1P25

C6205   C6206
4.7uF   100nF
C0402   C0402
X5R   X5R 50V
6.3V

REALTEK
RTL8723DS

GND   49

C6204 100nF C0402 X5R 16V   VD33   1   VA33_PA_S0
C6207 100nF C0402 X5R 16V   VD33   VA33_PAD_S0
C6208 100nF C0402 X5R 16V   VDD1P25 3 VA1P25_RTX_S0

R6209
DNP
VD33   WIFI_REG_ON   4   WL_DISn#/GPIO9
100K
R0402
5%

C6209 100nF C0402 X5R 16V   VDD1P25 5 VA1P25_BT_SYN
C6210 100nF C0402 X5R 16V   VD33   6 VA33_BT_SYN
C6211 100nF C0402 X5R 16V   VD33   7 VA33_WL_SYN
C6212 100nF C0402 X5R 16V   VDD1P25 8 VA1P25_WL_SYN
C6213 100nF C0402 X5R 16V   VDD1P25 9 VA1P25_RTX_S1
C6215 100nF C0402 X5R 16V   VD33   10 VA33_PAD_S1

ANT_JACK
ANT_JACK
ANT6200

ANT1   11 RFIO_BTG_S1

GND1
GND2

C6217   L6201   C6218
1.8pF   2.4nH   9pF   C6216 100nF C0402 X5R 16V   VD33   12 VA33_PA_S1
C0402   L0402   C0402
C0G   C0G
50V   50V

SW_LX   36
SW_GND   35
SD_D2   34   RTL8723DS_D2
SD_D3/GSPI_CSn 33   RTL8723DS_D3
SD_CMD/ GSPI_DI 32   RTL8723DS_CMD
SD_CLK/ GSPI_CLK 31   SDIO_CLK
SD_D0/GSPI_DO 30   RTL8723DS_D0
SD_D1/ GSPI_INT 29   RTL8723DS_D1
VDD_IO   28
UART_OUT 27   UART4_RXD
UART_CTS 26   UART4_RTS   R6210 2 DNP 10K R0402 5%
UART_IN 25   UART4_TXD

VCCIO_SDIO

C6214   C0402
100nF   X5R 16V

RTL8723DS_QFN48

C6219   C6220
100nF   100nF
C0402   C0402
X5R   X5R
16V   16V

SPS_LDO_SEL

LDO_MODE:
R6012=100K R6013=DNP L6000=0R

SPS_MODE:
R6012=DNP   R6013=100K   L6000=2.2uH

VCCIO_SDIO

R6211 1   2 0R R0402 5%   PCM_CLK
R6212 1   2 0R R0402 5%   PCM_SYNC
R6213 1   2 0R R0402 5%   PCM_IN
R6214
DNP
100K
R0402
5%

R6215 1   2 0R R0402 5%

1.25V Supply Mode Selection:
H_LDO/L_SPS

R6216
100K
R0402
5%

R6217 150R
R0402 5%

REF_CLK_OUT   1   2

L6202
470nH
150mA
5%
L0805

C6221 C0G 50V
100pF C0402

C6222
82pF
50V
C0402

XI

Y6200
X1   GND
GND   X2
DNP 24MHz
CRY4_3R20X2R50X0R80

C6223
DNP
15pF
C0G
50V
C0402

XO

C6224
DNP
15pF
C0G
50V
C0402

PCM_OUT

Rockchip
瑞芯微电子   Fuzhou Rockchip Electronics

Project: RK3308_AI-VA_MB_REF
File: 62.WIFI/BT COB-RTL8723DS
Date: Wednesday, July 04, 2018   Rev: 1.1
Designed by: Joseph   Sheet: 36 of 51

10/100M PHY-RTL8201F

This is a schematic diagram (Page 37 of 51) for the RK3308_AI-VA_MB_REF project — "65.10/100M PHY-RTL8201F" by Fuzhou Rockchip Electronics, designed by Joseph, dated Wednesday, July 04, 2018, Rev 1.1.

Option Table

	25MHz Crystal	NO 25MHz Crystal (Default)
Option1	0R	DNP
Option2	DNP	10K
Option3	DNP	0R
Option4	Be mounted	Not be mounted
Option5	R6518=4.7K R6519=DNP	R6518=DNP R6519=4.7K

RMII REF_CLK direction

Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

MII/RMII Selection

Pull High for RMII mode(default)

UTP / Fiber Selection

Pull Low for UTP Mode(default)
Pull High for Fiber Mode

PHY Address/LED

WOL/LED0 Selection

Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

POWER

Headphone

VCC_1V8_CODEC

R7000
100K
5%
R0402

PHONE_DET

Q7000 WNM2016-3/TR
SOT_23

C7000 47uF   E-A 6.3V
HPOUT_R

C7001 47uF   E-A 6.3V
HPOUT_L

Q7001 WNM2016-3/TR
SOT_23

R7001
470R
5%
R0402

R7002
470R
5%
R0402

PHONE_CTL

R7005
300K
5%
R0402

C7002
100nF
X5R
16V
C0402

R7003
DNP
22R
5%
R0402

R7004
DNP
22R
5%
R0402

C7003
DNP
100nF
X5R
16V
C0402

C7004
DNP
100nF
X5R
16V
C0402

ED7000
ESD5451N
ESD0402

ED7001
ESD5451N
ESD0402

ED7002
ESD5451N
ESD0402

J7000

PJ35106SY-P10
PJ6_D3R50_PJ35106SY-P10

LineIn Jack

J7001

LINE_IN   C7005 1uF   X5R C0402 6.3V

LINE_IN2   C7006 1uF   X5R C0402 6.3V

ED7003
ESD0402
ESD5451N

ED7004
ESD0402
ESD5451N

PJ35106SY-P10
PJ6_D3R50_PJ35106SY-P10

Rockchip
瑞芯微电子
Fuzhou Rockchip Electronics

Project:	RK3308_AI-VA_MB_REF
File:	70.AUDIO_Headphone/LineIn

Date:	Wednesday, July 04, 2018	Rev:	1.1
Designed by:	Joseph	Sheet:	38 of 51

AUDIO_PowerAmp-Analog

OUTPUT LC FILTER

EMI C-RC SNUBBER

VCC12V_PA

GND_PA

U7100
XA9220
/TPA3110

Power PAD

Pin	Name		Name	Pin
1	SD		PVCCL1	28
2	FAULT		PVCCL2	27
3	LINP		BSPL	26
4	LINN		OUTPL	25
5	GAIN0		PGND1	24
6	GAIN1		OUTNL	23
7	AVCC		BSNL	22
8	AGND		BSNR	21
9	GVDD		OUTNR	20
10	PLIMIT		PGND2	19
11	RINN		OUTPR	18
12	RINP		BSPR	17
13	NC		PVCCR1	16
14	PBTL		PVCCR2	15

AMP_SD#
AMP_FAULT
AMP_LINP
AMP_LINN
GAIN0
GAIN1

LINEOUT_L
LINEOUT_R
SPK_MUTE

AMP_RINN
AMP_RINP

C7100 1nF X5R 50V C0402
C7101 100nF X5R 25V C0402
CM7100 100uF/25V MTM-C

C7128 1nF X5R 50V C0402
C7129 100nF X5R 25V C0402
CM7101 100uF/25V MTM-C

L7101 IND_606045 15uH 3.4A 80mohm
L7103 IND_606045 15uH 3.4A 80mohm
L7104 IND_606045 15uH 3.4A 80mohm
L7107 IND_606045 15uH 3.4A 80mohm

SPEAKL1_P
SPEAKL1_N
SPEAKR1_P
SPEAKR1_N

J7100 JACK_1500_2P
J7101 JACK_1500_2P

ED7101 ESD9N12BA ESD0402
ED7100 ESD9N12BA ESD0402
ED7102 ESD9N12BA ESD0402
ED7103 ESD9N12BA ESD0402

Loopback

SPKL1_P
SPKL1_N
SPKR1_P
SPKR1_N

Ra R7127 22K R0402 5%   A SPKR1_P
Rb R7134 22K R0402 5%   B

Rc R7124 22K R0402 1%   C SPKL1_P
Rd R7135 22K R0402 1%   D

C7131 1nF X5R 50V C0402
C7135 1nF X5R 50V C0402
C7132 1nF X5R 50V C0402
C7136 1nF X5R 50V C0402

R7129 1.8K 1% R0402
R7136 1.8K 1% R0402
R7137 1.8K 1% R0402
R7138 1.8K 1% R0402

SPEAKR1_P
SPEAKR1_N
SPEAKL1_P
SPEAKL1_N

Adjust the value of Ra\Rb\Rc\Rd to make sure the DC offset Voltage
of Point A\B\C\D is less than 500mV.
Set the Boost PGA register to 0dB for loopback recording,
and fine tune the ALC register for adjustment of wave amplitudes
that algorithms require.

PCB Note:
GND_PA plane for Audio Amplifier,
separate from GND plane.

R7131 0R R0805 5%
R7133 0R R0805 5%

R7128 22R 5% R0402
R7123 0R 5% R0402
SPK_MUTE   AMP_SD#   AMP_FAULT

VCC12V_PA
R7119 DNP R0402
R7125 100K 5% R0402
GAIN0

VCC12V_PA
R7120 DNP R0402
R7126 100K 5% R0402
GAIN1

GND_PA

ROCKCHIP 瑞芯微电子   Fuzhou Rockchip Electronics

Project:	RK3308_AI-VA_MB_REF
File:	71.AUDIO_PA-XA9220/TPA3110
Date:	Wednesday, July 04, 2018
Rev:	1.1
Designed by:	Joseph
Sheet:	39 of 51

AUDIO_PowerAmp-Digital

LCDC_DEN/I2S1_SCLK_TX_M0 — R7200 1 22R 2 5% R0402 — I2S1_SCLK_TX_M0
LCDC_D1/I2S1_LRCK_TX_M0 — R7201 1 22R 2 5% R0402 — I2S1_LRCK_TX_M0
LCDC_D3/I2S1_SDO0_M0 — R7202 1 22R 2 5% R0402 — I2S1_SDO0_M0
LCDC_D7/I2S1_SDI0_M0 — R7203 1 22R 2 5% R0402 — I2S1_SDI0_M0

I2C1_SDA
I2C1_SCL
SPK_MUTE

Power

VCC_IO — R7211 1 0R 5% 2 R0603 — VDD_AMP

VDD_AMP
R7207 1 10K 5% R0402 2 — AMP_ERROR
R7208 1 DNP 10K 5% R0402 2

Note:
Device ID 7bit
due to ERROR pin state during power up

AMP_ERROR	Address of I2C
H	0x31
	0x30

**Remind: Loopback from Digital Amplifier
Get PCM Data at Post-Process Point**

VDD_AMP

R7205 DNP 1M 5% R0402

SPK_MUTE — R7215 1 DNP 0R 5% R0402 2 — AMP_ERROR

C7210 DNP 1uF X5R 6.3V C0402

U7200

ERROR	1	VDDL	23
PD		BST_LA	24
LRCIN	3	LA	22
BCLK	4	GNDL	21
SDATA	5	LB	20
SDATAO	8	BST_LB	19
SDA	6	BST_RA	18
SCL		RA	17
DVDD	9	GNDR	16
DGND	10	RB	15
VREG	11	BST_RB	13
GVDD	12	VDDR	14

Thermal Pad

XA8326
@AD82584F

PAD 25

I2S1_LRCK_TX_M0
I2S1_SCLK_TX_M0
I2S1_SDO0_M0
I2S1_SDI0_M0
I2C1_SDA
I2C1_SCL

C7215 1uF X5R 6.3V C0402
C7216 100nF X5R 16V C0402

VREG
GVDD
C7219 1uF X5R 25V C0603
C7220 1uF X5R 25V C0603
C7221 100nF X5R 25V C0402

VCC12V_PA

Place closed to pins.

CM7200 100uF/25V MTM-C
C7203 1uF X5R 25V C0603
C7204 100nF X5R 25V C0402

R7204 10R 5% R0402 DNP
R7206 DNP 10R 5% R0402
R7209 470pF DNP 50V X5R C0402

C7207 1 22nF 2 C0402 X5R 25V
C7211 1 22nF 2 C0402 X5R 25V
C7212 1 22nF 2 C0402 X5R 25V
C7213 1 22nF 2 C0402 X5R 25V

VCC12V_PA

Place closed to pins.

CM7201 100uF/25V MTM-C
C7223 1uF X5R 25V C0603
C7224 100nF X5R 25V C0402

R7209 10R 5% R0402 DNP
R7210 DNP 10R 5% R0402
C7227 470pF DNP 50V X5R C0402

Wide&Short

C7200 470pF X5R 50V C0402 DNP
L7200 15uH 3.4A IND_606045 80mohm
C7201 2.2uF X5R 25V C0603
C7205 220nF X5R 25V C0402

C7209 470pF DNP 50V X5R C0402
L7201 15uH 3.4A IND_606045 80mohm
C7206 2.2uF X5R 25V C0603

C7202 DNP 1nF X5R 50V C0402
ED7200 ESD9N12BA ESD0402

C7208 DNP 1nF X5R 50V C0402
ED7201 ESD9N12BA ESD0402

J7200 1 2 JACK_1500_2P

Wide&Short

Layout Note:Place close to speaker jack.

C7214 470pF X5R 50V C0402 DNP
L7202 15uH 3.4A IND_606045 80mohm
C7217 2.2uF X5R 25V C0603
C7222 220nF X5R 25V C0402

C7225 2.2uF X5R 25V C0603
L7203 15uH 3.4A IND_606045 80mohm

C7218 DNP 1nF X5R 50V C0402
ED7202 ESD9N12BA ESD0402

C7226 DNP 1nF X5R 50V C0402
ED7203 ESD9N12BA ESD0402

J7201 1 2 JACK_1500_2P

Wide&Short

AUDIO_PowerAmp-Analog

Loopback

3W/4ohm

VCC_AMP

U7300 XA8872
INN VOP
AB/D
CTRL VON
VREF GND VDD

D Mode.

LINEOUT_L
LINEOUT_R
SPK_MUTE

SPKL1_P
SPKL1_N
SPKR1_P
SPKR1_N

LINEOUT_R C7302 100nF C0402 X5R 16V R7301 47K 5% R0402
SPK_MUTE
AB/D R7304 10K 5% R0402
AB/D R7305 10K 5% R0402 DNP
C7306 100nF X5R 16V C0402

C7300 100nF X5R 16V C0402
C7301 10uF X5R 10V C0603

FB7300 600R-100M L0603 500mA 25% C7303 1nF X5R 50V C0402 SPEKR_P
FB7301 600R-100M L0603 500mA 25% SPEKR_N C7309 1nF X5R 50V C0402

ED7300 ESD9N12BA ESD0402
ED7301 ESD5451N ESD0402
J7300 JACK_1500_2P

SPKR_P R7300 1.8K 1 2 R0402 1% R7302 3.3K 1 2 R0402 1% C7305 2.2nF X5R 50V C0402 A SPKR1_P
Ra
R7303 390R R0402 1% C7304 22nF X5R 25V C0201
R7306 390R R0402 1% C7307 22nF X5R 25V C0402 R7308 3.3K 1 2 R0402 1% C7308 2.2nF X5R 50V C0402
SPKR_N R7307 1.8K 1 2 R0402 1% B SPKR1_N
Rb

Adjust the value of Ra\Rb\Rc\Rd to make sure the DC offset Voltage
of Point A\B\C\D is less than 500mV.
Set the Boost PGA register to 0dB for loopback recording,
and fine tune the ALC register for adjustment of wave amplitudes
that algorithms require.

VCC_AMP

U7301 XA8872
INN VOP
AB/D
CTRL VON
VREF GND VDD

D Mode.

LINEOUT_L C7312 100nF C0402 X5R 16V R7310 47K 5% R0402
AB/D
SPK_MUTE R7313 10K 5% R0402
C7316 100nF X5R 16V C0402

C7310 100nF X5R 16V C0402
C7311 10uF X5R 10V C0603

FB7302 600R-100M L0603 500mA 25% C7313 1nF X5R 50V C0402 SPEKL_P
FB7303 600R-100M L0603 500mA 25% SPEKL_N C7319 1nF X5R 50V C0402

ED7302 ESD9N12BA ESD0402
ED7303 ESD5451N ESD0402
J7301 JACK_1500_2P

SPKL_P R7311 1.8K 1 2 R0402 1% R7309 3.3K 1 2 R0402 1% C7315 2.2nF X5R 50V C0402 C SPKL1_P
Rc
R7312 390R R0402 1% C7314 22nF X5R 25V C0402
R7314 390R R0402 1% C7317 22nF X5R 25V C0402 R7316 3.3K 1 2 R0402 1% C7318 2.2nF X5R 50V C0402
SPKL_N R7315 1.8K 1 2 R0402 1% D SPKL1_N
Rd

Option1 VCC5V0_SYS R7317 0R R0805 5% VCC_AMP
Option2 VCC5V0_PA R7318 DNP 0R R0805 5% Only for 1Cell Battery scheme

MIC Array-Analog

Remind:
The Main Board is separate from MIC Arrary Board.
the Reference of Analog MIC Array Board please refer to
《RK3308_AI-VA_MIC_REF_V11》

VCC5V0_SYS

Note:All the Power filter capacitors should be placed close to the connector.

MICN3
MICP3
MICN4
MICP4
MICN5
MICP5
MICN6
MICP6
MICN7
MICP7
MICN8
MICP8

C7400
100nF
X5R
16V
C0402

C7401
4.7uF
X5R
10V
C0603

GND_32
32

ESD0402 ESD5451N DNP   2   1 ED7400   ADC_KEY_IN1
ESD0402 ESD5471X DNP   2   1 ED7401   MICN7
ESD0402 ESD5471X DNP   2   1 ED7402   MICP8
ESD0402 ESD5471X DNP   2   1 ED7403   MICN3
ESD0402 ESD5471X DNP   2   1 ED7404   MICP4
ESD0402 ESD5471X DNP   2   1 ED7405   MICN5
ESD0402 ESD5471X DNP   2   1 ED7406

MICBIAS1
MICP6
MICBIAS1
I2C1_SDA

ADC_HW_ID1   ED7408 1   2 DNP ESD5451N ESD0402
MICP7   ED7409 1   2 DNP ESD5471X ESD0402
MICN8   ED7410 1   2 DNP ESD5471X ESD0402
MICP3   ED7411 1   2 DNP ESD5471X ESD0402
MICN4   ED7412 1   2 DNP ESD5471X ESD0402
MICP5   ED7413 1   2 DNP ESD5471X ESD0402
MICN6   ED7414 1   2 DNP ESD5471X ESD0402

MICBIAS2
MICBIAS2
MIC_LED_EN
I2C1_SCL

GND_31
31

I2C1_SDA
I2C1_SCL
MIC_LED_EN
ADC_KEY_IN1
ADC_HW_ID1

C7405
100nF
X5R
16V
C0402

ED7407
DNP
ESD5471X
ESD0402

C7404
100nF
X5R
16V
C0402

ED7415
DNP
ESD5471X
ESD0402

J7400
30PIN FPC CON
CNN30_1R00_FP05SL_V

MIC Array-Digital

VCC5V0_SYS

Note:All the Power filter capacitors should be
placed close to the connector.

I2S0_MCLK
I2S0_SCLK_TX
I2S0_SCLK_RX/PDM_CLK
I2S0_LRCK_TX
I2S0_LRCK_RX
I2S0_SDO0
I2S0_SDO1
I2S0_SDO2
I2S0_SDO3
I2S0_SDI0/PDM_SDI0
I2S0_SDI1/PDM_SDI1
I2S0_SDI2/PDM_SDI2
I2S0_SDI3/PDM_SDI3
I2C1_SDA
I2C1_SCL
MIC_LED_EN
ADC_KEY_IN1
SPI0_RX
SPI0_TX
SPI0_CLK/I2C2_SDA
SPI0_CS/I2C2_SCL
ADC_HW_ID1
MIC_LED_EN

VCC_IO

C7500
4.7uF
X5R
10V
C0603

C7501
100nF
X5R
16V
C0402

C7502
4.7uF
X5R
10V
C0603

C7503
100nF
X5R
16V
C0402

ADC_HW_ID1

ED7500
DNP
ESD5451N
ESD0402

VCC_1V8

C7504
100nF
X5R
16V
C0402

C7505
4.7uF
X5R
10V
C0603

J7500
30PIN FPC CON
CNN80_1R00_FP05SL_V

GND_32
GND_31

ADC_KEY_IN1   ED7501 1   2 DNP ESD5451N ESD0402
R7500 1 22R 2 5% R0402 I2S0_MCLK   ED7507 1   2 DNP ESD5451N ESD0402
R7501 1 22R 2 5% R0402 I2S0_SCLK_RX/PDM_CLK   ED7508 1   2 DNP ESD5451N ESD0402
R7502 1 22R 2 5% R0402 I2S0_SCLK_TX   ED7509 1   2 DNP ESD5451N ESD0402
R7503 1 22R 2 5% R0402 I2S0_LRCK_RX   ED7510 1   2 DNP ESD5451N ESD0402
R7504 1 22R 2 5% R0402 I2S0_LRCK_TX   ED7511 1   2 DNP ESD5451N ESD0402
R7506 1 22R 2 5% R0402 I2S0_SDO1   ED7512 1   2 DNP ESD5451N ESD0402
R7508 1 22R 2 5% R0402 I2S0_SDO3   ED7513 1   2 DNP ESD5451N ESD0402
R7510 1 22R 2 5% R0402 I2S0_SDI1/PDM_SDI1   ED7514 1   2 DNP ESD5451N ESD0402
R7512 1 22R 2 5% R0402 I2S0_SDI3/PDM_SDI3   ED7515 1   2 DNP ESD5451N ESD0402
MIC_LED_EN   ED7516 1   2 DNP ESD5451N ESD0402
I2C1_SCL   ED7517 1   2 DNP ESD5451N ESD0402

ESD0402 ESD5471X DNP 2   1 ED7502 I2S0_SDO0   R7505 1 22R 2 5% R0402
ESD0402 ESD5471X DNP 2   1 ED7503 I2S0_SDO2   R7507 1 22R 2 5% R0402
ESD0402 ESD5471X DNP 2   1 ED7504 I2S0_SDI0/PDM_SDI0 R7509 1 22R 2 5% R0402
ESD0402 ESD5471X DNP 2   1 ED7505 I2S0_SDI2/PDM_SDI2 R7511 1 22R 2 5% R0402
ESD0402 ESD5471X DNP 2   1 ED7506 I2C1_SDA

I2C/SPI CONNECTOR

APIO2_VDD

J7501
SPI0_RX   1   2 SPI0_CLK/I2C2_SDA
SPI0_TX   3   4 SPI0_CS/I2C2_SCL
             5   6
CON6C

C7506
100nF
X5R
16V
C0402

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Project:	RK3308_AI-VA_MB_REF
File:	75.MIC Array Connector-Digital
Date:	Wednesday, July 04, 2018	Rev: 1.1
Designed by:	Joseph	Sheet: 43 of 51

SPDIF_OUT(Optical)

SPDIF_TX

R8100 1 2 22R 5%
R0402

C8100
DNP
22pF
C0G
50V
C0402

D8100
ESD5471X
ESD0402

VCC_IO

DJ8100
1
2
3
Drive IC LED
DLT2160A
DLT2160A

C8101
4.7uF
X5R
10V
C0603

C8102
100nF
X5R
16V
C0402

D8101
ESD5451N
ESD0402

SPDIF_IN(Optical)

SPDIF_RX

R8101 1 2 22R 5%
R0402

C8103
DNP
22pF
C0G
50V
C0402

D8102
ESD5471X
ESD0402

Note:
DLR2150 Support 25Mbps

VCC_IO

DJ8101
1
2
3
Receive IC
DLR2150
DLR2150

C8104
4.7uF
X5R
10V
C0603

C8105
100nF
X5R
16V
C0402

D8103
ESD5451N
ESD0402

SPDIF_OUT(Coaxial)

Option2

VCC5V0_SYS

L8200
180R-100M
L0603
DNP

C8200
DNP
10uF
X5R
10V
C0603

R8200
DNP
1.5K
5%
R0402

Q8200
DNP
S8050
SOT_23

SPDIF_TX

C8201 100nF
DNP
X5R 16V
C0402

R8201
DNP
2.2K
5%
R0402

R8202
DNP
3.3K
5%
R0402

R8203 75R
DNP 5% R0402

R8204
DNP
220R
5%
R0402

C8202
DNP 16V X5R
100nF C0402

Coaxial_SPDIF

R8205
DNP
100K
5%
R0402

ED8200
ESD5471X
ESD0402

JP8200
AV1-84-5G
AV1-84-5G

Option1

C8203 1uF
X5R 10V
C0402

R8206 240R 1%
R0402

R8207
110R
1%
R0402

SPDIF_IN(Coaxial)

C8204 100nF C0402 X5R 16V

VCC_IO

U8200
FIN1002
SOT_23_5

SPDIF_RX

VCC_IO

C8205
100nF
X5R
16V
C0402

ROUT 5

VCC 1

GND 2

RIN+ 3

RIN- 4

R8208
75R
1%
R0402

R8209
DNP
R0402

ED8201
ESD5471X
ESD0402

JP8201
AV1-84-5G
AV1-84-5G

R8210
0R
5%
R0402

C8206
DNP
100nF
X5R
16V
C0402

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Project:	RK3308_AI-VA_MB_REF
File:	82.SPDIF IN/OUT-Coaxial
Date:	Wednesday, July 04, 2018	**Rev:** 1.1
Designed by:	Joseph	**Sheet:** 45 of 51

Encryption chip

I2C1_SDA

I2C1_SCL

Note:
For MicArray Algorithm Use Only

U8600
ATSHA204A-SSHDA-T
SOP8_5R00X4R00X1R75

1	NC1	VCC	8
2	NC2	NC4	7
3	NC3	SCL	6	I2C1_SCL
4	GND	SDA	5	I2C1_SDA

VCC_IO

C8600
100nF
X5R
16V
C0402

TF Card

SDMMC_D0
SDMMC_D1
SDMMC_D2/UART2_RX_M1
SDMMC_D3/UART2_TX_M1
SDMMC_CMD

SDMMC_CLK
SDMMC_PWREN
SDMMC_DET

VCC_IO   VCC_SD

R9100   1 DNP   2 0R   5%
                        R0402

C9100
100nF
X5R
16V   Q9100   D9100   R9110
C0402   WPM2015-3/TR   ESD5451N   10K
           SOT_23   ESD0402   R0402
                                           5%

SDMMC_PWREN   1 R9101 2
                      10K 5%
                      R0402

VCC_SD

SDMMC_D2/UART2_RX_M1   R9103 1 22R 2 5% R0402   1 DATA2
SDMMC_D3/UART2_TX_M1   R9104 1 22R 2 5% R0402   2 CD/DATA3
SDMMC_CMD   R9105 1 22R 2 5% R0402   3 CMD
                                                         4 VDD
SDMMC_CLK   5 CLK
                                                         6 VSS
SDMMC_D0   R9106 1 22R 2 5% R0402   7 DATA0
SDMMC_D1   R9107 1 22R 2 5% R0402   8 DATA1
SDMMC_DET   R9102 1 22R 2 5% R0402   9 CD

J9100
TF_SD_SOCKET
TF-CKT01-009D

G4 G3 13 12
G1 G2 10 11

C9101   C9102
100nF   10uF
X5R   X5R
16V   6.3V
C0402   C0603

Close to TF

D9101   D9102   D9103   D9104   D9105   D9106   D9107
ESD5451N   ESD5471X   ESD5471X   ESD5471X   ESD5471X   ESD5471X   ESD5471X
ESD0402   ESD0402   ESD0402   ESD0402   ESD0402   ESD0402   ESD0402

Note:ESD5471X(Cj=9pF)
If TF Card word in SDMMC 2.0 mode,
ESD5471X is OK for SDMMC 2.0 mode.
If TF Card word in SDMMC3.0 mode,
need select smaller Junction capacitance of ESD,
Recommend ESD5341N:Cj=1pF.

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Project: RK3308_AI-VA_MB_REF
File: 91.TF Card
Date: Wednesday, July 04, 2018   Rev: 1.1
Designed by: Joseph   Sheet: 47 of 51

RECOVERY Key

ADC_KEY_IN1

C9200
1nF
C0402
X5R
50V

ED9200
ESD5451N
ESD0402

R9200 1 10K 2 1% R0402 VCC_1V8

R9201 1 100R 2 5% R0402

SW9200
Recovery

Note:C9200 should be placed
close to the A19 pin of RK3308

RESET Key

RESET

R9203 1 100R 2 5% R0402

SW9201
Reset

D9200
ESD5451N
ESD0402

IR Receiver

As IR_RX Funtion

VCC_IO

R9300
22R
5%
R0402

VCC_IO

R9301
4.7K 5%
R0402

DNP
C9300 1   2   4.7uF   X5R 10V
C0603
C9301 1   2   100nF   X5R 16V
C0402

IR_RX/PA_DRV

R9302
22R 5%
R0402

IR_RX

IR_VCC

C9302
1nF
X5R
50V
C0402

IR9300
OQSS-R12
IR-SIR8B39

1
2
3
4

G VS IR G

Project:	RK3308_AI-VA_MB_REF		
File:	93.IR Receiver		
Date:	Wednesday, July 04, 2018	Rev:	1.1
Designed by:	Joseph	Sheet:	49 of 51

Debug UART2

SDMMC_D2/UART2_RX_M1
SDMMC_D3/UART2_TX_M1

SPI2_RX/UART2_RX_M0
SPI2_TX/UART2_TX_M0

SPI2_RX/UART2_RX_M0   R9600 1 DNP 2 22R 5% R0402
SPI2_TX/UART2_TX_M0   R9601 1 DNP 2 22R 5% R0402

CN9600
NC

SDMMC_D2/UART2_RX_M1   R9602 1 22R 5% 2 R0402   UART2_RX   3
SDMMC_D3/UART2_TX_M1   R9603 1 22R 5% 2 R0402   UART2_TX   2
                                                              1

DNP

Layout Note:As soon as possible
reduce the branch of the two signals

1   1
ED9600   ED9601
ESD5451N   ESD5451N
ESD0402   ESD0402
2   2

M9900
MARK

M9901
MARK

M9902
MARK

M9903
MARK

M9904
MARK

M9905
MARK

H9900
HOLE_3R20

H9901
HOLE_3R20

H9902
HOLE_3R20

H9903
HOLE_3R20

HOLE_C3R20_C6R00   HOLE_C3R20_C6R00   HOLE_C3R20_C6R00   HOLE_C3R20_C6R00

SMTSO9900
SMTSO30100CTJ

SMTSO9901
SMTSO30100CTJ

SMTSO9902
SMTSO30100CTJ

SMTSO9903
SMTSO30100CTJ

ROCKCHIP
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Project:	**RK3308_AI-VA_MB_REF**		
File:	**99.MARK/HOLE**		
Date:	Wednesday, July 04, 2018	Rev:	1.1
Designed by:	Joseph	Sheet:	51 of 51