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Note

NOTE 1:

Component parameter description

- 1. DNP stands for component not mounted temporarily
- 2. If Value or option is DNP, which means the area is reserved without being mounted
- 3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:

Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note
Option
Description
Remind

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{|tem}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}



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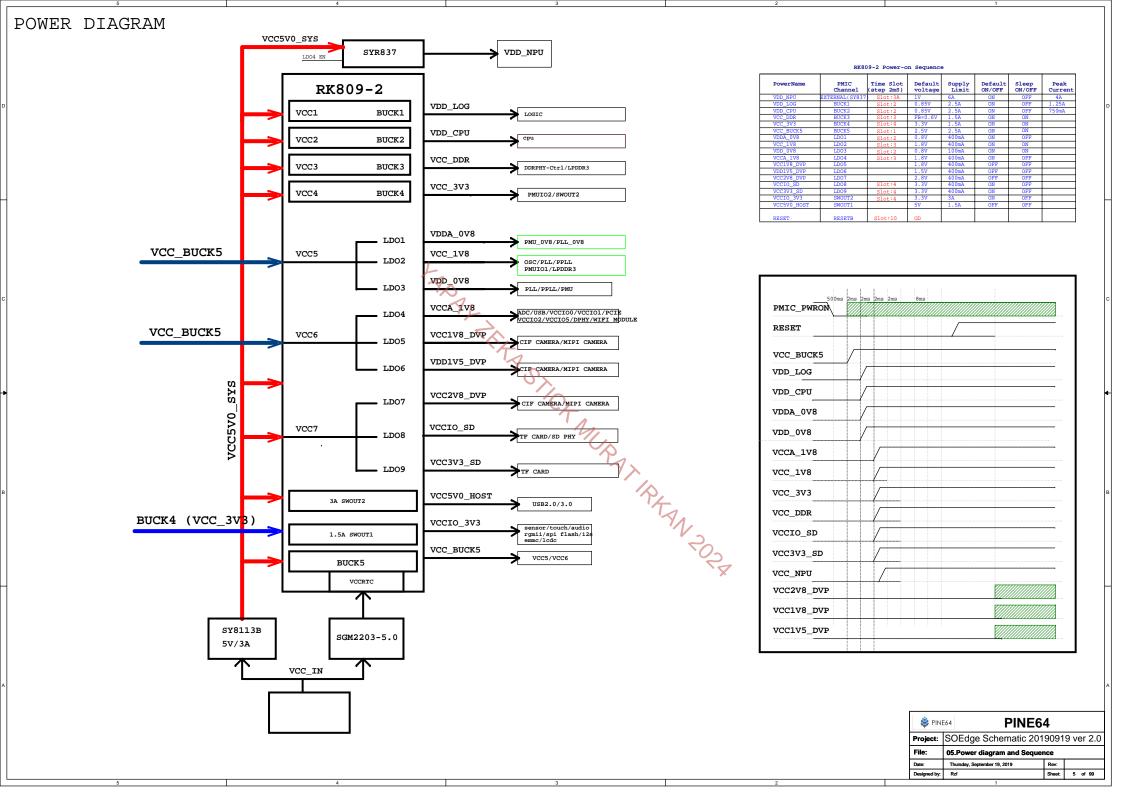
Version	Date	Author	Change List	Approved
V1.0	20181025		First edition for RK1808 ddr4	RZF
V2.0	20190919		SOEdge Schematic Released	
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
12C0	I2C0_SCL/GPI00_B0_u I2C0_SDA/GPI00_B1_u	PMUIO2	I2CO_SCL_PMIC I2CO_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz,400kHz
					SY837		BUCK	100kHz,400kHz
I2C1	I2C1_SCL/GPI00_C0_u I2C1_SDA/GPI00_C1_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC_3V3	GSL1680		Touch IC	100kHz,400kHz
			1					100kHz,400kHz
I2C2	I2C1_SCL/GPI01_B4_U I2C1_SDA/GPI01_B5_U	VCCIO_3V3	70		NC			100kHz,400kHz
			17	<u>ک</u>	MIPI CAMERA			
I2C3	GPIO2_D0/I2C3_SCL_U GPIO2_D1/I2C3_SDA_U	VCCA_1V8		VCCA_1V8	CIF CAMERA			
					BT1120			
				7	DIGITAL MIC			
I2C4	GPIO3_C2/I2C4_SCL_U	VCCIO_3V3			RGB LCD			
1201	GPIO3_C3/I2C4_SDA_U	_		VCCIO_3V3	PCIEX4			
					SENSOR			

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ROCKCHIP RK1808 ARM YAPAY ZEKA USB STICK RK1808 Power RK1808 GÜÇ / SASE (TOPRAK) GND(SASE) U1000P VDD LOG O-OVDD NPU W23 W17 AC25 AA21 L11 VSS_70 VSS_35 AA23 AL11 L13 VSS 69 VSS_36 AC23 AA3 L15 VSS_68 VSS_37 AE23 AE17 L17 VSS_67 Rackchip VSS_38 AJ25 **VSS 66** VSS_39 **E-S GORTA** L21 U25 ->>VDD_NPU_FB VSS_65 VSS_40 VSS_64 1.8volt VSS 63 AC19 W9 **Dual-core ARM Cortex-A35 CPU** AR3 VCC1V8 EFUSE O OVDD CPU VSS 62 AJ27 AW1 VSS_61 AVSS1_3 AV8 AV2 VSS 60 AVSS1 4 C120 AU3 VSS 59 AVSS1_5 100nF RK1808 AW5 **RK1808** VSS 58 AVSS1_6 AU7 X5R 100R R13 VSS_57 AVSS1_7 16V AG13 5% U13 VSS 56 AVSS1_8 R0201 C0201 AC13 VSS 55 AVSS1 9 U3 VSS_54 R25 VSS_53 AVSS2_1 B36 VSS 52 AVSS2 2 ARM BOWERED E33 VSS 51 AVSS2_3 E37 VSS 50 AVSS2 4 C37 VSS 49 AVSS2 5 G33 VSS_48 AVSS2_6 G37 VSS 47 AVSS2 7 L37 AVSS2 8 N37 VSS_45 AVSS2_9 AVSS2_10 R29 AVSS2_11 N33 AVSS2_12 U29 AVSS2_13 | R31 AVSS2_14 W27 AVSS2 15 Rk1808_Socket3 **RK1808** VDD LOG C101 C102 C103 100nF 100nF 100nF 22uF X5R X5R X5R X5R 16V 16V 16V 6.3V C0201 C0201 C0201 C0402 VDD NPU VDD CPU PINE64 ₱ PINE64 C108 C109 C110 C112 C118 C119 C113 C114 C115 C116 100nF 4.7uF 22uF X5R X5R X5R SOEdge Schematic 20190919 ver 2.0 X5R X5R X5R X5R X5R X5R 16V X5R X5R 16V 16V 16V 16V 16V 16V 6.3V 16V 16V 16V X5R 6.3V C0201 C0402 File: 10.RK1808 Power C0603 Thursday, September 19, 2019 Designed by: 10 of 99

