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## Note

### NOTE 1:

#### Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

### NOTE 2:

Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

## Bill of Materials

### Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

### Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}



PINE64

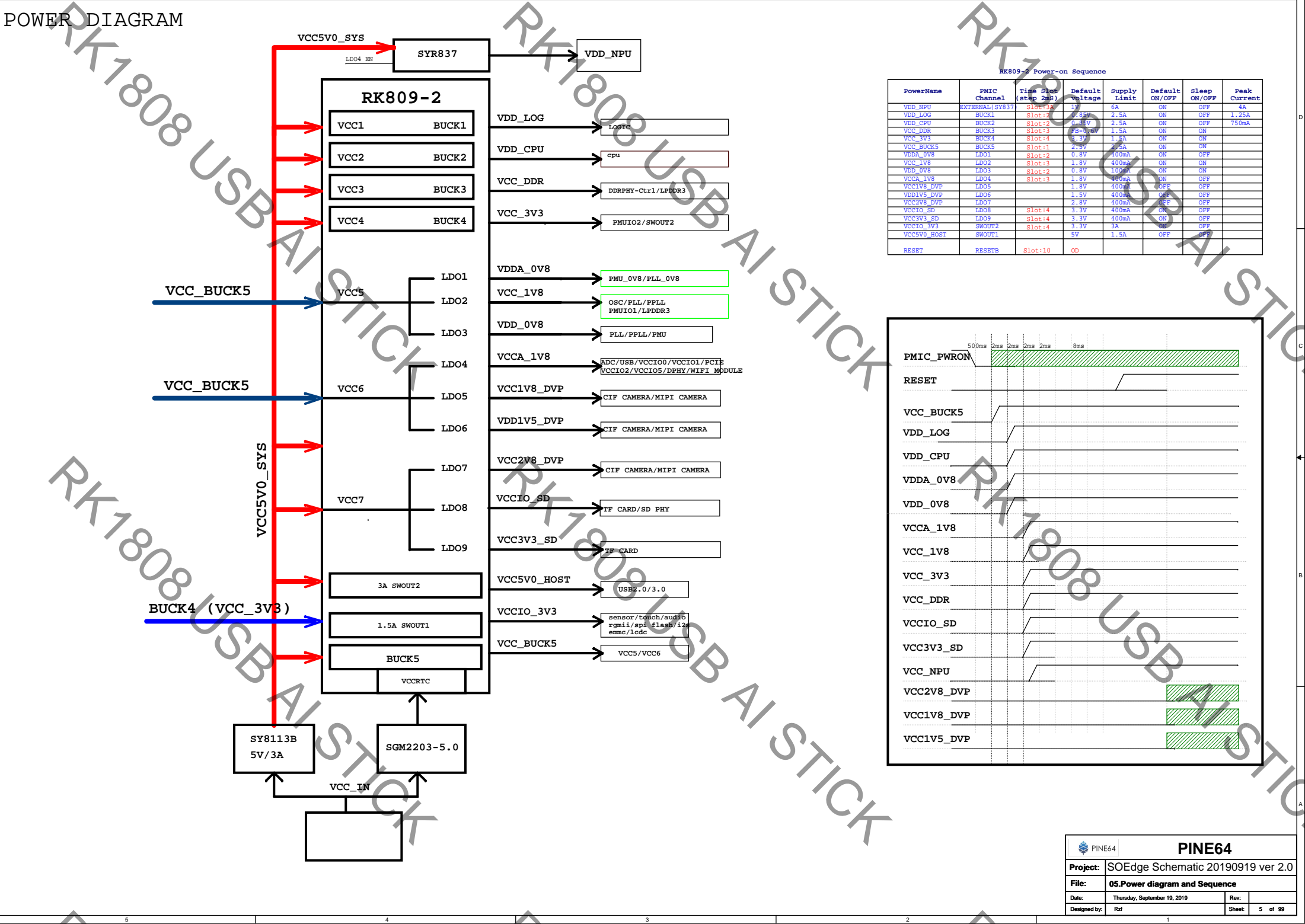
Project:	SOEdge Schematic 20190919 ver 2.0			
File:	01.Index			
Date:	Thursday, September 19, 2019	Rev:		
Designed by:	Rzf	Sheet:	1	of 99



# I2C MAP

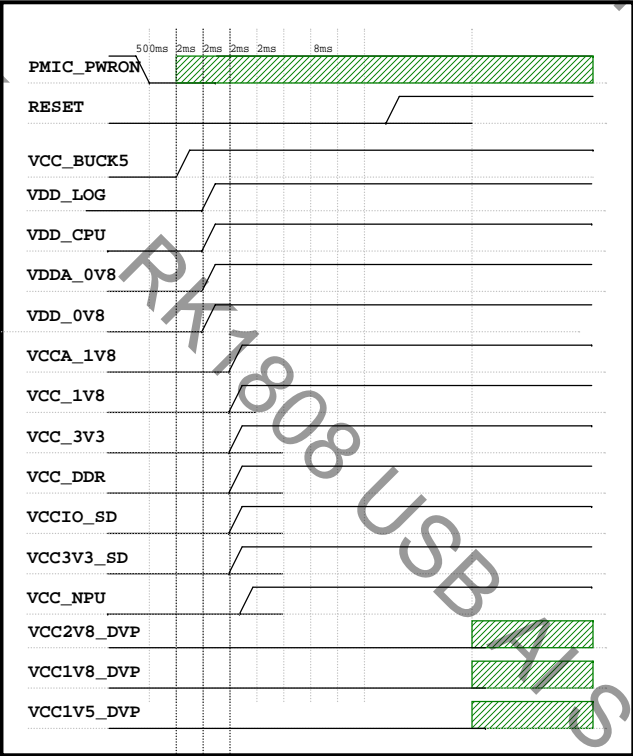
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPIO0_B0_u I2C0_SDA/GPIO0_B1_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz, 400kHz
					SY837		BUCK	100kHz, 400kHz
I2C1	I2C1_SCL/GPIO0_C0_u I2C1_SDA/GPIO0_C1_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC_3V3	GSL1680		Touch IC	100kHz, 400kHz
								100kHz, 400kHz
I2C2	I2C1_SCL/GPIO1_B4_U I2C1_SDA/GPIO1_B5_U	VCCIO_3V3			NC			100kHz, 400kHz
I2C3	GPIO2_D0/I2C3_SCL_U GPIO2_D1/I2C3_SDA_U	VCCA_1V8		VCCA_1V8	MIPI CAMERA			
					CIF CAMERA			
					BT1120			
I2C4	GPIO3_C2/I2C4_SCL_U GPIO3_C3/I2C4_SDA_U	VCCIO_3V3		VCCIO_3V3	DIGITAL MIC			
					RGB LCD			
					PCIEX4			
					SENSOR			

POWER DIAGRAM



RK809-2 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VDD_NPU	EXTERNAL(SY837)	Slot:1	1V	6A	ON	OFF	4A
VDD_LOG	BUCK1	Slot:2	0.95V	2.5A	ON	OFF	1.25A
VDD_CPU	BUCK2	Slot:2	0.8V	2.5A	ON	OFF	750ma
VCC_DDR	BUCK3	Slot:3	FB=0.9V	1.5A	ON	ON	
VCC_3V3	BUCK4	Slot:4	0.3V	1.5A	ON	ON	
VCC_BUCK5	BUCK5	Slot:1	2.8V	2.5A	ON	ON	
VDDA_0V8	LDO1	Slot:2	0.8V	400mA	ON	OFF	
VCC_1V8	LDO2	Slot:3	1.8V	400mA	ON	ON	
VDD_0V8	LDO3	Slot:2	0.8V	100mA	ON	ON	
VCCA_1V8	LDO4	Slot:2	1.8V	400mA	ON	OFF	
VCC1V8_DVP	LDO5	Slot:3	1.8V	400mA	OFF	OFF	
VDD1V5_DVP	LDO6		1.5V	400mA	OFF	OFF	
VCC2V8_DVP	LDO7		2.8V	400mA	OFF	OFF	
VCCIO_SD	LDO8	Slot:4	3.3V	400mA	ON	OFF	
VCC3V3_SD	LDO9	Slot:4	3.3V	400mA	ON	OFF	
VCCIO_3V3	SWOUT2	Slot:4	3.3V	5A	ON	OFF	
VCC5V0_HOST	SWOUT1		5V	1.5A	OFF	OFF	
RESET	RESETB	Slot:10	0D				

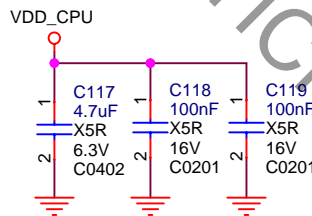
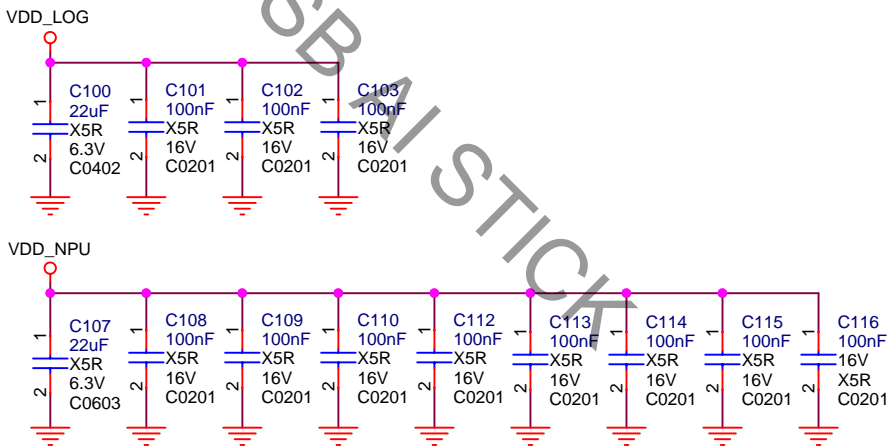
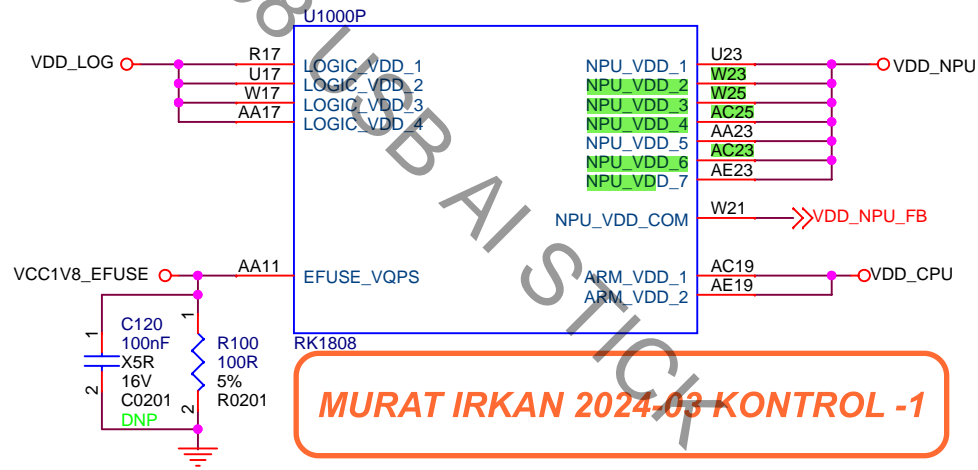


RK1808 Power

# RK1808 YAPAY ZEKA STICK

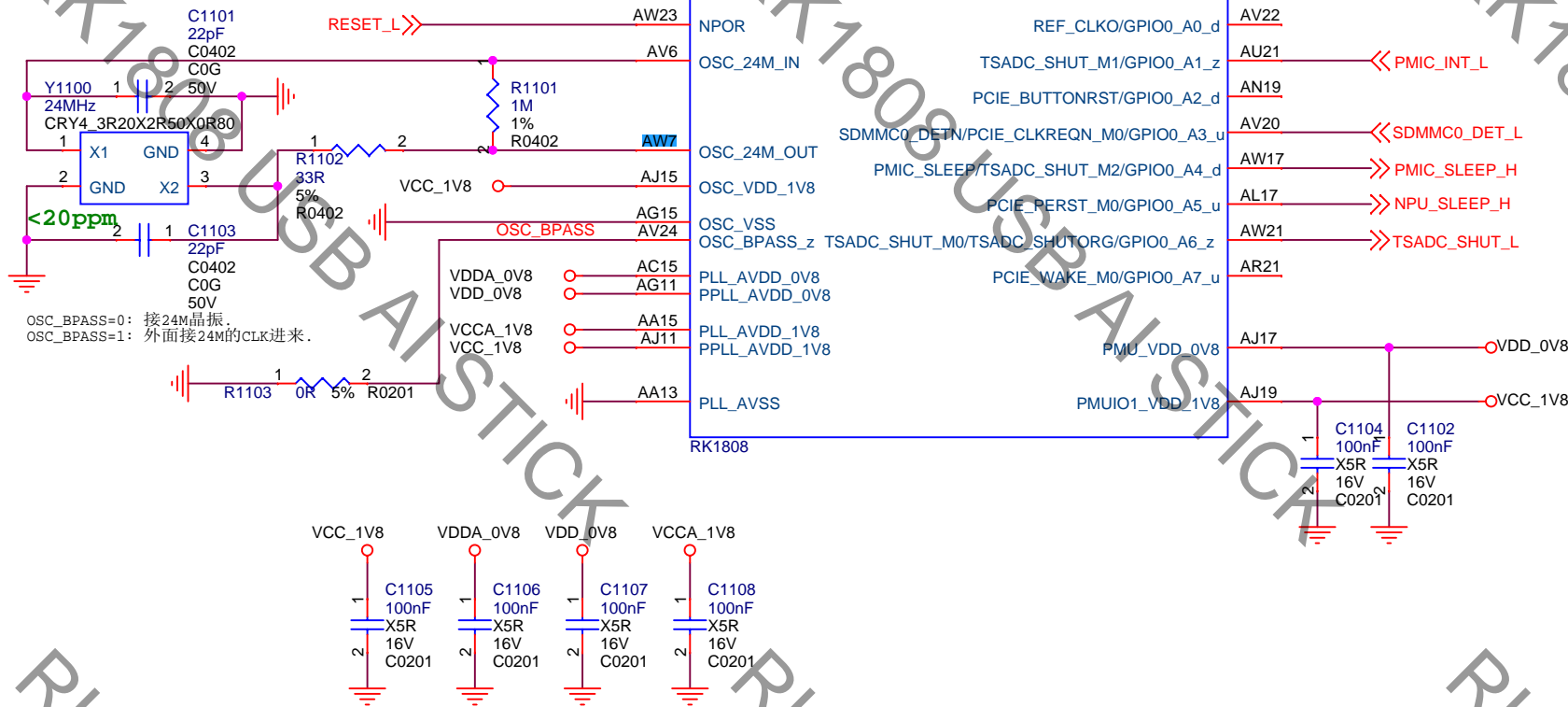
02/22/2024 03:11 AM

## YAPAY ZEKA -USB STICK GÜÇ SİSTEMİ

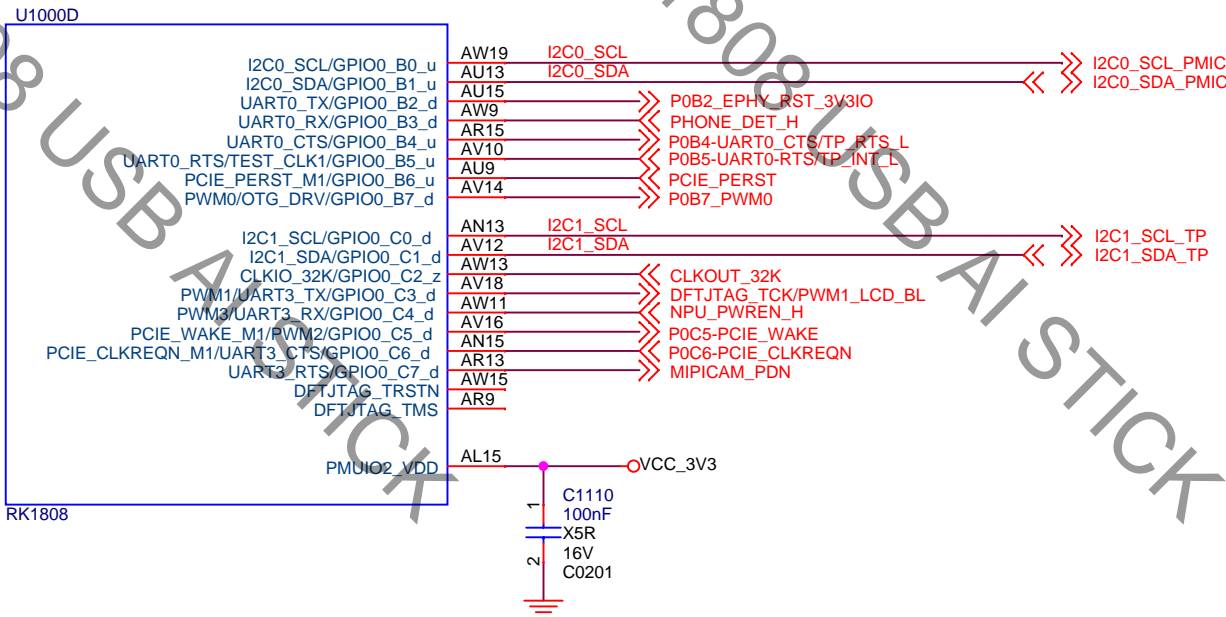



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Project:	SOEdge Schematic 20190919 ver 2.0
File:	10.RK1808 Power
Date:	Thursday, September 19, 2019
Designed by:	Rzf
Rev:	
Sheet:	10 of 99

## PMUIO1/OSC

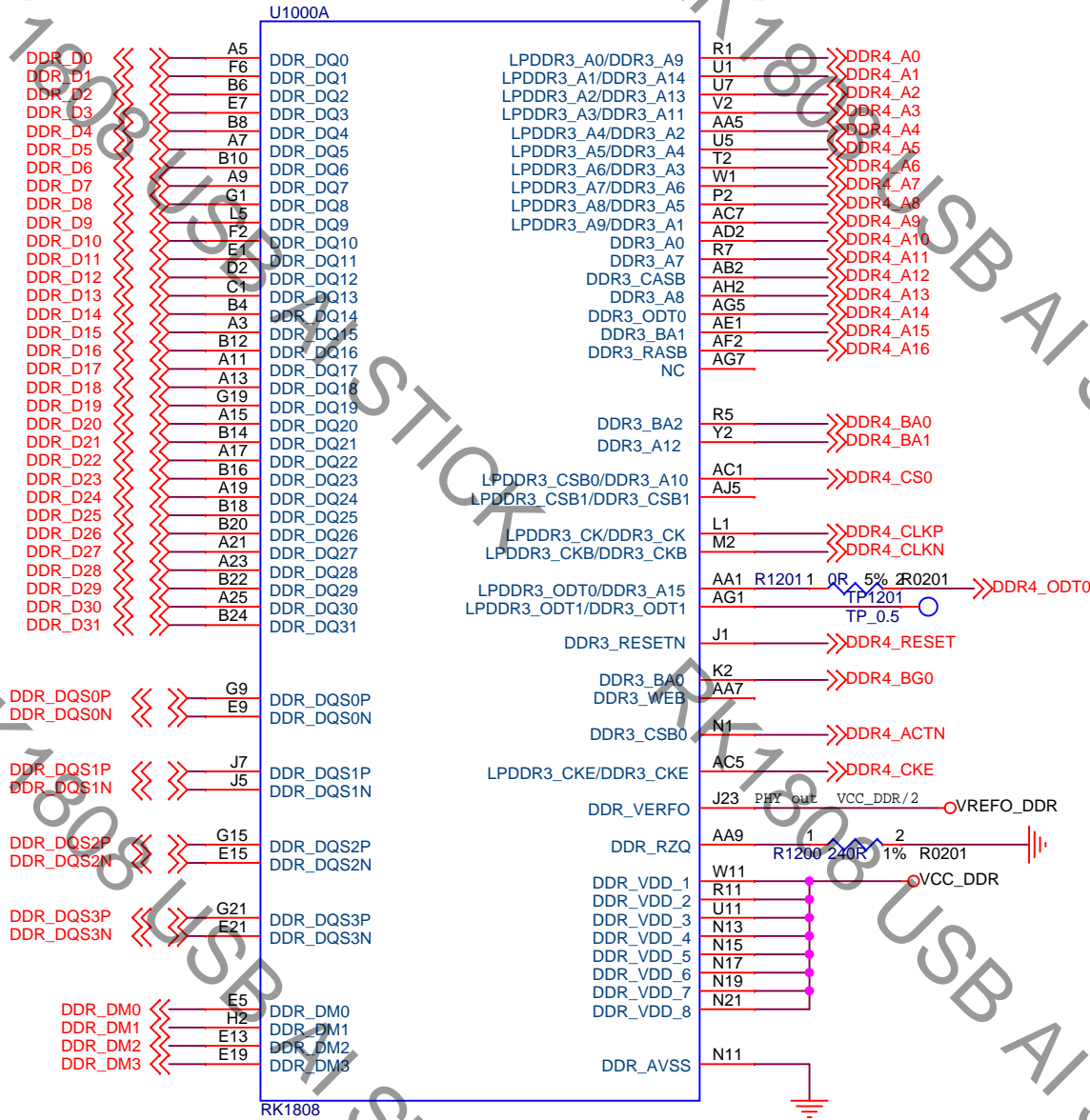


## PMUIO2

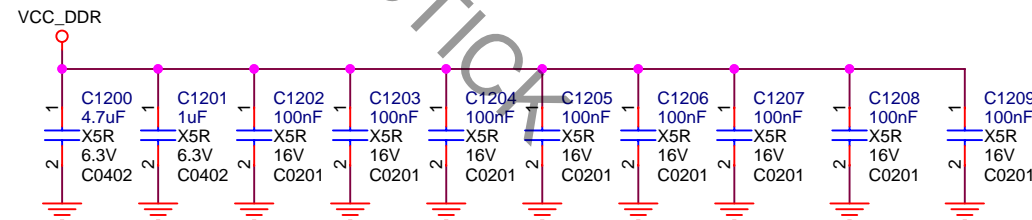


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<b>File:</b>	11.RK1808 OSC/PMUIO1/PMUIO2		
<b>Date:</b>	Thursday, September 19, 2019	<b>Rev:</b>	
<b>Designed by:</b>	Rzf	<b>Sheet:</b>	11 of 99

# DDR Controller

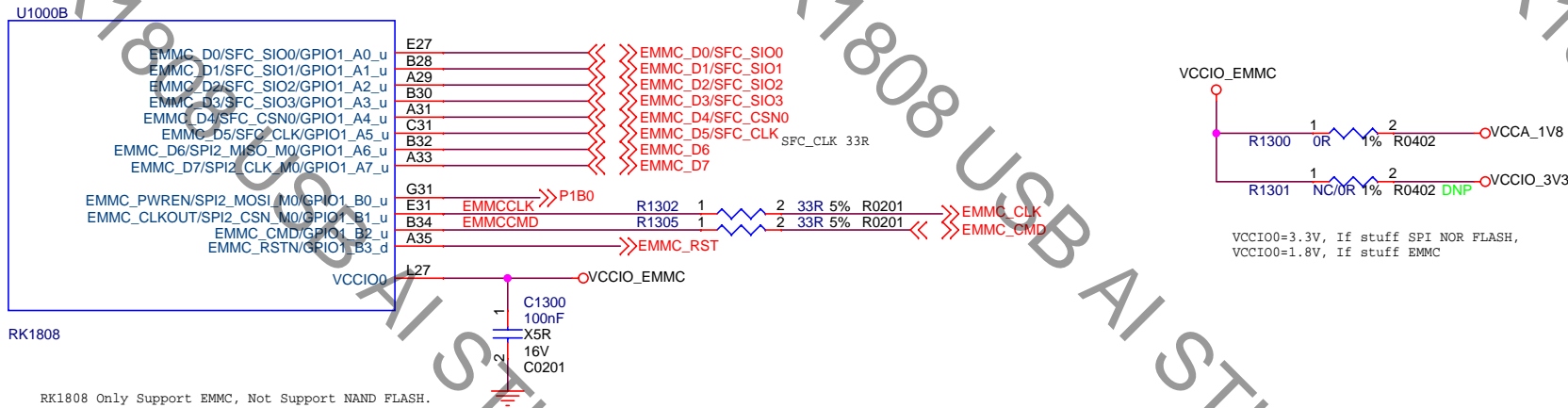


LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CBS0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN

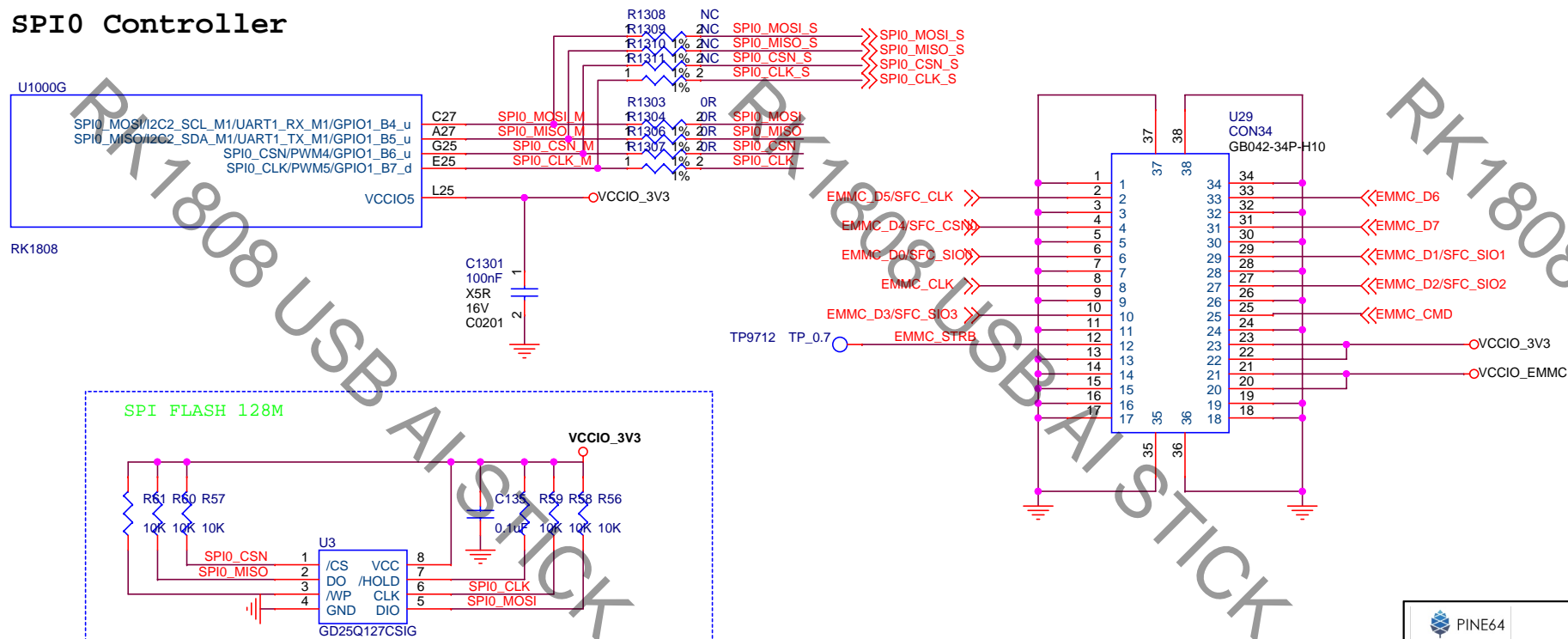





## EMMC/SFC Controller



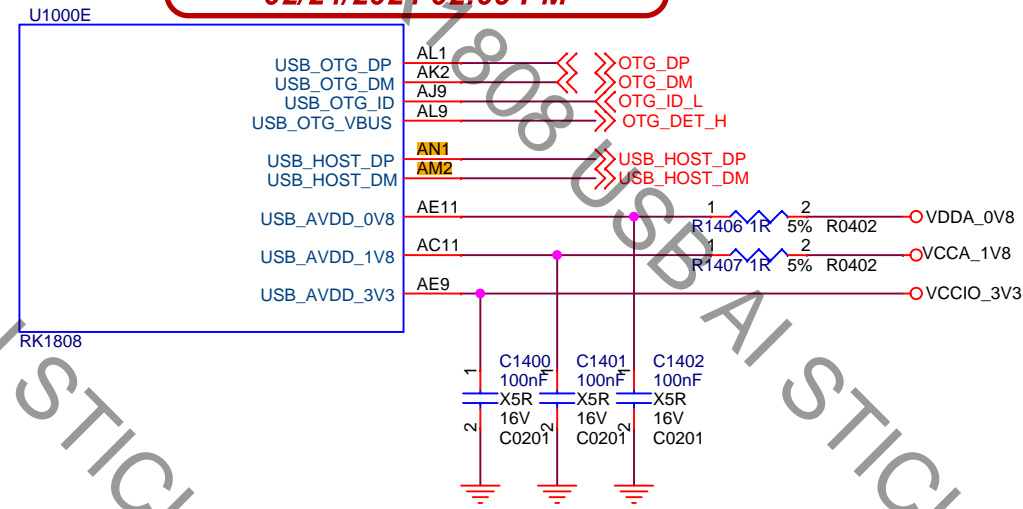
## SPI0 Controller



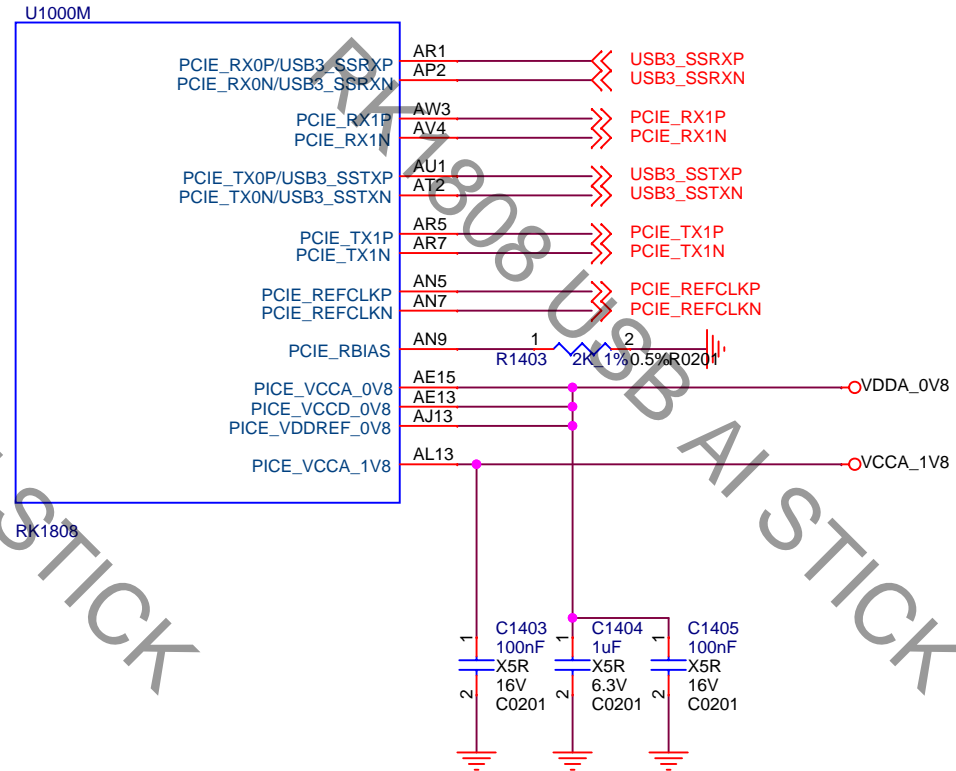
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Project:	SOEdge Schematic 20190919 ver 2.0		
File:	13.RK1808 EMMC /SPI Controller		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	Rzf	Sheet:	13 of 99



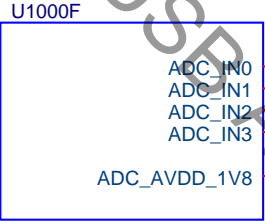
## USB Controller



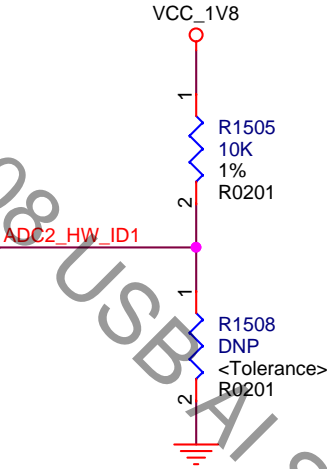
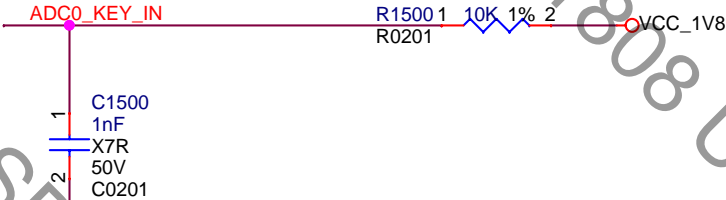
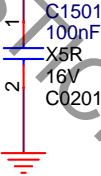
## PCIE Controller



SARADC/KEY



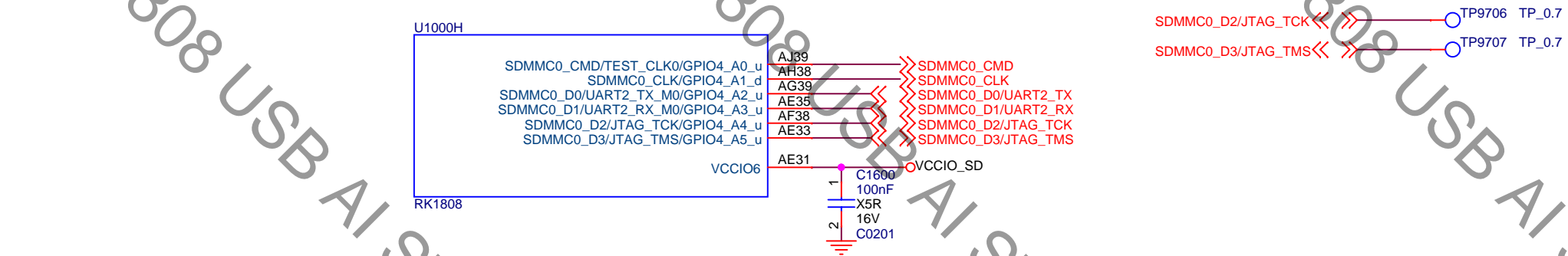
RK1808



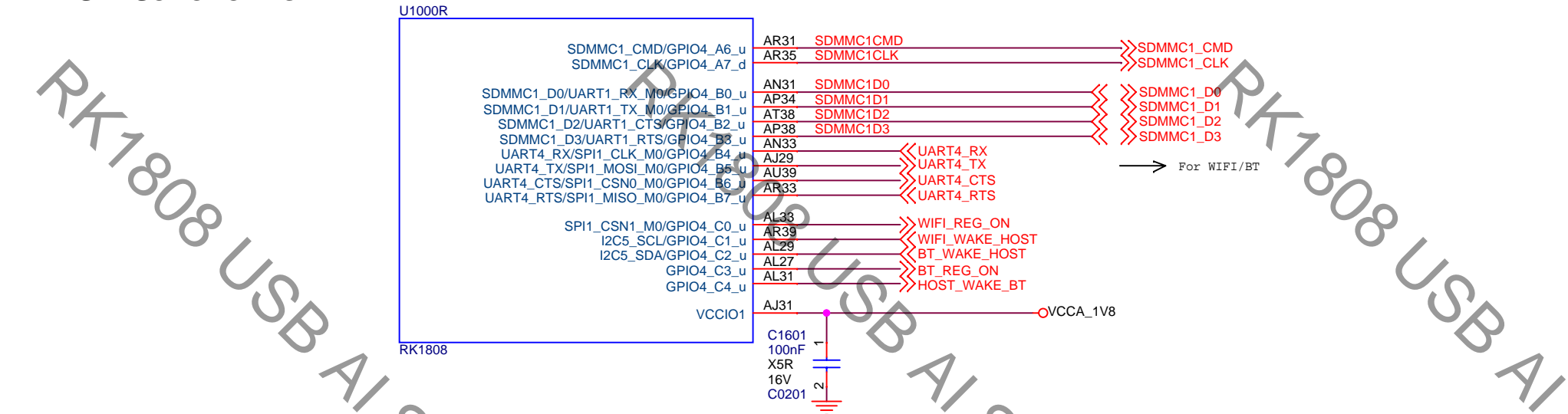
Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170

PINE64			
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	15.RK1808 SARADC/KEY		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	Rzf	Sheet:	15 of 99

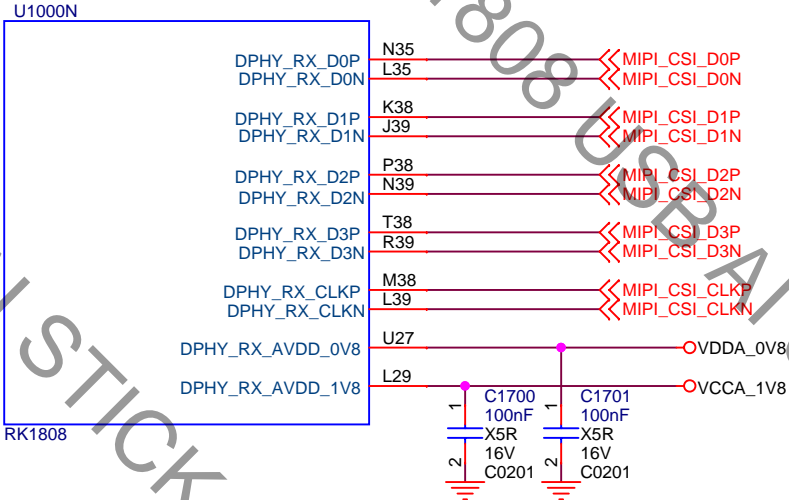
SDMMC0 Controller



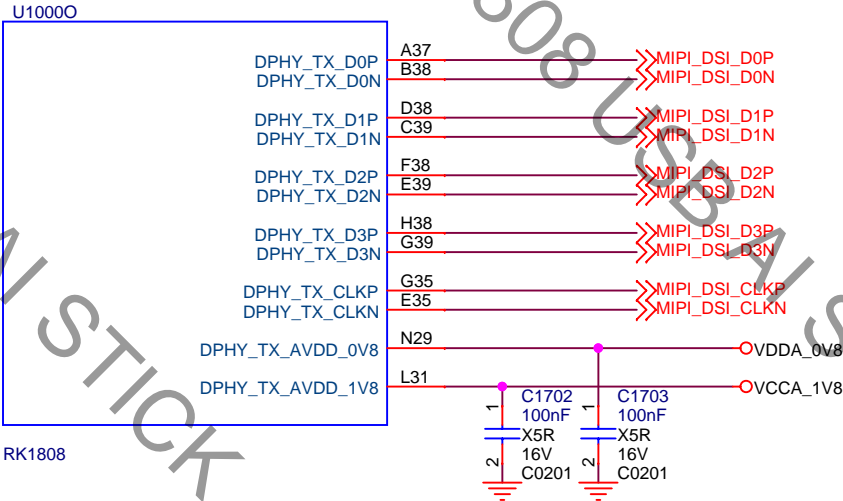
SDMMC1 Controller




MIPI CSI Controller

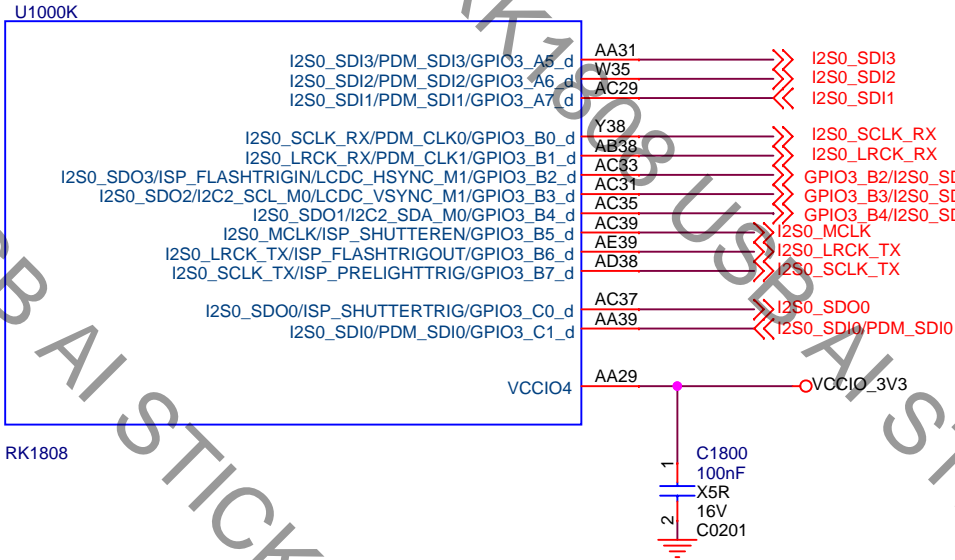


MIPI DSI Controller

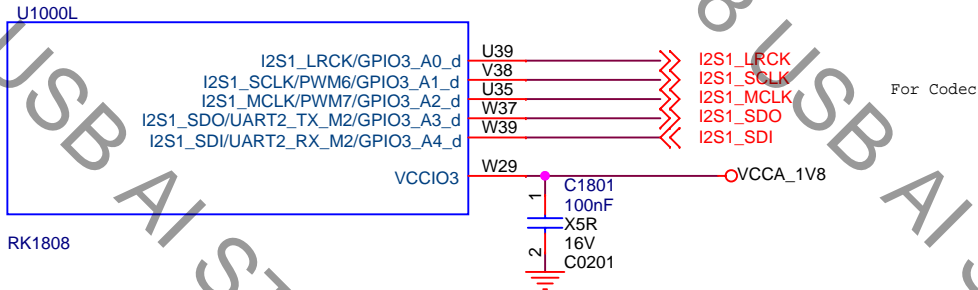



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File:	17.RK1808 MIPI DSI/CSI			
Date:	Thursday, September 19, 2019	Rev:		
Designed by:	Rzf	Sheet:	17 of 99	

I2S0 Controller



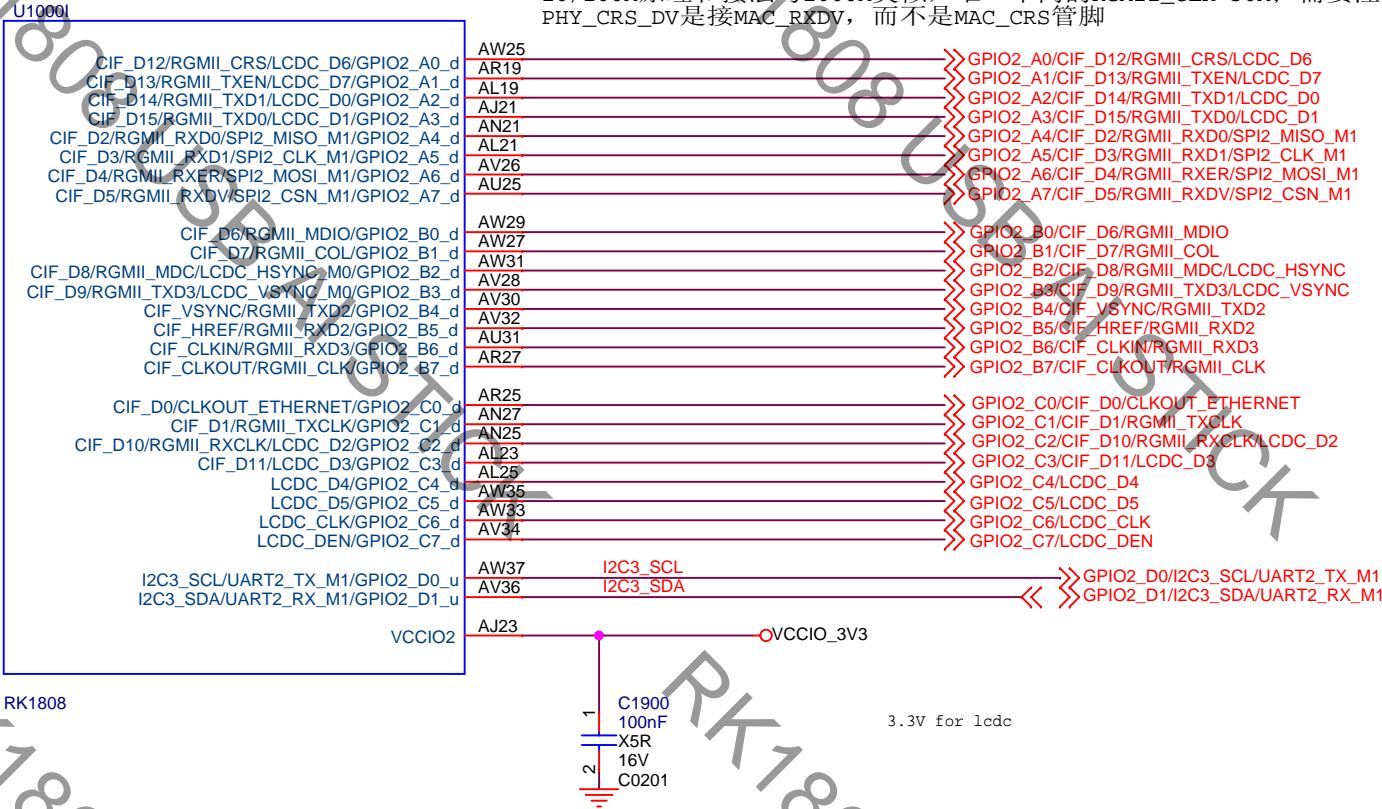
I2S1 Controller



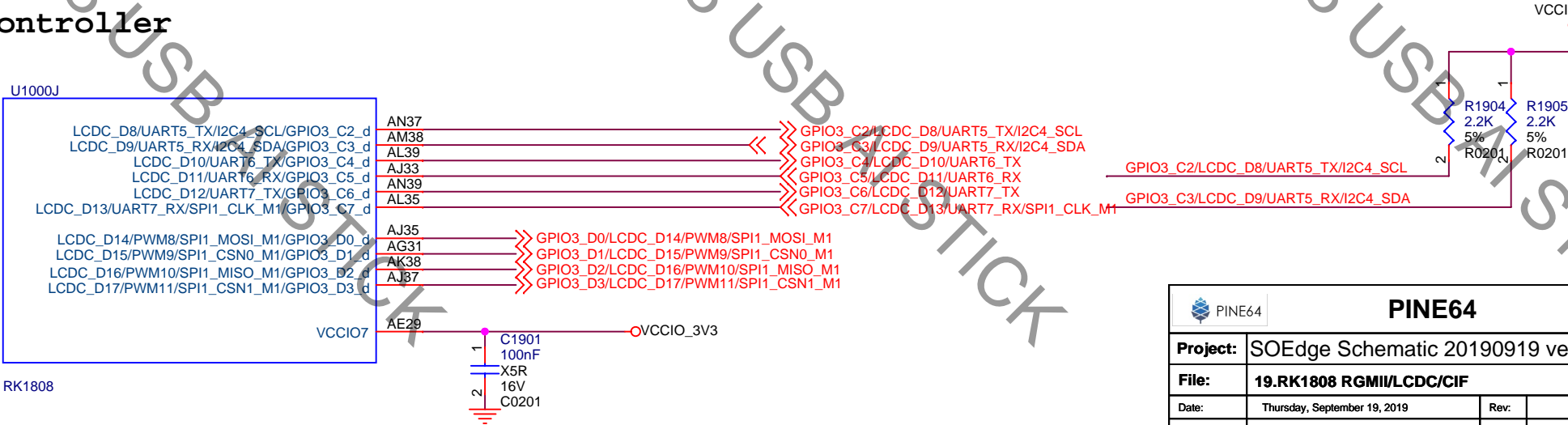
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<b>Project:</b> SOEdge Schematic 20190919 ver 2.0			
<b>File:</b> 18.RK1808 I2S0/I2S1			
<b>Date:</b>	Thursday, September 19, 2019	<b>Rev:</b>	
<b>Designed by:</b>	Rzf	<b>Sheet:</b>	18 of 99


CIF/RGMII/LCDC Controller

10/100M原理和接法与1000M类似，唯一不同的RGMII\_CLK=50M；需要注意的是10/100M的PHY\_CRS\_DV是接MAC\_RXDV，而不是MAC\_CRS管脚

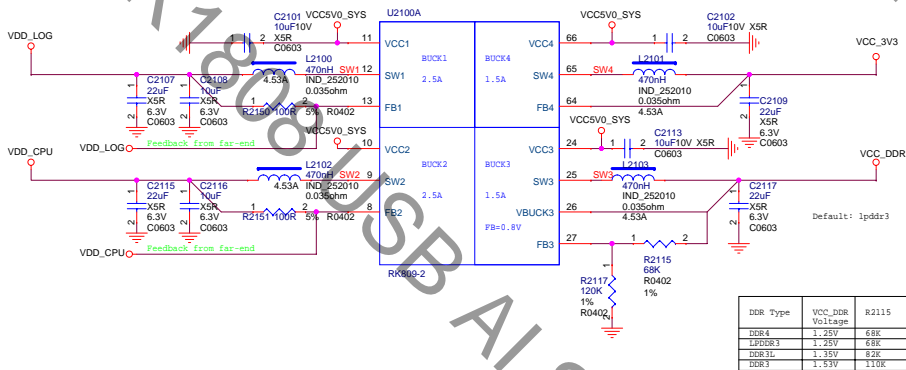


LCDC Controller

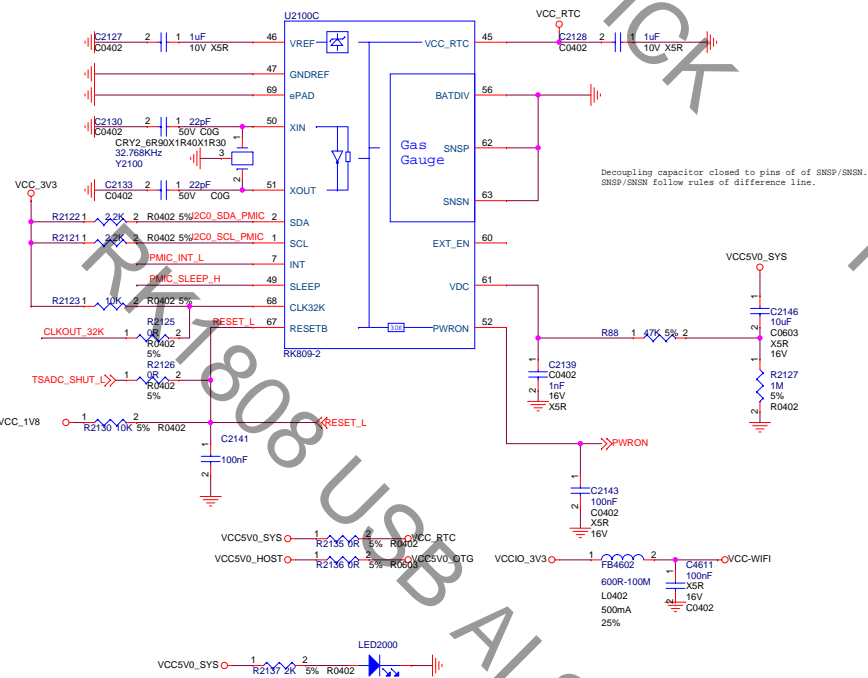


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<b>Project:</b>	SOEdge Schematic 20190919 ver 2.0		
<b>File:</b>	19.RK1808 RGMII/LCDC/CIF		
<b>Date:</b>	Thursday, September 19, 2019	<b>Rev:</b>	
<b>Designed by:</b>	Rzf	<b>Sheet:</b>	19 of 99

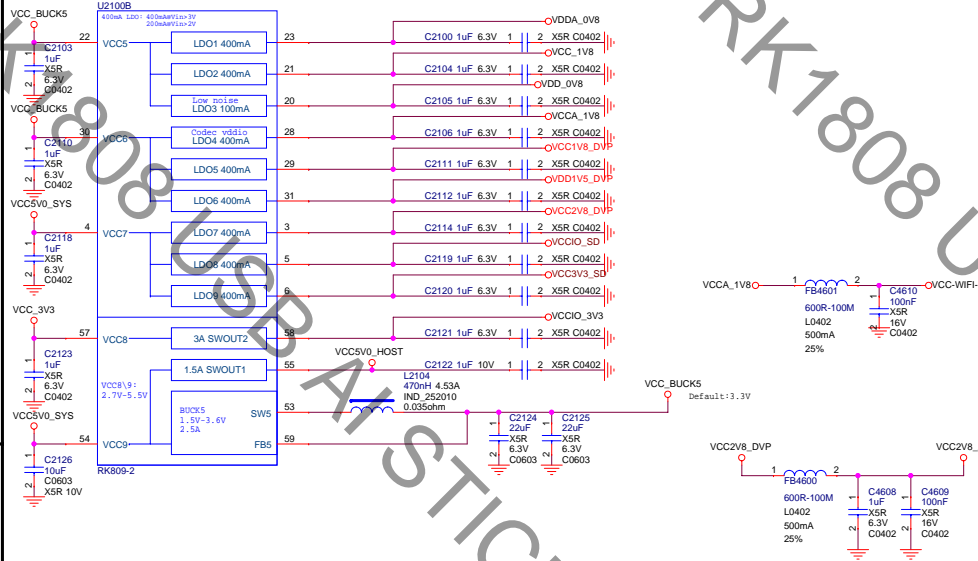
## PMIC RK809-1 DCDC



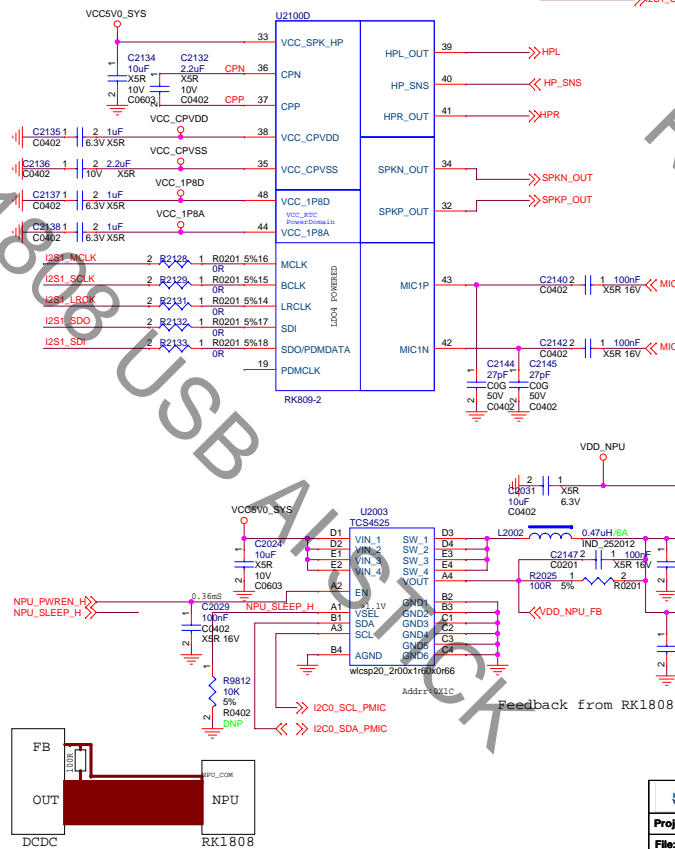
## PMIC RK809-1 Managerment



## PMIC RK809-1 LDO



## PMIC RK809-1 CODEC





DDR4-A2R98132 56R 1 DDR4 A2  
DDR4-A8R98142 56R 1 DDR4 A6  
DDR4-A1R98152 56R 1 DDR4 A11  
DDR4-A5R98162 56R 1 DDR4 A8

DDR4-BGR98172 56R 1 DDR4 BG0  
DDR4-A4R98182 56R 1 DDR4 A4  
DDR4-A5R98192 56R 1 DDR4 A5  
DDR4-BAR98202 56R 1 DDR4 BA0

DDR4-A1R98212 56R 1 DDR4 A19  
DDR4-A7R98222 56R 1 DDR4 A7  
DDR4-A0R98232 56R 1 DDR4 A0  
DDR4-ASR98242 56R 1 DDR4 A9

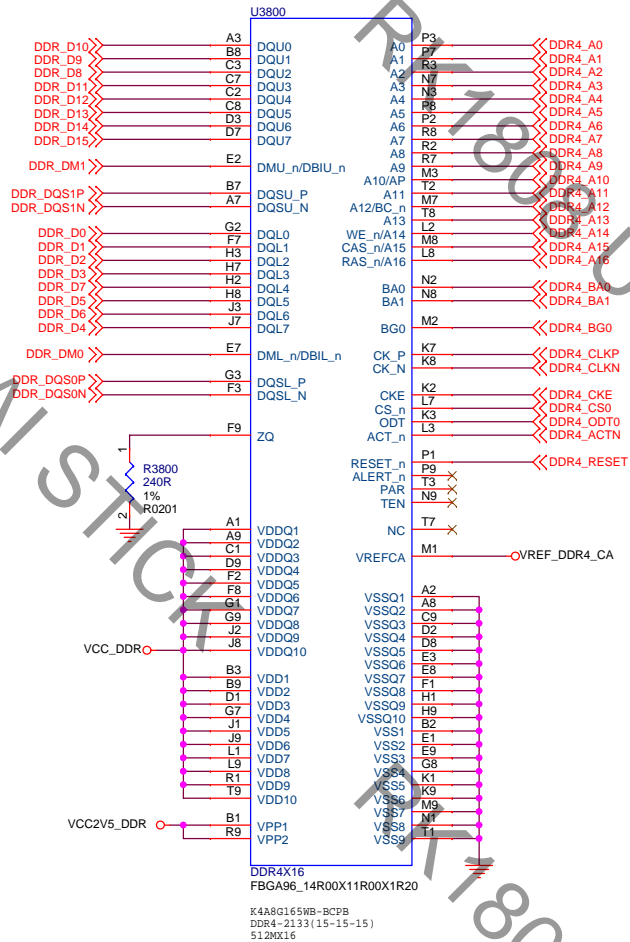
DDR4-A1R98252 56R 1 DDR4 A1  
DDR4-BAR98262 56R 1 DDR4 BA1  
DDR4-A1R98272 56R 1 DDR4 A10  
DDR4-A1R98282 56R 1 DDR4 A14

DDR4-CKE R98292 56R 1 DDR4 CKE  
DDR4-A12 R98302 56R 1 DDR4 A12  
DDR4-ACTN R98312 56R 1 DDR4 ACTN  
DDR4-A3 R98322 56R 1 DDR4 A3

DDR4-A15 R98332 56R 1 DDR4 A15  
DDR4-A16 R98342 56R 1 DDR4 A16  
DDR4-ODT R98352 56R 1 DDR4 ODT0  
DDR4-CS0 R98362 56R 1 DDR4 CS0

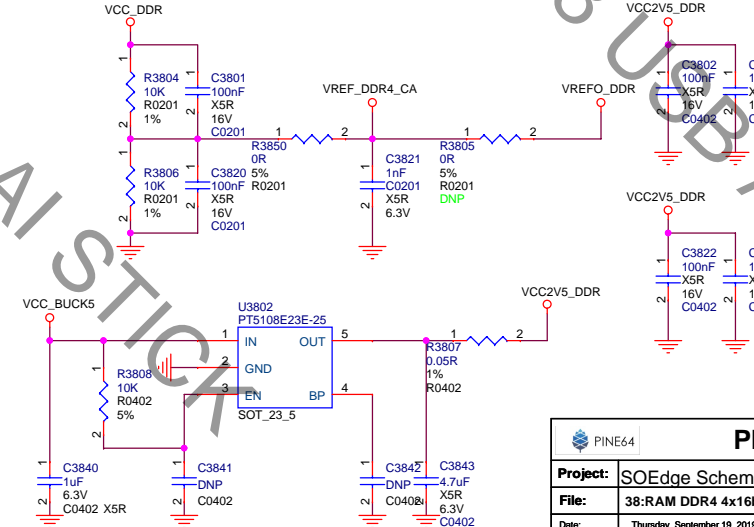
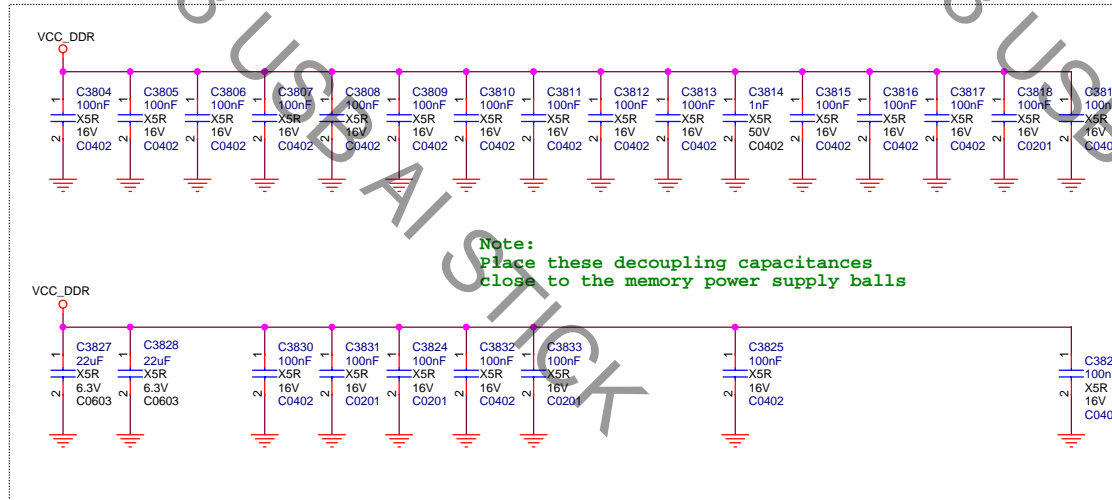
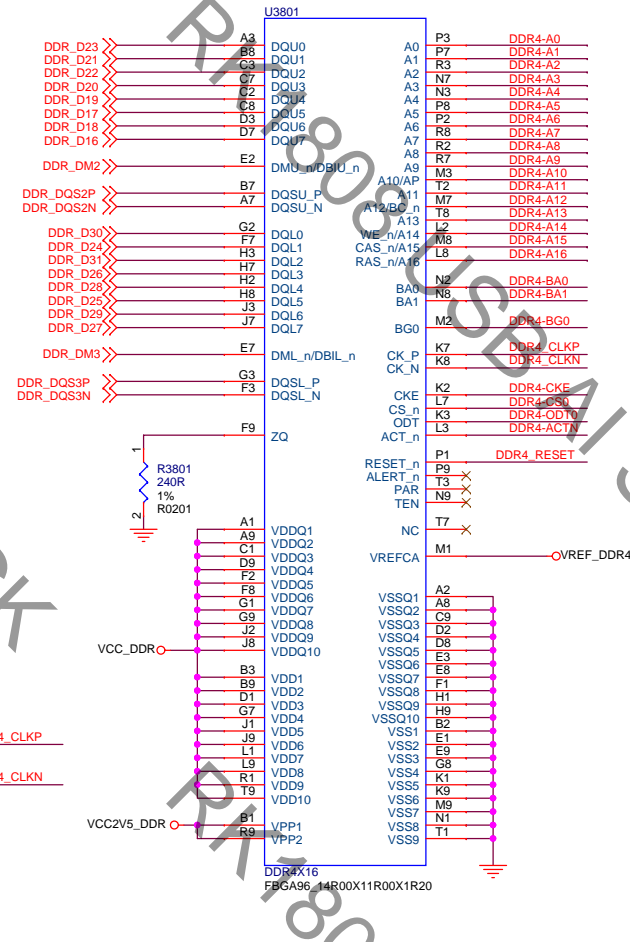
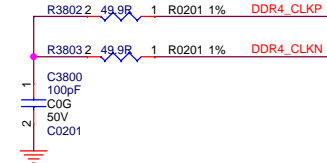
For Daisy Chain Scheduling

2X16bit DDR4



Date can be switched in group.

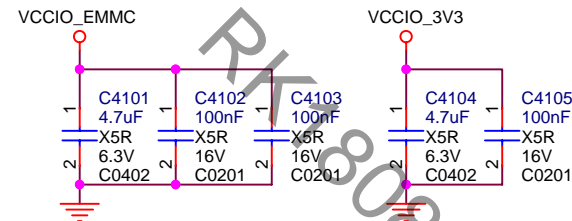
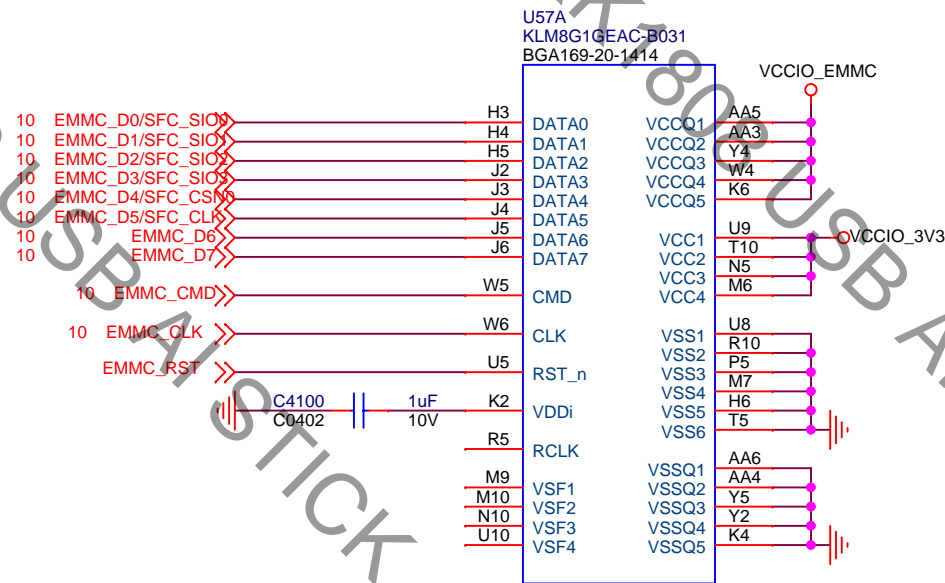
VDD(1.25V): Supply Voltage  
VDDQ(1.25V): Supply Voltage for output  
VPP(2.5V): Peak to Peak Voltage  
VPP must be equal or greater than VDD/VDDQ at all times.




PINE64			
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	38-RAM DDR4 4x16bit		
Date:	Thursday, September 19, 2019	Rev:	
Designed by:	XIAOHF	Sheet:	22 of 40

Remind: Refer to the latest AVL for parts selection.

eMMC



Remind: Refer to the latest AVL for parts selection.

 PINE64		<b>PINE64</b>	
<b>Project:</b>	SOEdge Schematic 20190919 ver 2.0		
<b>File:</b>	<b>41.EMMC</b>		
<b>Date:</b>	Thursday, September 19, 2019	<b>Rev:</b>	
<b>Designed by:</b>	Rzf	<b>Sheet:</b>	41 of 99

