Index

Note

NOTE 1:
Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:
Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

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Project:	SOEdge Schematic 20190919 ver 2.0		
File:	01.Index		
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Version	Date	Author	Change List	Approved
V1.0	*20181025*		*First edition for RK1808 ddr4*	*RZF*
V2.0	20190919		SOEdge Schematic Released	

PINE64	PINE64	
Project:	SOEdge Schematic 20190919 ver 2.0	
File:	**02.Revision History**	
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPIO0_B0_u I2C0_SDA/GPIO0_B1_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz,400kHz
					SY837		BUCK	100kHz,400kHz
I2C1	I2C1_SCL/GPIO0_C0_u I2C1_SDA/GPIO0_C1_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC_3V3	GSL1680		Touch IC	100kHz,400kHz
								100kHz,400kHz
I2C2	I2C1_SCL/GPIO1_B4_U I2C1_SDA/GPIO1_B5_U	VCCIO_3V3			NC			100kHz,400kHz
I2C3	GPIO2_D0/I2C3_SCL_U GPIO2_D1/I2C3_SDA_U	VCCA_1V8		VCCA_1V8	MIPI CAMERA			
					CIF CAMERA			
					BT1120			
I2C4	GPIO3_C2/I2C4_SCL_U GPIO3_C3/I2C4_SDA_U	VCCIO_3V3		VCCIO_3V3	DIGITAL MIC			
					RGB LCD			
					PCIEX4			
					SENSOR			

PINE64	**PINE64**
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File:	**04.I2C MAP**
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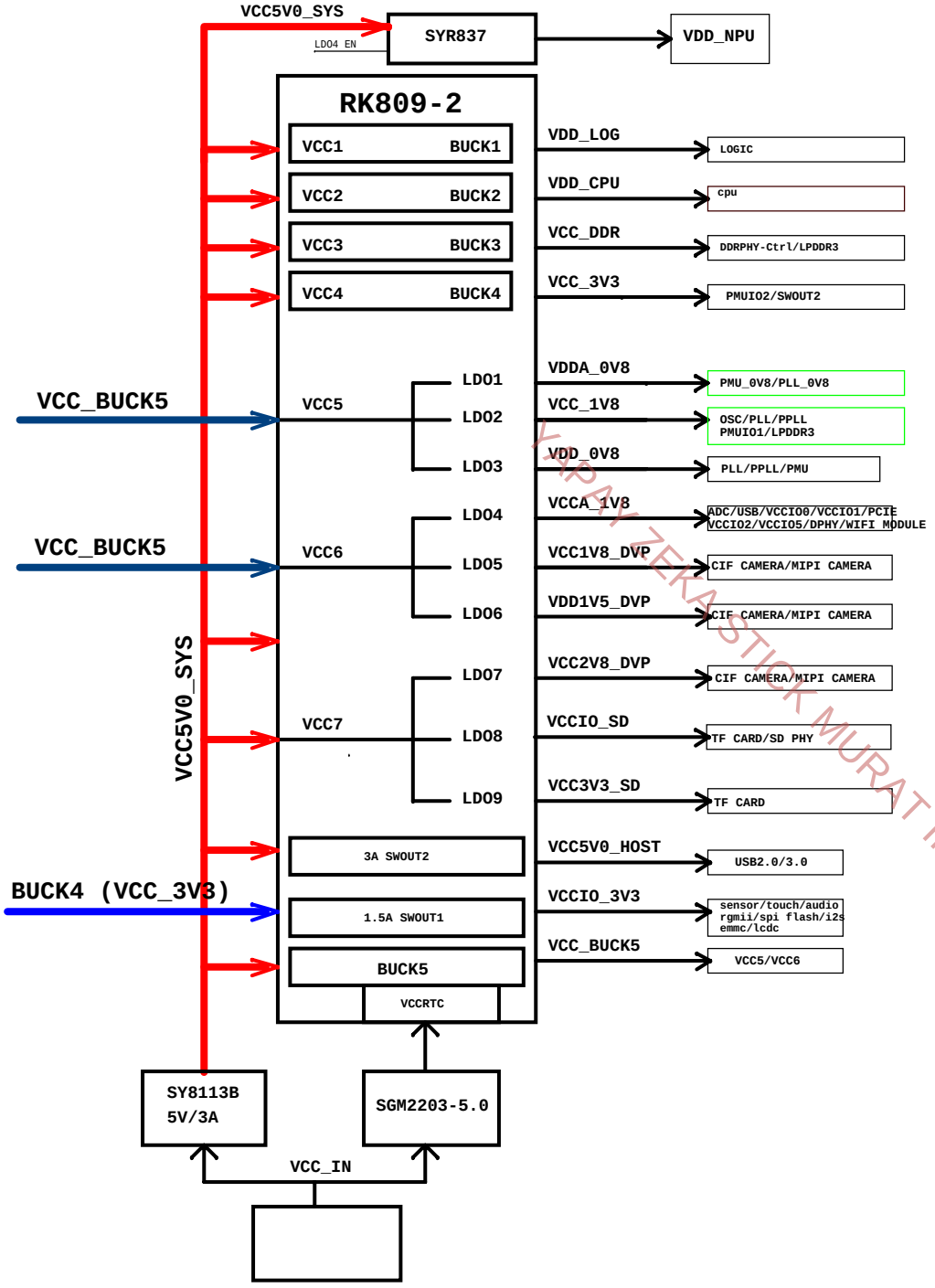
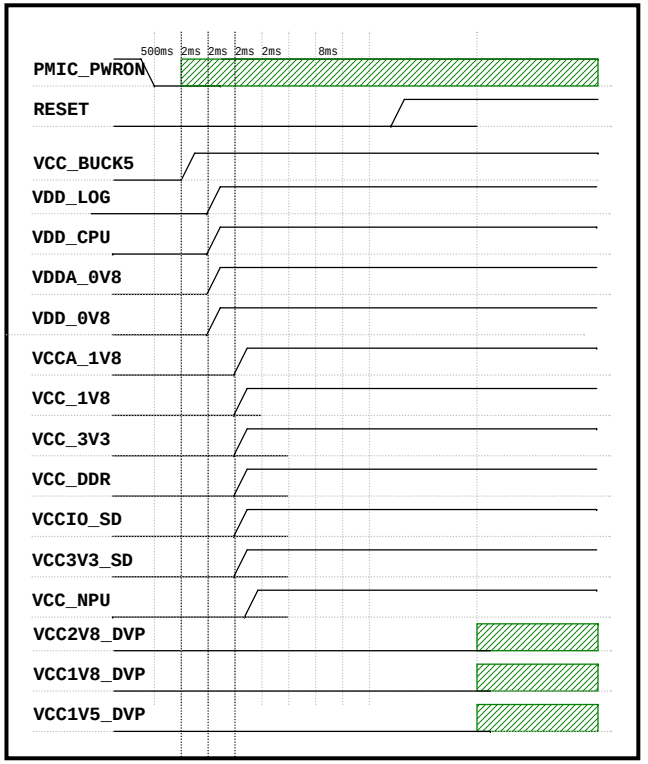
POWER DIAGRAM



RK809-2 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VDD_NPU	EXTERNAL(SY837)	Slot:3A	1V	6A	ON	OFF	4A
VDD_LOG	BUCK1	Slot:2	0.85V	2.5A	ON	OFF	1.25A
VDD_CPU	BUCK2	Slot:2	0.85V	2.5A	ON	OFF	750mA
VCC_DDR	BUCK3	Slot:3	FB=0.6V	1.5A	ON	ON	
VCC_3V3	BUCK4	Slot:4	3.3V	1.5A	ON	ON	
VCC_BUCK5	BUCK5	Slot:1	2.5V	2.5A	ON	ON	
VDDA_0V8	LDO1	Slot:2	0.8V	400mA	ON	OFF	
VCC_1V8	LDO2	Slot:3	1.8V	400mA	ON	ON	
VDD_0V8	LDO3	Slot:2	0.8V	100mA	ON	ON	
VCCA_1V8	LDO4	Slot:3	1.8V	400mA	ON	OFF	
VCC1V8_DVP	LDO5		1.8V	400mA	OFF	OFF	
VDD1V5_DVP	LDO6		1.5V	400mA	OFF	OFF	
VCC2V8_DVP	LDO7		2.8V	400mA	OFF	OFF	
VCCIO_SD	LDO8	Slot:4	3.3V	400mA	ON	OFF	
VCC3V3_SD	LDO9	Slot:4	3.3V	400mA	ON	OFF	
VCCIO_3V3	SWOUT2	Slot:4	3.3V	3A	ON	OFF	
VCC5V0_HOST	SWOUT1		5V	1.5A	OFF	OFF	
RESET	RESETB	Slot:10	OD				



PINE64	**PINE64**
Project:	SOEdge Schematic 20190919 ver 2.0
File:	**05.Power diagram and Sequence**
Date:	Thursday, September 19, 2019
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RK1808 Power

ROCKCHIP RK1808 ARM YAPAY ZEKA USB STICK

PINE64	PINE64
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File:	10.RK1808 Power
Date:	Thursday, September 19, 2019
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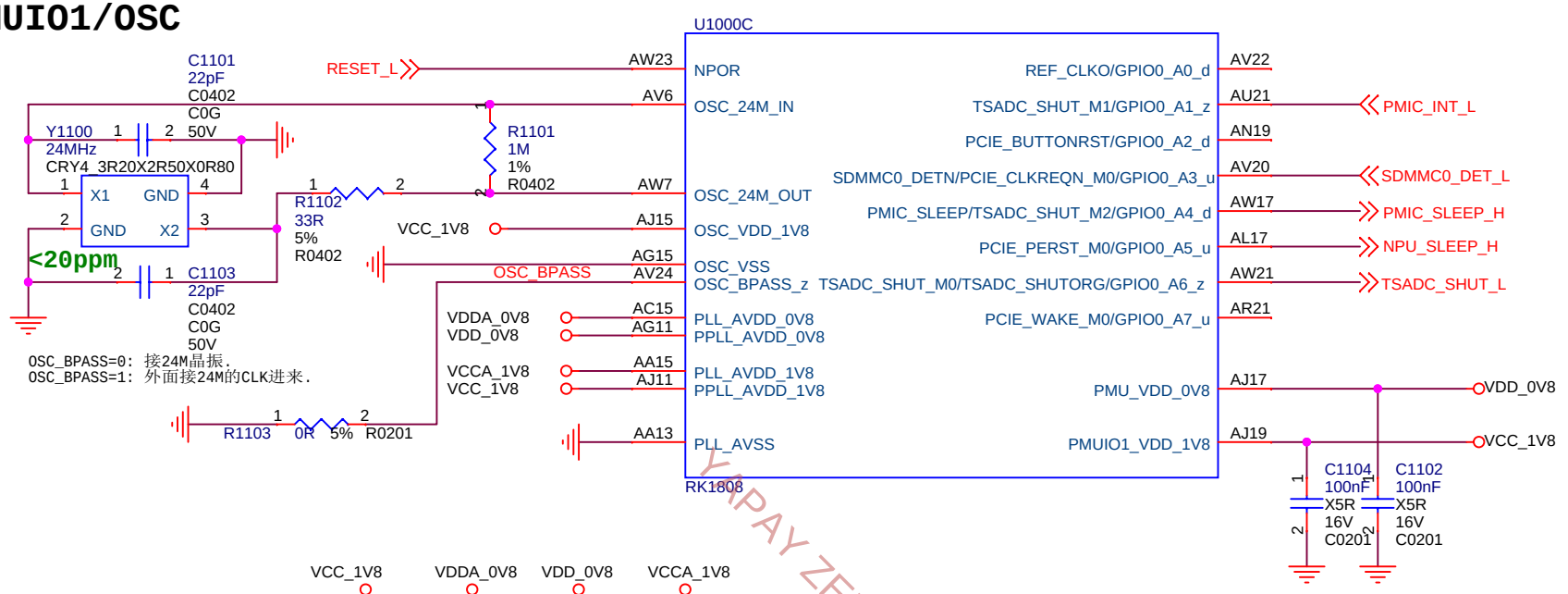
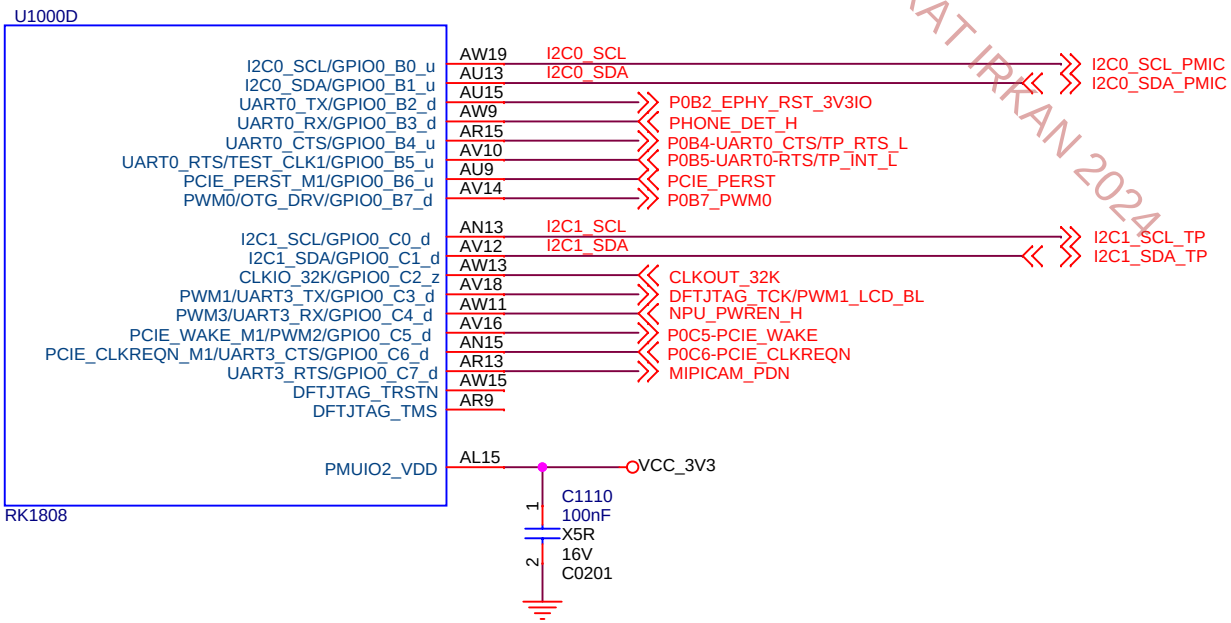
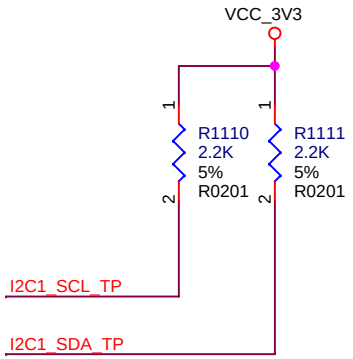
PMUIO1/OSC



PMUIO2





PINE64	**PINE64**
Project:	SOEdge Schematic 20190919 ver 2.0
File:	**11.RK1808 OSC/PMUIO1/PMUIO2**
Date:	Thursday, September 19, 2019
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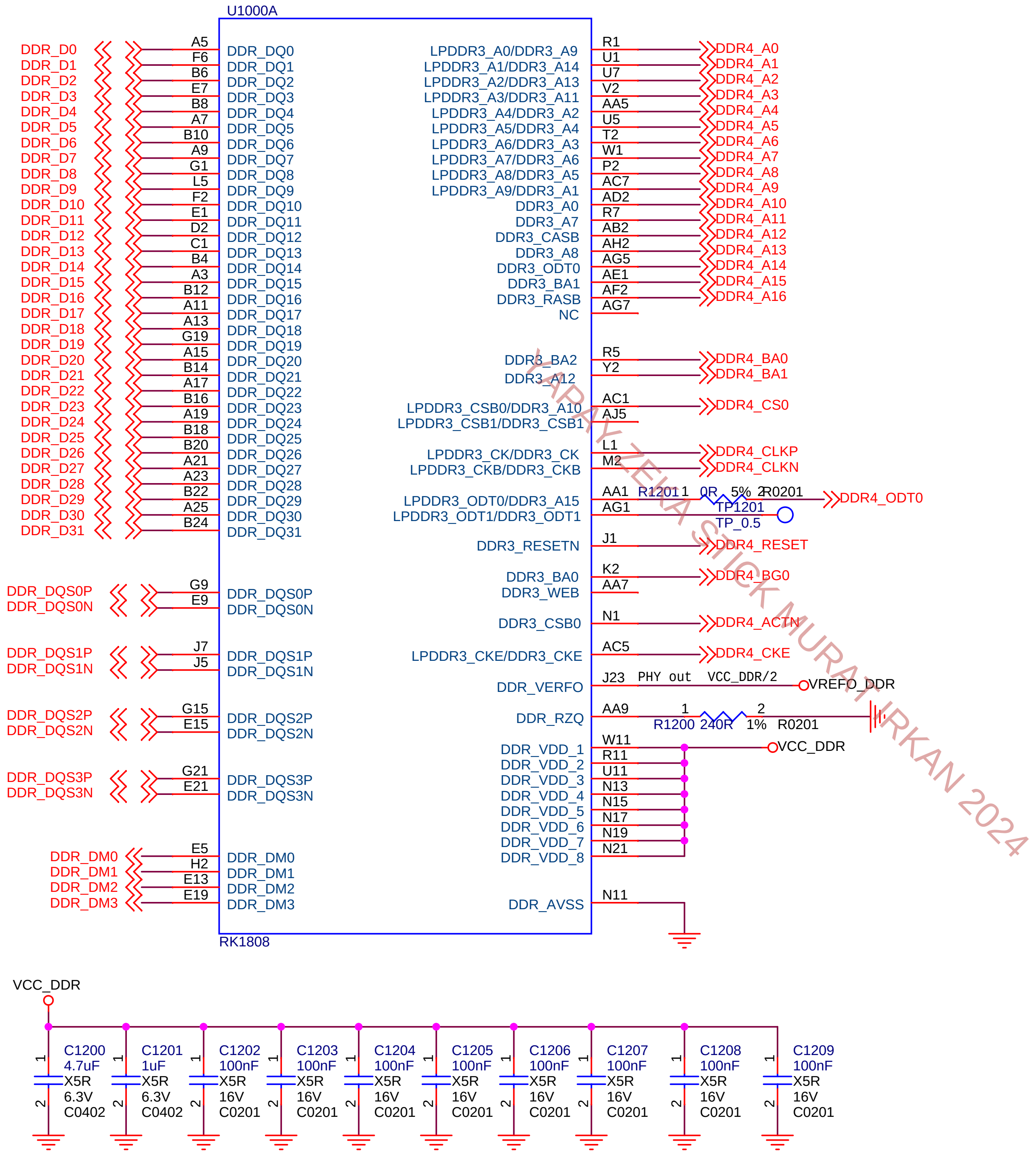
DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN

PINE64	PINE64		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	12.RK1808 DDR Controller		
Date:	Thursday, September 19, 2019	Rev:	
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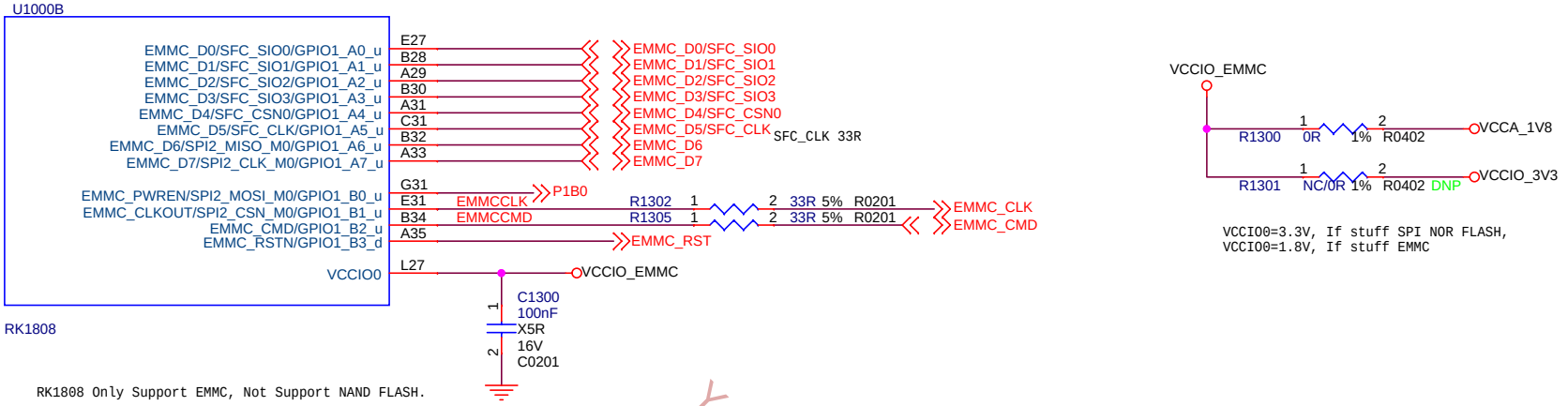
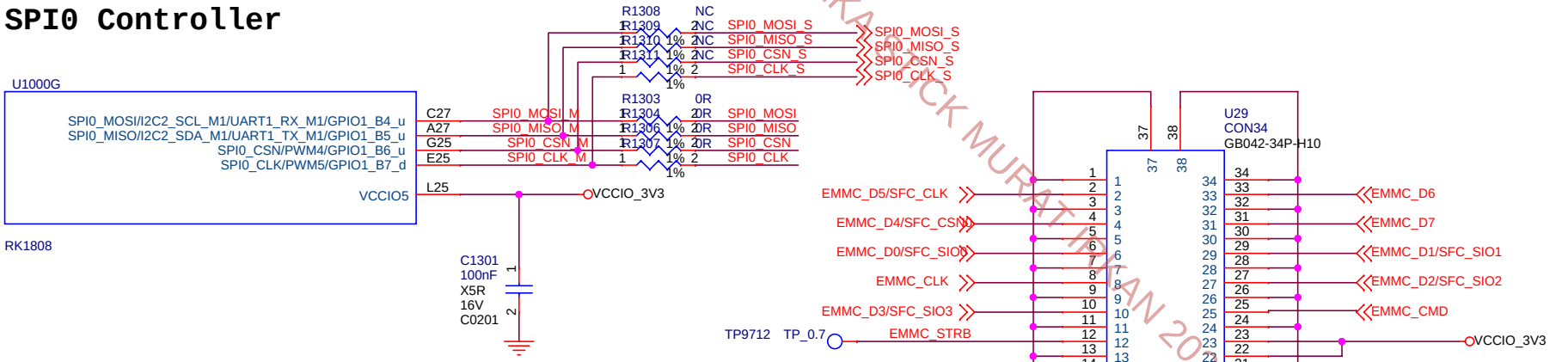
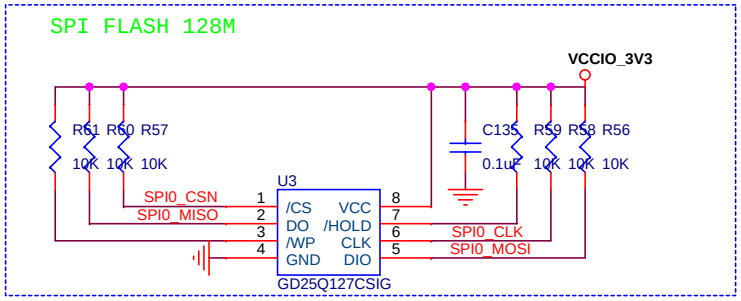
EMMC/SFC Controller



SPI0 Controller





PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**13.RK1808 EMMC /SPI Controller**		
Date:	Thursday, September 19, 2019	Rev:	
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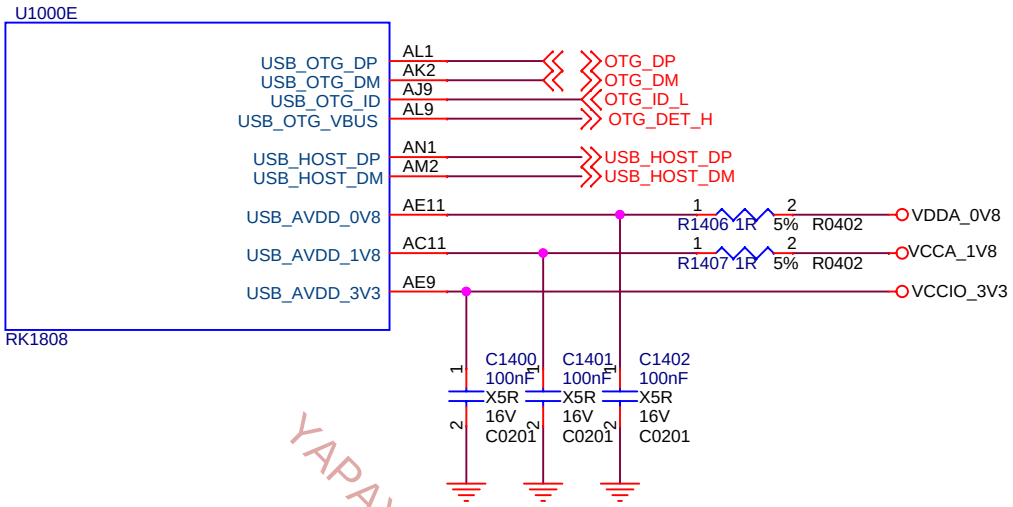
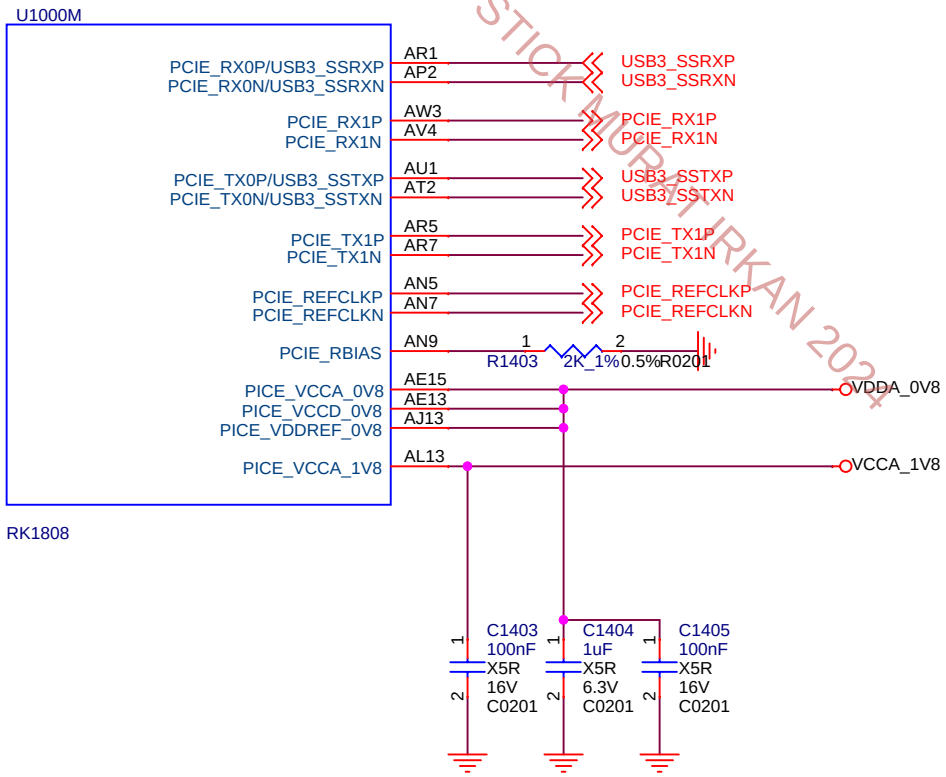
USB Controller



PCIE Controller



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**14.RK1808 USB/PCIE Controller**		
Date:	Thursday, September 19, 2019	Rev:	
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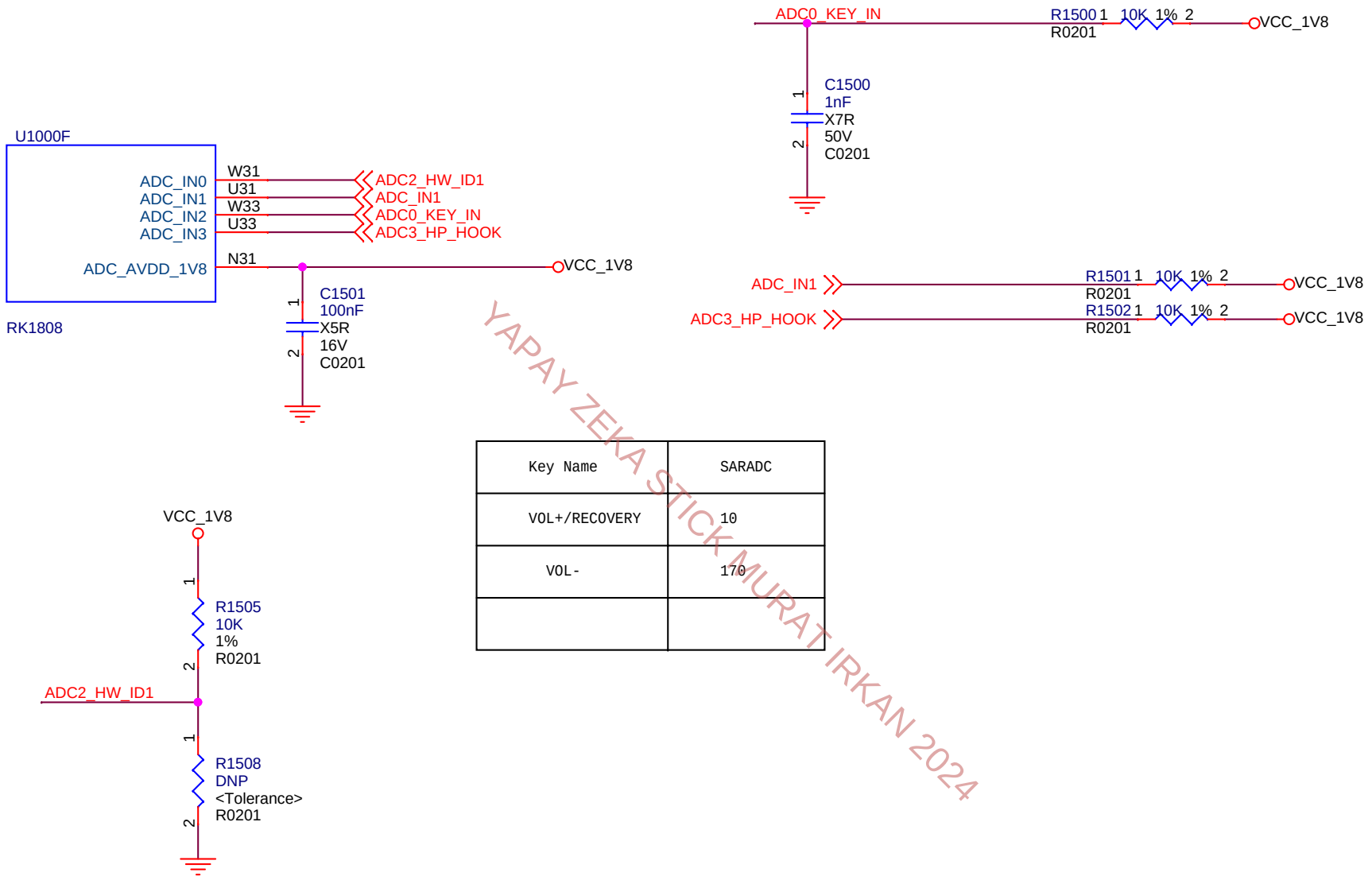
SARADC/KEY



Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170

PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**15.RK1808 SARADC/KEY**		
Date:	Thursday, September 19, 2019	Rev:	
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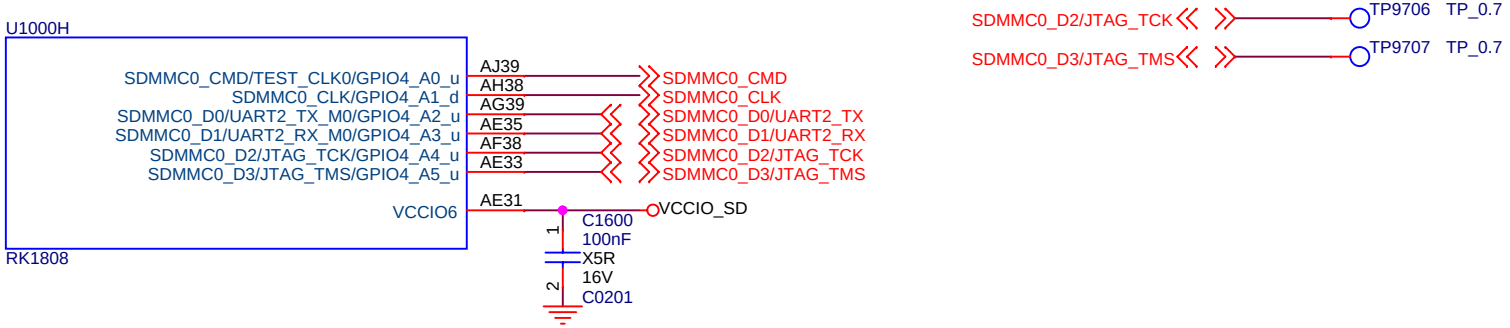
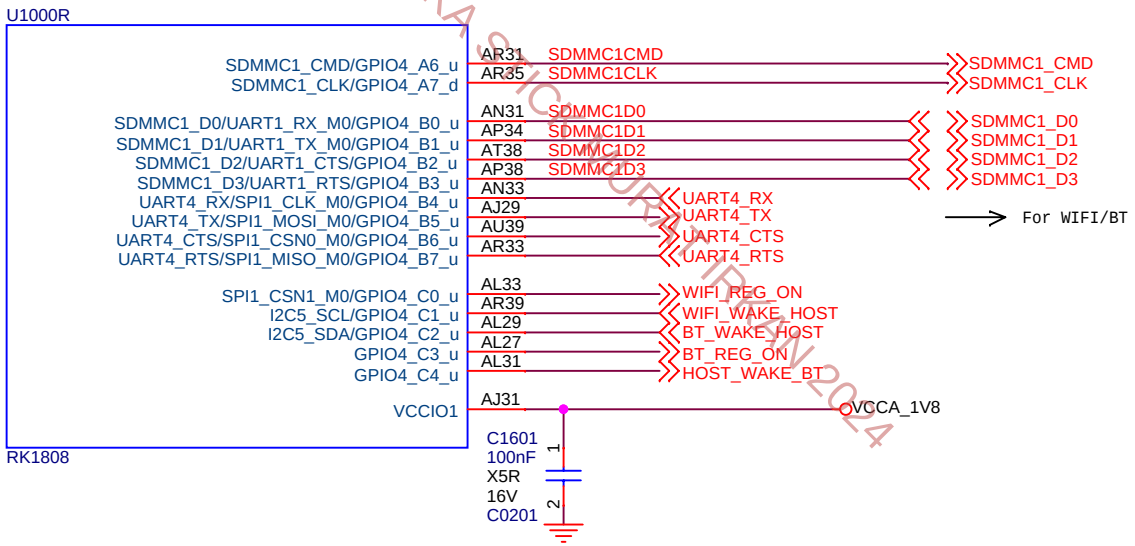
SDMMC0 Controller



SDMMC1 Controller



PINE64	PINE64
Project:	SOEdge Schematic 20190919 ver 2.0
File:	16.RK1808 SDMMC0/SDMMC1
Date:	Thursday, September 19, 2019
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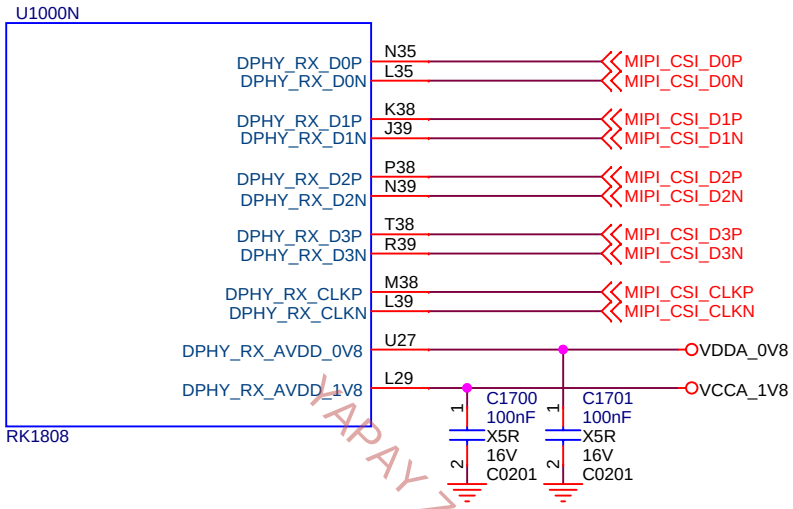
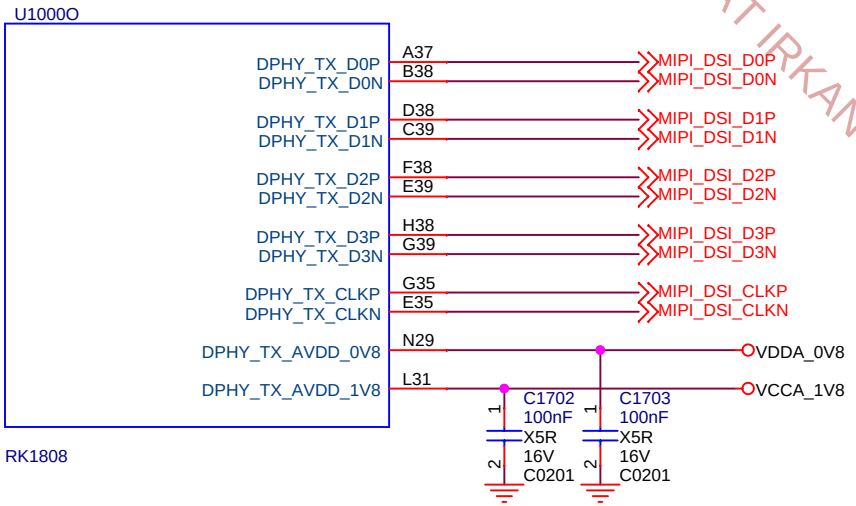
MIPI CSI Controller



MIPI DSI Controller



PINE64	PINE64		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**17.RK1808 MIPI DSI/CSI**		
Date:	Thursday, September 19, 2019	Rev:	
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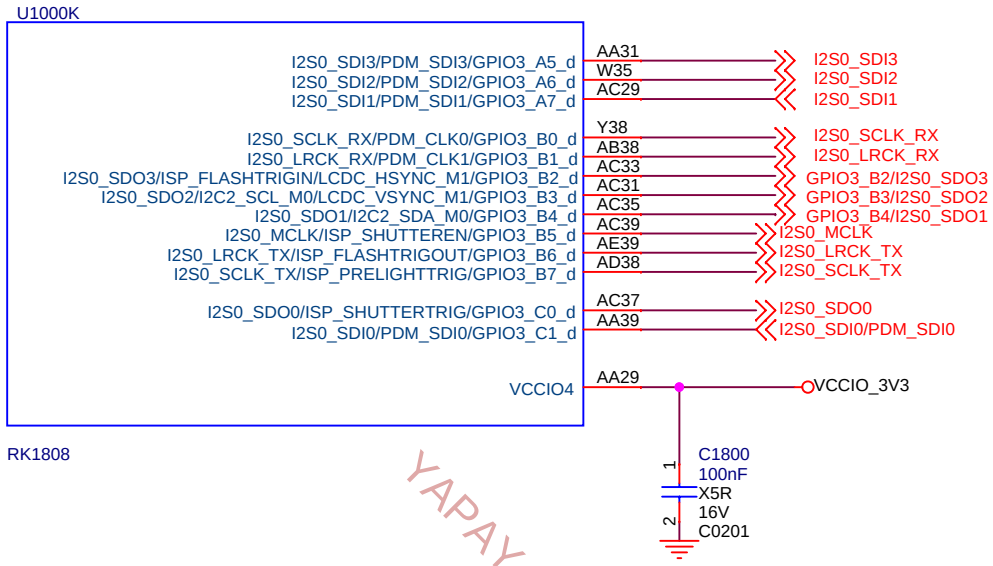
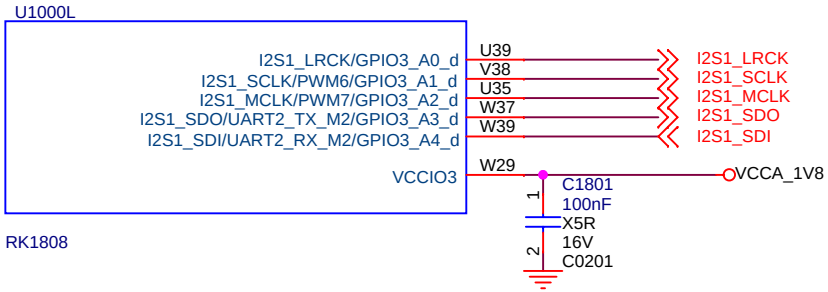
I2S0 Controller



I2S1 Controller



For Codec

PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**18.RK1808 I2S0/I2S1**		
Date:	Thursday, September 19, 2019	Rev:	
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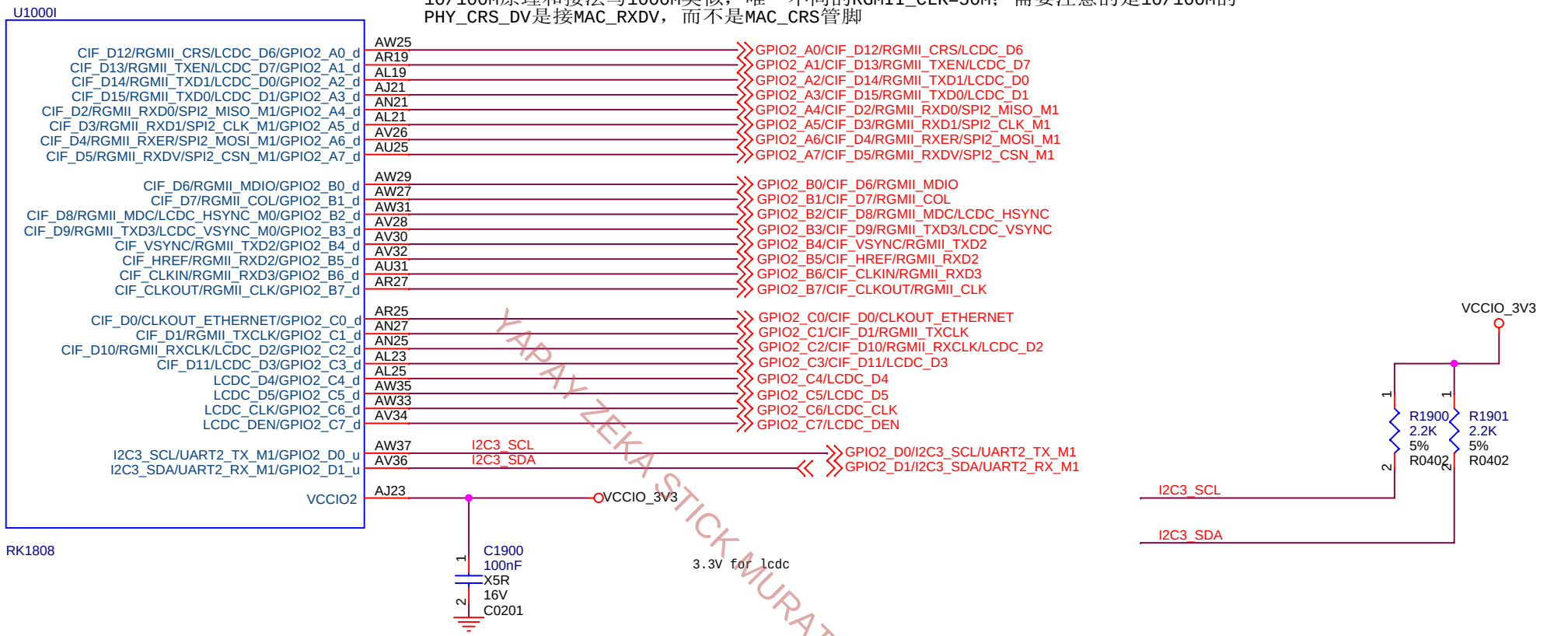
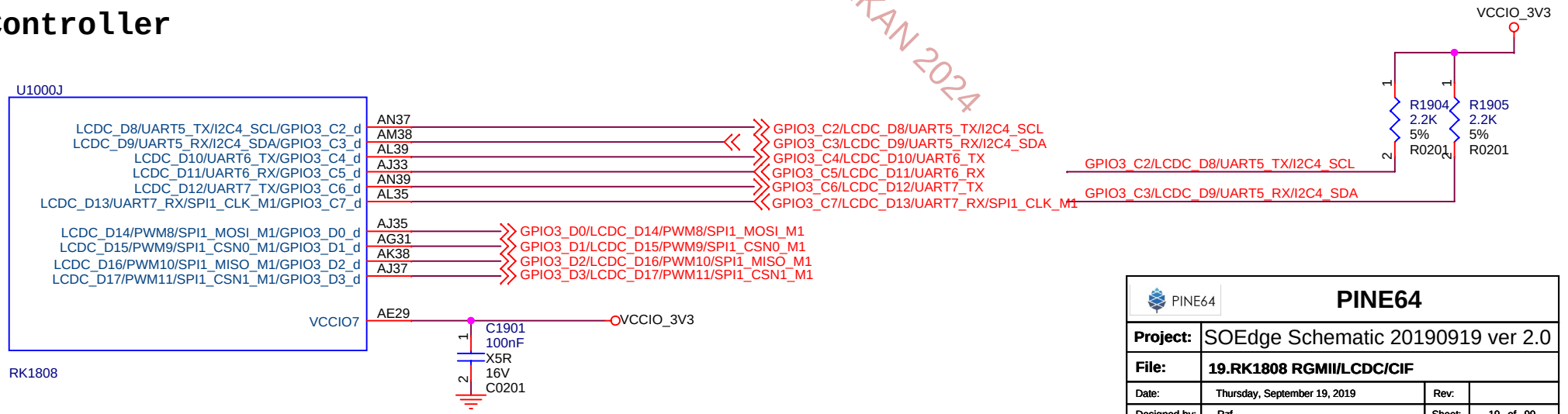
CIF/RGMII/LCDC Controller

10/100M原理和接法与1000M类似，唯一不同的RGMII_CLK=50M；需要注意的是10/100M的PHY_CRS_DV是接MAC_RXDV，而不是MAC_CRS管脚



LCDC Controller



PINE64	**PINE64**		
Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**19.RK1808 RGMII/LCDC/CIF**		
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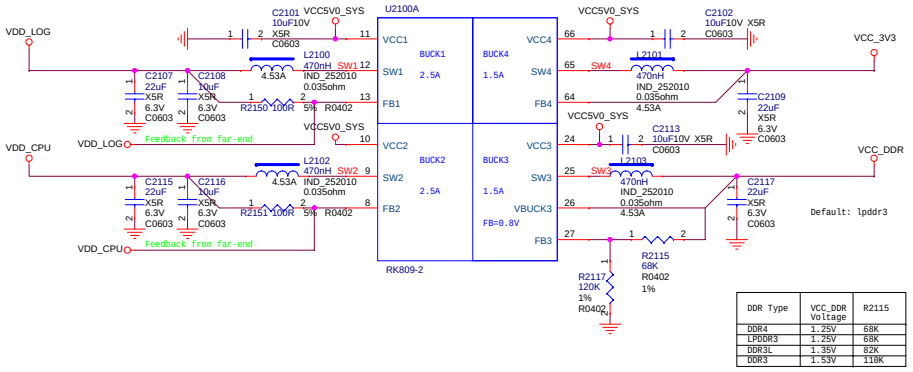
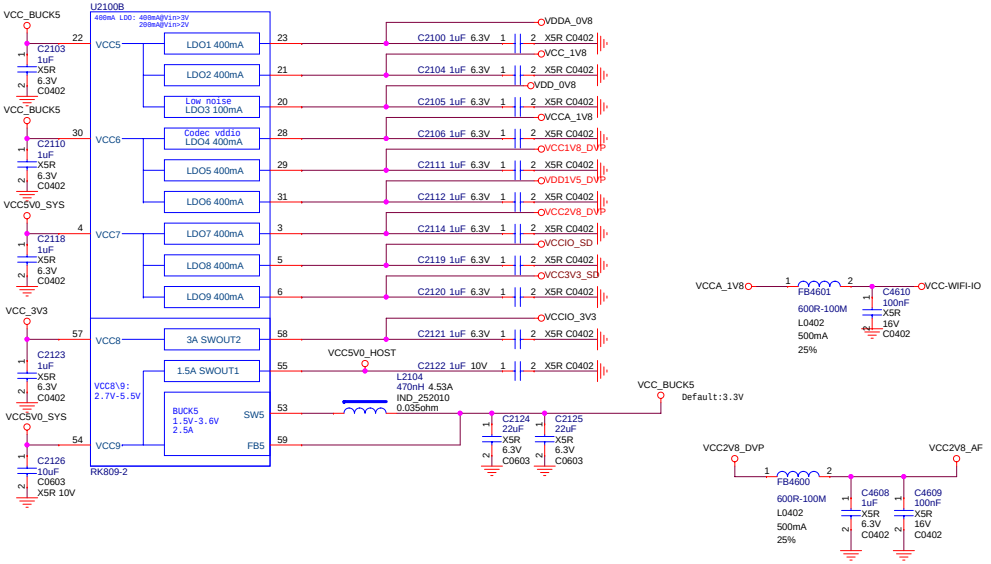
PMIC RK809-1 DCDC

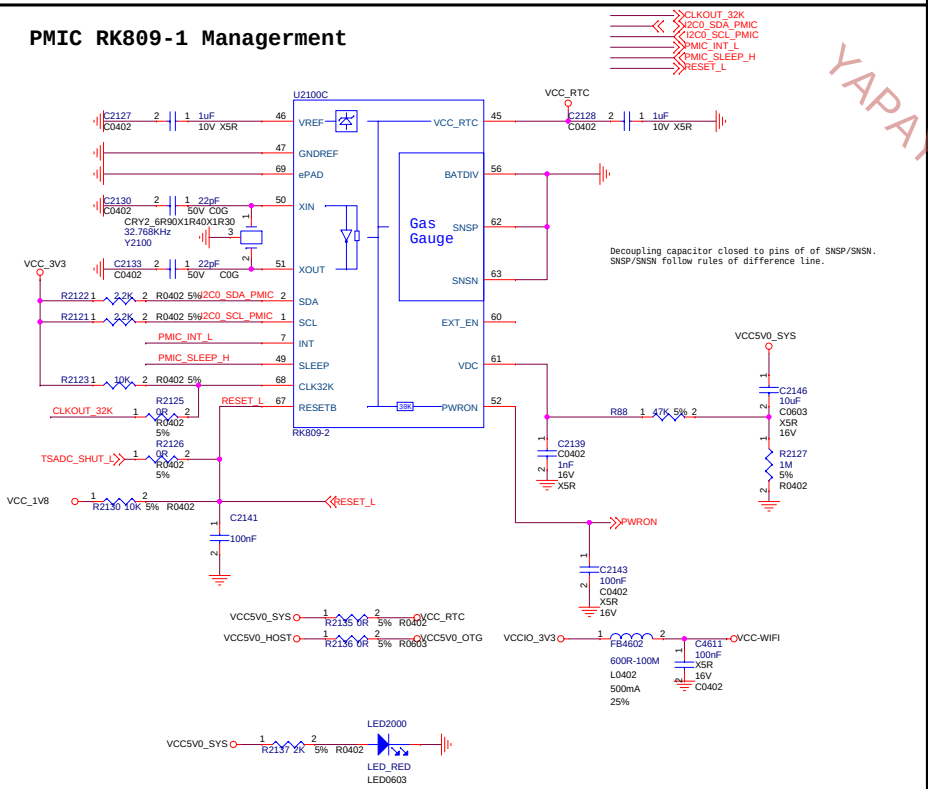


DDR Type	VCC_DDR Voltage	R2115
DDR4	1.25V	68K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	118K

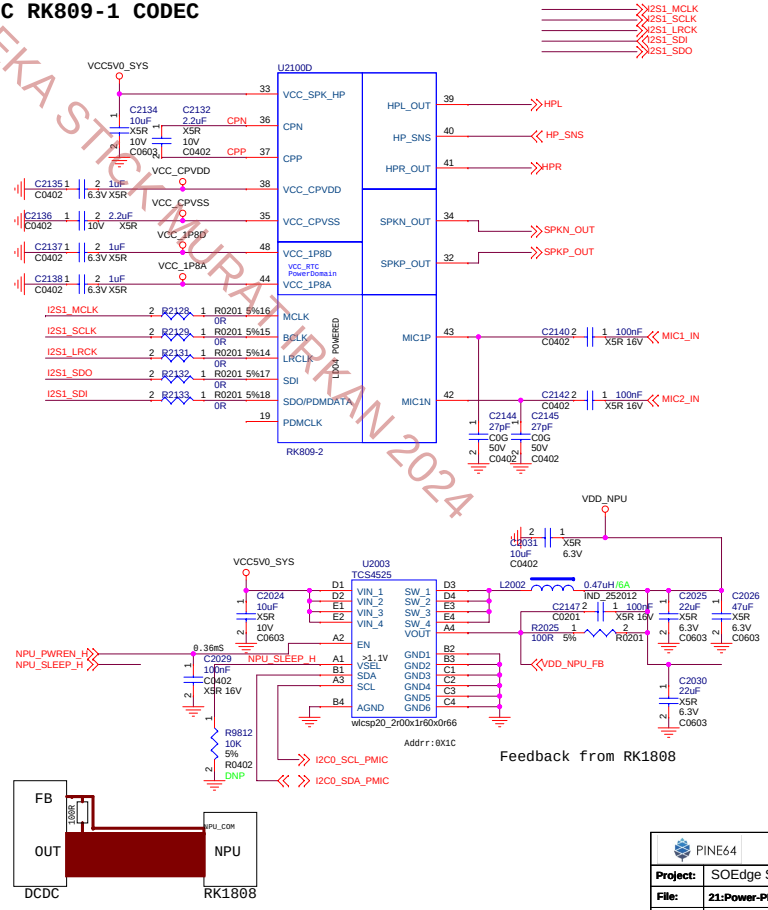
PMIC RK809-1 LDO



PMIC RK809-1 Managerment



PMIC RK809-1 CODEC



PINE64	PINE64
Project:	SOEdge Schematic 20190919 ver 2.0
File:	21:Power-PMIC RK809-2
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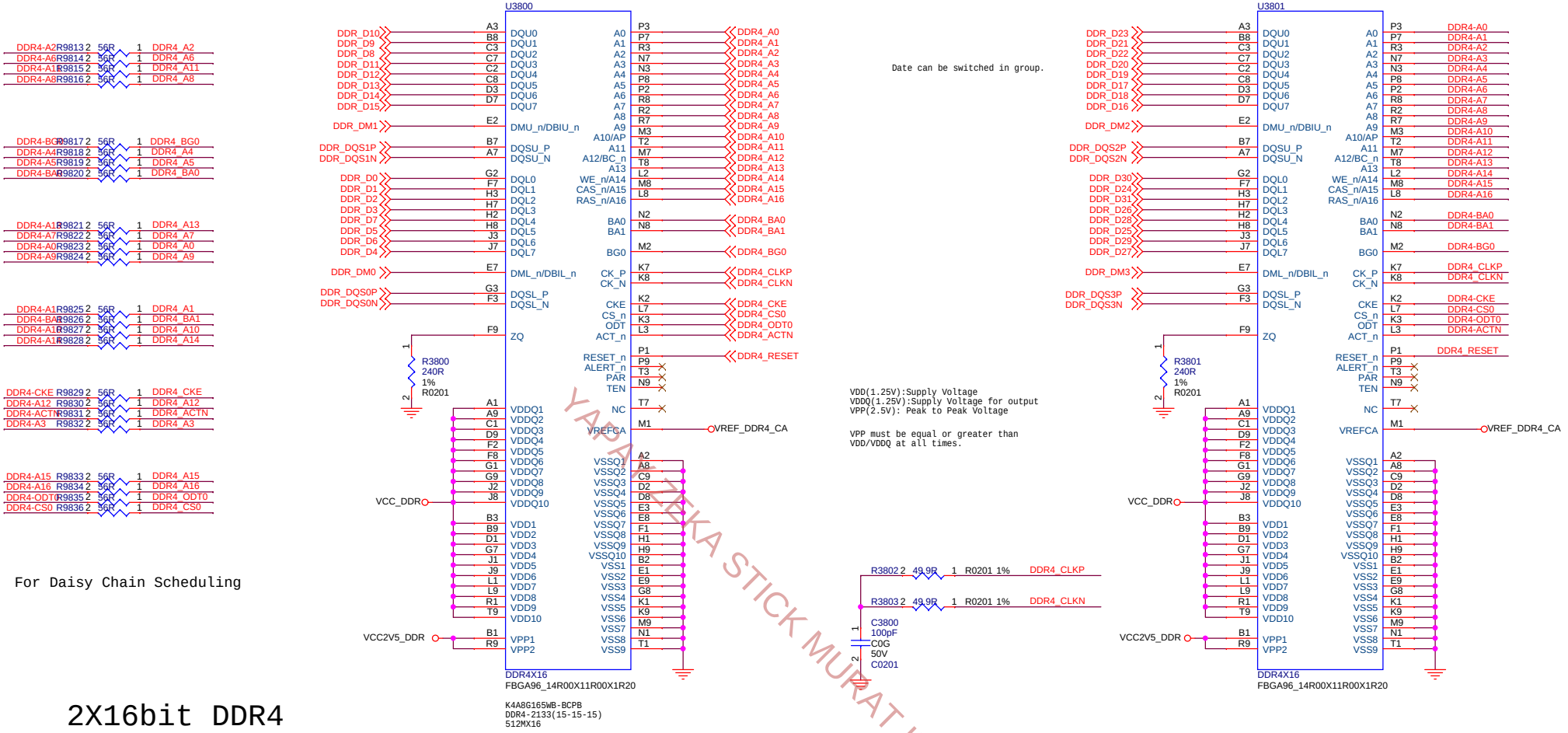
DDR4-A2 R9813 2 56R 1 DDR4_A2
DDR4-A6 R9814 2 56R 1 DDR4_A6
DDR4-A11 R9815 2 56R 1 DDR4_A11
DDR4-A8 R9816 2 56R 1 DDR4_A8
DDR4-BG0 R9817 2 56R 1 DDR4_BG0
DDR4-A4 R9818 2 56R 1 DDR4_A4
DDR4-A5 R9819 2 56R 1 DDR4_A5
DDR4-BA0 R9820 2 56R 1 DDR4_BA0
DDR4-A13 R9821 2 56R 1 DDR4_A13
DDR4-A7 R9822 2 56R 1 DDR4_A7
DDR4-A0 R9823 2 56R 1 DDR4_A0
DDR4-A9 R9824 2 56R 1 DDR4_A9
DDR4-A1 R9825 2 56R 1 DDR4_A1
DDR4-BA1 R9826 2 56R 1 DDR4_BA1
DDR4-A10 R9827 2 56R 1 DDR4_A10
DDR4-A14 R9828 2 56R 1 DDR4_A14
DDR4-CKE R9829 2 56R 1 DDR4_CKE
DDR4-A12 R9830 2 56R 1 DDR4_A12
DDR4-ACTN R9831 2 56R 1 DDR4_ACTN
DDR4-A3 R9832 2 56R 1 DDR4_A3
DDR4-A15 R9833 2 56R 1 DDR4_A15
DDR4-A16 R9834 2 56R 1 DDR4_A16
DDR4-ODT0 R9835 2 56R 1 DDR4_ODT0
DDR4-CS0 R9836 2 56R 1 DDR4_CS0
For Daisy Chain Scheduling
2X16bit DDR4
U3800
DDR_D10 DDR_D9 DDR_D8 DDR_D11 DDR_D12 DDR_D13 DDR_D14 DDR_D15
DDR_DM1
DDR_DQS1P DDR_DQS1N
DDR_D0 DDR_D1 DDR_D2 DDR_D3 DDR_D7 DDR_D5 DDR_D6 DDR_D4
DDR_DM0
DDR_DQS0P DDR_DQS0N
R3800 240R 1% R0201
VCC_DDR
VCC2V5_DDR
DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
DMU_n/DBIU_n
DQSU_P DQSU_N
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
DML_n/DBIL_n
DQSL_P DQSL_N
ZQ
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10
VPP1 VPP2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC_n A13 WE_n/A14 CAS_n/A15 RAS_n/A16
BA0 BA1 BG0
CK_P CK_N
CKE CS_n ODT ACT_n
RESET_n ALERT_n PAR TEN
NC VREFCA
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9
DDR4_A0 DDR4_A1 DDR4_A2 DDR4_A3 DDR4_A4 DDR4_A5 DDR4_A6 DDR4_A7 DDR4_A8 DDR4_A9 DDR4_A10 DDR4_A11 DDR4_A12 DDR4_A13 DDR4_A14 DDR4_A15 DDR4_A16
DDR4_BA0 DDR4_BA1 DDR4_BG0
DDR4_CLKP DDR4_CLKN
DDR4_CKE DDR4_CS0 DDR4_ODT0 DDR4_ACTN
DDR4_RESET
VREF_DDR4_CA
DDR4X16
FBGA96_14R00X11R00X1R20
K4A8G165WB-BCPB
DDR4-2133(15-15-15)
512MX16
Date can be switched in group.
VDD(1.25V):Supply Voltage
VDDQ(1.25V):Supply Voltage for output
VPP(2.5V): Peak to Peak Voltage
VPP must be equal or greater than VDD/VDDQ at all times.
R3802 2 49.9R 1 R0201 1% DDR4_CLKP
R3803 2 49.9R 1 R0201 1% DDR4_CLKN
C3800 100pF C0G 50V C0201
U3801
DDR_D23 DDR_D21 DDR_D22 DDR_D20 DDR_D19 DDR_D17 DDR_D18 DDR_D16
DDR_DM2
DDR_DQS2P DDR_DQS2N
DDR_D30 DDR_D24 DDR_D31 DDR_D26 DDR_D28 DDR_D25 DDR_D29 DDR_D27
DDR_DM3
DDR_DQS3P DDR_DQS3N
R3801 240R 1% R0201
VCC_DDR
VCC2V5_DDR
DDR4-A0 DDR4-A1 DDR4-A2 DDR4-A3 DDR4-A4 DDR4-A5 DDR4-A6 DDR4-A7 DDR4-A8 DDR4-A9 DDR4-A10 DDR4-A11 DDR4-A12 DDR4-A13 DDR4-A14 DDR4-A15 DDR4-A16
DDR4-BA0 DDR4-BA1 DDR4-BG0
DDR4_CLKP DDR4_CLKN
DDR4-CKE DDR4-CS0 DDR4-ODT0 DDR4-ACTN
DDR4_RESET
VREF_DDR4_CA
DDR4X16
FBGA96_14R00X11R00X1R20
YAPAY ZEKA STICK MURAT IRKAN 2024
VCC_DDR
C3804 C3805 C3806 C3807 C3808 C3809 C3810 C3811 C3812 C3813 C3814 C3815 C3816 C3817 C3818 C3819 100nF X5R 16V C0402
C3814 1nF X5R 50V C0402
C3818 C3819 C0201
Note:
Place these decoupling capacitances
close to the memory power supply balls
VCC_DDR
C3827 22uF X5R 6.3V C0603
C3828 22uF X5R 6.3V C0603
C3830 C3831 C3824 C3832 C3833 100nF X5R 16V C0402 C0201
C3825 100nF X5R 16V C0402
C3826 100nF X5R 16V C0402
Remind: Refer to the latest AVL for parts selection.
VCC_DDR
R3804 10K 1% R0201
C3801 100nF X5R 16V C0201
R3806 10K 1% R0201
C3820 100nF X5R 16V C0201
R3850 0R 5% R0201
VREF_DDR4_CA
C3821 1nF X5R 6.3V C0201
R3805 0R 5% R0201 DNP
VREFO_DDR
VCC2V5_DDR
C3802 C3803 100nF X5R 16V C0402
VCC_BUCK5
U3802 PT5108E23E-25
IN OUT GND EN BP
SOT_23_5
R3808 10K 5% R0402
R3807 0.05R 1% R0402
C3840 1uF 6.3V X5R C0402
C3841 DNP C0402
C3842 DNP C0402
C3843 4.7uF 6.3V X5R C0402
C3822 C3823 100nF X5R 16V C0402
PINE64
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File: 38:RAM DDR4 4x16bit
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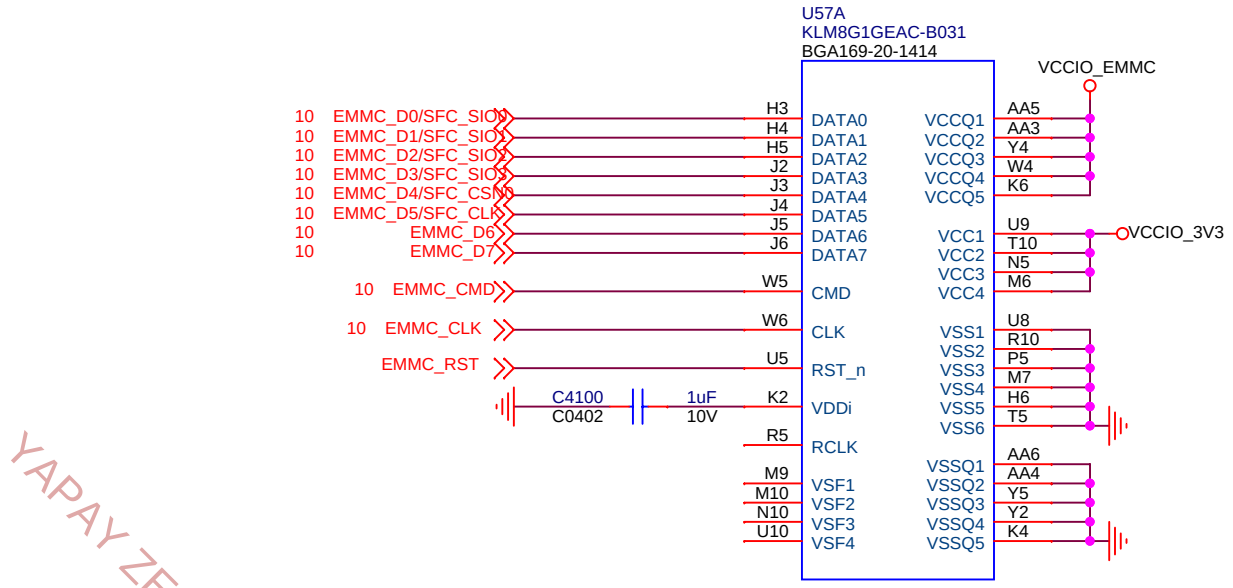
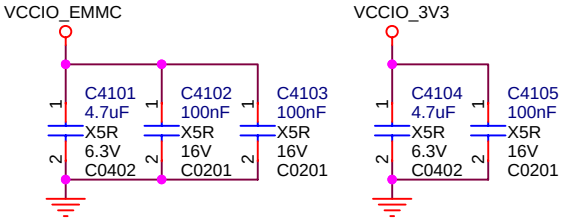
eMMC





Remind: Refer to the latest AVL for parts selection.

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Project:	SOEdge Schematic 20190919 ver 2.0		
File:	**41.EMMC**		
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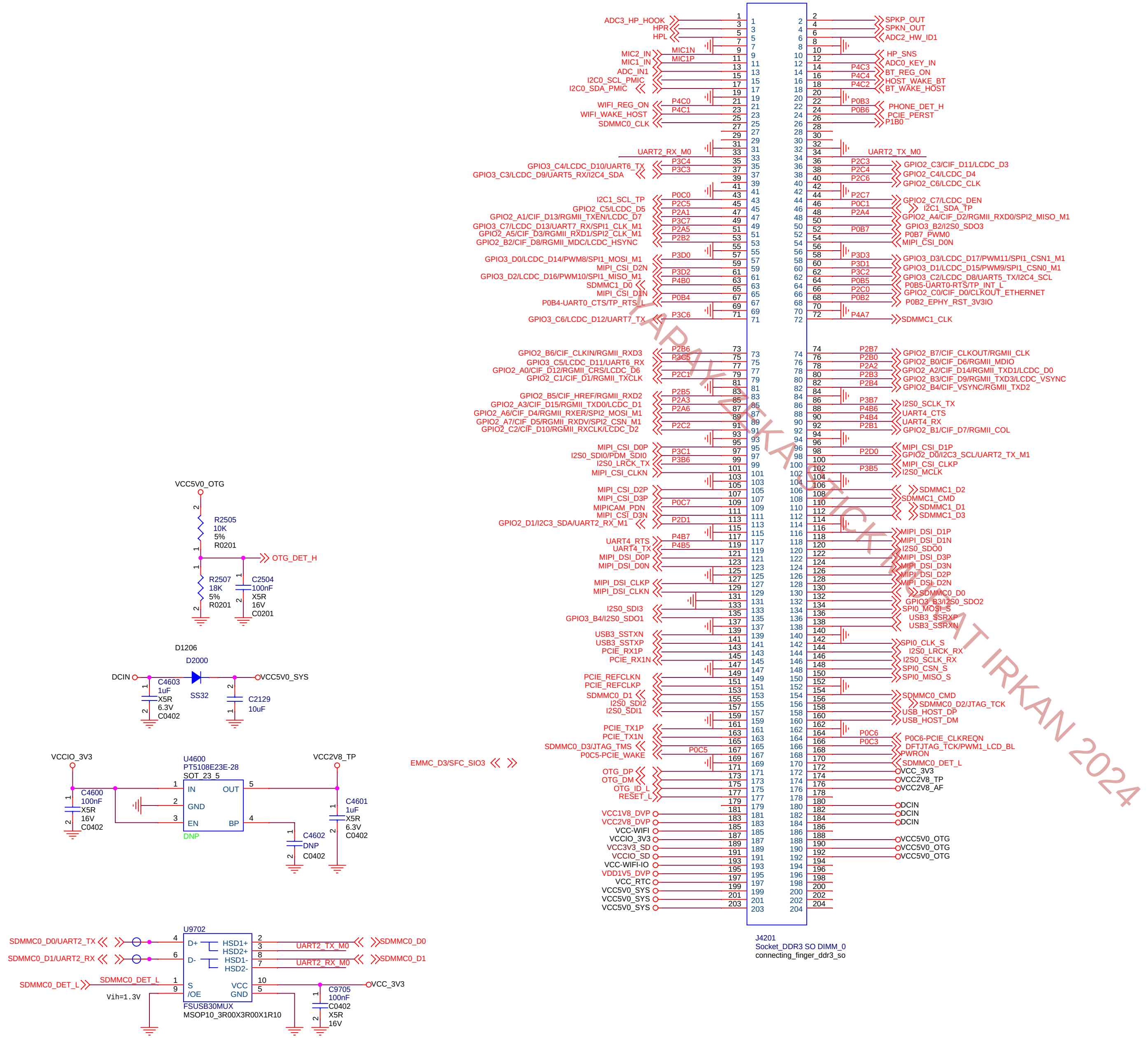
Designed by:	Rzf	Sheet:	41 of 99



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