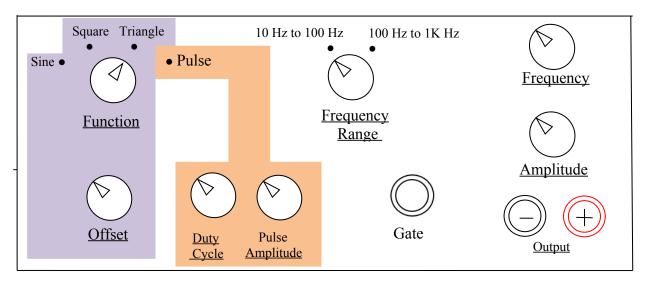
ECSE 371 V23.0

## Lab #6, Function Generator

Please carefully study H&H, Ch 4, including the Review section at the end. This is extremely valuable material. Study the circuit examples. Review the Canvas modules, especially "Op-Amp and Comparator Fundamentals" and the papers on waveform generation. For a better understanding of the generator controls and functions, investigate the operation of the simple analog-controlled function generators that are available in the lab. Operate the circuit on a +/-15 V bench supply. Saturday schematic required.

**Part 1:** Design a "Function Generator" that produces sine, square, triangle, and pulse waveforms. A sketch of an imaginary front panel is shown below, but you may use "dip switches" for the frequency range and single-turn "trimpots" mounted on your breadboard instead of panel-mount pots. The "Function" switch should be the supplied multi-pole "wafer" switch.



## **Specifications:**

Sine, triangle, and square wave outputs: 0 to 20Vpp, adjustable with the "Amplitude" control. Capable of sourcing and sinking 50mA with an external load. Rise and fall time of the square wave is to be < 100usec, measured with .01 $\mu$ Fd across output. Measure and record the THD of the triangle and sine waveforms. The THD should be less than 13% and 2%, respectively. Naturally, the amplitude of the output waveforms must be constant as the frequency changes. Record RT, FT (with .01uF), and sinewave THD (P) at one representative frequency and amplitude.

The "Offset" control applies to the sine, square, and triangle outputs. This control should shift the output waveform anywhere within the rails; (waveform may be clipped above +10V or below -10v). The output "Amplitude" control must **not** change the offset voltage, just the sine, square, or triangle wave amplitude.

<u>Pulse Output:</u> **0 to 10Vpk**. Capable of sourcing and sinking **200mA** into an external load. Rise and fall time of the pulse waveform is to be < **100 nsec**, measured with 1000 pFd across output. The Pulse Output has its own "Amplitude" control. The "Duty Cycle" control applies to the pulse waveform only, and should adjust from approximately zero to 100%.

Note that these rise and fall times are very fast, so the pulse output stage will be separate from the output stage used in the section above. Record RT and FT (with 1000pfd). Record the waveform of your pulse output at 5% duty cycle. (P)

ECSE 371 V23.0

<u>Gate</u>: this input enables and disables all the output waveforms. If there is no input, the generator operates normally. A logic high input (>2V) sets the output to 0 V.

## **Comments:**

Operate on +/- 15V bench supply.

All controls must operate independently; i.e. Offset must not change waveform amplitude, and vice versa.

For Saturday night, submit a preliminary schematic.

**For recitation:** prepare a clean, accurate, updated schematic; set up your generator and be prepared to demonstrate and show the output oscilloscope waveforms.

## **Notes:**

- ▶ Build and test **ONE STAGE AT A TIME**, but don't forget input and output loading.
- ► Carefully study the block diagram on page 3; your design should be very similar.
- ▶ No MOSFETS allowed in this project; only the specified analog ICs and stock BJTs: LM324/LM2902 quad op-amp. LM339/LM2901 quad comparator or similar.
- ► Work with an updated schematic; hand- drawn is OK and may be best to start.
- ► Concentrate on functionality; do **not** worry about trimming values.
- ► Bypass supply rails

Here are a few suggestions that might help you:

- 1. It is important for you to demonstrate functionality, rather than spending too much time on details like adjusting values to get a desired range. For example, if your waveforms look good but the frequency adjustment range is out of spec, I'd rather you continue on to the next part rather than get bogged down in adjusting values. You could always go back to it if you have time.
- 2. Always work with an updated schematic at hand. This is a very complicated project. A hand-drawn schematic is acceptable, but a <u>clear</u> and <u>accurate</u> version must be available for your recitation.
- 3. Remember to bypass your power supply rails.
- 4. Whenever you have a comparator circuit, carefully look at the entire rise and fall waveforms at a very fast sweep rate (< 1 microsecond per division) to be sure that you don't have oscillation. You should see a smooth, clean, vertical rise and fall with a slight rounding.
- 5. To prevent oscillation, keep the leads of all components connected to the positive input of a comparator very short; doing so will minimize the possibility of capacitively-coupled positive feedback which will cause oscillation. This will save you untold aggravation.

ECSE 371 V23.0

6. Using the "Larry oscillator" on a dual supply is fine; in the lecture handout use of a dual supply is discussed. Remember, however, that if you use a comparator its open-collector transistor has its emitter collected to the negative rail. Therefore, the output will swing from the negative rail to the positive rail. Note, however, that you will have 30 V dropped across the output pull-up resistor and you will have to be careful with the maximum sink current specification of the comparator. Also note that this oscillator does not produce a perfect triangle waveform unless additional steps are taken.

- 7. Depending on their design, the output stages you use for the sine-square-triangle output may not be appropriate for the pulse output. The pulse output requires very fast rise and fall times.
- 8. For the sine, square, and triangle functions, generating a waveform with a fixed, 50% duty cycle will be fine. However, for the pulse generator you need a duty cycle control that will change the pulse width without changing the frequency. Please study the block diagram provided. The approach shown is to use the sign/square/triangle generator to produce the pulse frequency, and also to generate a variable duty-cycle pulse by using a comparator to compare the triangle wave to a DC voltage. Changing this DC voltage will produce a variable duty-cycle pulse. See below:

