Implementation of a High-Speed Low-Power 32-Bit Adder in 70nm Technology

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Abstract— **In this article, the performance and power dissipation of two differential logic circuits in deep sub-micron technologies are obtained and compared together, and the superior topology is introduced. Low Voltage Swing (LVS) technique which improves circuit performance and lowers power consumption is described in detail. We conclude this article with the design, simulation and optimization of a high-speed low-power 32-bit adder using the LVS technique in 70nm technology. This circuit can operate at 10GHz clock frequency with power dissipation as low as 2.58 mW/GHz.**

I. Introduction

The demands for higher processing performance, more complex processors, and lower power dissipation lead to the reduction of the dimensions of the components integrated on one chip. With feature sizes being reduced towards deep sub-micron (DSM) generations, questions have arisen regarding the ability to achieve favorable cost versus performance/power trade-offs in CMOS technologies [1]. Digital circuit designers are looking for different ways to reduce noise in DSM circuits, while trying to improve performance, and reduce power dissipation of the circuits.

Low Voltage Swing (LVS) technique has been considered an efficient way to reduce power consumption while reaching higher speeds. In this technique internal nodes of the circuit have low voltage swing and output nodes have full voltage swing using sense amplifiers. The LVS technique can be used in busses to optimize signal transfer. These busses use LVS drivers and have sense amplifiers in their receivers [2]. In domino logic, output inverters can be implemented with low voltage output swing optimizing signal propagation time [3]. Some other designers use this technique in logic implementation using pass transistors [4]. An LVS clock signal can even be used to reduce power dissipation, while some LVS latches have been designed to work with such a clock signal [5, 6].

LVS logic has been used for implementation of the new generation of some processors. By using it, the integer core of the new Pentium 4 processor can operate at 7GHz which is twice the processor's frequency in 90nm technology [7].

In the next section, we will simulate a 4-bit adder using two types of differential logic. The simulation is done in 70nm BPTM (Berkeley Predictive Technology Model) for CMOS transistors [8]. In Section III, two types of sense amplifiers and their performance will be described. In Section IV, we will first implement a 16-bit adder, both in 100nm and 70nm technologies. After optimizing the circuit's speed and power dissipation in 70nm technology, we will implement a high-speed low-power 32-bit adder. Section V is dedicated to the conclusion and future work.

II. Simulating a 4-Bit Adder Using Two Kinds of Differential Logics

In this section, we will design and simulate two kinds of adders, using differential logics in 70nm technology. A 0.9V power supply is used for this technology in the simulations. We used the fully-differential dual-rail domino logic to implement the first adder. The sum-generate and carry-generate building blocks are shown in Fig. 1. Four building blocks of each circuit have been cascaded to make a 4-bit adder.

All outputs will go low at the low level of the clock signal. The high level of the clock signal starts the evaluation phase. All inputs are kept zero during the precharge phase. In the evaluation phase, complementary inputs are applied to each stage and the *carry-in* is kept at one. In this case, the maximum carry propagation time is stimulated. After finding maximum carry propagation time, we obtained maximum clock frequency of the circuit. For this circuit, we reached the maximum of 3GHz for clock frequency by simulating it in 70nm technology. Footer transistors are eliminated in this circuit to reach higher speed. This causes extra power dissipation and also causes the precharge time to increase.

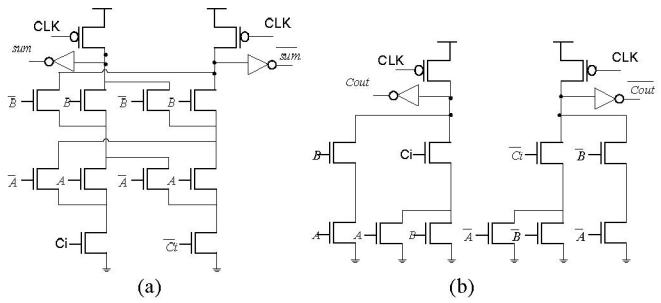


Fig. 1. Fully-differential dual-rail adder. (a) The sum-generate circuit. (b) The carry-generate circuit [9].

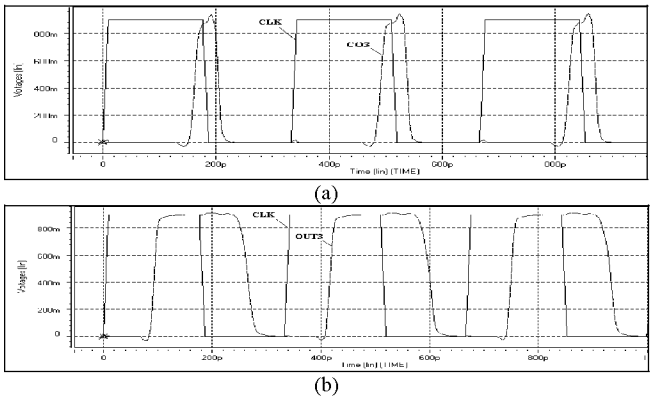


Fig. 2. Fully differential dual-rail adder output waveforms. (a) Carry-out (CO3) when inputs are complemented and carry-in is one. (b) Sum output (OUT3) of the last stage when inputs are complemented and carry-in is zero.

The outputs of the circuit are shown in Fig. 2.

Sakurai *et al.* [4] used the LVS (Low Voltage Swing) technique to improve the performance of their circuits. Applying this technique in DCN (Diffusion Connected Network) pass transistors in critical paths of a circuit will evaluate the logic functions which have low voltage swing. The output voltage swing of this kind of structure finds standard voltage swing using sense amplifiers [4].

The discussed 4-bit adder cannot directly use the LVS technique, since in cascading 1-bit adders, the output of each circuit is applied to the gate of one of the transistors of the next stage. If the input voltage is not high enough, the transistor may not turn on. The circuit's structure should be changed in order to use the LVS technique. Therefore, we used a type of differential logic which had been utilized in [7]. This differential logic is based on series pass transistors. All transistors in this network have low voltage swing to improve circuit performance. One stage of the adder with this logic is shown in Fig. 3.

In this circuit P, G and K are propagate, generate and kill signals respectively. These signals are generated with CDL (Complementary Domino Logic) circuits [7].

We cascaded four stages of the network shown in Fig. 3 to implement a 4-bit adder. We note that the transistors M1 and M2 are used only in the first stage.

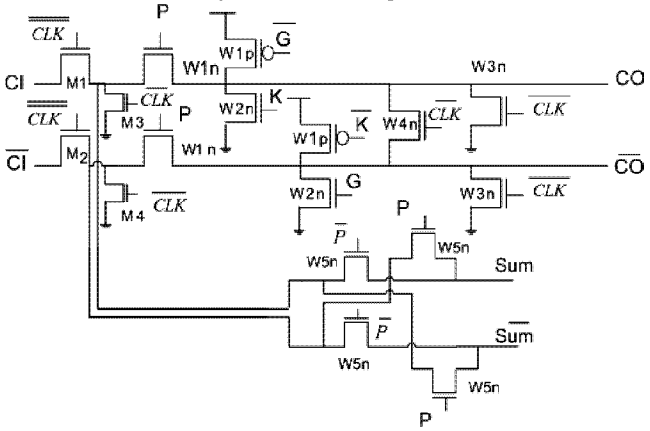


Fig. 3. One stage of the adder using LVS technique (modified version of the same figure in [7]).

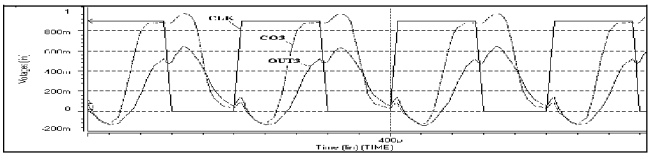


Fig. 4. Outputs of last stage of the adder using LVS technique without sense amplifier.

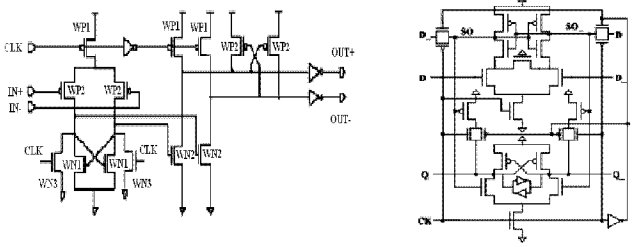


Fig. 5. Sense amplifiers. (a) LSA [7]. (b) SAFF [10].

Unlike the previous adder, this one has a *predischarge* phase. In order to show the output transition from *0* to *1*, this time we kept each of the inputs at the binary value 1111, and made the *carry-in*=1, so that *carry-out* and all *sum* outputs become 1. In this situation, the results are shown in Fig. 4. As seen in this figure, the *carry-out* output has full swing because it is generated by the G signal in the last stage. However, the *out3* output does not have full swing because it is passed and generated through a chain of pass transistors.

To reach the standard voltage levels, the outputs of the circuit were applied to some sense amplifiers. The result of the simulation which is shown in Fig. 4 comes with 10GHz clock frequency. So, the circuit can operate at 10GHz clock frequency if its sense amplifiers can accommodate this frequency. In the next section, we will review the design of a proper sense amplifier.

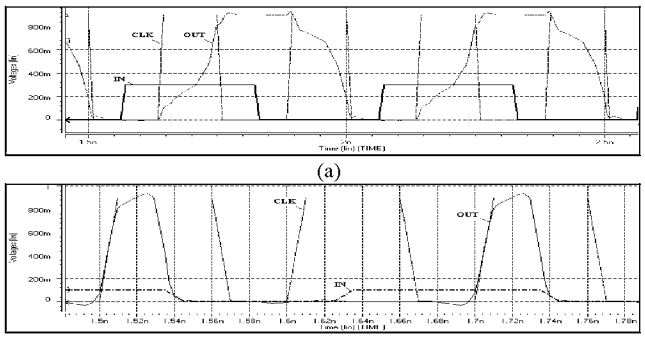
III. Sense Amplifiers

We have studied different types of sense amplifier (SA) structures. Besides Latched SA (LSA) which was implemented in 90nm technology and could operate at 7GHz clock frequency [7], we found one other appropriate SA that could potentially be used in LVS circuits. This SA is called sense amplifier flip-flop (SAFF) that can amplify its inputs and restore them to supply levels [10]. The schematics of these two circuits are shown in Fig. 5.

The SAs were simulated in 70nm technology. For 0.9V

TABLE I
W's of Latched Sense Amplifier Transistors after Optimization in 70nm Technology

WN1	420 nm
WN2	420 nm
WN3	140 nm
WP1	2.1 µm
WP2	420 nm



(a)

(b)

Fig. 6. The output waveforms of the sense amplifiers. (a) SAFF (b) Optimized LSA.

TABLE II
COMPARISON BETWEEN LSA AND SAFF IN 70NM TECHNOLOGY

	SAFF	LSA
Technology	70nm	70nm
Max freq	4GHz	10GHz
avgpower	23.9 µW/GHz	21.5 µW/GHz
maxpower	48.3 µW/GHz	61.9 µW/GHz

power supply, the minimum input level that the LSA can amplify is 0.1V, while it is 0.3V for the SAFF.

We reached the maximum of 4GHz clock frequency for SAFF, while by optimizing W's of the transistors, LSA can operate at 10GHz clock frequency. The results of optimization are shown in Table I. We note that these widths should remain technology-compatible as well in terms of ΔW steps.

These two SAs are compared in maximum clock frequency and power dissipation in Table II. As seen in the table, LSA consumes less power than SAFF, and its clock frequency is 2.5 times higher. We conclude that in 70nm technology and for the LVS circuits, optimized LSA is the best choice.

The output waveforms of the SAs are shown in Fig. 6.

Using this SA, we will implement a 16-bit carry-skip adder and a 32-bit carry select adder with the LVS technique in the next section.

IV. IMPLEMENTING A HIGH-SPEED LOW-POWER 32-BIT ADDER IN 70NM TECHNOLOGY

A. 16-Bit Carry-Skip Adder

A one-stage adder building block which uses LVS technique was shown in Fig. 3. We cascaded 16 blocks of its kind to implement a 16-bit adder. To reduce the carry propagation time, we used a carry-skip network as shown in Fig. 7 [7].

In [7], a 16-bit adder had been implemented in 90nm technology with 7GHz clock frequency. By optimizing the W's of the circuit's transistors, we implemented this 16-bit carry-skip adder in both 100nm and 70nm technologies. For circuits in 100nm technology, a 1.1V power supply was used. In 100nm technology, the adder was operating at

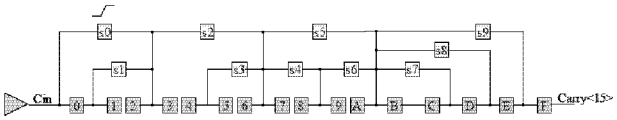


Fig. 7. Carry-skip network [7].

TABLE III
W'S OF LVS BUILDING BLOCK TRANSISTORS AFTER OPTIMIZATION IN 70NM TECHNOLOGY

W1N	1400 nm
W2N	700 nm
W3N	140 nm
W4N	140 nm
W5N	210 nm
W1P	1400 nm

a maximum frequency of 8GHz, and in 70nm technology, this maximum was at 10GHz. In Table III, the HSPICE optimization results obtained for the W's of the transistors used in building the LVS circuit -as shown in Fig. 3- are listed. The results are for 70nm technology.

The final output waveform of the 16-bit adder in 70nm technology, after passing through the SAs, is shown in Fig. 8.

After optimizing the speed of the circuit, we applied some techniques to reduce its power dissipation. Power dissipation of the circuit will be reduced by:

- Removing transistors M3 and M4 shown in Fig. 3. These transistors will cause DC power dissipation in a time equal to the propagation delay of a basic inverter. Therefore, they are removed from the first stage;
- Adding clock controlled NMOS transistors to pull down network of the CDL circuits that generate P, G, and K signals. This will prevent static power dissipation;
- In the reset phase of the LVS circuit G, $\overline{G}$, K, and $\overline{K}$ are precharged while P and $\overline{P}$ are predischarged.

Table IV shows the comparison between maximum clock frequency and power dissipation between two 16-bit carry-skip adders in 70nm and 100nm technologies after our modifications.

As shown in the table, by technology scaling, higher speeds and lower power dissipations can be obtained despite more severe static power consumption of 70nm technology.

B. 32-Bit Carry-Select Adder

Next, we designed and simulated a high-speed low-power 32-bit adder in 70nm technology.

To make a 32-bit adder, we adapted and optimized the 16-bit carry-skip adder proposed in [7] as our main block. We used three of these blocks to make a 32-bit carry-select adder. The circuit is shown in Fig. 9.

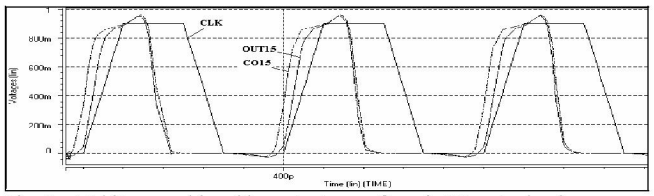


Fig. 8. 16-bit carry-skip adder output waveform in 70nm technology.

The lower 16 bits of inputs A and B are applied to the first 16-bit adder block, and also the circuit's *carry-in*. The upper halves of the input bits are applied to both of the remaining parallel 16-bit adder blocks. From these two blocks, one has *0* as its permanent *carry-in* input and the other has *1*. The outputs of these two adders and also their *carry-outs* are the inputs of a multiplexer. The first block will produce the lower significant output bits. The *carry-out* of this block is used as the select input of the 2-1 multiplexer. Outputs of this multiplexer are 17 bits. Therefore, the output of the multiplexer provides the remaining output bits of the whole adder and also its *carry-out*. This adder has a delay equal to the delay of a 16-bit carry-skip adder plus the delay of a multiplexer. In order to reach a better functionality, the sense amplifiers for the 16 most significant output bits were transferred to the output of the multiplexer.

In Table V, a 16-bit adder is compared with a 32-bit adder in 70nm technology.

It is shown in the table that the 32-bit adder can operate with 10GHz clock frequency similar to the 16-bit adder. Its power dissipation is higher than that of the 16-bit adder, because it uses three times more transistors.

V. Conclusion and Future Work

In this article, we were looking for the highest speed and the lowest power logic to be used in processors of 70nm technology. In our research, we used a technique called LVS or low voltage swing technique. This technique employs differential pass transistor logic to improve speed and reduce power dissipation.

In [7] this technique was used to implement the integer core of the Pentium 4 processor. This circuit can operate at 7GHz clock frequency in 90nm technology. We adapted this technique to implement a 16-bit carry-skip adder. By a modified design and optimization, this adder can operate at an 8GHz clock frequency with 2.22 mW/GHz in 100nm technology, and with 10GHz clock frequency and 0.97 mW/GHz in 70nm technology.

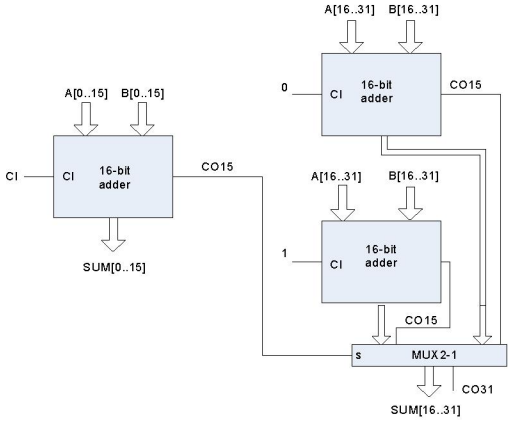


Fig. 9. 32-bit carry-select adder.

TABLE IV
Comparison between Two 16-Bit Carry-Skip Adders in 70 and 100nm Technologies

Technology	70nm	100nm
Max freq	10GHz	8GHz
avgpower	0.97 mW/GHz	2.22 mW/GHz
maxpower	2.93 mW/GHz	5.35 mW/GHz

TABLE V
Comparison between 16-Bit and 32-Bit Adders in 70nm Technology

	16 bit adder	32 bit adder
Max freq	10GHz	10GHz
Max t_p	97 ps	99 ps
avgpower	0.97 mW/GHz	2.58 mW/GHz
maxpower	2.93 mW/GHz	7.71 mW/GHz

Next, we designed a 32-bit carry-select adder using the LVS technique for the next generation of processors in 70nm technology. This circuit can operate at 10GHz clock frequency with power dissipation as low as 2.58 mW/GHz.

Looking for proper structures to deal with sub 50nm technologies with higher performance and lower power dissipation, defines our future work.

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