International Institue of Information Technology Bangalore

Digital CMOS VLSI Design

Implementation of a High-Speed Low-Power 32-Bit Adder

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Abstract

The paper addresses the design of a high-speed, low-power 32-bit adder suitable for modern processors. By comparing two types of differential logic circuits, the authors of the paper identify efficient design strategies for deep sub-micron (DSM) technologies. We will employ the Low Voltage Swing (LVS) technique to minimize power consumption and optimize speed. The final design operates at 10 GHz with a power dissipation of only 2.58 mW per GHz, demonstrating its suitability for energy-efficient and high-performance applications.

Introduction

Shrinking the size of circuits to DSM scales introduces challenges like increased noise, delays, and power dissipation. These issues can hinder the performance of digital circuits, particularly in processors that require both speed and energy efficiency. To tackle these challenges, we use the LVS technique. LVS reduces voltage fluctuations in the circuit's internal nodes while maintaining full voltage swings at the outputs using sense amplifiers. This technique enhances speed and reduces power consumption, making it ideal for applications like adders. Adders are fundamental in processors, and we aim to implement a 32-bit adder using LVS, optimized for performance in 70nm technology.

Dual Differential 4-Bit Adder

We begin by designing and simulating a fully-differential dual-rail 4-bit adder to validate our methods. We use dual-rail domino logic, a design approach where every bit of data is represented by two complementary signals. This ensures higher accuracy and reduces the likelihood of errors. The 4-bit adder comprises sum-generation and carry-generation blocks, which are fundamental components of any adder. By cascading four such blocks, we create a functioning 4-bit adder. Simulations reveal that the adder achieves a clock frequency of up to 3 GHz in 70nm technology, demonstrating the potential of the chosen techniques for building larger adders.

The transistor logic that is being used here is the Dynamic Pass Transistor logic. It has been used to reduce the number of transistors in the circuit in order to increase the overall speed of the circuit. The given dynamic logic is unfooted to reduce the delay. Below is the logic used in the adder :

`Sum (Sum)` : Sum $= A \oplus B \oplus C$

`Carry-Out (Cout)` : Cout $= (A \cdot B) + (C_i \cdot (A \oplus B))$

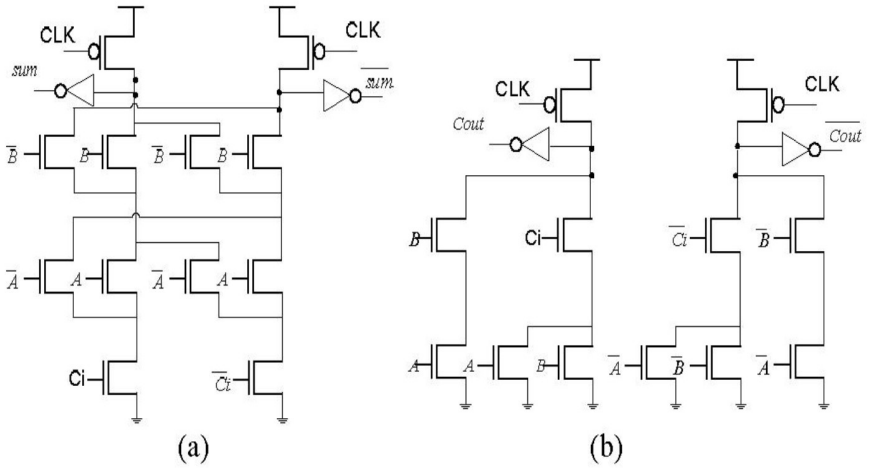

FIGURE 1 – Dual Differential Adder given in the paper.

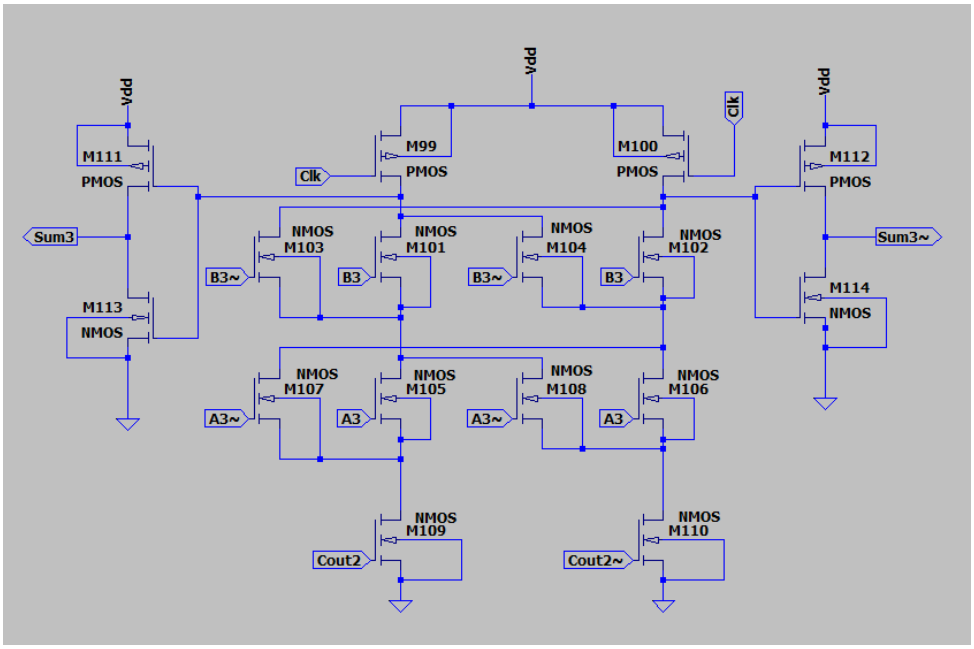

FIGURE 2 – Dual Differential Adder Sum part in ltpsice for 1 bit.

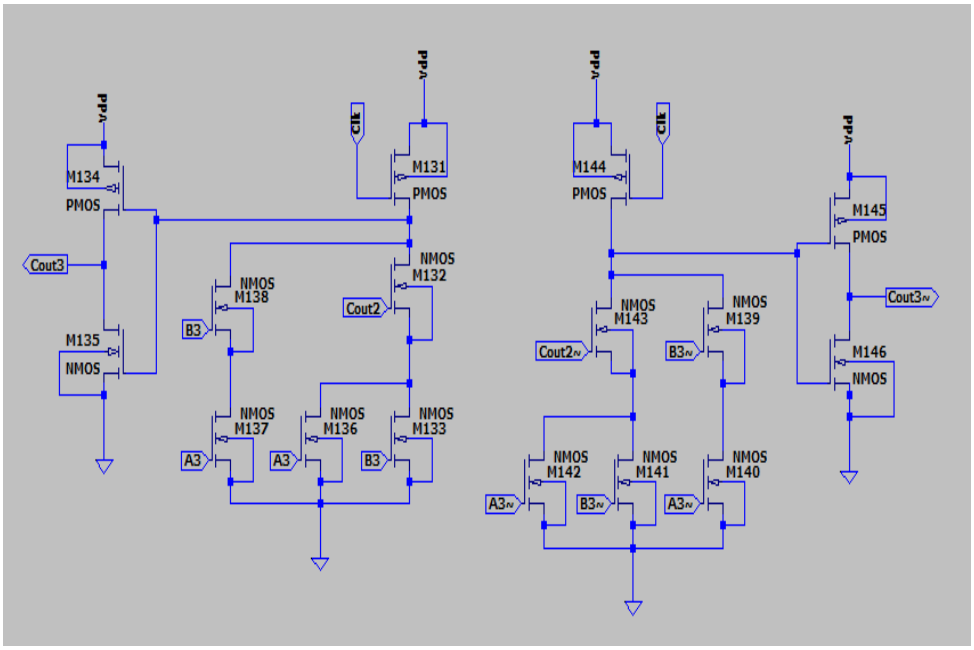

FIGURE 3 – Dual Differential Adder Cout part in ltspice for 1 bit.

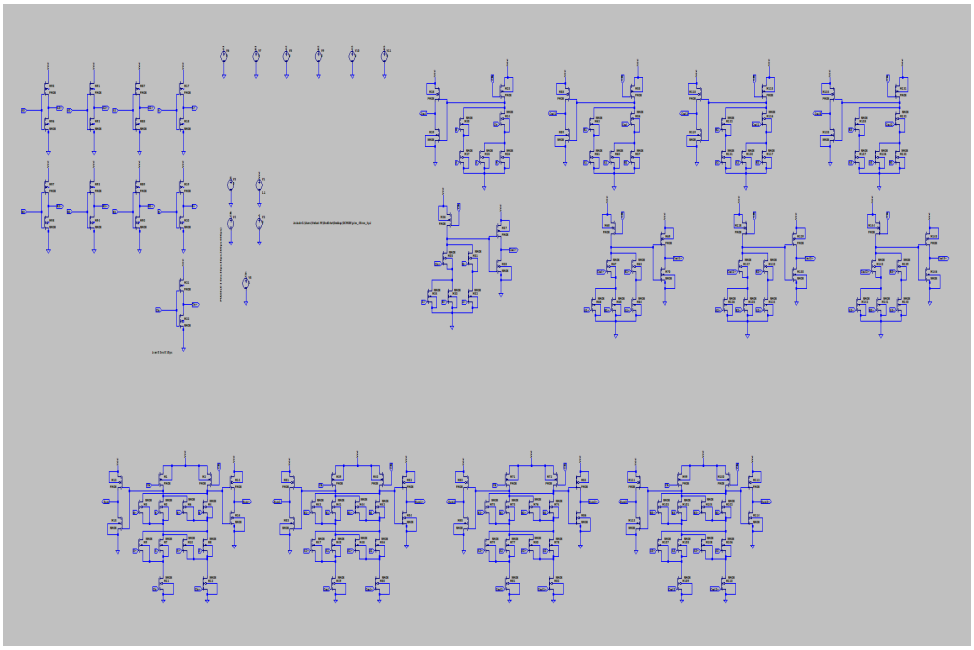

FIGURE 4 – Entire Dual Differential adder in ltspice for 4 bit.

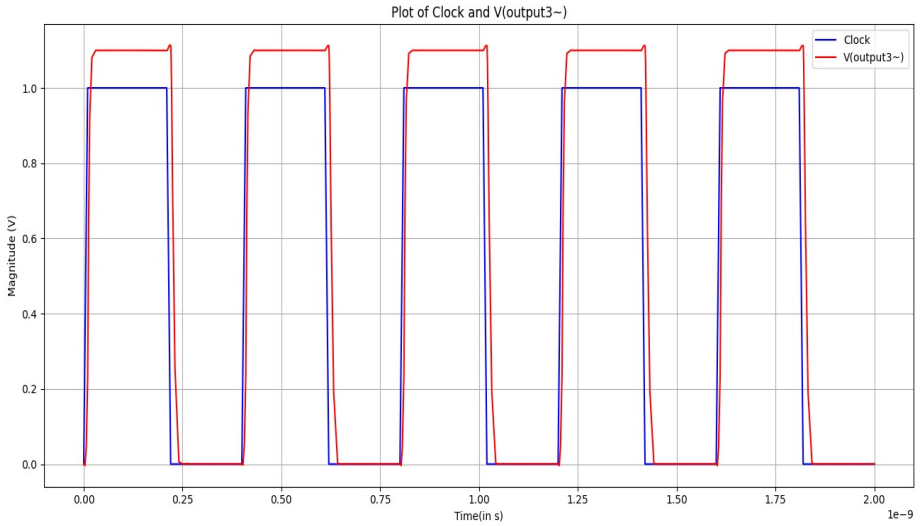

FIGURE 5 – co3 output for Cin=1, A=1, B=1.

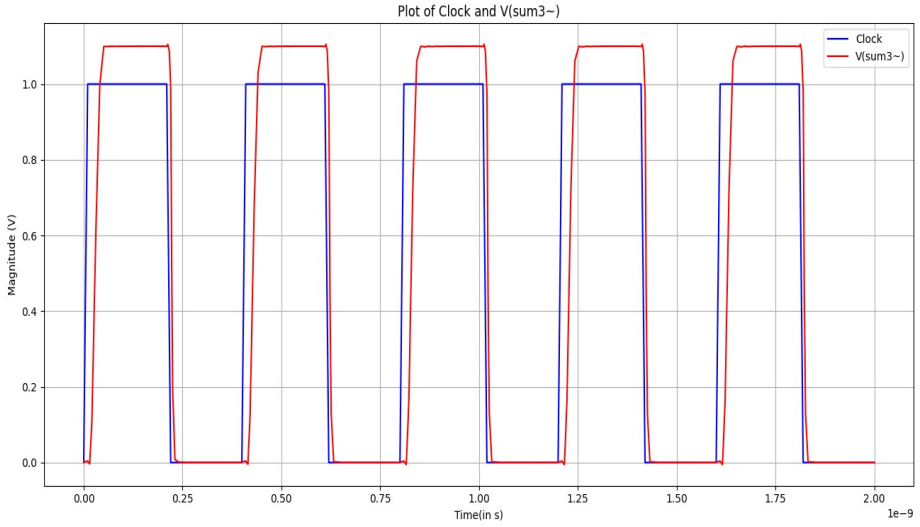

FIGURE 6 – sum3 output for Cin=1, A=1, B=1.

Low Voltage Swing Techniques

Low voltage swing techniques are critical in modern digital circuit design, especially in deep submicron technology nodes, where power efficiency and heat dissipation are key challenges. These techniques reduce power consumption and delay by lowering the amplitude of voltage transitions that represent binary states. Traditional voltage levels such as 5V or 3.3V are reduced to much lower levels, often around 1.8V or less.

0.1 Overview of Low Voltage Swing Techniques

The following are some commonly employed techniques for achieving low voltage swings in digital circuits :

- **Reduced-Swing Differential Signaling** : Involves using differential pairs with a smaller voltage swing (often a fraction of the main supply voltage). Minimizes power loss as switching activity reduces current spikes and capacitive losses.
- **Source-Coupled Logic (SCL)** : Operates at reduced voltage swings and is often used in high-speed, low-power circuits like transceivers and RF modules. Uses current-steering mechanisms instead of traditional CMOS switching to limit voltage swings and maintain speed.
- **Dynamic Threshold MOS (DTMOS)** : Utilizes a lower threshold voltage during operation, which reduces the necessary voltage swing for a switch. Beneficial for ultra-low-power applications where voltage levels are critically low.
- **Swing-Limited CMOS Logic** : Limits the output swing of CMOS gates by modifying the circuit design to achieve lower swings, such as by using feedback or adding resistive elements. Reduces dynamic power dissipation as switching power is proportional to the square of the swing voltage.
- **Low-Swing Bus Encoding** : Optimizes bus voltage swings, typically on long interconnects, by encoding signals in a way that minimizes transitions or reduces swing on data lines. Reduces noise and overall power consumption for on-chip and off-chip buses.

0.2 Advantages of Low Voltage Swing Techniques

Implementing low voltage swing techniques addresses several challenges of deep submicron design :

- `Power Efficiency` : Reduced voltage swings directly lower dynamic power consumption.
- `Delay Reduction` : Smaller voltage transitions result in faster switching speeds.
- `Thermal Management` : Lower power dissipation helps in minimizing heat generation, improving device reliability.

These techniques ensure operational integrity and speed while meeting the stringent power and thermal constraints of modern electronic designs.

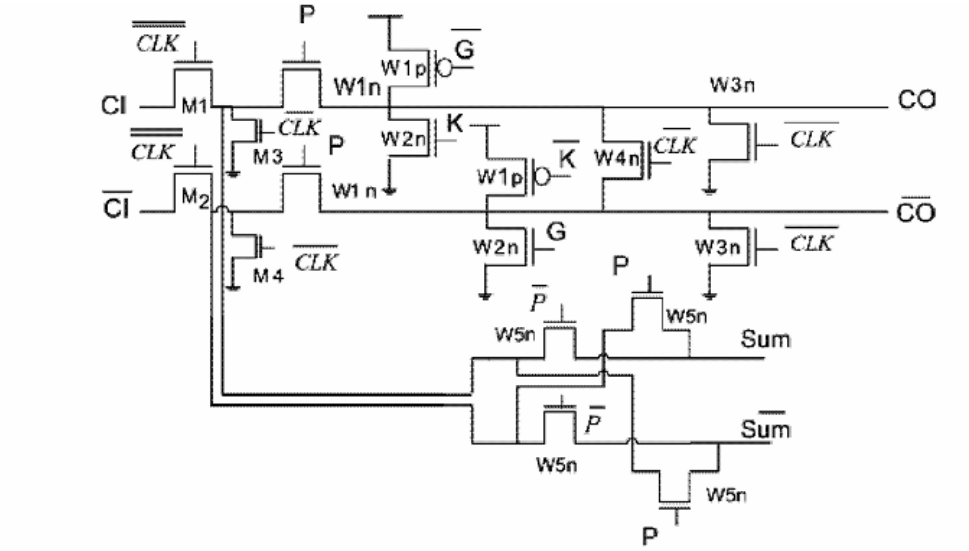

FIGURE 7 – One bit adder using LVS given in paper.

P	G	C_{in}	C_{out}
0	0	X	0
X	1	X	1
1	0	1	1
1	0	0	0

TABLE 1 – Truth Table for Carry Generation

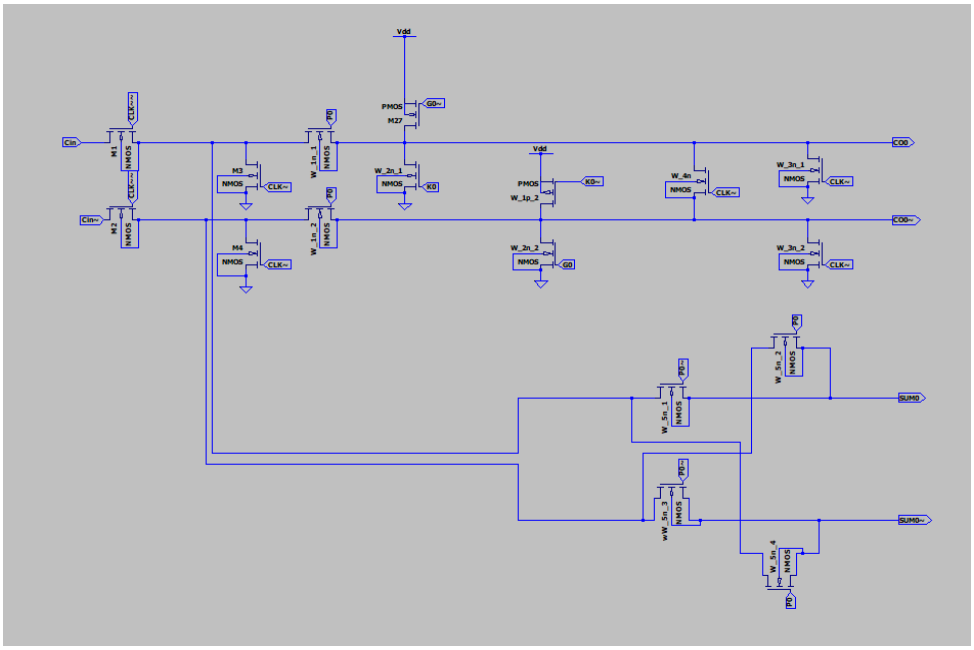

FIGURE 8 – One bit adder using LVS implementation in ltspice.

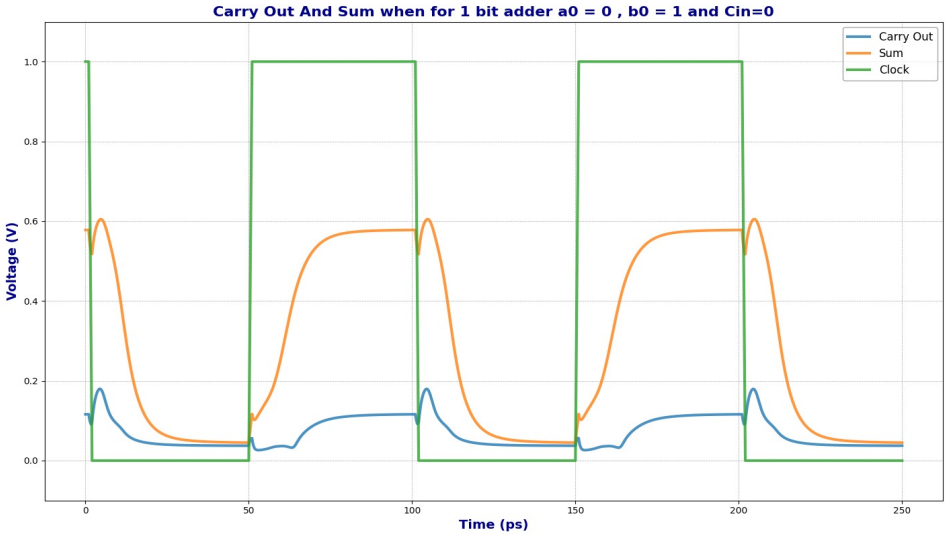

FIGURE 9 – One bit LVS adder output without SAFF

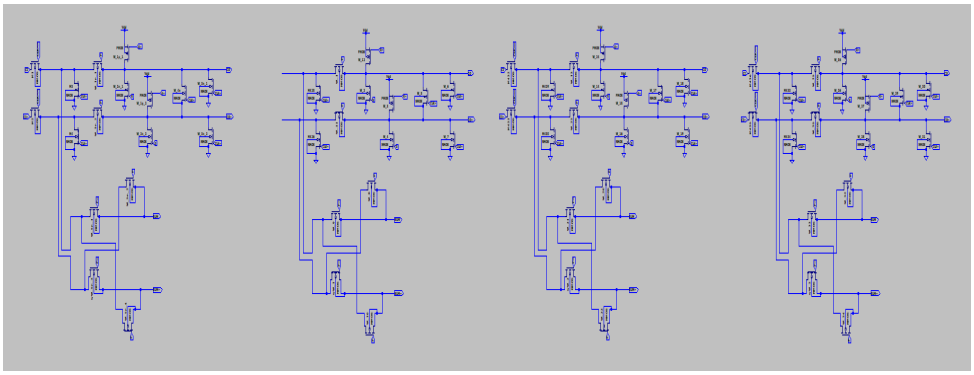

FIGURE 10 – 4 bit adder using LVS implementation in ltspice.

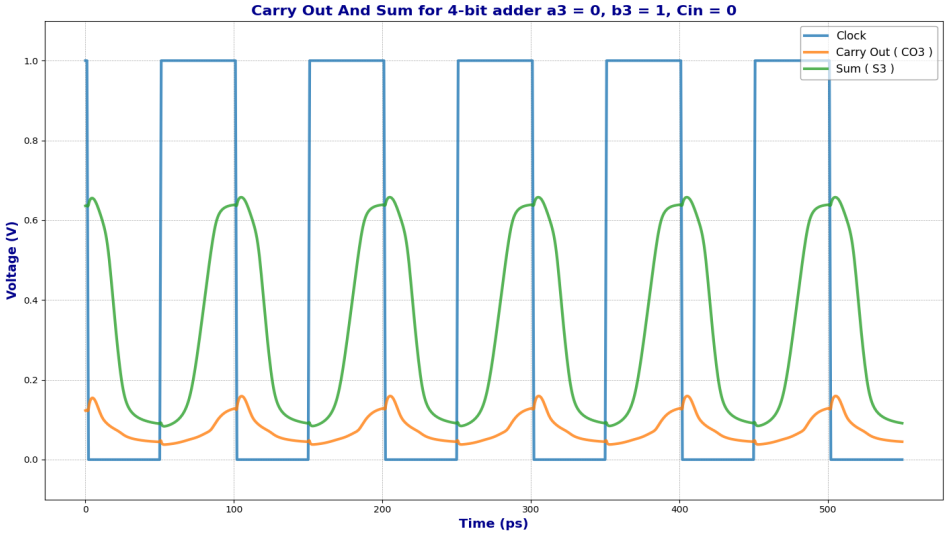

FIGURE 11 – 4 bit LVS adder output without LSA. A=1 B=1 Co=0

Latched Sense Amplifier Theory

A **latched sense amplifier** is a type of sense amplifier commonly used in memory systems, such as SRAM (Static Random-Access Memory) and DRAM (Dynamic Random-Access Memory), to read stored data efficiently and quickly. It amplifies weak signals from memory cells to a readable logic level while maintaining low power consumption and fast operation.

Key Concepts

1. **Weak Signal from Memory Cells :**
   — Memory cells output weak voltage differences due to capacitance or small currents. These small differences need amplification to be interpreted as logical 0 or 1.
2. **Sense Amplifier Operation :**
   — Detects small voltage differences between bit lines (bit line and complementary bit line) and amplifies them to full logic levels.
3. **Latching Mechanism :**
   — A latched sense amplifier uses *positive feedback* to quickly drive the output to a stable logic state (0 or 1) and hold it until the next read operation.

Structure and Working

1. **Differential Pair :**
   — The sense amplifier typically uses a differential pair of transistors to sense small voltage differences between the bit lines.
   — This design provides high sensitivity and noise rejection.
2. **Positive Feedback Loop :**
   — The latched configuration incorporates cross-coupled inverters or similar circuits to form a *positive feedback loop*.
   — This feedback mechanism quickly reinforces the initial voltage difference, pulling one output to a strong 0 and the other to a strong 1.
3. **Precharging :**
   — Before a read operation, the bit lines are precharged to a known voltage (usually half of the supply voltage).
   — This precharging ensures consistent operation of the sense amplifier.
4. **Enable Signal :**
   — A control signal (often called *Sense Enable*) activates the sense amplifier during the memory read cycle.
   — The enable signal ensures that the amplifier operates only when valid data is present on the bit lines.
5. **Speed and Efficiency :**
   — The positive feedback mechanism allows for fast amplification, making latched sense amplifiers suitable for high-speed memory systems.

Advantages

— **Speed :** Latching provides rapid signal amplification, improving memory read speeds.
— **Low Power Consumption :** Only activated during read cycles, reducing overall power usage.
— **Noise Immunity :** Differential sensing enhances noise rejection, improving reliability.

Applications

— Used in SRAM and DRAM to sense and amplify data stored in memory cells.
— Found in high-speed memory interfaces and modern processors where quick access to data is critical.

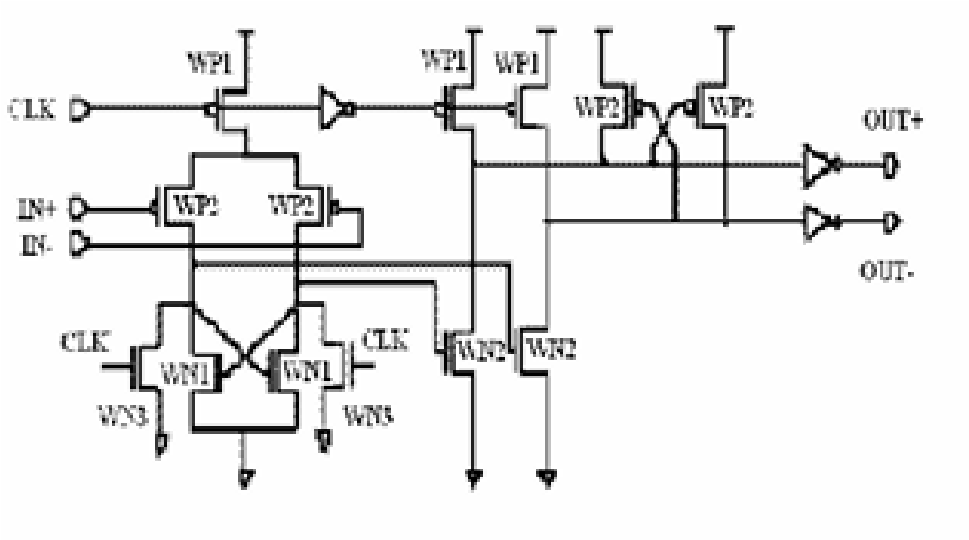

FIGURE 12 – LSA adder given in paper

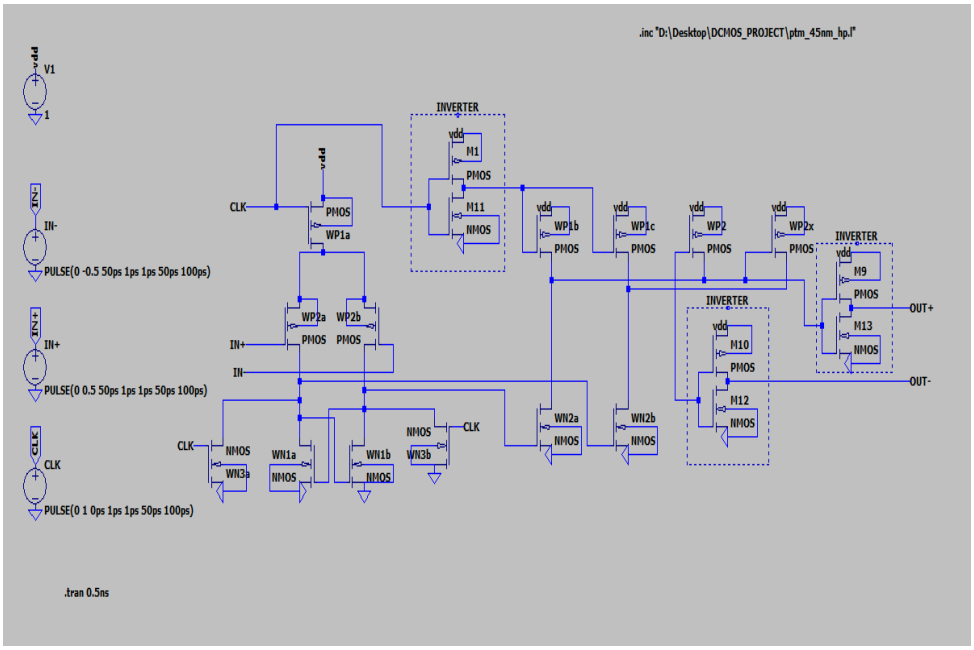

FIGURE 13 – LSA adder implemented by us on LTSPICE

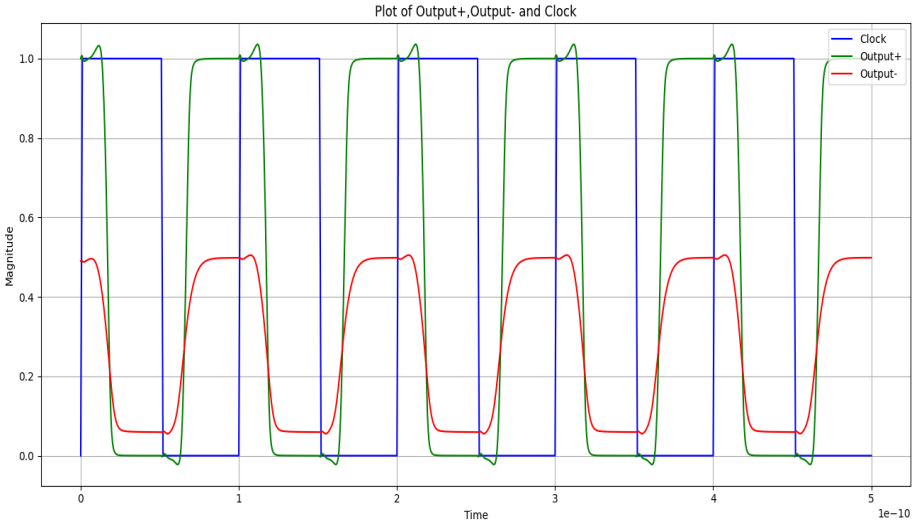

FIGURE 14 – LSA output

Use of SAFF in LVS Technology

In LVS (Layout Versus Schematic) technology, the Sense-Amplifier-Based Flip-Flop (SAFF) is used as a reliable memory element in digital circuits. The SAFF helps differentiate between low and high voltage levels by amplifying the low input values. This amplification ensures that even small voltage differences are detected accurately, providing stable data latching during the clock transition. The SAFF's ability to operate reliably under clock-level transitions and to amplify the input voltage makes it ideal for high-speed and low-voltage applications.

1 Advantages

- **Improved Reliability :** Unlike MS latches, SAFF is less susceptible to errors due to transparent behavior, especially when there is insufficient margin between clock phases.
- **Voltage Amplification :** SAFF amplifies low input voltages, helping to accurately differentiate between low and high voltage levels, improving detection and data integrity.
- **Better Robustness :** It operates effectively under varying clock transitions (low-to-high or high-to-low), ensuring stable latch operation.
- **Faster Operation :** SAFF reduces timing errors and improves the overall performance of digital circuits, which is crucial in high-speed applications.

2 Disadvantages

- **Complexity in Layout :** The design and layout of SAFF-based circuits may be more complex compared to simpler flip-flops.
- **Increased Power Consumption :** The SAFF circuit may require more power due to the pulse-generating and sensing stages, which could be a concern in low-power designs.
- **Layout Sensitivity :** Variations in the layout process may affect the timing and reliability of the SAFF, especially when scaling down to smaller process nodes.

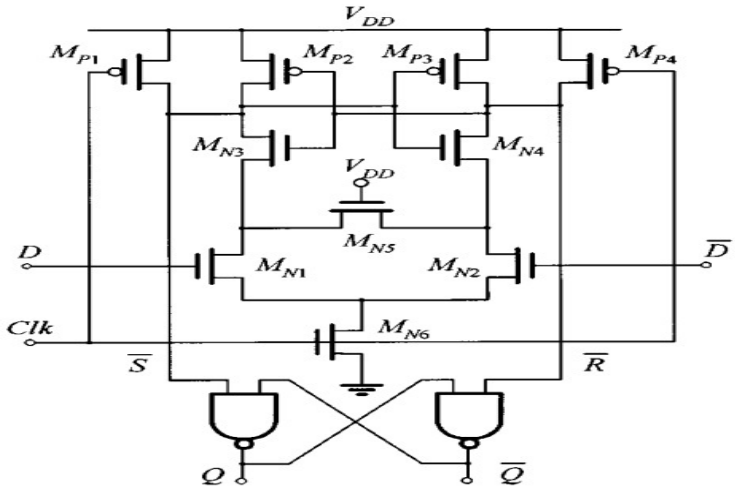

FIGURE 15 – Sense amplifier based flip flop

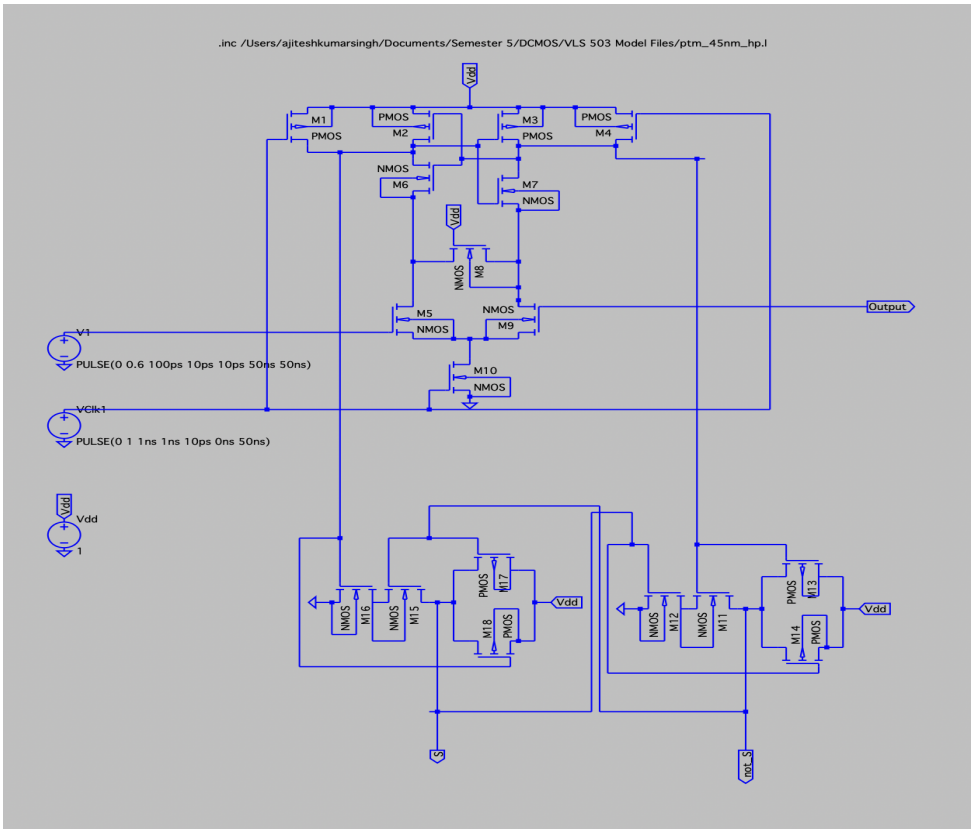

FIGURE 16 – SAFF implemented by us on LTSPICE

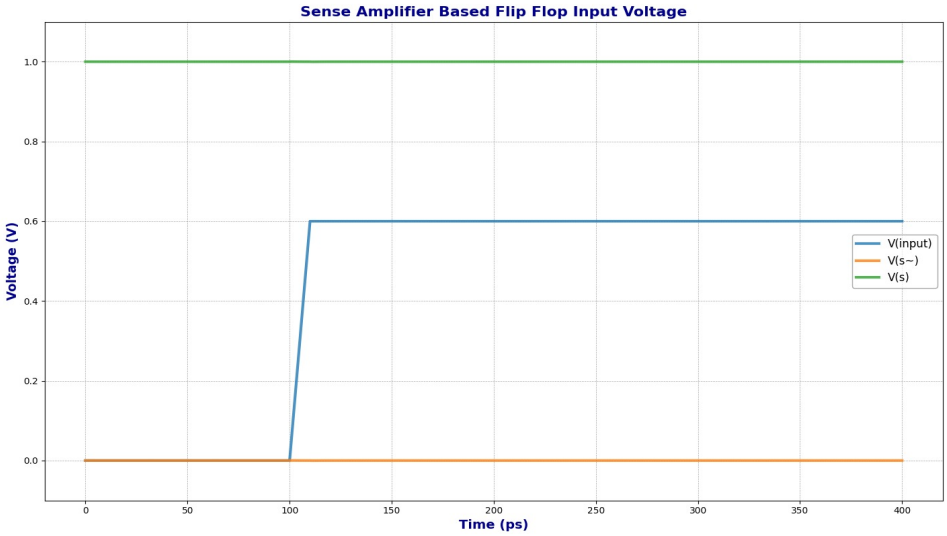

FIGURE 17 – SAFF Output

Carry-Skip Adder : Equations and Explanation

Introduction

A **Carry-Skip Adder (CSA)** is a type of adder used in digital circuits to perform fast binary addition. It reduces the delay caused by carry propagation by skipping over blocks of bits where the carry can pass directly. This is achieved by using **group generate (G)** and **group propagate (P)** signals. These signals determine whether a carry is generated or propagated in a particular group of bits.

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Key Concepts

— **Generate Signal** (G) : Indicates that a carry is generated in a particular bit or group of bits.
— **Propagate Signal** (P) : Indicates that a carry is propagated through a particular bit or group of bits.
— **Hierarchical Computation** : The adder breaks the bits into groups, computes local G and P signals, and then combines them hierarchically to determine the final carry.

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Equations and Explanation

Group Generate Equations

In the first step, the generate signals for smaller groups of bits are calculated :

$$G_{4:1} = G_{4:4} + P_{4:4}G_{3:1} \quad \text{(Group generate for bits 4 to 1)}$$
$$G_{3:1} = G_{3:3} + P_{3:3}G_{2:1} \quad \text{(Group generate for bits 3 to 1)}$$
$$G_{2:1} = G_{2:2} + P_{2:2}G_{1:1} \quad \text{(Group generate for bits 2 to 1)}$$

Here, $G_{i:j}$ represents the carry generated in the bit range i to j, while $P_{i:j}$ indicates the carry propagation.

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Group Generate Equations

Bits 8 to 5 :

$$G_{8:5} = G_{9:8} + P_{8:8}G_{7:5} \quad \text{(Group generate for bits 8 to 5)}$$
$$G_{7:5} = G_{7:7} + P_{7:7}G_{6:5} \quad \text{(Group generate for bits 7 to 5)}$$
$$G_{6:5} = G_{6:6} + P_{6:6}G_{5:5} \quad \text{(Group generate for bits 6 to 5)}$$

Bits 12 to 9 :

$$G_{12:9} = G_{12:12} + P_{12:12}G_{11:9} \quad \text{(Group generate for bits 12 to 9)}$$
$$G_{11:9} = G_{11:11} + P_{11:11}G_{10:9} \quad \text{(Group generate for bits 11 to 9)}$$
$$G_{10:9} = G_{10:10} + P_{10:10}G_{9:9} \quad \text{(Group generate for bits 10 to 9)}$$

Bits 16 to 13 :

$$G_{16:13} = G_{16:16} + P_{16:16}G_{15:13} \quad \text{(Group generate for bits 16 to 13)}$$
$$G_{15:13} = G_{15:15} + P_{15:15}G_{14:13} \quad \text{(Group generate for bits 15 to 13)}$$
$$G_{14:13} = G_{14:14} + P_{14:14}G_{13:13} \quad \text{(Group generate for bits 14 to 13)}$$

Propagation Across Larger Groups

The results from smaller groups are combined to compute the carry propagation across larger groups :

$$G_{4:0} = G_{4:1} + P_{4:1}G_{0:0} \quad \text{(Propagate across bits 4 to 0)}$$
$$G_{8:0} = G_{8:5} + P_{8:5}G_{4:0} \quad \text{(Propagate across bits 8 to 0)}$$
$$G_{12:0} = G_{12:9} + P_{12:9}G_{8:0} \quad \text{(Propagate across bits 12 to 0)}$$
$$G_{16:0} = G_{16:13} + P_{16:13}G_{12:0} \quad \text{(Propagate across bits 16 to 0)}$$

These equations show how the carry propagates efficiently across the entire input range by leveraging group computations.

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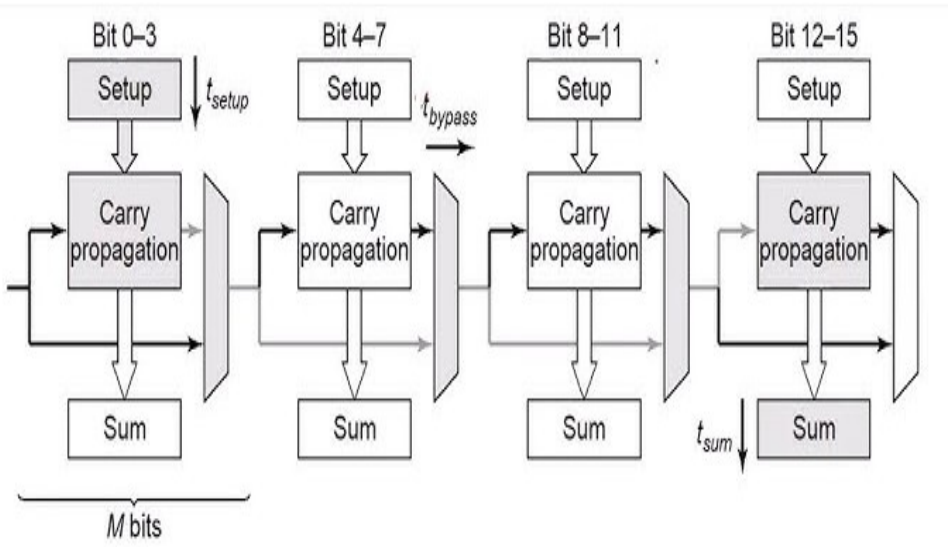

FIGURE 18 – Carry Skip adder

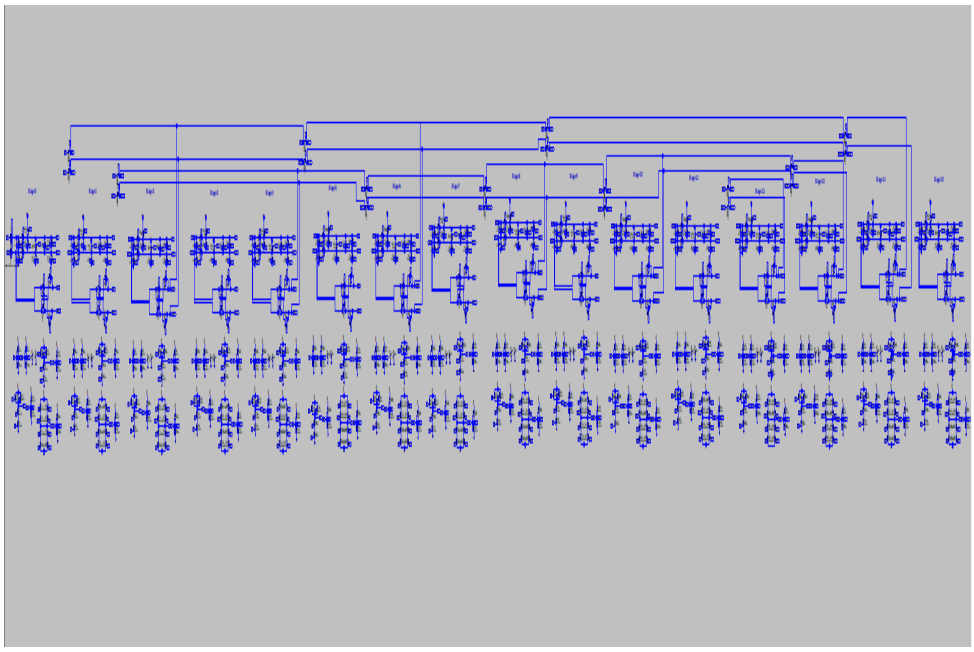

FIGURE 19 – 16-Bit Adder implementation on ltspice

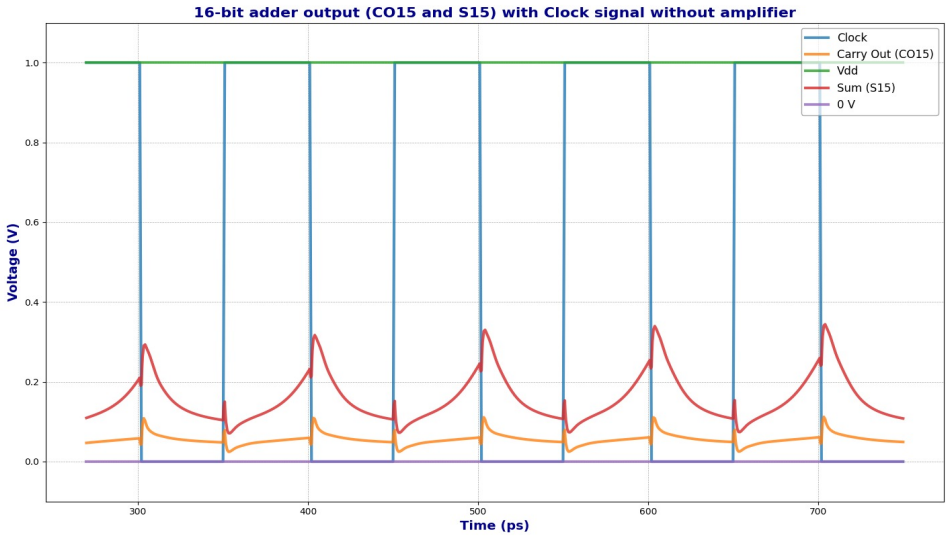

FIGURE 20 – 16 bit LVS adder output without LSA

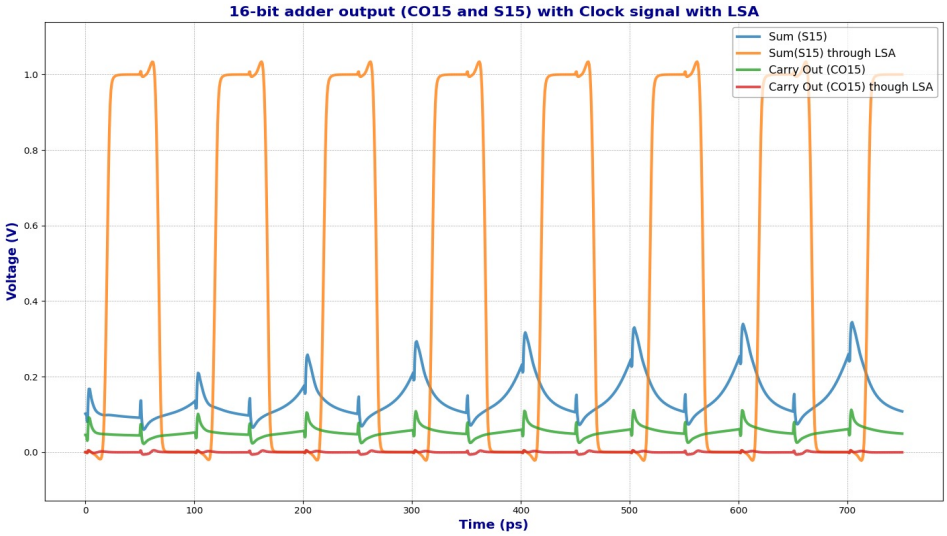

FIGURE 21 – 16 bit LVS adder output with LSA

Effect on Power Consumption and Capacitance

As technology node size decreases (e.g., from 70nm to 45nm or smaller), the sizes of transistors and parasitic capacitances associated with them also decrease. This reduction in capacitance directly affects dynamic power, as given by the equation :

$$P_{\text{dynamic}} = \alpha C V_{\text{dd}}^2 f \tag{1}$$

where :

- α is the activity factor, representing the average switching frequency,
- C is the capacitance of the circuit,
- V_{dd} is the supply voltage,
- f is the clock frequency.

Since capacitance C is reduced in smaller nodes, the energy required to charge and discharge nodes with each transition decreases. Thus, for the same α, circuits in smaller technology nodes consume less dynamic power due to lower capacitance.

Operating Voltage (V_{dd})

As technology scales down, operating voltages V_{dd} also tend to decrease to prevent excessive electric fields that can damage smaller transistors. Since dynamic power scales with V_{dd}^2, lower supply voltage

Conclusion

We successfully demonstrate the use of the Low Voltage Swing (LVS) technique to design a high-speed, low-power 32-bit adder optimized for deep sub-micron (DSM) technology. By leveraging the LVS method, we achieve significant improvements in both speed and energy efficiency. The designed adder operates at a clock frequency of 10 GHz and

exhibits a remarkably low power dissipation of 2.58 mW per GHz, making it suitable for integration into modern processors.

Through simulations and optimization, we show that smaller technology nodes, such as 70nm, enhance performance and reduce power requirements compared to older 100nm technology. We also validate the efficiency of Latched Sense Amplifiers (LSA), which provide better signal amplification while consuming less power than alternative designs. The 32-bit adder is built using a carry-select structure, which reduces delays by processing carry operations in parallel, further enhancing its suitability for high-speed applications.

Références

[1] F. Kashfi and Others, "Implementation of a high-speed low-power 32-bit adder in 70nm technology," in *Proceedings of the IEEE International Conference on VLSI Design*, 2006. [Online]. Available : https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1692509

[2] D. J. Deleganes, M. Barany, G. Geannopoulos, K. Kreitzer, A. P. Singh, and S. Wijeratne, "Low-voltage-swing logic circuits for a 7ghz x86 integer core," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, 2004. [Online]. Available : https://sci-hub.se/10.1109/isscc.2004.1332640

[1] [2]