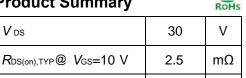
Features

- Enhancement mode
- Very low on-resistance RDS(on) @ VGS=4.5 V
- Fast Switching
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



ID

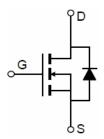


120

Α



TO-252-2L top view



Schematic diagram

Maximum ratings, at TA =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
V _{(BR)DSS}	Drain-Source breakdown voltage		30	V
I _s	Diode continuous forward current $T_{\rm C}$ =25°C		120	Α
	Continuous drain current@VGS=10V	T _C =25°C	120	А
I _D		T _C =100°C	80	А
I _{DM}	Pulse drain current tested ①	T _C =25°C	480	А
EAS	Avalanche energy, single pulsed ②		100	mJ
P_{D}	Maximum power dissipation $T_C = 25^{\circ}C$		45	W
Vgs	Gate-Source voltage		±20	V
$T_{STG}T_{J}$	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.4	°C/W	
$R_{_{ heta JA}}$	Thermal Resistance Junction-Ambient	62	°C/W	



Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V ID=250µA	30			V
	Zero Gate Voltage Drain Current	VDS=24V,VGS=0V			1	μΑ
DSS	Zero Gate Voltage Drain Current(Tj=85°C	VDS=24V,VGS=0V			30	μΑ
l _{GSS}	Gate-Body Leakage Current	VGS=±20V,VDS=0V			±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	Vps=Vgs,Ip=250µA	1.0	1.5	2.5	٧
R _{DS(ON)}	Drain-Source On-State Resistance③	Vgs=10V, ID=30A		2.5	3.5	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance③	Vgs=4.5V, ID=30A		3.9	4.5	mΩ
	Electrical Characteristics @ T _j = 25°C	unless otherwise	stated)	•		
C _{iss}	Input Capacitance			2921		pF
C _{oss}	Output Capacitance	VDS=15V,VGS=0V, f=1MHz		440		pF
C _{rss}	Reverse Transfer Capacitance	1-11/11/2		416		pF
R_g	Gate Resistance	f=1MHz		1.2		Ω
Q_{α}	Total Gate Charge			63		nC
Q _{gs}	Gate-Source Charge	Vps=15V,lp=20A, Vgs=10V		13		nC
Q_{gd}	Gate-Drain Charge	_ V00=10 V		16		nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time			14		nS
t _r	Turn-on Rise Time	VDD=20V, ID=20A,		18		nS
t _{d(off)}	Turn-Off Delay Time	Rg=3Ω,		99		nS
t _f	Turn-Off Fall Time	VGS=10V		45		nS
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	IsD=20A,Vgs=0V		0.79	1.2	V
t _{rr}	Reverse Recovery Time	Tj=25 °C ,Isd=20A,		32		nS
Q _{rr}	Reverse Recovery Charge	VGS=0V di/dt=100A/µs		31		nC
	1	J	ı			

NOTE:

 $[\]ensuremath{\textcircled{1}}$ Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax} , starting $T_J = 25^{\circ}C$, L = 0.5 mH, $R_G = 25\Omega$, $I_{AS} = 20A$, $V_{GS} = 10V$. Part not recommended for use above this value

③ Pulse width ≤ 300 μ s; duty cycle≤ 2%.



Typical Characteristics

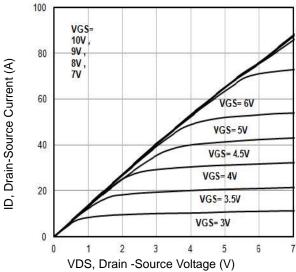


Fig1. Typical Output Characteristics

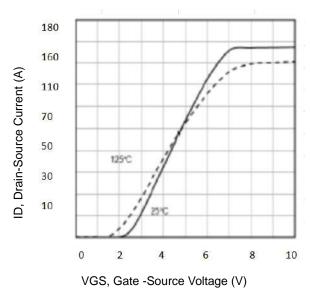


Fig3. Typical Transfer Characteristics

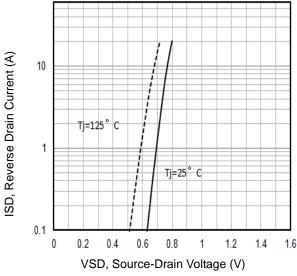


Fig5. Typical Source-Drain Diode Forward Voltage

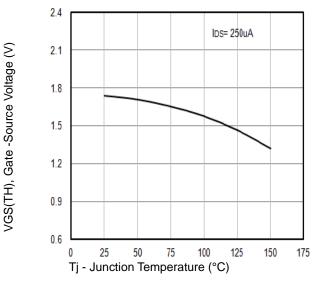


Fig2. $V_{GS(TH)}$ Galle,-Source Voltage at $U_{GS(TH)}$ Galle,

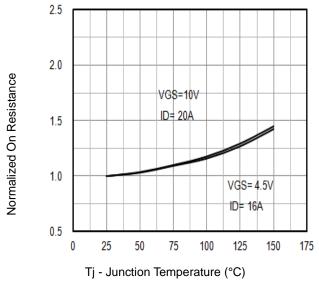


Fig4. Normalized On-Resistance Vs. Tj

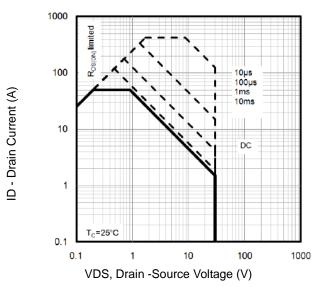


Fig6. Maximum Safe Operating Area



Typical Characteristics

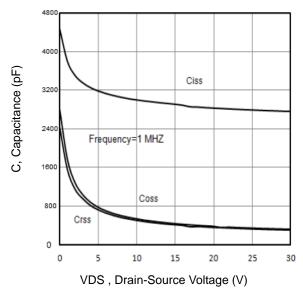


Fig7. Typical Capacitance Vs.Drain-Source Voltage

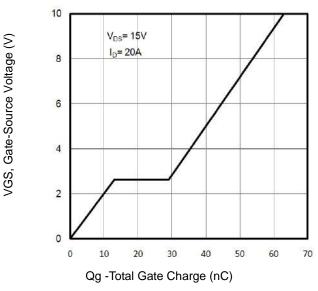
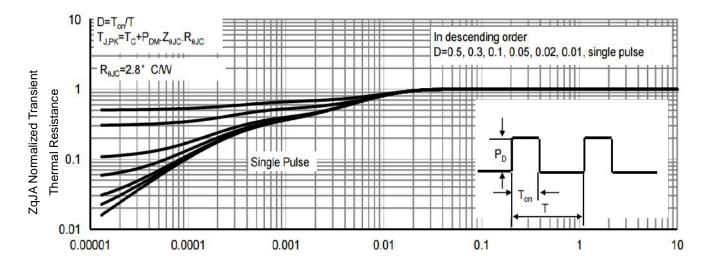


Fig8. Typical Gate Charge Vs.Gate-Source Voltage



Pulse Width (s)

Fig9. Normalized Maximum Transient Thermal Impedance

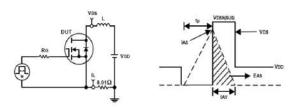


Fig10. Unclamped Inductive Test Circuit and waveforms

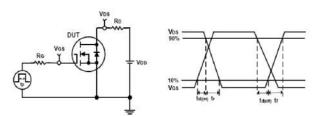


Fig11. Switching Time Test Circuit and waveforms



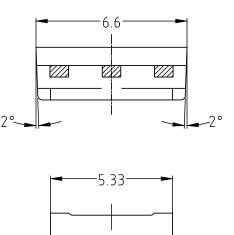


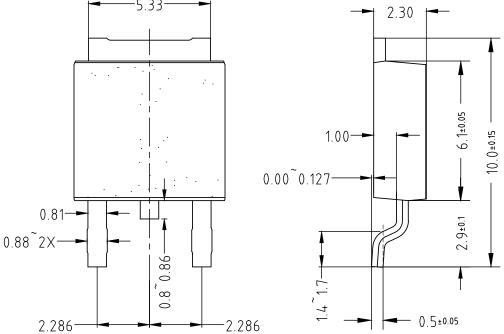
Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30N120KQ-R	30N120	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	AS 30N120 □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□

TO-252







ASDM30N120KQ

30V N-Channel MOSFET

IMPORTANT NOTICE

Xi'an Ascend Semiconductor incorporated MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Xi'an Ascend Semiconductor Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Xi'an Ascend Semiconductor Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Xi'an Ascend Semiconductor Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume.

all risks of such use and will agree to hold Ascendsemi Incorporated and all the companies whose products are represented on Xi'an Ascend Semiconductor Incorporated website, harmless against all damages.

Xi'an Ascend Semiconductor Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Xi'an Ascend Semiconductor Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Xi'an Ascend Semiconductor Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

unintended or unauthorized application.

www.ascendsemi.com

NOV 2018 Version1.0 7/7 Ascend Semicondutor Co.,Ltd