8-bit Timer Module

Document Information:
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Revision: 0.2
Modify date: 11 November 2018

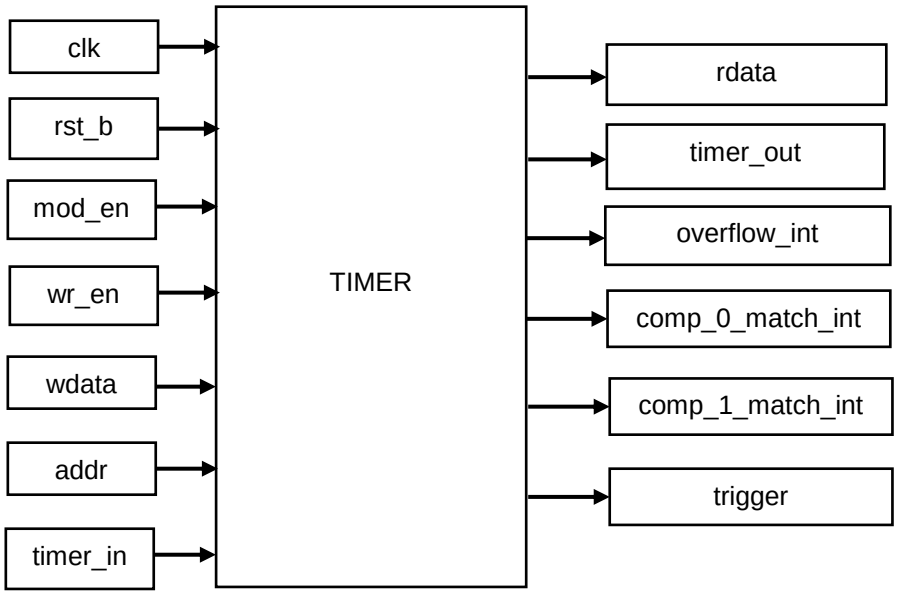
1. Introduction

The 8-bit timer is a general purpose simplified counter module, it includes a bidirectional counter, an interruption generation block, input pulse or external clock mode count mode, provides a method to generate a PWM signal and a trigger signal generated according timer events.

2. Overview

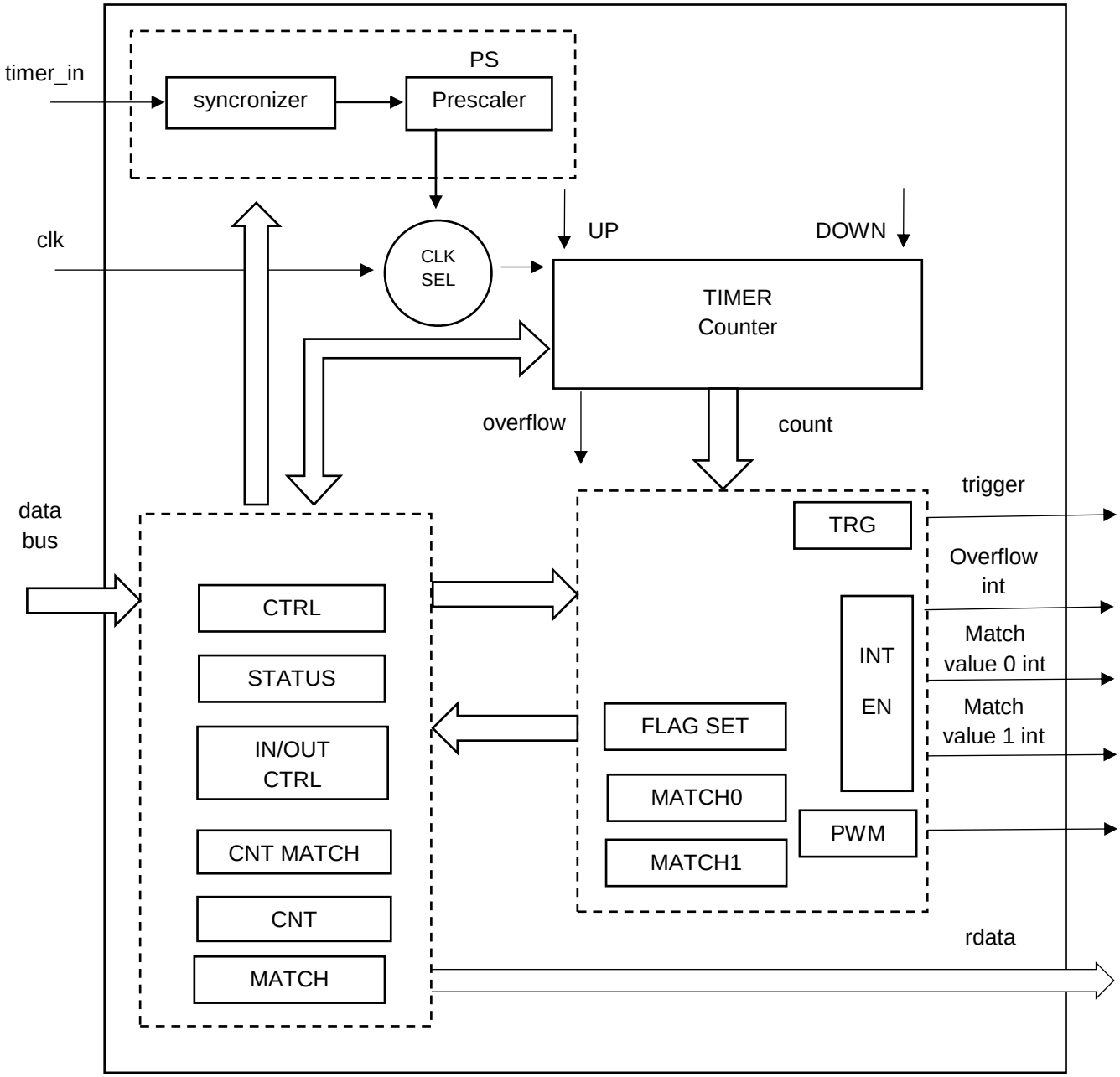
The counter has 2 operation modes, normal and inverse counter modes with initial value configuration register and match value registers can be easily adjusted to generate interruption signals periodically.
PWM can be generated using Match count 0 and Match count 1 timer events, trigger signal can be triggered according same events to produce a 1 cycle pulse, it can be used to start some other block actions as ADC conversions or UART transmissions.

3. Pin diagram



Timer has an interface for register access and the clock and reset inputs, it also has the timer_in that can be connected to a pulse input pad or to an external clock signal.
Output interface includes the read data (rdata) providing register access read value, 3 interruption signals, timer_out is the PWM signal output and trigger is shared between the 3 events: overflow, match 0, match 1.

4. **Block diagram**



4.1 Counter

Counter is bidirectional, Up or Down mode, it supports free running counting mode and restricted MIN to MAX count modes.

4.2 Input block

Includes edge detectors and prescaler components.

4.2.1 Prescaler

Prescaler can divide the input frequency by 2,4,8,16,32,64,128 factor

4.2.2 Synchronizer

Takes input signal and passes it by two flip flops to synchronize with Timer clock.

4.3 Output block

Includes interruption/flag, PWM, trigger generation.

4.4 Registers block

Internal register block contains all the register fields in the same component.

5. Features

5.1 Prescaler

An external clock signal can be divided by half factors to get longer times.

5.2 Input pulse counter

An input signal rising or falling edge can be used to increment or decrement the counter.

5.3 External clock support

External clock signal can be connected to timer_in input and can be used to increment/decrement the counter, the frequency can be divided according the prescaler.

5.4 Interruption generation

Interruptions can be generated for the next timer events:

5.4.1 Overflow

Interruption signal can be generated using the control register configuration OVF_EN enable bit, every time there is a transition from max value (Actually 0xFF) to minimal counter value, 0x0 if CNT_INIT register not configured otherwise the value configured at CNT_INIT.

5.4.2 Match 0,1 interruption

Interruption signals are generated using the control register configuration CTN_M1_EN and CTN_M2_EN enable bits, every match between counter actual value and Match value configured in registers CNT_M1 and CNT_M2 triggers the respective interruption signal.

5.5 Counter Initialization

The counter initial value is 0 by default but it can be replaced for a user defined value writing at CNT_INT register

5.6 Counter inverse mode

Counter direction is defined by control register CTRL configuration bit MODE, default mode is up count mode MODE=0 if this bit is set MODE=1 the count direction will be reversed. This configuration is expected to be done during no operation mode, control register bit is with default value START=0.

5.7 Trigger generation

Counter generates a trigger signal according overflow or match 0/1 event, depending which is selected.

6. Signal description

Below tables show the input and output signals

6.1 Input signals

Name	Size (bits)	Description	Notes
clk	1	Clock input	
rst_b	1	reset	Active low
addr	6	register address	
mod_en	1	module is selected for register access	Active High
wr_en	1	1: module access for writing 0: module access for reading	
timer_in	1	External clock or pulse input	
wdata	8	register write data	

Table 1

6.2 Output signals

Name	Size (bits)	Description	Notes
rdata	8	Clock input	
overflow_int	1	Timer overflow event interruption	Active High
comp_0_match_int	1	Timer comparator 0 match event interruption	Active High
comp_1_match_int	1	Timer comparator 1 match event interruption	Active High
timer_out	1	PWM output	
trigger	1	Trigger output	

Table 2

7. Memory map and register definition

7.1 Register summary

Timer module has 6 configuration registers listed in the table below

Offset	Register name	Description	Width (bits)	Access	Reset value
0x0	CTRL	Timer enable/configuration	8	R/W	0
0x1	CTRL_IN	Control input	8	R/W	0
0x2	CTRL_OUT	Control output	8	R/W	0
0x4	STATUS	Timer status	8	R/W	0
0x8	CNT_INIT	Timer initialization	8	R/W	0
0x9	CNT_MIN	Counter min	8	R/W	0
0xA	CNT_MAX	Counter max	8	R/W	0
0xB	CNT	Actual counter value	8	RO	0
0xC	CNT_M1	Counter match value 0	8	R/W	0
0xD	CNT_M2	Counter match value 1	8	R/W	0

7.2 Register description

7.2.1 Control register CTRL

Control register configures main features as operation mode, clock source and has the start bit to enable counter operation.

Diagram

Bits	7	6	5	4	3	2	1	0
R	FREE	M1_INT	M0_INT	OVF_INT	CLK_SEL		CNT MODE	START
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
START	Starts counter operation, set this bit after configuration
FREE	• 0 Non-free run count mode, it considers MAX MIN values • 1 Force free run count, don't apply MAX MIN configuration

CNT MODE	• 0 Count up • 1 Count down
CLK_SEL	• 0 System clock • 1 External clock
M0_INT	Enables interruption for match between counter register CNT value with counter match 0 register value: M0F
M1_INT	Enables interruption for match between counter register CNT value with counter match 1 register value: M1F
OVF_INT	Enables interruption for match between counter register CNT value with max counter register value 0xFF: STATUS OVF

7.2.2 Control register input CTRL_IN

Diagram

Bits	7	6	5	4	3	2	1	0
R		PS						IN_EDGE
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
IN_EDGE	Select between positive or negative edge to trigger counter when input counter mode is selected • 0 Positive edge • 1 Negative edge
PS	Prescaler factor value for external clock 000 - Divide by 1 001 - Divide by 2 010 - Divide by 4 011 - Divide by 8 100 - Divide by 16 101 - Divide by 32 110 - Divide by 64 111 - Divide by 128

7.2.3 Control register output CTRL_OUT

Diagram

Bits	7	6	5	4	3	2	1	0
R		M1 TRG	M0 TRG	OVF TRG			INV	PWM
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
PWM	Output pin timer_out toggles according counter MIN and MAX value, when there is a match of MIN value and counter CNT value output is set, when there is a match of MAX value and CNT value output is cleared. • 0 PWM generation disabled • 1 PWM generation enabled
INV	Invert output • Output is not inverted • Output is inverted
OVF TRG	Overflow trigger When enabled a pulse is generated when there is a counter overflow
M0 TRG	Match 0 output trigger When enabled a pulse is generated when there is a counter match 0 event
M1 TRG	Match 1 output trigger When enabled a pulse is generated when there is a counter match 1 event

7.2.4 Status register STATUS

Status register shows flags for counter match values and overflow events

Diagram

Bits	7	6	5	4	3	2	1	0
R						M1F	M0F	OVF
W1C*								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
OVF	Overflow Flag • 1 Counter overflow since the last time this bit has been cleared • 0 Counter overflow has not occurred since last time this bit cleared About Clearing this flag: Writing 1 to this position clears the flag and the interruption signals is consequently disabled Writing 0 to this position does nothing
M0F	Match Counter 0 Flag • 1 Counter value has matched with CTN_M0 register value since last time this bit has been cleared • 0 Counter value did not match or matches with CTN_M0 register value since last time this bit has been cleared About Clearing this flag: Writing 1 to this position clears the flag and the interruption signals is consequently disabled Writing 0 to this position does nothing
M1F	Match Counter 1 Flag • 1 Counter value has matched with CTN_M1 register value since last time this bit has been cleared • 0 Counter value did not match or matches with CTN_M1 register value since last time this bit has been cleared About Clearing this flag: Writing 1 to this position clears the flag and the interruption signals is consequently disabled Writing 0 to this position does nothing

* **W1C:** Write 1 to clear

7.2.5 Counter initialization register CNT_INIT

Counter initial value can be initialized using this register

Diagram

Bits	7	6	5	4	3	2	1	0
R	INIT_VAL							

W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
INIT_VAL	Initial Value This value defines the initial value for counter operation

7.2.6 Counter minimal value register CNT_MIN

Counter value minimal count value register

Diagram

Bits	7	6	5	4	3	2	1	0
R	MIN_VAL							
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
MIN_VAL	Minimal Value When max value is reached counter returns to this value when non-free running mode is selected

7.2.7 Counter maximum value register CTN_MAX

Counter value maximum count value register

Diagram

Bits	7	6	5	4	3	2	1	0
R	MAX_VAL							
W								
Reset	1	1	1	1	1	1	1	1

Fields

Field	Function
MAX_VAL	Maximum Value Counter goes up until this value is reached when non-free running mode is selected

7.2.8 Counter register CNT

Contains the actual counter count value

Diagram

Bits	7	6	5	4	3	2	1	0
R	CNT_VAL							
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
CNT_VAL	Counter Value The actual timer's counter value **Note**: This register can only be read, it is not possible to modify this value

7.2.9 Counter Match 0 CNT_M0

Contains the match value 0

Diagram

Bits	7	6	5	4	3	2	1	0
R	CNT_MATCH							
W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
CNT_MATCH	Counter match value 0 This value is used to compare with counter value and set M0F flag in STATUS register and the corresponding interruption signal when enabled interruption generation.

7.2.10 Counter Match 1 CNT_M1

Contains the match value 1

Diagram

Bits	7	6	5	4	3	2	1	0
R	CNT_MATCH							

W								
Reset	0	0	0	0	0	0	0	0

Fields

Field	Function
CNT_MATCH	Counter match value 1 This value is used to compare with counter value and set M1F flag in STATUS register and the corresponding interruption signal when enabled interruption generation.

8. Functional description

Timer can be configured for the next operation modes

8.1 Free counter mode

Timer counts from 0x0 to 0xFF and starts again indefinitely

8.2 Normal count mode

Timer is configured with an initial count value and a top count maximum value, count starts from this initial value and runs up until maximum value is reached, when maximum value is reached count starts again.

8.3 Inverse count mode

Timer is configured in the same way as normal count mode, but the count starts from maximum value and continues counting down until reaches minimum value, when minimum value is reached count starts again.

Note: when maximum value is not configured (0x0) the maximum value is 0xFF

8.4 Input edge counter mode

Timer counts according input pin pulses, negated edge or positive edge trigger can be selected according control register 2.

8.5 Prescaler for external clock

8.6 PWM generation

8.7 Trigger generation

A trigger signal is generated based in the timer events, overflow and counter match value events can be configured to generate a trigger signal.

9. Initialization & Configuration

9.1 Free run operation

- Write to the Count match 0 and Count match 1 registers according desired match values
- Set the Control register bits M0_INT, M1_INT and OVF_INT if required
- Set the Control register bit START bit

Counter starts running until reach max value 0xFF then starts again.

9.2 Normal count operation

- Write to the count match 0 and count match 1 registers according desired match values
- Write to counter initialization register and counter max value register according expected values.
- Set the control register bits M0_INT, M1_INT and OVF_INT if required
- Set the control register bit START bit

9.3 Inverse count operation

- Write to the Count match 0 and Count match 1 registers according desired match values
- Write to counter initialization register and counter max value register according expected values.
- Set the control register bits M0_INT, M1_INT and OVF_INT if required
- Set the control register bit MODE
- Set the control register bit START bit

9.4 Interruptions

9.4.1 Overflow interruption

Overflow interruption is generated when STATUS register OVF flag is set and the OVF_INT bit is set in Control register.

9.4.2 Counter match 0 interruption

Counter match 0 interruption is generated when STATUS register M0F flag is set and the Control register CTRL bit M0F_INT is enabled.

9.4.3 Counter match 1 interruption

Counter match 1 interruption is generated when STATUS register M0F flag is set and the Control register CTRL bit M1F_INT is enabled.

10. Counter/Event time diagrams

10.1 Free run count mode

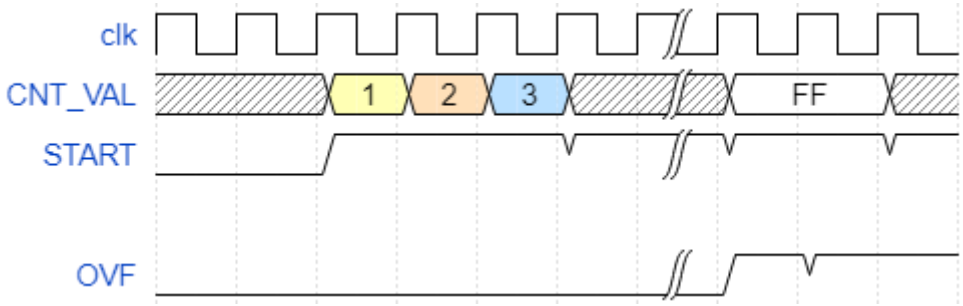
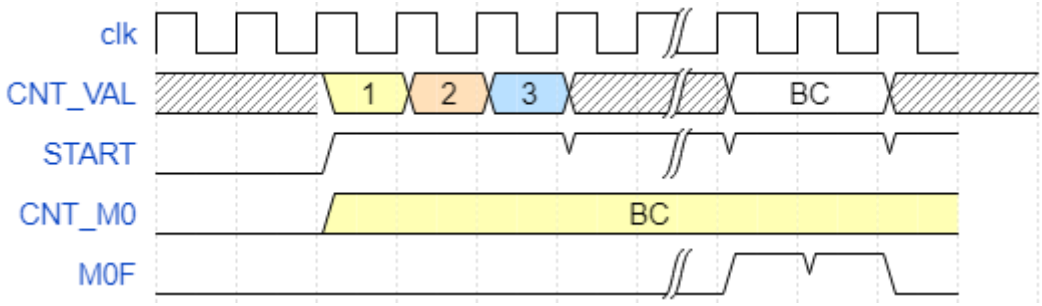
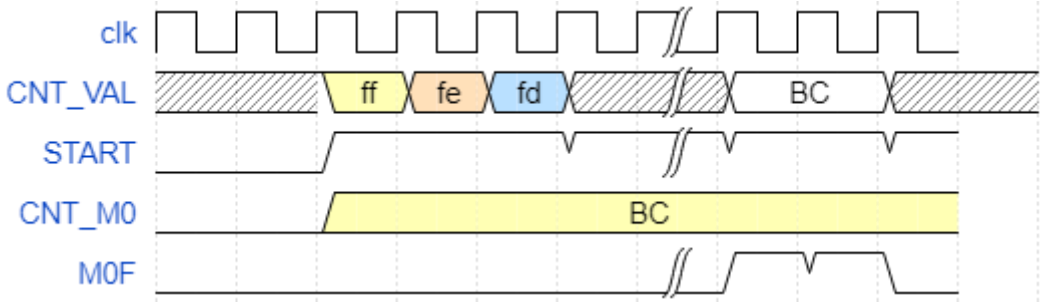


Figure 1

10.2 Normal count mode



10.3 Reverse count mode



11. Additional

11.1 Folders organization

11.1.1 Host

This design files can be accessed/copied from https://github.com/joselcuevam/timer

11.1.2 Structure

Files are organized according the next parts

11.1.2.1 RTL

Contains all design data files, top design RTL and sub components.

11.1.2.2 TESTBENCH

Contains testbench related files, includes top testbench instantiation, test components as macros, modules, tasks etc.

11.1.2.3 doc

Includes this file and additional documents

11.1.2.4 make

Includes scripts for compilation, elaboration and simulation.

11.1.2.5 tool_data

Include files used by tools.

11.2 Simulation time diagrams

11.2.1 Free run mode starting

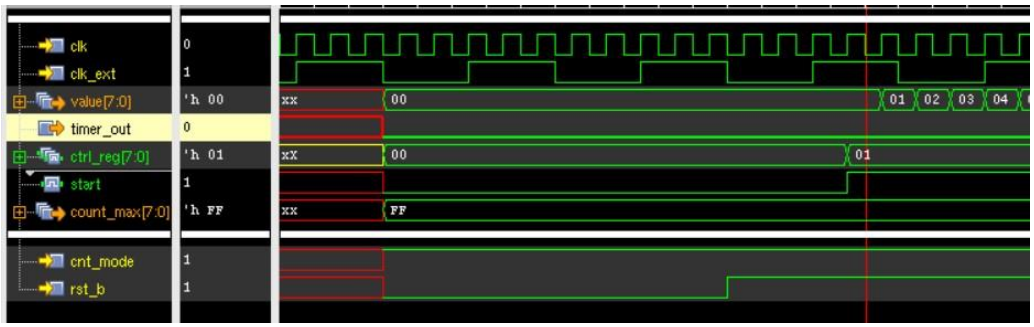


Figure 2 free run mode starting

11.2.2 Free run mode overflow

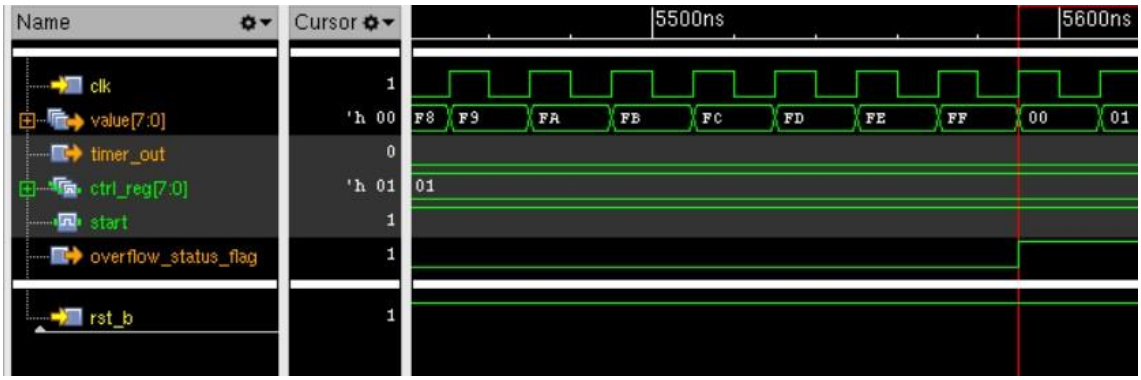


Figure 3 timer free run mode overflow

11.2.3 Free run mode (down count mode) starting

For this mode configure first CNT_INIT = FF then the CNT_MODE bit before setting START bit.

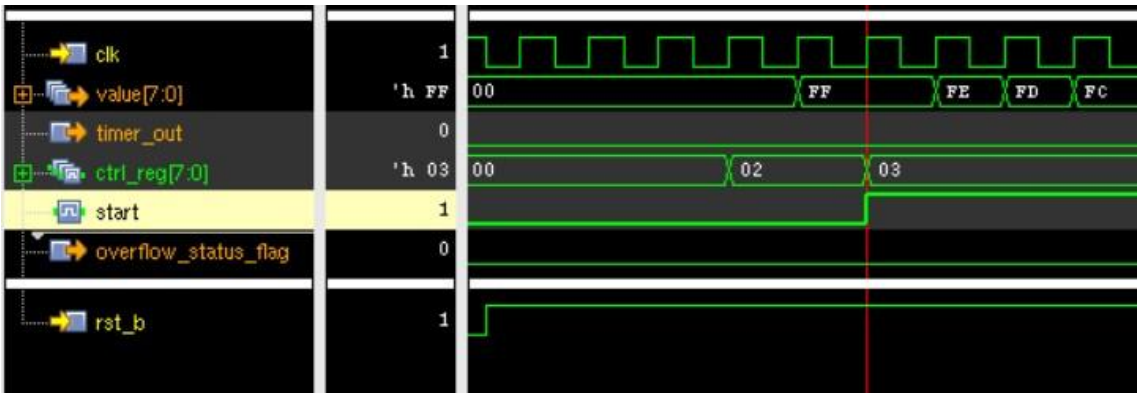


Figure 4 free run, down count mode starting

11.2.4 Free run mode (down count mode) overflow

For this mode configure first CNT_INIT == FF value then the CNT_MODE bit before setting START bit.

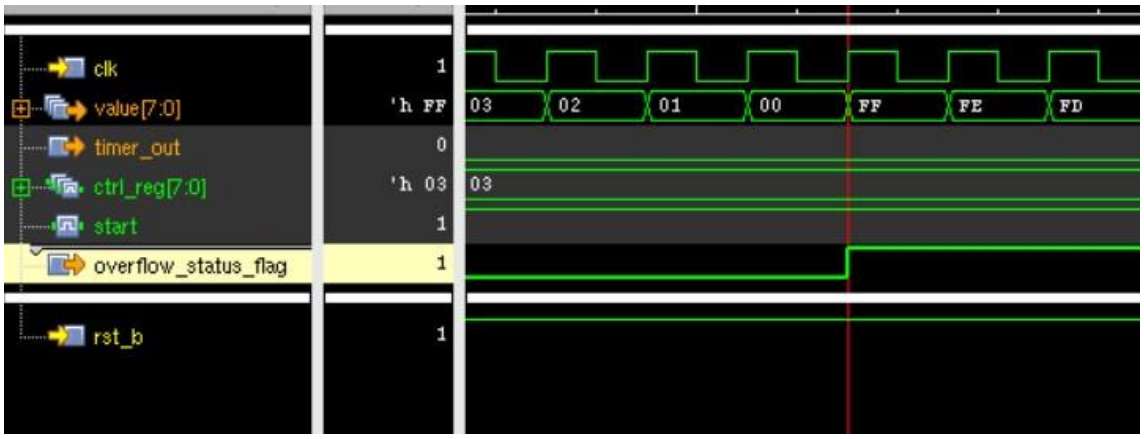


Figure 5 free run, down count mode overflow

11.2.5 Up count mode starting

MAX and MIN count values have been configured before starting counter

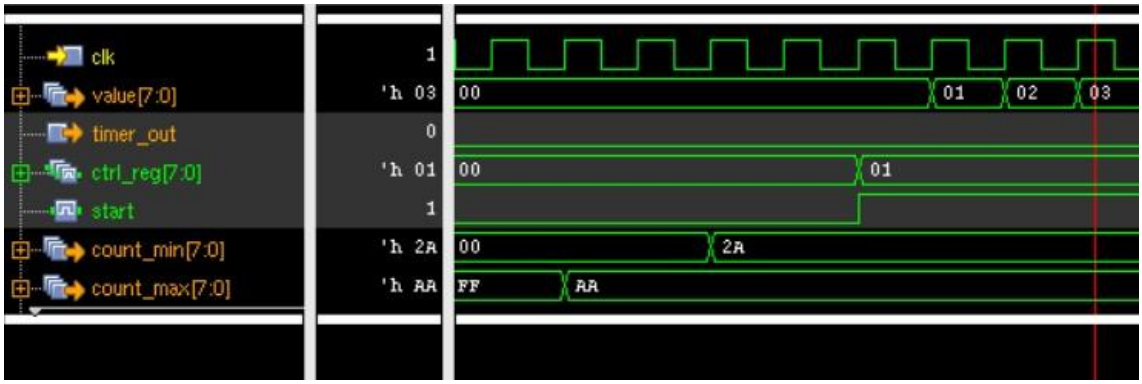
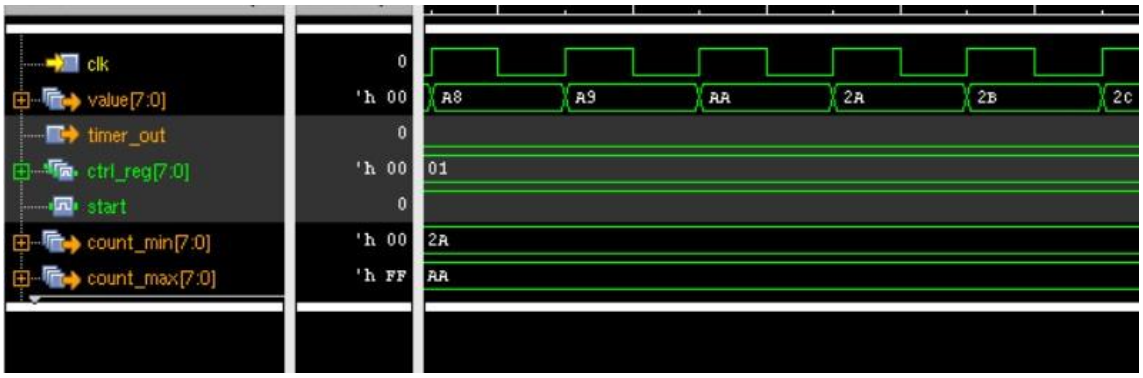


Figure 6 Up count starting

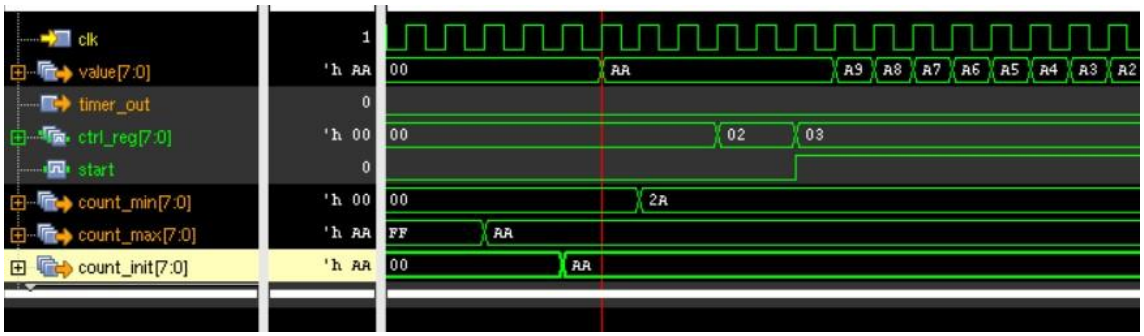
11.2.6 Up count mode returns

When MAX value is reached counter returns to MIN value



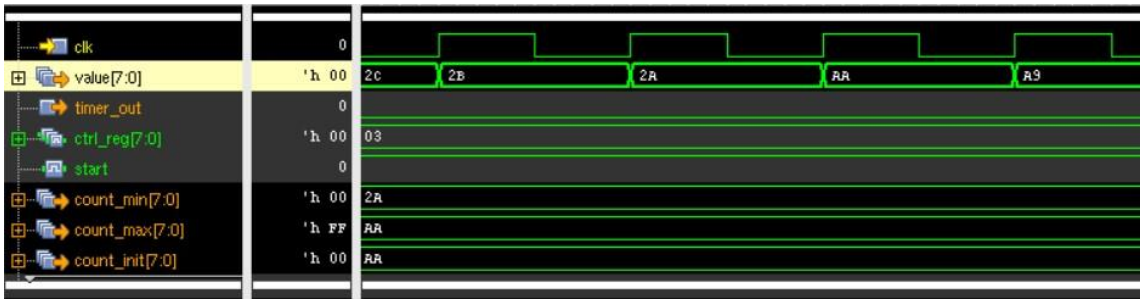
11.2.7 Down count mode starting

MAX and MIN values are configured, and initial value is set same as MAX value to avoid the counter starting with initial value of zero.



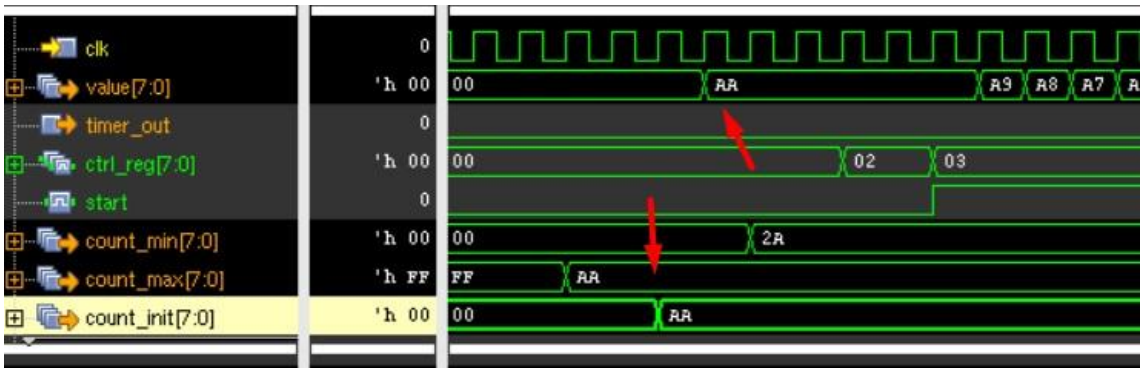
11.2.8 Down count mode returns

Counter Wraps from MIN to MAX value and count is restarted



11.2.9 Counter value initialization

Counter initial value is set according user needs with the CNT_IN register, by default initial count value is zero.



11.2.10 Input pulses counter

In this mode counter increases according pulses in the input pin, max value it can go is 10.

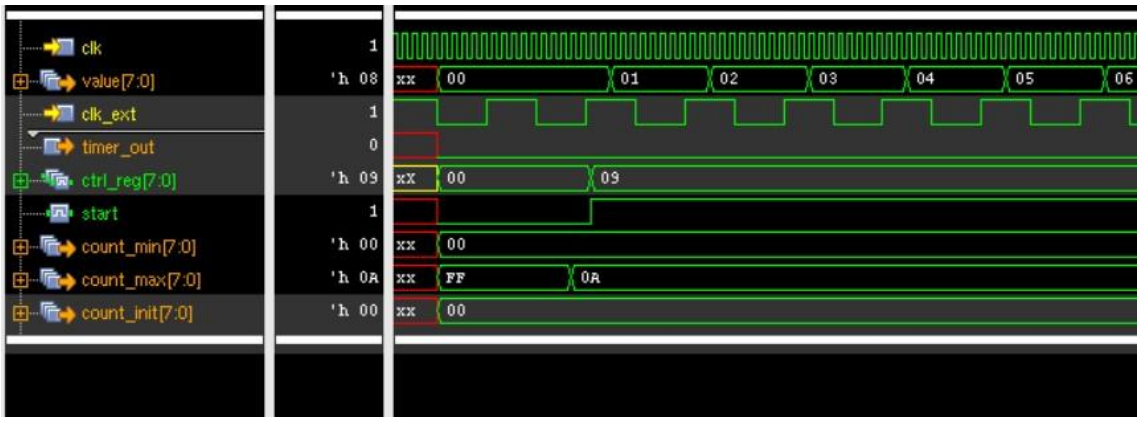


Figure 7counter triggered by input pulses

11.2.11 PWM generation

Matching CNT_M0 and CNT_M1 toggles output generating the PWM waveform, match 0 event sets output and match 1 events clears output signals.

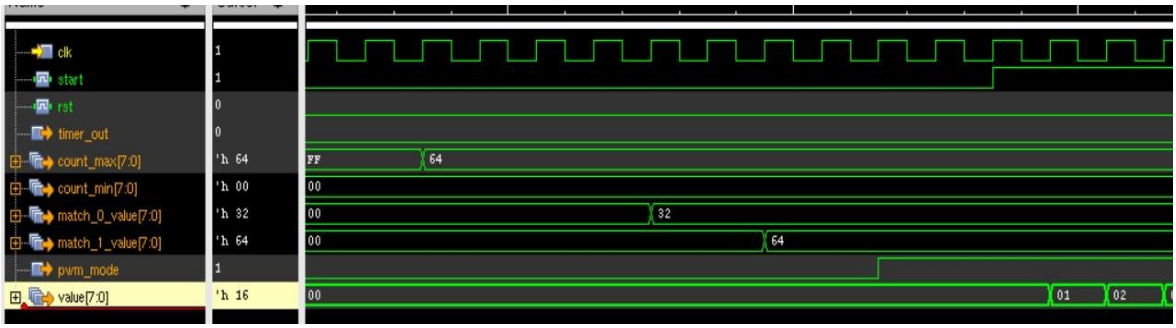


Figure 8 Register values configured according

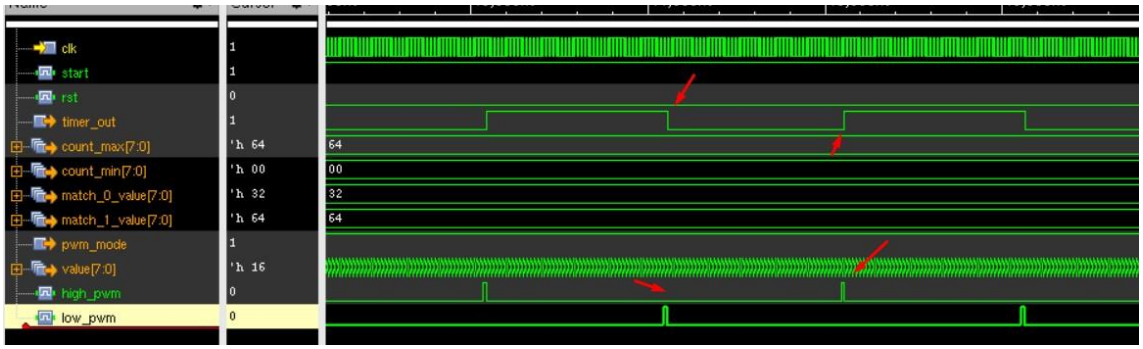


Figure 9 timer out is set/clear according matches

11.2.12 Counter match flags

The next graphic sow the time diagram Flags are set

Figure 10 Match 0 sets flag

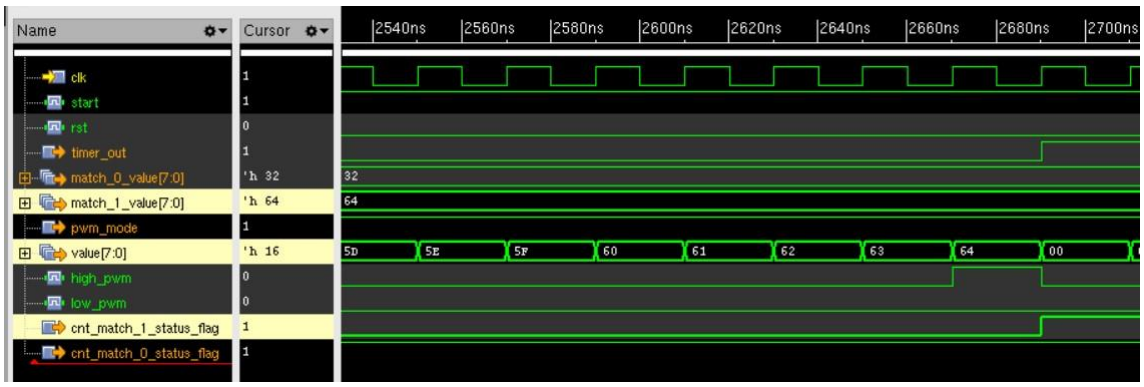


Figure 11 Match 1 sets flag

11.2.13 Interruption generation

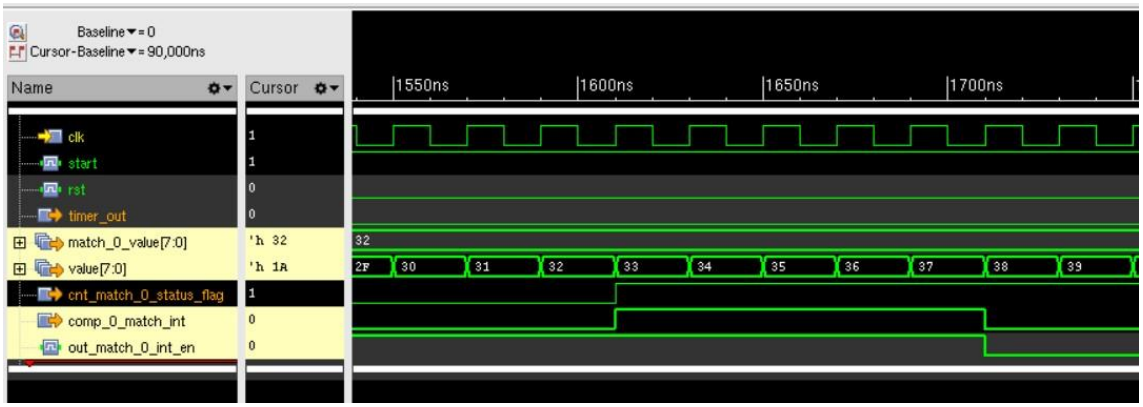


Figure 12 Match value interruption

11.2.14 Overflow interruption

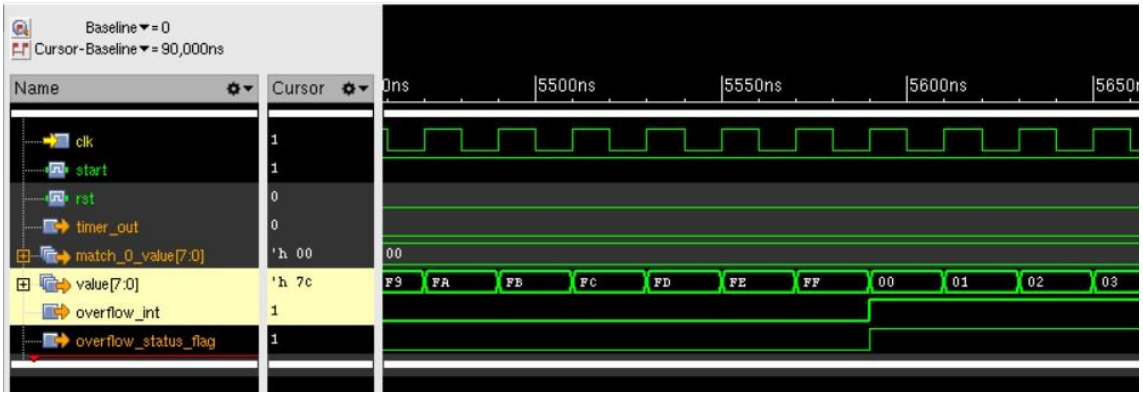
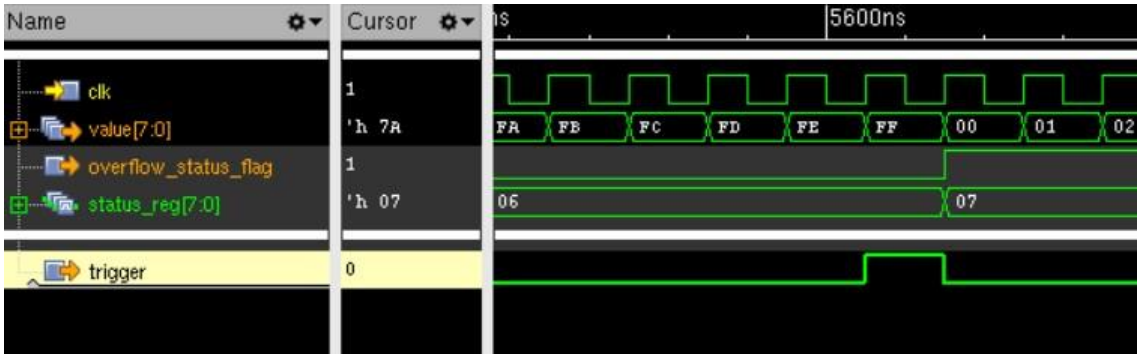


Figure 13 Overflow interruption

11.2.15 Input Prescaler

Figure 14 Prescaler enabled with PS=3

11.2.16 Trigger generation free run mode overflow



11.2.17 Trigger generation match counter