|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Operation | MemRead | MemWrite | RegWrite | ALUControl | MemToReg | RegDst | ALUSRC |
| Lw 00 | 1 | 0 | 1 | 01 | 1 | 0 | 1 |
| Sw 01 | 0 | 1 | 0 | 01 | 0 | 0 | 1 |
| Add 11 | 0 | 0 | 1 | 01 | 0 | 1 | 0 |
| Addi 10 | 0 | 0 | 1 | 01 | 0 | 0 | 1 |