How to develop IBIS model

INTRODUCTION

IBIS-model (I/O Buffer Information Specification) used for signal integrity analysis and crosstalk into the digital circuit boards. This specification describes the EIA and ANSI standards (656-A) and is supported by most manufacturers of integrated circuits, supplying to the market the IBIS-models of their products. On the other hand, this format is supported by almost all the design and modeling systems. So, what is the IBIS format? This is the format of the external electronic device description as a "black box" without regard to its internal structure and functioning. Simplistically, this format can be regarded as an attempt to present an integrated circuit in the form of a resistive matrix of complex impedances. As a rule, IBIS-model parameters are obtained on the basis of knowledge of the current-voltage characteristics for different logic states the conclusions DC, parasitic shell parameters and transfer characteristics on an ideal resistive load. This approach means that to get the IBIS-model, you can either perform a series of test measurements to appropriate conditions, or by doing a full SPICE-simulation of the internal circuitry of the device.

PROBLEM

In ideal, all placed on the market electronic components must be developed by the manufacturer IBIS-model. Even though the available libraries are extensive enough, there is always the possibility that any product (eg, new) will they be absent. In addition, the quality of available models may be insufficient.

If IBIS-model of any chip absent, than, as a rule, there is no precise and SPICE- model. Mathematical modeling in this case is impossible, so the developer is left with no choice but to sacrifice the accuracy or build their own IBIS-model based on physical measurements. In the latter case, it will be able to receive the correct model of the specific device.

Although the theory behind the physical measurements required for IBIS-model is quite simple, its practical implementation may be considerably more difficult. Accounting for parasitic effects, the chip configuration to produce the correct state on the findings, the precise definition of high-speed transmission characteristics and data, changing in the course of its operation, can be very difficult, if not impossible.

Imagine that we want to develop a model of an imaginary IBIS- chip packaged in a PGA package with 200-pin, which is fine for most modern microcontrollers. The device has a pair of multi-bit data bus tri-state

address and control bus, and more. Consider a step by step process of creating IBIS- model.

DEFINING OUTPUT TYPES

It is necessary to measure only one terminal of each I / O type (for example, the driver 20 mA bidirectional output CMOS receiver). To do this, refer to the documentation relevant information and findings of the group I / O type. Even if it is not always possible, it is hoped that the behavior of the different conclusions one bus will be identical. We assume that we have managed to reduce the pin count to ten types for our case.

SETTING THE DESIRED STATE CONCLUSIONS

Let's start to build a model with DATA0 type pins. From the documents we know that they are bi-directional 3.3-V CMOS drivers. The first dimension, which we will carry out - is the removal of the current-voltage characteristics of the output in different logical states (LOW, HIGH, HIGHZ) in the range of operating voltages, for example, from -1 to +4.3 V. The first problem that we face, is how to ensure the desired logic state output?

If need be construct a circuit, it can be quite difficult, expensive and may require additional time for the control device we researched. If it is intended to measure several different types of chips, it might be unreasonably expensive. However, we assume that our device supports boundary-scan according to the industry standard JTAG Boundary Scan IEEE 1149.1 and allows you to control the state of its findings through the crystal is available in the serial port with an ordinary personal computer.

CONFIGURING TEST ICs

In addition to the JTAG control lines, we need to bring to analyzed device several other important signals, for example, at least one supply voltage and the ground probe. If we are going to test only one device, all these signals can be started immediately to the right conclusions. If you intend to measure several similar products (especially in BGA or SOIC package), it would be useful to produce a test board with pad and socket for connecting.

MEASUREMENT OF CURRENT-VOLTAGE CHARACTERISTICS

Having completed all preparatory operations, we can apply for the analyzed device power supply and install the DATA0 conclusions in the desired state. First, measure the current-voltage characteristics, which set the DATA0 output to a state with a low level (LOW), will begin to change the voltage on it and measure amperage simultaneously. To do this it is best to use a programmable voltage source that can properly vary the voltage and protect the chip from over- amperage. We save all the data and repeat all the measurements for

the states with a high level (HIGH) and high impedance (HIGHZ).

MEASUREMENTS AC

To generate IBIS-model measurements you must perform a series of transient characteristics. These characteristics represent a registration form driver output signal to an ideal resistive load. For standard CMOS ICs such a load is two resistors of 50 ohms to "land" on the power. And to avoid the effects of parasitic load must be connected directly to the output device.

The number of time-change points must be sufficient to obtain a correct idea of the shape of the front and rear edges. If the output has a rise time of 1ns, then counts the number of time should not be less than 10. All removed transitional characteristics should be relatively synchronizes the start time, which could be done by using the clock JTAG.

SPURIOUS OUTPUT OPTIONS

For quality IBIS-model, we need to know the parasitic capacitance and inductance of the output. Assuming that the data shown in the product documentation.

BUILDING A MODEL

Now that we have all necessary data, we can convert them to IBIS model. This in itself is not easy, and we need a special program. However, the ideal package for this problem is now on the market does not exist. The biggest challenge here is to get the corrected current-voltage characteristics necessary for the formation of the IBIS-model. Therefore, the aim of this work is to create extensions for embedded CAD Cadence Virtuoso, performs automatic generation of IBIS models for this class of devices, such as transmitters differential signaling LVDS standard.

AUTOMATIC GENERATION

To automatically generate IBIS-model used SKILL language. SKILL allows access to the tool environment and manage all components of the environment tools: manage project procedures, automatically process simulation results used to develop custom extensions.

In the language SKILL was developed a set of scripts, each script developed generates a certain portion of the data ibis-specifications (qualitative and numerical data). Launching consistently produced a set of scripts, we get a complete specification for the ibis-model of the selected device (SPICE-shaped model). To apply the tools developed by the user is required to create a transistor model of the test device, plug it into a symbol of pre-prepared test environment scheme templates and run the automatic process of modeling. The generated pattern can be used for analyzing the physical integrity of the signal in Virtuoso and any other CAD systems, such SigXplorer.

Manually creating IBIS models requires about an hour of work a qualified technician. Given that the design process itself may be of the iterative nature, the time loss can become significant. Applying the developed module, the same object can be achieved in less than a minute. This significantly reduces the likelihood of making a mistake.

CONCLUSION

Check the quality of the generated model was carried out by the example of the classical structure of the LVDS transmitter. Comparison of the simulation results in the time domain transistor circuit and generated on the basis of its IBIS model revealed their identity.

Now applying the developed module, the task generation ibis-model in less than a minute can be solved. This significantly reduces the likelihood of making a mistake. The process of creating IBIS models are fully automated, which makes it possible to use it for solving optimization problems transistor circuit.

In future use module designed to generate structures LVDS models, apply it to optimize the parameters of the transmission path as a whole.