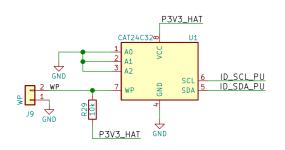
### 40-Pin HAT Connector

		× 1	40HAT P3V3	J3 P5V	2	P5V HAT
	I2C_SDA	3		P5V	4	P5V_HAT
	I2C_SCL	5	BCM2		6	GND
	12 0 0 0 0		ВСМ3	GND	8 ×	
	GND	× /	BCM4	BCM14	10 ×	
	OND		GND	BCM15	12 X	PCM_CLK
		× 11	BCM17	BCM18		GND
		× 13	BCM27	GND	14	GND
		× 15	BCM22	BCM23	16 ×	
0	P3V3_HAT	17	P3V3	BCM24	18	INT_U8
•	SPI_MOSI	19	BCM10	GND	20	GND
	SPI_MISO	21	ВСМ9	BCM25	22	INT_U9
	SPI_CLK	_ 23	BCM11	BCM8	24	SPI_CS_U8
	GND	25	GND	BCM7	26	SPI_CS_U9
	ID_SDA	27	DCM0	BCM1	28	ID_SCL
		× 29	BCM5	GND	30	GND
		×31			32	PWM0
	PWM1	33	BCM6	BCM12	34	GND
	PCM_FS	35	BCM13	GND	36 ×	
	101213	37	BCM19	BCM16	38 X	
	GND	× 37	BCM26	BCM20	38 ×	PCM_DATA
	UND	39	GND	BCM21	40	PCM_DATA

#### HAT ID-EEPROM

The HAT spec requires this EEPROM with system information to be in place in order to be called a HAT. It is set up as write protected (WP pin held high) and can be enabled for writing by placing a jumper on J9 or by bridging TP1.





# **PWM Connectors**



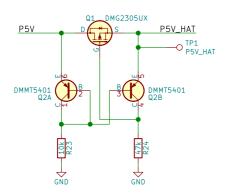
# Mounting Holes



# **5V Powered HAT Protection**

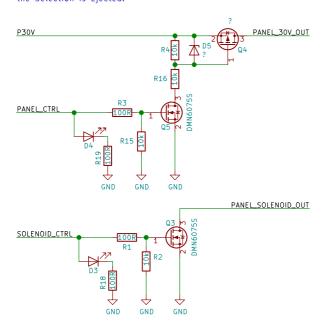
This is the recommended 5V rail protection for a HAT with power going to the Pi.

See https://github.com/raspberrypi/hats/blob/master/designguide.md
#back-powering-the-pi-via-the-j8-gpio-header



## Panel Power Switching

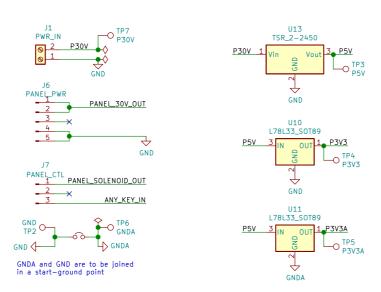
The Panel's Solenoid and Bulbs are driven from 30V. During Standby the RaspberryPi turns of the Panel via Q4. Q3 controls the Selection—Solenoid. Normally Q3 is turned on and allows a Selection on the Panel. When Q3 is turned off for a brief Moment, the Selection is Ejected.



**Audio DAC** 

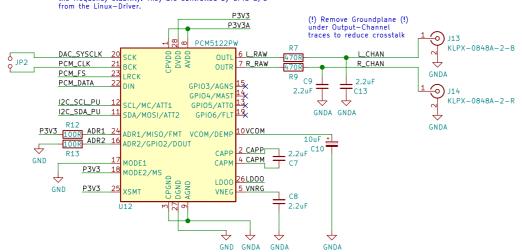
### Power Section

The Hat is powered from an external 30V 2A Power-Brick.
P30V is directly switched to the Panel's Solenoid and Light Bulbs through Q4.
P5V is generated from P30V by U13 and passed to the RaspberryPi through the Protection Circuit around Q1.
P3V3 is generated from P5V5 by U10 for all the local, digital ICs.
P3V3A is generated from P5V5 by U11 for the Analog Portion of the Audio DAC U12.
GND and AGND is joined in a Star-Grounding-Point to minimize Crosstalk from the Digital to the Analog side.



# Audio Connector

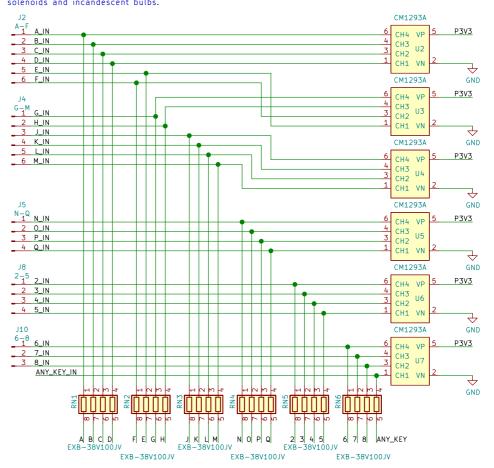
The System-Clock SCK is generated with a PLL internally from PCM\_FS. Alternatively one could add 2 extra Oscillatory to enhance the frequency stability. They are controlled by GPIO 3/6 from the Linux-Driver.



Decoupling between CPVDD / CPGN				en	
P3V3A C1 10uF C2 1uF	C3 10uF C4 1uF	C5 10uF C6 1.1uF	C110 10uF C12 1uF	12C_SDA_PU	P3V3
CNDA	CND.	CND.	CNDA		

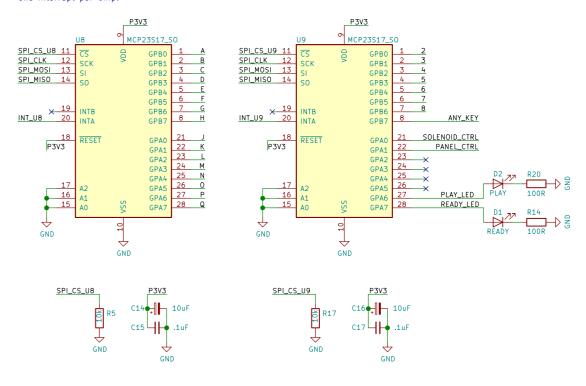
# Panel Connectors & Input-Protection

All Inputs are equipped with 3.3V Transient Suppression Diodes and series resistors to protect against ESD and inductive coupled Transients to support the the long cable runs and close high-current solenoids and incandescent bulbs.



#### **GPIO Port Extender**

Two MCP23S17 (SPI 16bit Port Extender) read from the Panel-IOs and to drive the FETs which control the Panel-Power. Q8 and Q9 each have their own Chip-Select and Interrupt-Line. The Interrupt-Mirror-Feature is used, to only have one Interrupt per Chip.





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