Architecting Millisecond Test Solutions for Wireless Phone RFIC's

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ABSTRACT

Today's low cost wireless phones have driven a need to be able to economically test high volumes of complex RF IC's at a fraction of the cost of the IC. In June of 2001 the IBM test development group developed a strategy and design to test complex wireless phone front end components for a fraction of the cost of using traditional ATE or rack and stack test solutions. In this paper the architecture of the system is described as well as some of the design, maintenance and implementation considerations. The system is designed to bring the cost of complex manufacturing test of RF IC's equivalent to that of testing discrete components such as resistors or capacitors. Given the drastic reduction of test cost and the relative ease of implementation of this solution this architecture sets the bar for future RF test solutions. To the best of our knowledge, this architecture has resulted in the fastest RF tester in the world.

1. INTRODUCTION

The commercial wireless industry has driven a need for very low cost RF IC's built with very low cost packages and manufacturing processes. A key contributor to the cost of manufacturing an RF IC packaged part is the module final test. Up until that step in the manufacturing process the components can be handled in a batch mode with standard high volume wafer fabrication and package part assembly equipment. Once the part hits RF test it must be individually placed in a precision socket with precision pressure, and electromagnetic isolation, and must be tested at a very narrow band, high frequency, low signal level. We originally set our objective to figure out how to completely RF test a part for less than a penny/part. The ability to mechanically handle individual components and place them in a precision socket quickly and repeatable has been addressed by the commercial handler manufacturers with a range of efficiencies. The actual RFICs are electrically tested with either of rack and stack bench top equipment connected to a PC or with commercially available Automatic Test Equipment. Usually the most costly and complex component in the systems is the RF receiver, or spectrum analyzer and most systems are only configured to handle only one receiver per system. These receivers must handle a frequency range between 100MHz and 6GHz and have a very high dynamic range capable of measuring stringent two tone signals such as Adjacent Channel Power (ACPR) or Third Order Intercept (IP3). These signals are difficult to measure because they consist of a primary high power frequency or tone at 900MHz to 6GHz which is adjacent to a very low level noise tones 10MHz away which must be measured repeatable to 0.1dB accuracy. The high susceptibility of the Device Under Test DUT to electromagnetic noise from it's immediate surroundings and the need for an extremely sensitive, precision RF receiver to be able to make these type of measurements tends prohibit parallel site testing. In this paper we describe a method we have used in IBM to address these constraints. It is a test system architecture incorporating some fairly simple circuits that can be applied to the RF test board to convert the RF signal to a DC signal. This critical step makes a major impact to the cost of test for an RF component by converting the test system from a complex RF single site tester to an extremely fast, inexpensive multi-site DC tester. The result of this work drives the cost of test of these systems to that of a high throughput DC parametric tester.

2. COST OF TEST

Test cost is driven by two main factors, time spent per part testing it and the costs associated with the implementation and equipment used for the test.

Total Test Time	Test Costs
Handler Capability	Test System Capital
Index Time of Handler	Handler Capital
Tester Capability/Speed (Electrical Test Time)	Operations Overhead (Operator, Building, Maintenance)
Handler/Tester/Controller Communications Time	Test Hardware & Software Development Engineering

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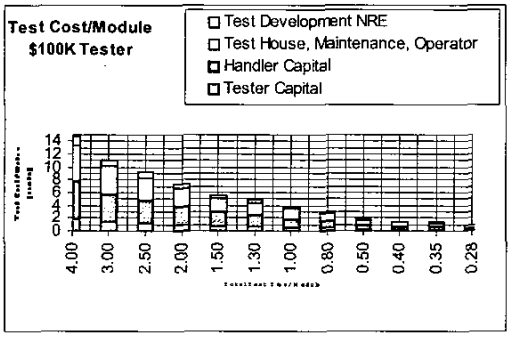
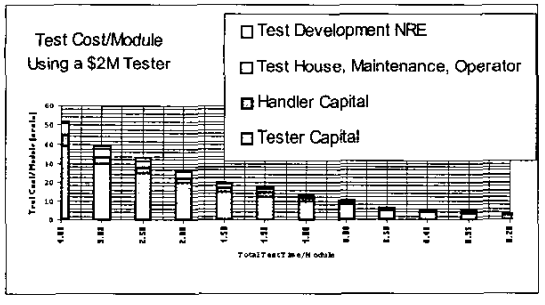
In order to understand the impact of these two factors the cost/module is calculated verses test time assuming the following manufacturing costs:

- The Handler Costs $300K and is flat depreciated over 5 years.
- An RF Tester Cost $2M and is flat depreciated over 5 years.
  The low cost tester costs $100K and is flat depreciated over 5 years
- It costs $50/Hr to run the manufacturing floor and maintain and operate the tester.
- It costs $150K in hardware and labor to develop a Unique RF test solution. This cost is spread over an estimated 2 year lifetime of a product .

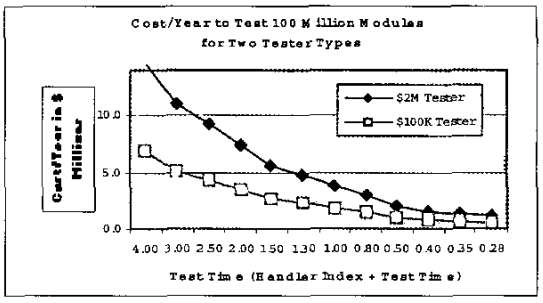
In the following plot the cost contributors to testing a part for various test times is illustrated. The lowest limit on the test is set to 280msec from a 200msec hander index time and 80msec test time.



The primary contributor to the product cost is the tester capital followed by the operations and handler cost. Driven mainly by the high test capital cost, the lowest possible cost/part is 3.6cents/module. In order to get to a 1cent/module cost, the same chart is plotted using a $100K tester instead of a $2Million tester.



In this plot a 280msec total test time, using a $100K tester leads to a 1cent/module total cost of test adder. Additionally at a 280msec each tester is capable of 50 to 100 Million modules/year. Specifically, if the manufacturing test floor runs 17 hrs/day, 7 days/week, and 48 weeks/year or 5712 Hrs/year the total capacity at a 280msec total test time is 73 million modules. At this capacity one or two testers can normally handler the entire products requirements, reducing the additional cost to maintain multiple systems, correlated across a test floor. This is illustrated in the chart below for a $2M Tester and a $100K tester.



For a high volume product requiring 100 million modules/year, at a 4sec test time, 20 testers are required at a cost between $7M and $15M per year depending on the cost of the tester. At a 280msec total test time the cost drops to between $1M and $600K per year to test 100M modules. So as expected, both test time and tester capital cost pay a major role in both the cost per module and the total cost to support the test floor.

Therefore the first conclusion reached was:
In order to reach our target of a 1cent/part test cost adder an RFIC tester/handler system was required that could reach a 0.28sec/module test time and use a tester that costs less then $100K.

3. RF TEST HARDWARE DEV.

The cost of getting an RF product onto a tester is primarily driven by the test fixture hardware design, build and debug. The test code development time is a know, predictable quantity that normally takes less time then the design of the hardware. A poor hardware methodology on the other hand can easily lead to substantial delays and cost over runs. The subject of RF test hardware development methodology was extensively covered in last years ITC Paper. [1] Having robust RF board design and simulation skills, and tools is absolutely critical to containing schedules, development

[1] "Moving from Mixed Signal to RF Test Hardware Development", M. Slamani, J. Ferrario, R. Wolf, H. Ding, Proceedings of the International Test Conference 2001, page 948

costs and surviving in the RF test business. Regardless of what tester you connect the part to you're in the RF board design business. At a very minimum the test board has a socket with a finite parasitic inductance and capacitance that is different then the interconnect the part will see on the phone board. This will drive a different RF load matching circuit. Over the last several years our test lab has developed over a hundred RF test solutions for a wide range of design teams. Independent of the tester, it has been necessary to incorporate some subset of the follow set of functions on the test board or in the test fixture to bridge from the standard commercial testers to the device under test.

- Match the device impedance to the 50 ohm transmission line
- Convert the RF signal from differential to single ended or vis versa
- Switch the RF signal to the RF and analog ports of the tester
- Filter input or output signals
- Filter power supply or control line signals
- Amplify low level noise signals so you can get enough power to the receiver
- Set up RF coupled bias tees, to AC and DC couple to a line
- Lock a VCO signal using a phase lock loop (PLL)
- Phase shift a signal 90 degrees to create a fixed I Q signals
- Attenuate high power signals
- Isolate signals from RF reflections

Having the engineering capability to design these functions onto a test board is a minimum requirement in the RF test development process. The RFIC design team may already have some of this circuitry defined as part of an evaluation board or previous phone board design.

4. OPTIONS TO BUILDING RF TEST HARDWARE

An option to developing RF test hardware is to develop some sort of analog Built In Self Test (BIST) function in the IC[2]. This has become a standard procedure for logic type products and has been used in our lab for very high speed 10Gbit and 40Gbit optical drive circuits. Although it removes the problems associated with coupling high frequency signals on or off the chip, ABIST does not seem to have gained popularity for wireless phone RFICs because:

Cost in Increased Die Size - Analog circuits tend to take up a sizable amount of space for even the simplest functions. This is inconsistent with trying to reach a minimum die size and minimum wafer costs.

Performance – Adding additional circuitry to the extremely parasitic sensitive RF lines is not trivial and can easily degrade the parametric performance of the IC. Designs are often already trying to push the limits of the process technology. Even industry standard ESD protection is often deleted from the RF IC pins to preserve the integrity of the RF signals.

Package Cost – Adding additional Pins for internal self test could easily drive a larger die size and or package size. Even the cost of adding additional wirebonds is a factor for low cost RFICs.

Functional Test Verses Fault Coverage – For logic components there may be little to no yield difference between a a functional test and a BIST based fault coverage type test. If all of the gates are good the part is good. In the RFICs we have observed the circuits are very serial so DC supply and leakage tests are usually adequate to determine if a die is operational. But most of the designs we have seen also seem to be pushing the limit of the process technology so some form of functional RF verification testing is required. Adding design margin although desirable, does not seem to be the norm. In an application where Analog self-test circuits were observed it added almost 100% to the die size, degraded the performance of the die and ended up being pulled from the die after the first release. .

An Accurate, High Resolution DC Test May Be Adequate - For some simpler single band RF IC's for which we had testing millions of devices, it was found that they never failed for just an RF test without also failing a sensitive DC test. On these products we were able to replace 100% RF testing with periodic RF sampling tests.

Based on the above items it was concluded that ABIST would not be available and what was required was a tester with accurate, sensitive DC measurement capability as well as RF test capability.

[2] "A Stand-alone Integrated Test Core for Time and Frequency Domain Measurements" M. Hafed, N.Abaskharoun, G. Roberts - McGill University, Proceedings of the 2000 International Test Conference.

5.0 ARCHITECTING A VERY LOW COST TESTER - (The Handler)

With test times in the mill-seconds and on the order of the handler index time it was important in the test system design not to de-couple the handler from the tester. In the sub-second regime the interaction of the handler, tester and controller play a critical role in the total test time. In order to develop a millisecond testers the following steps were taken:

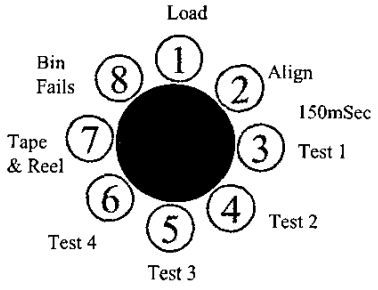
1) Find a handler that can serially place a component into the socket with the fastest index time possible.
2) Develop the RF hardware to optimize the handler throughput and minimize capital investment.
3) Fine tune the composite tester/handler combination for optimum throughput.
4) Do all GPIB communications during the idle handler load time.

Note from item 1 above the handler determines what the tester look like verses taking the approach of developing a test on the best RF tester then moving it to a handler. Both the handler index time as well as the test solution need to be sub one second in order to get a total sub one second test time.

5.1 COMPONENT HANDLERS

Three types of handler modes of operation were considered.

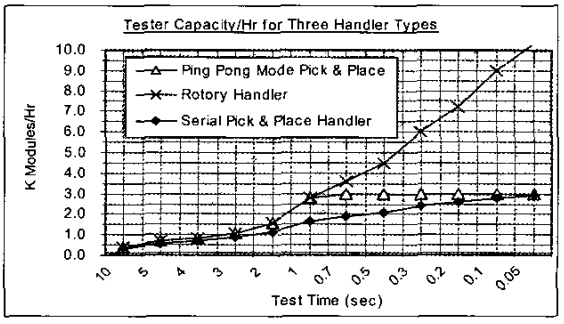
1. Rotary Mode - In this mode the handler has multiple arms and will que up the parts in an assemble line fashion such that the handler tasks are broken up into smaller ones which are each done in Parallel. This allows the handler to narrow down the effective index time to that of the longest individual step. The index time of the rotary handler we used was 150msec.



2. Pick & Place Mode - The handler can operate serially or in parallel to pick up the devices and place them in a test socket. Index times of the handlers we used were around 1.2 sec/part.

3. Pick & Place Handler in Ping Pong Mode - There are two sockets on the test board. While the tester is testing one part the handler is dropping the other part off and queuing a second part over the second socket. When the first part is finished testing the second part is quickly placed into the second socket. If the test time is greater then 1.2 seconds, the index time is 0.3 seconds. If the test time is less then 1.2 seconds the total test plus index time remains at 1.2 seconds independent of the test time.

In the chart below the throughput of these three modes are plotted verses test time. Only the single site pick and place handling is considered. Due to the electromagnetic field cross talk effects, increased noise level and limited RF test receiver resources, parallel testing of wireless components was not pursued.



Note from the chart as expected Ping Pong Mode testing was better then single site testing on a pick and place tool but for test times below 1 second the rotary handler had a sizable throughput advantage. Although we never needed to break up our test the rotary style handler would have allowed us to break up the test into eight sub-tests. In this case parallel testing may have been possible due to the larger distance between fixtures which would have enabled shielding but you don't get the same time savings as with the parallel pick and place type handlers. The throughput using a rotary handler can be three times that of the pick and place handler as test times fall below 100msec.

- **Strip Handlers** were not considered because of the high tester plus handler capital cost, they drive major changes in the packaging lines and the engineering problems associated with trying to RF probe multiple

adjacent RF components. For package manufacturers who already have this equipment it is worth future investigations if the RF tests can be staggered across the sites.

- **Multi-site pick and place or gravity feed handlers** were not considered because of RF cross talk effects between adjacent sites. Another mode that can be used with these handlers is to serially test the RF portion and parallel test the DC. In our experience the RF tests consumed 60% to 80% of the test time. If we consider a 1 second test time with parallel test on 30% of the tests we have:

(1 sec for 2 parts + 0.7 sec serial test overlap)
=> (0.85 sec/part)
(1 sec for 4 parts + 2.1 sec serial test overlap)
=> (1+2.1)/4 = 0.78 sec/part)
(1 sec for 8 parts + 4.9 sec overlap
=> (5.9/8 = 7.4sec/part)

So as the number sockets went up:

- The test time/part goes down
- The Jam rate associated with getting 4, or 8 small RF devices aligned in the socket correctly goes up, (We struggled with 2 in parallel) and
- The complexity of the Tester and a test board capable of the switching the RF signal around to multiple sites goes up.

Multi-site testing was only used for products which had a small amount of RF with a large amount of mixed signal or DC testing.

Since most of our products were dominated by RF tests, the rotary handler approach was used for most of the RF front end components.

6.0 ARCHITECTING A VERY LOW COST TESTER (VLCT) - (THE TEST HARDWARE)

6.1 THEORY OF OPERATION

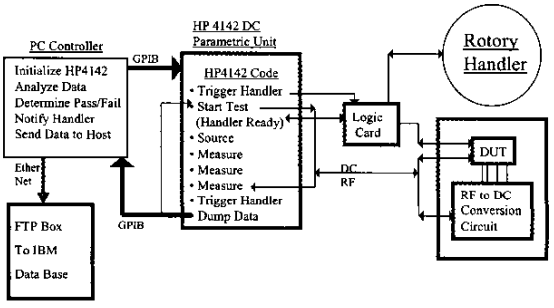
The equipment used on our sub 200msec RF tester was as follows:

- A Fast Accurate DC Source Measurement Unit with:
  - * Nano-amp resolution
  - * Micro-volt resolution
  - * Internal microprocessor
  - * Analog Feedback Capability
- A Parallel and serial logic card
- RF to Analog Conversion Circuitry
- A Fast Computer
- A Frequency Counter and Power Meter for system calibration.

The system works as follows. A PC dumps a program into the HP4142 microprocessor, then the HP4142 runs on its own as it tests all of the product. When the test is complete, the handler moves off to get a new part. While the handler is unloading and loading a new part the HP4142 sends the PC the raw data on the part and gets ready for the next part. No time is lost in PC to HP4142 communications so there is no penalty to using relatively slow GPIB communications. This is an important factor that leverages the built in delay of a rotary handler between the time it tests a part to the time it needs to bin the part. Logic commands are generated by a logic card that is triggered by the HP4142 trigger. The HP4142 analog feedback unit is used to set current or voltage when a predefined value is not known, such as setting the power on a power amp. Since it is an analog feedback loop it works faster then a software loop and the controller to instrumentation communications can be avoided.

A block diagram of the system is shown above.

Another extremely important feature of this system is the



ability to make highly accurate, high resolution DC current measurements. The HP4142 has highly repeatable anno amp current source and measurement resolution which is better then most larger RF ATE systems. It has be seen that there is a close relationship between the DC parameters and the RF parameter so in many cases a tight DC test will catch the majority of the fails without the need to even do the RF test.[3]

The Key benefits of this systems are:

1) No time is lost due to GPIB instrument to instrument communications. Communication, which are required are done using single pulse triggers between the HP4142, the controller Logic Card and the DUT card. The time consuming process of data transfer between the HP4142 and the PC is done in dead-time while the handler is indexing.

[3] "Production DC Screening for RF Performance of a 900MHz Monolithic Low Noise Amplifier", Sang-Gug Lee, R. Douglas Schultz, IEEE 1995 Microwave and Millimeter-Wave Monolithic Circuits Symposium.

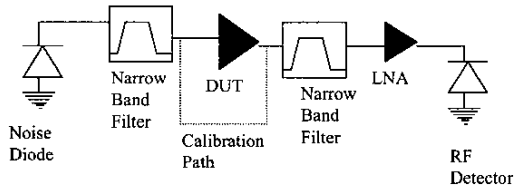
2) There is only one source/measurement instrument. Measurements such as RF power, RF noise figure, ACPR, IP3 and Phase noise are done on the DUT board and converted into a DC measurement.

This strategy results in RF measurements taking the same time as it takes the HP4142 to make an analog measurement.

7.0 RF TO DC DIRECT CONVERSION ELECTRONICS

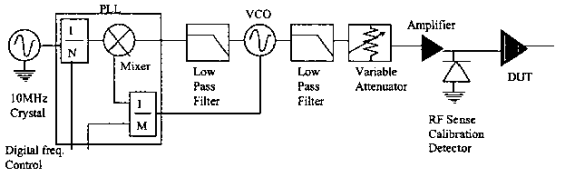
Commercial RF test equipment consists of a microwave source and receiver. Both the sources and the receivers are designed to cover a wide range of frequencies and powers. In the initial stages of characterization, this flexibility is a necessary feature, which enables very rapid program changes. But once the part reaches the final stage of production, only a few worst-case frequencies or powers are actually required to guarantee the performance of the device. The degree of purity and dynamic range of these few critical frequencies can directly effect the test time. Noise in the signal normally drives increased measurement averaging and increased test time. When the measurement requirement becomes very limited, such as the measurement of one tone next to a higher power tone, then a very focused narrow band measurement circuit can often do a better job then a broad band receiver. We have seen a narrow band circuit specifically designed with passive filters for one frequency and mounted right on the test board as close to the part as possible has a higher signal to noise ratio and requires less averaging if any. Four circuits are shown here which have been used on test boards to do RF to analog signal conversion.

7.1 RF Power/Noise Figure Detector Schematic



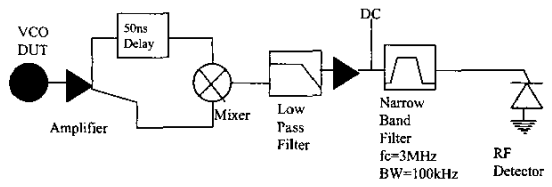
This circuit is used to measure the noise figure and gain of a device under test (DUT). The noise diode generates a broad band RF signal which is filtered in the narrow band filter. By varying the DC bias on the diode, multiple powers can be obtained. On the receiver side a narrow band filter is used to filter out any out of band noise, the Low Noise Amplifier mounted within an inch of the part is used to amplify the signal into the RF detector. All of the components used did not have a high sensitivity to temperature. The total uncompensated error in the circuit between -20C and 80C was 1dB. We did mount a thermistor on the board in our initial design for temperature compensation but so far we to have found it unnecessary. There is a calibration path around the part that is used to verify the circuit performance. This circuit has been used on a dual band LNA receiver chip to reduce the test time from 1 sec/part to 150msec/part. Both the source and detection of the circuit is done with an HP4142 DC source monitor channel.

7.2 RF & LO Source Schematic



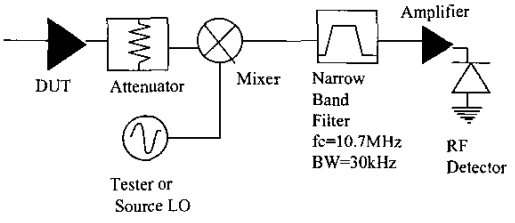
This circuit is used when a specific tone is required for either an LO or a mixer input and replaces the testers RF source. The frequency of the circuit is limited to a narrow band of the VCO. The PLL has digital control lines which are used to adjust the frequency. The RF sense detector is used to monitor the variable attenuator, VCO and amplifier power. An external frequency counter is used to periodically check the VCO frequency. The PLL was an off the shelf, self contained part. There are commercially available modules which included the entire circuit and are controlled via several digital pins. We preferred this approach so we would have more control over the VCO source and filtering. The spectral purity of this source was compared with our commercial RF manufacturing test systems. Not only did the source have a cleaner signal to noise ratio, it also lead to a lower test time when used as an LO source for an IP3 measurement. The major draw back of using these circuits as a source is the limited frequency range. The wider the frequency range of the VCO the worse the phase noise, so we tended to use very limited frequency range VCOs.

7.3 Phase Noise and the RF Discriminator Schematic

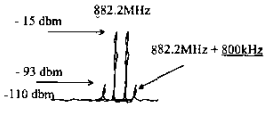


This Phase noise circuit was used to measure the phase noise of an RF VCOs. In this circuit the RF signal is split with a 90 degree phase shift so that the signals that meet at the mixer will cancel if the phase noise is zero. If the phase noise is not zero then only the low frequency phase error comes out of the mixer. The signal is then passed through a low pass filter to eliminate the high frequency term from the mixer. A DC sense line is used to adjust the delay to the 90 degree phase shift. The narrow band filter is used to place a window around the phase noise which is consistent with the test requirements. The Q of this filter is extremely important but achievable with off the shelf components. The RF detector then measures the power in that window without the need for averaging or stepping through the window in discrete frequency steps. A complex RF phase noise measurement is now reduced to a simple DC voltage measurement.

7.4 ACPR & IP3 Measurement Schematic



IP3 or ACPR measurements both involve measuring a small tone adjacent to a larger tone. The problem is the larger tone will saturate the receiver due to limitations in the receiver dynamic range. Filtering out the primary signal is not an option due to how close the adjacent signal is to the primary relative to the high primary signal frequency. So the signal is down converted with a mixer to a lower frequency where it is possible to filter out the primary signal. An attenuator is placed in between the DUT and the mixer to prevent reflections from the mixer getting back into the DUT. The narrow band filter is lined up to include just the adjacent tone. The RF detector is used to convert the power measurement into a DC voltage. A complex time consuming IP3 measurement is reduced to a DC voltage measurement. Prior to using this circuit the IP3 test had been the longest test for mixer components. After implementation of the circuit the test time reduced 100x for both the overall test as well as this specific test.



8.0 System Maintenance, Calibration and Reliability

Each of the circuits have some method of self calibration to ensure that the components haven't drifted. On the DUT board the components are covered with an RF metal cage to protect the circuit and DUT from stray EM fields. A temperature monitor is placed on the board next to the components to monitor temperature and generate compensation factors.

Over the past two years in manufacturing the top two failing instruments on our 35 RF commercial test systems has been either the microwave source or the receiver. These microwave instruments are complex units with hundreds of components with potential to fail.

The RF to DC circuits above consist of passive components, and in most cases less then five active components. Each of the components are military spec, high reliability components. If there is an equal probability of failure for every component then just based on pure probability the chances of a component failure using a commercial Receiver or Source is hundreds of times higher then one of these simple circuits. We expected the amplifiers to be our main source of failure. So we have not had a single active component fail. The sources of fails we have seen have been:

- Cracked surface mount passive components or
- Loose mechanical connections due to handler vibration fatigue.

We are addressing both of these concerns buy increasing the strength of the DUT boards and mechanically isolating critical measurement circuits from the DUT board and test head.

The main commercial measurement unit was the HP4142 which has been in commercial service for over ten years. It has it's own self calibration and self diagnostics capability. It's easy to replace faulty SMUs

on the test floor without any expensive maintenance contracts. Agilent will be coming out with a new version of this box which will allow us to write longer programs into the HP4142.

The only other critical component is the PC. The speed of the PC is not that critical because the entire test is run by the HP4142. The PC handles getting the data out of the HP4142, controlling the handler, monitoring the systems and sending the data to the host.

9.0 Conclusion

An architecture for an RF test system is described that reduces the time to test an RF part from seconds to 10s of milliseconds. It also reduces the complexity of the test programming and tester equipment to that of a DC parametric tester. The system adds complexity to the test fixture or test board design but the added upfront engineering work results in a faster test time, lower cost test equipment, the need for fewer testers and less complex test programming. The RF to DC conversion and DC to RF circuitry can be managed and grouped into common reusable blocks reducing the engineer work associated with follow-on programs. The system is based on the fastest known handlers for the given package types and takes advantage of the handler software and hardware design to maximize throughput on the system. The RF electronics is at least a factor of 100 less complex then the standard RF test instruments resulting in a very highly reliable and easy to maintain system. The system calibration relies on a highly reliable, commercially available DC parametric analyzer to detect shifts in the RF source and measurement circuitry. In the future we will continue to expand the library of RF to DC and DC to RF test fixture components as new products emerge and apply the same libraries to larger devices to enable complex RF components to be tested on existing mixed signal or logic testers.