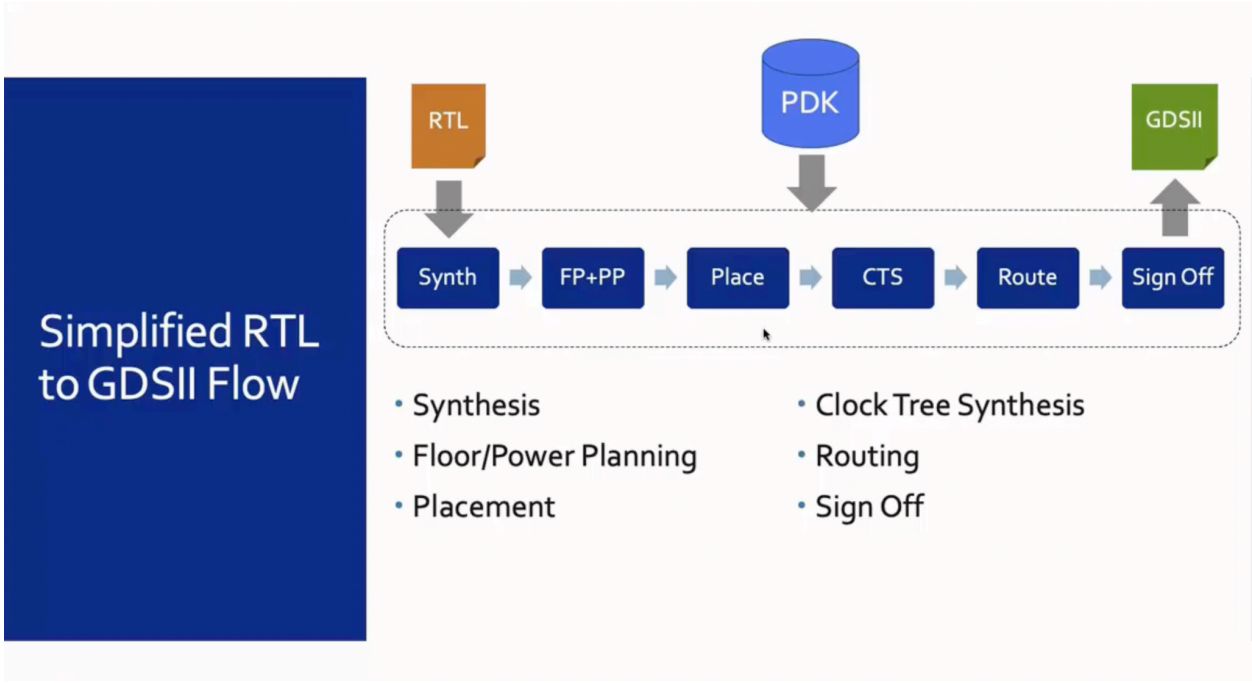
Day 1

Simplified RTL to GDSII Model



Synthesis:

The RTL file is converted into a gate level netlist using components from the Standard Cell Library.

Floor Planning & Power Planning:

Floor Planning: Determines the position of components on the chip to minimize area, including the placement of I/O pins, ports, and pads.

Power Planning: Designs the power supply network (VDD and GND) using power rings, power straps, and power pads, typically on the top metal layers for minimal resistance and delay.

Placement:

Placement is performed in two stages: Global Placement (finding ideal positions for each cell but the cells may overlap) and Detailed Placement (where cell positions obtained from Global placement are minimally altered and are optimally placed following placement rules).

Clock Tree Synthesis:

Clock routing is performed before signal routing to address clock skew i.e, the difference in time for the clock to reach various destinations.

Symmetric Tree Structures (H-tree, I-tree, X-tree) are used to eliminate clock skew.

Routing:

Signal routing is performed using the remaining metal layers and is divided into Global Routing (generates a routing guide based on PDK instructions) and Detailed Routing (actual routing according to the guide).

Sign-off:

Once routing is completed, the chip undergoes various checks during the sign-off stage:

Physical Verification Checks: Design Rule Check (DRC) and Layout vs. Schematic (LVS). DRC verifies design rule compliance, while LVS ensures functional correctness against the gate-level netlist.

Timing Checks: Static Timing Analysis (STA) checks the design for timing violations.

Getting familiar with the Basics

Commands used:

```
cd Desktop/work/tools/openlane_working_dir/openlane
docker
./flow.tcl -interactive
package require openlane 0.9
prep -design picorv32a
run_synthesis
```

Task 1

To calculate the flop ratio and percentage

Flop Ratio = No of D flip flops/Total Number of cells

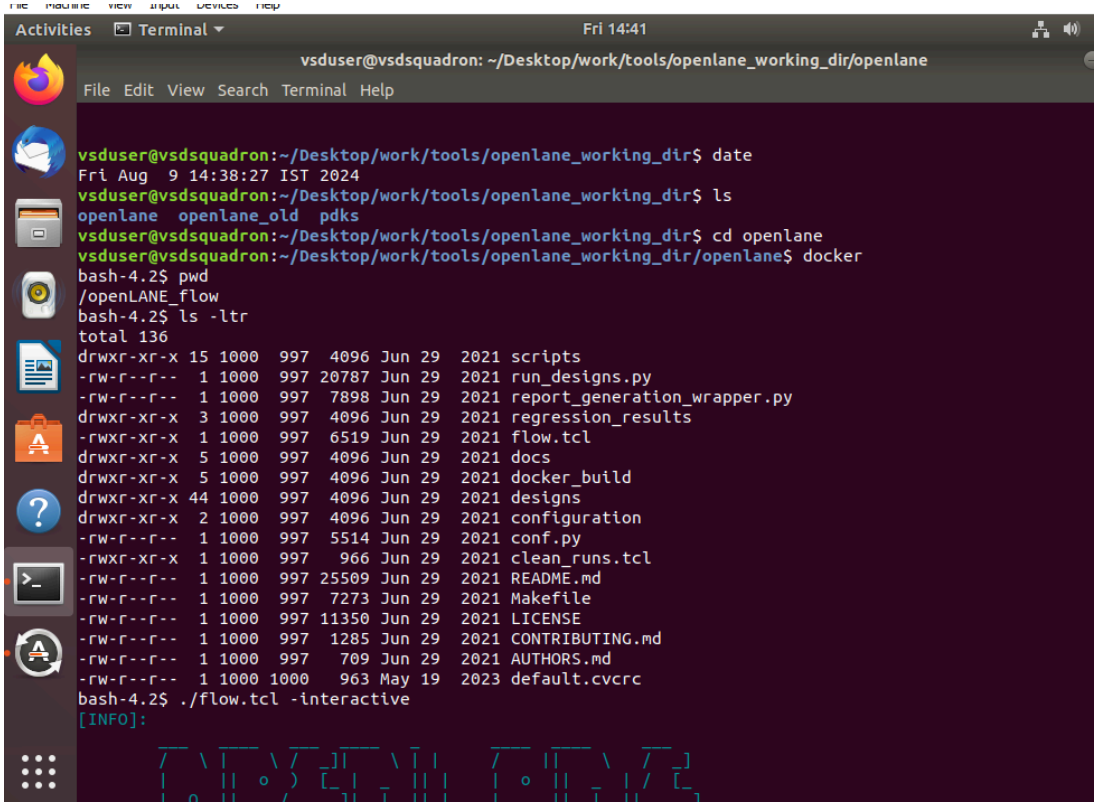
= 1613/14876

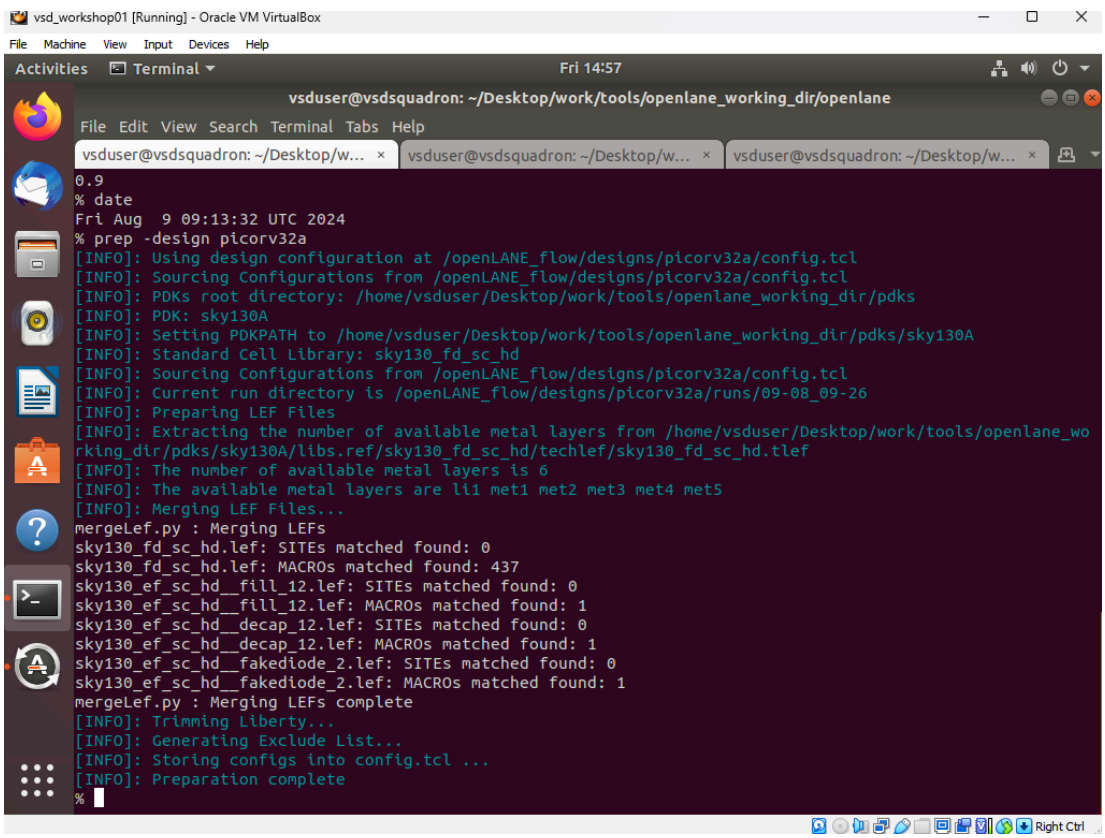
=0.1084

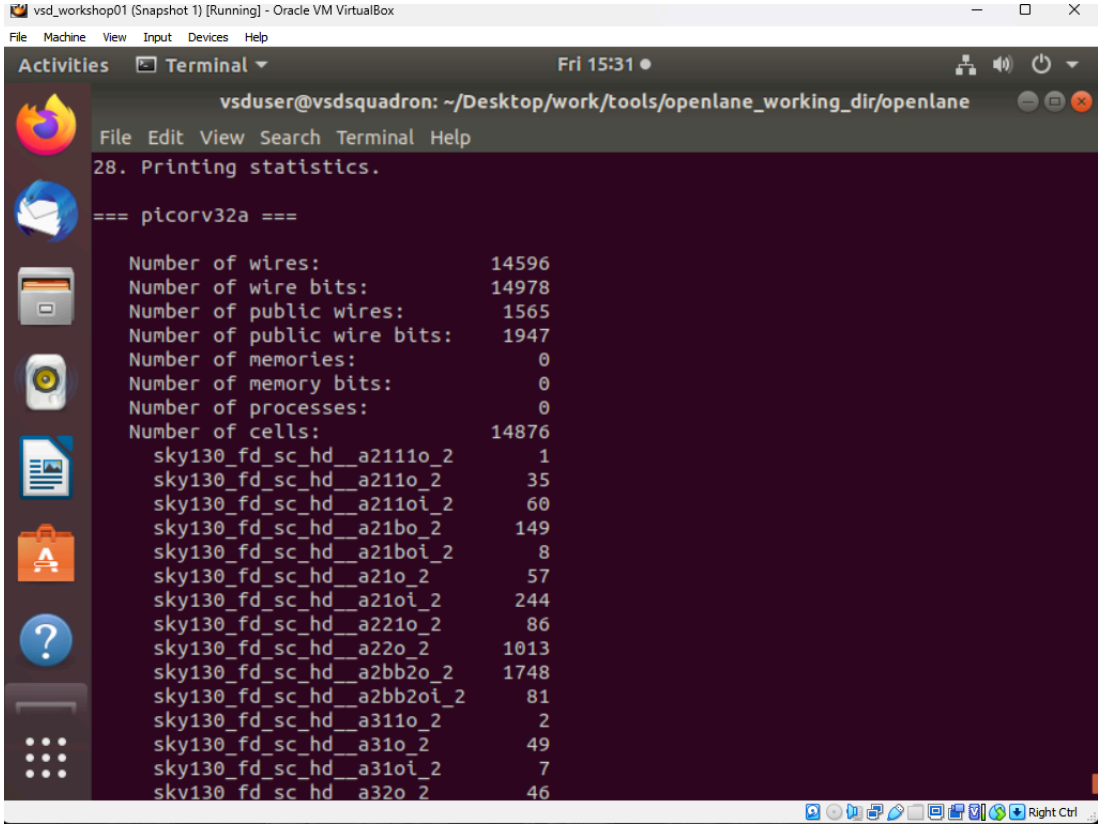
Percentage = Flop ratio x 100

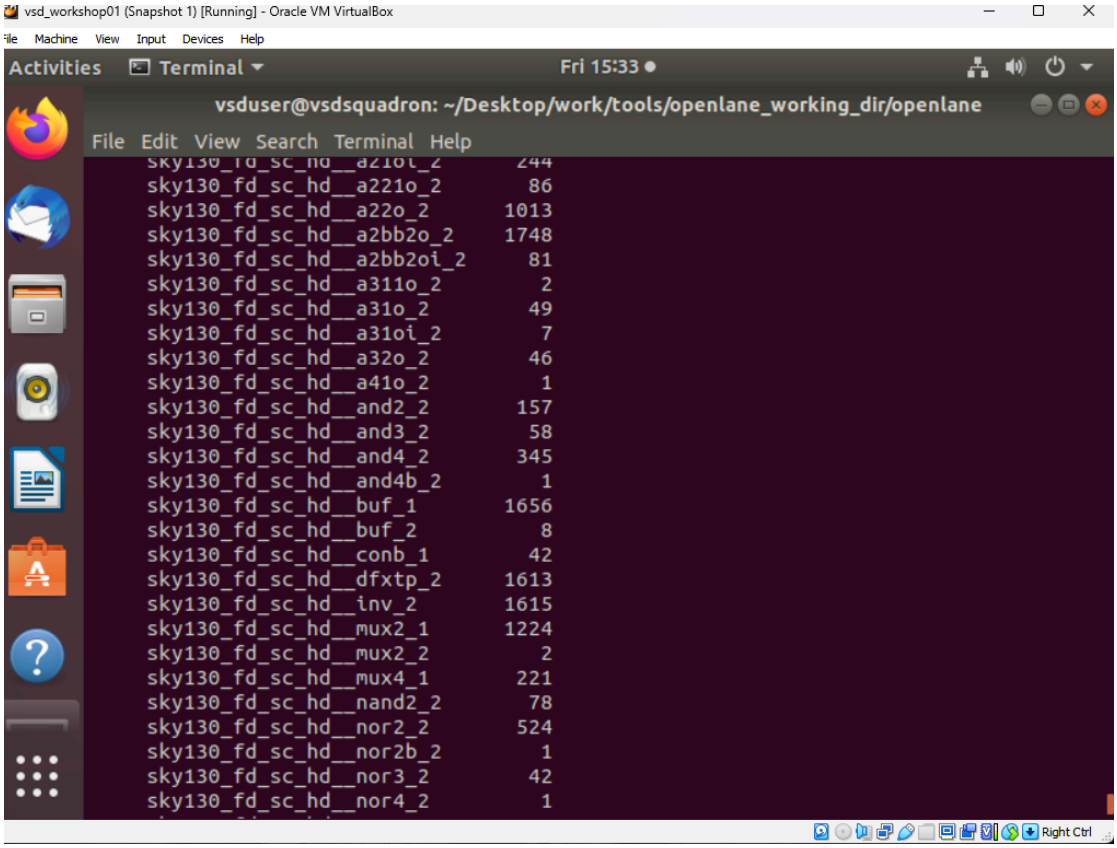
= 0.1084 x 100

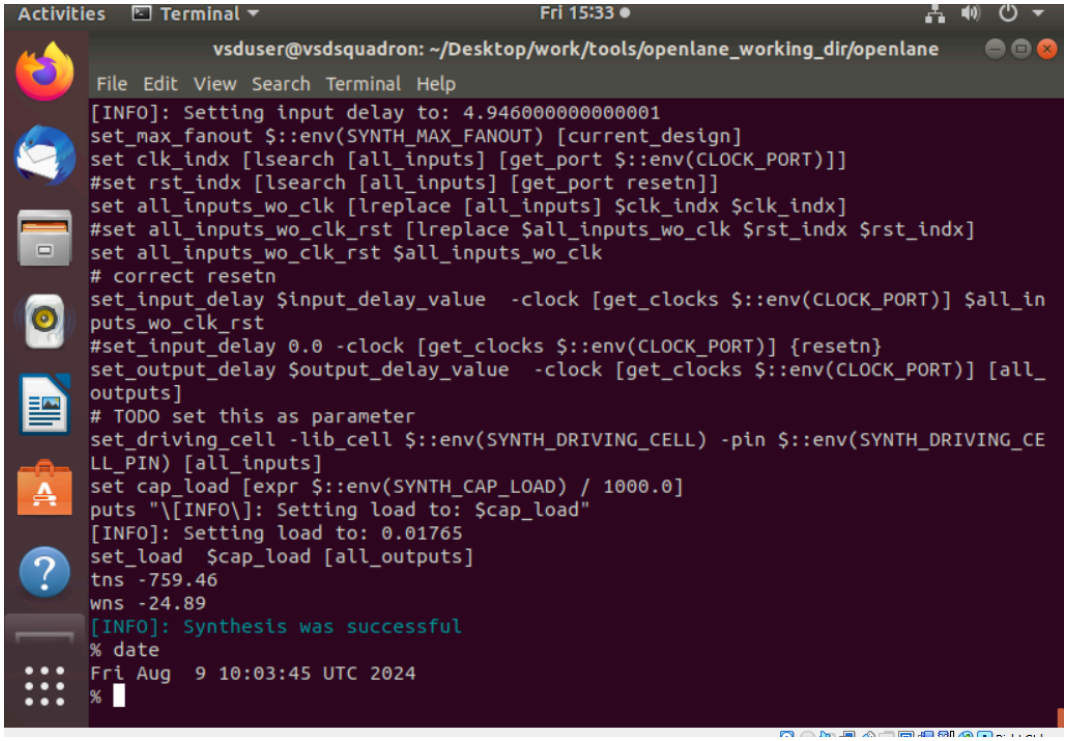
= 10.84%


Activities
Terminal
Fri 14:41
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ date
Fri Aug 9 14:38:27 IST 2024
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls
openlane openlane_old pdks
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ pwd
/openLANE_flow
bash-4.2$ ls -ltr
total 136
drwxr-xr-x 15 1000 997 4096 Jun 29 2021 scripts
-rw-r--r-- 1 1000 997 20787 Jun 29 2021 run_designs.py
-rw-r--r-- 1 1000 997 7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x 3 1000 997 4096 Jun 29 2021 regression_results
-rwxr-xr-x 1 1000 997 6519 Jun 29 2021 flow.tcl
drwxr-xr-x 5 1000 997 4096 Jun 29 2021 docs
drwxr-xr-x 5 1000 997 4096 Jun 29 2021 docker_build
drwxr-xr-x 44 1000 997 4096 Jun 29 2021 designs
drwxr-xr-x 2 1000 997 4096 Jun 29 2021 configuration
-rw-r--r-- 1 1000 997 5514 Jun 29 2021 conf.py
-rwxr-xr-x 1 1000 997 966 Jun 29 2021 clean_runs.tcl
-rw-r--r-- 1 1000 997 25509 Jun 29 2021 README.md
-rw-r--r-- 1 1000 997 7273 Jun 29 2021 Makefile
-rw-r--r-- 1 1000 997 11350 Jun 29 2021 LICENSE
-rw-r--r-- 1 1000 997 1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r-- 1 1000 997 709 Jun 29 2021 AUTHORS.md
-rw-r--r-- 1 1000 1000 963 May 19 2023 default.cvcrc
bash-4.2$ ./flow.tcl -interactive
[INFO]:


vsd_workshop01 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
Activities
Terminal
Fri 14:57
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/w...
vsduser@vsdsquadron: ~/Desktop/w...
vsduser@vsdsquadron: ~/Desktop/w...
0.9
% date
Fri Aug 9 09:13:32 UTC 2024
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/09-08_09-26
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are li1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd__fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd__fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd__decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd__decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd__fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd__fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
%
Right Ctrl


vsd_workshop01 (Snapshot 1) [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
Activities
Terminal
Fri 15:31
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
28. Printing statistics.
=== picorv32a ===
Number of wires: 14596
Number of wire bits: 14978
Number of public wires: 1565
Number of public wire bits: 1947
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 14876
sky130_fd_sc_hd__a2111o_2 1
sky130_fd_sc_hd__a211o_2 35
sky130_fd_sc_hd__a211oi_2 60
sky130_fd_sc_hd__a21bo_2 149
sky130_fd_sc_hd__a21boi_2 8
sky130_fd_sc_hd__a21o_2 57
sky130_fd_sc_hd__a21oi_2 244
sky130_fd_sc_hd__a221o_2 86
sky130_fd_sc_hd__a22o_2 1013
sky130_fd_sc_hd__a2bb2o_2 1748
sky130_fd_sc_hd__a2bb2oi_2 81
sky130_fd_sc_hd__a311o_2 2
sky130_fd_sc_hd__a31o_2 49
sky130_fd_sc_hd__a31oi_2 7
sky130_fd_sc_hd__a32o_2 46
Right Ctrl


vsd_workshop01 (Snapshot 1) [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
Activities
Terminal
Fri 15:33
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd__a21oi_2 244
sky130_fd_sc_hd__a221o_2 86
sky130_fd_sc_hd__a22o_2 1013
sky130_fd_sc_hd__a2bb2o_2 1748
sky130_fd_sc_hd__a2bb2oi_2 81
sky130_fd_sc_hd__a311o_2 2
sky130_fd_sc_hd__a31o_2 49
sky130_fd_sc_hd__a31oi_2 7
sky130_fd_sc_hd__a32o_2 46
sky130_fd_sc_hd__a41o_2 1
sky130_fd_sc_hd__and2_2 157
sky130_fd_sc_hd__and3_2 58
sky130_fd_sc_hd__and4_2 345
sky130_fd_sc_hd__and4b_2 1
sky130_fd_sc_hd__buf_1 1656
sky130_fd_sc_hd__buf_2 8
sky130_fd_sc_hd__conb_1 42
sky130_fd_sc_hd__dfxtp_2 1613
sky130_fd_sc_hd__inv_2 1615
sky130_fd_sc_hd__mux2_1 1224
sky130_fd_sc_hd__mux2_2 2
sky130_fd_sc_hd__mux4_1 221
sky130_fd_sc_hd__nand2_2 78
sky130_fd_sc_hd__nor2_2 524
sky130_fd_sc_hd__nor2b_2 1
sky130_fd_sc_hd__nor3_2 42
sky130_fd_sc_hd__nor4_2 1
Right Ctrl


Activities
Terminal
Fri 15:33
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_in
puts_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_
outputs]
TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CE
LL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
% date
Fri Aug 9 10:03:45 UTC 2024
%