ECE 6348 VLSI DESIGN PROJECT

4 BIT JOHNSON COUNTER

SUBMITTED BY

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1. Aim

To design a 4 bit Johnson counter by choosing an appropriate flip flop and to simulate the behavior of an optimized schematic and layout with the help of Cadence IC Design Tool for a chosen CMOS Technology.

2. Introduction

2.1. Flip Flops

Flip Flops are synchronous bi-stable devices which are basic units of a digital circuits. It is a memory cell that can store one bit data. These flip flops basically provide the out in both normal and complemented form. Set of flip flops are usually combined to store and hold multiple bits data. Flip flops are also used in sequential logic circuits. There are different types of flip flops that hold and manipulate the data in different ways. Figure shows the various kinds of flip flops and their nature on handling the data.

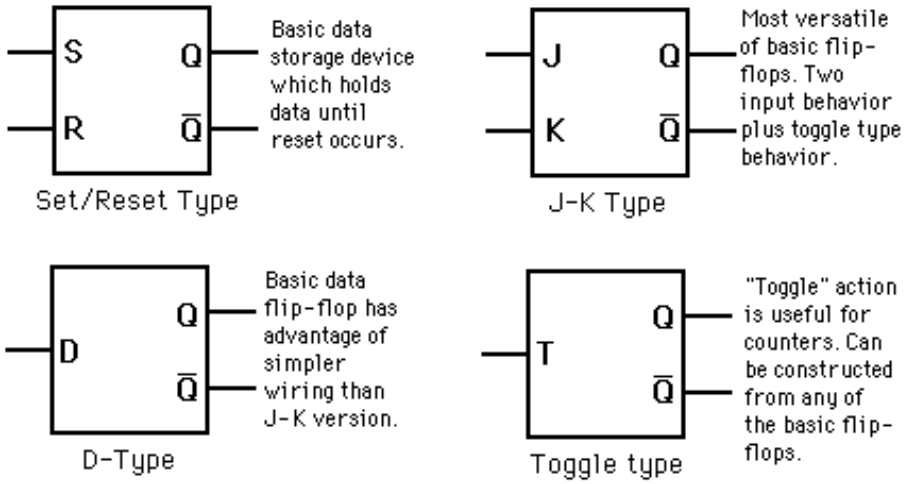

Fig1: Different Types of Flip Flops and their method of handling data

2.2. Counters

Counters are basically designed using ‘set of flip flops’ called registers. Counters are of two types based on the clock provided to the subsequent flip flops with respect to the previous flip

flop. In other words all the flip flops in the counter have the same frequency of clock then they are called ‘Synchronous’. Whereas when subsequent flip flops work on different clock frequencies then those categories of counters are called ‘Asynchronous’.

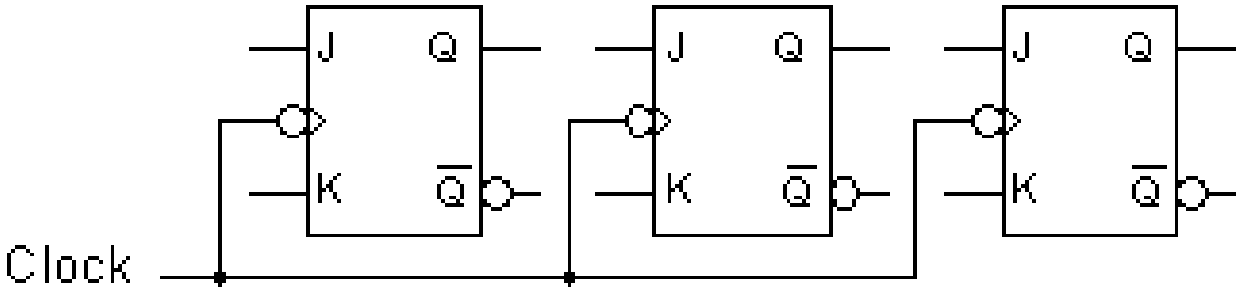

Fig2: Synchronous counter in which same frequency of clock is provided to all the J K Flip Flops

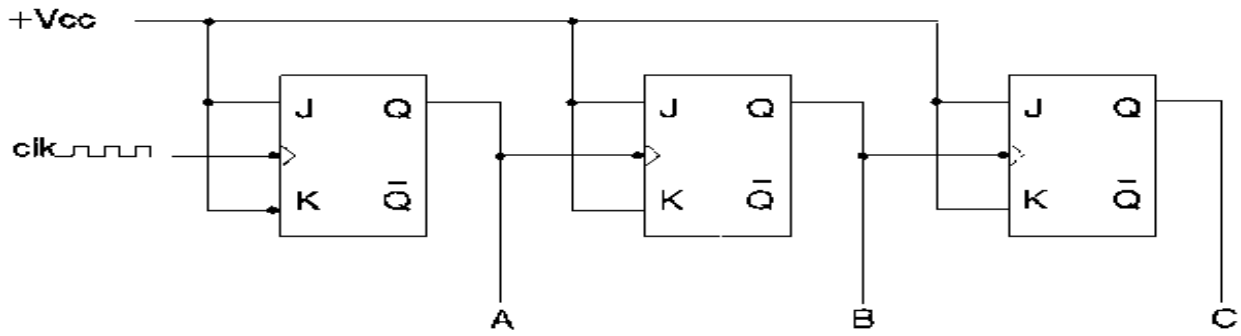

Fig3: Asynchronous counter in which different frequency of clock is provided to all the J K Flip Flops

2.2.1. Ring Counters

Ring Counter are special counters where the output of final flip flop is fed back as input to the first flip flop. For an ‘n’ bit ring counter we have ‘n’ number of flip flops and called a modulo-n counter. It produces 2n states before repeating the states again.

In this project we have designed a 4 bit Johnson Counter which is a special type of Ring Counter using a D Flip flop.

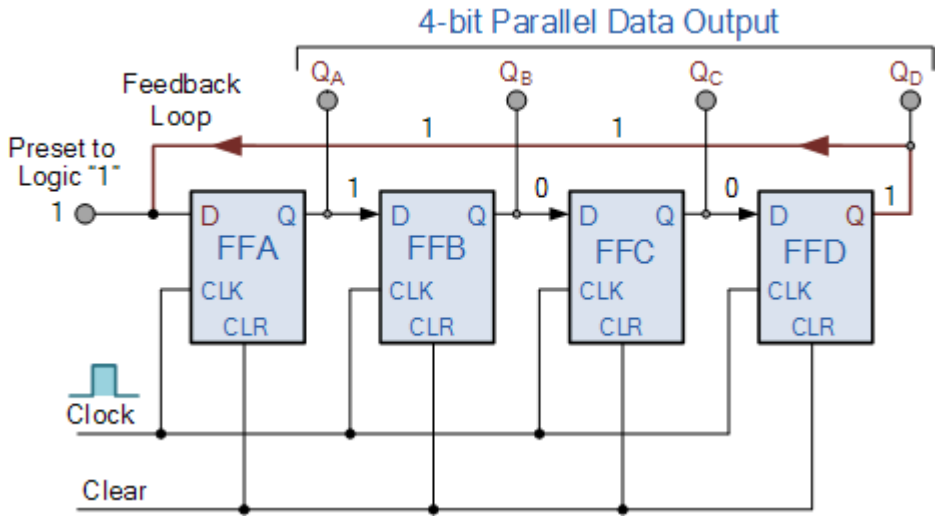

Fig4: 4-bit Ring Counter using D Flip Flop

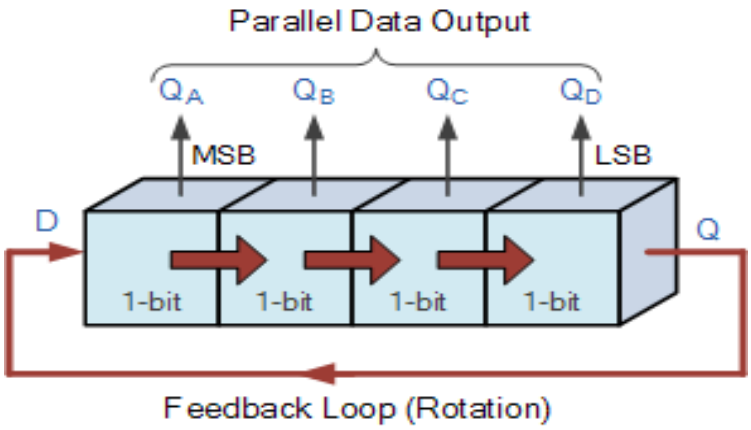

Fig5: Block Diagram of movement of data bit across D Flip Flops in the Ring Counter

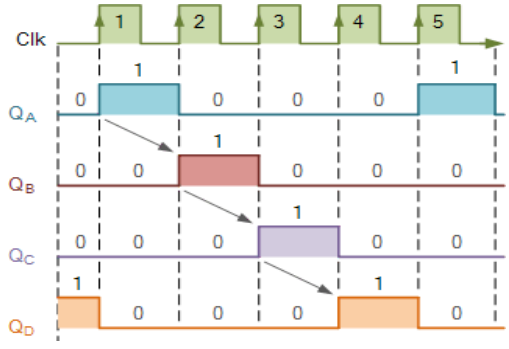

Fig6: Movement of data bit across D Flip Flops in the Ring Counter

3. Approach

We followed the following approach to design a 4 bit Johnson Counter:

Step 1: Design of D flip flop in Cadence

- Basic two input NAND gate and NOT gate schematics using CMOS logic
- The NAND and NOT circuits were simulated and tested for various input combinations.
- The NAND and NOT gates were combined to design a D Flip Flop
- The D flip flop Schematic was simulated and tested for varied input combinations.

Step2: Design of 4 bit Johnson Counter in Cadence

- Four D flip flops were connected sequentially and the complemented output of the final flip flop was fed back as the input to the first flip flop.
- The 4 bit Johnson counter was simulated and tested to observe the 2n=8 states.

Step3: Drawing Schematic for D Flip Flop in Cadence

- The schematic of the D Flip Flop was drawn into a stick diagram based on Euler graph concept.
- The layout was verified by running the Design Rule Checker.

Step4: Extraction

- The layout was extracted.

Step5: Layout to Schematic Check

- Layout vs Schematic was verified using LVS.

4. D Flip Flop

A D flip flop is the flip flop that gives out the input data as it is to the output whenever the clock is enabled. D Flip Flop is a great choice compared to the other as it has only one input to be provided compared to SR and JK flip flop.

In our project we have used a negative edge triggered D flip flop to design our Counter. Then symbol for negative edge triggered D flip flop is as follows:

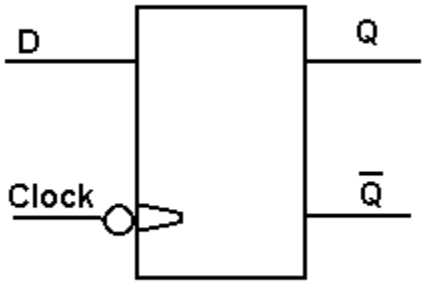

Fig7: Negative edge triggered D Flip Flop

The gate level circuit and the truth table for the negative edge triggered D flip flop is as follows:

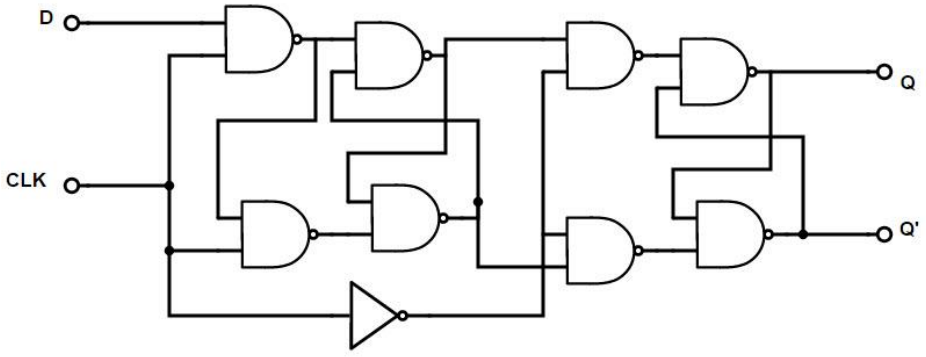

Fig8: Gate Level Circuit of Negative edge triggered D Flip Flop

D	Q	Clk	Qnext
0/1	0/1	X	0/1
1	x	Falling Edge	0
0	x	Falling Edge	1

Table1: Truth Table for Negative Edge Triggered D Flip Flop

5.Johnson Counter

Johnson Counter is basically a special category of ring counters. It is also known twisted tail counter or Mobius counter because the inverted output of the last flip flop is given as input to the first flip flop. This inverted output as input is what characterizes the counting behavior of a Johnson Counter.

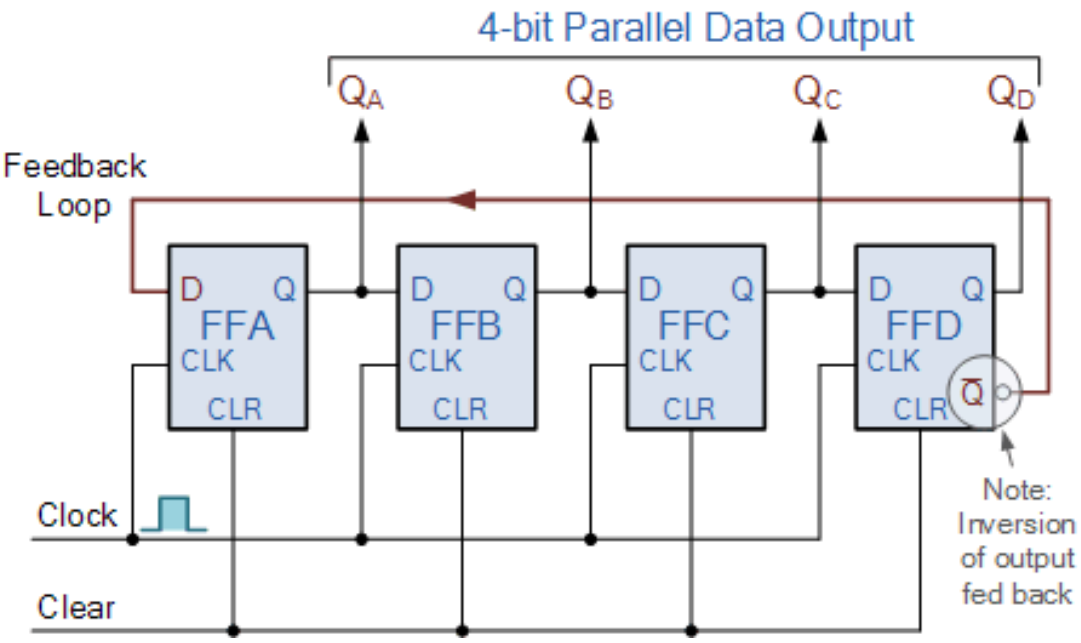

Fig9: 4-bit Johnson Counter

If a Johnson Counter has n flip flops it counts 2n stages after which it repeats the sequence. In our project we used a 4-bit Johnson counter that counts upto 2n=8states. Figure depicts the truth table for a 4-bit Johnson's Counter.

As observed from the Table 2 the at the fist clock cycle all the outputs are one. During the second cycle the inverted output of the final flip flop i.e. 0 is fed into the first flip flop. This 0 shifts its position from the least significant bit to the most significant bit. Similarly the inputs which follow move in a ring pattern and repeats itself after eight clock cycles.

One of the major advantages of a Johnson Counter is that it can count up to 2n states with just half the number of flip flops as other ring counters. But Johnson Counter also come at the cost of extra hardware to decode it stages. This put Johnson Counter somewhere in the middle ground between ring and binary counters.

Clock Pulse Number	FFA	FFB	FFC	FFB
0	0	1	1	1
1	0	0	1	1
2	0	0	0	1
3	0	0	0	0
4	1	0	0	0
5	1	1	0	0
6	1	1	1	0
7	1	1	1	1

Table2: Truth Table for 4-bit Johnson Counter

6. VLSI Schematic for 4-bit Johnson Counter

We split the 4 bit Johnson counter into individual D flip flops. The D flip flops were further broken down into eight 2-input NAND gates and one inverter.

6.1. NOT Gate

The schematic, symbol, test bench and graph of the NOT gate was drawn as follows:

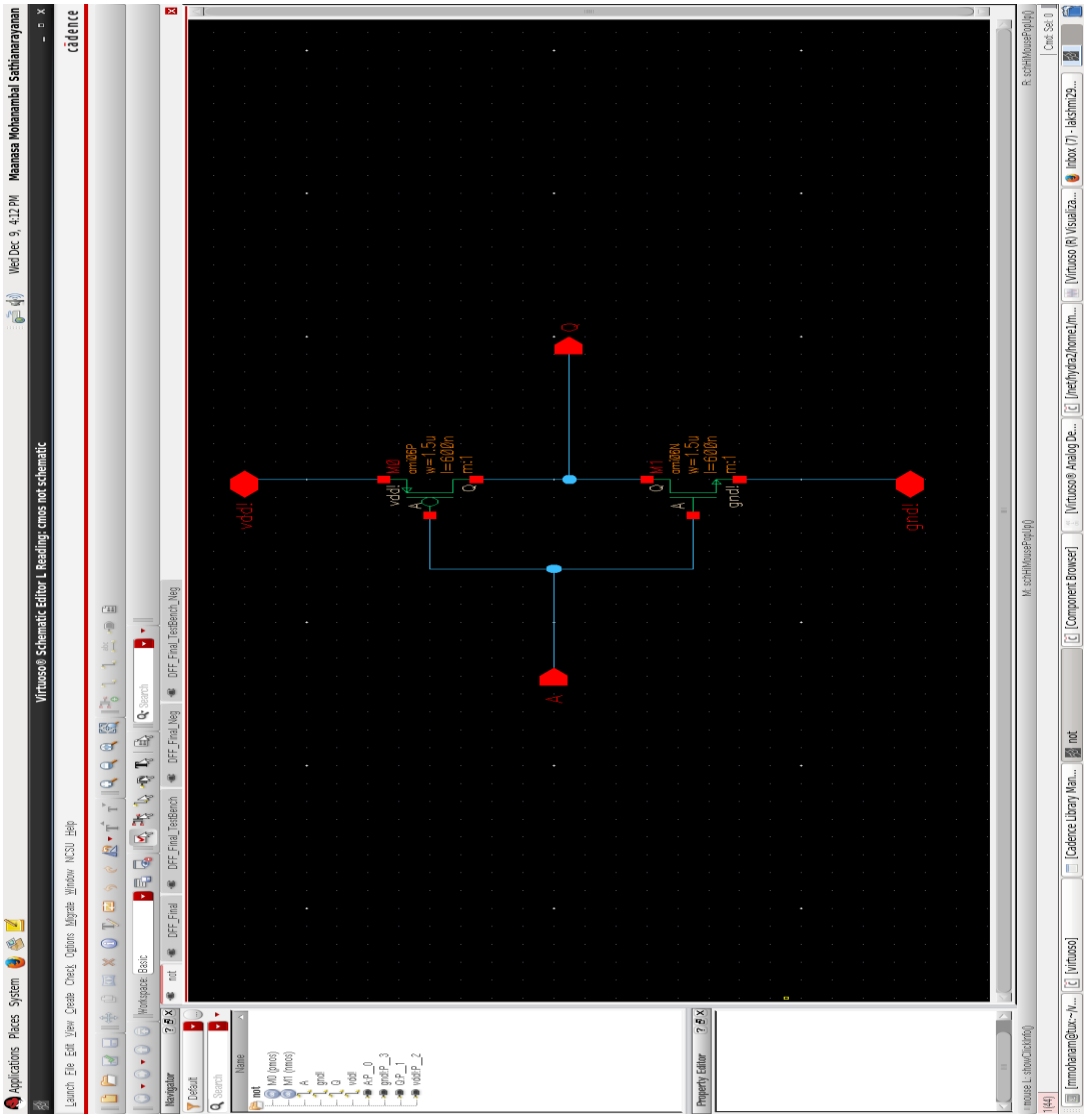

Fig1: Schematic of NOT Gate

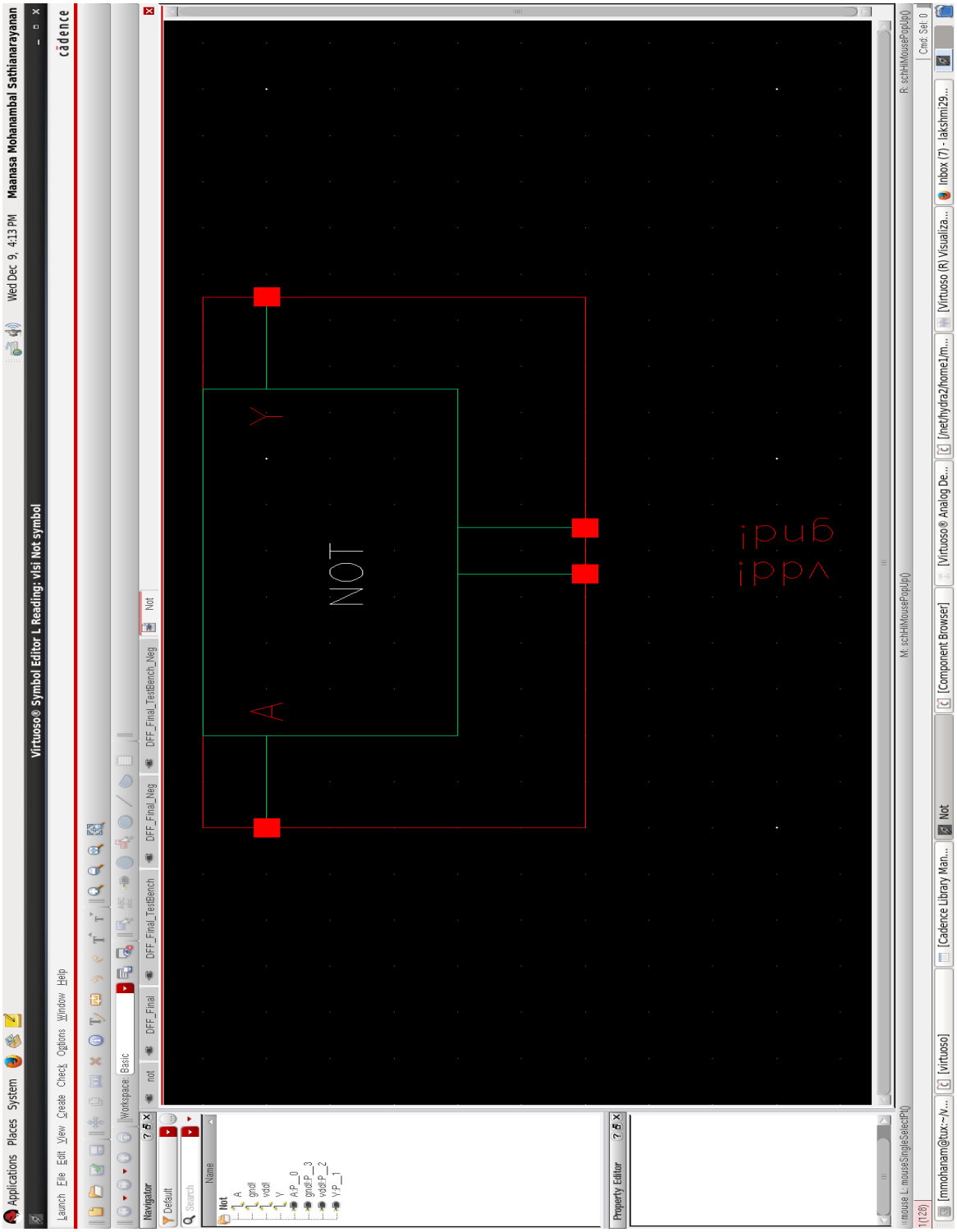

Fig2: Symbol of NOT Gate

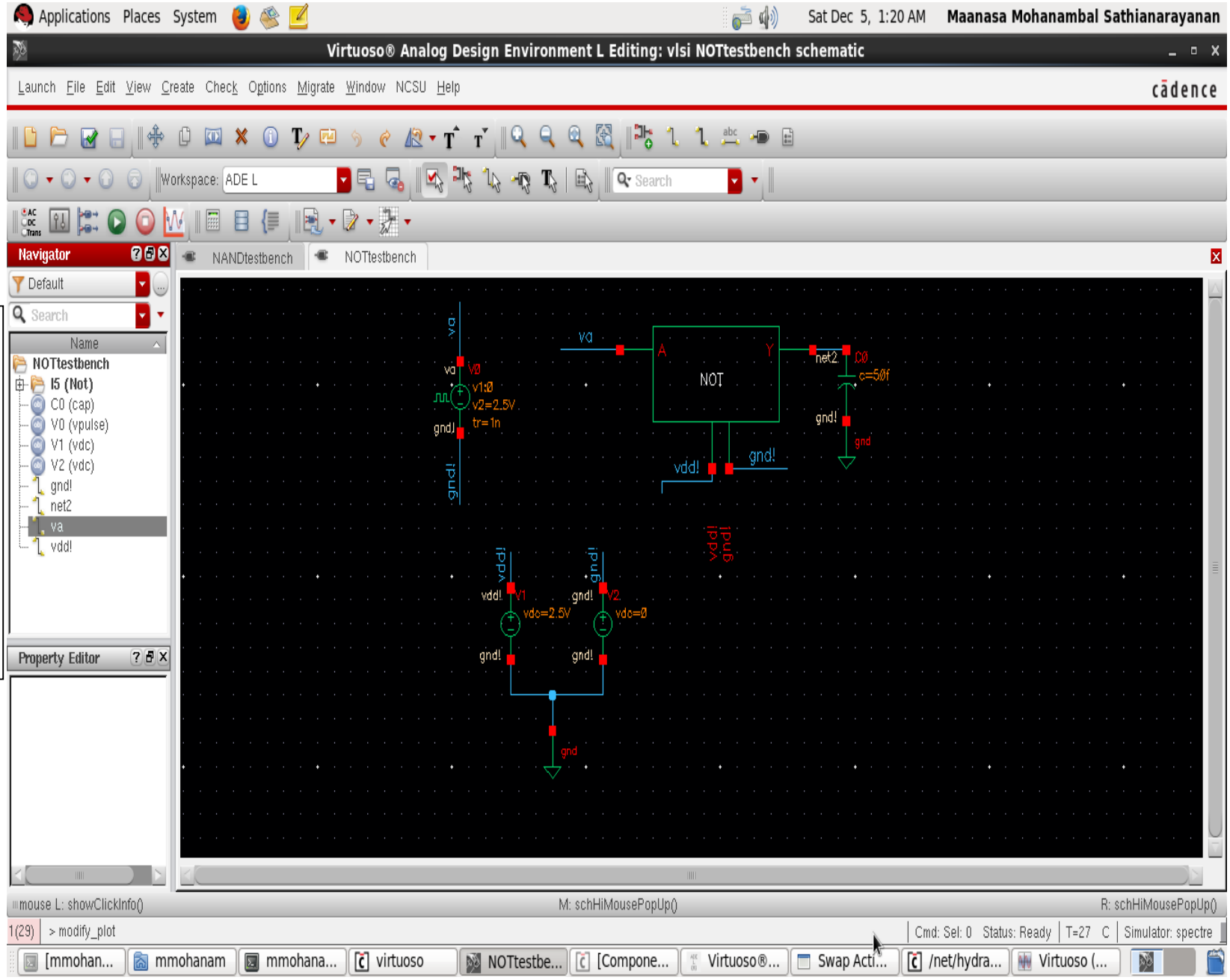

Fig3: Test Bench for NOT Gate

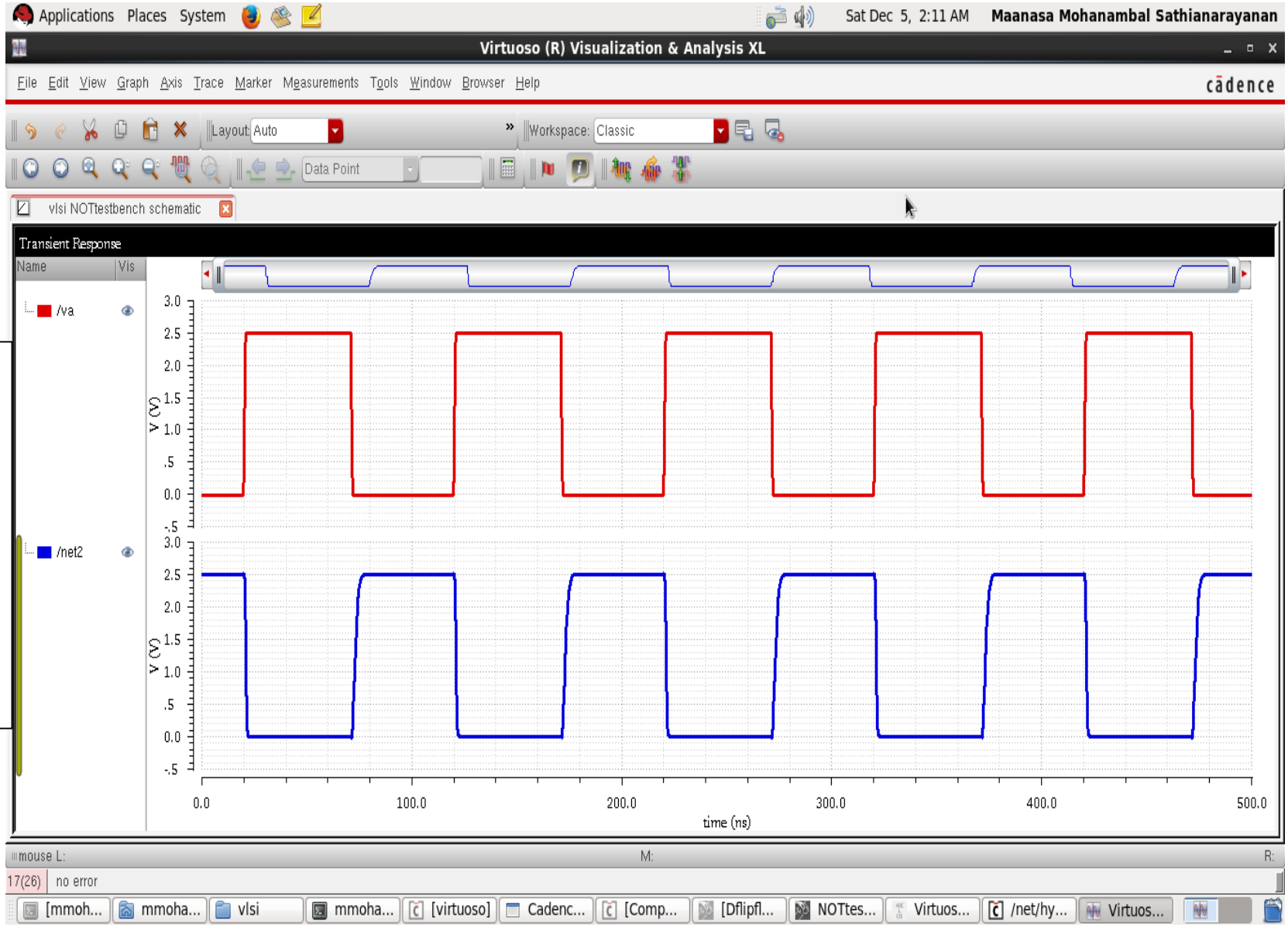

Fig4: Graph for NOT Gate

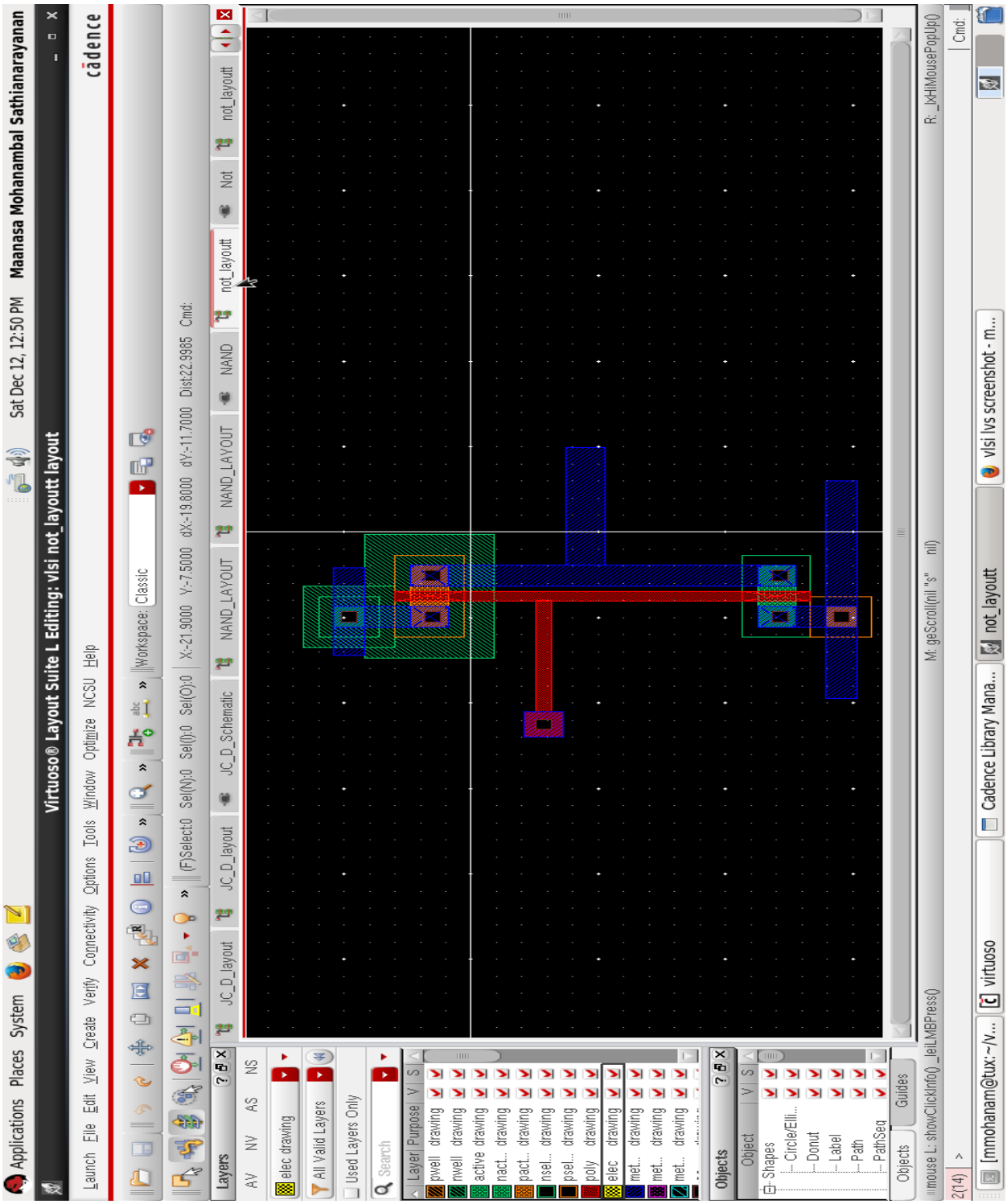

Fig5 : Layout of NOT Gate

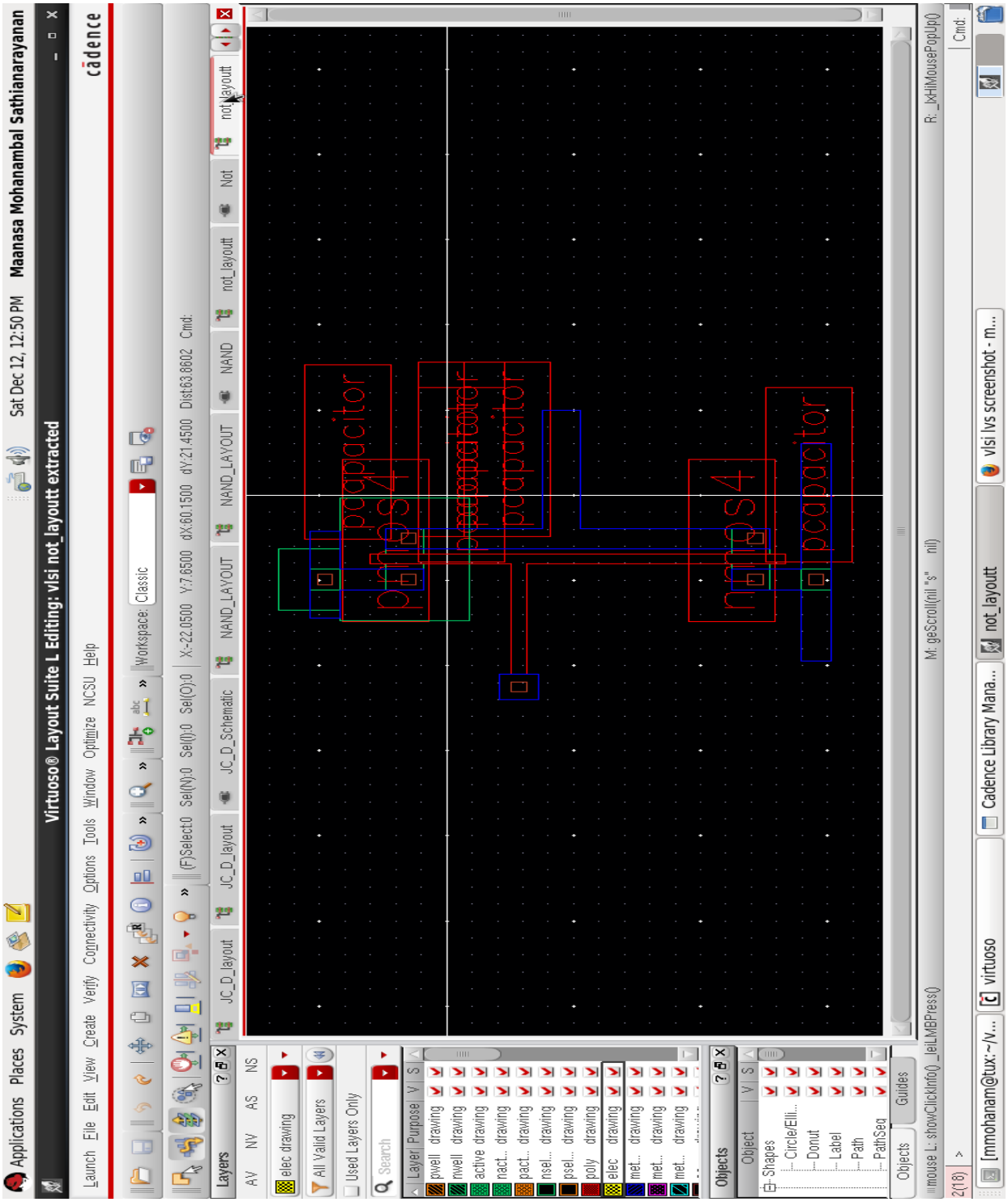

Fig6: Extract of NOT Gate

Fig7 : Net List of NOT Gate

Fig8: LVS Match for NOT Gate

6.2. Two input NAND Gate

The schematic, symbol, test bench and graph of the NAND gate was drawn as follows:

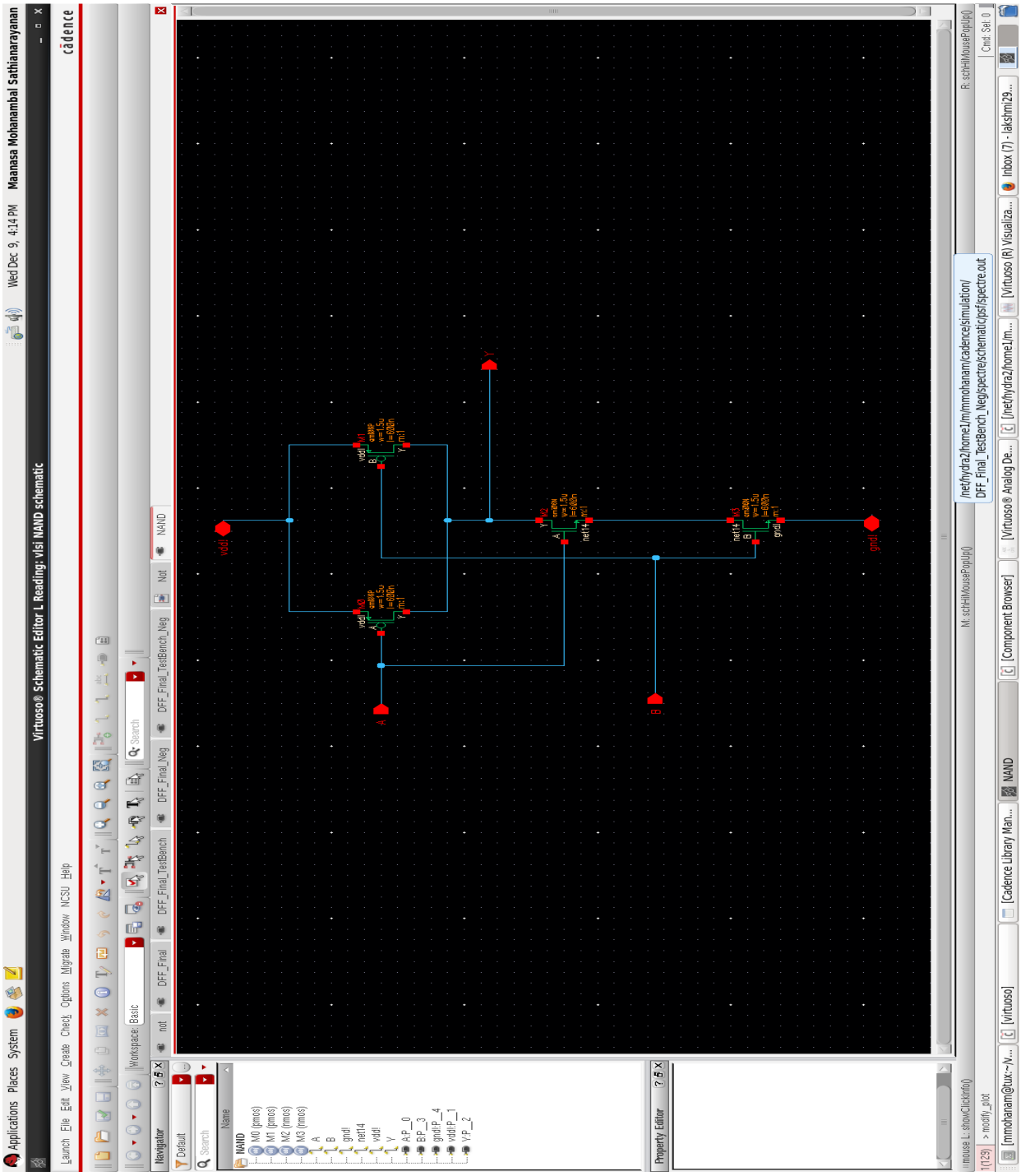

Fig9: Schematic of NAND Gate

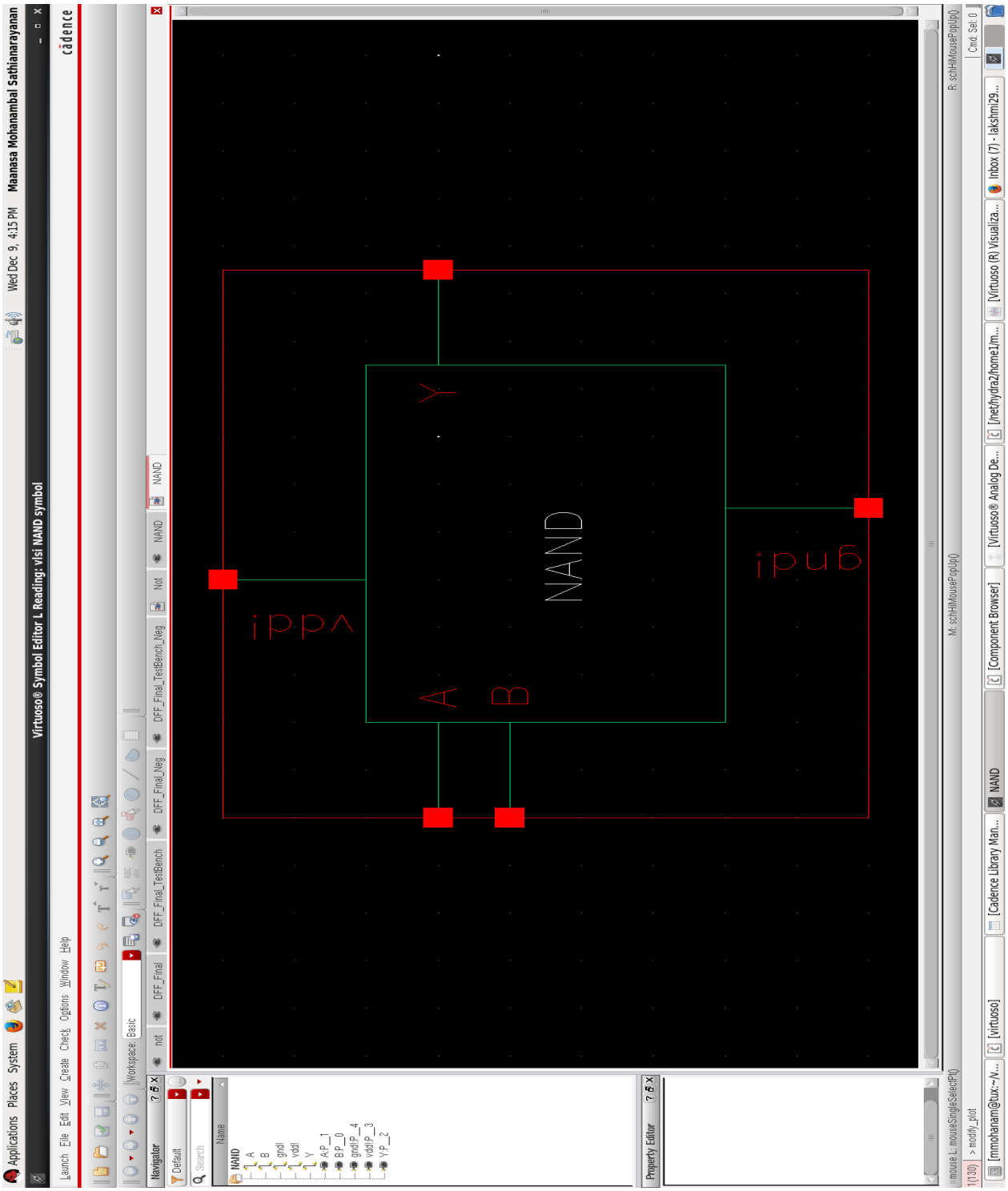

Fig10: Symbol of NAND Gate

Fig11: Test bench of NAND Gate

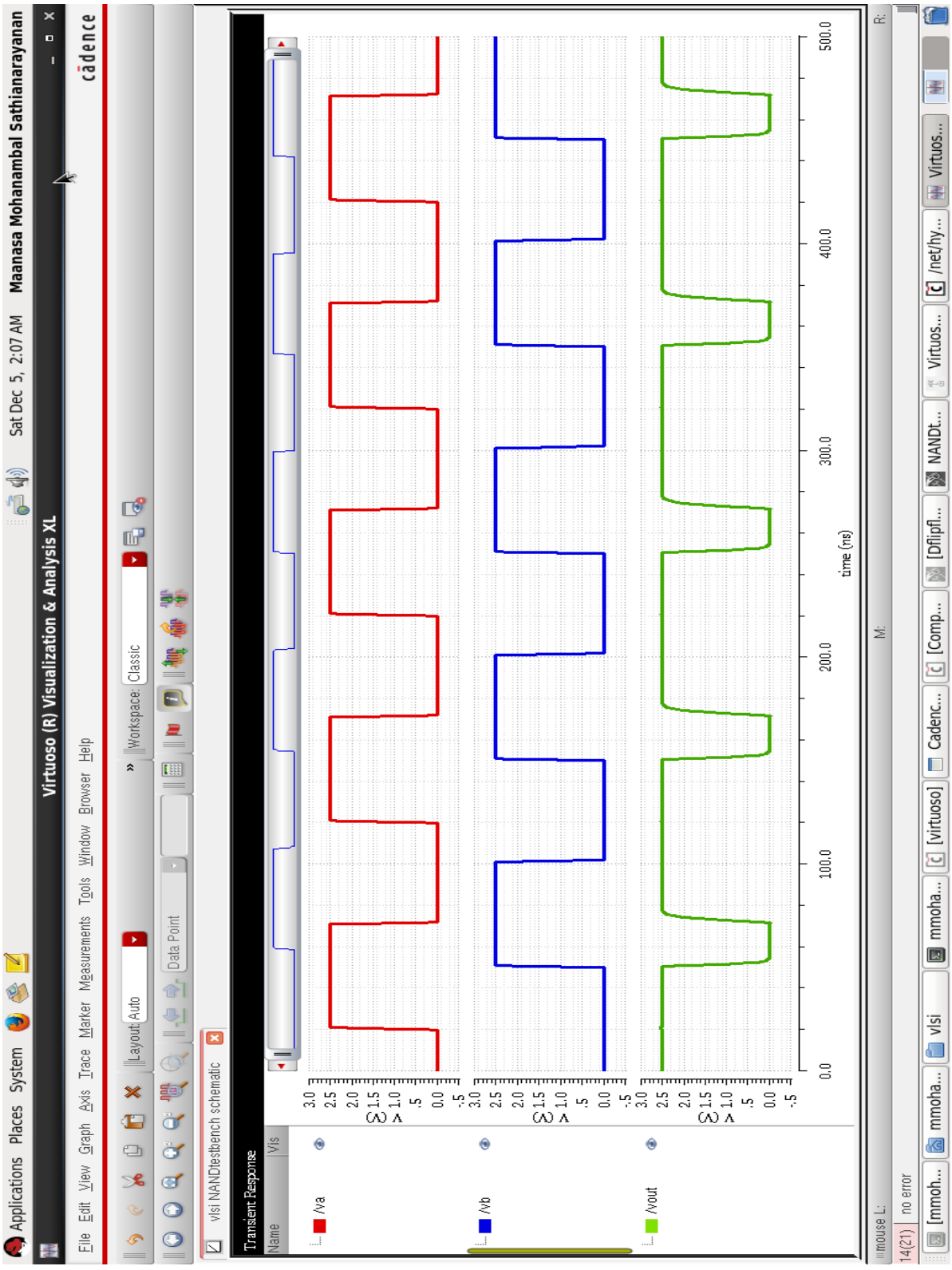

Fig12: Graph of NAND Gate

Fig13 : Layout of NAND Gate

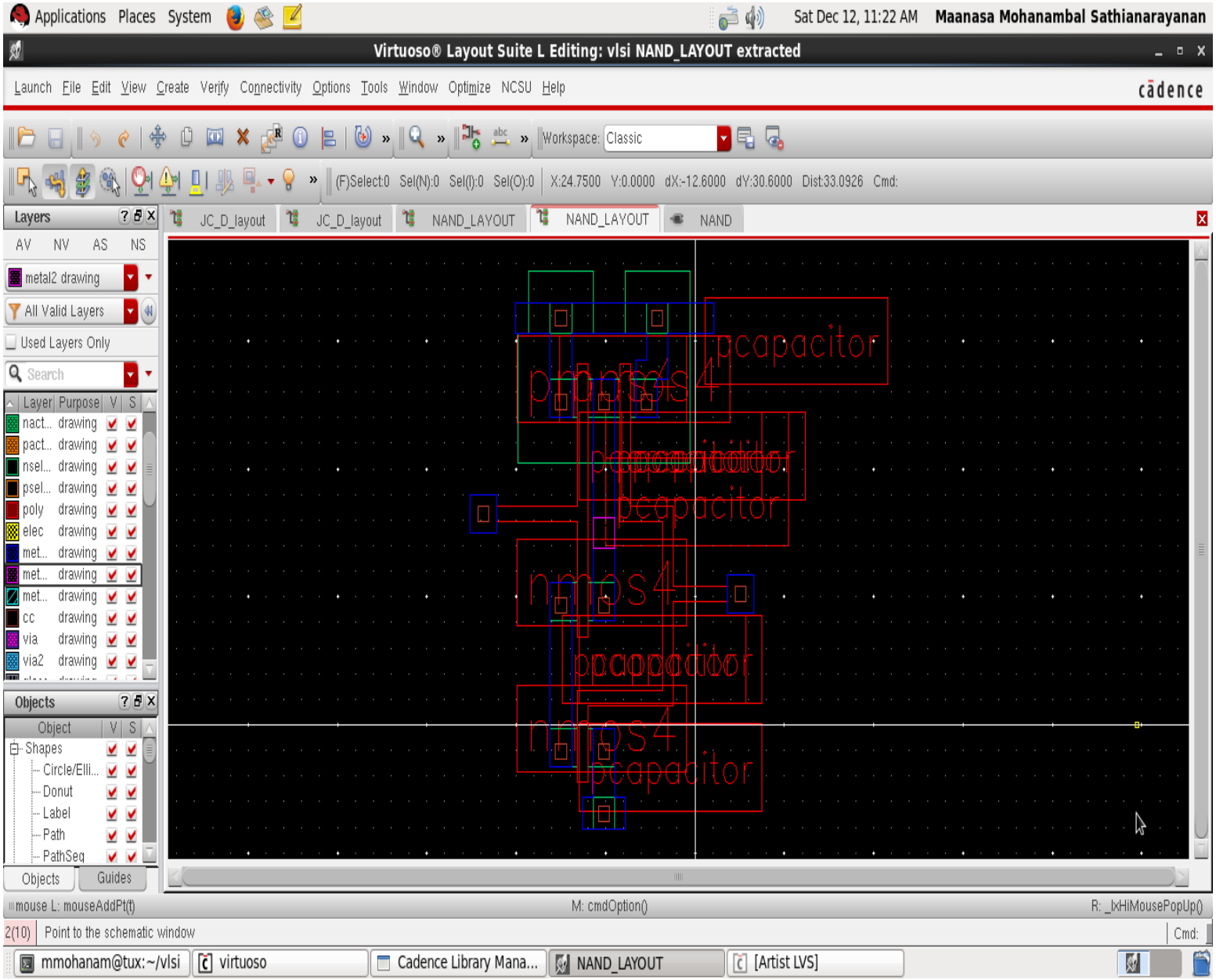

Fig14: Extracted View of NAND Gate

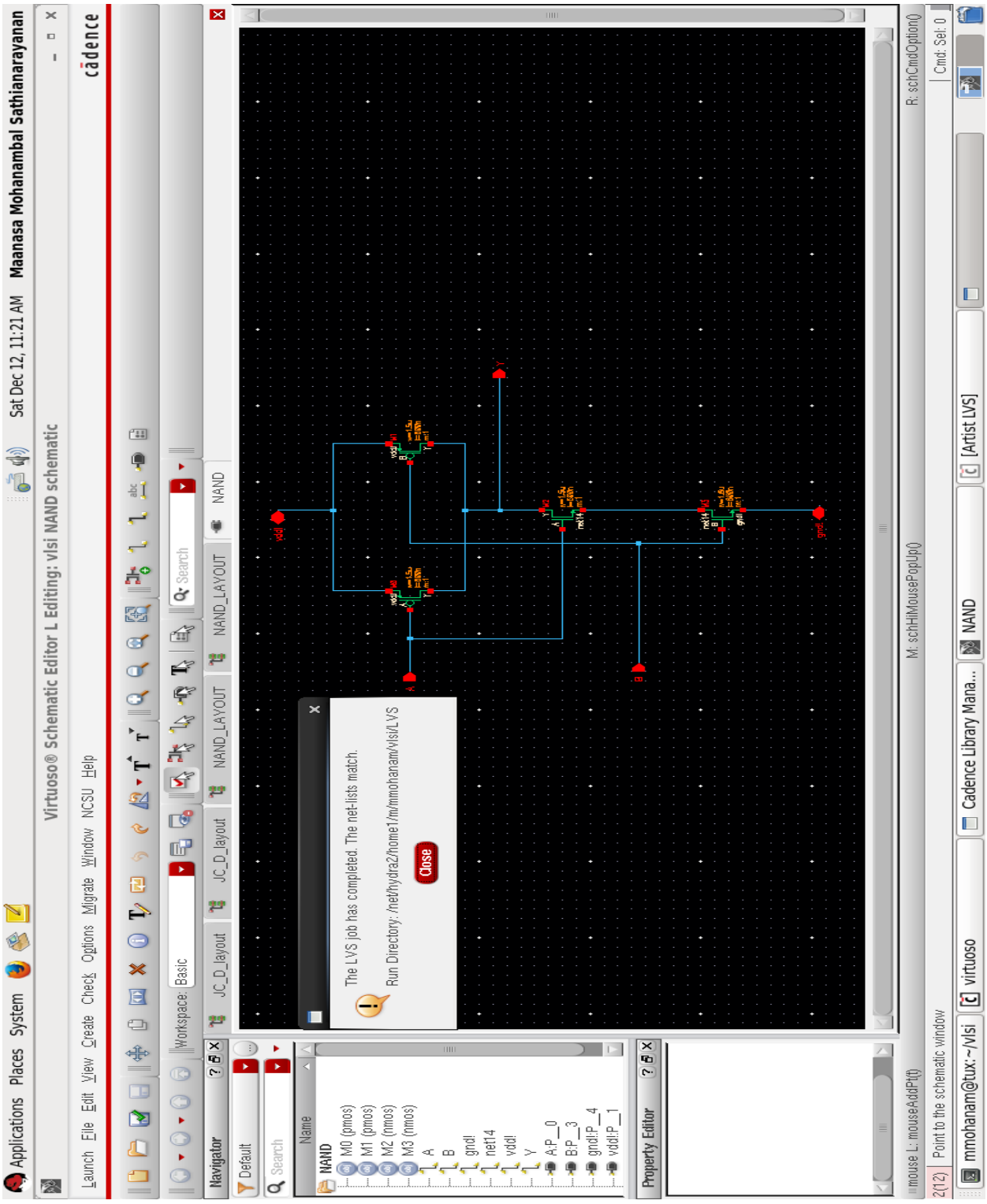

Fig15 : LVS Match for NAND Gate

6.3. Negative Edge Triggered D Flip Flop

The schematic, symbol, test bench and graph of the Negative Edge Triggered D Flip Flop was drawn as follows:

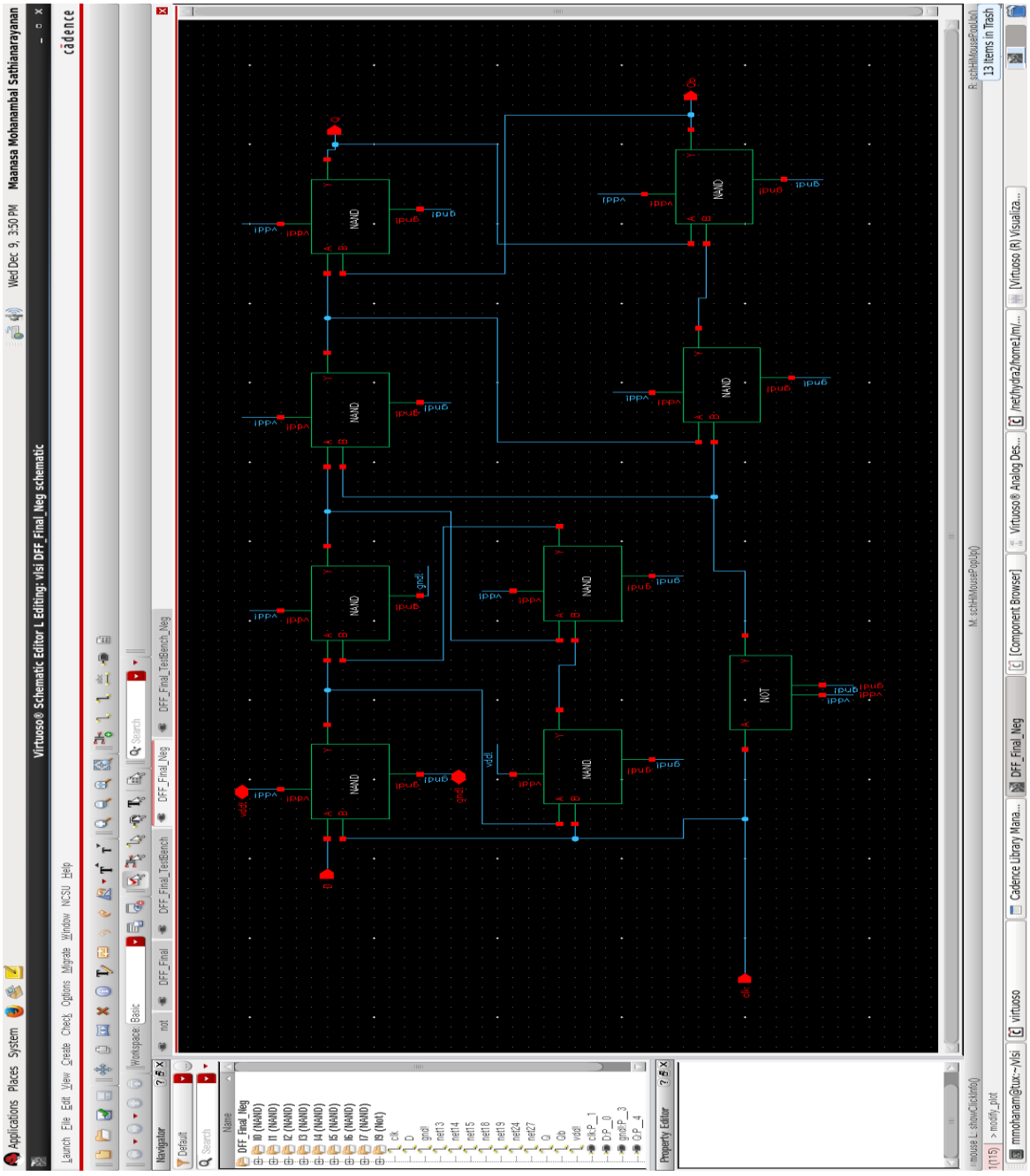

Fig16: Schematic of D Flip Flop

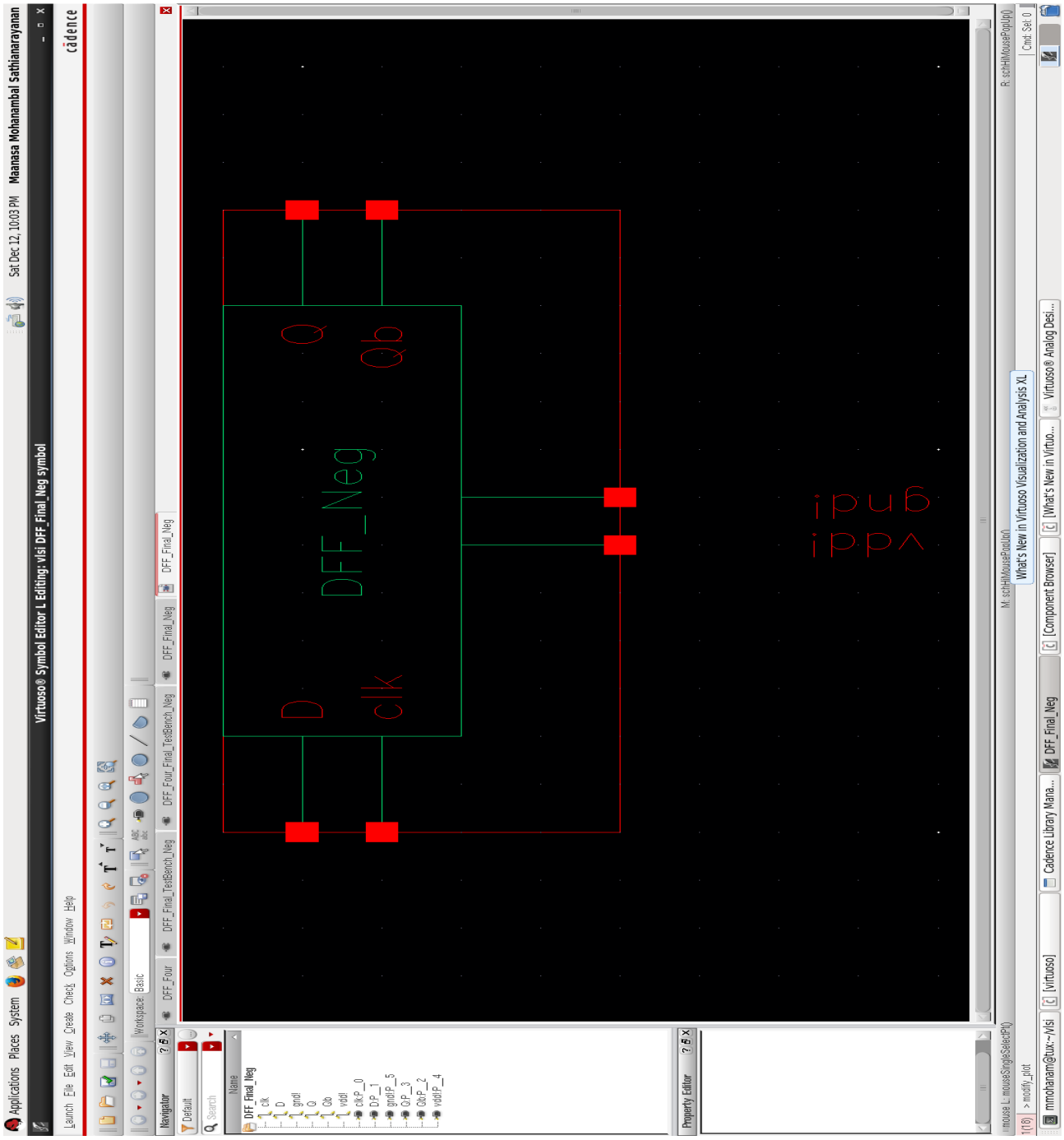

Fig17: Symbol of D Flip Flop

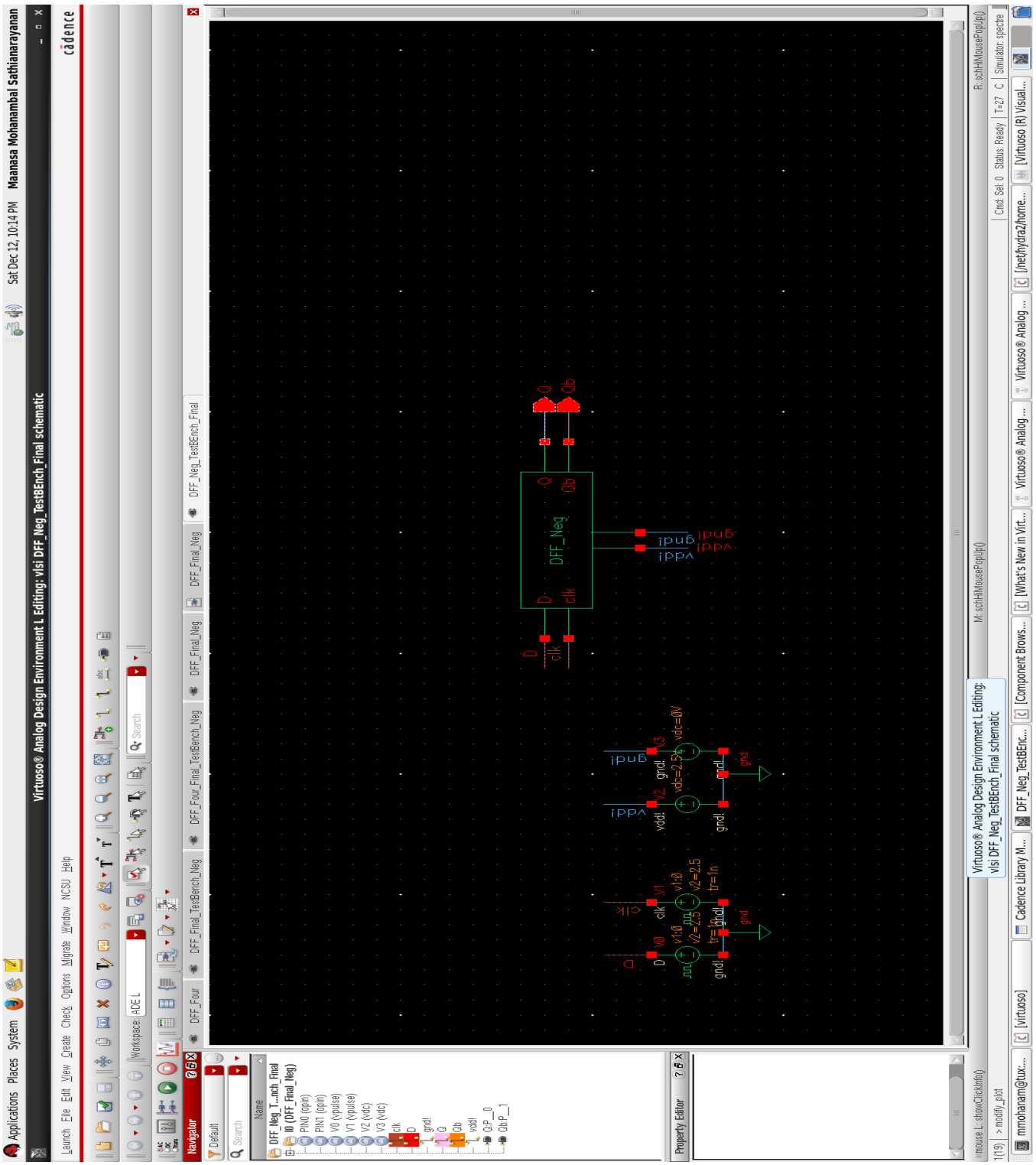

Fig18: Test bench for D Flip Flop

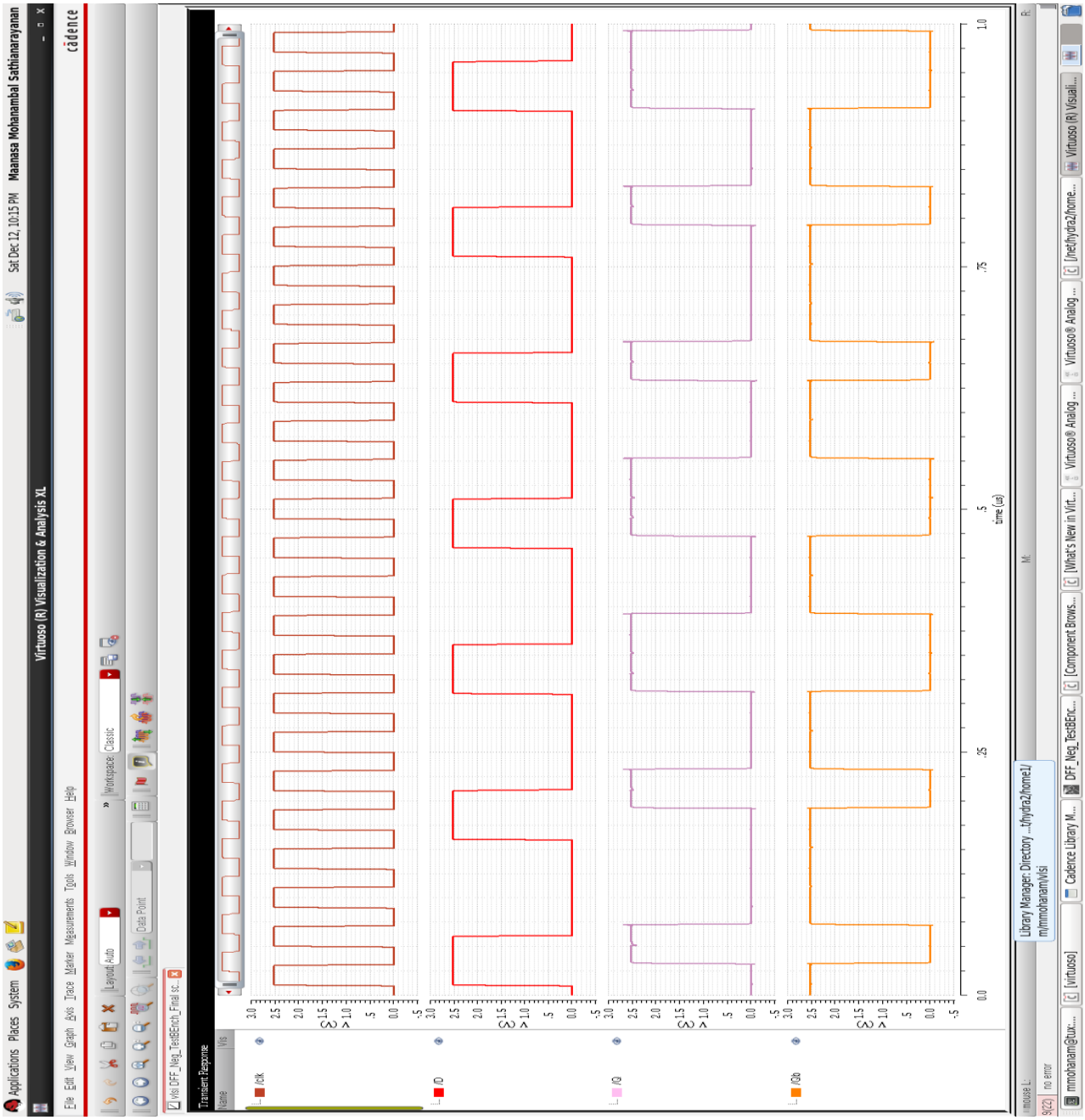

Fig19 : Graph of D Flip Flop

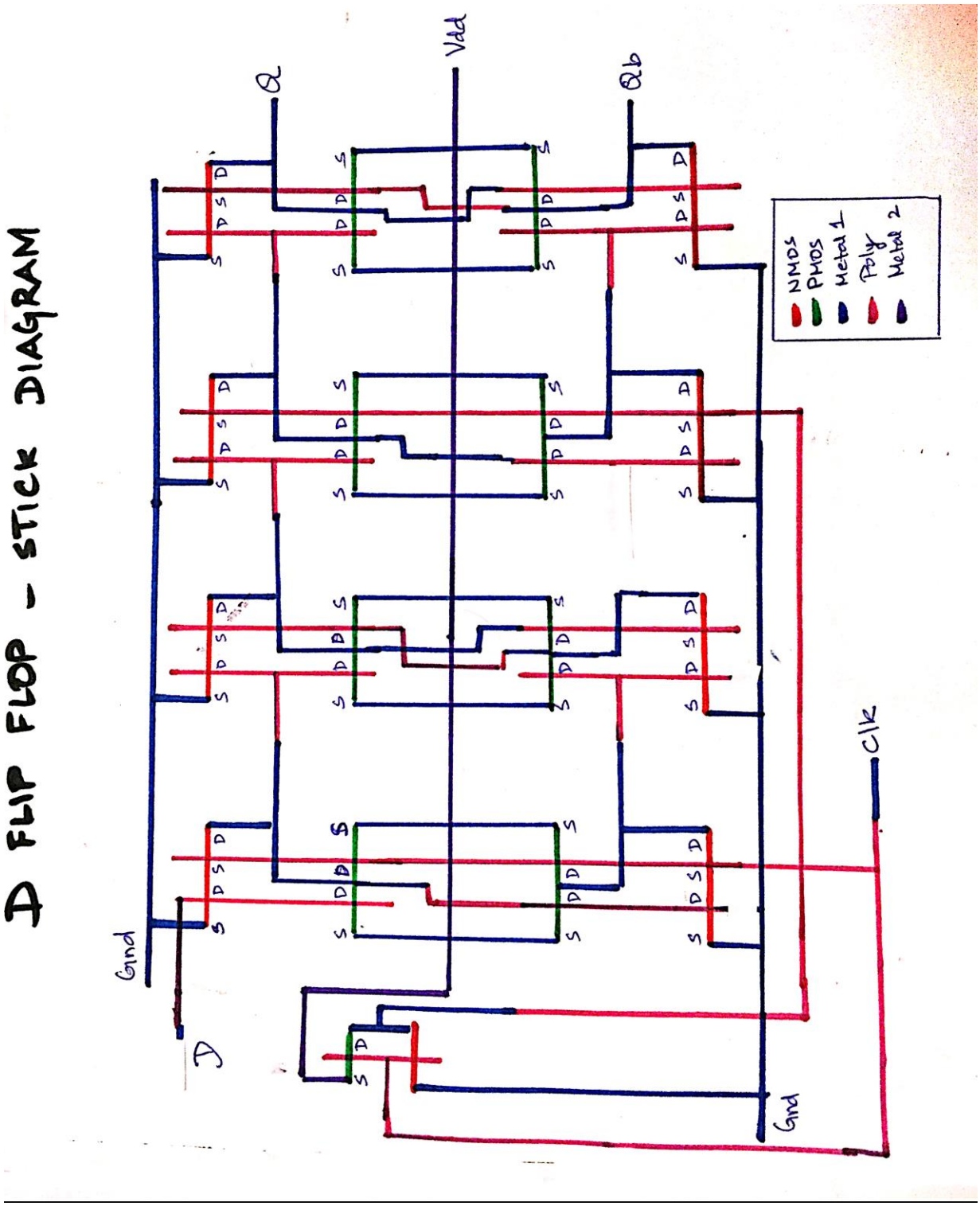

Fig20 : Stick diagram of Negative Edge Triggered D Flip Flop

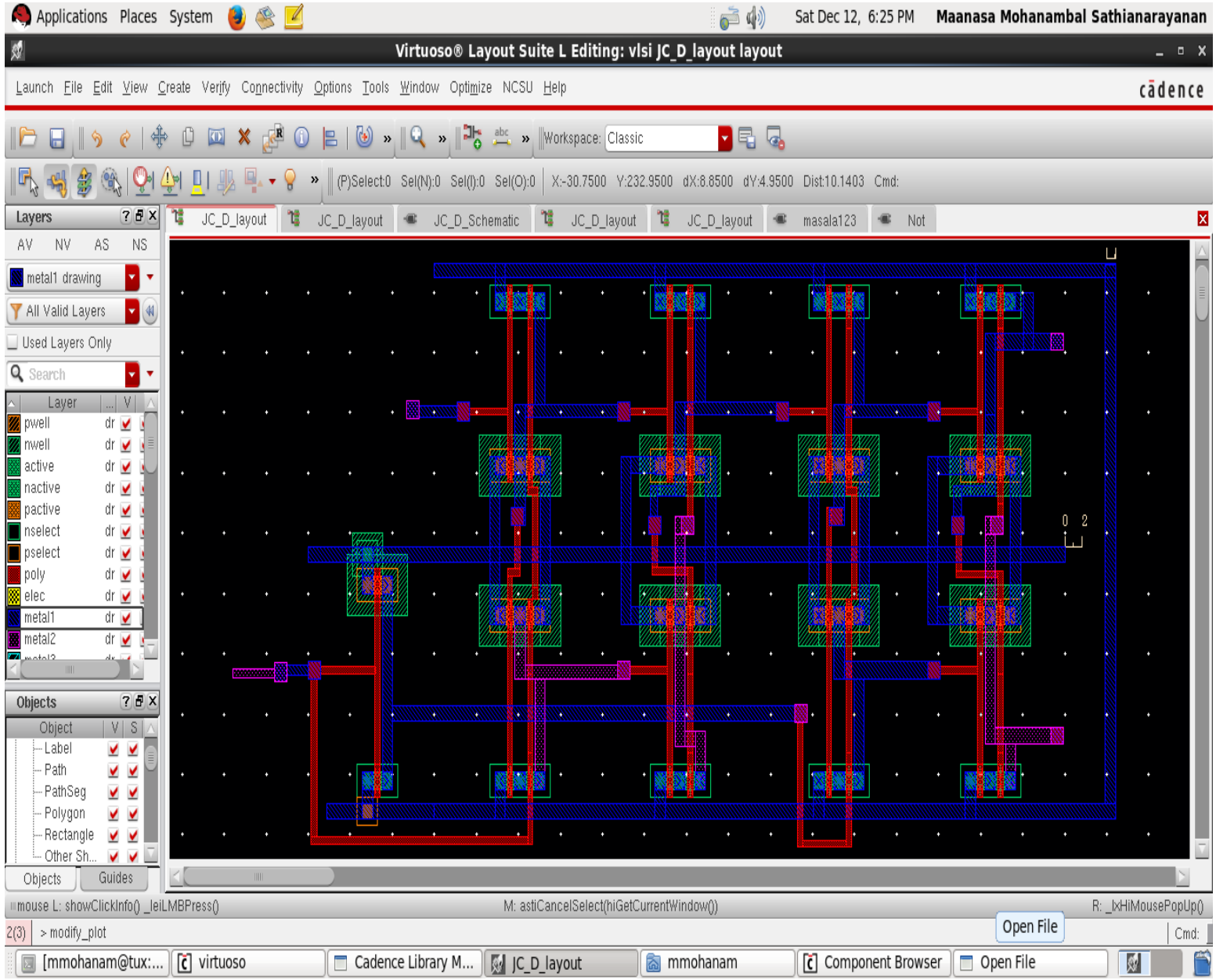

Fig21 : Layout of D Flip Flop

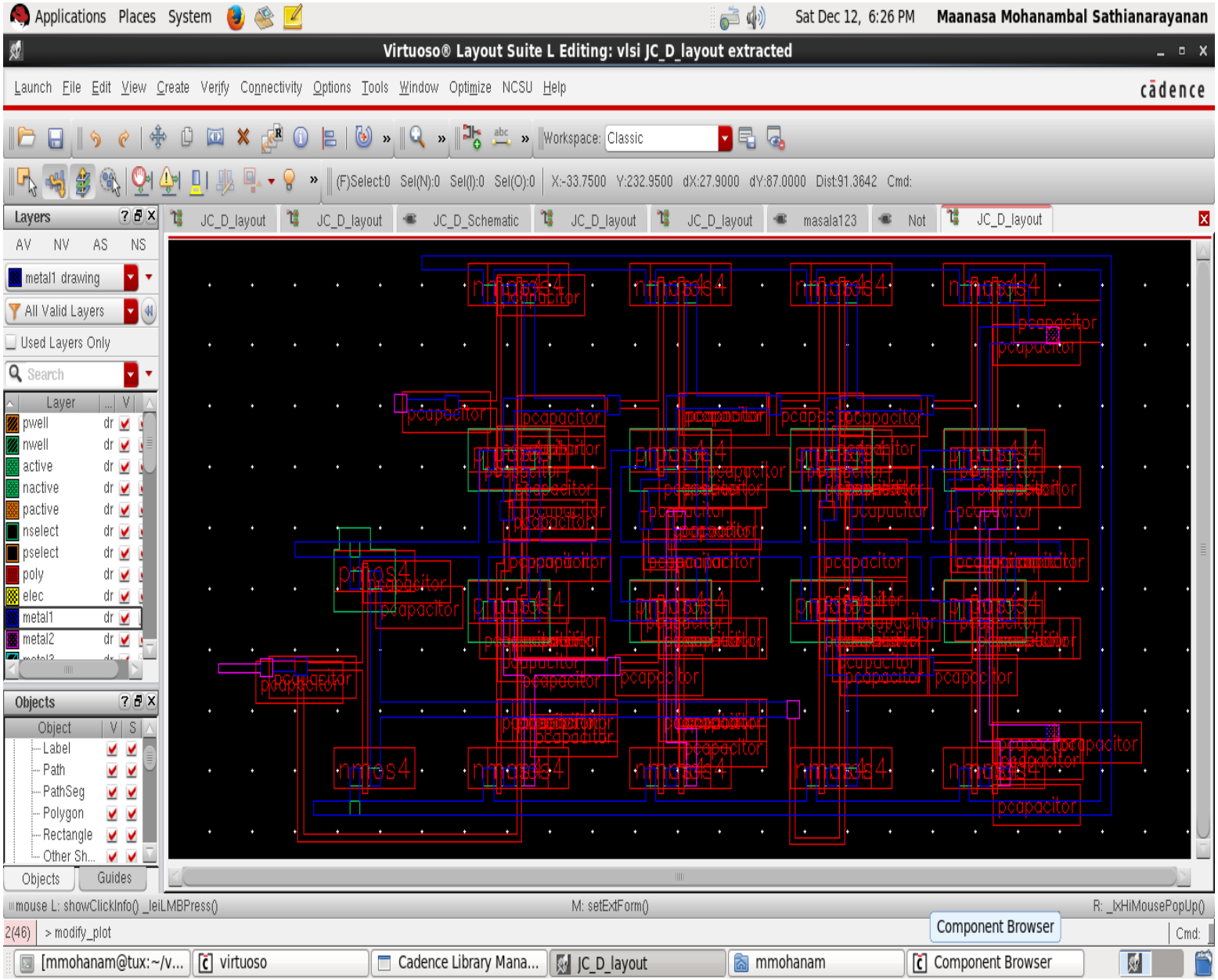

Fig22 : Extracted View of D Flip Flop

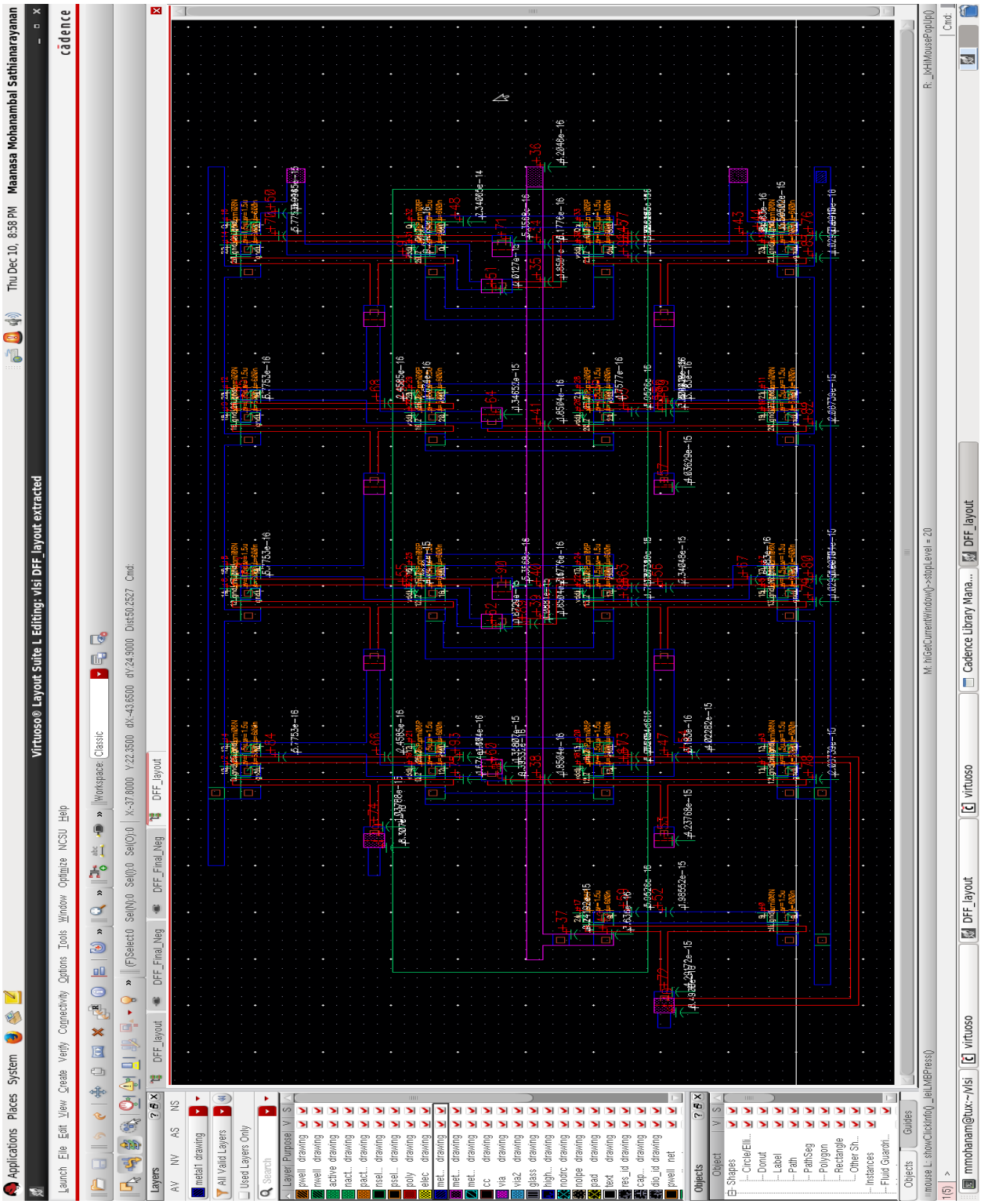

Fig23 : Net List of D Flip Flop

6.4. 4 Bit Johnson Counter

The schematic, symbol, test bench and graph of the 4 bit Johnson Counter was drawn as follows:

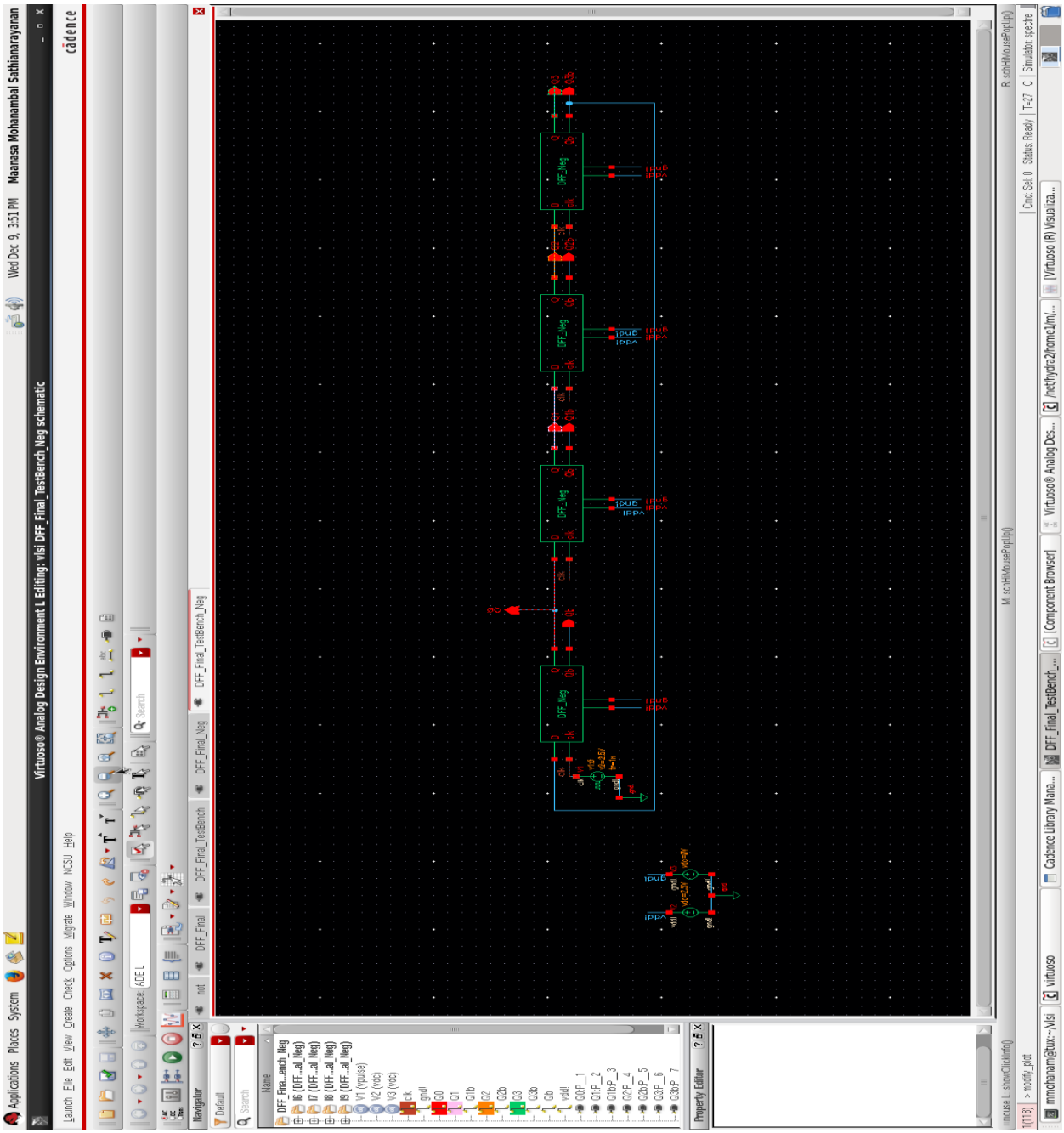

Fig24: Schematic of 4 Bit Johnson Counter

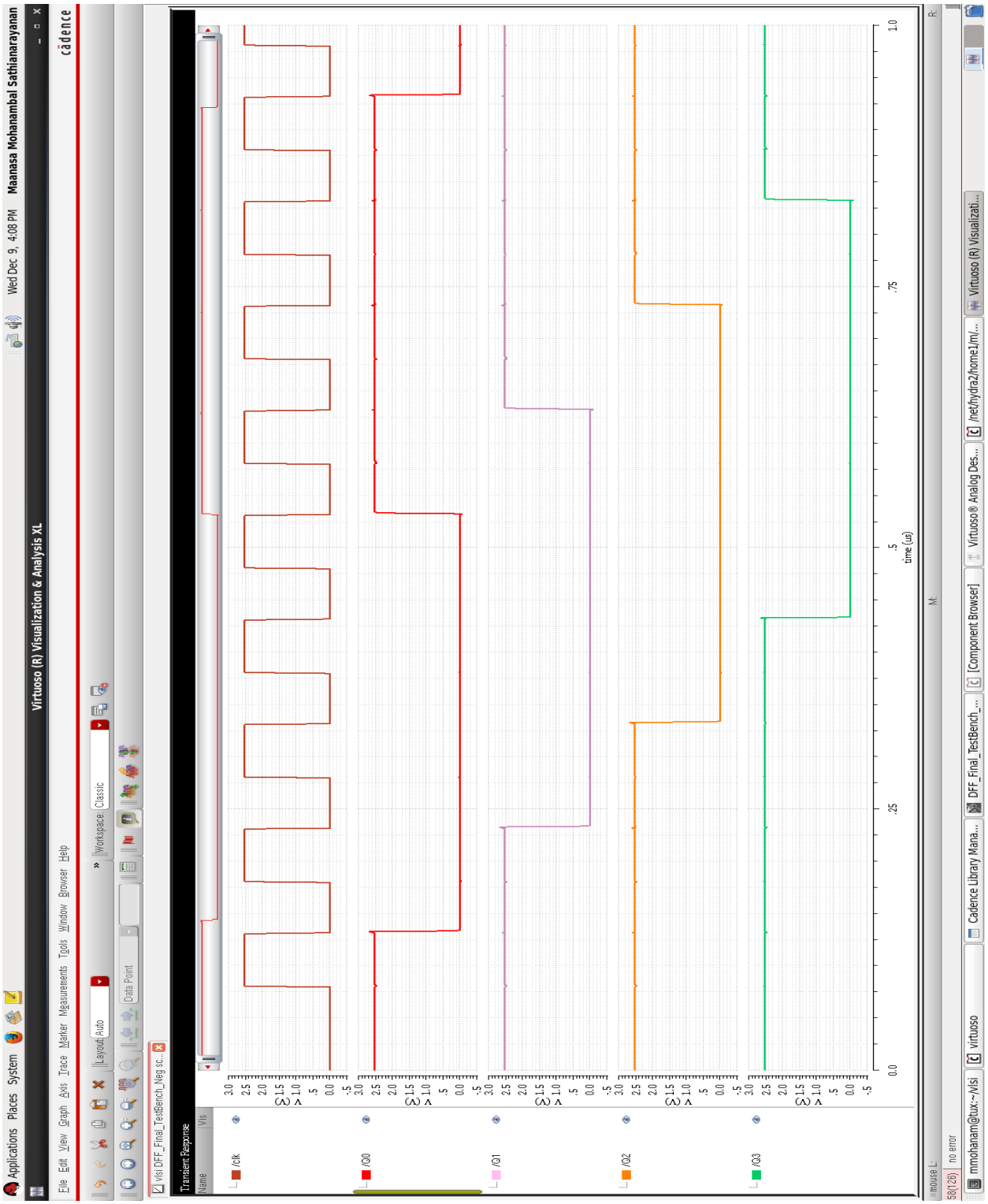

Fig25 : Graph of 4 Bit Johnson Counter

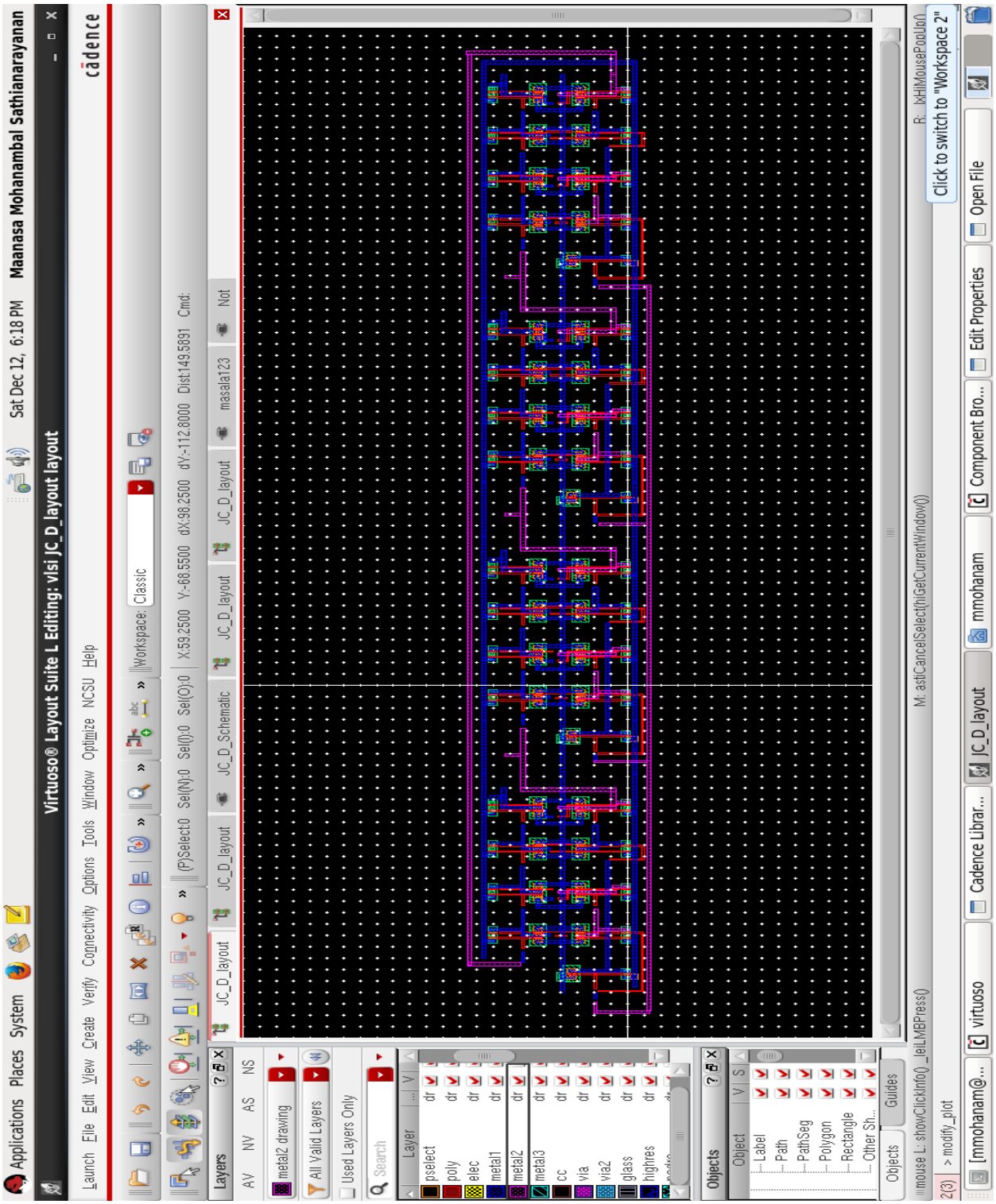

Fig26 : Layout of 4 Bit Johnson Counter

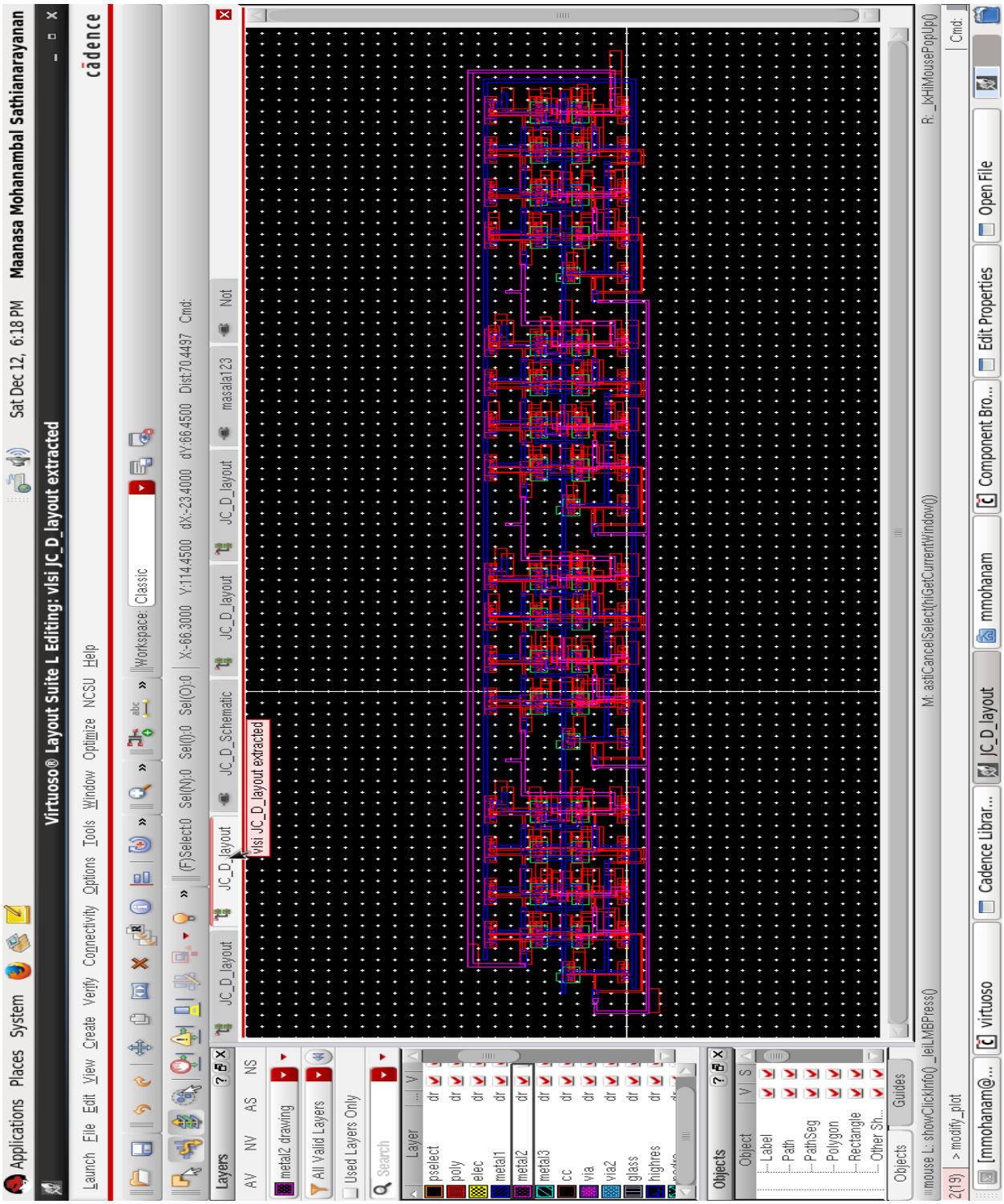

Fig27 : Extracted View of 4 Bit Johnson Counter

7. Applications of a Johnson Counter

Standard 2, 3 or 4-stage Johnson Ring Counters can be used to divide the frequency of signal by varying their feedback connections and divide-by-3 or divide-by-5 outputs are also available. For example, a 3-stage Johnson Ring Counter could be used as a 3-phase, 120 degree phase shift square wave generator by connecting to the data outputs at A, B and NOT-B. The standard 5-stage Johnson counter such as the commonly available CD4017 is generally used as a synchronous decade counter/divider circuit. Other combinations such as the smaller 2-stage circuit which is also called a “Quadrature” (sine/cosine) Oscillator or Generator can be used to produce four individual outputs that are each 90 degrees “out-of-phase” with respect to each other to produce a 4-phase timing signal as shown below.

References

[1]http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/flipflop.html

[2]http://www.physics.mcmaster.ca/phy4d6/Lab/chapter7.htm

[3]www.nzdl.com

[4]https://www.bing.com/images/search?q=neg+edge+triggered+d+flip+flop+truth+table&view=detailv2&qpvt=neg+edge+triggered+d+flip+flop+truth+table&id=9B4ED454CA8BFF4507D87E181F85191ACC6812C7&selectedIndex=5&ccid=zTu5AOOb&simid=608008967246644220&thid=OIP.Mcd3bb900e39b53186d9e37cfed9fb808o0&ajaxhist=0

[5]http://www.electronics-tutorials.ws/sequential/seq_6.html