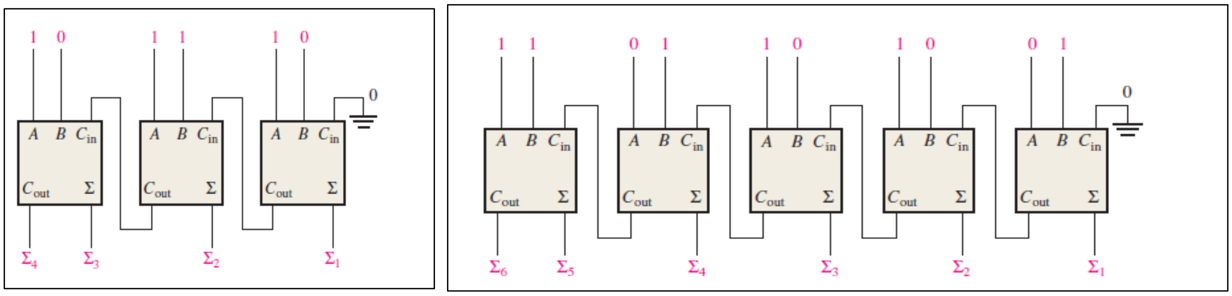
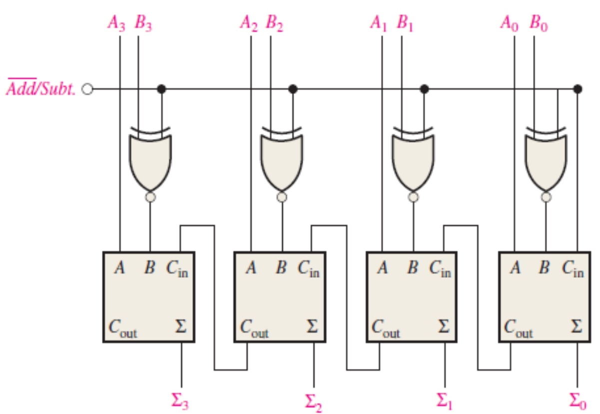
Assignment- 3

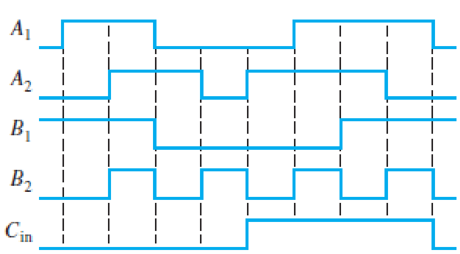
1. For the parallel adder in Figure, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.



2. The circuit shown in Figure is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a) Explain what happens when the *Add*/*Subt*. input is HIGH. (b) What happens when *Add*/*Subt*. is LOW? (c) assume the inputs are *Add*/*Subt*. 5 1, *A* = 1010, and *B* = 1101. What is the output?



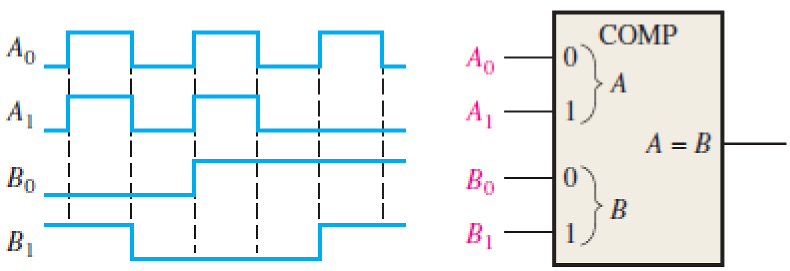
3. The input waveforms in Figure are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.



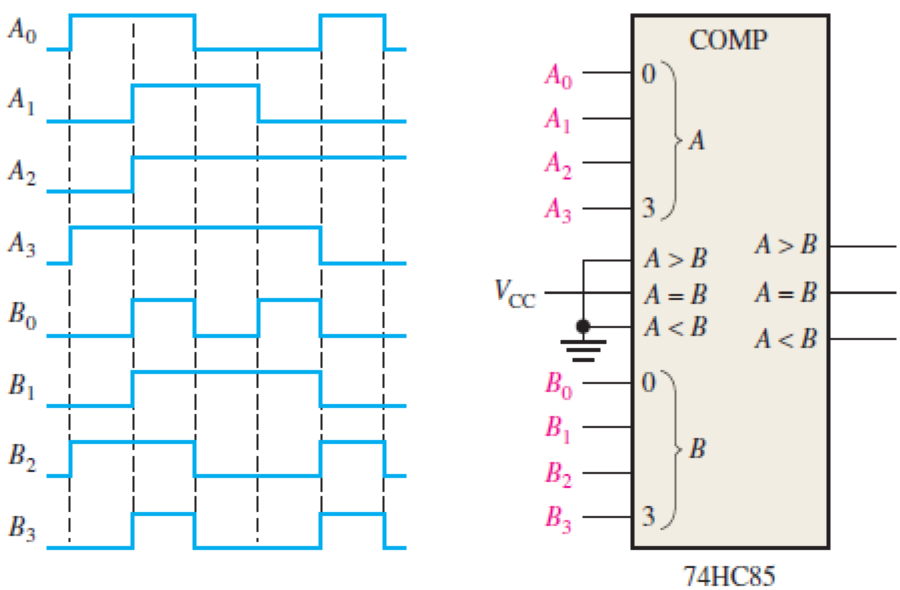
4. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

5. The waveforms in Figure are applied to the comparator as shown. Determine the output ($A = B$) waveform.

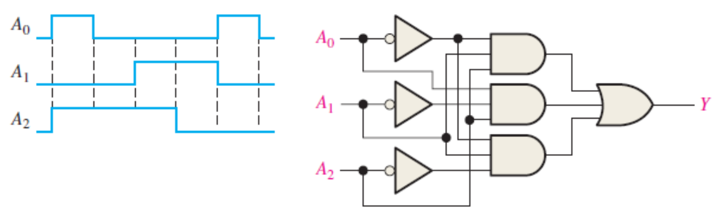


6. For the 4-bit comparator in Figure, plot each output waveform for the inputs shown. The outputs are active-HIGH.

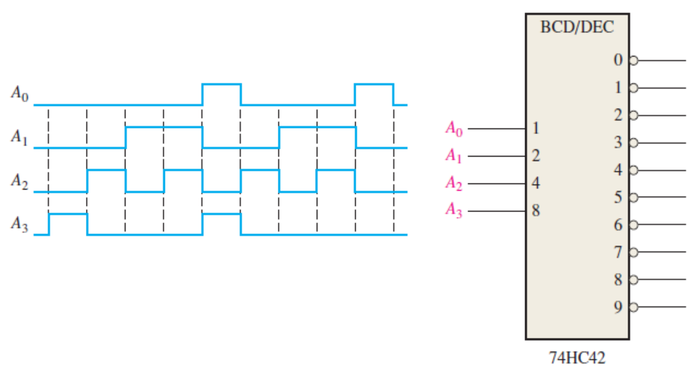


7. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required: (a) 1101 (b) 1000 (c) 11011 (d) 11100
8. Solve above Problem, given that an active-LOW (0) output is required.
9. You wish to detect only the presence of the codes 1010, 1100, 0001, and 1011. An active-HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be LOW.

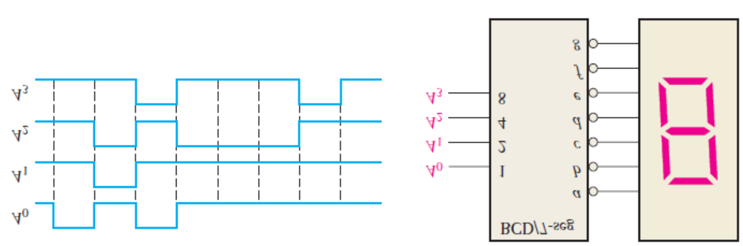
10. If the input waveforms are applied to the decoding logic as indicated in Figure 6–76, sketch the output waveform in proper relation to the inputs.



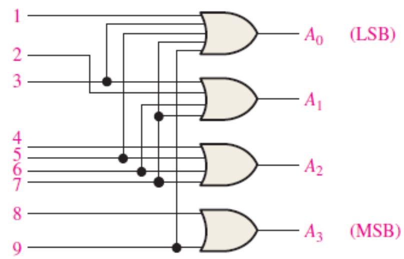
11. BCD numbers are applied sequentially to the BCD-to-decimal decoder in Figure 6–77. Draw a timing diagram, showing each output in the proper relationship with the others and with the inputs.



12. A 7-segment decoder/driver drives the display in Figure . If the waveforms are applied as indicated, determine the sequence of digits that appears on the display.



13. For the decimal-to-BCD encoder logic of Figure, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD (8421) code?

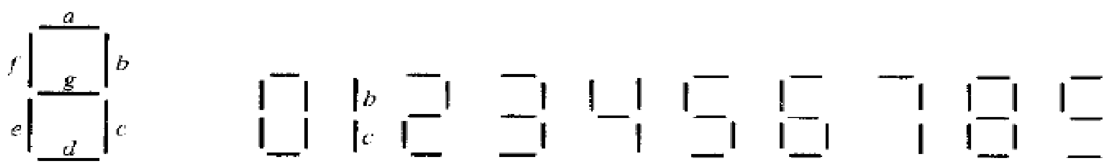


14. A 74HC147 encoder has LOW levels on pins 2, 5, and 12. What BCD code appears on the outputs if all the other inputs are HIGH?
15. Design a logic circuit whose output is High only when a majority of inputs A, B and C are Low.
16. Design a circuit that produced a HIGH out only when all three inputs are at the same level.
17. The notataion x1 x0represents a two-bit binary number that can have any value (00, 01, 10,11); for example , when x1= 1, x0 = 0 , the binary number is 10, and so on. Similarly y1, y0 represent another two-bit binary number. Design a logic circuit, using x1,x0,y1, and y0 inputs , whose output will be HIGH only when the two binary numbers x1 x0 and y1 y0 are opposite.
18. A four-bit binary number is represented as A3, A2, A1, A0, where A3 , A2, A1 and A0 represent the individual bits and A0 is equal to the LSB. Design a logic circuit that will produce a HIGH out put whenever the binary number is greater than 0010 and less than1000.
19. Write the function table for a half subtractor (input A and B, output DIFF and CARRY). From the function table, design two logic circuits that will act as half subtractor.
20. Derive an expression for 2-bit magnitude comparator using Table.

A2	A1	B2	B1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

21. A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a

display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d. e,j, g) select the corresponding segments in the display, as shown in Fig. P4-l6(a). The numeric designation chosen to represent the decimal digit is shown in Fig. P4-16(b). Design the BCD-to-seven-segment decoder using a minimum number of NAND gates. The six invalid combinations should result in a blank display.



(a) Segment designation (b) Numerical designation for display

22. Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:
(a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001
23. Show the logic required to convert a 10-bit Gray code to binary and use that logic to convert the following Gray code words to binary:
(a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001

24. For the multiplexer in Figure1, determine the output for the following input states: D0 = 1, D1 = 0, D2 = 0, D3 = 1,
(a) S0 = 0, S1 = 1 (b) S1 = 0, S1 = 1 (c) S0 = 1, S1 = 0

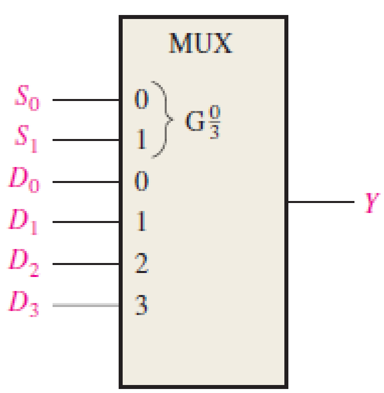


Figure1

25. If the data-select inputs to the multiplexer in above Figure1 are sequenced as shown by the waveforms in Figure2, determine the output waveform with the data inputs specified in Problem3.

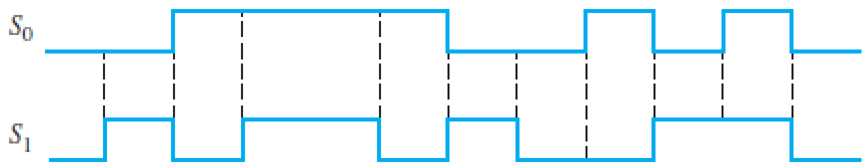
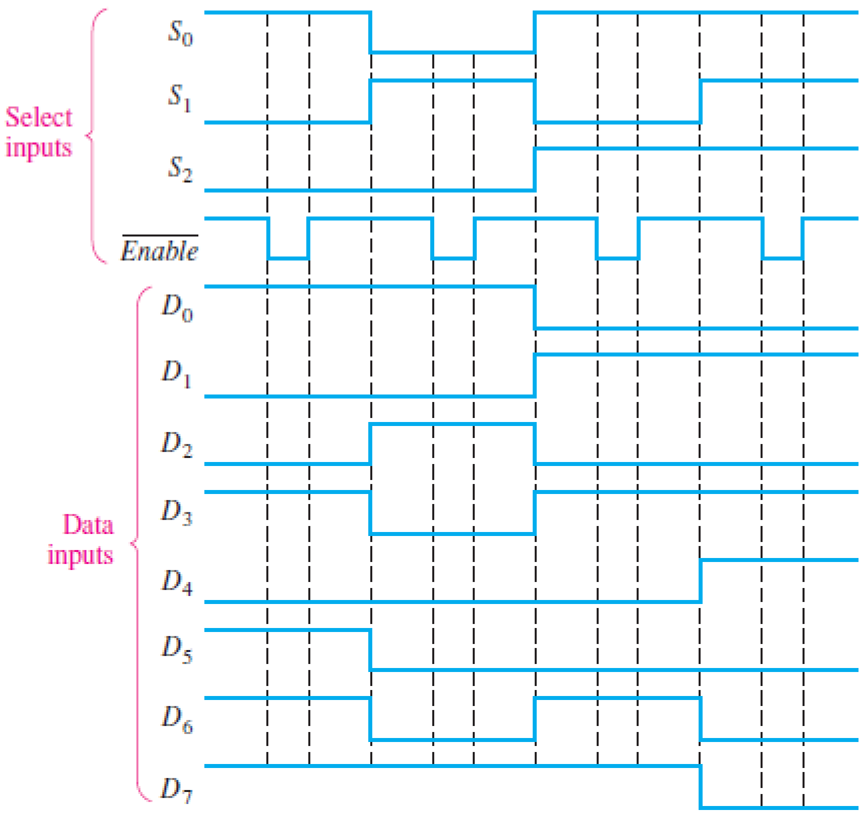


Figure2

26. The waveforms in Figure3 are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the Y output waveform.



27. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.
28. Implement the following Boolean function using decoder.
    $F(A, B, C, D) = \Sigma\,(1, 2, 3, 7, 9, 13, 15)$

29. Implement the logic function in table by using a 74S151 8 input data selector/multiplexer. $X(A_3, A_2, A_1, A_0) = \sum(2,3,4,8,9,10,11,15)$
30. Implement a full adder circuit by using:
    (a)3 – to - 8 line Decoder (b) 4 X 1 Multiplexers.

31. Construct a 16 X 1 multiplexer with two 8x1 and one 1x4 multiplexers. Use block diagrams.