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Faculty of Engineering, Built Environment and Information Technology

DEPARTMENT OF ELECTRONIC ELECTRIC AND COMPUTER ENGINEERING (EECE)

EES 424

ASSIGNMENT 2: RESEARCH PROPOSAL

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A. Problem Statement

There is a wealth of knowledge pertaining to the implementation of a sigmoid activation function of a field programmable gate array (FPGA). These onboard application methods include, however, not limited to the A-Law method proposed by [1]. This proposal will focus on using a piece wise function to potentially implement a sigmoid function on the FPGA as performed by [1] on the Altera Cyclone V SoC FPGA.

B. Research Statements

1. Can the piece wise function be used to implement a sigmoid as an activation function on a FPGA?
2. Can the system be deployed with a maximum error rate below 10% and a mean error rate below 5%?

II. Research Model

A. Model Description

The figure below is the hardware architecture as proposed by [2].

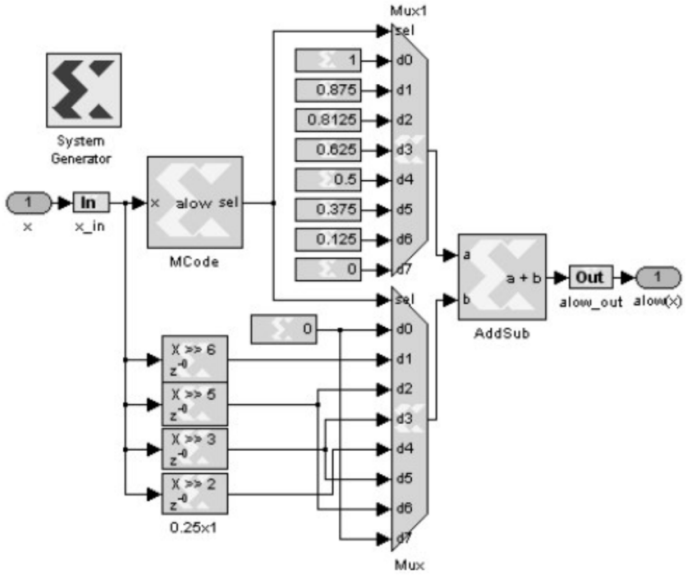

Fig. 1: Hardware architecture of the A Law approximation

The A-law method approximates the sigmoid function by taking the sigmoid function over the range of -8 to 8 and dividing it into 8 piecewise functions. By doing this the gradient of each of those points can be calculated and combined to approximate the sigmoid. However, this approximation will not result in a very closely matched function. An attempt will be made to increase the piecewise function from 8 data points to 16 data points in doing this the potential error should be reduced as the area between the ideal sigmoid and the approximated sigmoid will be reduced.The design will need to functional on the FGPA device supplied. From past experience it well know that working with decimal data can cause problems. One potential solution as suggested in [3] is to scale the decimal values to a large enough value to make the result an integer. This is a potention solution to the floating point values.

TABLE I: Break points of the A LAW approximation

x	-8.0	-4.0	-2.0	-1.0	1.0	2.0	4.0	8.0
y	0.0	0.0625	0.12	0.25	0.75	0.87	0.937	1.0

The table above contains the data points that the sigmoid was partitioned into. There are 8 points that were used to approximate the sigmoid in fig.2. The blue signal is the A-Law Python approximation and the orange signal is an ideal sigmoid with 100 data points.

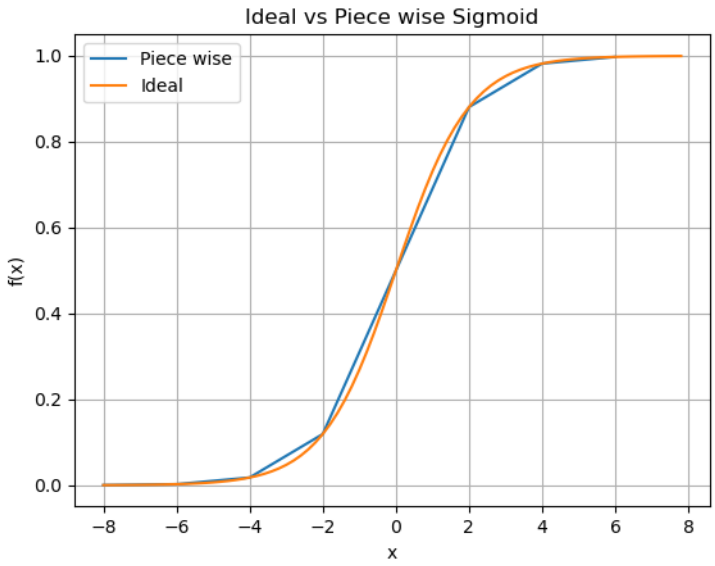

Fig. 2: Ideal sigmoid vs piece wise function of the sigmoid

In the figure above an ideal sigmoid is plotted on the same axis using the data points present in table.I.
One of the more critical areas for success would be the efficient use of the FPGA resources although the device utilisation is not yet know for the hardware the model will be implemented on, one can get a sense of idea looking at the implementation performed by [2]. Device usage was as follows in the table below.The higher the device utilisation the longer it would take the sofware to synthesise the design.

TABLE II: Resource Allocation for Hardware Implementation of Sigmoid on 4VSX35 FPGA[2]

Slices	LUTs	RAMBs	DSPs	Total equivalent gates count	Max frequency (MHz)	Estimated power consumed
29	31	1	1	66	268.168	607.02

B. Data collection

A serial communication link will be established the system deployed and a suitable computer. The serial(RS232) data that has been read will be saved to an appropriate file format for analysis at a later point. The computer will control the number of data points that will need to be read. A code written in Python running on the computer, will send the transmission start and stop command to the system to perform the necessary data acquisition.

C. Analysis Of Acquisitioned Data

To validate the captured data it will need to be compared to set function such as eq.1. The reference curve which is represented by eq.1 will be plotted in Python. The collected data will also be plotted in Python on the same axis.

$$f(x) = \frac{1}{1 + e^{-x}}. \tag{1}$$

Having both figures plotted on the same axis to make a comparison and as well as perform the necessary adjustments on the piece wise function and ideal function. This will allow for the error between the two functions to be computed. This error will be the area between the actual ideal sigmoid and the generated model within Python and VHDL. This will need to considered for the entire range of all the sigmoid models. A successful implementation would mean absolute error of below 5% for the entire range of the research model as suggested by [2]

D. Experimental Method

A high level system will be designed in Python to emulate the sigmoid function. This function will be of high accuracy using libraries in Python. The objective to attempted to minimise the error between the ideal sigmoid and the piece wise function. For this ideal representation, 100 points are used to simulate high accuracy while piecewise function is constructed by using 8 points. This figure simply a representation of how the model can be implemented. If the resolution of the system is increased ie: using more points such as 16 points. This would reduce the error between the ideal model and the simulate model. Once satisfied with the high level and low level Python models a low level VHDL model will be designed. A strategy needs to be devised to read float values from the FPGA moreover, how to process the floating point data.

E. Resource Planning

The figure below depicts a potential Gantt chart outlining the time line for the project life cycle.

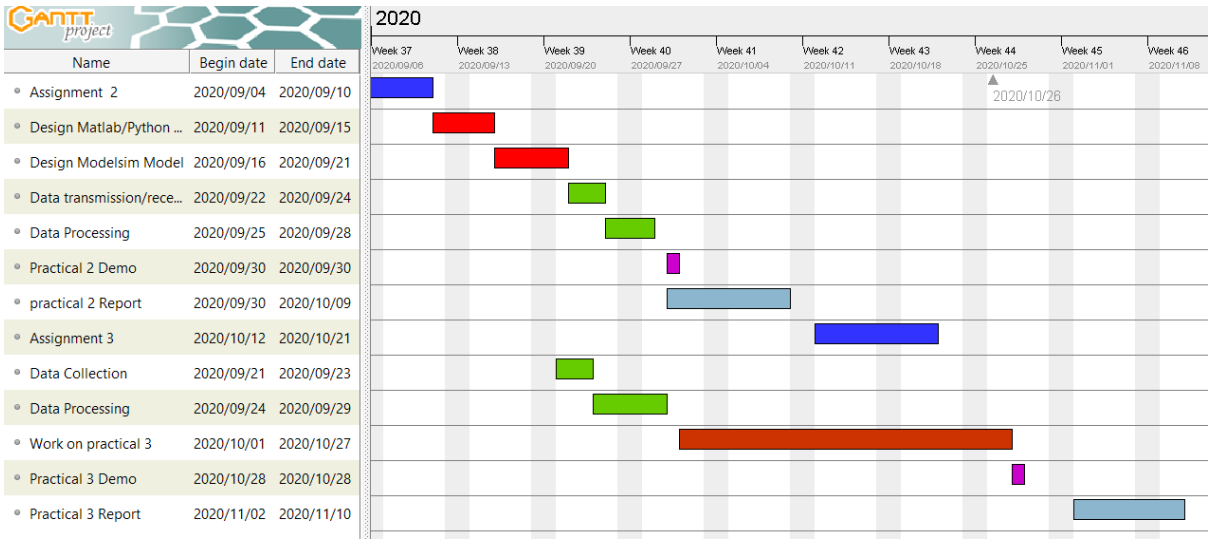

Fig. 3: Gantt chart of the research project.

REFERENCES

[1] D. J. Myers and R. A. Hutchinson, "Efficient implementation of piecewise linear activation function for digital vlsi neural networks," *Electronics Letters*, vol. 25, no. 24, 1989.

[2] A. Tisan, S. Oniga, D. Mic, and B. Attila, "Digital implementation of the sigmoid function for fpga circuits," *ACTA TECHNICA NAPOCENSIS Electronics and Telecommunications*, vol. 50, 01 2009.

[3] F. Vahid, *Digital Design 2nd Edition with RTL Design, VHDL, and Verilog and Verilog for Digital Design Set*. John Wiley & Sons Canada, Limited, 2010. [Online]. Available: https://books.google.co.za/books?id=BC-5uAAACAAJ