ECEN 5613 | **Embedded System Design** | Spring 2019

**Lab #2 Signoff Sheet**

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, February 15, 2019 (Part 1 Elements) and Friday, February 22 2019 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

**Student Name:** RUSHI JAMES MACWAN

**Honor Code Pledge**: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

**Student Signature:** Rushi J. Macwan

**Signoff Checklist**

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.

03/15

- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.

4/1

- ☑ Shows and discusses logic analyzer screen captures:

4/1

- ☑ Assembly program and timer ISR functional:

03/15

**TA signature and date** 4/1

Part 2 Required and Supplemental Elements

03/20

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☑ 74LS374 debug port functional
- ☑ Understands timing analysis, setup/hold/propagation
- ☑ MSP432 code build process, basic LED program execution

03/20

**TA signature and date** 4/1

**Instructor/TA Comments:** ☐ ☐ ☐

| **FOR INSTRUCTOR USE ONLY**<br>**Part 1 Elements** | Not Applicable | Poor/Not Complete | Meets Requirements | Exceeds Requirements | Outstanding |
|---|---|---|---|---|---|
| Schematics, SPLD code | ☐ | ☐ | ☐ | ☑ | ☐ |
| Hardware physical implementation | ☐ | ☐ | ☐ | ☑ | ☐ |
| Part 1 Required Elements functionality | ☐ | ☐ | ☐ | ☐ | ☐ |
| Sign-off done without excessive retries | | ☐ | ☑ | | |
| Student understanding and skills | ☐ | ☐ | ☐ | ☑ | ☐ |
| Overall Demo Quality (Part 1 Elements) | ☐ | ☐ | ☐ | ☑ | ☐ |

| **FOR INSTRUCTOR USE ONLY**<br>**Part 2 Elements** | Not Applicable | Poor/Not Complete | Meets Requirements | Exceeds Requirements | Outstanding |
|---|---|---|---|---|---|
| Schematics, SPLD code | ☐ | ☐ | ☐ | ☑ | ☐ |
| Hardware physical implementation | ☐ | ☐ | ☑ | ☐ | ☐ |
| Part 2 Required Elements functionality | ☐ | ☐ | ☑ | ☐ | ☐ |
| Supplemental Elements functionality | ☐ | ☐ | ☑ | ☐ | ☐ |
| Sign-off done without excessive retries | | ☑ | ☐ | | |
| Student understanding and skills | ☐ | ☐ | ☐ | ☑ | ☐ |
| Overall Demo Quality (Part 2 Elements) | ☐ | ☐ | ☐ | ☑ | ☐ |

NOTE: This signoff sheet should be the top/first sheet of your submission.

→ LED toggling for every 200 ms is shown. 03/06.

→ Part 1 delayed due to lack of logic analyzer analysis. +neat work