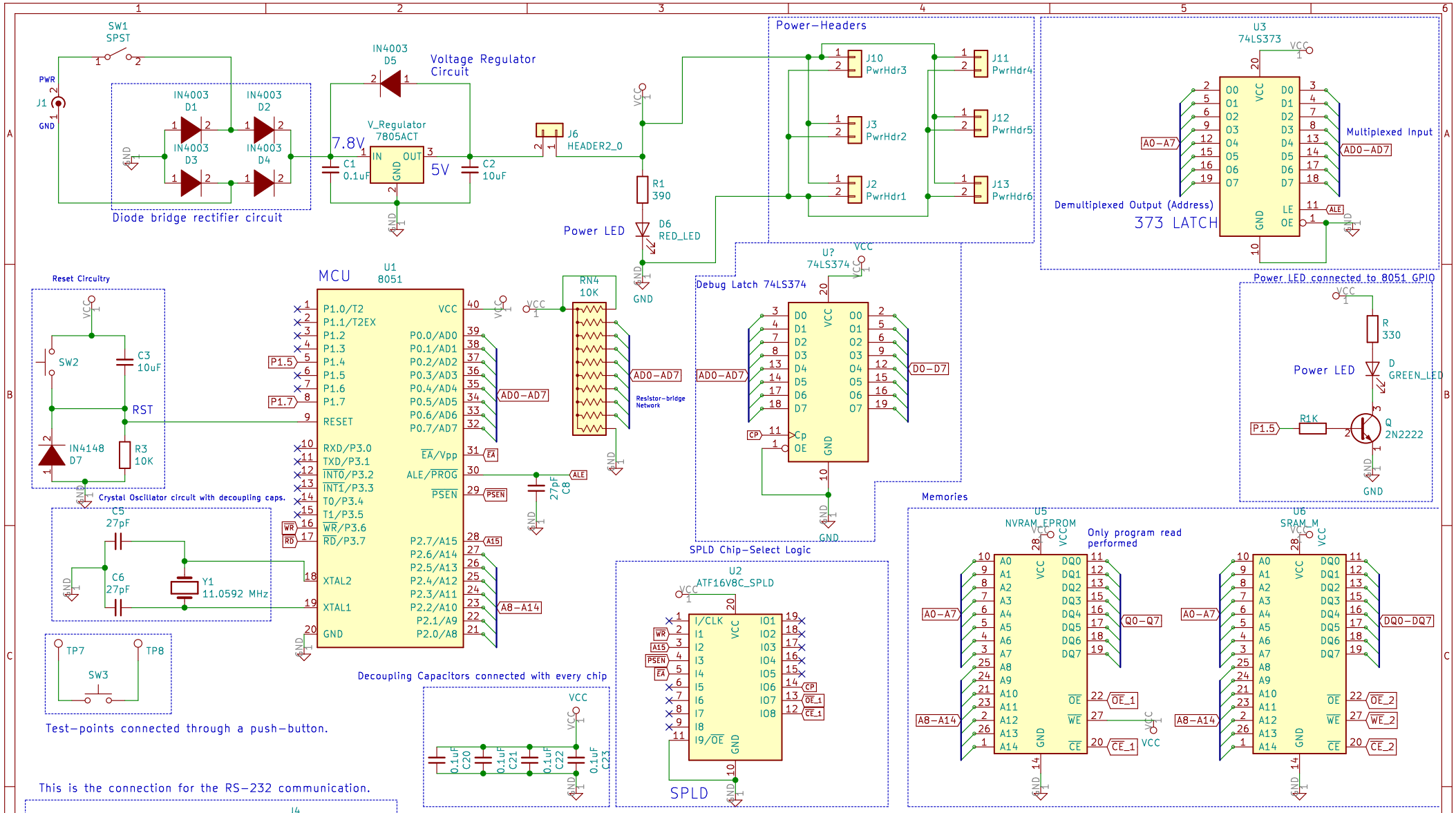

Lab-2 Circuit Diagram
This circuit diagram includes the decoding circuitry. The NVRAM will only drive the 8051 data bus while a code is read from it. To meet the goals, the SPLD decode logic has been designed in a fashion to meet all the requirements.

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ECEN 5613 - Embedded System Design
Lab-2 Circuit Schematics

Sheet: /
File: xyz.sch

Title: 8051 Basic Circuit (Lab-2)

Size: A4	Date: 9th March 2019	Rev: 002
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This schematic has been created by Rushi James Macwan. Credits and Courtesy to the class slides provided by Prof. McClure and the help & guidance received from the TAs.