Electrical, Computer & Energy Engineering
UNIVERSITY OF COLORADO BOULDER

ECEN 5613 Lab-1 Report

Course Name: Embedded System Design
Student Name: ***RUSHI JAMES MACWAN***

This submission is created by Rushi James Macwan. Credits and courtesy to the TAs (Tristan and Kiran) for their immense help and support.

Lab-1 Part-1

1. Bytes of code space my program requires – 56 Bytes

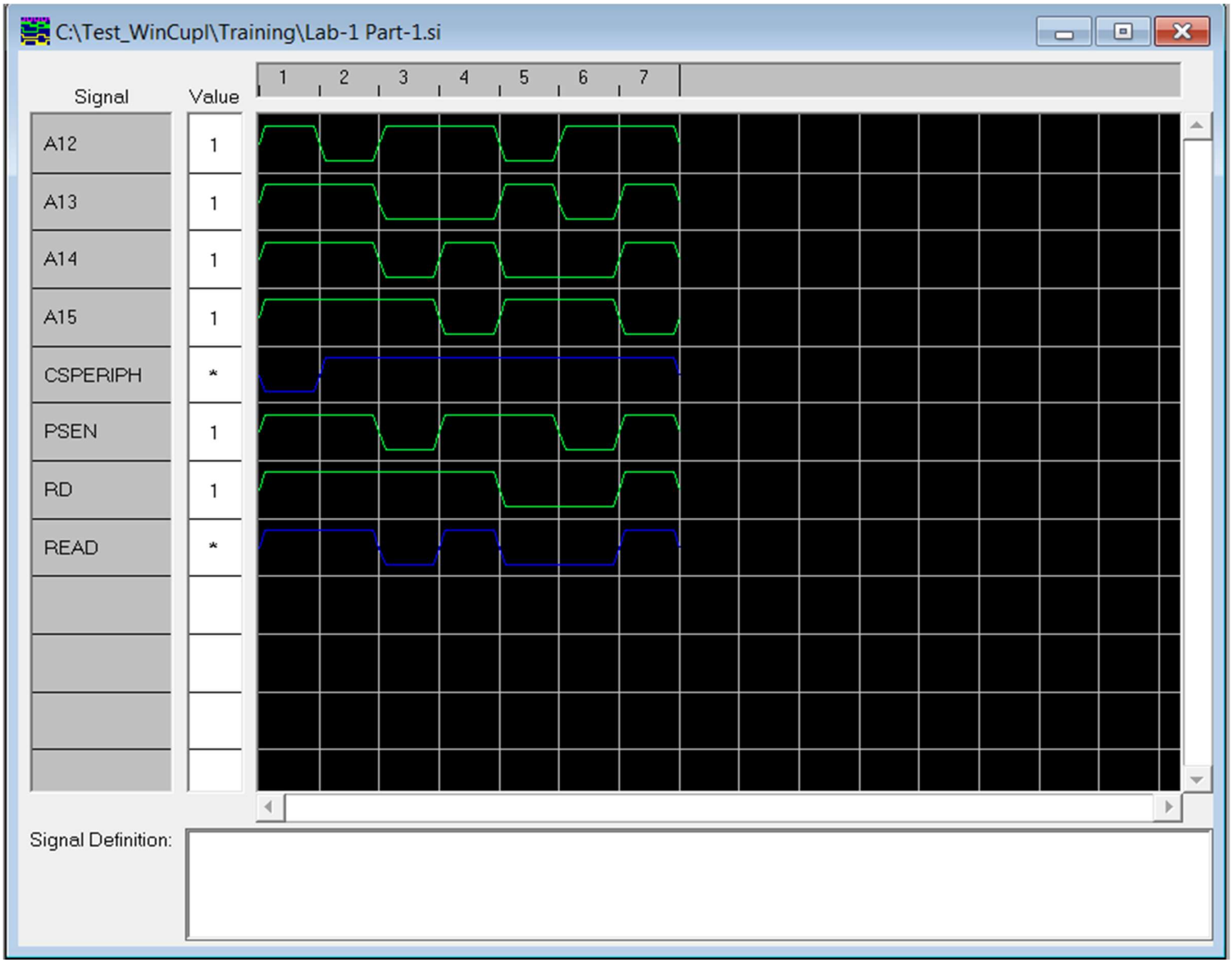
   I came to this number by looking at the starting and ending addresses of the program. In other words, I read the memory address spaces corresponding to the first and last program instructions. My code ran from 0x0000h to 0x0037h which corresponds to a space of 56 bytes in the memory.

2. The program required an execution time of 22.0630787 us.

   I came to this number by the fundamental idea that for every 6 states of the MCU, there exists 12 oscillator cycles. Given the IDE output, my program took 122 states in order to reach ENDLOOP. Thus, corresponding to 122 states, we would get 244 cycles given the information earlier.

   Secondly, every second, there exists 11.0592 M cycles because the oscillator frequency is 11.0592 MHz. Therefore, to run 244 cycles, it will take 22.0630787 us while it is true that every second, there are 11.0592 M cycles.

SPLD WinSim output:

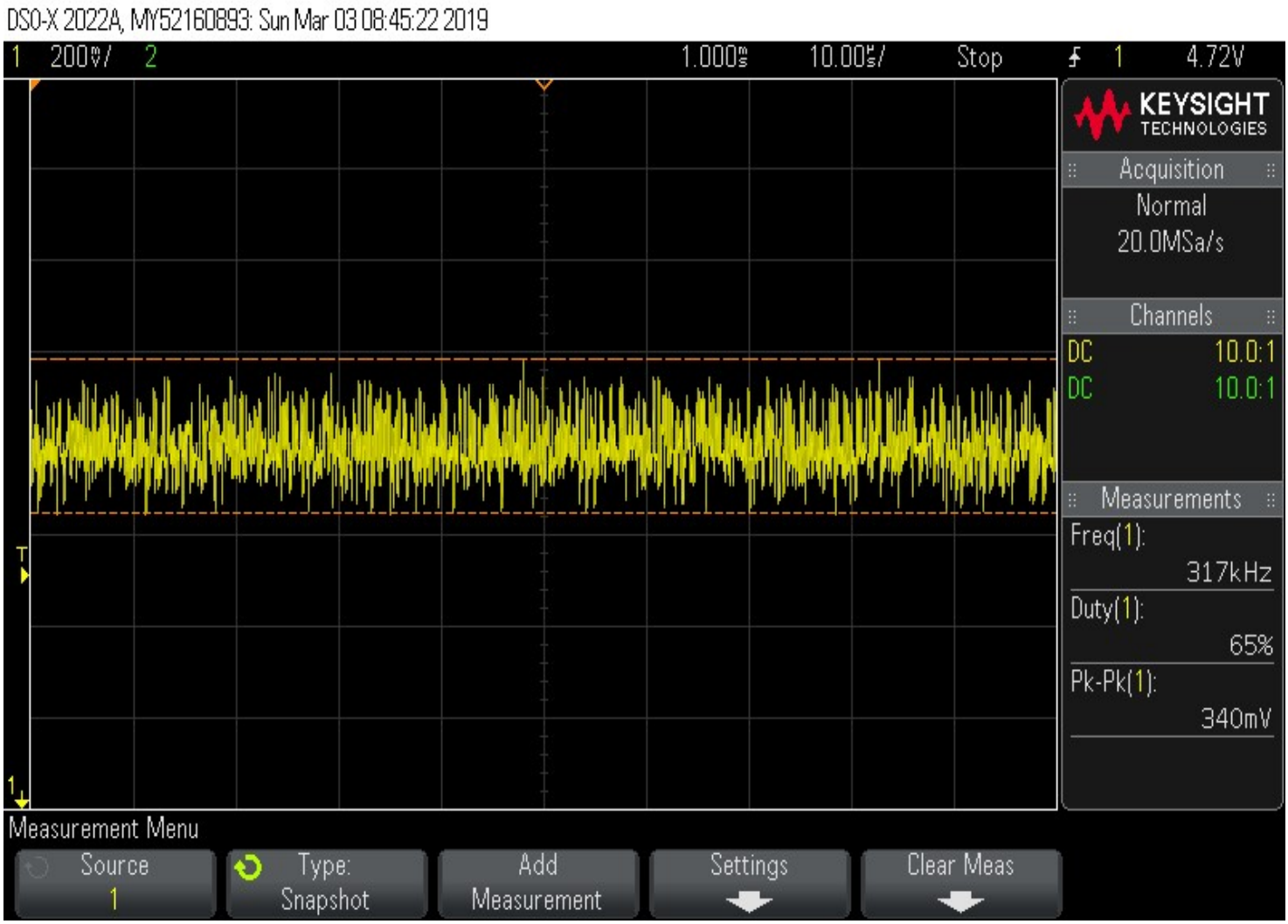


Lab-1 Part-2

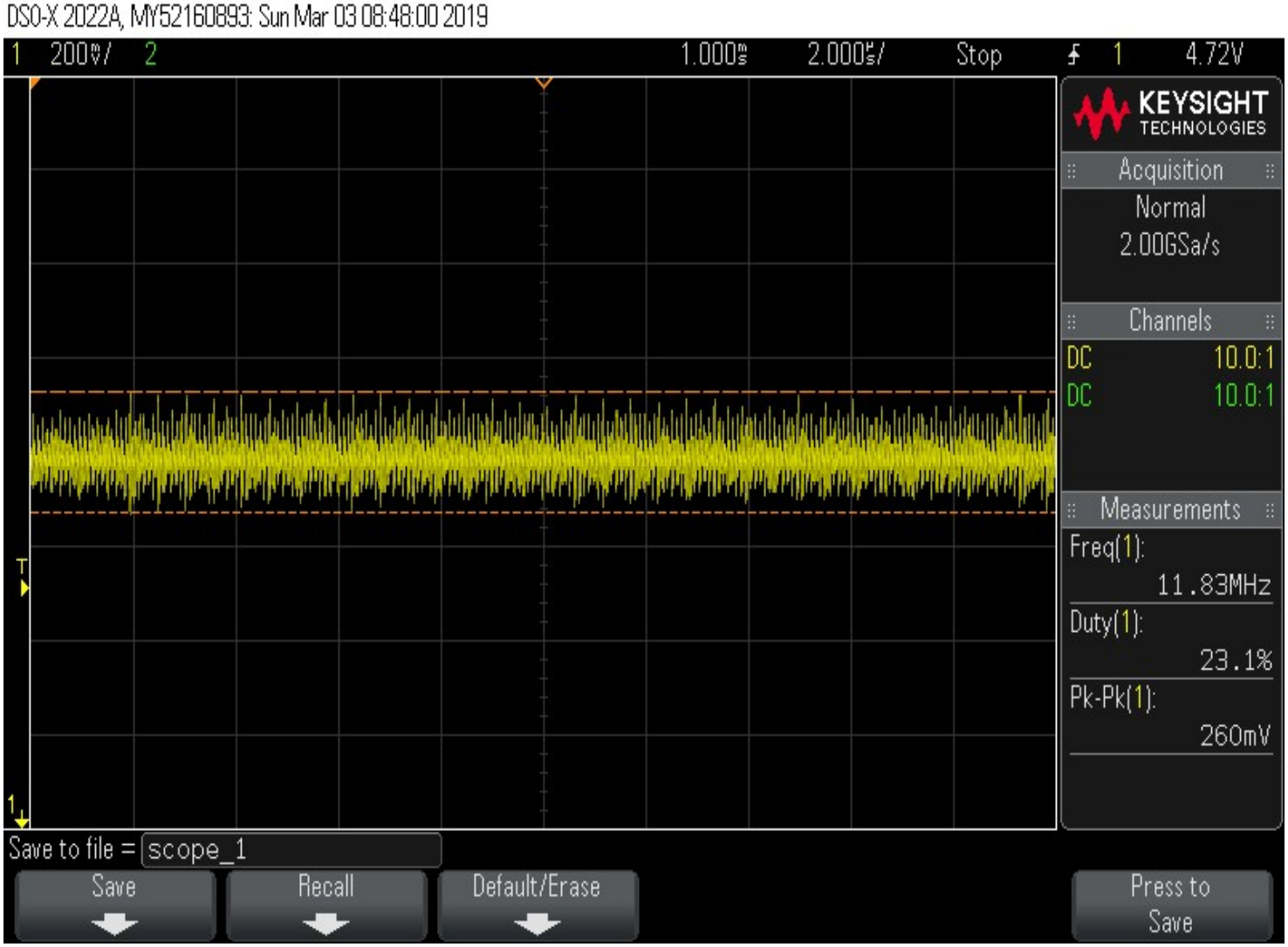
The KiCad lab schematic file is placed separately in the submission folder.

1. Voltage present at the regulator input – 7.48 V (Using multimeter)
2. Voltage present at the regulator output – 5.00 V (Using multimeter)
3. Peak-to-Peak noise present across the processor (8051) VCC and GND:

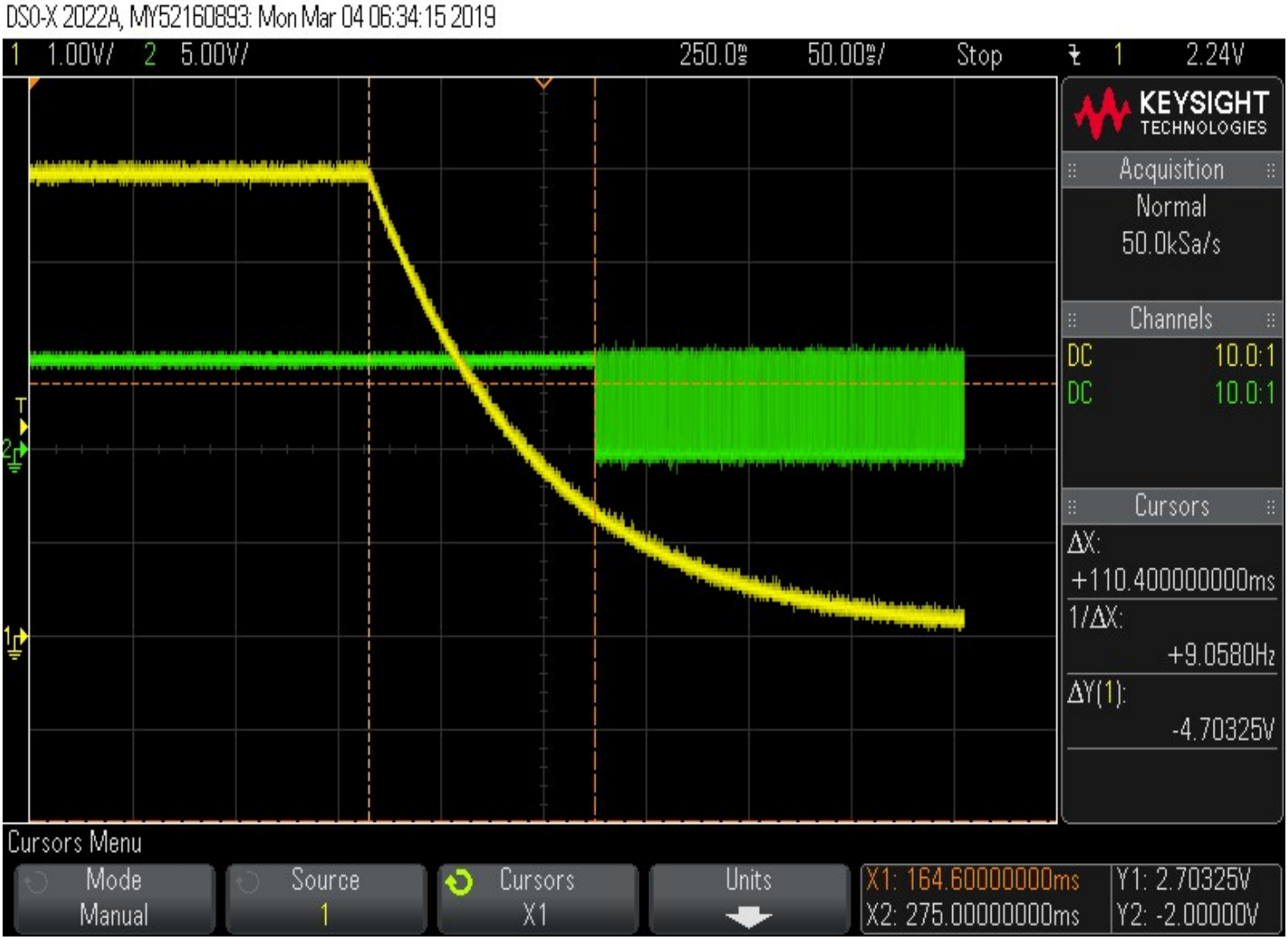
For measurements on top side of the package – 340 mV



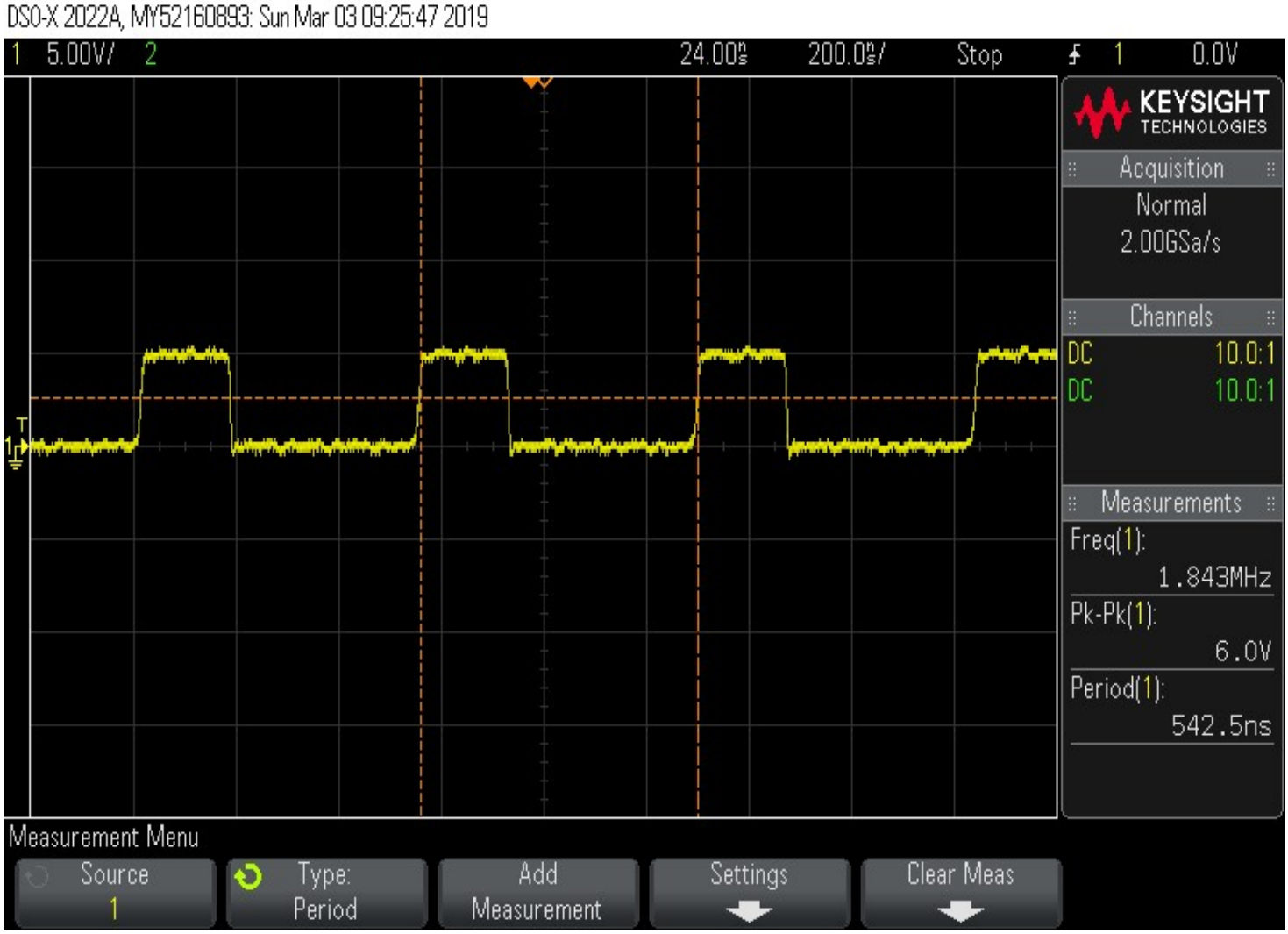
For measurements on bottom side of the package – 260 mV



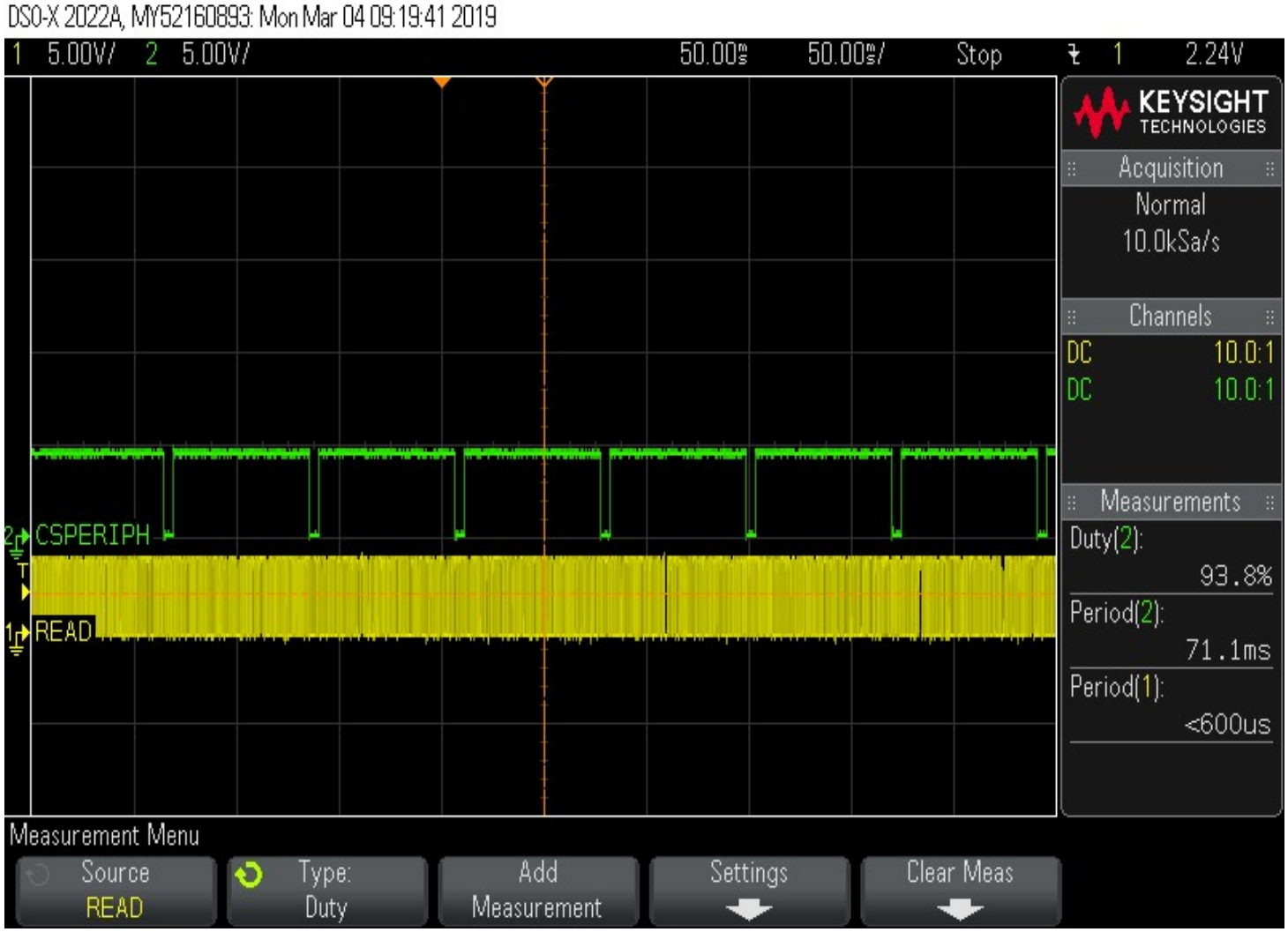
4. Time for which the processor is held in reset after the run-time reset push-button is released – 110.40 mS

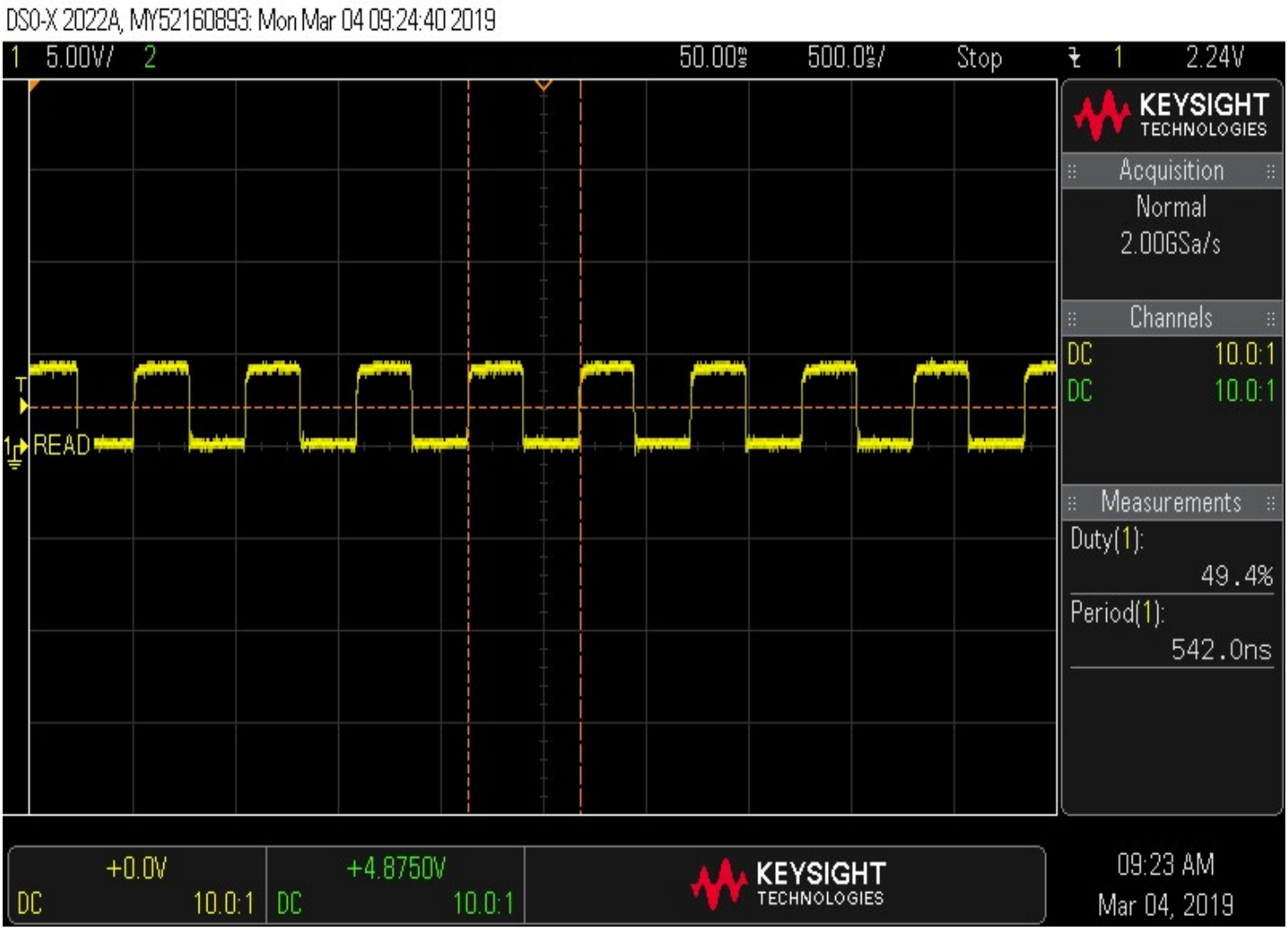


5. Frequency present on the ALE pin – 1.843 MHz



6. Duty-cycle present on the CSPERIPH signal while measuring both the outputs from the SPLD (i.e. READ and CSPERIPH signals) – 15/16 or in other words 93.8%


DSO-X 2022A, MY52160893: Mon Mar 04 09:19:41 2019
1 5.00V/ 2 5.00V/
50.00ms
50.00ms/
Stop
1 2.24V
KEYSIGHT TECHNOLOGIES
Acquisition
Normal
10.0kSa/s
Channels
DC 10.0:1
DC 10.0:1
Measurements
Duty(2):
93.8%
Period(2):
71.1ms
Period(1):
<600us
CSPERIPH
READ
Measurement Menu
Source READ
Type: Duty
Add Measurement
Settings
Clear Meas



Conclusion:-

From this laboratory, I personally learnt/polished the following skillsets:

1. Soldering and Wire-wrapping
2. Using an IDE to simulate the behavior of a MCU
3. Using WinCupl and WinSim tools to program a PLD
4. A way to run a very old tool on a relatively new computer
5. Deciphering datasheets
6. Understanding the basic aspects of designing a piece of hardware (e.g. decoupling capacitances involved, cold solder joints, inductance involved with overuse of wire-wraps, etc.)
7. Debugging skills by hands-on work on the lab hardware
8. Polished my knowledge of using a DSO and DM

9. Refreshed concepts about Assembly Language Programming
10. Timing concepts in digital circuits
11. A tool to design schematics (i.e. KiCad)
12. “Discovered that the DSO I have been using in the laboratory is showing a faulty time. This is because while I took some of these screenshots today (3rd March at around 4.00 PM MT), the DSO scope shots showed – 4th March, around 6.30 AM which probably corresponds to somewhere in the East.”

I am very happy to take this course. I fall out of phase because my initial decision was wrong in taking two heavy subjects along with a part-time job at the same time. However, I have made every effort to overcome my mistake by taking only two subjects this semester with no other obligations. I am already learning so heavily from the labs. I plan to do my best and be successful at this course.

Thanks.