LAB REPORT

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Section	:	B
Semester	:	2nd
Experiment No	:	09

Experiment name: Study of Asynchronous Counter

AIM:

(i) To design a 0 to 12 bit up counter.

(ii) To design a 15 to 3 bit down counter.

Learning objective:

(i) To Learn about asynchronous counter and its application.

(ii) To Learn the design of asynchronous up counter and down counter.

Components required:

IC 7476, Patch Cords & IC trainer kit

Theory:

A counter in which each flip flop is triggered by the output goes to previous flip-flop. As all the flipflops don't state change state simultaneously, spike occur at the output. To avoid this, Strobe pulse is required. Because of propagation delay the operating

speed of asynchronous counter is low. Asynchronous counters are easy and simple to construct.

Procedure:

(i) All the components for their workings were checked.

(ii) The appropriate IC into the IC base was inserted.

(iii) Connections were made as shown in the circuit diagram.

(iv) The truth table was verified and the outputs were also verified.

Truth Table for 0-12 up counter:

Counter state	Q_3 Q_2 Q_1 Q_0	Counter state	Q_3 Q_2 Q_1 Q_0
0	0 0 0 0	7	0 1 1 1
1	0 0 0 1	8	1 0 0 0
2	0 0 1 0	9	1 0 0 1
3	0 0 1 1	10	1 0 1 0
4	0 1 0 0	11	1 0 1 1
5	0 1 0 1	12	1 1 0 0
6	0 1 1 0	13	0 0 0 0

(iii)

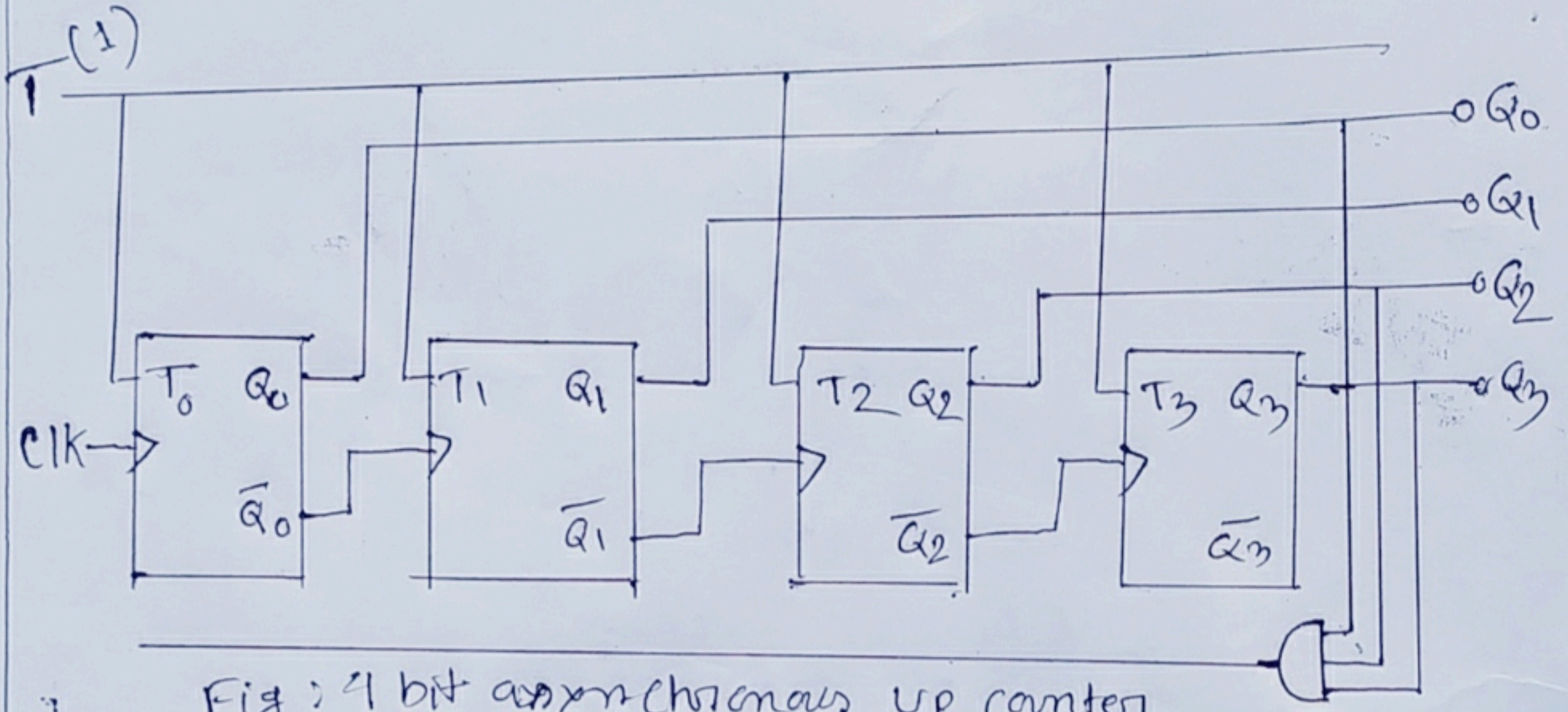

Fig : 4 bit asynchronous up counter

Truth Table for 15 to 3 down counter

Counter state	Q_3 Q_2 Q_1 Q_0	Counter state	Q_3 Q_2 Q_1 Q_0
15	1 1 1 1	8	1 0 0 0
14	1 1 1 0	7	0 1 1 1
13	1 1 0 1	6	0 1 1 0
12	1 1 0 0	5	0 1 0 1
11	1 0 1 1	4	0 1 0 0
10	1 0 1 0	3	0 0 1 1
9	1 0 0 1	2	0 0 1 0

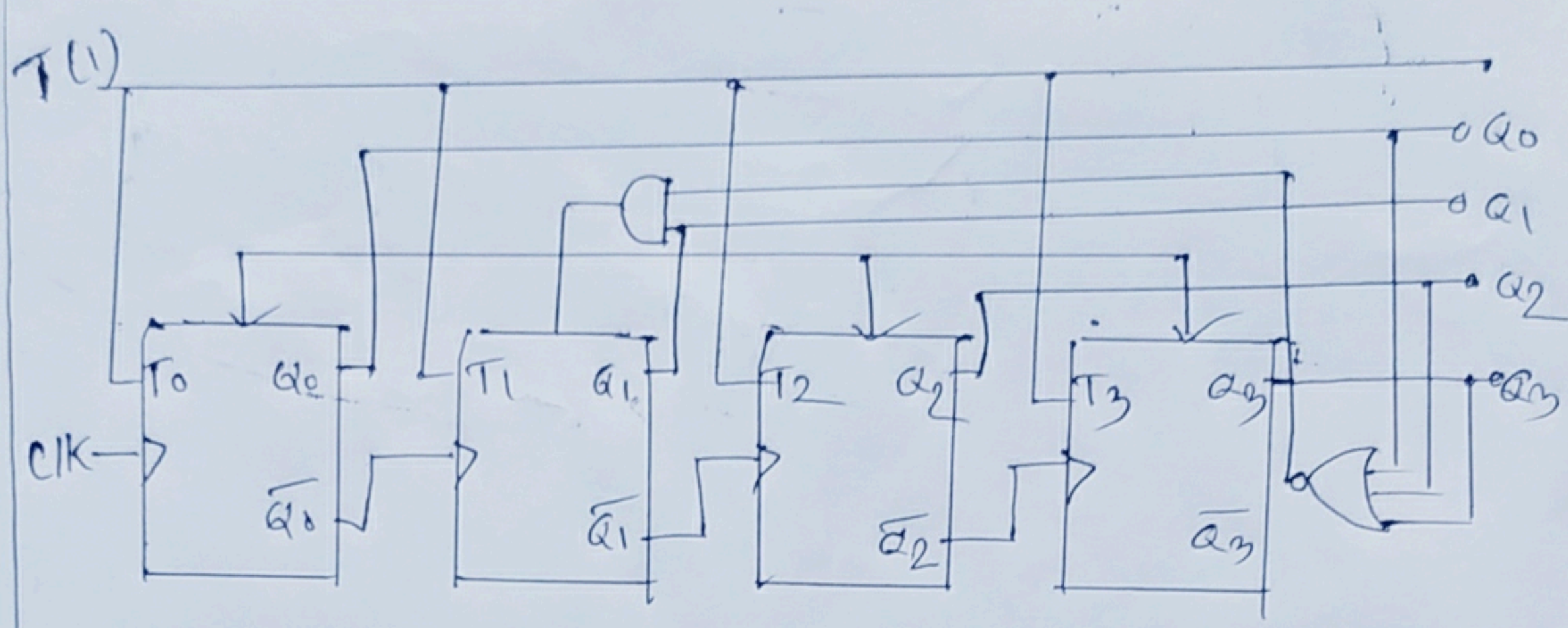

Fig : 4 Bit asynchronous Dum Counter

Result : The working method of asynchronous counters is verified.

Viva question :

Q. What is an asynchronous counters?

Ans: The output of which sequential circuit counter is free from clock signal is called asynchronous counters.

Q. How is it different from synchronous counters?

Ans: In synchronous counter every flip-flops are connected with same clock signal, where in asynchronous counter flip flop are not connected to same clock signal, they seperate their signal from previous output.