LAB REPORT

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Computer Science and Engineering

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Section : A

Semester : 1-2

Experiment No : 9

Experiment: Study of Asynchronous Counter.

AIM:

i. To design a 0 to 12 bit up counter.

ii. To design a 15 to 3 down counter.

Learning Objectives:

i. To learn about Asynchronous counters and its applications

ii. To learn the design of asynchronous up counters and down counters.

Components required: IC 7476, patch cords & IC trainer kit.

Theory:

A counter in which each flip flop is triggered by the output goes to previous flip flop. As all the flip-flops donot change state simultaneously spike occurs at the output. To avoid this, strobe pulse is required. Because of the propagation delay the operating speed of asynchronous counters is low. Asynchronous counters are easy and simple to construct.

Procedure:

i. Check All the componetits for their working were checked.

ii. The appropriate IC into the IC base was inserted

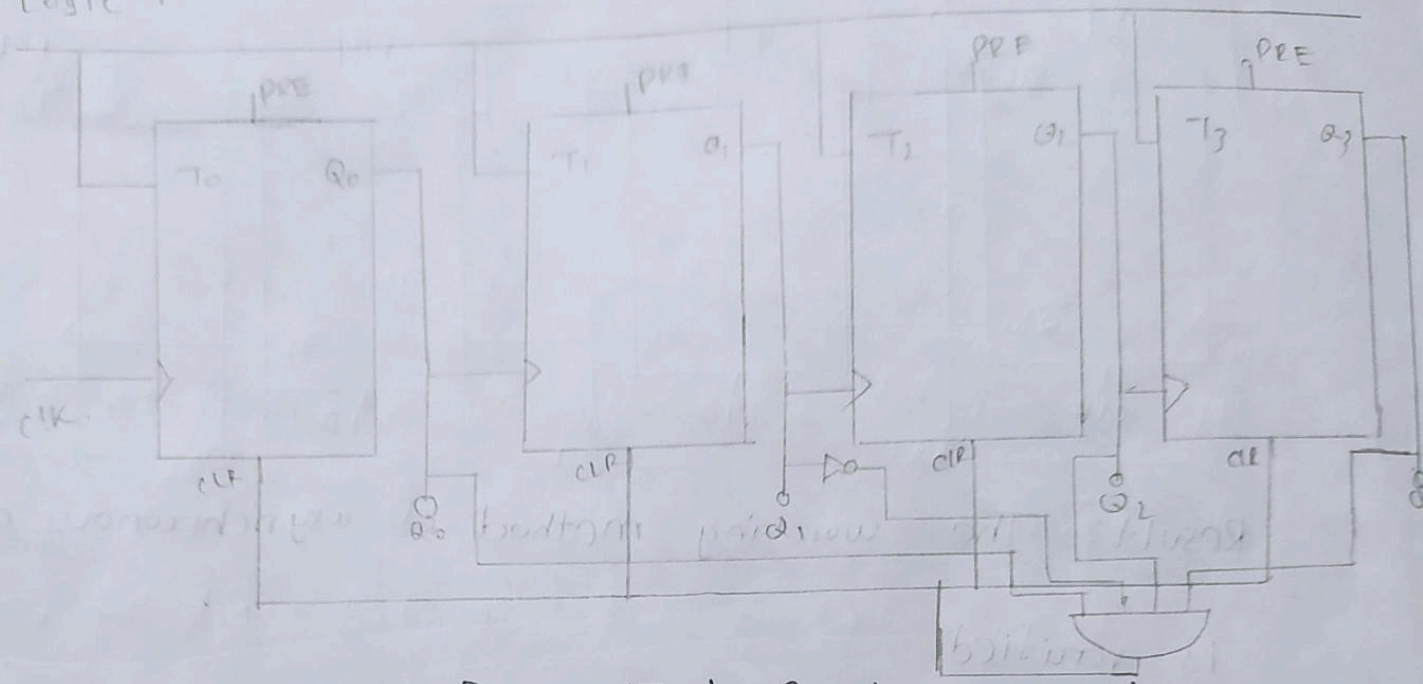
iii. Connections were made as shown in the circuit diagram.

iv. The truthtable was verified and the outputs were also verified.

Truth table for 0-12 UP Counter:

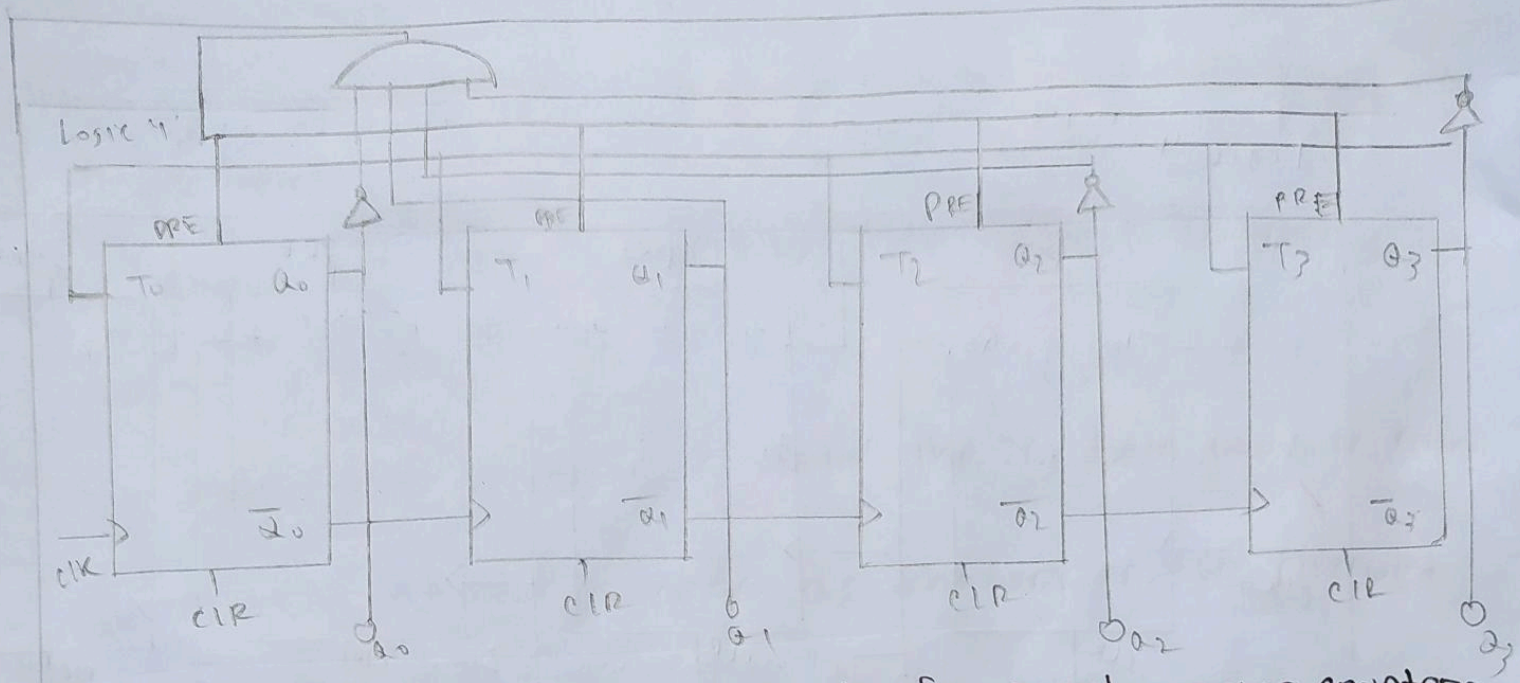
Counter state	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0

Counter state	Q_3	Q_2	Q_1	Q_0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	0	0	0	0



Truth table for 15 to 3 down counter:

Counter States	Q_3	Q_2	Q_1	Q_0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	1	1	1	1



Result: The working method of asynchronous counters is verified.

Viva Questions:

Q. What is an asynchronous counter?

Ans: The output of which sequential circuit counter is free from clock signal is called asynchronous counter.

Q. How is it different from a synchronous counter?

Ans. In synchronous counter every flip flops are connected with same clock signal, where in asynchronous counter flip flop are not connected to same clock signal, they generate their signal from previous output.