LAB REPORT

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Computer Science and Engineering

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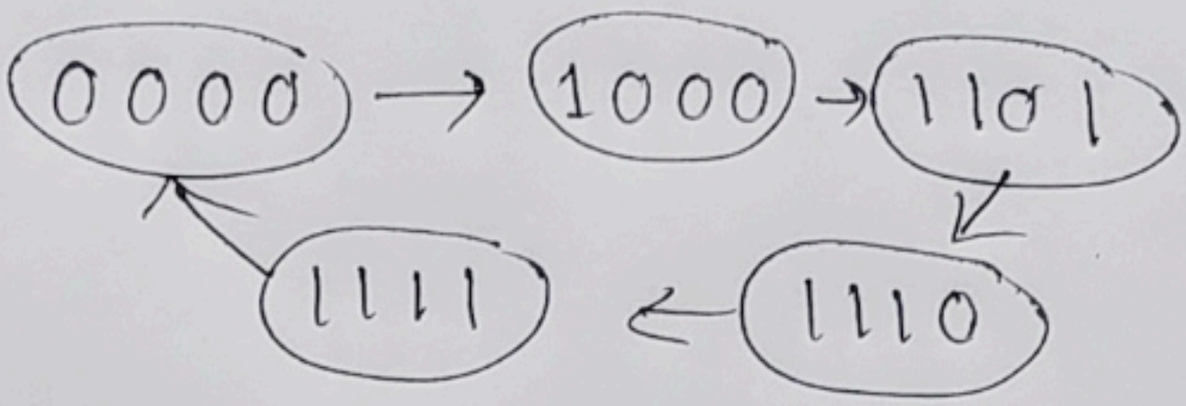
Section	:	B
Semester	:	2nd Semester
Experiment No	:	08

Experiment name : Synchronous Counters -

AIM : To design and test 4 bit binary synchronous counter using Flip Flop. IC 7476 (JK flip flop) for the given sequence.



Learning objective:

(i) To Learn abaut synchronous counter and its application.

(ii) To Learn the design of synchronous counter.

Components Required :

IC 7476, Patch cards, IC trainer kit.

Theory:

A counter is which Pach flip-flop is triggered by the output goes to previous flipflop. As all the flip flops do not chenge states simutaneasly in asynchronous counter spike occur at the output. To avoid this, steke pulse is required

Because of propagation delay, the opperating speed of asynchronus counter is low. This problem can be solved by triggering all the flip flop in synchronus with the clock signal and such counter are called synchronous counters.

Procedure;

(i) Check all the components for their working.
(ii) Insert the appropriate IC into the IC base.
(iii) Make connections as shown in the circuit diagram.
(iv) Verify the truth table and observe the outputs.

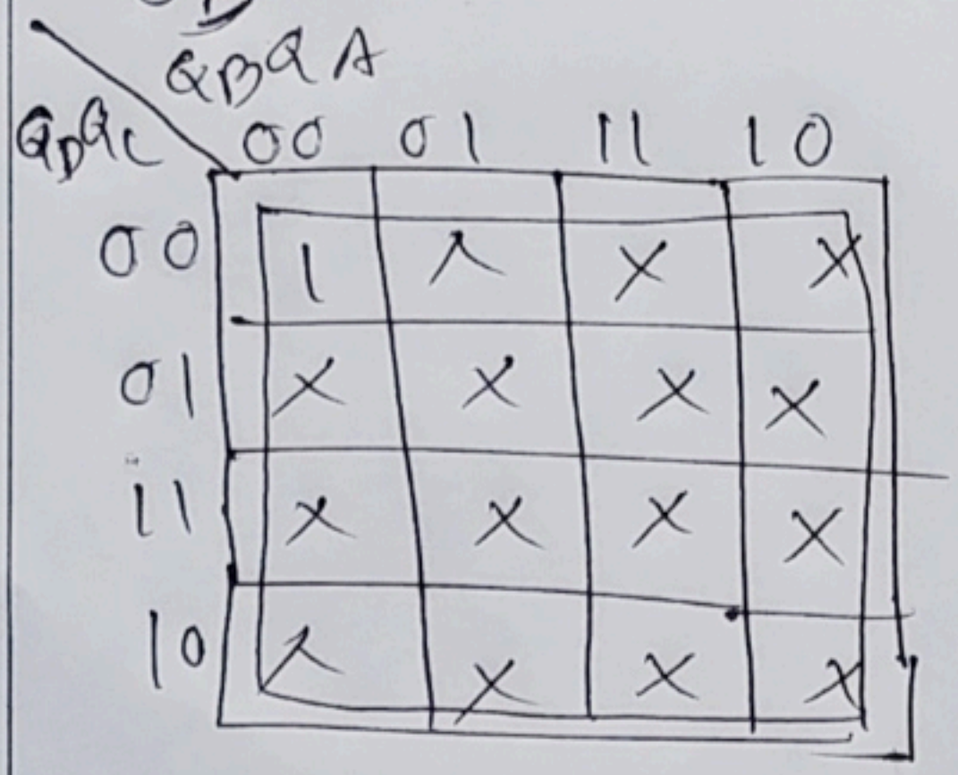
JK FF excitation table -

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Circuit excitation table:

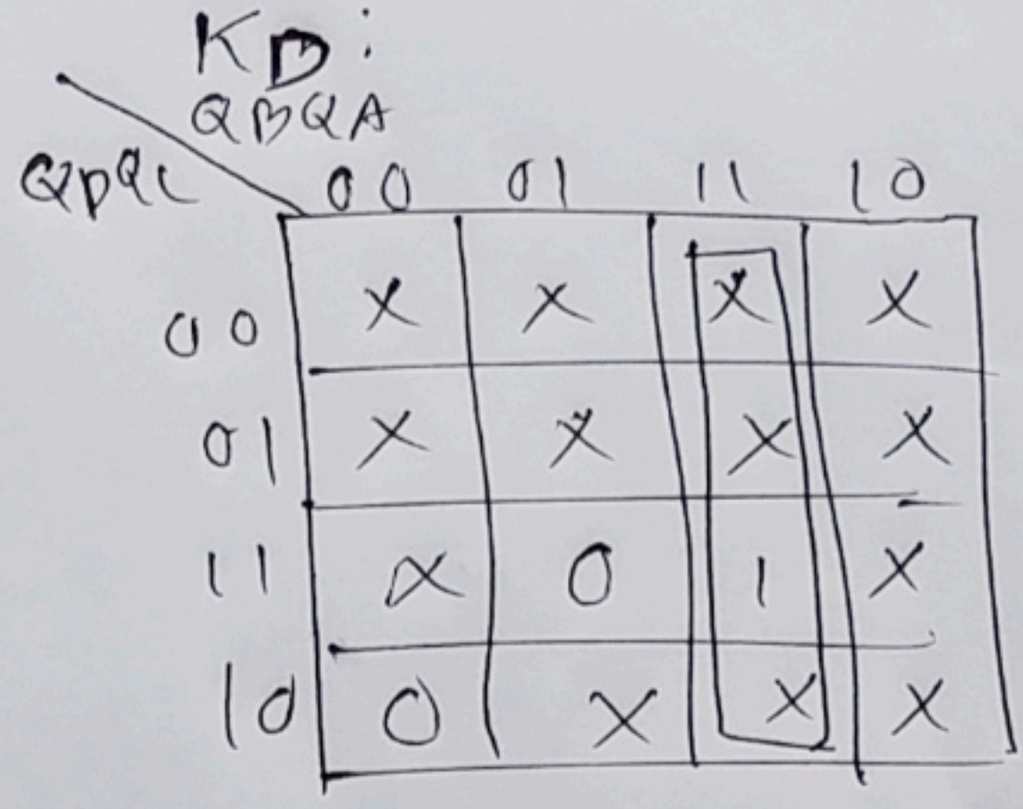
Q_D	Q_C	Q_B	Q_A	Q_D^t	Q_C^t	Q_B^t	Q_A^t	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	1	0	0	0	1	X	0	X	0	X	0	X
1	0	0	0	1	1	0	1	X	0	1	X	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

J_B:



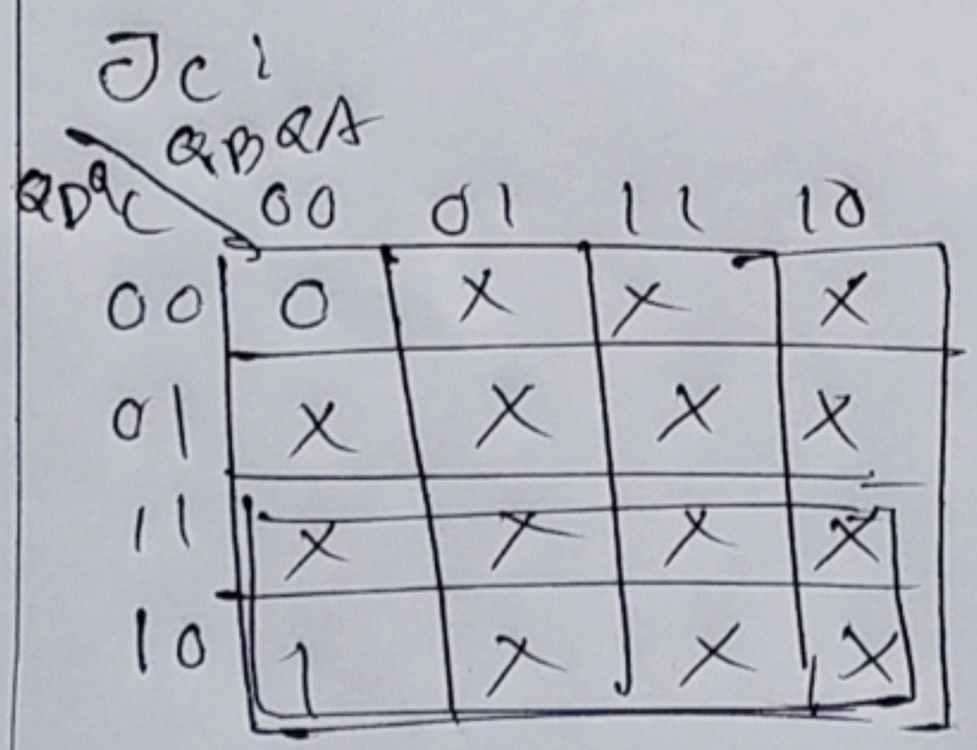
$J_D = 1$

K_D:



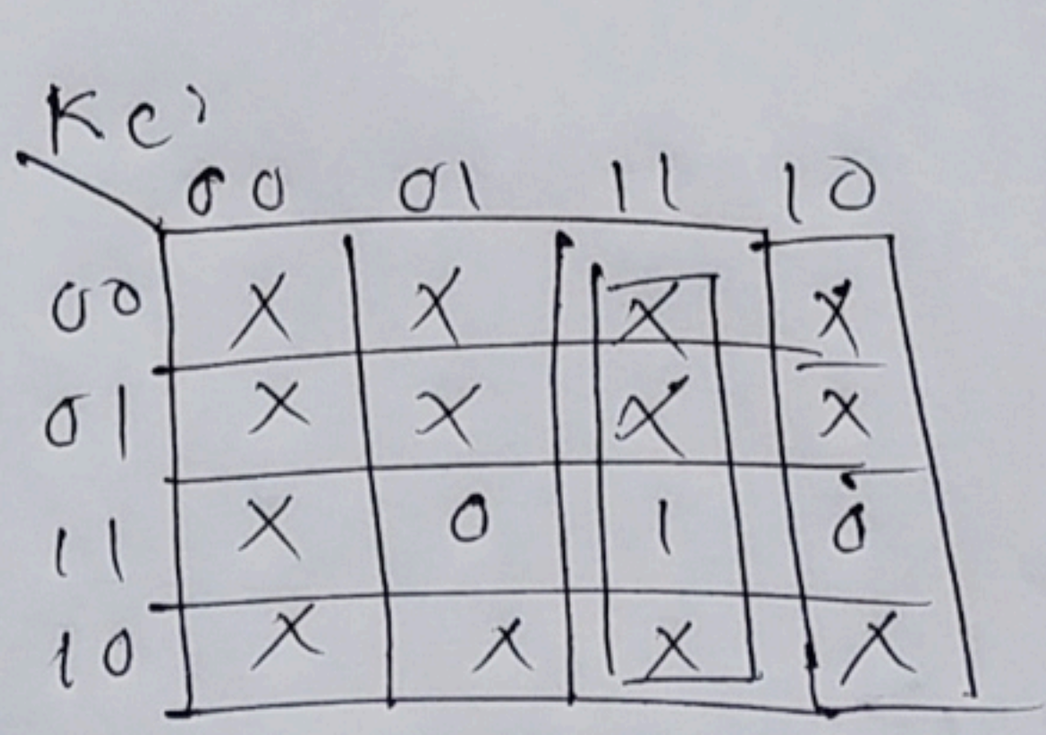
$K_D = Q_B Q_A$

J_C:



$J_C = Q_D$

K_C:



$K_C = Q_B Q_A$

J_B :

Q_D\$Q_B Q_A$	00	01	11	10
00	0	X	X	X
01	X	X	X	X
11	X	1	X	X
10	0	X	X	X

$J_B = Q_A$

K_B :

Q_D\$Q_B Q_A$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	1	0
10	X	X	X	X

$K_B = Q_A$

J_A :

Q_D\$Q_B Q_A$	00	01	11	10
00	0	X	X	X
01	X	X	X	X
11	X	X	X	1
10	1	X	X	X

$J_A = Q_D$

K_A :

Q_D\$Q_B Q_A$	00	01	11	10
00	X	1	X	X
01	X	X	X	X
11	X	X	1	X
10	X	X	X	X

$K_C = \overline{Q_B}\,1$

$J_D = 1$, $K_D = Q_B Q_A$

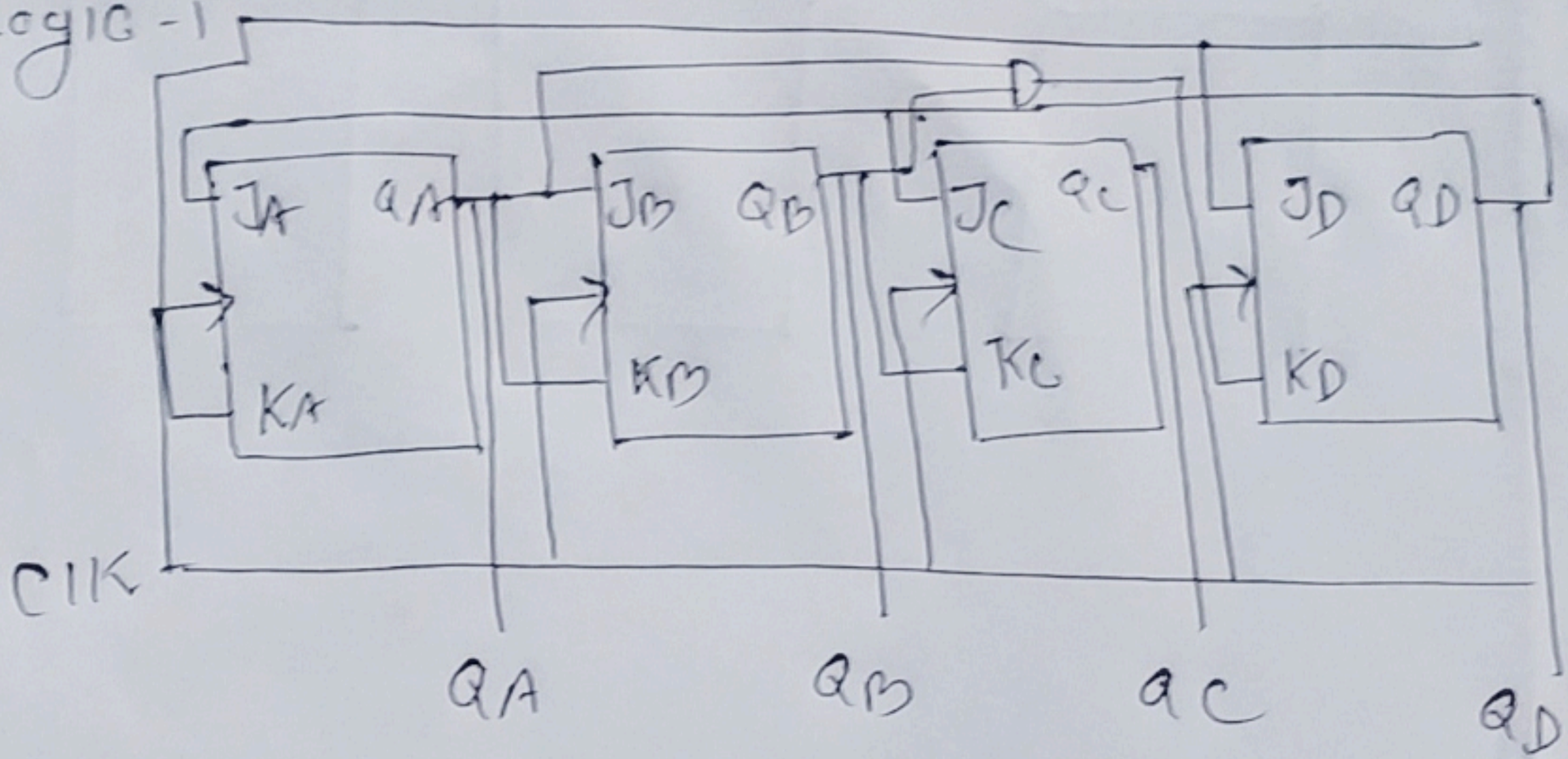
$J_C = Q_D$, $K_C = Q_B Q_A$

$J_B = Q_A$, $K_B = Q_A$

$J_A = Q_D$, $K_A = 1$

Circuit Diagram

Logic -1



Result:

The working of synchronous counter is verified.

Viva question:

a. what are synchronous counters?

Ans: Synchronous counters are so called because the clock pulse input of all the individual flip flop with the counter are all

together at the same time by the same clock pulse signal.

Q. what are the advantages of synchronous counters?

Ans: The advantages of synchronous counters are as follows. Yes easier to design. that the asynchronous counters. It acts simultaneously. No propagation delay associated with it. Count sequence is controlled using logic gates, error chances are lower.

Q. what is an excitation table?

Ans: The table which has the minimum inputs and which will excite or trigger the flip flop to go from its present state to the next state.

Q. write the excitation table for D & TFF.

Ans:

D FF

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T FF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0