COE 381

16-bit Microprocessor Simulation Presentation

Class: BSc. Computer Engineering 3

Group Name: Tensor

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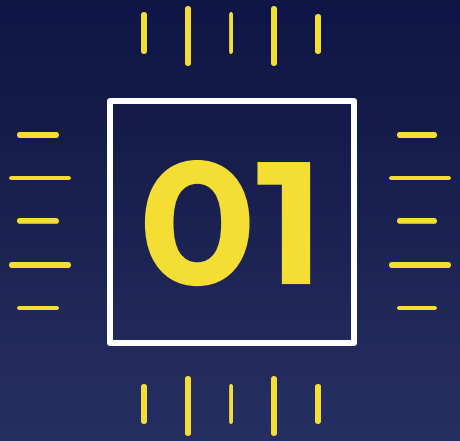
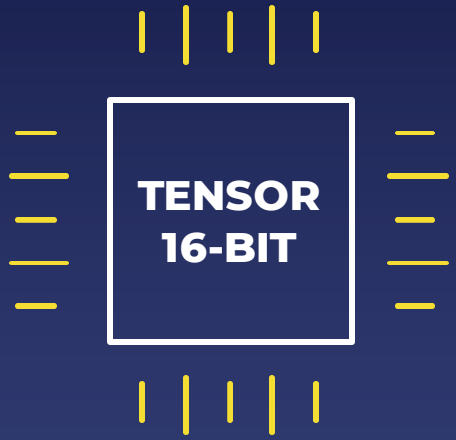


OVERVIEW

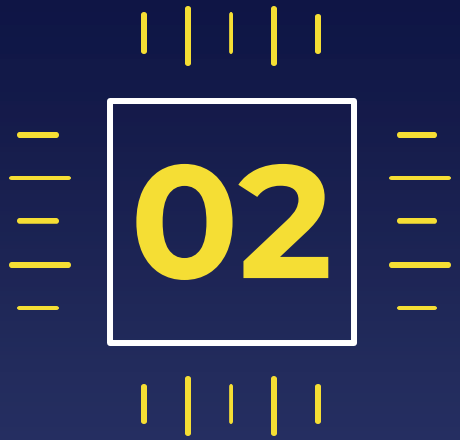
SPECIFICATIONS



ADDRESS BIT WIDTH	16 BITS
DATA BUS WIDTH	16 BITS
INSTRUCTION LENGTH	16 BITS
REGISTER COUNT	16
INSTRUCTION COUNT	14

OVERVIEW

- 16-bit microprocessor
- Based on RISC architecture inspired by MIPS I
- Harvard Architecture – separate instruction and data memory
- Memory is word-addressable (16 bits per location)
- Total Memory addressable = 2^{16} x 2 bytes = 128 KB.



ISA

Instruction Set Architecture

ISA - Overview

- The microprocessor can operate on 14 basic instructions.
- Each instruction falls under one of three categories

Category	Instructions
Arithmetic/Logic	ADD, ADDI, INCR, SUB, SUBI, DECR, AND, OR, XOR, NOT
Data Transfer	LOAD, STORE, MOV
Branch	JUMP

ISA – Instruction Format

- For simplicity, all instructions have a maximum length of 16 bits
- Each of the 14 instructions follows one of four instruction formats
- The instruction formats are as follows:
  - R-format
  - I-format
  - M-format
  - J-format

ISA – R-Format Instructions

- For instructions that utilize 3 registers.

OPCODE	Rd	Rs	Rt
4 bits	4 bits	4 bits	4 bits

  - Rd – destination register
  - Rs & Rt – source registers

- ***Instructions:*** ADD, SUB, AND, OR, XOR, NOT, MOV
- Some instructions won't use all three registers. Eg. NOT

ISA – I-Format Instructions

- For instructions that utilize 2 registers and an immediate value from the instruction.

OPCODE	Rd	Rs	Immediate
4 bits	4 bits	4 bits	4 bits

  - Rd – destination register
  - Rs – source registers
  - Immediate – 4-bit immediate value

- ***Instructions:*** ADDI, SUBI, INCR, DECR

ISA – M-Format Instructions

- For that utilize one register and an immediate value .

OPCODE	Rd	Immediate
4 bits	4 bits	8 bits

  - Rd – destination/source register
  - Immediate – 8-bit immediate value for memory addressing

- ***Instructions:*** LOAD, STORE
- For the STORE instruction, Rd is used as a source register.

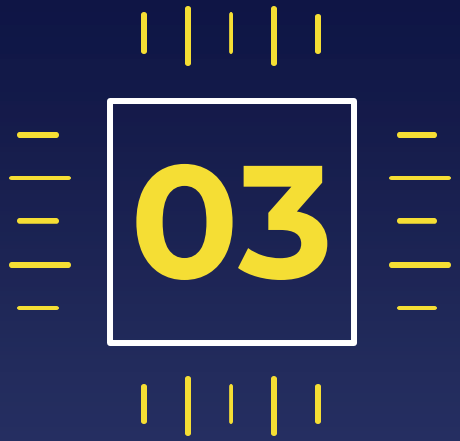
ISA – J-Format Instructions

- For the JUMP instruction that utilizes only an immediate value .

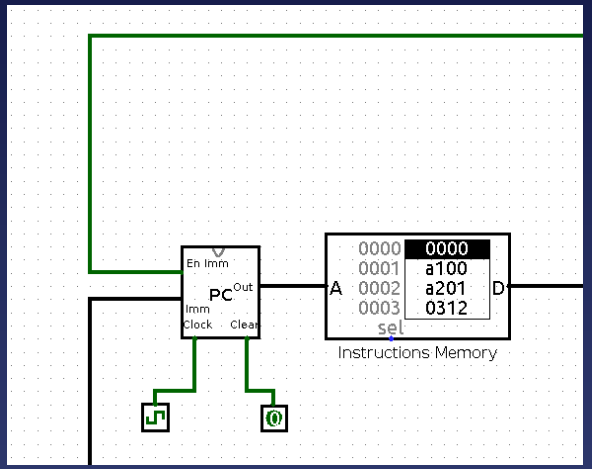
OPCODE	Immediate
4 bits	8 bits

  - Immediate – 12-bit immediate value for memory addressing

- ***Instructions:*** JUMP



COMPONENTS

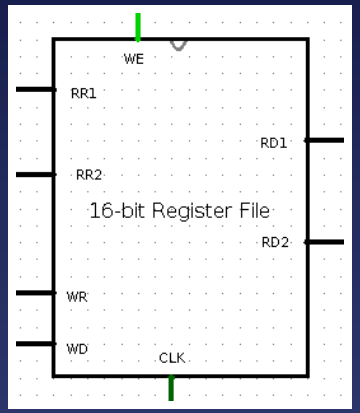


Program Counter

The program counter loads the address of the next instruction to be executed when it is triggered by the clock.

It can also be made to branch / jump to a specified address in the instruction memory

Register File



The register file is simply a housing for all 16 general-purpose registers used by the microprocessor.

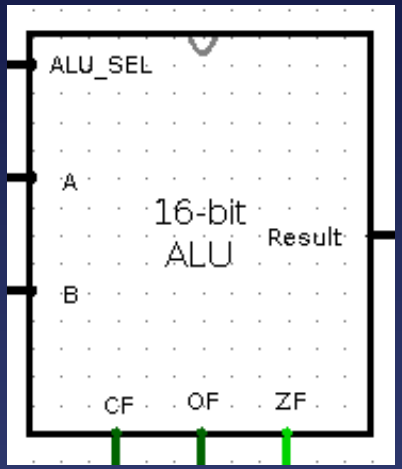
Statistics:

2 read-data ports, **2** read-address ports

1 Write-data port, **1** Write-address port

1 Write-enable, **1** clock

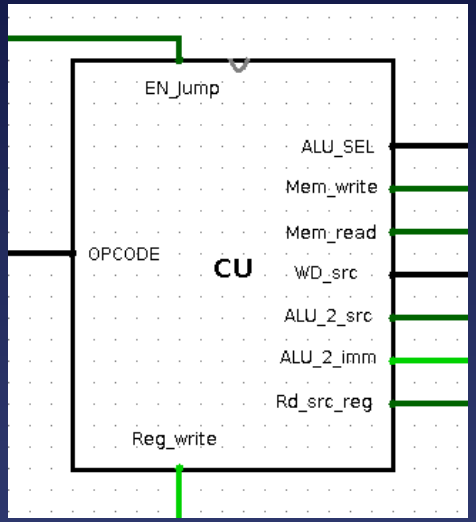
Arithmetic Logic Unit (ALU)



The ALU contains sub-circuits which are responsible for performing all arithmetic and logic operations defined in the ISA.

It uses the `ALU_SEL` control signal to determine which sub-circuit is required to perform a certain operation.

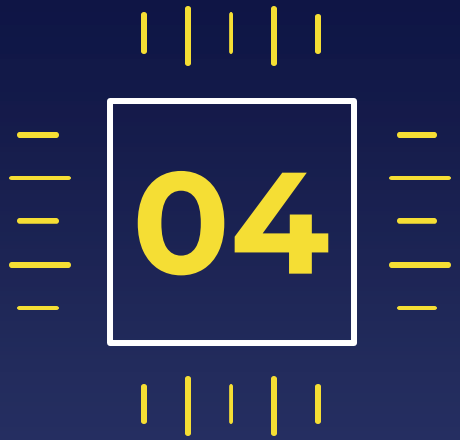
It also has carry, overflow, and zero flags.



Control Unit

The control unit is the operations manager.

It emits specific control signals for each operation, that direct the other components to successfully execute the instruction.



LIMITATIONS

What constraints does this design come with?

LIMITATIONS

- The I-format instructions reserve only 4 bits for the immediate, hence they can access a small range of numbers (0 to 2^4-1 for unsigned and -2^3 to 2^3-1 for signed)
- The JUMP instruction can only go as far as memory address 2^{12} whereas the farthest addressable memory location is 2^{16} - 1.

LIMITATIONS

- The LOAD and STORE instructions can only access as far as memory address 2^8-1 because their instruction format (M-format) permits only an 8-bit immediate for specifying memory addresses.

THANKS!

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