Short version of PCB Layout Guideline for DDR3 UDIMM and Leveled Components Implemented with UNIPHY Controller on Stratix III and Stratix IV Device Families Up to 533MHz (1066Mbps)

Recommended Termination Scheme (for single rank only)

When using DIMMs, you have no concerns about terminations on memory clocks, addresses, and commands. If you are using components, use an external parallel termination of 40 Ω to V_{TT} at the end of the fly-by daisy chain topology on the addresses and commands. For memory clocks, use an external parallel termination of 75 Ω differential at the end of the fly-by daisy chain topology on the memory clocks. Using fly-by daisy chain topology helps reduce any stub reflection. Keep the length of the traces to the termination to within 0.5 inch (14 mm). Use resistors with tolerances of 1 to 2%.

	SSTL 15 IO Standard [1]	FPGA Side on-board termination[2]	Memory Side Termination For Write	Memory Driver Strength for Read
DQ	Class I R50C/G50C [4]	N/A	60Ω ODT[3][5]	40Ω[3][5]
DQS	Differential Class I R50C/G50C [4]	N/A	60Ω ODT[3][5]	40Ω[3][5]
DM	Class I with R50C [4]	N/A	60Ω ODT[3][5]	40Ω[3][5]
Address and command	Class I with max drive strength	N/A	39Ω on-board termination to Vtt[6]	
CK/CK#	Differential Class I R50C	N/A	On board[6]: 2.2pf compensation cap before the first component; 36 Ω termination to Vtt for each arm (72Ω differential); add 0.1uF right before Vtt	

Note:

(1) These settings will be implemented by UNIPHY IP automatically

(2) Altera recommend using dynamic On-Chip-Termination (OCT) available to Stratix III and Stratix IV families

(3) These settings can be set in UNIPHY memory settings panel

(4) R50C means series 50Ω with cal (for write); G50C means parallel 50Ω with cal (for read)

(5) These recommendation are not rigid, simulate with real board stackup/trace to get optimal settings

(6) For DIMM these are already implement on DIMM card; for component topology is recommended to mimic termination scheme on DIMM card on your board

Layout Guidelines

Disclaimer:

Altera strongly recommend users do a board level simulation to ensure the timing specs in this section are met. Trace length number listed are only for typical case and might not reflect your particular board for the reason of board material, geometry, crosstalk, etc.

Trace Length Matching Requirement

Clock signals

- Clocks must maintain a length matching between clock pairs of ±5 ps or approximately ± 25 mils (0.635 mm).

- Differential clocks need to maintain length matching between positive and negative signals of ±2 ps or approximately ± 10 mils (0.254 mm), routed in parallel.

Address and Command signals

- Route all addresses and commands to match the clock signals to within ±25 ps or approximately ± 125 mil (± 3.175 mm) to each discrete memory component.

DQ/DQS/DM

- All signals within a given byte-lane group must be matched in length with a maximum deviation of ±10 ps or approximately ± 50 mils (± 1.27 mm).

- Ensure all signals within a given byte lane group are routed on the same layer to avoid layer to layer transmission velocity differences, which otherwise increase the skew within the group.

- DQ, DQS, DM signal don't need to be "in order", meaning it's not required that signals in group 1 arrive later than group 0, group 2 later than group 1 and so on.
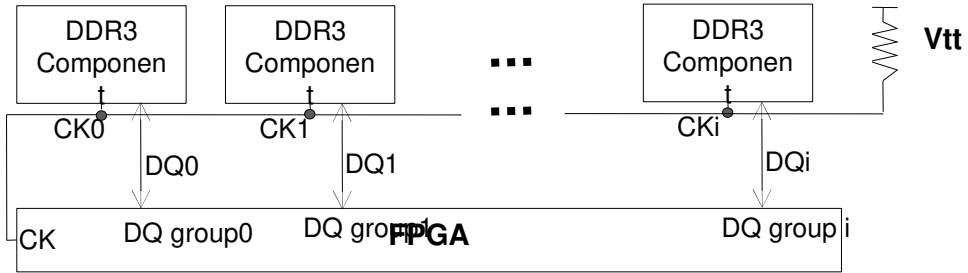
(CKi – CK) = CLK signal propagation delay to device i
DQSi = DQ/DQS signals propagation delay for group i

Fig. 1

DQS to clock

Timing between DQS and clock signal on each device is dynamically calibrated if leveling is enabled. To meet tDQSS, make sure the following layout rules are followed:

- Clock signal propagation delay is no shorter than propagation delay of DQS signal at every device; in fig 1 above, it means:

$$(CKi – CK) – DQSi > 0 \quad (0 =< i < \text{number of components} – 1)$$

- Total skew of CLK and DQS signal between groups is less than one clock cycle

$$(CKi – CK + DQSi)max – (CKi – CK + DQSi)min < 1 * Tck$$

These rules are to ensure during write leveling calibration we can put delay on the DQS signal to align DQS and clock, and to make sure skew is too large for the leveling circuit's capability

Maximum/Minimum Trace Length

- Maximum trace length for all signals from FPGA to first DIMM slot is 4.5 inches. Maximum trace length for all signals from DIMM slot to DIMM slot is 0.425 inches.

- When interfacing with multiple DDR3 SDRAM components, the maximum trace length for address, command, control and clock from FPGA to first component is maximum 7 inches, there's no minimum trace length requirement other than clock signal propagation delay has to be longer than DQS and address, command control signal need to match clock signal.

- The maximum length of clock/addr/command from the first SDRAM to the last SDRAM must be no more than 6 inches (approximately 153 mm) or 0.69 t_{CK}

- Ensure signal integrity is good at all memory devices in board simulation

General Routing Guidelines

Route using 45° angles and *not* 90° corners. Do not route critical signals across split planes. Route over appropriate V_{CC} and ground planes. Avoid routing memory signals closer than 25-mil (0.635 mm) to the memory clocks. Keep the signal routing layers close to ground and power planes. All specified delay matching requirements include PCB trace delays, different layer propagation velocity variance, and crosstalk. To minimize PCB layer propagation variance, Altera recommend that signals from the same net group always be routed on the same layer.

Clock Routing Guidelines

Route clocks on inner layers with outer-layer run lengths held to under 500 mils (12.7 mm).

- 10-mil spacing for parallel runs < 0.5 inches
  (2× trace-to-plane distance)

- 15-mil spacing for parallel runs between 0.5 and 1.0 inches
  (3× trace-to-plane distance)

- 20-mil spacing for parallel runs between 1 and 6 inches
  (4× trace-to-plane distance)

The space between differential pairs must be at least 2× the trace width of the differential pair to minimize loss and maximize interconnect density. For example, differential clocks must be routed differentially (5 mil trace width, 10-15 mil space on centers, and equal in length to signals in the Address/Command Group). Take care with the via pattern used for clock traces. To avoid transmission-line-to-via mismatches, Altera recommends that your clock via pattern be a Ground-Signal-Signal-Ground (GSSG) topology (via topology: GND | CLKP | CLKN | GND).

Address and Command Routing Guidelines

Similar to the clock signals in DDR3 SDRAM, address and command signals are routed in a daisy chain topology from the first SDRAM to the last SDRAM. Ensure that each net maintains the same consecutive order. Unbuffered DIMMs are more susceptible to crosstalk and are generally noisier than buffered DIMMs. Route the address and command signals of unbuffered DIMMs on a different layer than DQ and DM, and with greater spacing. Do not route differential clock and clock enable signals close to address signals.

Spacing rules for address and command and CLK signals

- 4 mils for parallel runs < 0.1 inch (approximately 1× spacing relative to plane distance)

- 10 mils for parallel runs < 0.5 inch (approximately 2× spacing relative to plane distance)

- 15 mils for parallel runs between 0.5 and 1.0 inches (approximately 3× spacing relative

to plane distance)

- 20 mils for parallel runs between 1.0 and 6.0 inches (approximately 4× spacing relative

to plane distance)

DQ, DQS, and DM Routing Guidelines

Maintain all other signals to a spacing that is based on its parallelism with other nets:

- 5 mils for parallel runs < 0.5 inches (approximately 1× spacing relative to plane distance)

- 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2× spacing relative to plane distance)

- 15 mils for parallel runs between 1.0 and 6.0 inches (approximately 3× spacing relative to plane distance)

Do not use DDR3 deskew to correct for more than 20 ps of DQ group skew. The deskew algorithm only removes the following possible uncertainties:

- Minimum and maximum die IOE skew or delay mismatch

- Minimum and maximum device package skew or mismatch

- Board delay mismatch of 20 ps

- Memory component DQ skew mismatch

Hence increasing any of these four parameters runs the risk of the deskew algorithm limiting, failing to correct for the total observed system skew. If the algorithm cannot compensate without limiting the correction, timing analysis shows reduced margins.