DH: Lab assignment 4

UNIVERSITY OF TWENTE.

Date:
October 8, 2025

Authors:
Cezar Stoica (s3401987)

Group:
6

Chapter 1

Level 1

1.1 ISA Table

Mnemonic	Operands	Description	Example
LOAD	Rdest, [addr]	Load data from memory to register	LOAD R1, [10]
STORE	Rsrc, [addr]	Store register data to memory	STORE R1, [20]
ADD	Rdest, R1, R2	Add R1 and R2 $\rightarrow$ Rdest	ADD R3, R1, R2
SUB	Rdest, R1, R2	Subtract R2 from R1 $\rightarrow$ Rdest	SUB R3, R1, R2
MUL	Rdest, R1, R2	Multiply R1 and R2 $\rightarrow$ Rdest	MUL R3, R1, R2
JMP	addr	Jump to instruction address	JMP 12
BEQ	R1, R2, addr	If R1=R2, jump to addr	BEQ R1, R2, 8
HALT	—	Stop program execution	HALT

Table 1.1: Instruction Set Architecture (ISA) for Level 1 processor.

1.2