

Quadrature Down Converter

Design, Simulations and Applications

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Abstract—This paper presents the design, simulation, and functional analysis of a quadrature down-converter. It begins with a brief overview of the purpose and applications of down-conversion, followed by a detailed breakdown of the system into its fundamental components. Each part is examined to highlight its role in the overall operation. The individual elements are then integrated into a complete circuit. Finally, the paper provides a comparative analysis of theoretical simulations and practical results, validating the effectiveness and accuracy of the proposed design for each individual components as well as the practical challenges faced while integrating the final down converter.

Index Terms—quadrature, oscillator, down conversion, mixer, filter, image rejection, modulation, switch, in-phase, quadrature phase

I. INTRODUCTION

Modern wireless communication systems require efficient frequency translation techniques to process high-frequency signals. Quadrature downconversion is a widely used approach in receiver front-ends, particularly in applications such as Bluetooth, Wi-Fi, and other RF systems. It enables the extraction of in-phase (I) and quadrature-phase (Q) components of a signal, which are essential for digital modulation and demodulation techniques.

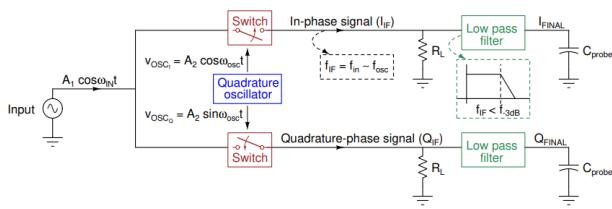


Fig. 1. Block diagram for a Quadrature Down Converter

As shown above, the input signal $v_{in} = A_1 \cos \omega_{in} t$ is mixed with $v_{OSC_I} = A_2 \cos \omega_{OSC} t$ and $v_{OSC_Q} = A_2 \sin \omega_{OSC} t$ to produce in-phase and quadrature-phase signals respectively, with a phase difference of 90° . Mixing of these two signals is the same as their product, which may be simplified to:

$$v_{IF_I} = \frac{A_1 A_2}{2} (\cos(\omega_{in} - \omega_{OSC})t + \cos(\omega_{in} + \omega_{OSC})t)$$

$$v_{IF_Q} = \frac{A_1 A_2}{2} (\sin(\omega_{in} + \omega_{OSC})t - \sin(\omega_{in} - \omega_{OSC})t)$$

These signals are fed to a low-pass filter so that only the difference frequency is obtained at I_{FINAL} and Q_{FINAL} , which is quite low, and the very high sum frequency is filtered out.

In this project, we design and simulate a quadrature down-converter using analog building blocks such as a quadrature oscillator, mixer (switch), and low-pass filter. All circuit modules are implemented and analyzed using LTSpice. The objective is to demonstrate frequency downconversion of a high-frequency input signal into its intermediate frequency (IF) components while preserving phase information.

The simulation-based approach enables performance evaluation of individual blocks and the complete system, focusing on aspects such as waveform behavior, frequency spectra, and I/Q signal isolation.

II. SIGNIFICANCE AND APPLICATION OF QUADRATURE DOWN CONVERTER

Quadrature down-conversion plays a vital role in modern communication systems due to its ability to process complex modulated signals efficiently. The following points highlight its significance:

A. Information Recovery

Modern digital modulation schemes such as QAM and PSK encode information in both amplitude and phase. To accurately recover this information, the receiver must:

- Preserve both amplitude and phase relationships,
- Process positive and negative frequency components independently,
- Maintain orthogonality between signal components.

The in-phase and quadrature (I-Q) architecture achieves this by utilizing two parallel signal paths with a 90° phase difference.

$$v_{IF_I} = v_{in} \times v_{OSC_I} = \frac{A_1 A_2}{2} (\cos(\omega_{in}t - \omega_{OSC}t) + \cos(\omega_{in}t + \omega_{OSC}t))$$

$$v_{IF_Q} = v_{in} \times v_{OSC_Q} = \frac{A_1 A_2}{2} (\sin(\omega_{in}t + \omega_{OSC}t) - \sin(\omega_{in}t - \omega_{OSC}t))$$

B. Image Rejection

Image rejection is a critical application of quadrature processing. In conventional heterodyne receivers, an image frequency at $2f_{LO} - f_{RF}$ can interfere with the desired signal. Quadrature architectures eliminate this image through internal signal processing, rather than relying on bulky external filters, thus reducing component count and enabling higher levels of integration.

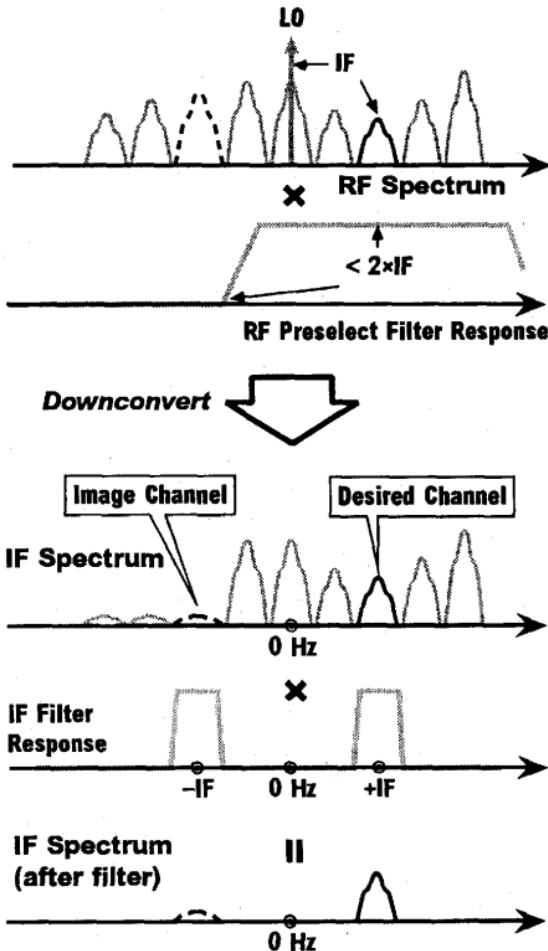


Fig. 2. Image rejection in quadrature processing

C. Spectral Efficiency

Quadrature processing enhances spectral efficiency by transmitting information on both I and Q channels. This effectively doubles the data throughput within the same bandwidth compared to single-channel systems. Such efficiency is essential in modern wireless systems, where spectrum is both scarce and expensive.

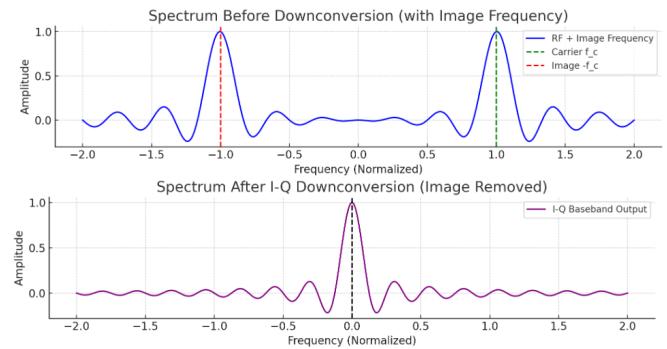


Fig. 3. Orthogonal Demodulation Image term folds into Orthogonal phase and cancels

D. Hardware Simplification and Complex Modulation Support

Quadrature processing simplifies hardware design by:

- Replacing bulky intermediate-frequency (IF) and image-reject filters with integrated analog or digital signal processing,
- Supporting advanced modulation schemes like 64-QAM through independent modulation of I and Q components,
- Enabling software-defined operation compatible with multiple communication standards.

III. QUADRATURE OSCILLATOR

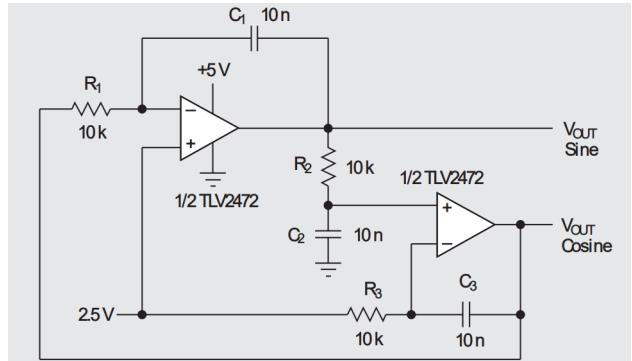


Fig. 4. Schematic of Quadrature oscillator

A quadrature oscillator is designed to generate two sinusoidal signals with a 90° phase difference. The topology employed utilizes two operational amplifiers (op-amps), each contributing to the generation of these phase-shifted waveforms. The circuit, illustrated in Fig. 2, can be understood by analyzing it in two stages.

In the first stage, the initial op-amp functions as an integrator, with a capacitor providing negative feedback from the output to the input. When a sinusoidal input—such as a cosine wave—is applied, the output of this op-amp becomes a sine wave, effectively achieving a 90° phase shift. This output is then passed through an RC filter to suppress high-frequency components.

In the second stage, the filtered signal serves as the input to the second op-amp, which also operates as an integrator.

Consequently, if a sine wave is input to this stage, the output becomes a cosine wave—reconstructing the original input. Through this configuration, the circuit continuously regenerates two sinusoidal signals that are 90° out of phase, thus realizing quadrature oscillation.

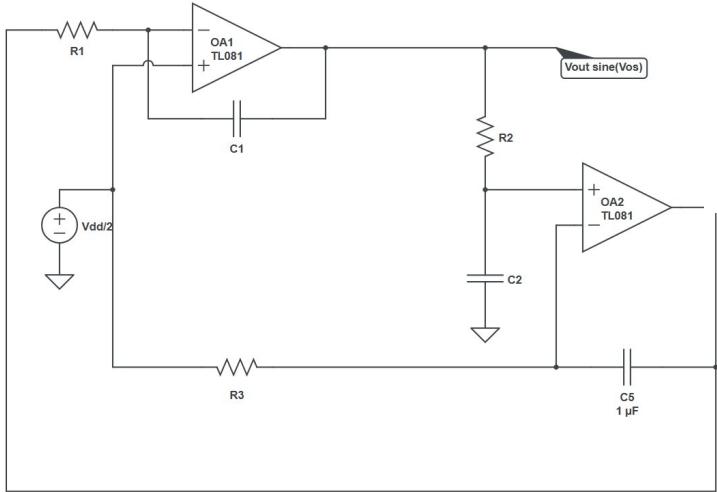


Fig. 5. Topology of Quadrature oscillator

CALCULATIONS

Traversing from V_{OS} to V_{+2} ; V_{+2} to V_{OC} ; V_{OC} to V_{OS} loop:-

- $V_{OS} \rightarrow V_{+2}$

As we can see, it is a simple voltage divider:

$$\Rightarrow V_{+2} = \frac{\frac{1}{C_2 S}}{R_2 + \frac{1}{C_2 S}} V_{OS}$$

$$\Rightarrow V_{+2} = \frac{1}{1 + R_2 C_2 S} V_{OS} \quad (1)$$

- $V_{+2} \rightarrow V_{OC}$

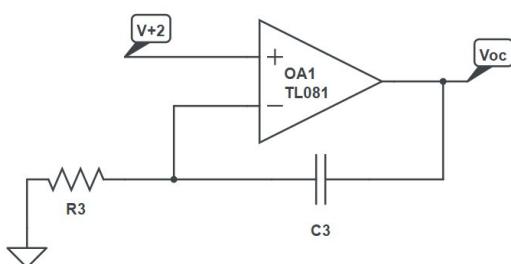


Fig. 6. Non-Inverting Amplifier

$$V_{OC} = \left(1 + \frac{\frac{1}{C_3 S}}{R_3} \right) V_{+2}$$

$$\Rightarrow V_{OC} = \frac{1 + R_3 C_3 S}{R_3 C_3 S} V_{+2} \quad (2)$$

- $V_{OC} \rightarrow V_{OS}$

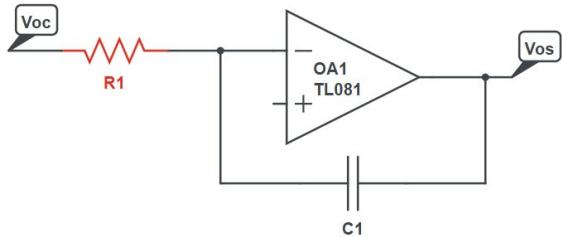


Fig. 7. Inverting Amplifier

$$V_{OS} = \left(-\frac{\frac{1}{C_1 S}}{R_1} \right) V_{OC}$$

$$\Rightarrow V_{OS} = -\frac{1}{R_1 C_1 S} V_{OC} \quad (3)$$

The loop gain of the system should be 1 for a stable oscillation.

$$\Rightarrow (1) \times (2) \times (3) = 1$$

$$-\frac{1}{R_1 C_1 S} \times \frac{1 + R_3 C_3 S}{R_3 C_3 S} \times \frac{1}{1 + R_2 C_2 S} = 1$$

Substituting $S = j\omega$, we get

$$-\frac{1}{R_1 C_1(j\omega)} \times \frac{1 + R_3 C_3(j\omega)}{R_3 C_3(j\omega)} \times \frac{1}{1 + R_2 C_2(j\omega)} = 1$$

For practical purposes let us design it such that

$$\Rightarrow R_1 C_1 = R_2 C_2 = R_3 C_3 \quad (4)$$

$$\Rightarrow -\frac{1}{(RC)^2 (j\omega_0)^2} = 1$$

$$\Rightarrow \omega_0 = -\frac{1}{RC}$$

$$\Rightarrow f_{osc} = \frac{\omega_{osc}}{2\pi} = \frac{1}{2\pi RC} \quad (5)$$

$$\Rightarrow RC = \frac{1}{2\pi f_{osc}}$$

→ We are required to obtain $f_{osc} = 100\text{KHz}$

$$\Rightarrow RC = \frac{1}{2\pi \times 100 \times 10^3} \approx 1.59 \times 10^{-6}$$

→ For our circuit let's take the value of

$$\boxed{R = 5K\Omega} \quad (6)$$

$$\Rightarrow C = 0.318nF$$

$$\boxed{C \approx 0.32nF} \quad (7)$$

→ V_{DD}/V_{SS} depends upon the Op-Amp model selection. In our case, we have used UA741. So we will take $V_{DD} = 5V$ and $V_{SS} = 2.5V$

A. Simulations

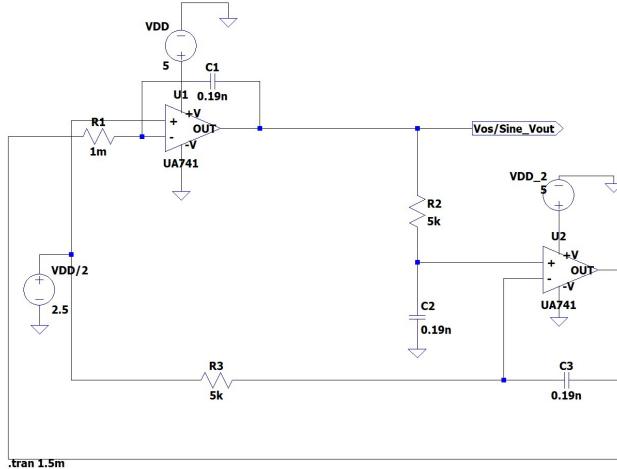


Fig. 8. Realizing oscillator on LTSPICE.

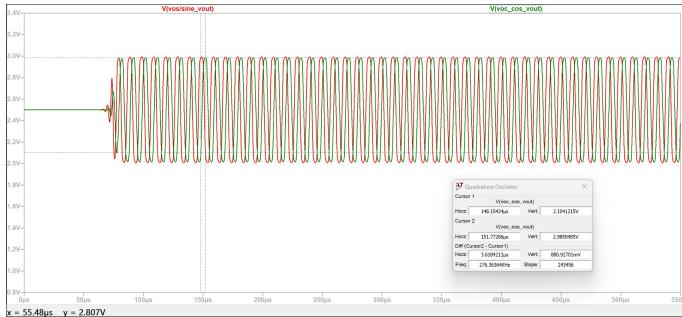


Fig. 9.

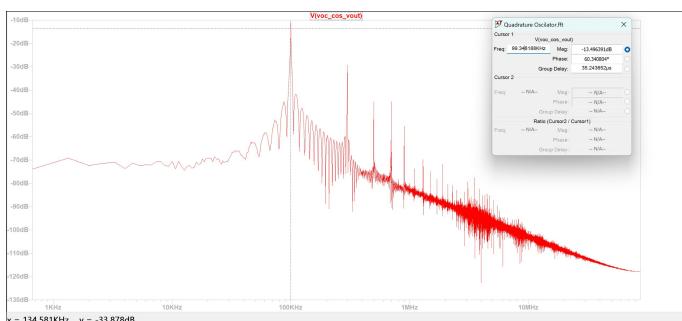


Fig. 10. FFT plot of Cosine wave which is output of our simulation

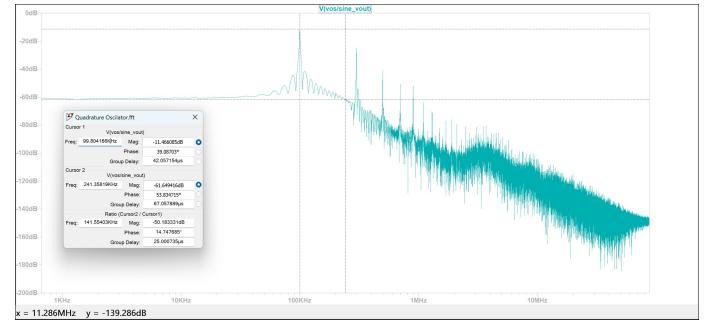


Fig. 11. FFT plot of Sine wave which is output of our simulation

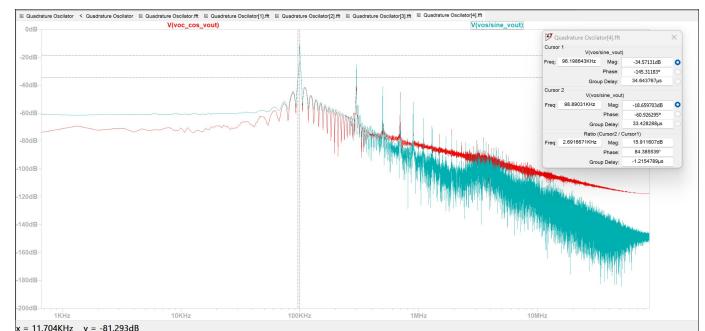


Fig. 12. Combined FFT plot showing 90° phase difference

IV. SWITCH(MIXER) DESIGN

The primary goal of our project is to down-convert a high-frequency input signal to a lower output frequency. Specifically, Our aim is to extract the original message frequency from a modulated input signal that comprises both the carrier and the message frequencies. This is accomplished by generating a high-amplitude signal at the desired message frequency and filtering out all unwanted frequency components.

The core device used for this frequency translation is the mixer, which combines the message signal with a signal generated by a quadrature oscillator. The mixer effectively blends these two inputs to produce new frequency components, including the desired message frequency.

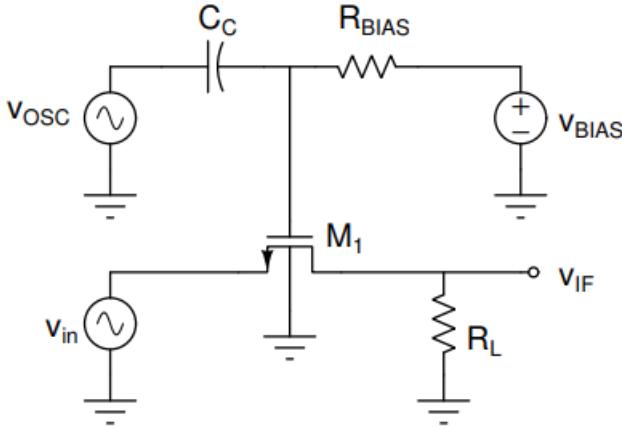


Fig. 13. Switch(Mixer) circuit

A mixer/switch functions as a signal multiplier; it multiplies two input signals. A basic mixer configuration consists of a MOSFET, a coupling capacitor, a bias and a load resistor, and a DC supply as bias voltage.

In our design, the oscillator frequency (V_{OSC}) is set equal to the carrier frequency, while the bias voltage (V_{BIAS}) is chosen close to the MOSFET's threshold voltage. From the perspective of the oscillator, the circuit behaves as a high-pass filter—allowing AC components to pass while blocking DC. Conversely, from the bias voltage side, it acts as a low-pass filter—blocking AC and passing only DC.

As a result, the gate of the MOSFET receives a composite signal: an AC component from the oscillator superimposed on a DC offset provided by (V_{BIAS}) when ($V_{OSC} > 0$), the MOSFET operates in the linear (on) region and when ($V_{OSC} < 0$), it switches off (cutoff region). This alternating on-off behavior essentially mimics a switching action at the oscillator frequency.

A. (Intuitive) Working of Mixer

- From the circuit, the voltage at the gate terminal is observed to be:

$$V_{GS} = V_{OSC} + V_{BIAS} = V_{OSC} + V_T$$

- For the NMOS transistor to conduct, it must be in the linear region, which requires:

$$V_{GS} \geq V_T$$

Conversely, if $V_{GS} < V_T$, the MOSFET operates in the cutoff region.

- During the positive half-cycles of the oscillator signal:

$$V_{OSC} + V_T \geq V_T \Rightarrow V_{GS} \geq V_T$$

This implies the MOSFET is on, allowing the signal at the source terminal to pass through to the drain terminal, where the mixer output is taken.

- During the negative half-cycles of the oscillator signal, by similar reasoning, $V_{GS} < V_T$. Hence, the MOSFET

turns off, and the channel between source and drain is cut off.

- Since the oscillator frequency is high, the signal rapidly oscillates between positive and negative values, effectively switching the MOSFET on and off. This switching behavior produces a square-wave-like modulation that mixes with the input signal at the output of the mixer.

B. Design, Simulation and Results

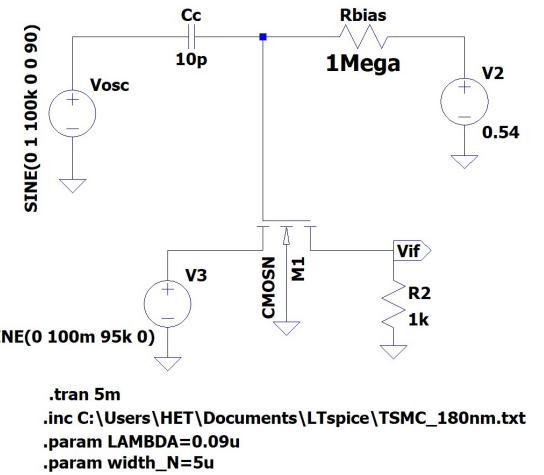


Fig. 14. LTSpice circuit for Mixer

In this design, $R_{BIAS} = 1M\Omega$ and $C_c = 10pF$. Bias voltage is taken to be just greater than the threshold voltage of the MOSFET so that we can observe a properly on and off switching MOSFET. The NMOS used in our design has the following characteristics:

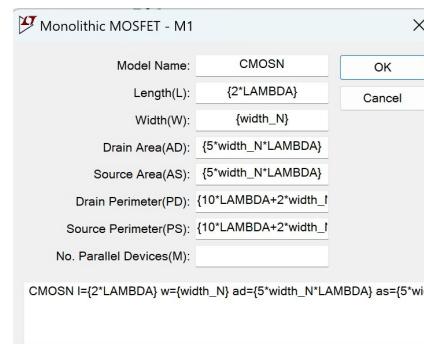


Fig. 15. NMOS Parameters for simulation

The following are the time domain plots and FFTs of the mixer outputs for various input frequencies:

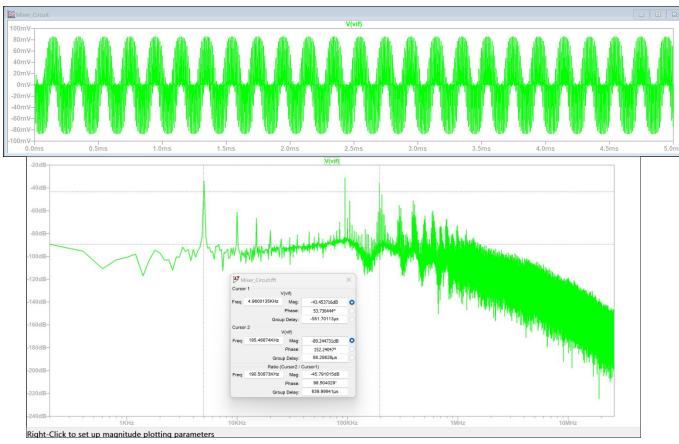


Fig. 16. Frequency and Transient response at FIN = 95KHz, we get peaks at 5KHz, 95KHz, and 195KHz.

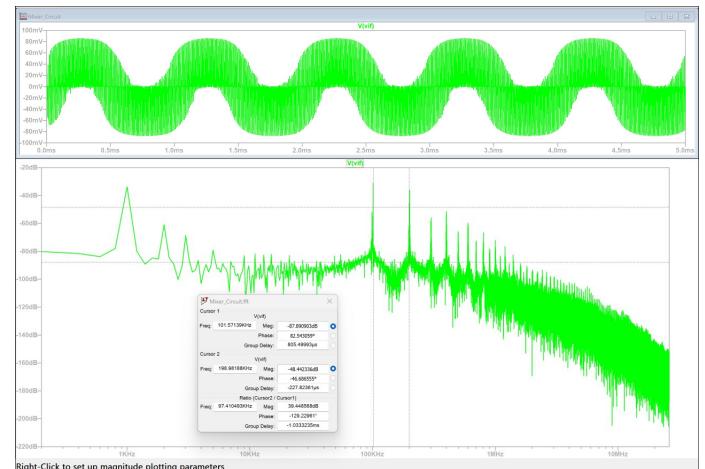


Fig. 19. Frequency and Transient response at FIN = 101KHz, we get peaks at 101KHz,201KHz.

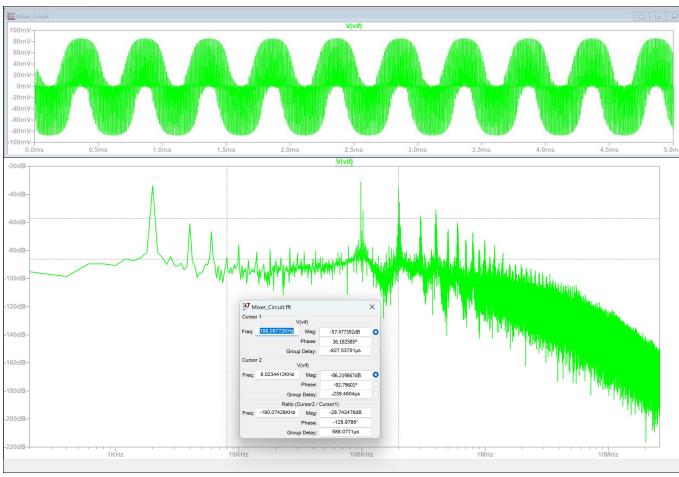


Fig. 17. Frequency and Transient response at FIN = 98KHz, we get peaks at 5K 98KHz, 198KHz.

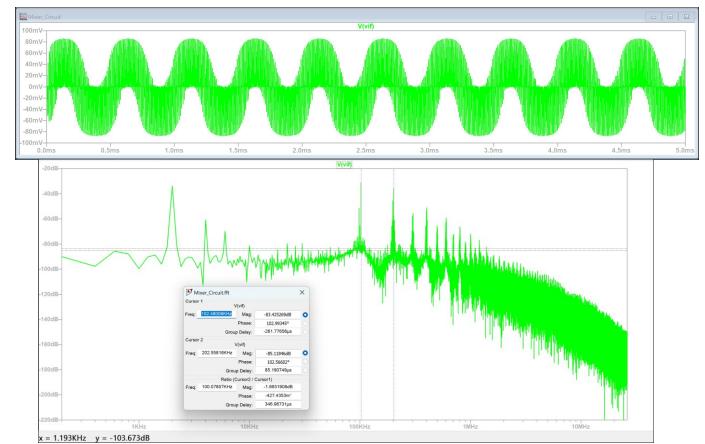


Fig. 20. Frequency and Transient response at FIN = 102KHz, we get peaks at 102KHz, 202KHz.

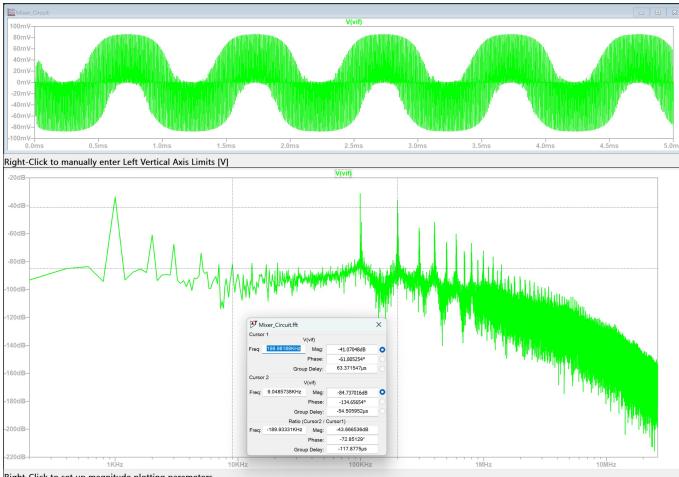


Fig. 18. Frequency and Transient response at FIN = 99KHz, we get peaks at 99KHz, 199KHz.

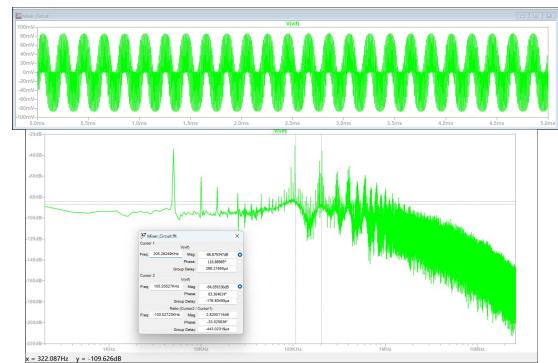


Fig. 21. Frequency and Transient response at FIN = 105KHz, we get peaks at 105 KHz, 205KHz.

V. LOW PASS FILTER

A low-pass filter is an electronic circuit that allows low-frequency signals to pass through while attenuating (reducing)

high-frequency components. Its operation is based on the frequency-dependent impedance of its components—typically resistors and capacitors in an RC configuration.

A. Working of Low Pass Filter

- At low frequencies, the capacitor behaves like an open circuit, allowing signals to pass through with minimal attenuation.
- At high frequencies, the capacitor acts as a short circuit, diverting the signal away from the output.
- The RC low-pass filter functions as a frequency-dependent voltage divider:
 - At low frequencies, most of the input voltage appears across the output (across the capacitor).
 - At high frequencies, more voltage is dropped across the resistor, resulting in reduced output amplitude.
- The resistor controls the current flow into the capacitor and influences the capacitor's charging and discharging rate.

B. Determination of Cutoff Frequency, R and C

The cutoff frequency f_c is the point where the filter starts to attenuate higher-frequency signals significantly. It is determined using the resistor R and capacitor C values, given by the formula:

$$f_c = \frac{1}{2\pi RC} \quad (8)$$

1) Formulae:

$$\text{Intensity} = 20 \log_{10} |H(\omega)|$$

where $H(\omega)$ is the transfer function in frequency response of system

$$V_{out} = \frac{X_c}{X_c + R} V_{in} = \frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + R} V_{in}$$

where Capacitor Impedance, $X_c = \frac{1}{j\omega C}$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega RC}$$

Amplitude Gain

$$= -20 \log_{10} \frac{1}{1 + j\omega RC}$$

2) Calculations:

$$f_c = \frac{1}{2\pi RC} = 2\text{KHz}$$

We have taken $R = 2\text{K}\Omega$

$$\Rightarrow C = \frac{1}{2\pi R f_c} = \frac{1}{2\pi \times 2 \times 10^3 \times 2 \times 10^3} = 3.979 \times 10^{-8} F \approx 39.79 \text{nF}$$

C. Simulations

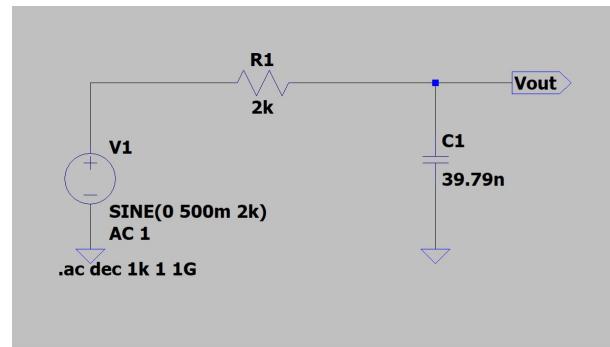


Fig. 22. Realizing RC low pass filter with cut off frequency 2KHz on LTSPICE.

1) Frequency Response: The frequency response shows a change in behavior near 1.99 KHz(cutoff frequency), marking significant attenuation as it approaches 1 kHz (input signal frequency).

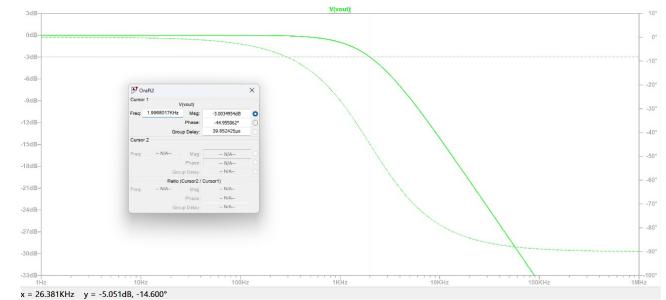


Fig. 23. Frequency response of RC low pass filter

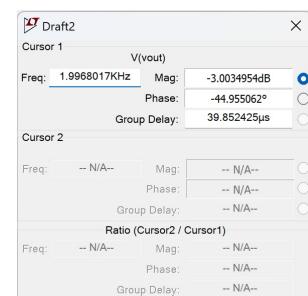


Fig. 24. we get -3dB frequency at 1.99KHz.

2) Transient Response: The transient response illustrates how the filter behaves under different frequency inputs (e.g., 20 kHz, 10 kHz, 1 kHz), showing varying degrees of attenuation and signal shaping.

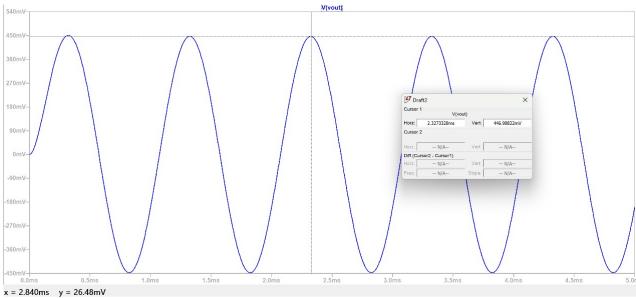


Fig. 25. Frequency = 1k

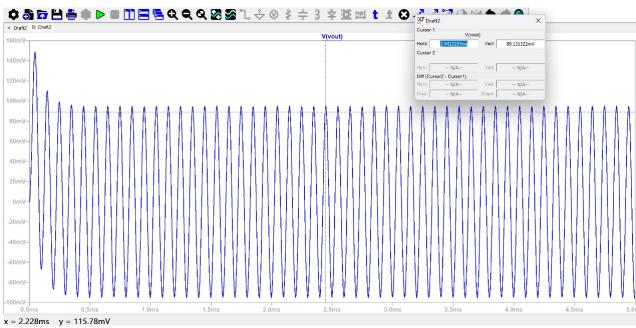


Fig. 26. Frequency = 10k

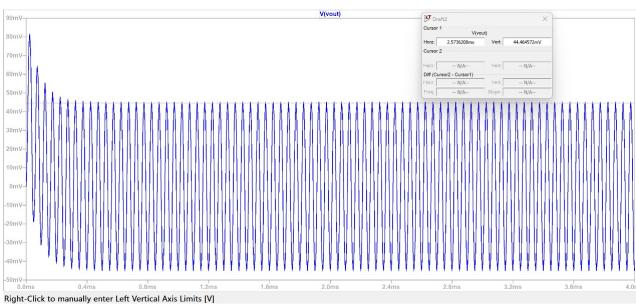


Fig. 27. Frequency = 20k

VI. COMPLETE CIRCUIT PROTOTYPE DESIGN

The first part of our circuit is oscillator, which takes DC voltage as input for VDD, VSS of Op-amps. The output of this oscillator consists of 2 signals, one sine and other cosine, both at a phase difference of 90° . These signals act as oscillator signals in mixer, the cosine output wave is input for the Inphase mixer, and sine wave for quadrature-phase mixer. The input signal for the mixer's, are given from the wave generator. The output of the mixer is passed through the low pass filter to filter out any frequency greater than 2KHz. Finally, we have 2 output signals from the low pass filters, one in-phase component and other quadrature phase component.

A. Complete circuit realized on LTSPICE

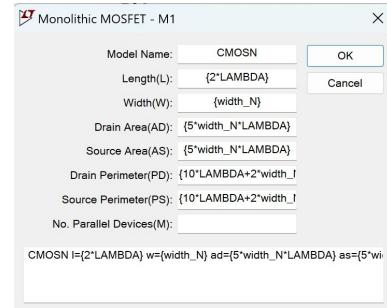


Fig. 29. NMOS Paramerters

B. Simulation Plots and Results

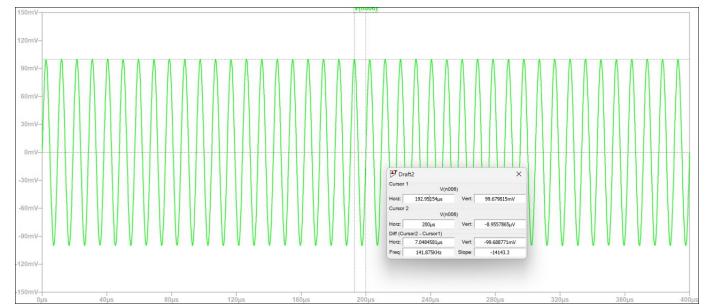


Fig. 30. Input signal with amplitude 100mV, frequency 105KHz.

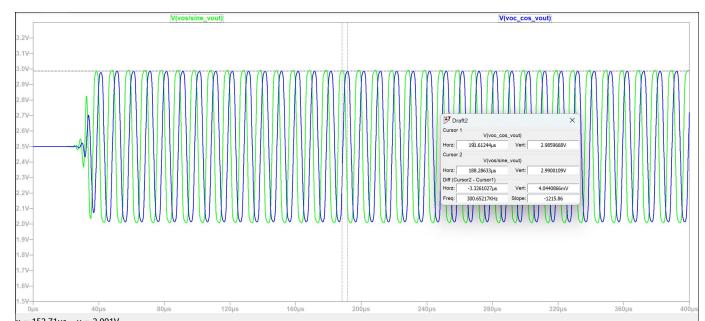


Fig. 31. Transient plots for in-phase and quadrature-phase components of the oscillator, showing 90° phase shift

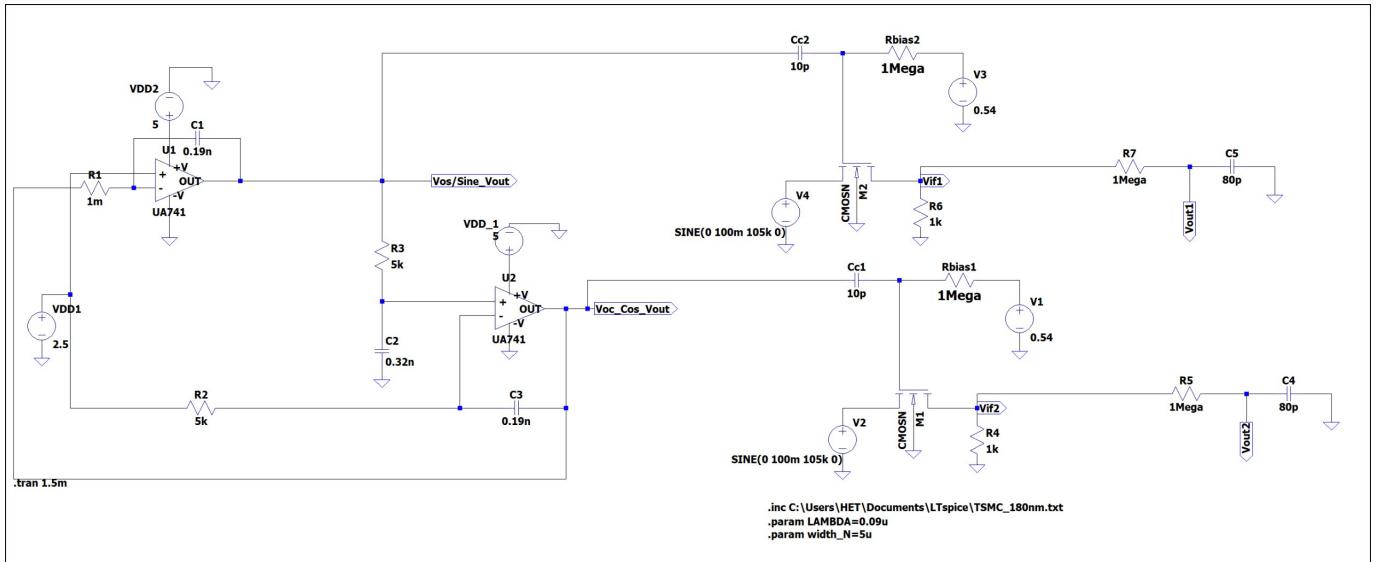


Fig. 28. LTSPICE circuit for the complete QDC prototype

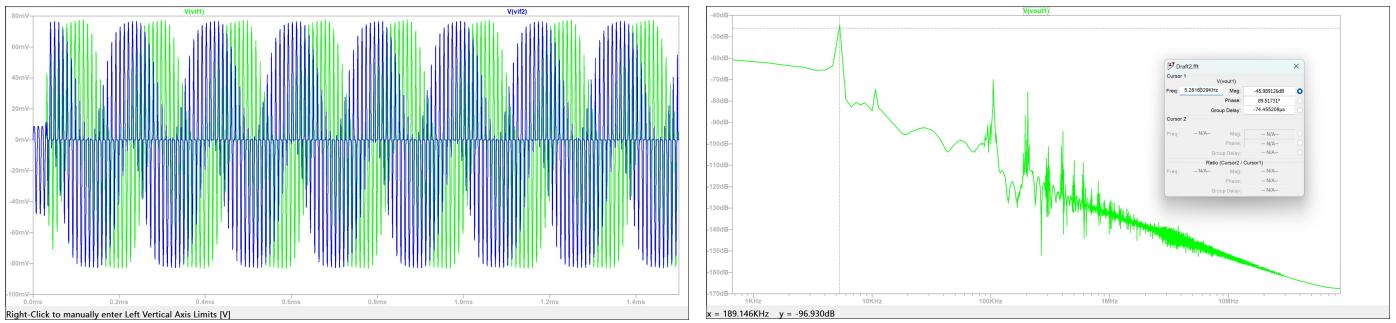


Fig. 32. Output of mixer when the above-mentioned output signals of oscillator and V_{in} are given input to the mixer.

Fig. 34. FFT plot of quadrature-phase output

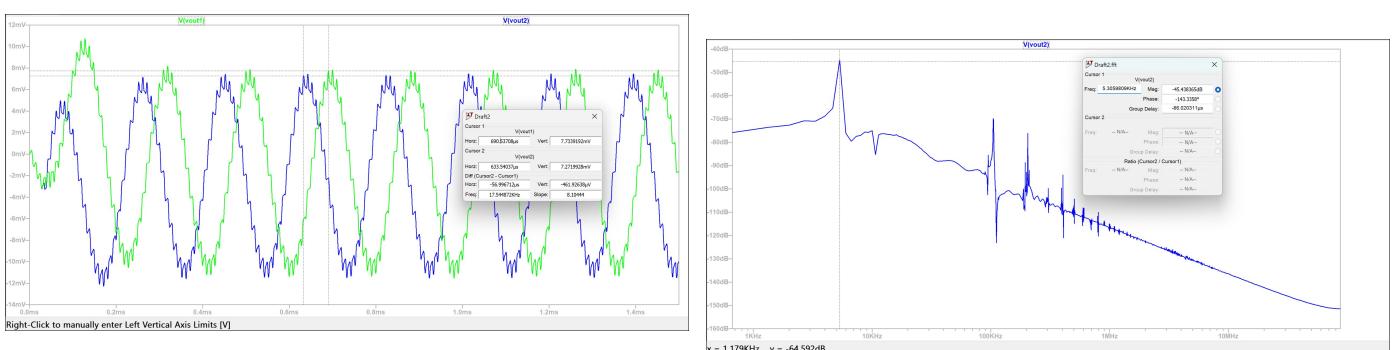


Fig. 33. Final output plot of QDC showing in-phase and quadrature-phase components of input signal with phase difference of 90°

Fig. 35. FFT plot of in-phase output

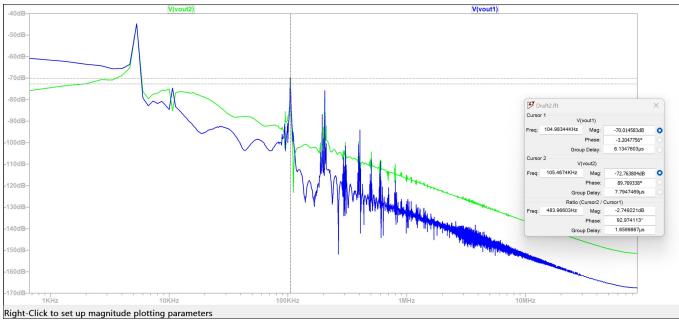


Fig. 36. Combined FFT of both components, shows 92° phase difference

VII. ACKNOWLEDGMENT

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