# 1. Description

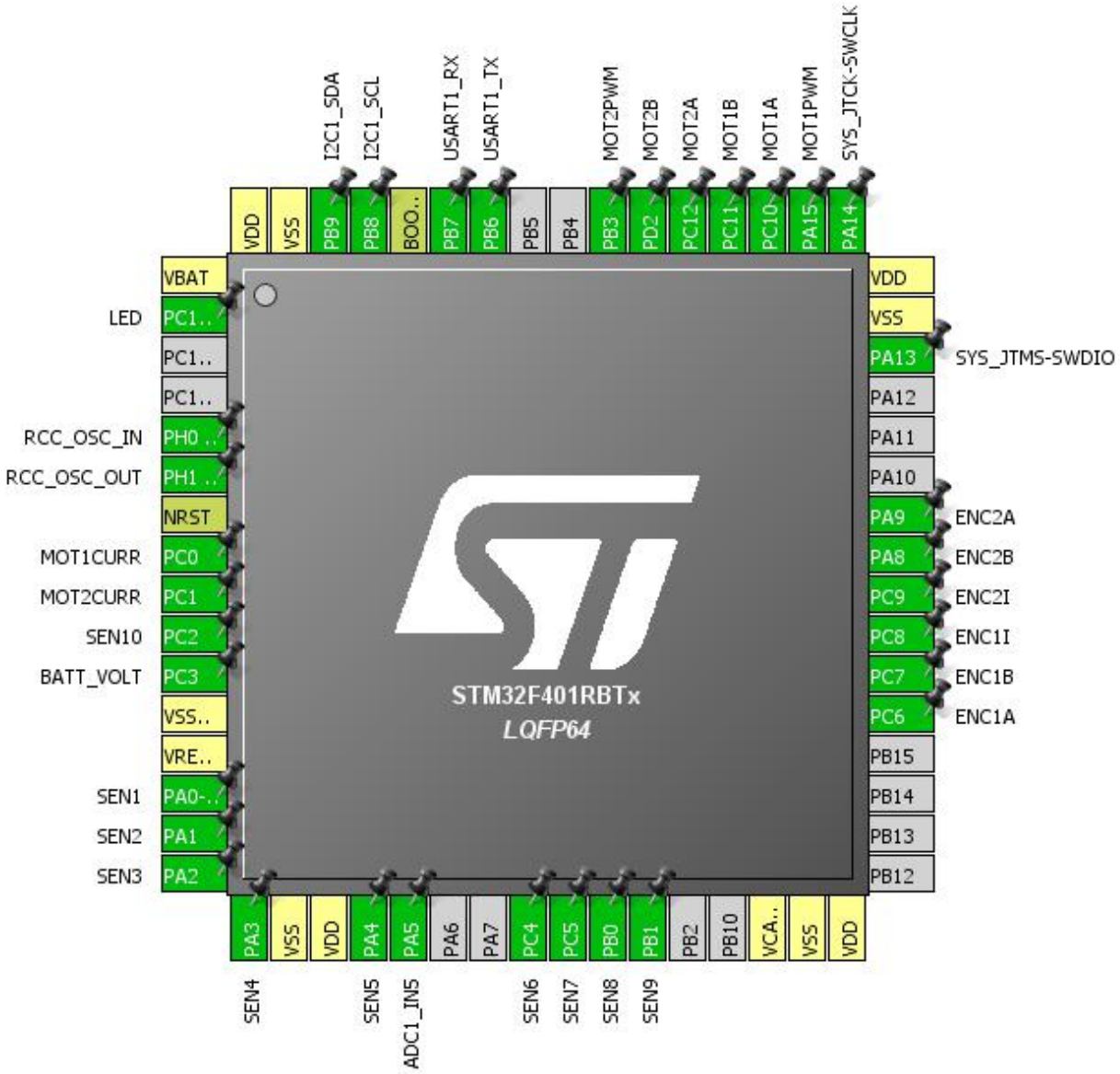
## 1.1. Project

| | |
|---|---|
| Project Name | LF2 |
| Board Name | LF2 |
| Generated with: | STM32CubeMX 4.23.0 |
| Date | 02/26/2018 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F401 |
| MCU name | STM32F401RBTx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

# 2. Pinout Configuration



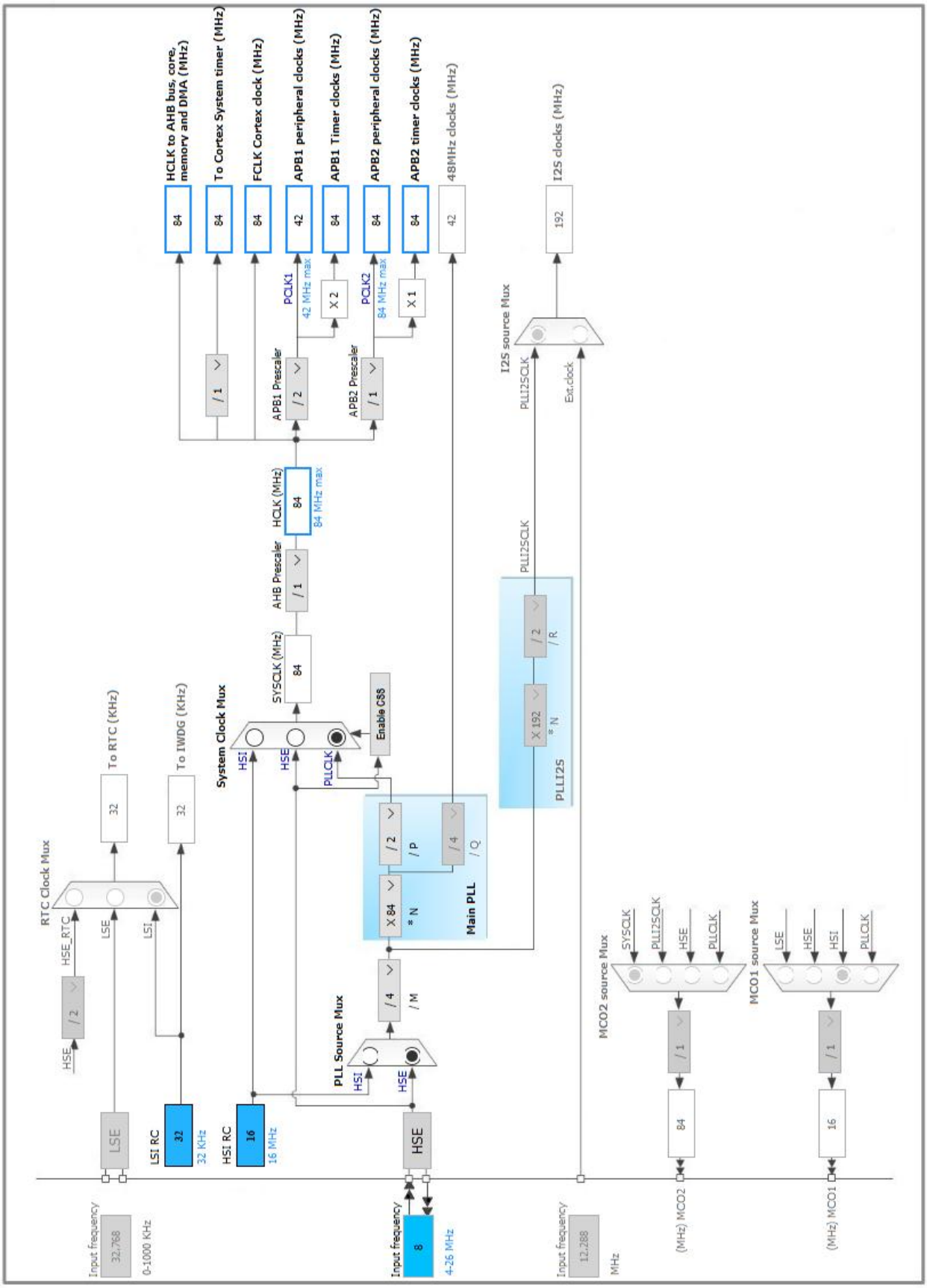
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 2 | PC13-ANTI_TAMP * | I/O | GPIO_Output | LED |
| 5 | PH0 - OSC_IN | I/O | RCC_OSC_IN | |
| 6 | PH1 - OSC_OUT | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 8 | PC0 | I/O | ADC1_IN10 | MOT1CURR |
| 9 | PC1 | I/O | ADC1_IN11 | MOT2CURR |
| 10 | PC2 | I/O | ADC1_IN12 | SEN10 |
| 11 | PC3 | I/O | ADC1_IN13 | BATT_VOLT |
| 12 | VSSA/VREF- | Power | | |
| 13 | VREF+ | Power | | |
| 14 | PA0-WKUP | I/O | ADC1_IN0 | SEN1 |
| 15 | PA1 | I/O | ADC1_IN1 | SEN2 |
| 16 | PA2 | I/O | ADC1_IN2 | SEN3 |
| 17 | PA3 | I/O | ADC1_IN3 | SEN4 |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 20 | PA4 | I/O | ADC1_IN4 | SEN5 |
| 21 | PA5 | I/O | ADC1_IN5 | |
| 24 | PC4 | I/O | ADC1_IN14 | SEN6 |
| 25 | PC5 | I/O | ADC1_IN15 | SEN7 |
| 26 | PB0 | I/O | ADC1_IN8 | SEN8 |
| 27 | PB1 | I/O | ADC1_IN9 | SEN9 |
| 30 | VCAP1 | Power | | |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 37 | PC6 | I/O | TIM3_CH1 | ENC1A |
| 38 | PC7 | I/O | TIM3_CH2 | ENC1B |
| 39 | PC8 * | I/O | GPIO_Input | ENC1I |
| 40 | PC9 * | I/O | GPIO_Input | ENC2I |
| 41 | PA8 | I/O | TIM1_CH1 | ENC2B |
| 42 | PA9 | I/O | TIM1_CH2 | ENC2A |
| 46 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 47 | VSS | Power | | |
| 48 | VDD | Power | | |
| 49 | PA14 | I/O | SYS_JTCK-SWCLK | |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 50 | PA15 | I/O | TIM2_CH1 | MOT1PWM |
| 51 | PC10 * | I/O | GPIO_Output | MOT1A |
| 52 | PC11 * | I/O | GPIO_Output | MOT1B |
| 53 | PC12 * | I/O | GPIO_Output | MOT2A |
| 54 | PD2 * | I/O | GPIO_Output | MOT2B |
| 55 | PB3 | I/O | TIM2_CH2 | MOT2PWM |
| 58 | PB6 | I/O | USART1_TX | |
| 59 | PB7 | I/O | USART1_RX | |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 | I/O | I2C1_SCL | |
| 62 | PB9 | I/O | I2C1_SDA | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. ADC1

**mode: IN0**
**mode: IN1**
**mode: IN2**
**mode: IN3**
**mode: IN4**
**mode: IN5**
**mode: IN8**
**mode: IN9**
**mode: IN10**
**mode: IN11**
**mode: IN12**
**mode: IN13**
**mode: IN14**
**mode: IN15**

### 5.1.1. Parameter Settings:

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 6 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | **Enabled *** |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | **EOC flag at the end of all conversions *** |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | **14 *** |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel 12 *** |
| Sampling Time | **144 Cycles *** |

| | |
|---|---|
| Rank | **2 *** |
| Channel | **Channel 9 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **3 *** |
| Channel | **Channel 8 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **4 *** |
| Channel | **Channel 15 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **5 *** |
| Channel | **Channel 14 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **6 *** |
| Channel | **Channel 5 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **7 *** |
| Channel | **Channel 3 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **8 *** |
| Channel | **Channel 2 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **9 *** |
| Channel | **Channel 1 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **10 *** |
| Channel | Channel 0 |
| Sampling Time | **144 Cycles *** |
| Rank | **11 *** |
| Channel | **Channel 10 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **12 *** |
| Channel | **Channel 11 *** |
| Sampling Time | **144 Cycles *** |
| Rank | **13 *** |
| Channel | **Channel 13 *** |
| Sampling Time | **144 Cycles *** |

| | |
|---|---|
| Rank | **14 *** |
| Channel | **Channel 4 *** |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *5.2. I2C1*

**I2C: I2C**

### 5.2.1. Parameter Settings:

**Master Features:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Clock Speed (Hz) | 100000 |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |
| General Call address detection | Disabled |

## *5.3. RCC*

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

### 5.3.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 2 WS (3 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |

| | |
|---|---|
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 2 |

## 5.4. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 5.5. TIM1

**Combined Channels: Encoder Mode**

### 5.5.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **65535 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Encoder:**

| | |
|---|---|
| Encoder Mode | **Encoder Mode TI1 and TI2 *** |
| ____ Parameters for Channel 1 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |

## 5.6. TIM2

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

### 5.6.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **23 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **99 *** |
| Internal Clock Division (CKD) | No Division |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## 5.7. TIM3

**Combined Channels: Encoder Mode**

### 5.7.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **65535 *** |

| | |
|---|---|
| Internal Clock Division (CKD) | No Division |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Encoder:**

| | |
|---|---|
| Encoder Mode | **Encoder Mode TI1 and TI2 *** |
| ____ Parameters for Channel 1 ____ | |
| Polarity | **Falling Edge *** |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |

## *5.8. TIM11*

**mode: Activated**

### 5.8.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **999 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **167 *** |
| Internal Clock Division (CKD) | No Division |

## *5.9. USART1*

**Mode: Asynchronous**

### 5.9.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |

| | |
|---|---|
| Parity | None |
| Stop Bits | 1 |

### Advanced Parameters:

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC0 | ADC1_IN10 | Analog mode | No pull-up and no pull-down | n/a | MOT1CURR |
| | PC1 | ADC1_IN11 | Analog mode | No pull-up and no pull-down | n/a | MOT2CURR |
| | PC2 | ADC1_IN12 | Analog mode | No pull-up and no pull-down | n/a | SEN10 |
| | PC3 | ADC1_IN13 | Analog mode | No pull-up and no pull-down | n/a | BATT_VOLT |
| | PA0-WKUP | ADC1_IN0 | Analog mode | No pull-up and no pull-down | n/a | SEN1 |
| | PA1 | ADC1_IN1 | Analog mode | No pull-up and no pull-down | n/a | SEN2 |
| | PA2 | ADC1_IN2 | Analog mode | No pull-up and no pull-down | n/a | SEN3 |
| | PA3 | ADC1_IN3 | Analog mode | No pull-up and no pull-down | n/a | SEN4 |
| | PA4 | ADC1_IN4 | Analog mode | No pull-up and no pull-down | n/a | SEN5 |
| | PA5 | ADC1_IN5 | Analog mode | No pull-up and no pull-down | n/a | |
| | PC4 | ADC1_IN14 | Analog mode | No pull-up and no pull-down | n/a | SEN6 |
| | PC5 | ADC1_IN15 | Analog mode | No pull-up and no pull-down | n/a | SEN7 |
| | PB0 | ADC1_IN8 | Analog mode | No pull-up and no pull-down | n/a | SEN8 |
| | PB1 | ADC1_IN9 | Analog mode | No pull-up and no pull-down | n/a | SEN9 |
| I2C1 | PB8 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | |
| | PB9 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | |
| RCC | PH0 - OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1 - OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM1 | PA8 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | ENC2B |
| | PA9 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | ENC2A |
| TIM2 | PA15 | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | MOT1PWM |
| | PB3 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | MOT2PWM |
| TIM3 | PC6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | ENC1A |
| | PC7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | ENC1B |
| USART1 | PB6 | USART1_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PB7 | USART1_RX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| GPIO | PC13-ANTI_TAMP | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED |
| | PC8 | GPIO_Input | Input mode | **Pull-up *** | n/a | ENC1I |
| | PC9 | GPIO_Input | Input mode | **Pull-up *** | n/a | ENC2I |
| | PC10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | MOT1A |
| | PC11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | MOT1B |
| | PC12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | MOT2A |
| | PD2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | MOT2B |

## 6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| ADC1 | DMA2_Stream0 | Peripheral To Memory | Low |
| USART1_RX | DMA2_Stream2 | Peripheral To Memory | Low |

### *ADC1: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *USART1_RX: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| TIM1 break interrupt and TIM9 global interrupt | true | 0 | 0 |
| TIM1 update interrupt and TIM10 global interrupt | true | 0 | 0 |
| TIM1 trigger and commutation interrupts and TIM11 global interrupt | true | 0 | 0 |
| TIM1 capture compare interrupt | true | 0 | 0 |
| TIM3 global interrupt | true | 0 | 0 |
| USART1 global interrupt | true | 1 | 0 |
| DMA2 stream0 global interrupt | true | 0 | 0 |
| DMA2 stream2 global interrupt | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1 global interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F401 |
| MCU | STM32F401RBTx |
| Datasheet | 024738_Rev8 |

7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | null |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | LF2 |
| Project Folder | C:\Users\matt\Documents\STM CUBE\LF2 |
| Toolchain / IDE | EWARM |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.18.0 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |