EE 224 Project
Version 0.01

This semester, you will be designing an E5M3 floating point multiplier. This multiplier is intended for use in AI chips. It is 9 bits (There is a sign bit also). The data is encoded as:

What	Bits	Comment
S	1	Floating point is sign magnitude
E	5	The exponent. In Excess 15 format
M	3	The fraction (the actual fraction is 4 bits. There is an assumed hidden 1)

This is one more bit than the NVIDIA 8 bit format. However, the hardware can accept E5M2 by setting the low order bit to zero. This allows working with data created for the E5M2 standard.

The floating point multiplier has two 9 bit inputs A and B, and produces a 9 bit output Z. There is a push_in signal, and the design provides a push_out signal. The push signals indicate when data is present on the module input, and results available on the module output. The goal is a 2Ghz clock. The design may be broken into pipeline stages if required.

Speed is important in this design. The multiplier Does not produce any errors. Instead, it "saturates" to a largest and smallest number. Saturation to the largest number is an exponent of 11111 with a Mantissa of 100, and the smallest exponent is anything less than zero which is converted to a true zero. (E 00000 M 000).

For this design, clock rate is more important than cost. The multiplier may be faster in complementary CMOS.

A zero is indicated by the E and M fields being zero. The sign is ignored in determining a zero. (Yes, FP has a -0)

A test bench written in VerilogA will be provided. You should pass the test bench for full credit.

Search online for descriptions of IEEE floating point as background. The IEEE floating point spec is available from the library (online is easiest). Search for ISBN : 1-5044-5924-5 (or IEEE Std 754)