Experiment 3: Combinational Circuit 3

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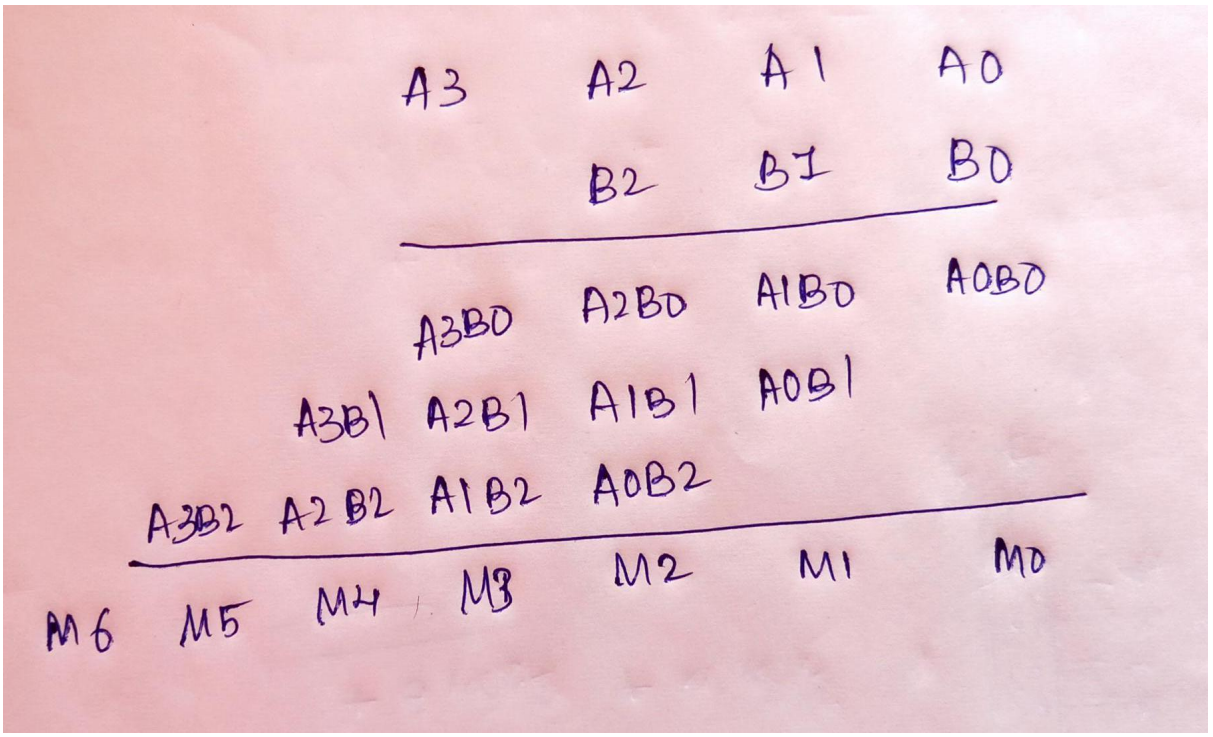
Overview of the experiment:

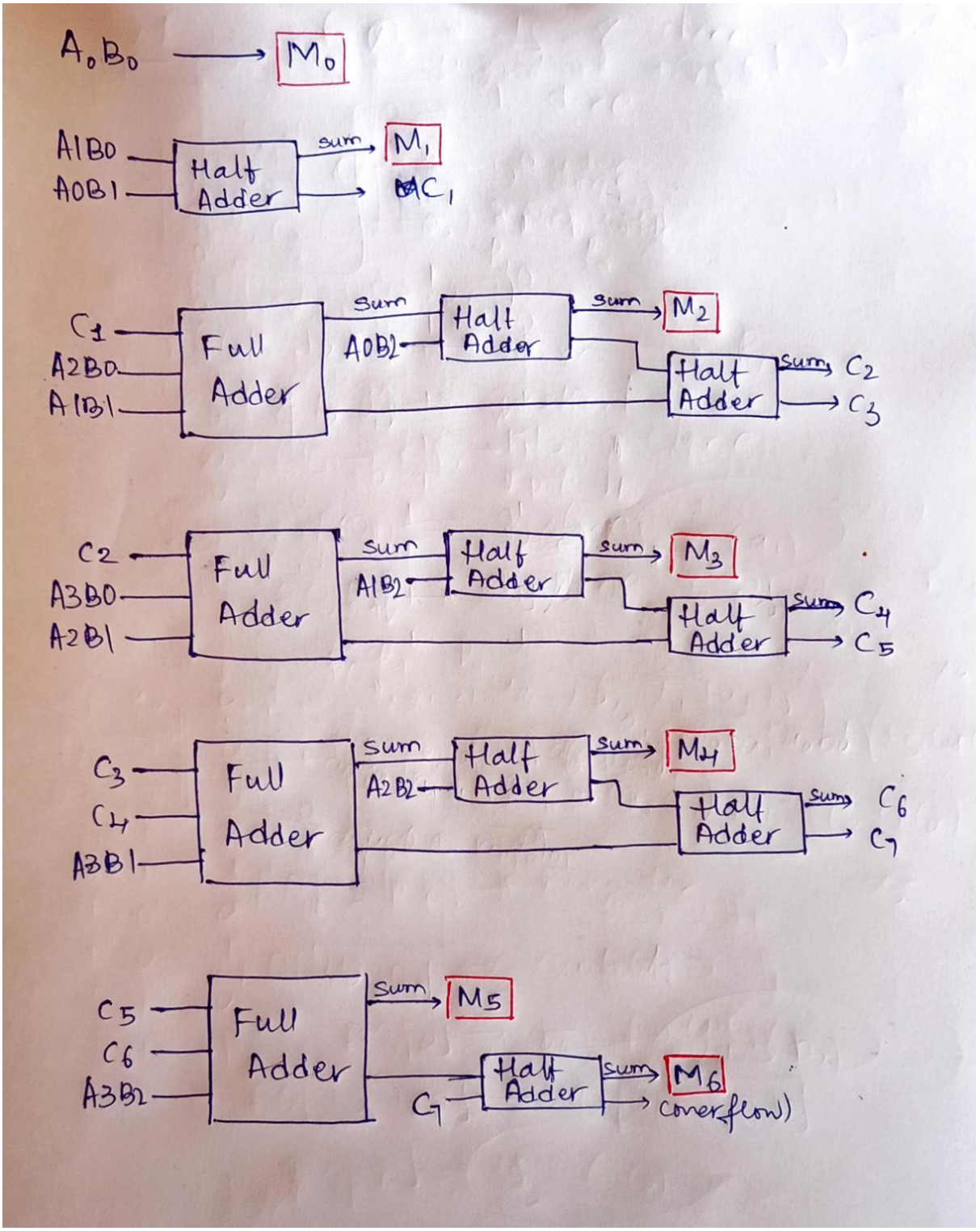
The purpose of the experiment is to build a multiplier circuit of one 4 bit input and one 3 bit input and test the correctness of that using test cases.
In this report I present in a brief how the experiment was conducted and would also present the results of the experiment

Approach to the experiment:

A 4 bit binary number $A3A2A1A0$ is multiplied with a 3 digit binary number $B2B1B0$ their product is given by.



The circuit diagram of the above logic expression constructed by the use of Half adders and Full adders is as below.



The 7 bit binary number $M6M5M4M3M2M1M0$ is the output of the multiplier

Design document and VHDL code

For the experiment an entity was created for the multiplier with suitable inputs and outputs. The architecture “struct” of the entity made use of the And gate and half adder from “Gates” file which was loaded in as package and full adder from “Fulladder” file loaded in as a package “FA”.

The architecture of this is as follows

```
architecture struct of Mult4x3 is
  signal c1,c2,c3,c4,c5,c6,c7,x1,x2,x3,y1,y2,y3,y4,z1,z2,z3,q,d1,d2,d3,d4,d5,
  d6,d7,d8,d9,d10,d11: std_logic;
begin
    v:AND_2 port map (A => A0,B => B0,Y => M0);
        v1:AND_2 port map (A => A1,B => B0,Y =>d1 );
        v2:AND_2 port map (A => A0,B => B1,Y => d2);
        v3:AND_2 port map (A => A2,B => B0,Y => d3);
        v4:AND_2 port map (A => A1,B => B1,Y => d4);
        v5:AND_2 port map (A => A0,B => B2,Y => d5);
        v6:AND_2 port map (A => A3,B => B0,Y => d6);
        v7:AND_2 port map (A => A2,B => B1,Y => d7);
        v8:AND_2 port map (A => A1,B => B2,Y => d8);
        v9:AND_2 port map (A => A3,B => B1,Y => d9);
        v10:AND_2 port map (A => A2,B => B2,Y => d10);
        v11:AND_2 port map (A => A3,B => B2,Y => d11);
        ha1:HALF_ADDER port map (A => d1,B => d2,S => M1,C => c1);
        fa1:Full_Adder port map (A => d3,B => d4,Cin => c1,S => x1,Cout
=>y1 );
        ha2:HALF_ADDER port map (A => x1,B => d5,S => M2,C => z1);
        ha3:HALF_ADDER port map (A => z1,B => y1,S => c2,C => c3);

        fa2:Full_Adder port map (A => d6,B => d7,Cin => c2,S => x2,Cout
=>y2 );
        ha4:HALF_ADDER port map (A => x2,B => d8,S => M3,C => z2);
        ha5:HALF_ADDER port map (A => z2,B => y2,S => c4,C => c5);

        fa3:Full_Adder port map (A => d9,B => c3,Cin => c4,S => x3,Cout
=>y3 );
        ha6:HALF_ADDER port map (A => x3,B => d10,S => M4,C => z3);
        ha7:HALF_ADDER port map (A => z3,B => y3,S => c6,C => c7);
```

fa4:Full_Adder port map (A => d11,B => c5,Cin => c6,S => M5,Cout =>y4);

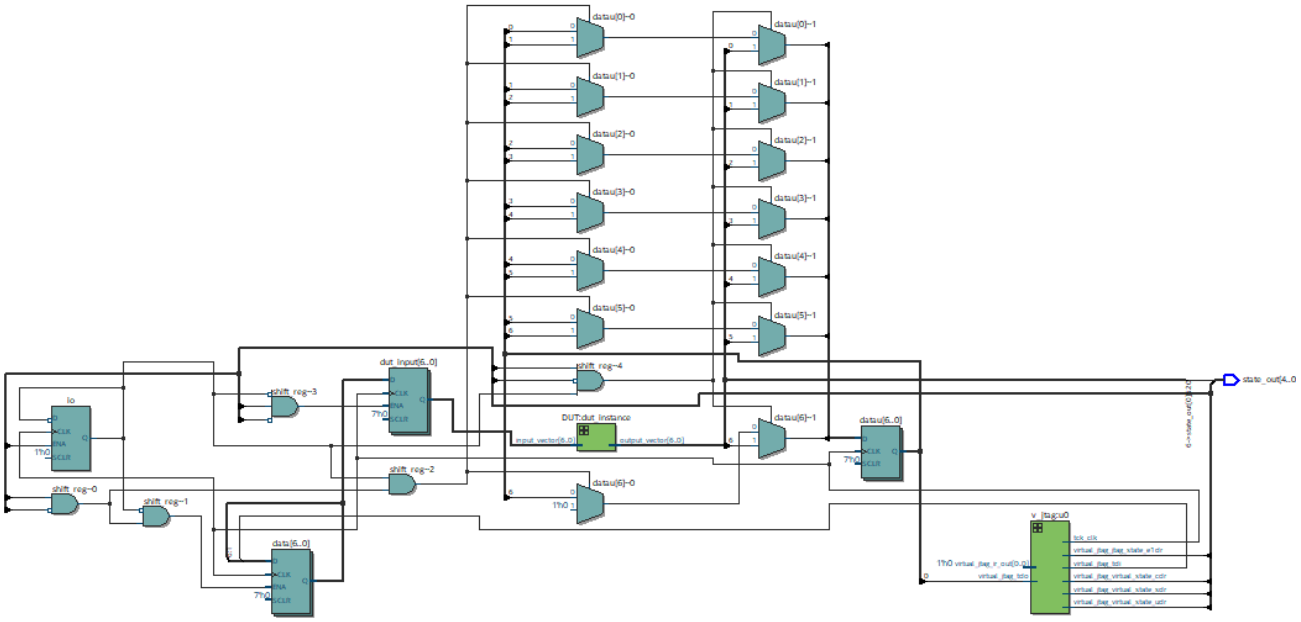
ha8:HALF_ADDER port map (A => y4,B => c7,S => M6,C =>q);

end struct;

In order to test the correctness of the design on hardware we made use of scanchain. This also allowed us to check if our could be actually implemented on hardware. We generated a svf file which was loaded onto the krypton board,which was later used to run the scanchain test.

RTL View:

RTL view of the Multiplier with scanchain



DUT Input/Output Format:

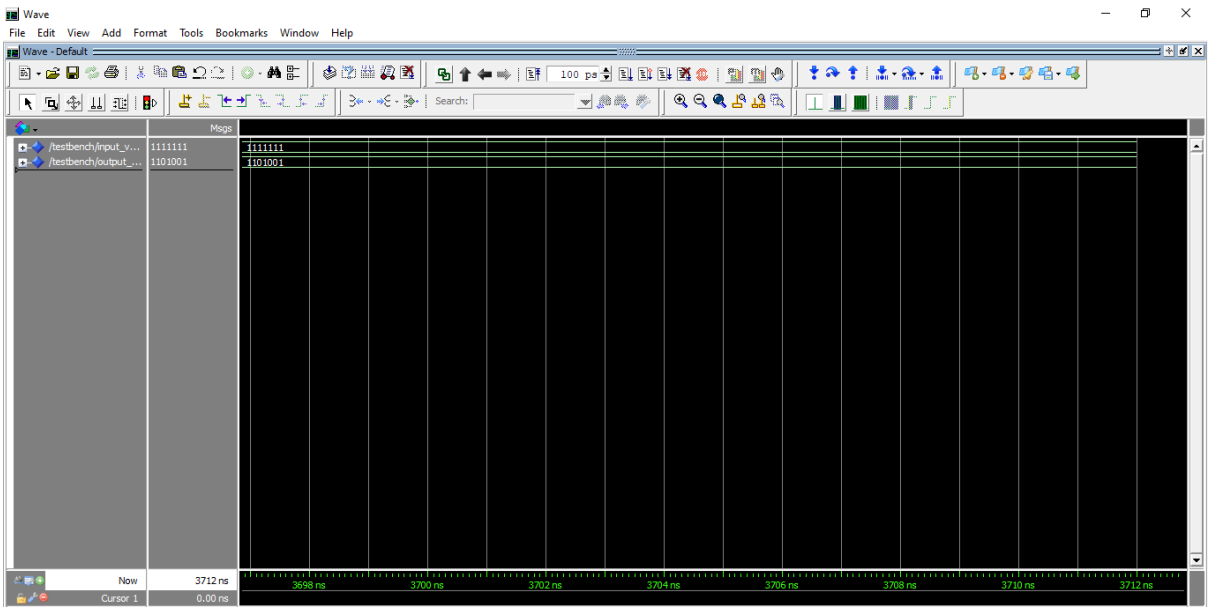
The input vector to the multiplier is of length 7 i.e a 4 bit number$A3A2A1A0$ and a 3 bit number $B2B1B0$. $A3$ is the msb of the input and $B0$ is the output.

Output of the multiplier is a 7 bit number $M6M5M4M3M2M1M0$ as it is evident $M6$ is the msb and $M0$ is the lsb.
Some test cases from the tracefile are

Input	Output
0101010	0001010
0101011	0001111
0101100	0010100
0101101	0011001
0101110	0011110
0101111	0100011

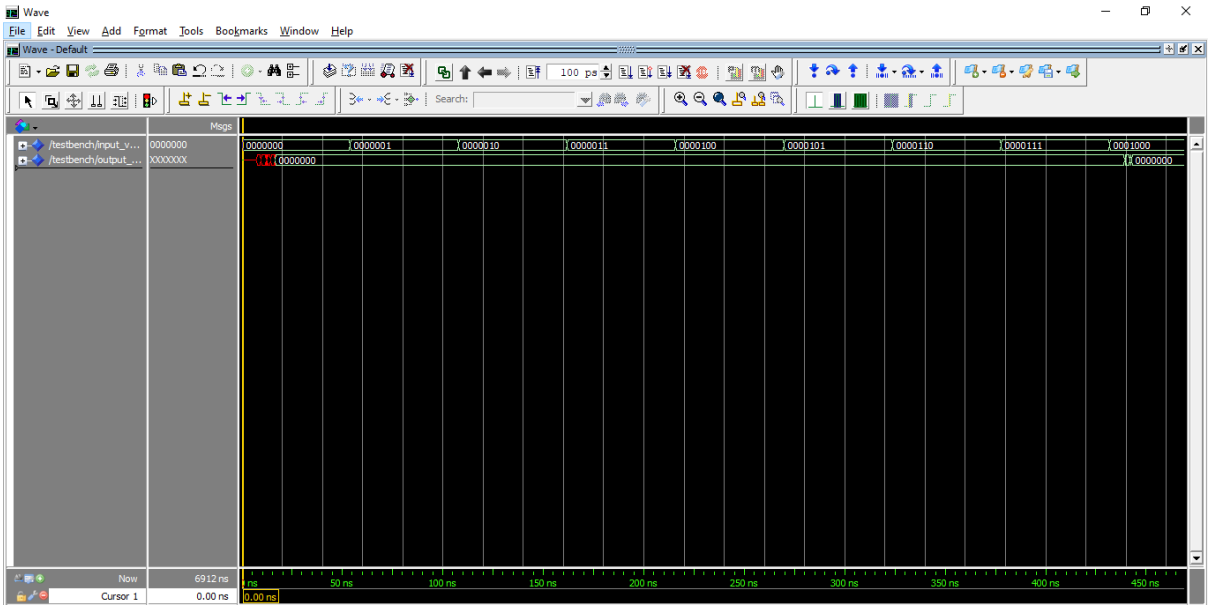
RTL Simulation:

RTL simulation of Multiplier



Gate-level Simulation:

Gate level simulation of Multiplier



Observation:

Upon testing using scanchain we got an output file *out.txt* which contained the result of the experiment. In it we get to see if the design made by us is correct and if the design could be implemented on hardware. All the test cases passed in scanchain which assures the correctness of the design