Rohith R

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Education

BITS Pilani, India
Bachelor of Engineering (Hons.), Computer Science, 2017.
Cumulative Grade Point Average (CGPA) : 7.145
Fields of interest: Operating Systems, Computer Architecture, High Performance and Parallel Computing

Bachelor Thesis

Simulation and Scheduling of Many-Core Architecture
Supervisor : Dr. Lam Siew Kei, Nanyang Technological University
Research involves finding efficient scheduling algorithms taking into consideration the effects of difference in the performance of the cores and their reliability.
Using a mathematical model to evaluate the efficiency of cores based on frequency, process variation and electromigration. Integrating Hotspot, McPat and Snipersim to build a power and thermal aware scheduler inside Sniper and evaluating reliablity of the system at various epochs and optimise MTTF.

Work Experience

Intuit IDC, Bangalore
Software Developer Intern
Project: Enabling Drag-and-Drop in Multi-Window mode, android-N
Collaborated with Intuit and Google engineers to get review of work

State e-gov agency, Chennai
Software Developer Intern
Project: Track the bus timings, frequency and routes in real time and update the user using an app

Projects

Improve efficiency of C++ Thrust Library
Mentor : Dr. Santonu Sarkar — Collaborators : **Siemens Research Lab**
Optimised the well-known GPU algorithms like Scan, Reduce, Transpose to use shared memory and provided the exact same abstraction as C++ STL for using the algorithms.
Introduced a new data structure called **Shared Vector** inside Thrust to provide STL like iterator over shared memory.

Evaluted the performance using well-known benchmarks and got 18% increase in performance compared to existing Thrust library and 11% LOC decrease compared to native cuda implementation.

BITS-OS and MIT-JOS
Basic OS from scratch, for learning low level operations of OS
Implemented VGA, keyboard, hardware clock drivers along with mini shell

Completed MIT-6.828 Postgraduate OS Labs in 2nd year
Implemented Backtrace, Paging, Memory and Process Management in JOS kernel

MIPS Architecture and Cache design
Mentor : Dr. Biju K.R.
Implemented VLIW architecture with 5 stage pipeline
Studied and implemented advanced caches like Phase, Way-Prediction and Way-Halting caches in Verilog

Cluster computing using Raspberry Pi
Made a cluster of Raspberry Pi's and did job scheduling
Implemented a dynamic load balancing algorithm to distribute tasks and evaluated performance of the new scheduling algorithm.

Teaching/ Mentoring

Department of Computer Science, BITS Pilani
Teaching Assistant, Data Structures and Algorithms, Spring,2016

Technology Incubator Programme, BITS Pilani
Project Mentor, Operating System from Scratch, Fall, 2015
Project Mentor, Intro. to Competitive Coding, Fall, 2014 and Spring, 2015

Skills

C++/C, Java (Android), Python, Cuda, Verilog, PHP & MySQL

Co-curricular

Vice President, ACM Chapter, BITS Pilani Goa Campus
Developer @ Mobile App Club, BITS Pilani Goa Campus

References

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