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Charging Infrastructure

Lecture-34

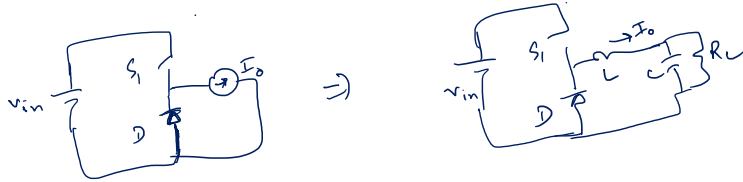
Soft Switching In Half Bridge Configuration

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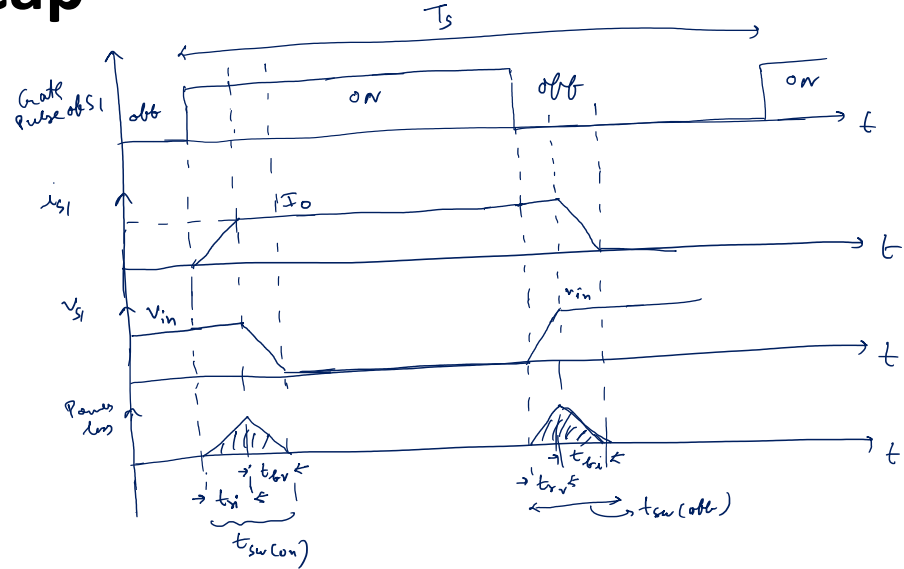


Recap

$$P_{sw} = \frac{V_{in} I_o}{2} (t_{sw(on)} + t_{sw(off)}) f_{sw}$$



- Switching loss depends on
- Switching frequency
 - The blocking voltage
 - The current during switching instant
 - time required for turning-on & turning-off



$$t_{sw(on)} = t_{tri} + t_{brv}$$

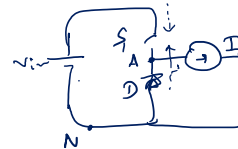
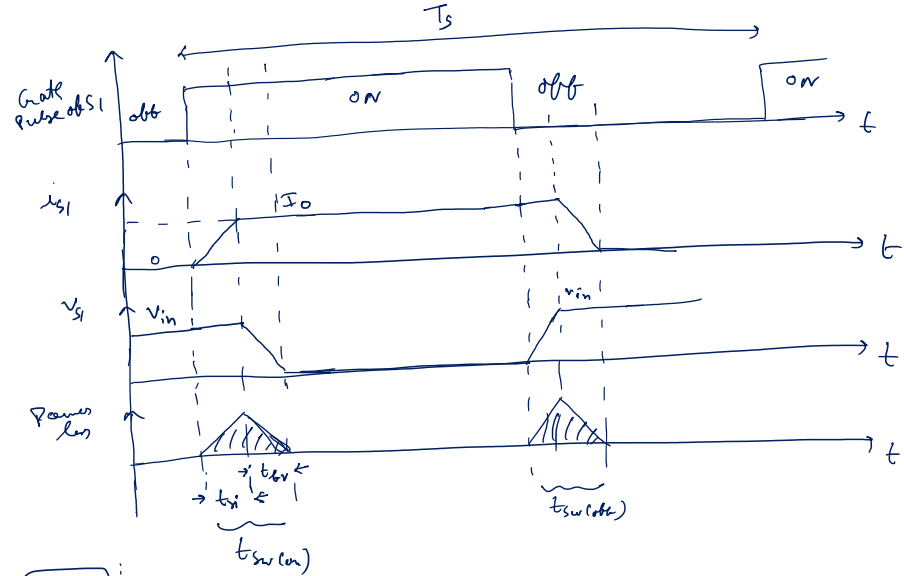
$$t_{sw(off)} = t_{brv} + t_{tri}$$

$$P_{sw} = P_{sw(con)} + P_{sw(off)}$$

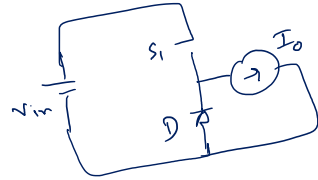
$$P_{sw} = \frac{V_{in} I_o}{2} (t_{sw(con)} + t_{sw(off)}) f_{sw}$$

during $t_{sw(con)}$ & $t_{sw(off)}$ following takes places

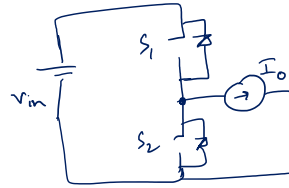
- The loss \rightarrow reduced $\eta \rightarrow$ limits f_{sw}
- $\frac{\Delta V}{\Delta t} \rightarrow (V_{in}) \approx \frac{dv}{dt}, \frac{di}{dt}$
 $\frac{\Delta V}{\Delta t} \rightarrow$ (how fast the switch S_1 is getting ON)
- Electromagnetic interference due to $\frac{dv}{dt}, \frac{di}{dt}$
- high $\frac{dv}{dt}, \frac{di}{dt}$ there are $\frac{dv}{dt}$ & $\frac{di}{dt}$ related problems
- To reduce P_{sw} , the $t_{sw(off)}$ & $t_{sw(con)}$ need to be reduced
 however it leads to higher $\frac{di}{dt}$ & $\frac{dv}{dt}$
- $\frac{dv}{dt} \rightarrow$ false turn-on of the devices
- $\frac{di}{dt} \rightarrow$ oscillation in gate-source voltage



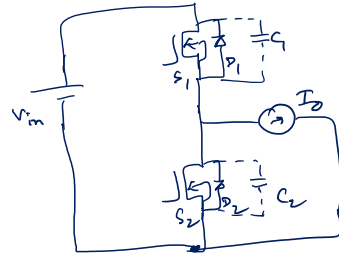
$V_{AN} \rightarrow V_{in}$ voltage will come
 $\rightarrow 0$ to V_{in}



\Rightarrow



\Downarrow



C_1, C_2 are the output capacitance of MOSFETs S_1 & S_2

$$P_{sw} = P_{sw(con)} + P_{sw(off)}$$

$$P_{sw} = \frac{V_{in} I_o}{2} (t_{sw(con)} + t_{sw(off)}) f_{sw}$$

⇒ During turn-on, if somehow we ensure that voltage falls to zero, before current start rising, then the $t_{sw(con)}$ period can be avoided (overlapping of current rise & voltage fall can be avoided).

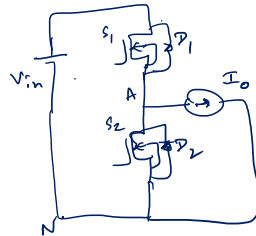
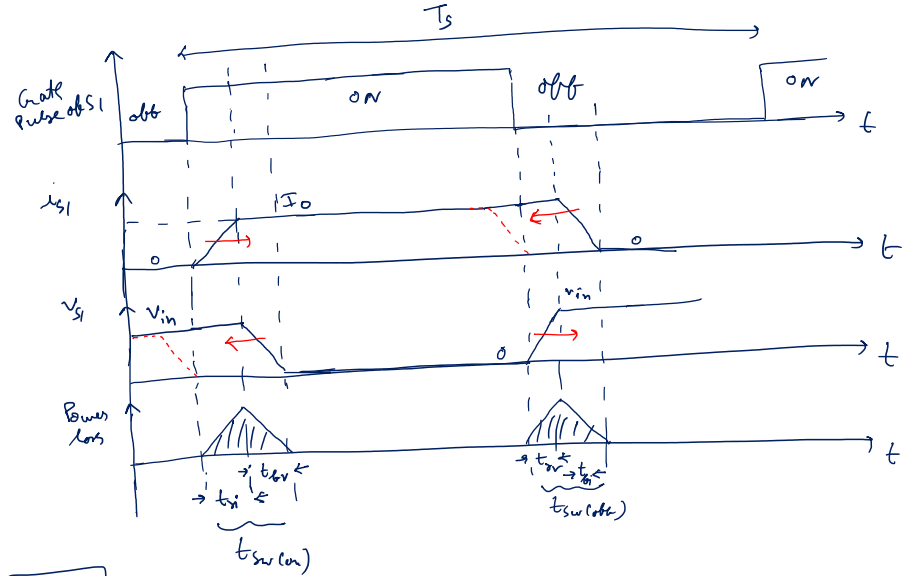
$$\Rightarrow P_{sw(con)} = 0$$

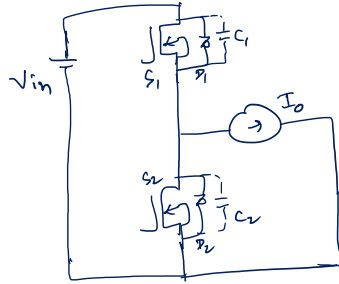
⇒ Zero voltage switching → turn-on

⇒ During turn-off, if somehow we ensure that current goes to zero, before voltage start rising, then the $t_{sw(off)}$ (overlapping period of current fall and voltage rise) can be avoided

$$\Rightarrow P_{sw(off)} = 0$$

⇒ Zero current switching — turn-off





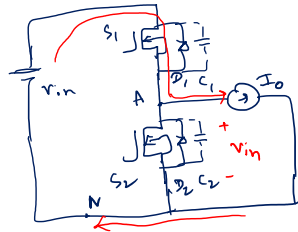
S_1 & S_2 are complementary to each other; and there is deadtime during transition from off to on

$$S_1 = 1, \quad S_2 = 0 \quad \rightarrow \text{deadtime}$$

$$S_1 = 0, \quad S_2 = 1$$

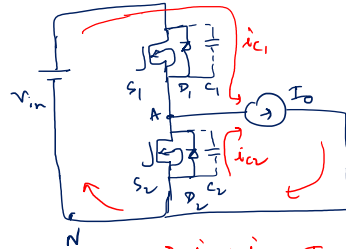
S_1 is turned on ; S_2 is turned on
 S_1 is turned off ; S_2 is turned off

S_1 is turned-off \Rightarrow S_1 goes from ON to off



S_1 is ON
 S_2 is off

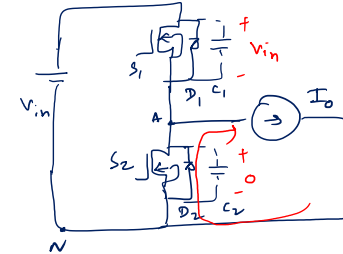
$$V_{AN} = V_{in}$$



deadtime
 S_1 is off & S_2 is off

$\Rightarrow i_{C1} + i_{C2} = I_o$
 C_2 is discharging
 C_1 is charging
 $V_{C2} \downarrow ; V_{C1} \uparrow$
 V_{AN} is reducing

\Rightarrow

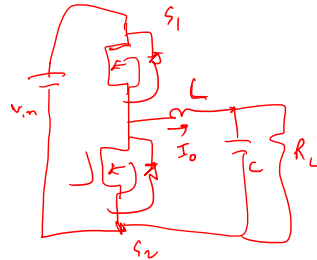
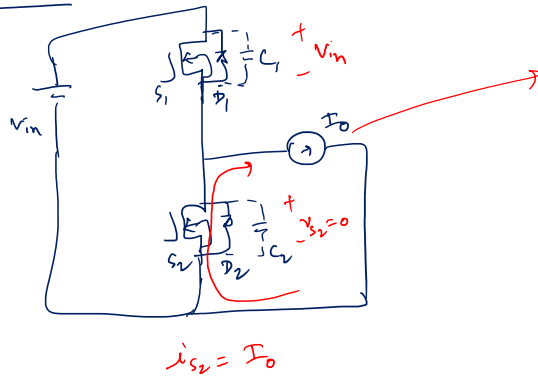


$I_o = i_{D2}$
 $V_{C2} = 0 ; V_{C1} = V_{in}$
 $V_{S2} = 0$

$$V_{AN} = 0$$

$$\Rightarrow \frac{dv}{dt} \text{ is limited} \Rightarrow \frac{dv}{dt} = \frac{I_o}{C_1 + C_2}$$

turning on S_2 (Gate pulse to S_2)



ZVS of Switch S_2
during turn-on of S_2

Solo-switching of S_2

$$\Rightarrow P_{sw(on)} = 0 ; \text{ limited } \frac{dV}{dt} = \frac{I_o}{C_1 C_2}$$

\Rightarrow Sufficient deadtime is provided such that V_{C2} goes to '0', simultaneously V_{C1} goes to $V_{in} \Rightarrow$ required condition

C_1 is charging to V_{in} (from 0) & C_2 is discharging from (V_{in} to 0), thus

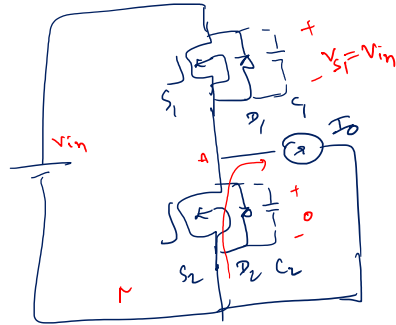
$$\text{Energy in capacitance} = \frac{1}{2} C_1 V_{in}^2 + \frac{1}{2} C_2 V_{in}^2$$

$$\text{Energy associated with } I_o \text{ flowing through inductor } L = \frac{1}{2} L I_o^2$$

\Rightarrow The necessary condition is

$$L I_o^2 > C_1 V_{in}^2 + C_2 V_{in}^2$$

When S_1 is turning on (going from off to on)



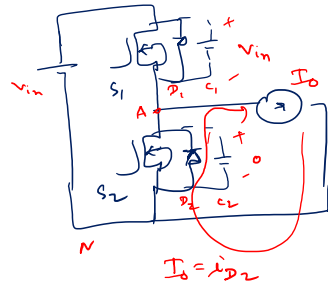
S_1 is off

S_2 is ON

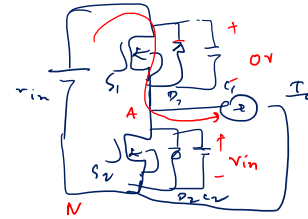
$$I_o = i_{s2}$$

$$V_{AN} = 0$$

\Rightarrow



\Rightarrow



$$I_o = i_{s1}$$

Some non-zero $P_{sw(on)}$

S_1 is ON

S_2 is OFF

$$\Rightarrow V_{AN} = V_{in}$$

S_1 is OFF

S_2 is OFF

deadtime

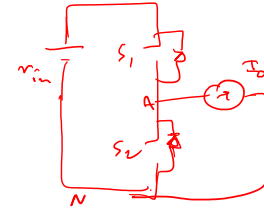
$$V_{AN} = 0$$

\Rightarrow Some non-zero $P_{sw(on)}$

\Rightarrow high $\frac{dv}{dt}$

\Rightarrow hard-switching of S_1

- ⇒ S_1 turns ON with hard-switching
- ⇒ S_2 turns ON with Soft-switching (ZVS)
- ⇒ ZCS is difficult for Voltage source fed half-bridge converter since they have non-zero current coming out of its pole.
- ⇒ ZCS is possible if during operation of circuit I_o goes to zero for eg, DCM, FB converters operation.



Thank You

