Intel Corporation, Programmable Solutions Group

European Regional Application Engineering Team

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Students Interest Group „SNS Delta Power”

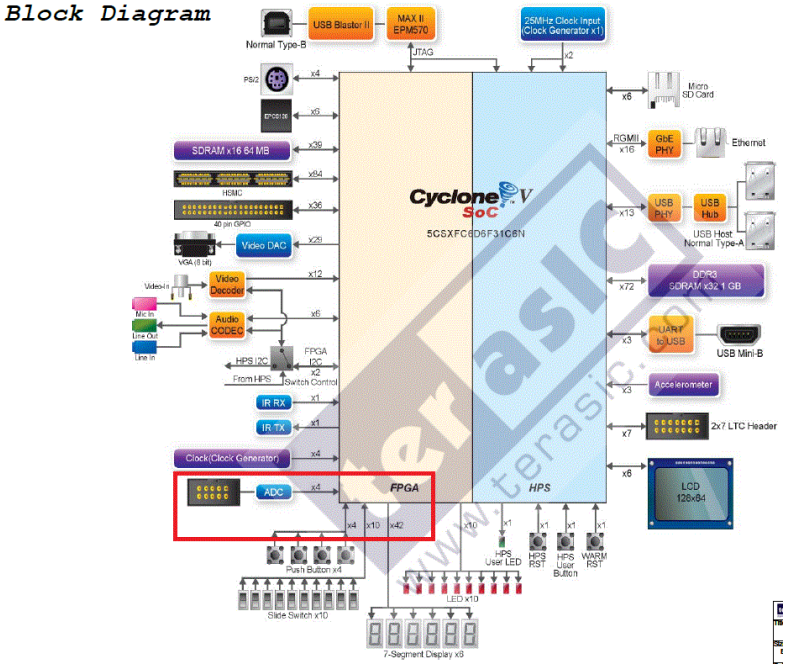
Design Challenge No. 3

Implementation of Digital Voltmeter on Four 7-Segment Displays

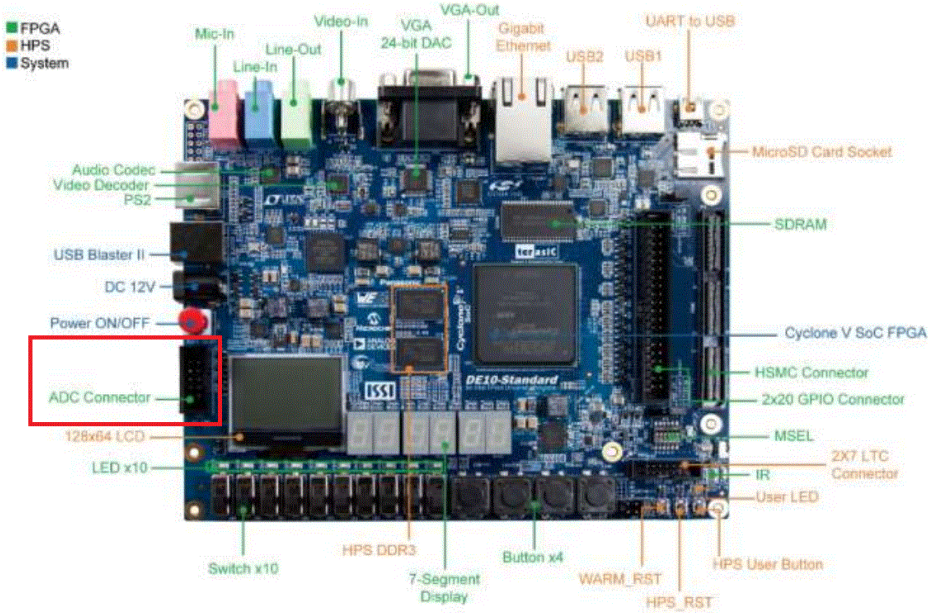
Version 0.1 7/12/2020

Using DE10-Standard development kit, let's implement digital voltmeter covering voltage range 0…+4.096 V. Four conversions should be occurring every one second and result be presented on four 7-segment displays (0…4096 mV).

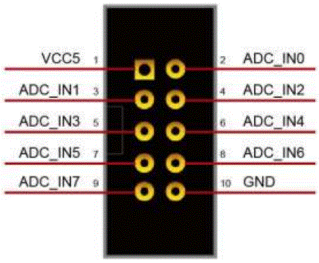
Although Cyclone V SoC FPGA device does not contain integrated analog-digital converter, a high precision one is available externally on the board:



The converter comprises of eight analog input channels, each of them is fed from pin header at left bottom connector of the development kit:



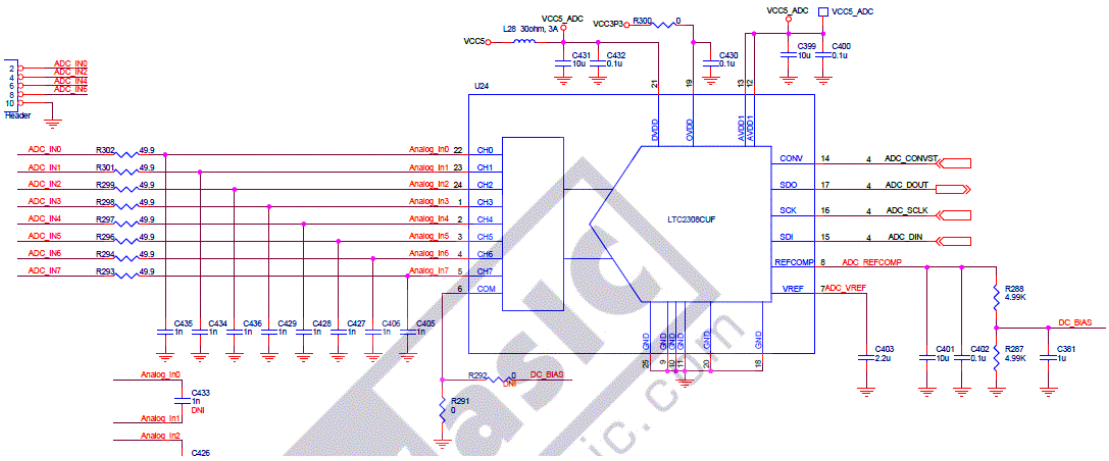
Detailed pinout of the header is shown below. Please be aware of side notch positioning - double check with digital multimeter location of VCC5 pin (5.0 Volts supply).



As on-board external A/D converter LTC2308 can convert voltages up to +4.096V, one or two AA/AAA sized 1.5V batteries should be used as voltage source. Staying within 3.0…3.1V voltage limit will ensure safe operation of the analog-digital converter. Let's use ADC_IN0 input pin for measurements. Negative terminal of battery should be connected to the ground pin GND.

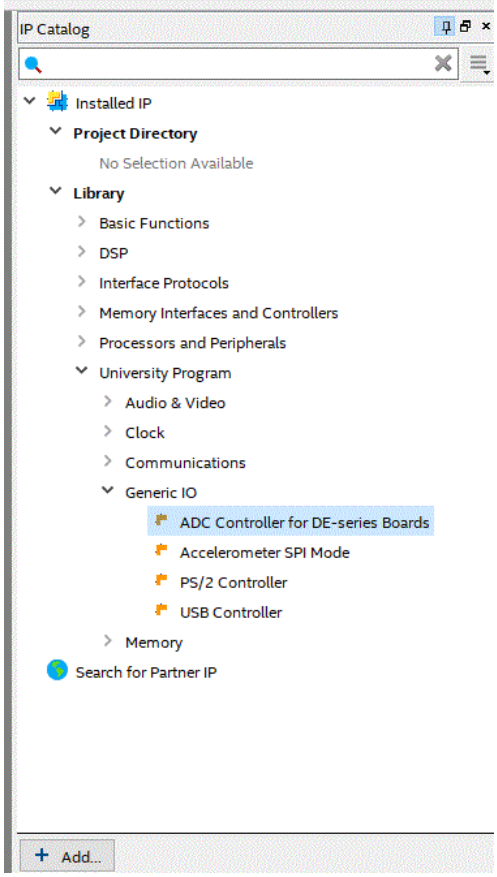
Caution! With winter season approaching, relative air humidity is at all year low of 30-40%. This increases risk of Electrostatic Discharge (ESD) events while working on the development kit. Injection of electrostatic charge (voltage up to 8 kV) can permanently damage sensitive microelectronic components of the DE10-Standard board. Please do not touch electronic components and handle the printed circuit board by metal distance legs attached to its edges. These legs are galvanically connected to ground plane of the board. It would be also wise to avoid wearing synthetic clothing, stay away from carpets and even touch central heating radiator in your room (😊) briefly prior to connecting test batteries to the ADC connector of the board.

Below schematic is an insert from DE10-Standard electrical diagrams document. It shows connectivity of the LTC2308 A/D converter chip. ADC_IN0 channel 0 input voltage is passed on to a first order low-pass RC passive filter – 50 ohm R302 resistor and 1 nF C435 capacitor. Internal multiplexor allows to choose one of eight available inputs for A/D conversion. Supply voltage VCC5_ADC connected to pins 12 and 13 is a low noise 5.0V supply for analog section circuitry of the LTC2308 part. Internal voltage reference VREF of 4.096V is generated from the VCC5_ADC. Pin 7 allows to connect the VREF to external capacitor of 2.2 uF. C403 filters high frequency noise.
Analog-digital converter's resolution is 12 bits. This means 2^12=4,096 quantization levels between 0 and 4.096V. In other words, 1LSB (least significant bit) step is equal 4.096V/2^12=1mV/LSB.
LTC2308 chip communicates with Cyclone V FPGA device via three wire serial port compatible with SPI (Serial Port Interface) specification. The wires are: SCK clock, SDI data input and SDO data output. Additional input to the A/D converter is conversion start CONV.



Detailed description of SPI communication is available in datasheet of the LTC2308 device. There is no need to design SPI master interface inside FPGA as readily available IP Core can be used from within Quartus Lite software suite.

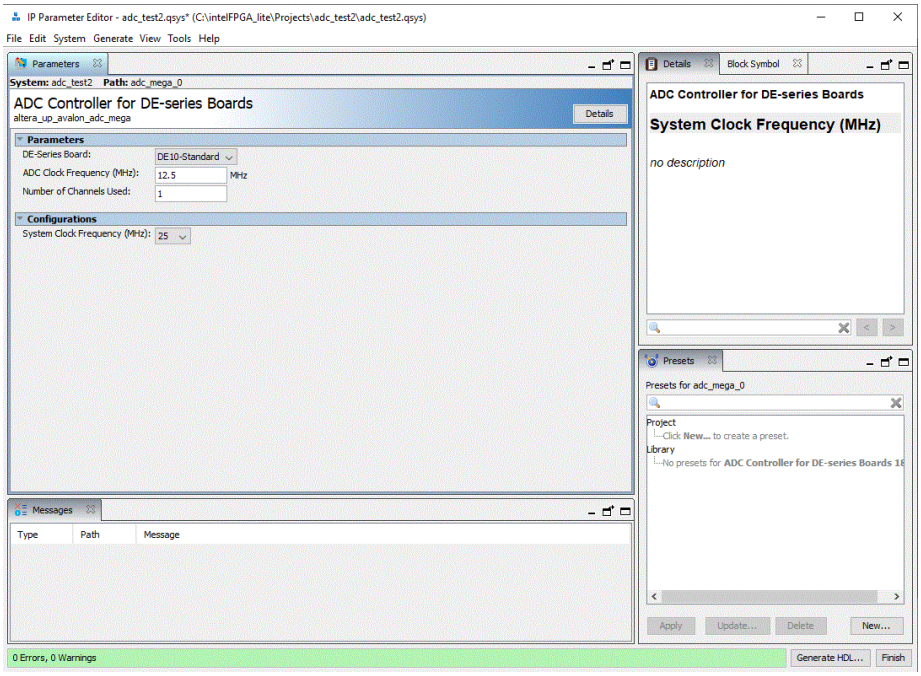
After new project creation in Quartus 20.1 Lite, please go to IP Catalog -> Installed IP ->Library -> University Program -> Generic IO -> ADC Controller for DE-series Boards:



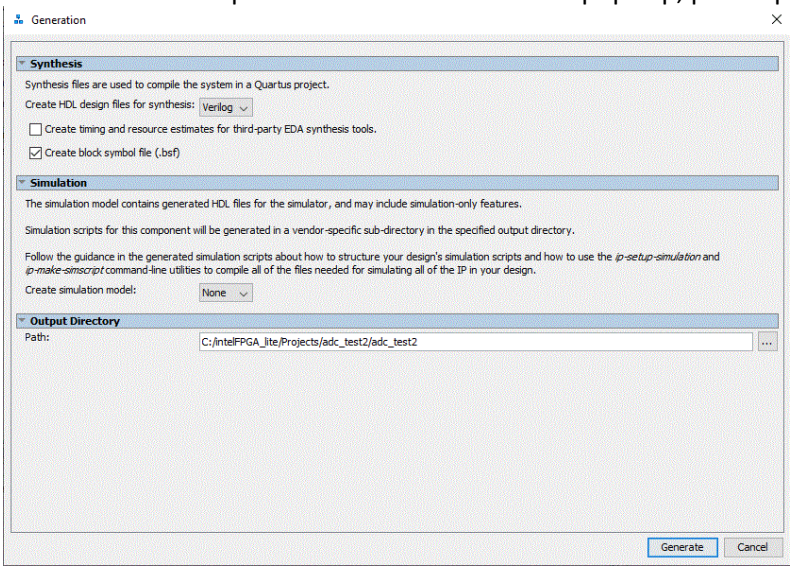
Upon double click, IP Parameter Editor opens. We can set:

- ADC Clock Frequency 12.5 MHz. This is the SCK clock speed on the SPI interface

- Number of Channels Used 1. Only one of eight available analog inputs will be used for measurements
- System Clock Frequency 25 MHz. Defines speed of internal clock that runs the entire ADC Controller IP Core



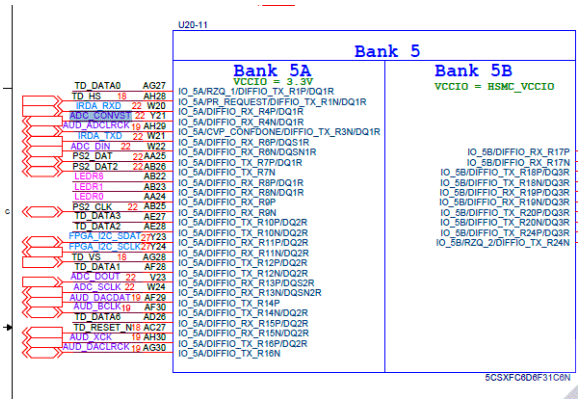
Then “Generate HDL…” button can be pressed. Generation window pops up, please press “Generate”:



Three files get generated:

1) adc_test2.v is top-level module of the controller. Pinout of the IP Core:

Port	Direction	Description
CLOCK	Input	Core clock of 25 MHz, to be sourced from PLL
RESET	Input	Core reset, to be sourced from PLL's locked output (invert)
ADC_SCLK	Output	SPI port clock, goes to A/D converter
ADC_CS_N	Output	Conversion start pulse, goes to A/D converter
ADC_DIN	Output	SPI data out, goes to A/D converter
ADC_DOUT	Input	SPI data input, comes from A/D converter (serialized conversion result)
CH0[11:0]	Output	Channel 0 conversion result, parallel data



Ports ADC_SCLK, ADC_CS_N, ADC_DIN and ADC_DOUT should be mapped to FPGA pins W24, Y21, W22 and V23 respectively. Please remember to choose correct voltage domain to adhere with the A/D converter chip's requirements. Output bus CH0[11:0] is channel 0 voltage conversion result. This 12-bit BCD data should be encoded into four 7-segment displays. Please remember to register the encoders outputs prior to sending data to FPGA output pins.

2) Submodule adc_test2_adc_mega_0.v . This file contains parameters that define exact implementation of the ADC Controller IP. It also nests the actual SPI controller submodule altera_up_avalon_adv_adc. "always @ (posedge CLOCK)" statement implements a free-running conversion scheme around the A/D converter. Upon receiving "done" flag from the SPI controller, a "go" pulse is generated to initiate next conversion. IP Core logic runs the A/D converter close to its maximum speed of 500 kilosamples per second. As we want to present only 4 samples every one second, there is no need to use this handshaking scheme. "done" flag is not needed and "go" pulse should be generated from additional BCD counter (frequency divider).
3) Altera_up_avalon_adv_adc.v . This file contains the main Finite State Machine logic that realizes the SPI controller for A/D converter slave and de-serializes conversion results. It doesn't require any modifications.

Bonus Task: please try to implement "Hold and Average" function on the digital voltmeter. Upon pressing Hold microswitch, seven segment displays should freeze with the latest measurement result. Frozen value should be then loaded into memory buffer (reg statement) and normal display operation resumed after pressing another microswitch labeled as Release. After using Hold button four times, average voltage should be displayed.

Hint: You can use one 14-bit register and 14x12 bits adder to realize adder-accumulator block. Upon four accumulations, average value can be simply calculated as division by 4. As binary arithmetic is used, this is achievable as shift right by two positions.

Should you needed any more information or required some support, please don't hesitate to contact us.

Good luck! 😉
Regional FPGA Applications Team, Intel/Gdańsk

References:

(1) "Altera Cyclone V SoC Development & Education Board (DE10-Standard)", development kit board electrical diagrams: https://rocketboards.org/foswiki/pub/Documentation/DE10Standard/DE10-Standard_Schematic.pdf
(2) "Linear Technology LTC2308 Low Noise, 500ksps, 8-Channel, 12-Bit ADC", on-board analog-to-digital converter datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/2308fc.pdf
(3) "DE10-Standard User Manual": https://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=1081&FID=551f9fbfa8ed07843cd51831db1b04dd